

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

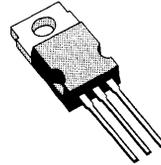
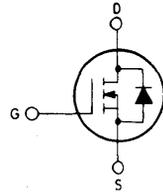
TYPE	V _{DSS}	R _{DS(on)}	I _D
SGSP351	100 V	0.6 Ω	6 A

- HIGH SPEED SWITCHING APPLICATIONS
- DC/DC APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROL

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include stepper motor and printer hammer drives and switching power supplies


TO-220
**INTERNAL SCHEMATIC
DIAGRAM**

ABSOLUTE MAXIMUM RATINGS

V _{DS}	Drain-source voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain-gate voltage (R _{GS} = 20 KΩ)	100	V
V _{GS}	Gate-source voltage	± 20	V
I _D	Drain current (cont.) at T _c = 25°C	6	A
I _D	Drain current (cont.) at T _c = 100°C	4	A
I _{DM} (*)	Drain current (pulsed)	24	A
I _{DLM} (*)	Drain inductive current, clamped	24	A
P _{tot}	Total dissipation at T _c < 25°C	50	W
	Derating factor	0.4	W/°C
T _{stg}	Storage temperature	- 65 to 150	°C
T _j	Max. operating junction temperature	150	°C

(*) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj - case}$	Thermal resistance junction-case	max	2.5	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
------------	-----------------	------	------	------	------

OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$	$V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$				250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$				± 100	nA

ON (*)

$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $V_{GS} = 10 \text{ V}$	$I_D = 3 \text{ A}$ $I_D = 3 \text{ A}$			0.6 1.2	Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 \text{ V}$	$I_D = 3 \text{ A}$	1			mho
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$	$f = 1 \text{ MHz}$		180	250	pF
C_{oss}	Output capacitance					100	pF
C_{rss}	Reverse transfer capacitance					40	pF

SWITCHING

$t_d(on)$	Turn-on time	$V_{DD} = 50 \text{ V}$	$I_D = 3 \text{ A}$		10	15	ns
t_r	Rise time	$V_I = 10 \text{ V}$	$R_I = 4.7 \Omega$		25	35	ns
$t_d(off)$	Turn-off delay time	(see test circuit)			25	35	ns
t_f	Fall time				15	20	ns

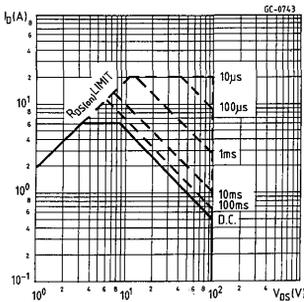
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} Source-drain current				6	A
$I_{SDM} (*)$ Source-drain current (pulsed)				24	A
V_{SD} Forward on voltage	$I_{SD} = 6\text{ A}$ $V_{GS} = 0$			1.35	V
t_{rr} Reverse recovery time	$I_{SD} = 6\text{ A}$ $V_{GS} = 0$ $di/dt = 25\text{ A}/\mu\text{s}$		120		ns

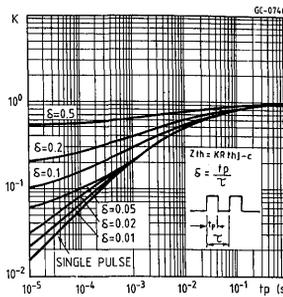
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

(*) Pulse width limited by safe operating area

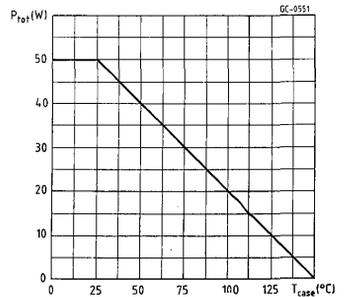
Safe operating areas



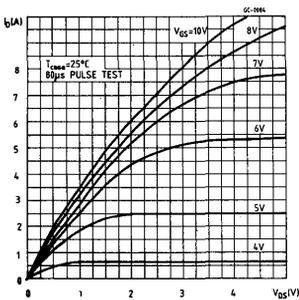
Thermal impedance



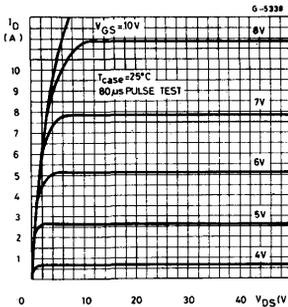
Derating curve



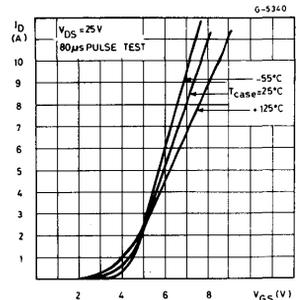
Output characteristics



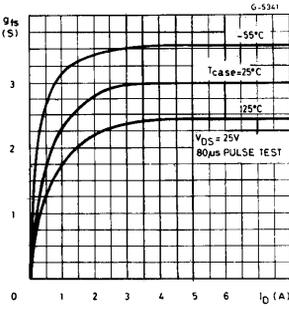
Output characteristics



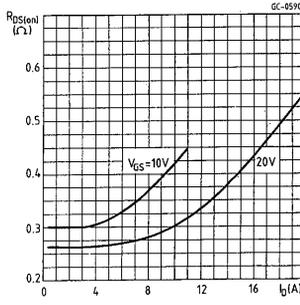
Transfer characteristics



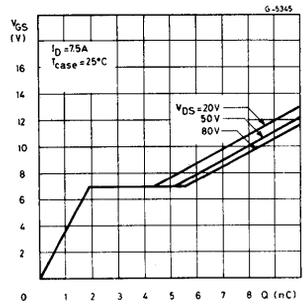
Transconductance



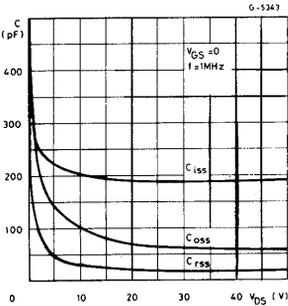
Static drain-source on resistance



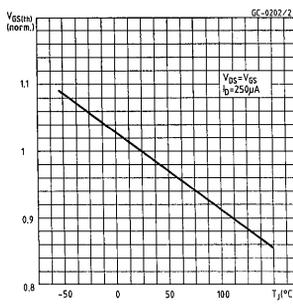
Gate charge vs gate-source voltage



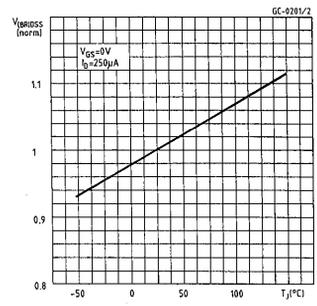
Capacitance variation



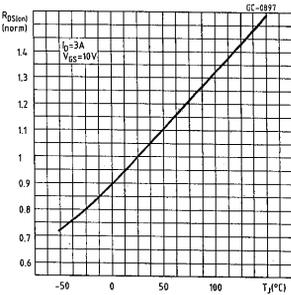
Normalized gate threshold voltage vs temperature



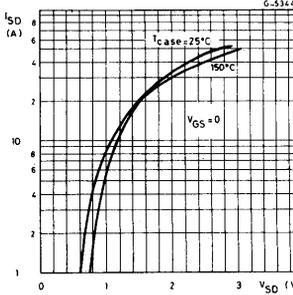
Normalized breakdown voltage vs temperature



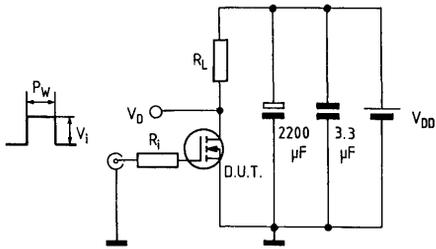
Normalized on resistance vs temperature



Source-drain diode forward characteristics

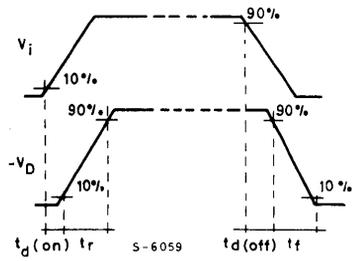


Switching times test circuit for resistive load

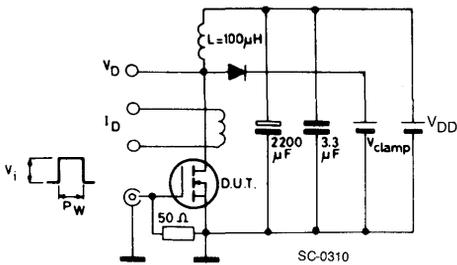


Pulse width $\leq 100 \mu\text{s}$
 Duty cycle $\leq 2\%$

Switching time waveforms for resistive load

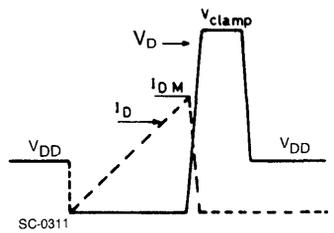


Clamped inductive load test circuit

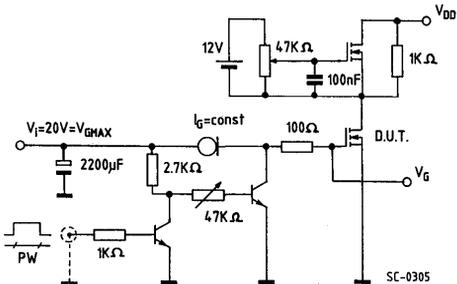


$V_i = 12 \text{ V}$ - Pulse width: adjusted to obtain specified I_{DM} , $V_{\text{clamp}} = 0.75 V_{(BR)}$ DSS.

Clamped inductive waveforms



Gate charge test circuit



$V_i = 20\text{V} = V_{GMAX}$
 $I_G = \text{const}$
 PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit

