

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

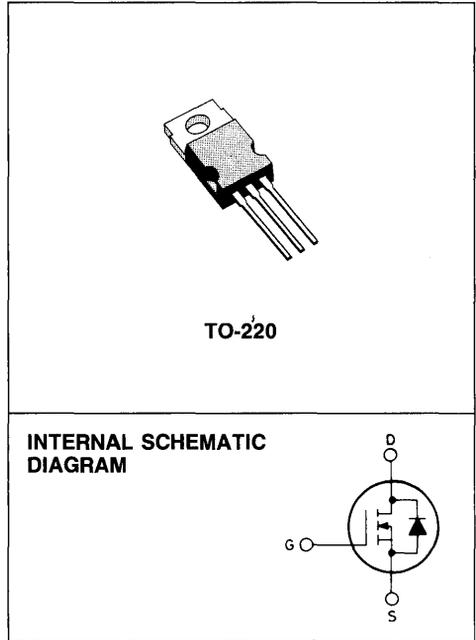
TYPE	V _{DSS}	R _{DS(on)}	I _D
SGSP361	100 V	0.15 Ω	18 A
SGSP362	80 V	0.1 Ω	22 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR UPS APPLICATIONS
- ULTRA FAST SWITCHING
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ♦
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include UPS, battery chargers, printer hammer drivers, solenoid drivers and motor control.



ABSOLUTE MAXIMUM RATINGS

	SGSP361	SGSP362	
V _{DS}	100	80	V
V _{DGR}	100	80	V
V _{GS}		±20	V
I _D	18	22	A
I _D	11	14	A
I _{DM} (*)	72	88	A
P _{tot}		100	W
		0.8	W/°C
T _{stg}	-65 to 150		°C
T _j	150		°C

(*) Pulse width limited by safe operating area
 ♦ Introduced in 1988 week 44

THERMAL DATA

$R_{thj - case}$	Thermal resistance junction-case	max	1.25	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A$ for SGSP361 for SGSP362	$V_{GS} = 0$	100 80		V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^{\circ}C$		250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 100	nA

ON (*)

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu A$	2		4	V
$R_{DS (on)}$	Static drain-source on resistance	$V_{GS} = 10 V$ $I_D = 9 A$ for SGSP361 $I_D = 11 A$ for SGSP362 $V_{GS} = 10 V$ $I_D = 9 A$ for SGSP361 $I_D = 11 A$ for SGSP362	$T_c = 100^{\circ}C$			0.15 0.1 0.3 0.2	Ω Ω Ω Ω

ENERGY TEST

I_{UIS}	Unclamped inductive switching current (single pulse)	$V_{DD} = 30 V$ starting $T_j = 25^{\circ}C$ for SGSP361 for SGSP362	$L = 100 \mu H$	18 22			A A
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DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 V$	$I_D = 9 A$	4.5			mho
C_{iss}	Input capacitance	$V_{DS} = 25 V$	$f = 1 MHz$		950	1200	pF
C_{oss}	Output capacitance	$V_{GS} = 0$				480	pF
C_{rss}	Reverse transfer capacitance					230	pF

ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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SWITCHING

$t_{d(on)}$	Turn-on time	$V_{DD} = 50\text{ V}$ $I_D = 11\text{ A}$ $V_i = 10\text{ V}$ $R_i = 4.7\ \Omega$ (see test circuit)		20	30	ns
t_r	Rise time			50	65	ns
$t_{d(off)}$	Turn-off delay time			65	85	ns
t_f	Fall time			25	35	ns

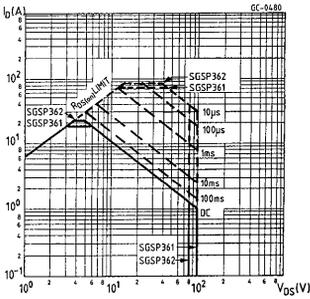
SOURCE DRAIN DIODE

I_{SD}	Source-drain current	for SGSP361			18	A
		for SGSP362			22	A
$I_{SDM} (*)$	Source-drain current (pulsed)	for SGSP361			72	A
		for SGSP362			88	A
V_{SD}	Forward on voltage	$V_{GS} = 0$				
		$I_{SD} = 18\text{ A}$ for SGSP361			1.35	V
		$I_{SD} = 22\text{ A}$ for SGSP362			1.35	V
t_{rr}	Reverse recovery time	$I_{SD} = 22\text{ A}$	$V_{GS} = 0$		180	ns
		$di/dt = 25\text{ A}/\mu\text{s}$				

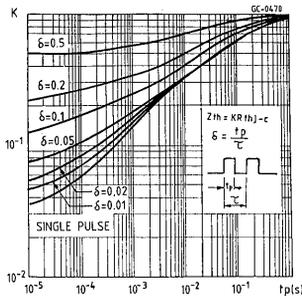
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

(*) Pulse width limited by safe operating area

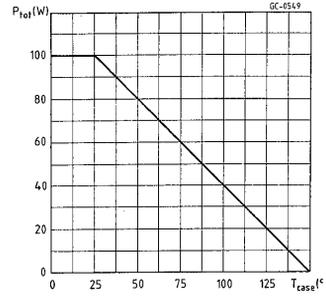
Safe operating areas



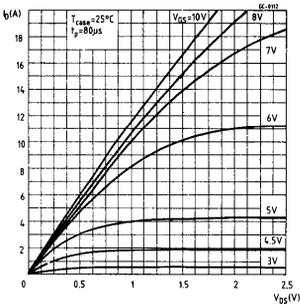
Thermal impedance



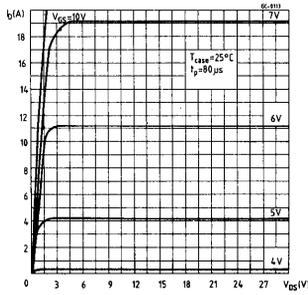
Derating curve



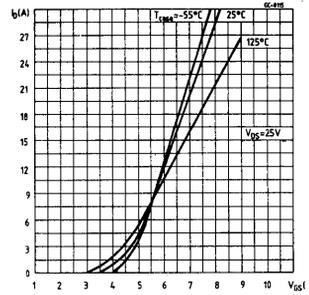
Output characteristics



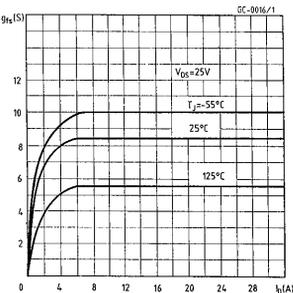
Output characteristics



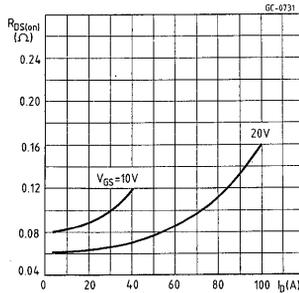
Transfer characteristics



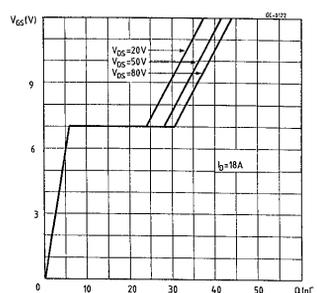
Transconductance



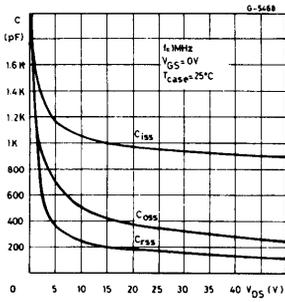
Static drain-source on resistance



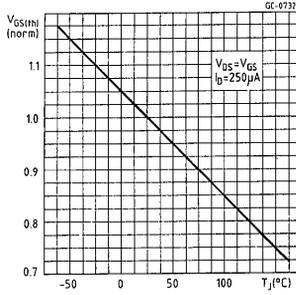
Gate charge vs gate-source voltage



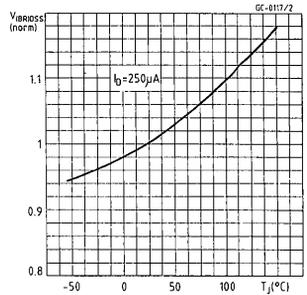
Capacitance variation



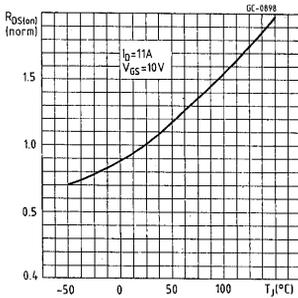
Normalized gate threshold voltage vs temperature



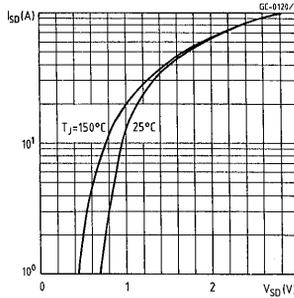
Normalized breakdown voltage vs temperature



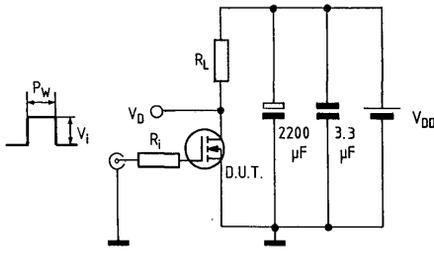
Normalized on resistance vs temperature



Source-drain diode forward characteristics

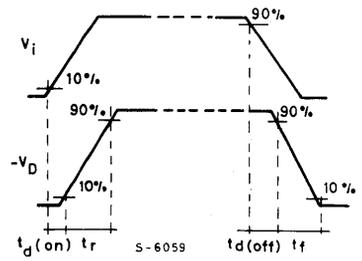


Switching times test circuit for resistive load

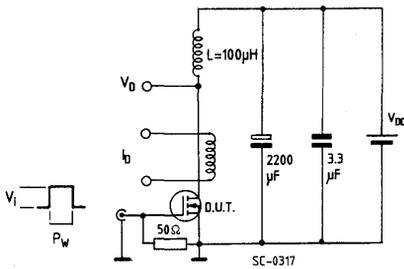


Pulse width $\leq 100 \mu\text{s}$
Duty cycle $\leq 2\%$

Switching time waveforms for resistive load

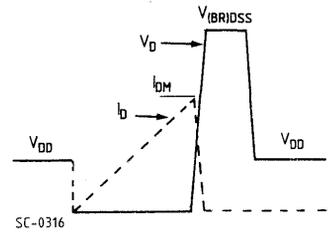


Unclamped inductive load test circuit

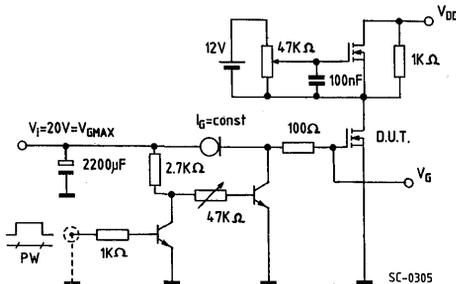


$V_i = 12 \text{ V}$ - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit

