SGS-THOMSON
MICROELECTRONICS

SGSP364
SGSP369

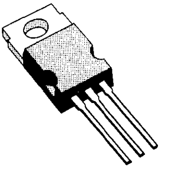
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP364	450 V	1.5 Ω	5 A
SGSP369	500 V	1.5 Ω	5 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - FOR ELECTRONIC LAMP BALLAST
- ULTRA FAST SWITCHING
- EASY DRIVE - REDUCED COST AND SIZE

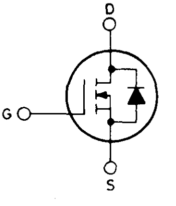
INDUSTRIAL APPLICATIONS:
- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC switch, constant current source, ultrasonic equipment and electronic ballast for fluorescent lamps.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		SGSP364	SGSP369	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	450	500	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	450	500	V
V_{GS}	Gate-source voltage	± 20		V
I_D	Drain current (cont.) at $T_c=25°C$	5		A
I_D	Drain current (cont.) at $T_c=100°C$	3		A
I_{DM} (•)	Drain current (pulsed)	20		A
I_{DLM} (•)	Drain inductive current, clamped	20		A
P_{tot}	Total dissipation at $T_c<25°C$	100		W
	Derating factor	0.8		W/°C
T_{stg}	Storage temperature	– 65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max	1.25	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25°C$ unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\,DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$ for **SGSP364** for **SGSP369**	 450 500			 V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} =$ Max Rating $V_{DS} =$ Max Rating x 0.8 $T_c = 125°C$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V			±100	nA
ON (*)						
$V_{GS\,(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$R_{DS\,(on)}$	Static drain-source on resistance	$V_{GS} = 10$ V $I_D = 2.5$ A $V_{GS} = 10$ V $I_D = 2.5$ A $T_c = 100°C$			1.5 3	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	$V_{DS} = 25$ V $I_D = 2.5$ A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$		780	1000 200 130	pF pF pF
SWITCHING						
$t_{d\,(on)}$ t_r $t_{d\,(off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	$V_{DD} = 250$ V $I_D = 2.5$ A $V_i = 10$ V $R_i = 4.7\ \Omega$ (see test circuit)		20 30 85 25	30 40 110 35	ns ns ns ns

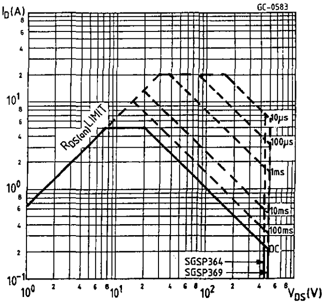
ELECTRICAL CHARACTERISTICS (Continued)

SOURCE DRAIN DIODE

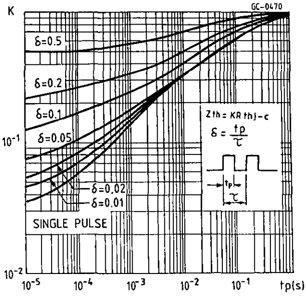
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)				5 20	A A
V_{SD}	Forward on voltage	I_{SD} = 5 A V_{GS} = 0			1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A V_{GS} = 0 di/dt = 100 A/μs		470		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

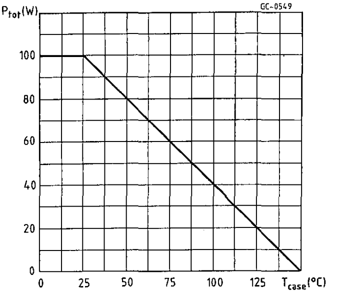
Safe operating areas



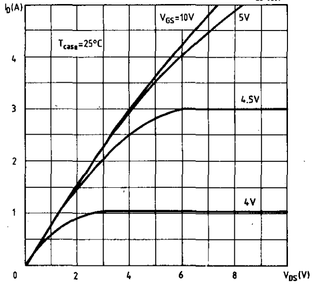
Thermal impedance



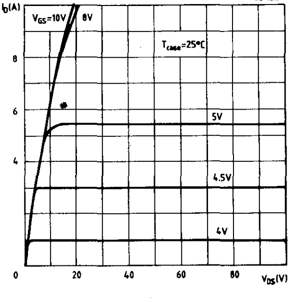
Derating curve



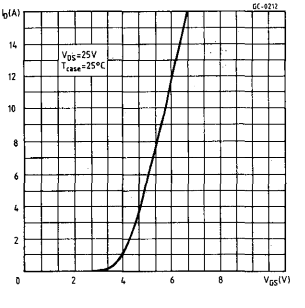
Output characteristics



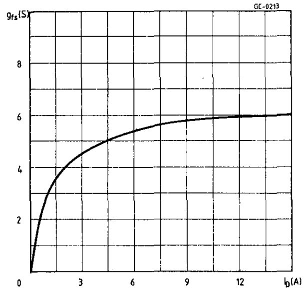
Output characteristics



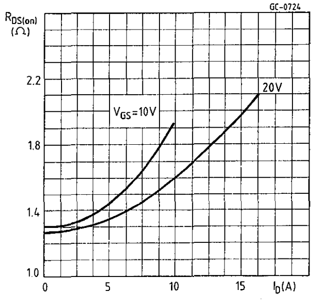
Transfer characteristics



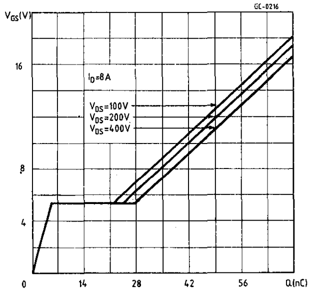
Transconductance



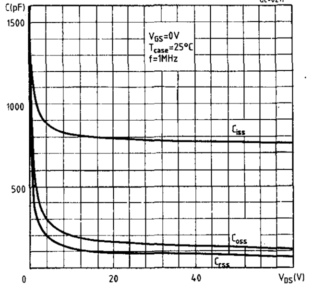
Static drain-source on resistance



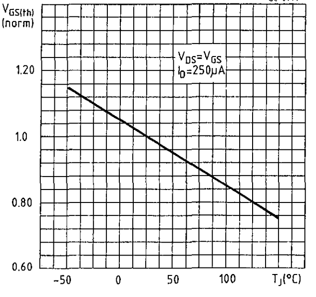
Gate charge vs gate-source voltage



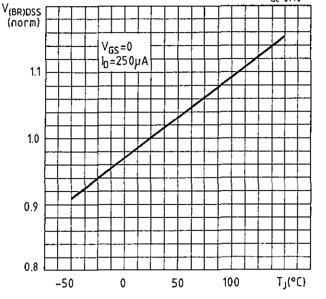
Capacitance variation



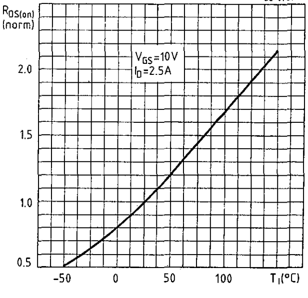
Normalized gate threshold voltage vs temperature



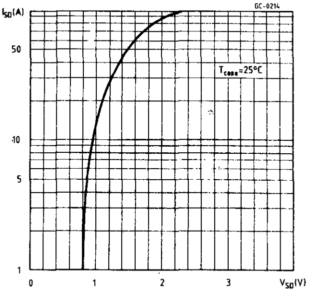
Normalized breakdown voltage vs temperature



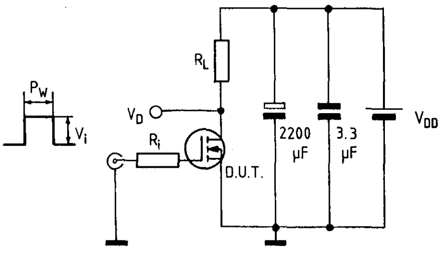
Normalized on resistance vs temperature



Source-drain diode forward characteristics

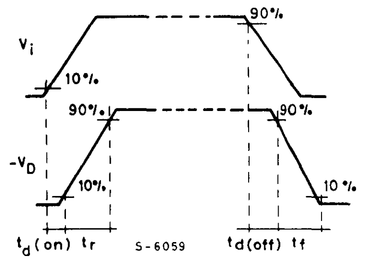


Switching times test circuit for resistive load

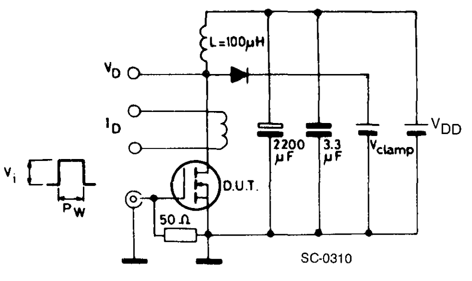


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

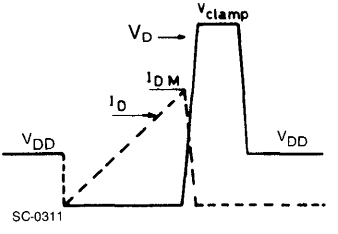


Clamped inductive load test circuit

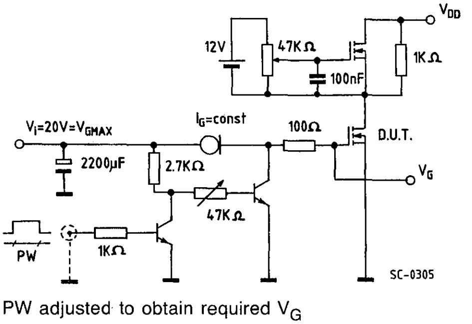


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit