SGS-THOMSON MICROELECTRONICS

SGSP461 SGSP462

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

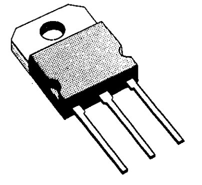
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP461	100 V	0.15 Ω	20 A
SGSP462	80 V	0.1 Ω	25 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR UPS APPLICATIONS
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ♦
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

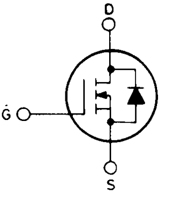
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical applications include UPS, battery chargers, printer hammer drivers, solenoid drivers and motor control.



TO-218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP461	SGSP462	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	80	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	20	25	A
I_D	Drain current (cont.) at $T_c=100°C$	13	16	A
I_{DM} (•)	Drain current (pulsed)	80	100	A
P_{tot}	Total dissipation at $T_c<25°C$	125		W
	Derating factor	1		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
♦ Introduced in 1988 week 44

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit

OFF

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$ Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP461** for **SGSP462**	 100 80			 V V
I_{DSS} Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS} Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA

ON (*)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$ Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS(on)}$ Static drain-source on resistance	V_{GS} = 10 V I_D = 10 A for **SGSP461** I_D = 12.5 A for **SGSP462** V_{GS} = 10 V T_c = 100°C I_D = 10 A for **SGSP461** I_D = 12.5 A for **SGSP462**			 0.15 0.1 0.3 0.2	 Ω Ω Ω Ω

ENERGY TEST

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
I_{UIS} Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP461** for **SGSP462**	 20 25			 A A

DYNAMIC

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} Forward transconductance	V_{DS} = 25 V I_D = 12.5 A	4.5			mho
C_{iss} Input capacitance C_{oss} Output capacitance C_{rss} Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		950	1200 480 230	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit

SWITCHING

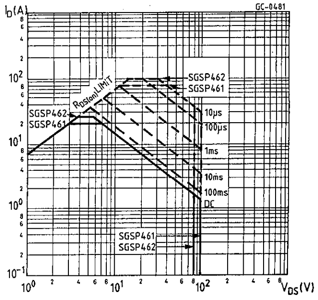
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$t_{d\ (on)}$	Turn-on time	V_{DD} = 50 V I_D = 12.5 A		20	30	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		60	80	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		65	85	ns
t_f	Fall time			25	35	ns

SOURCE DRAIN DIODE

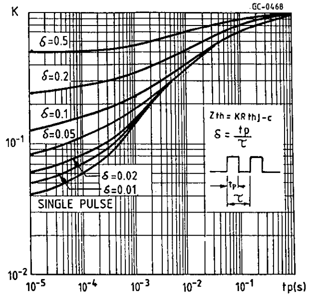
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	for **SGSP461**			20	A
		for **SGSP462**			25	A
I_{SDM} (•)	Source-drain current (pulsed)	for **SGSP461**			80	A
		for **SGSP462**			100	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 20 A for **SGSP461**			1.35	V
		I_{SD} = 25 A for **SGSP462**			1.35	V
t_{rr}	Reverse recovery time	I_{SD} = 25 A V_{GS} = 0 di/dt = 25 A/μs		190		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

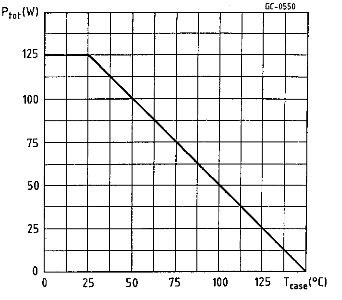
Safe operating areas



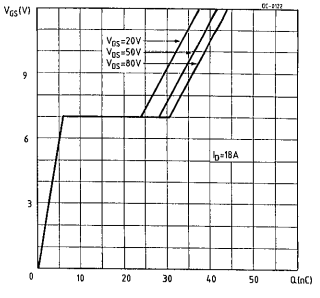
Thermal impedance



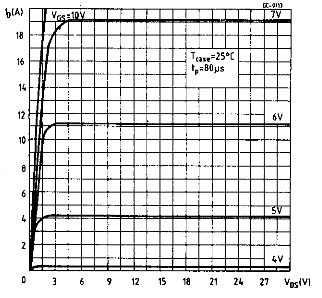
Derating curve



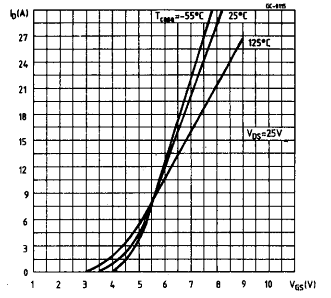
Output characteristics



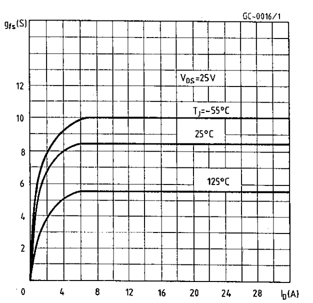
Output characteristics



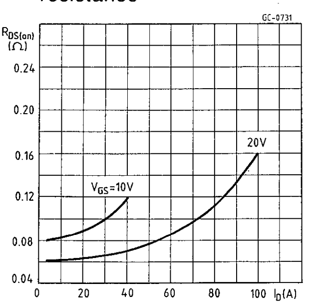
Transfer characteristics



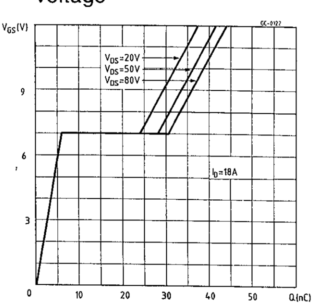
Transconductance



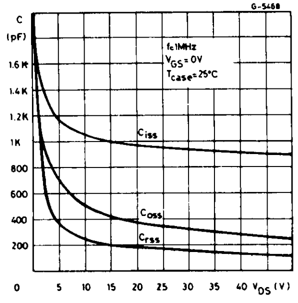
Static drain-source on resistance



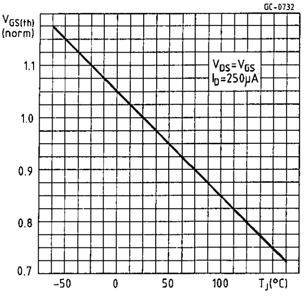
Gate charge vs gate-source voltage



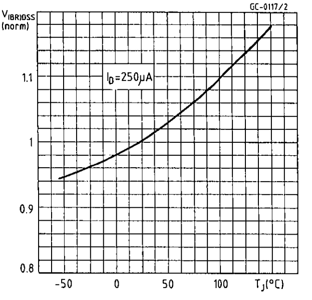
Capacitance variation



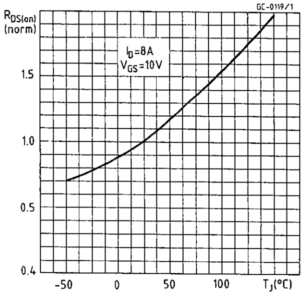
Normalized gate threshold voltage vs temperature



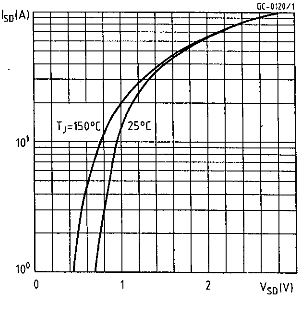
Normalized breakdown voltage vs temperature



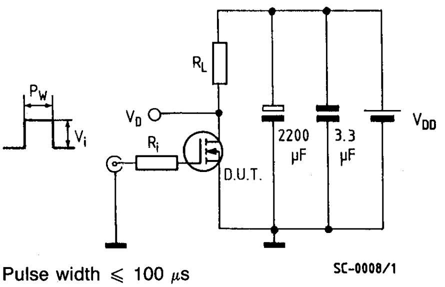
Normalized on resistance vs temperature



Source-drain diode forward characteristics

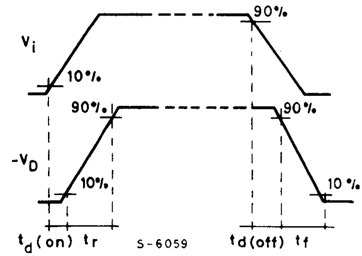


Switching times test circuit for resistive load

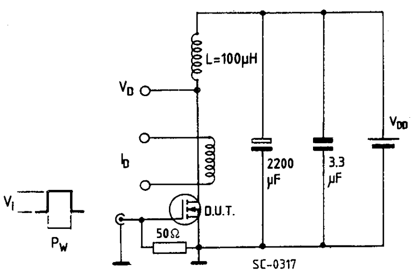


Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

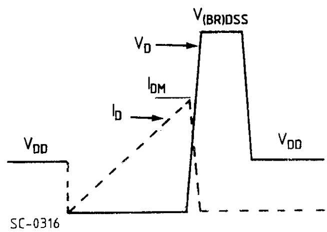


Unclamped inductive load test circuit

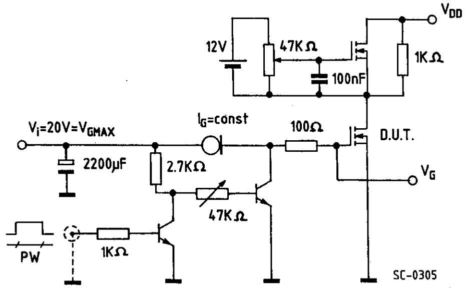


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit