



**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTORS**

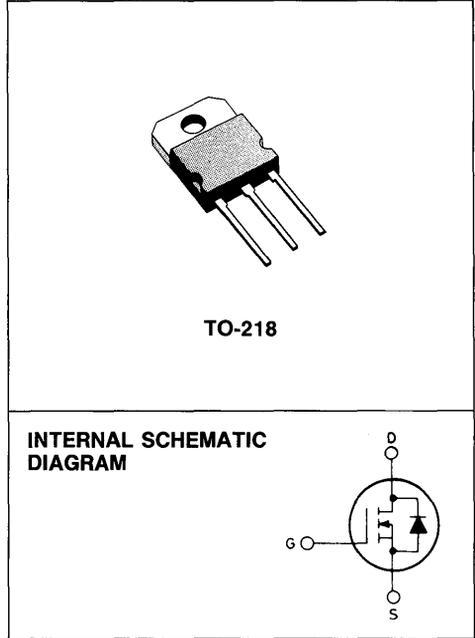
TYPE	V _{DSS}	R _{DS(on)}	I _D
SGSP491	60 V	0.033 Ω	40 A
SGSP492	50 V	0.033 Ω	40 A

- HIGH SPEED SWITCHING APPLICATIONS
- 50 - 60 VOLTS FOR INVERTER AND UPS
- HIGH CURRENT - V_{DS(on)} ≤ 1V at 20A
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ♦
- EASY DRIVE - REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

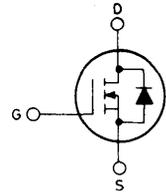
- DC/DC CONVERTERS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications such as DC/DC converters, UPS, inverters, battery chargers and solar power converters.



TO-218

**INTERNAL SCHEMATIC
DIAGRAM**



ABSOLUTE MAXIMUM RATINGS

	SGSP491	SGSP492	
V _{DS}	60	50	V
V _{DGR}	60	50	V
V _{GS}		±20	V
I _D	40		A
I _D	25		A
I _{DM} (*)	160		A
P _{tot}	150		W
	1.2		W/°C
T _{stg}	-65 to 150		°C
T _j	150		°C

(*) Pulse width limited by safe operating area

♦ Introduced in 1988 week 44

THERMAL DATA

$R_{thj - case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ for SGSP491 for SGSP492	$V_{GS} = 0$	60 50		V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^\circ\text{C}$		250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 100	nA

ON (*)

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$R_{DS (on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ $V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}$ $I_D = 20 \text{ A}$			33 66	$\text{m}\Omega$ $\text{m}\Omega$

ENERGY TEST

I_{UIS}	Unclamped inductive switching current (single pulse)	$V_{DD} = 30 \text{ V}$ starting $T_j = 25^\circ\text{C}$	$L = 100 \mu\text{H}$	40			A
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DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 \text{ V}$	$I_D = 20 \text{ A}$	10			mho	
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$	$f = 1 \text{ MHz}$		1900	2800	pF	
C_{oss}	Output capacitance					1500		pF
C_{rss}	Reverse transfer capacitance					850		pF

SWITCHING

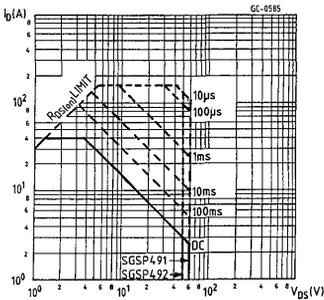
$t_{d (on)}$	Turn-on time	$V_{DD} = 25 \text{ V}$ $V_i = 10 \text{ V}$	$I_D = 20 \text{ A}$ $R_i = 4.7 \Omega$		35	45	ns
t_r	Rise time				110	145	ns
$t_{d (off)}$	Turn-off delay time	(see test circuit)			90	120	ns
t_f	Fall time				55	70	ns

ELECTRICAL CHARACTERISTICS (Continued)

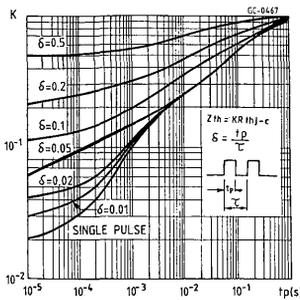
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (*)	Source-drain current Source-drain current (pulsed)			40 160	A A
V_{SD}	Forward on voltage	$I_{SD} = 40\text{ A}$	$V_{GS} = 0$	1.4	V
t_{rr}	Reverse recovery time	$I_{SD} = 40\text{ A}$ $di/dt = 25\text{ A}/\mu\text{s}$	$V_{GS} = 0$	140	ns

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%
 (*) Pulse width limited by safe operating area

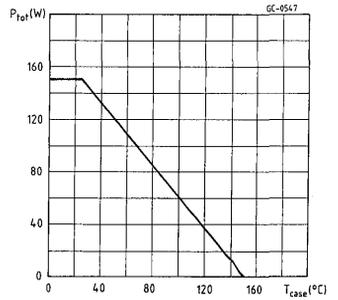
Safe operating areas



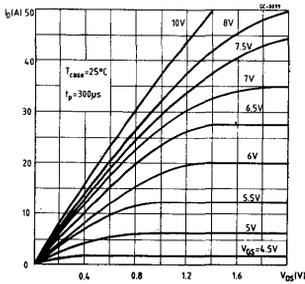
Thermal impedance



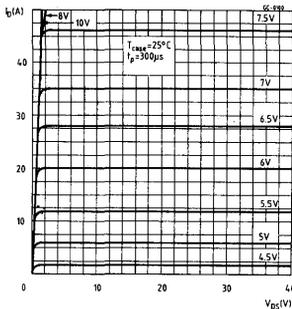
Derating curve



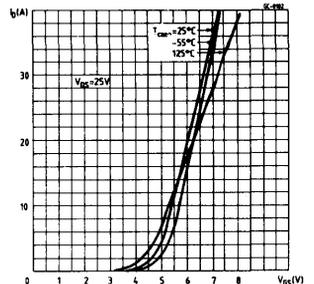
Output characteristics



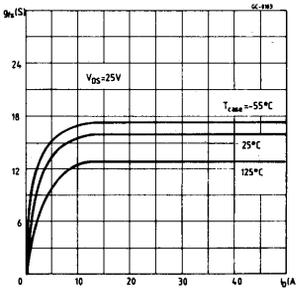
Output characteristics



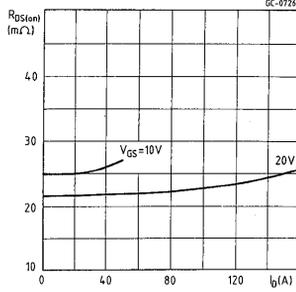
Transfer characteristics



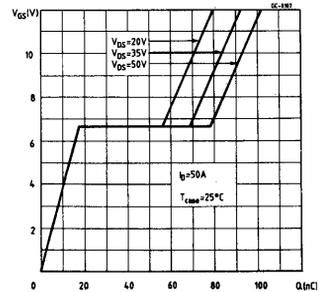
Transconductance



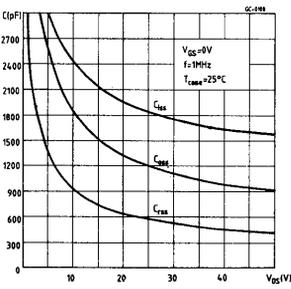
Static drain-source on resistance



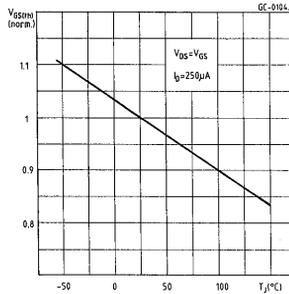
Gate charge vs gate-source voltage



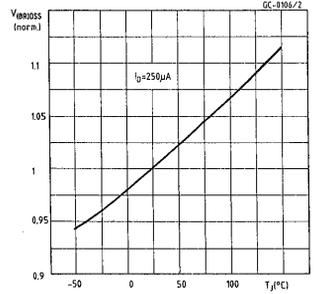
Capacitance variation



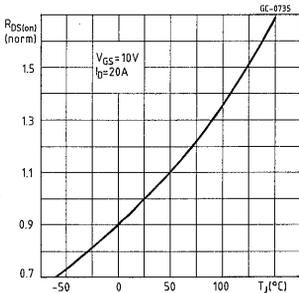
Normalized gate threshold voltage vs temperature



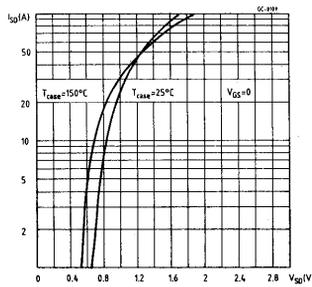
Normalized breakdown voltage vs temperature



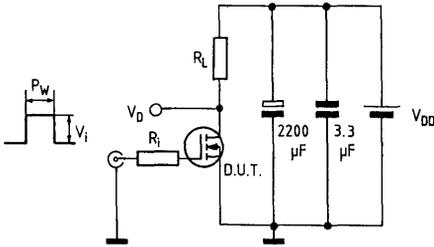
Normalized on resistance vs temperature



Source-drain diode forward characteristics



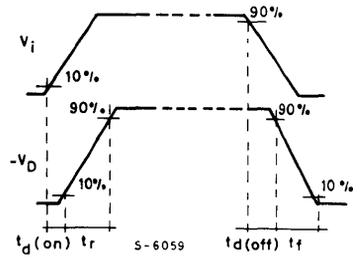
Switching times test circuit for resistive load



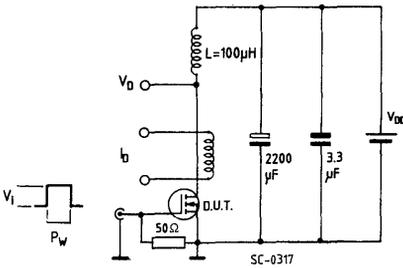
Pulse width $\leq 100 \mu\text{s}$
 Duty cycle $\leq 2\%$

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Switching time waveforms for resistive load



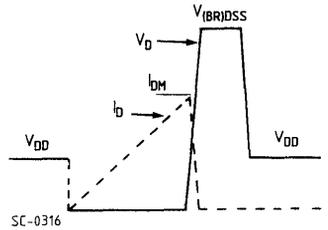
Unclamped inductive load test circuit



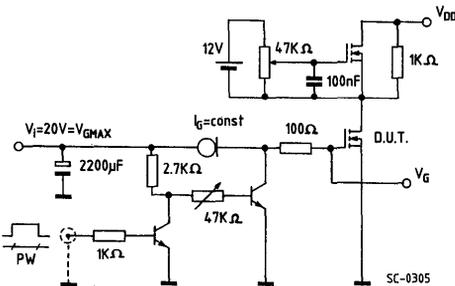
$V_i = 12 \text{ V}$ - Pulse width: adjusted to obtain specified I_{DM}

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Unclamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
 Jedec test circuit

