SGS-THOMSON MICROELECTRONICS

SGSP577

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

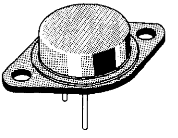
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP577	200 V	0.17 Ω	20 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH CURRENT - FOR TELECOMM POWER SUPPLIES
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

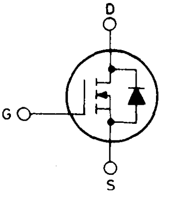
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS FOR ROBOTICS.

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include robotics, UPS, SMPS and DC/DC converters, electric vehicle drives and a DC switch for telecommunications.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	200	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	200	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	20	A
I_D	Drain current (cont.) at $T_c=100°C$	13	A
I_{DM} (•)	Drain current (pulsed)	80	A
I_{DLM} (•)	Drain inductive current, clamped	80	A
P_{tot}	Total dissipation at $T_c<25°C$	150	W
	Derating factor	1.2	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj-case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 10 A V_{GS} = 10 V I_D = 10 A T_c = 100°C			0.17 0.34	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 10 A	8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900	2200 550 260	pF pF pF
SWITCHING						
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 100 V I_D = 10 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		30 50 110 35	40 65 145 45	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

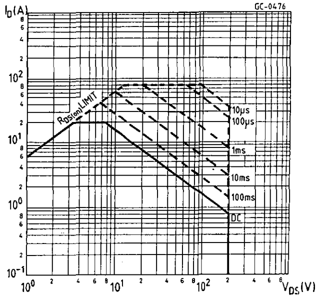
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

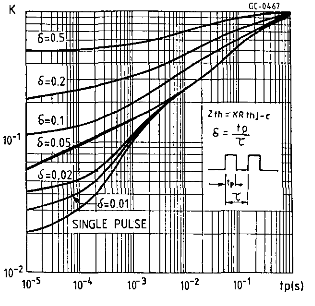
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)				20 80	A A
V_{SD}	Forward on voltage	I_{SD} = 20 A V_{GS} = 0			1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A V_{GS} = 0 di/dt = 100 A/μs		320		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

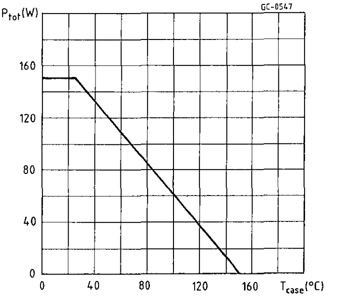
Safe operating areas



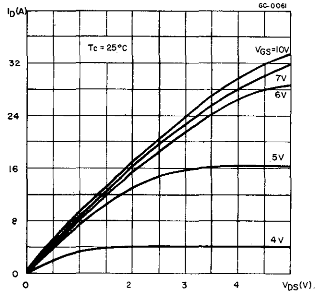
Thermal impedance



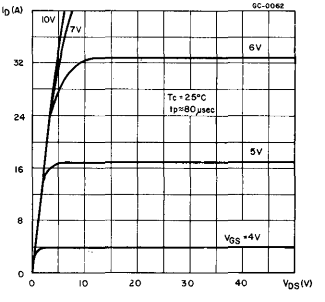
Derating curve



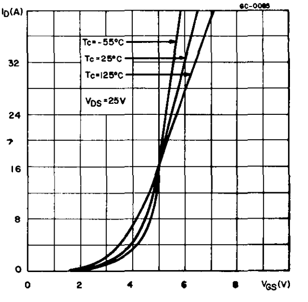
Output characteristics



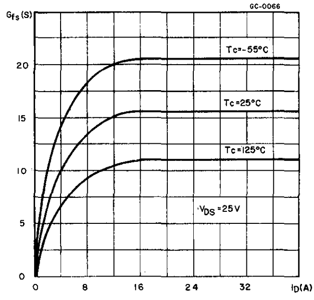
Output characteristics



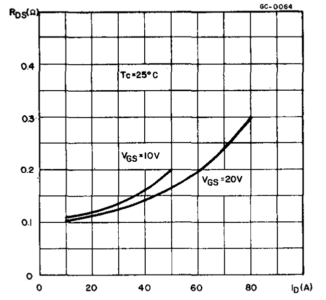
Transfer characteristics



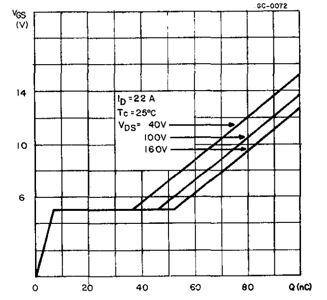
Transconductance



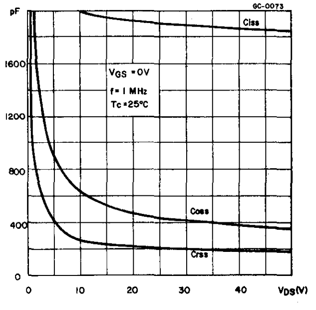
Static drain-source on resistance



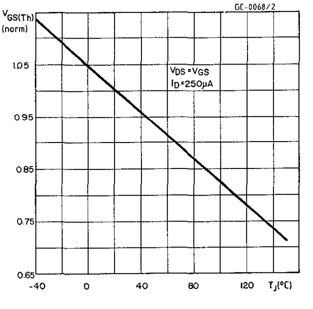
Gate charge vs gate-source voltage



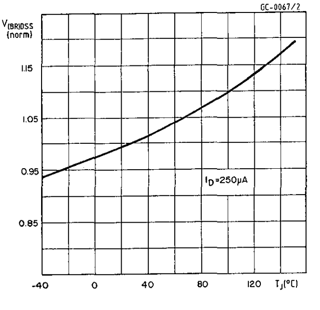
Capacitance variation



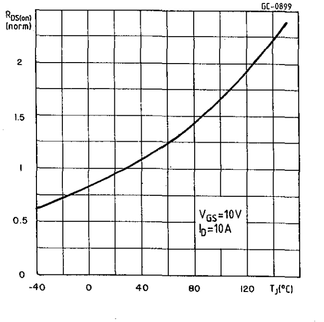
Normalized gate threshold voltage vs temperature



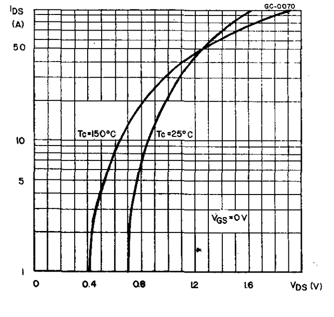
Normalized breakdown voltage vs temperature



Normalized on resistance vs temperature



Source-drain diode forward characteristics



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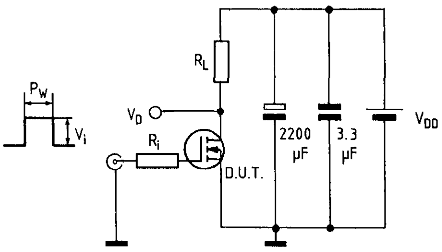
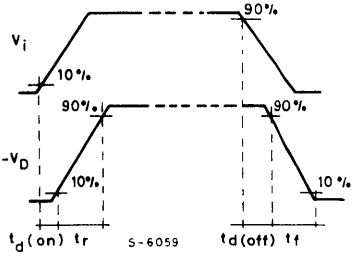
Switching times test circuit for resistive load

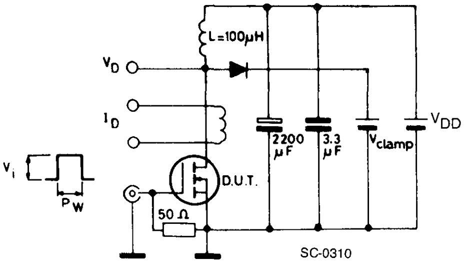


Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
$V_i = 10$ V

Switching time waveforms for resistive load

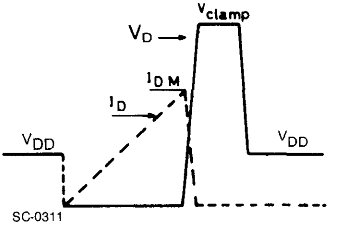


Clamped inductive load test circuit

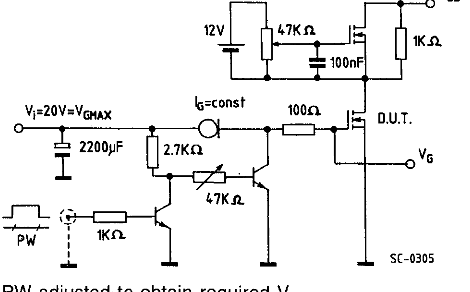


$V_i =$ 12 V - Pulse width: adjusted to obtain specified I_{DM}, $V_{clamp} = 0.75\ V_{(BR)\ DSS}$.

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit