

**N - CHANNEL ENHANCEMENT MODE
 POWER MOS TRANSISTOR MODULE**

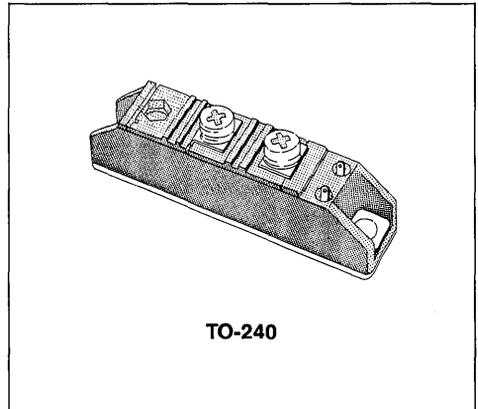
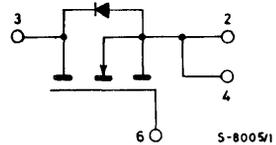
TYPE	V _{DSS}	R _{DS(on)}	I _D
SGS100MA010D1	100 V	0.014 Ω	120 A

- ISOLATED POWERMOS MODULE
- HIGH POWER
- FAST SWITCHING
- EASY DRIVE
- EASY TO PARALLEL

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS
- INVERTERS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and fast switching of this TRANSPACK module make it ideal for high power, high speed switching applications. Typical applications include DC motor control (variable frequency control) switching mode power supplies, uninterruptible power supplies, DC/DC converters and high frequency welding equipment. The large RBSOA and absence of second breakdown in POWER MOS make this TRANSPACK module very rugged. This, together with the isolated package with its optimised thermal performance, make this module extremely effective in high power applications.


TO-240
**INTERNAL SCHEMATIC
 DIAGRAM**

ABSOLUTE MAXIMUM RATINGS

V _{DS}	Drain-source voltage (V _{GS} =0)	100	V
V _{DGR}	Drain-gate voltage (R _{GS} =20 KΩ)	100	V
V _{GS}	Gate-source voltage	±20	V
I _D	Drain current (cont.) at T _c =25°C	120	A
I _D	Drain current (cont.) at T _c =100°C	75	A
I _{DM}	Drain current (pulsed)	400	A
P _{tot}	Total dissipation at T _c < 25°C	400	W
	Derating factor	3.2	W/°C
T _{stg}	Storage temperature	-65 to 150	°C
T _j	Max. operating junction temperature	150	°C
V _{ISO}	Insulation withstand voltage (AC)	2500	V

THERMAL DATA

$R_{thj - case}$	Thermal resistance junction-case	max	0.31	°C/W
$R_{thc - h}$	Thermal resistance case-heatsink	max	0.20	°C/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 2 \text{ mA}$	$V_{GS} = 0$	100		V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$	$T_j = 125^\circ\text{C}$		500 2	μA mA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$		-	± 400	nA

ON*

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 2 \text{ mA}$	2		4 V
$R_{DS (on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$	$I_D = 50 \text{ A}$			14 m Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 \text{ V}$	$I_D = 50 \text{ A}$	20		mho
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$	$f = 1 \text{ MHz}$		11200	pF
C_{oss}	Output capacitance				4200	pF
C_{rss}	Reverse transfer capacitance				1700	pF

SWITCHING

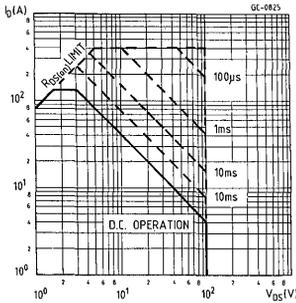
$t_{d (on)}$	Turn-on time	$V_{DD} = 50 \text{ V}$	$I_D = 50 \text{ A}$		120	ns
$(di/dt)_{on}$	Turn-on current slope	$R_i = 50 \Omega$	$V_i = 10 \text{ V}$		100	A/ μs
$t_{d (off)}$	Turn-off delay time				2	μs
t_f	Fall time				300	ns

ELECTRICAL CHARACTERISTICS (Continued)

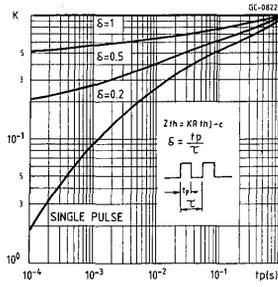
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)			120 400	A A
V_{SD}	Forward on voltage	$I_{SD} = 120\text{ A}$	$V_{GS} = 0$	2	V
t_{rr}	Reverse recovery time	$I_{SD} = 120\text{ A}$	$di/dt = 100\text{ A}/\mu\text{s}$	400	ns

* Pulsed: Pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

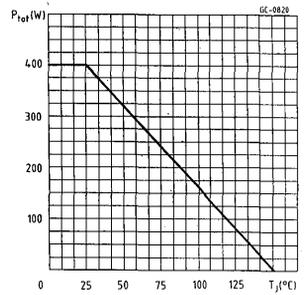
Safe operating areas



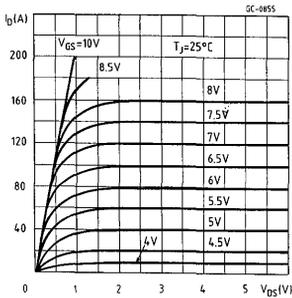
Thermal impedance



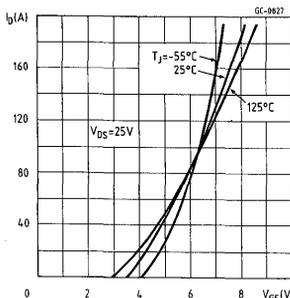
Derating curve



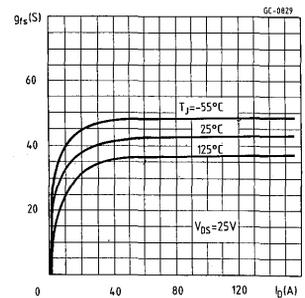
Output characteristics



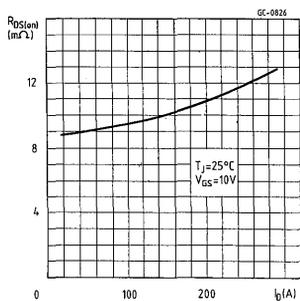
Transfer characteristics



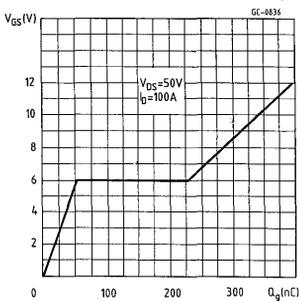
Transconductance



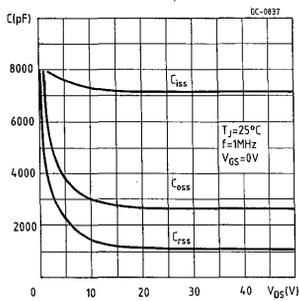
Static drain-source on resistance



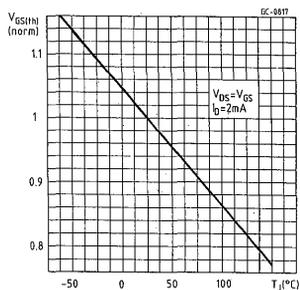
Gate charge vs gate-source voltage



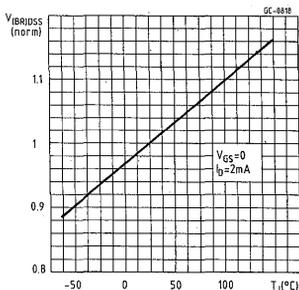
Capacitance variation



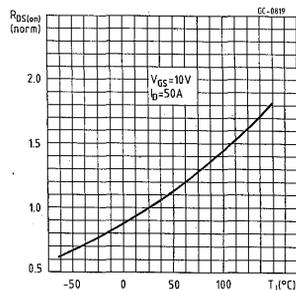
Normalized gate threshold voltage vs temperature



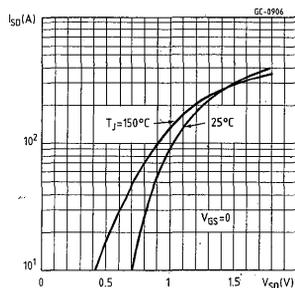
Normalized breakdown voltage vs temperature



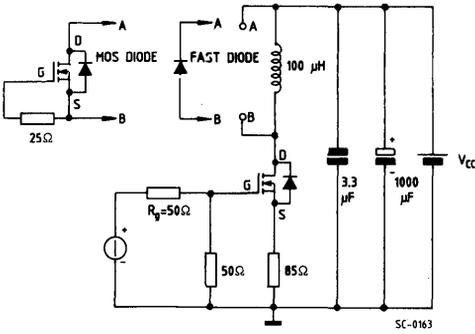
Normalized on resistance vs temperature



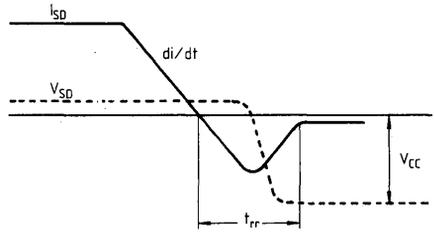
Source-drain diode forward characteristics



Test circuit for inductive load switching and diode reverse recovery times

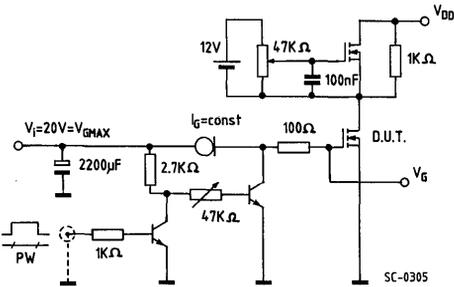


Diode reverse recovery time waveform



SC-0162

Gate charge test circuit



PW adjusted to obtain required V_G