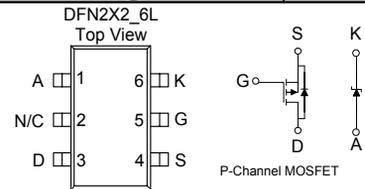


P-Channel 20-V (D-S) MOSFET With Schottky Diode

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN2X2_6L saves board space
- Fast switching speed
- High performance trench technology

MOSFET PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
-20	0.090 @ $V_{GS} = -4.5V$	-4.5
	0.120 @ $V_{GS} = -2.5V$	-4.5
SCHOTTKY PRODUCT SUMMARY		
V_{KA} (V)	V_f (V) Diode Forward Voltage	I_F (A)
20	0.46V @ 0.5A	1



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage (MOSFET)		V_{DS}	-20	V
Reverse Voltage (Schottky)		V_{KA}	20	
Gate-Source Voltage (MOSFET)		V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ C$) (MOSFET) ^a	$T_A = 25^\circ C$	I_D	-4.5	A
	$T_A = 70^\circ C$		-4.5	
Pulsed Drain Current (MOSFET) ^b		I_{DM}	-8	
Continuous Source Current (MOSFET Diode Conduction) ^a		I_S	-4.5	
Average Forward Current (Schottky)		I_F	1	
Pulsed Forward Current (Schottky)		I_{FM}	2	
Maximum Power Dissipation (MOSFET) ^a	$T_A = 25^\circ C$	P_D	6.5	
	$T_A = 70^\circ C$		5	
Maximum Power Dissipation (Schottky) ^a	$T_A = 25^\circ C$		7.3	
	$T_A = 70^\circ C$		4.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	52	65	
	Steady State		12.5	16	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

MOSFET SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.4			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-10	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-8			A
Drain-Source On-State Resistance ^A	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -1 \text{ A}$			0.090	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -1 \text{ A}$			0.120	
Forward Transconductance ^A	g_{fs}	$V_{DS} = -5 \text{ V}, I_D = -1 \text{ A}$		3		S
Diode Forward Voltage	V_{SD}	$I_S = -1.6 \text{ A}, V_{GS} = 0 \text{ V}$		-0.70		V
Dynamic^B						
Total Gate Charge	Q_g	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_D = -3.6 \text{ A}$		6.0		nC
Gate-Source Charge	Q_{gs}			0.80		
Gate-Drain Charge	Q_{gd}			1.30		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -5 \text{ V}, R_L = 5 \text{ OHM},$ $V_{GEN} = -4.5 \text{ V}, R_G = 6 \text{ OHM}$		6.5		ns
Rise Time	t_r			20		
Turn-Off Delay Time	$t_{d(off)}$			31		
Fall-Time	t_f			21		

SCHOTTKY SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Forward Voltage Drop	V_F	$I_F = 0.5 \text{ A}$			0.46	V
		$I_F = 0.5 \text{ A}, T_J = 125^\circ\text{C}$			0.53	V
Maximum Reverse Leakage Current	I_{rm}	$V_r = 5 \text{ V}$			0.041	mA
		$V_r = 30 \text{ V}, T_J = 75^\circ\text{C}$			4	
		$V_r = 30 \text{ V}, T_J = 125^\circ\text{C}$			28	
Junction Capacitance	C_T	$V_r = 10 \text{ V}$		30		pF

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

Typical Electrical Characteristics

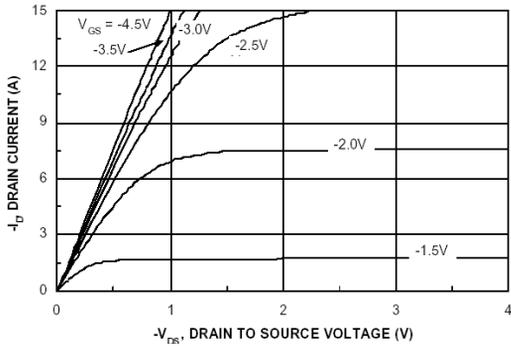


Figure 1. On-Region Characteristics

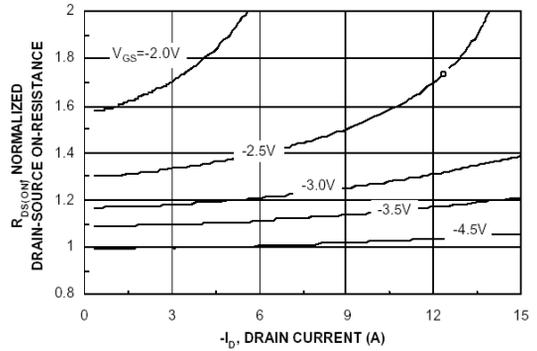


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

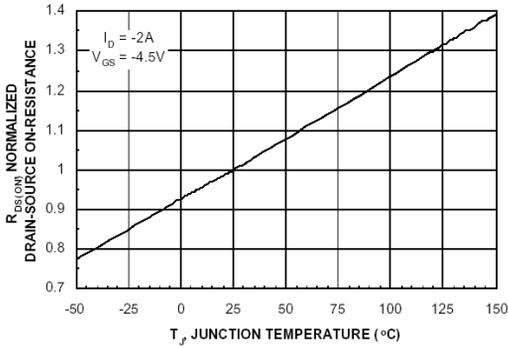


Figure 3. On-Resistance Variation with Temperature

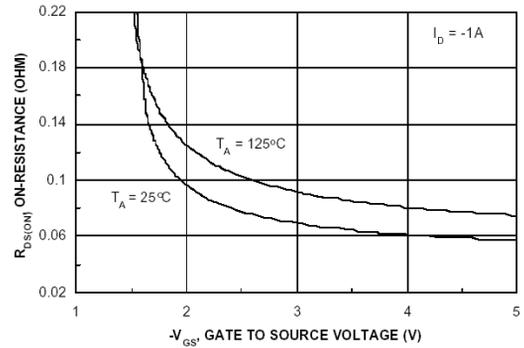


Figure 4. On-Resistance Variation with Gate to Source Voltage

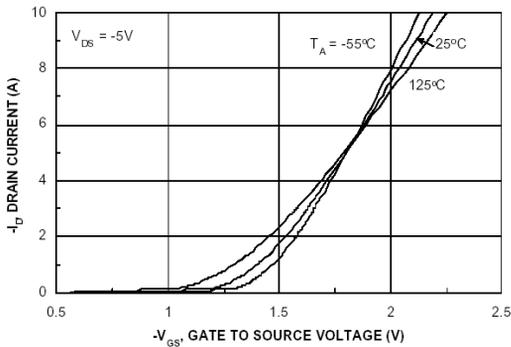


Figure 5. Transfer Characteristics

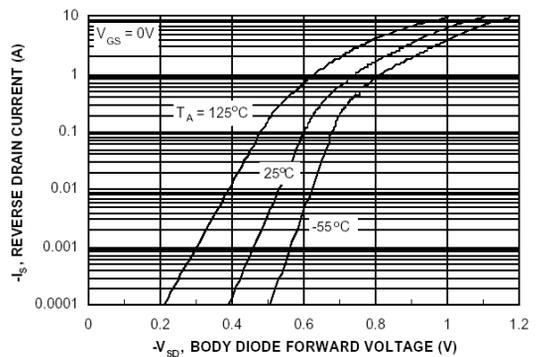


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Electrical Characteristics

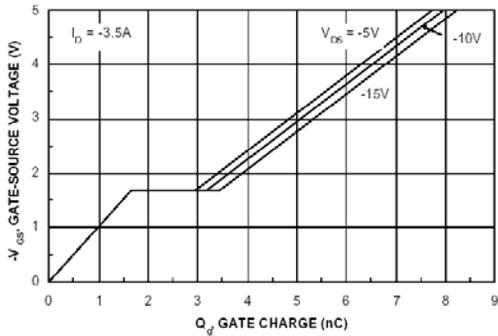


Figure 7. Gate Charge Characteristic

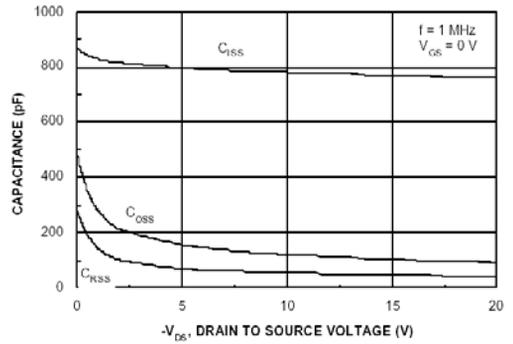


Figure 8. Capacitance Characteristic

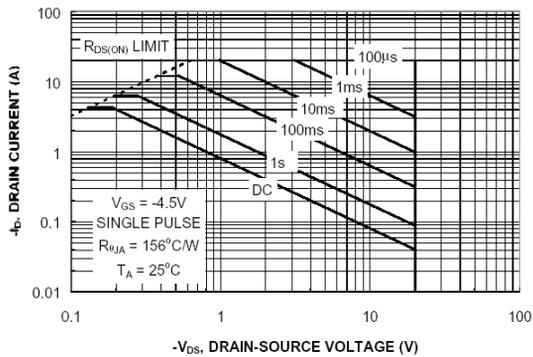


Figure 9. Maximum Safe Operating Area

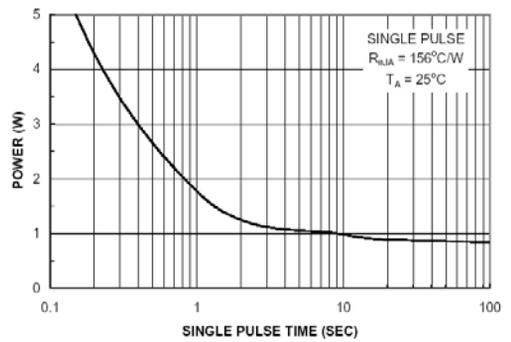


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

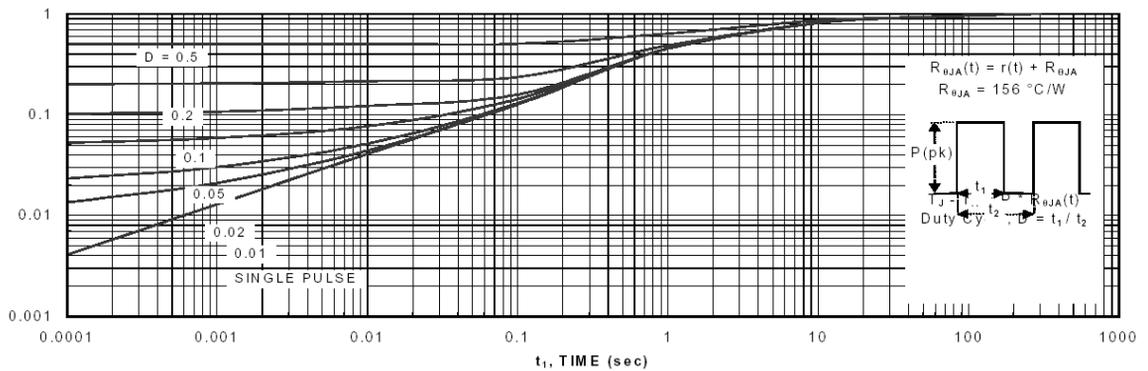
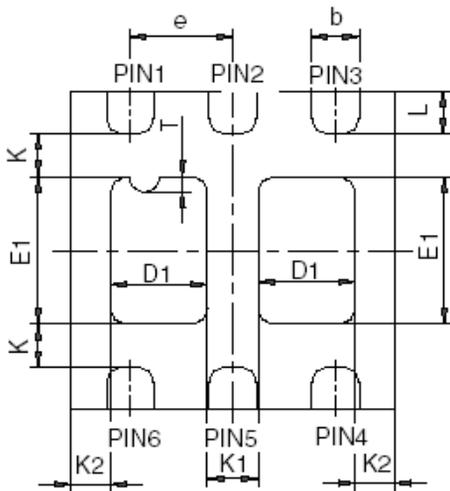


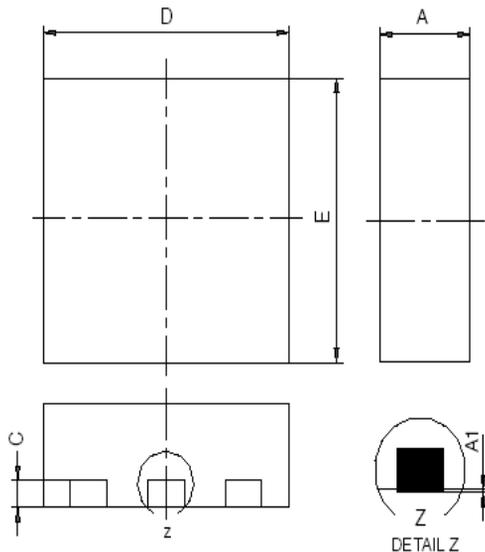
Figure 11. Transient Thermal Response Curve.

Package Information



BACKSIDE VIEW OF DUAL

DIM	DUAL PAD					
	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032
A1	0		0.05	0		0.002
b	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.00 BSC			0.079 BSC		
D1	0.600	0.650	0.700	0.024	0.026	0.028
E	2.00 BSC			0.079 BSC		
E1	0.81	0.86	0.91	0.032	0.034	0.036
e	0.65 BSC			0.026 BSC		
K1	0.25	0.30	0.35	0.010	0.012	0.014
K2	0.65 BSC			0.026 BSC		
L	0.250	0.300	0.350	0.01	0.012	0.014



ECN History

A: New Product

A to B: Add Typical Electrical
Characteristics &
Package