

N-Channel 20-V (D-S) MOSFET

Key Features:

- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed

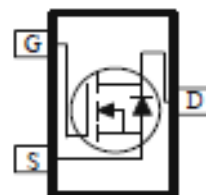
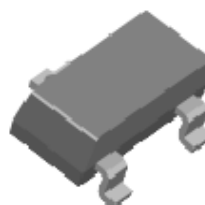
Typical Applications:

- Power Routing
- Li Ion Battery Packs
- Level Shifting and Driver Circuits

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (m Ω)	I_D (A)
20	25 @ $V_{GS} = 4.5V$	5.9
	35 @ $V_{GS} = 2.5V$	5.0



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	5.9	A
	$T_A = 70^\circ\text{C}$		4.7	
Pulsed Drain Current ^b		I_{DM}	20	
Continuous Source Current (Diode Conduction) ^a		I_S	1.9	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.3	W
	$T_A = 70^\circ\text{C}$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	100	$^\circ\text{C/W}$
	Steady State		166	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

Electrical Characteristics

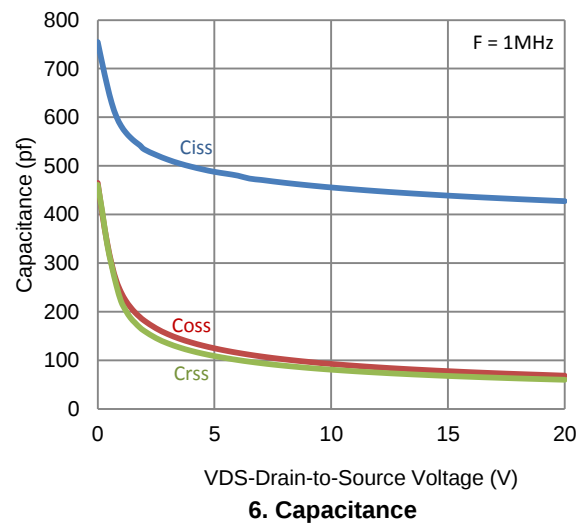
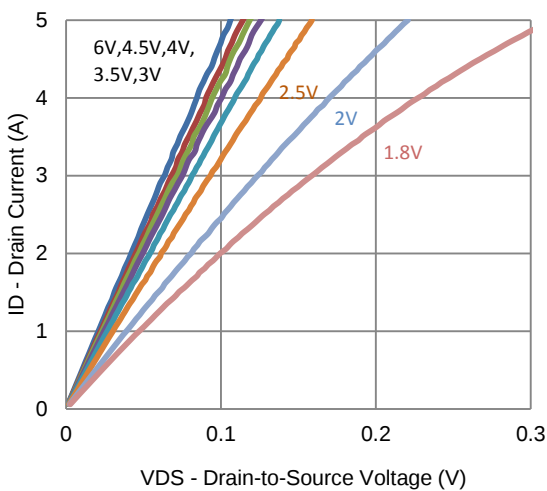
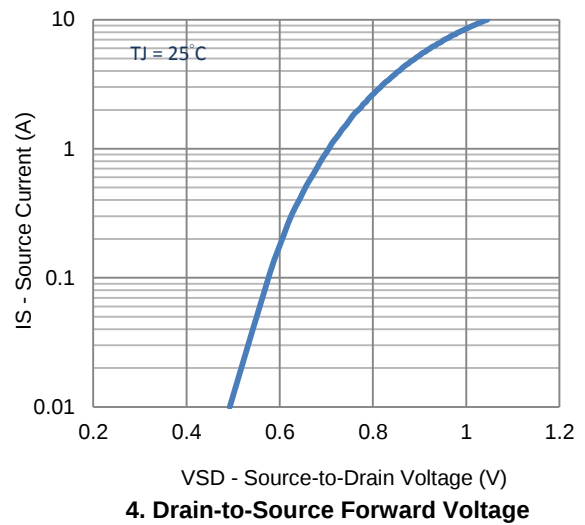
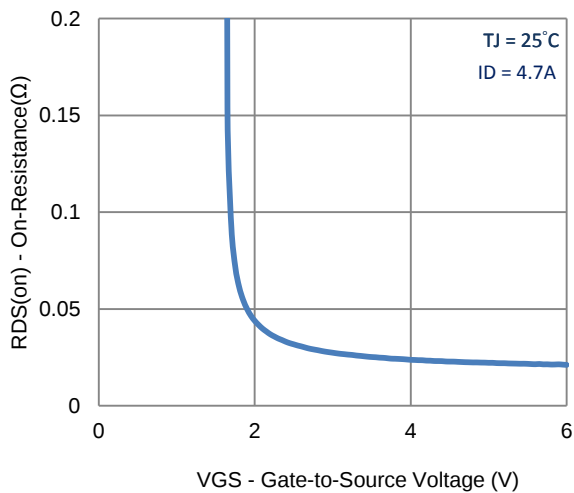
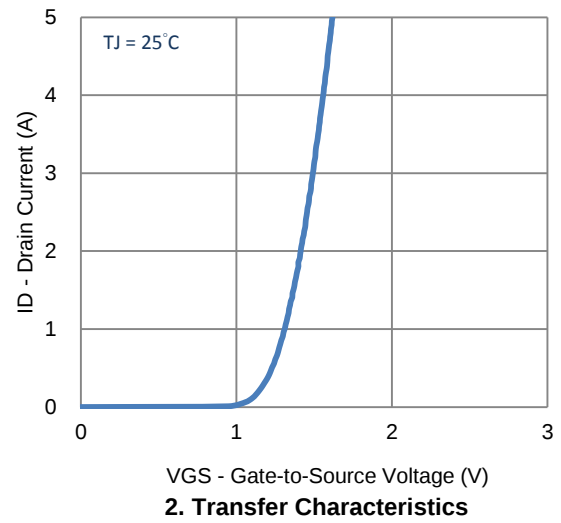
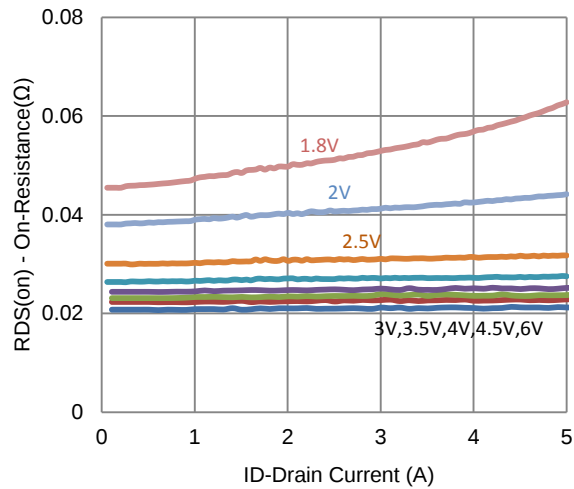
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.4			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 8 V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 V, V_{GS} = 0 V$			1	uA
		$V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55^\circ C$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 4.5 V$	10			A
Drain-Source On-Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5 V, I_D = 4.7 A$			25	mΩ
		$V_{GS} = 2.5 V, I_D = 3.8 A$			35	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 V, I_D = 4.7 A$		8		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 0.95 A, V_{GS} = 0 V$		0.71		V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 10 V, V_{GS} = 4.5 V,$ $I_D = 4.7 A$		6.9		nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			2.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 10 V, R_L = 2.2 \Omega,$ $I_D = 4.7 A,$ $V_{GEN} = 4.5 V, R_{GEN} = 6 \Omega$		9		ns
Rise Time	t_r			22		
Turn-Off Delay Time	$t_{d(off)}$			36		
Fall Time	t_f			16		
Input Capacitance	C_{iss}	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1 Mhz$		438		pF
Output Capacitance	C_{oss}			77		
Reverse Transfer Capacitance	C_{rss}			67		

Notes

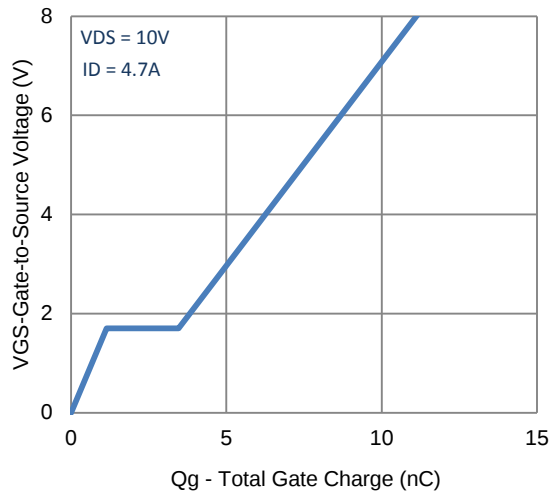
- a. Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

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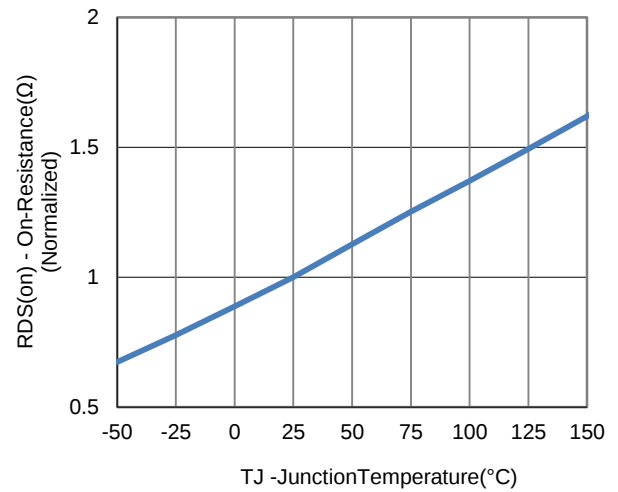
Typical Electrical Characteristics



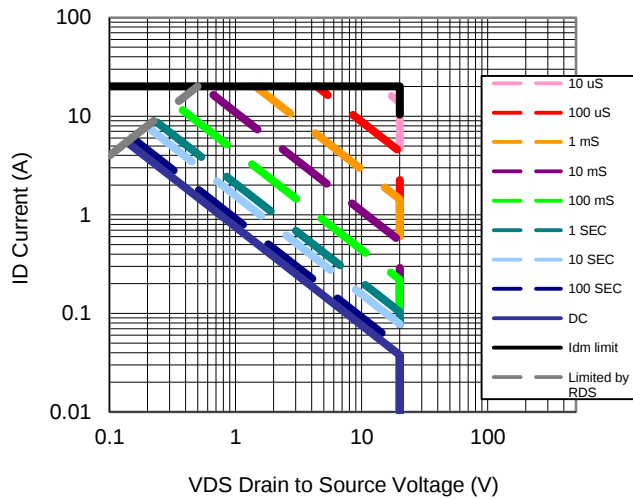
Typical Electrical Characteristics



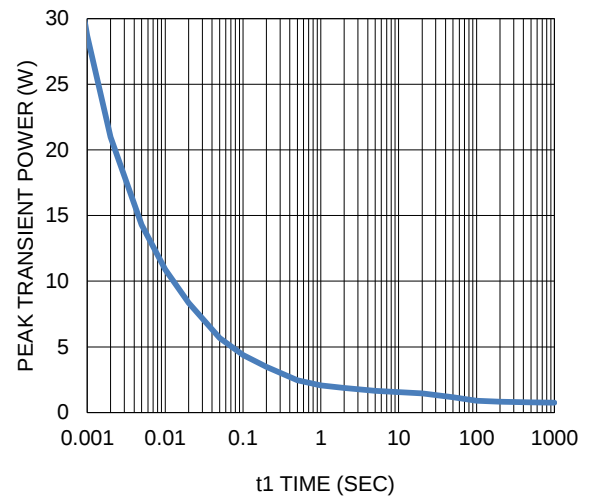
7. Gate Charge



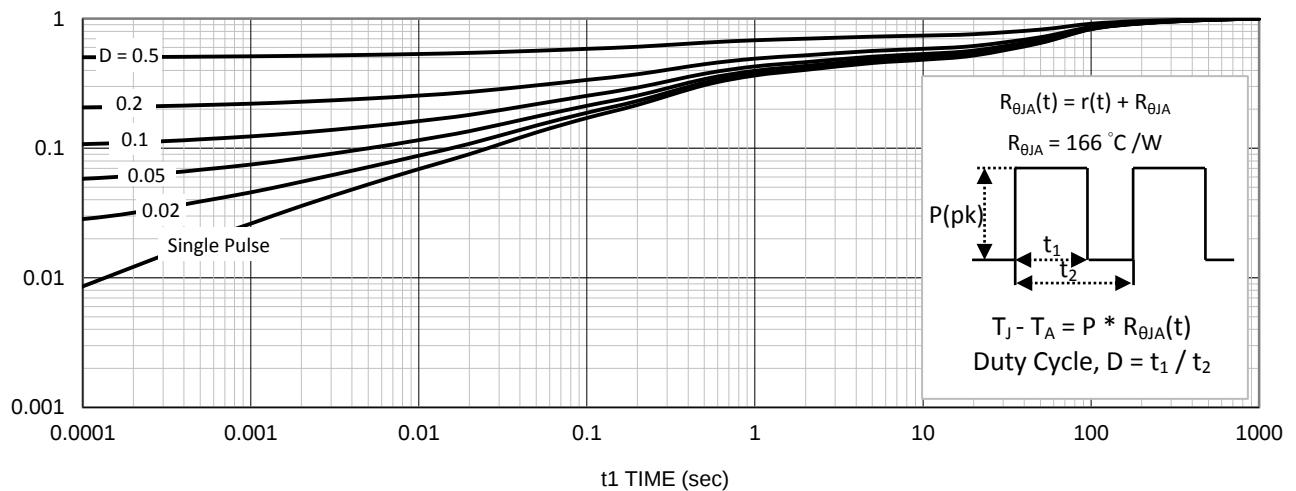
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area

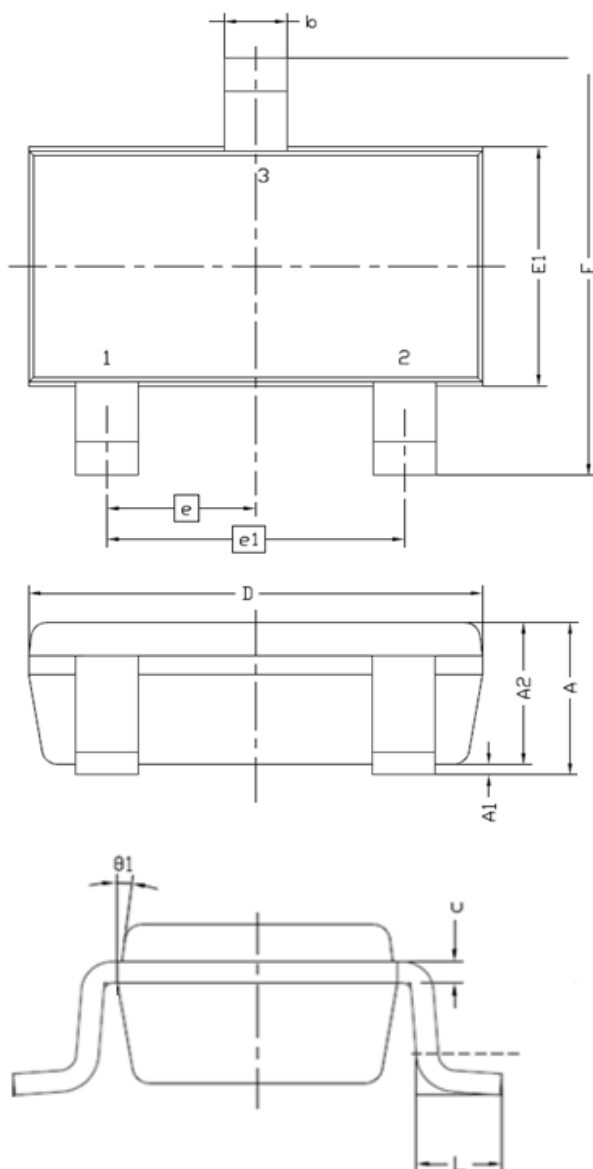


10. Single Pulse Maximum Power Dissipation



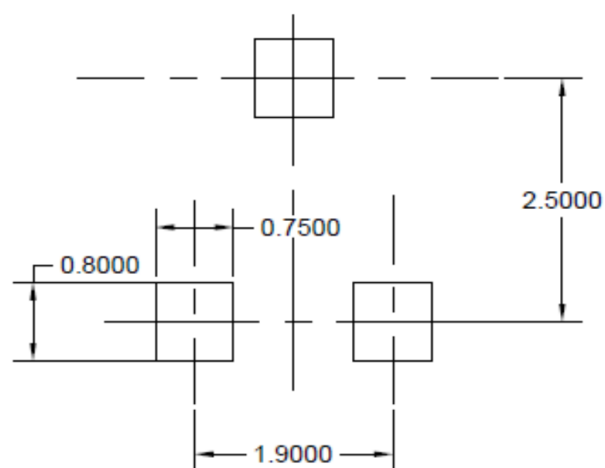
11. Normalized Thermal Transient Junction to Ambient

Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.25
A1	0	0.13
A2	0.7	1.15
b	0.3	0.5
c	0.08	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.9	1
e1	1.8	2
L	0.3	0.6
θ1	7° NOM	

Recommended Pad Layout



Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance

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