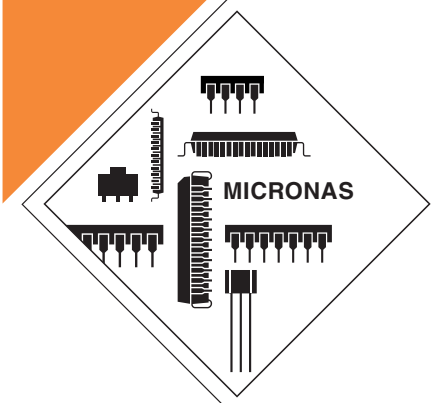


DATA SHEET

CDC 3207G-C3
Automotive Controller

Edition Feb. 10, 2005
6251-589-1DS

MICRONAS

Contents

1. Introduction

Release Note: Revision bars indicate significant changes to the previous edition.

The device is a microcontroller for use in automotive applications. The on-chip CPU is an ARM® processor ARM7TDMI™ with 32-bit data and address bus, which supports Thumb™ format instructions.

The chip contains timer/counters, an interrupt controller, a multichannel A/D converter, a stepper motor and LCD driver, CAN interfaces, PWM outputs and a crystal clock multiplying PLL.

This document provides MCM Flash hardware-specific information. General information on operating the IC can be found in the document “CDC32xxG-C Automotive Controller - Family User Manual, CDC3205G-C Automotive Controller” (6251-579-1DS)”.

1.1. Features

Table 1–1: CDC32xxG-C Family Feature List

Item	CDC3205G-C EMU	This Device: CDC3207G-C MCM Flash	CDC3217G-C MCM Flash	CDC3257G-C2 MCM Flash	CDC3272G-C Mask ROM	CDC3231G-C Mask ROM
Core						
CPU	32-bit ARM7TDMI™					
CPU-active operation modes	DEEP SLOW, SLOW, FAST and PLL					
Power-saving operation modes (CPU inactive)	IDLE, WAKE and STANDBY					
CPU clock multiplication	PLL delivering up to 50 MHz					
EMI reduction mode	selectable in PLL mode					
Oscillators	4 to 5 MHz quartz and 32 kHz internal RC					
RAM, zero wait state, 32 bit wide	32 Kbyte			12 Kbyte	16 Kbyte	6 Kbyte
ROM	ROMless, ext. up to 4 M × 32/ 8 M × 16	512-Kbyte Flash (256 K × 16) top-boot conf.	1024-Kbyte Flash (512 K × 16) top-boot conf.	256-Kbyte Flash (128 K × 16) top-boot conf.	384 Kbyte (96 K × 32/ 192 K × 16)	128 Kbyte (32 K × 32/ 64 K × 16)
Boot ROM	8 Kbyte (special function ROM)					
Digital watchdog	✔					
Central clock divider	✔					
Interrupt controller expanding IRQ	40 inputs, 16 priority levels					26 inputs, 16 priority levels
Port interrupts including slope selection	6 inputs					5 inputs
Port wake-up inputs including slope/level selection	10 inputs					

Table 1–1: CDC32xxG-C Family Feature List

Item	CDC3205G-C EMU	This Device: CDC3207G-C MCM Flash	CDC3217G-C MCM Flash	CDC3257G-C2 MCM Flash	CDC3272G-C Mask ROM	CDC3231G-C Mask ROM
Patch module	10 ROM locations					
Boot system	allows in-system downloading of external code to Flash memory via JTAG				-	
Device lock module	inhibits access to internal firmware, lock can be set by customer				-	
Analog						
Reset/Alarm	combined input for regulator input supervision					
Clock and supply supervision	✔					
10-bit ADC, charge balance type	16 channels (each selectable as digital input)					
ADC reference	VREF pin, P1.0 pin, P1.1 pin or VREFINT internal bandgap selectable					
Comparators	P06COMP with 1/2 AVDD reference, WAITCOMP with internal bandgap reference					
LCD	internal processing of all analog voltages for the LCD driver					
Communication						
DMA	3 DMA channels, one each for serving the graphics bus interface, SPI0 and SPI1					-
UART	2: UART0 and UART1					UART0
Synchronous serial peripheral interfaces	2: SPI0 and SPI1, DMA supported					
Full CAN modules V2.0B each with a 32-object RAM (LCAN000E)	4: CAN0, CAN1, CAN2 and CAN3			2: CAN0 and CAN1		1: CAN0
DIGITbus	1 master module					-
I^2C	2 master modules: I2C0 and I2C1					I2C0
Graphics bus interface	8-bit data bus, DMA supported, e.g., for connection of EPSON SED 1560 LCD controller					-
Input & Output						
Universal ports selectable as 4:1-mux LCD segment/back-plane lines or digital I/O ports	up to 52 I/O or 48 LCD segment lines (= 192 segments), individually configurable as I/O or LCD					up to 50 I/O or 46 LCD segment lines (= 184 segments)
Universal port slew rate	SW-selectable					
Stepper motor control modules with high-current ports	7 modules, 32 dI/dt-controlled ports					4 modules 23 dI/dt-controlled ports

Table 1–1: CDC32xxG-C Family Feature List

Item	CDC3205G-C EMU	This Device: CDC3207G-C MCM Flash	CDC3217G-C MCM Flash	CDC3257G-C2 MCM Flash	CDC3272G-C Mask ROM	CDC3231G-C Mask ROM
PWM modules, each configurable as two 8-bit PWMs or one 16-bit PWM	6 modules: PWM0/1, PWM2/3, PWM4/5, PWM6/7, PWM8/9 and PWM10/11					5 modules: PWM0/1, PWM2/3, PWM4/5, PWM6/7, PWM8/9
Pulse/frequency modulator	2: PFM0 and PFM1					-
Audio module with auto-decay	✔					
SW-selectable clock outputs	2					
Polling/flash timer output	1 high-current port output operable in power-saving operation modes					
Timers & Counters						
16-bit free-running counters with capture/compare modules	CCC0 with 4 CAPCOM CCC1 with 2 CAPCOM					CCC0 with 4 CAPCOM
16-bit timers	1: T0					
8-bit timers	4: T1, T2, T3 and T4					
Real-time clock, delivering hours, minutes and seconds	✔					
Miscellaneous						
Scalable layout in CAN, RAM and ROM	-	✔				
Various HW options selectable at random	set by copy from user program storage during system start-up					
JTAG interface	allows Flash programming				✔	✔
On-chip debug aids	Embedded trace module, JTAG	JTAG				
Core bond-out	✔	-				
Supply voltage	3.5 to 5.5 V (limited I/O performance below 4.5 V)					
Case temperature range	0 °C to +70 °C	–40 °C to +105 °C				
Package						
Type	ceramic 257PGA	plastic 128QFP 0.5 mm pitch				
Bonded pins	256	128	128	128	126	111

1.2. Abbreviations

ADC	Analog-to-Digital Converter
AM	Audio Module
CAN	Controller Area Network
CAPCOM	Capture/Compare
CCC	Capture/Compare Counter
CPU	Central Processing Unit
DMA	Direct Memory Access
ERM	EMI Reduction Mode
ETM	Embedded Trace Module
I2C	I^2C Bus Interface
LCD	Liquid Crystal Display
P06COMP	P0.6 Alarm Comparator
PWM	Pulse Width Modulator
SM	Stepper Motor Control Module
SPI	Serial Synchronous Peripheral Interface
T	Timer
UART	Universal Asynchronous Receiver/Transmitter
WAITCOMP	Wait Comparator

1.3. Block Diagram

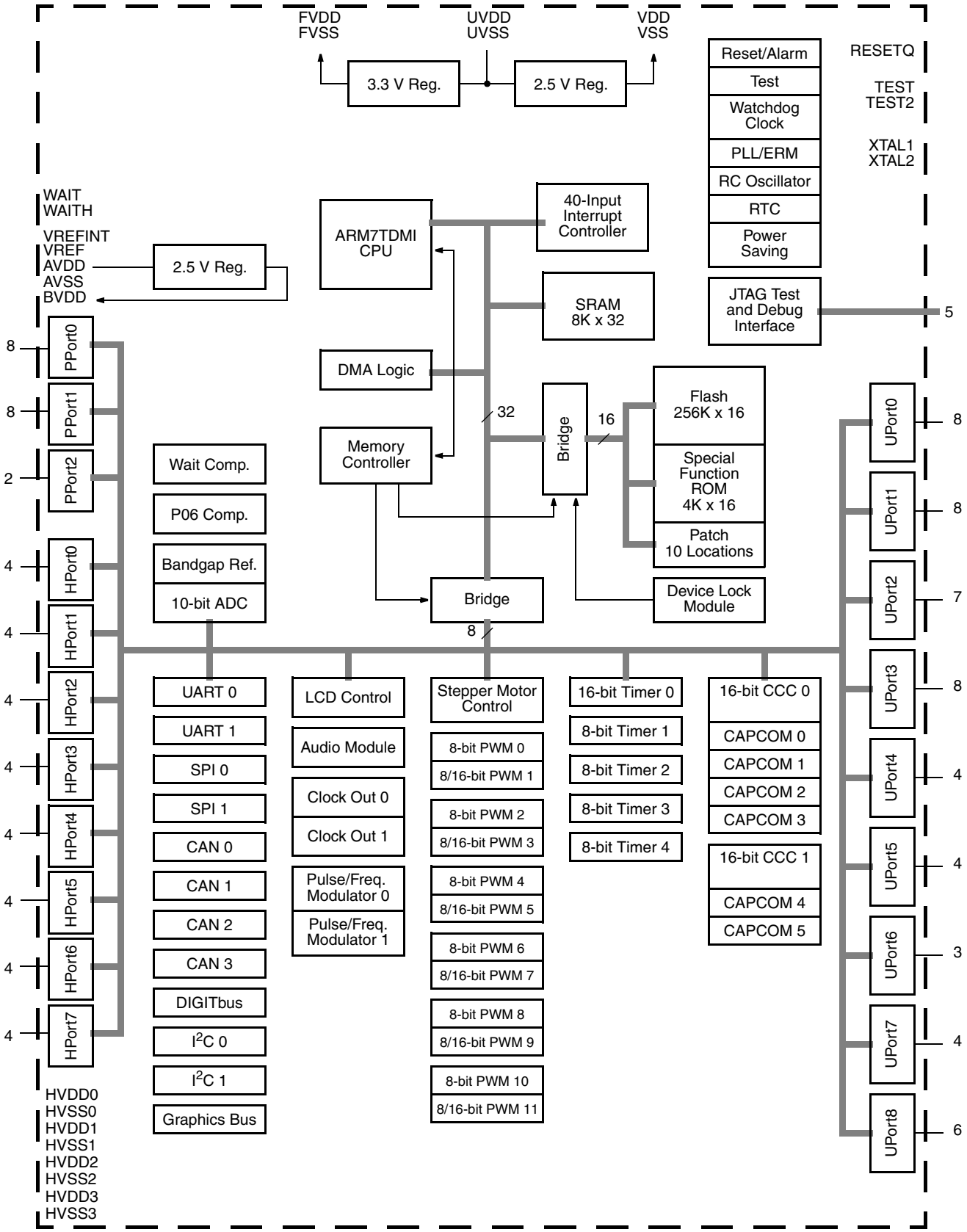
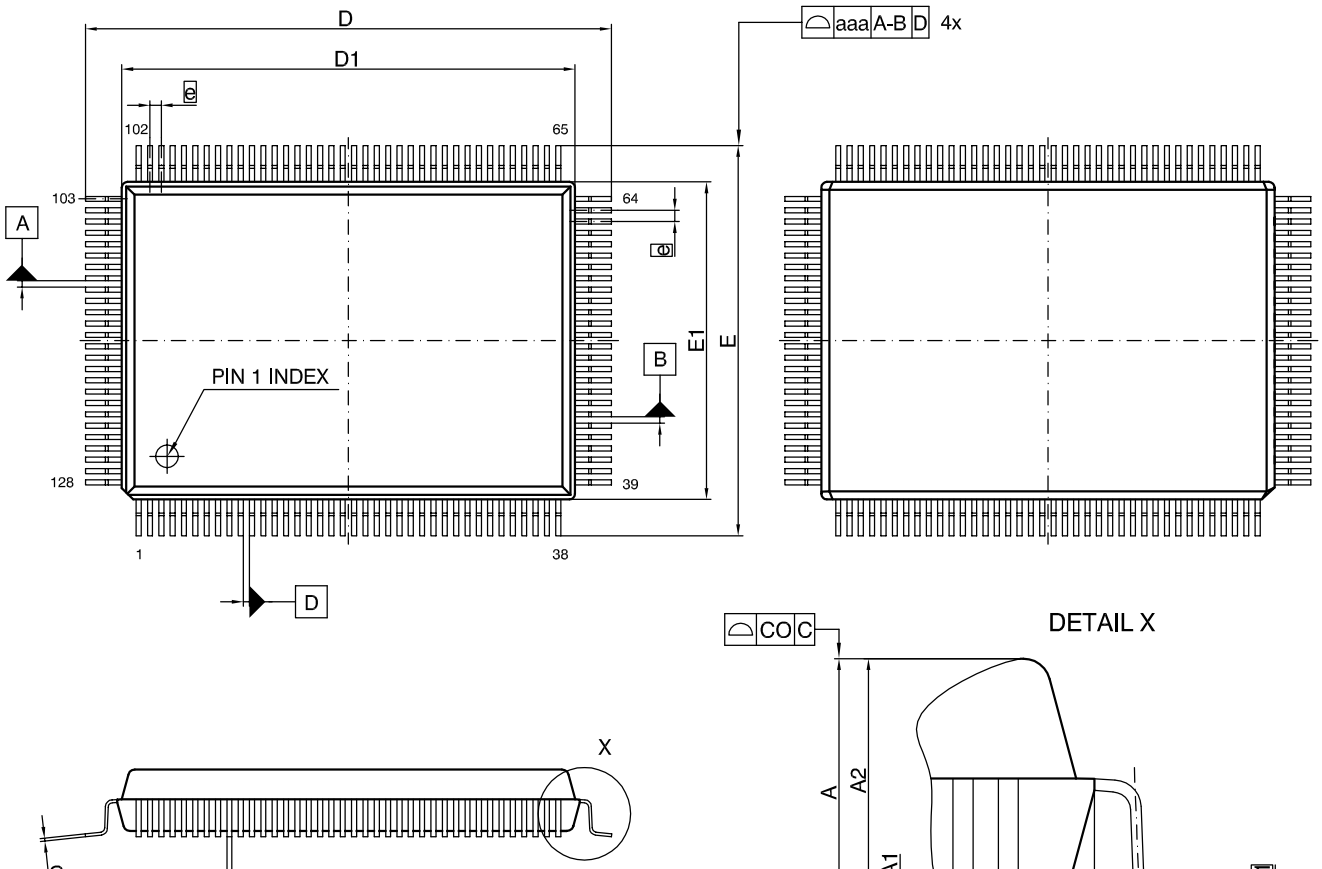


Fig. 1–1: CDC3207G-C block diagram

2. Packages and Pins

2.1. Package Outline Dimensions



UNIT	L2	Θ
mm	1.7 1.5	0°-7°

* does not include dambar protrusion of 0.08 max. per side

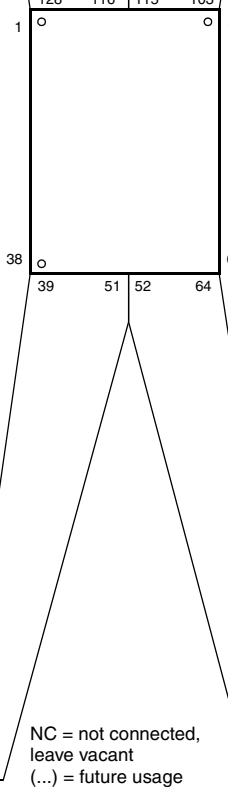
UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	3.2 2.8	0.5 0.1	2.8 2.6	0.2	0.27 0.17	0.2	0.21 0.13	0.1	23.2	20.0	17.2	14.0	0.5	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-04-16	06607.0001.4	SPZG001007_001_02

Fig. 2–1:
PMQFP128-2: Plastic **M**etric **Q**uad **F**lat **P**ackage, **128** leads, 14 × 20 × 2.7 mm^3
Ordering code: MF
Weight approximately 1.8 g

2.2. Pin Assignment

Pin Functions				Note	Pin No.
LCD Mode	Port Special Out	Port Special In	Basic Function		
SEG3.1	CC1-OUT	CC1-IN / TMS	U3.1		116
SEG3.0	CC2-OUT	CC2-IN / TDI	U3.0		117
			TEST2		118
			UVDD		119
			UVSS		120
SEG2.6	DIGIT-OUT	DIGIT-IN	U2.6		121
SEG2.5	CC1-OUT	UART0-RX	U2.5		122
SEG2.4	UART0-TX	DIGIT-IN/CC1-IN	U2.4		123
SEG2.3	CC2-OUT	UART1-RX	U2.3		124
SEG2.2	UART1-TX	CC2-IN	U2.2		125
SEG7.7	CO0		U7.7/GD7	1,2	126
SEG7.6	CO1		U7.6/GD6	1,2	127
SEG7.5	LCK/PFM1		U7.5/GD5	1,2	128
SEG7.4	CC5-OUT	CC5-IN	U7.4/GD4	1,2	1
			FVDD	1,2	2
			FVSS	1,2	3
SEG5.3	CC4-OUT	CC4-IN	U5.3/GD3	1	4
SEG5.2	SDA1	SDA1	U5.2/GD2	1	5
SEG5.1	SCL1	SCL1	U5.1/GD1	1	6
SEG5.0	PFM0		U5.0/GD0	1	7
SEG2.1	SDA0	WP6/SDA0/CAN0-RX	U2.1		8
SEG2.0	SCL0/CAN0-TX	SCL0	U2.0		9
SEG1.7	PFM0	WP0/PINT0	U1.7		10
SEG1.6	INTRES/CO0	PINT1	U1.6		11
SEG1.5	CO1/CO0Q	PINT2	U1.5		12
			TEST		13
			RESETQ/ALARMQ		14
			XTAL2		15
			XTAL1		16
			VSS		17
			VDD		18
SEG1.4	ITSTOUT/AM-OUT		U1.4		19
SEG1.3	MTO/AM-PWM	WP3	U1.3		20
SEG1.2	INTRES/T0-OUT	MTI/ITSTIN	U1.2		21
SEG1.1	T1-OUT		U1.1		22
SEG1.0	T2-OUT		U1.0		23
SEG0.7	T3-OUT	WP4	U0.7		24
SEG0.6	CC3-OUT/T4-OUT	CC3-IN	U0.6		25
SEG0.5	CC3-OUT	PINT4	U0.5		26
SEG0.4	CO1	PINT5	U0.4		27
SEG0.3	PWM0		U0.3		28
SEG0.2	PWM1		U0.2		29
SEG0.1	PWM2		U0.1		30
SEG0.0	PWM3		U0.0		31
	SME1+/PWM4	SME-COMP3	H7.3	1	32
	SME1-/PWM6	SME-COMP2	H7.2	1	33
	SME2+/PWM8	SME-COMP1	H7.1	1	34
	SME2-/PWM9	SME-COMP0	H7.0	1	35
			HVDD2	1,2	36
			HVSS2	1,2	37
	PWM8		H6.3	1,2	38
	PWM9		H6.2	1,2	39
	PWM10		H6.1	1,2	40
	PWM11		H6.0	1,2	41
	SMD1+	SMD-COMP3	H5.3		42
	SMD1-	SMD-COMP2	H5.2		43
			HVDD0		44
			HVSS0		45
	SMD2+	SMD-COMP1	H5.1		46
	SMD2-	SMD-COMP0	H5.0		47
	SMA1+	SMA-COMP3	H4.3		48
	SMA1-	SMA-COMP2	H4.2		49
	SMA2+	SMA-COMP1	H4.1		50
	SMA2-	SMA-COMP0	H4.0		51



Pin No.	Note	Pin Functions			
		Basic Function	Port Special In	Port Special Out	LCD Mode
115		U3.2	CC0-IN / TCK	CC0-OUT	SEG3.2
114		U3.3		CO0/TDO	SEG3.3
113		U3.4	SPI0-CLK-IN	SPI0-CLK-OUT	SEG3.4
112		U3.5	SPI0-D-IN	TO3	SEG3.5
111		U3.6		SPI0-D-OUT	SEG3.6
110		U3.7	SPI1-CLK-IN	SPI1-CLK-OUT	SEG3.7
109		U4.0	SPI1-D-IN	CC0-OUT	BP0
108		U4.1	CC0-IN	SPI1-D-OUT	BP1
107		U4.2		CAN0-TX	BP2
106		U4.3	CAN0-RX/WP5	TO2	BP3
105	1,2	U8.0		CC4-OUT	SEG8.0
104	1,2	U8.1		CC3-OUT	SEG8.1
103	1,2	U8.2	LCD-CLK-IN	CAN3-TX	SEG8.2
102	1,2	U8.3	CAN3-RX/WP9	LCD-CLK-OUT	SEG8.3
101	1,2	U8.4	LCD-SYNC-IN	CAN2-TX	SEG8.4
100	1,2	U8.5	CAN2-RX/PINT3/ WP8	LCD-SYNC-OUT	SEG8.5
99	1	U6.0		CAN1-TX	SEG6.0
98	1	U6.1	CAN1-RX/WP7	GOEQ	SEG6.1
97	1	U6.2		GWEQ	SEG6.2
96	1	P2.0			
95		P2.1			
94		P0.0	CC4-IN		
93		P0.1			
92		P0.2			
91		P0.3			
90		P0.4			
89		P0.5			
88		P0.6	P0.6 Comp.		
87		P0.7			
86		WAITH			
85		WAIT			
84		BVDD			
83		AVSS			
82		AVDD			
81		VREFINT			
80		VREF			
79		P1.0	VREF0/WP1		
78		P1.1	VREF1/WP2		
77		P1.2	PINT0		
76		P1.3	PINT1		
75		P1.4	PINT2		
74		P1.5	PINT3		
73		P1.6	PINT4		
72		P1.7	PINT5		
71	1	H0.0	SMG-COMP0	SMG2-/PWM7	
70	1	H0.1	SMG-COMP1	SMG2+/PWM5	
69	1	H0.2	SMG-COMP2	SMG1-/PWM3/POL	
68	1	H0.3	SMG-COMP3	SMG1+/PWM1	
67	1,2	HVSS3			
66	1,2	HVDD3			
65	1,2	H1.0	SMF-COMP0	SMF2-	
64	1,2	H1.1	SMF-COMP1	SMF2+	
63	1,2	H1.2	SMF-COMP2	SMF1-	
62	1,2	H1.3	SMF-COMP3	SMF1+	
61		H2.0	SMC-COMP0	SMC2-	
60		H2.1	SMC-COMP1	SMC2+	
59		HVSS1			
58		HVDD1			
57		H2.2	SMC-COMP2	SMC1-	
56		H2.3	SMC-COMP3	SMC1+	
55		H3.0	SMB-COMP0	SMB2-	
54		H3.1	SMB-COMP1	SMB2+	
53		H3.2	SMB-COMP2	SMB1-	
52		H3.3	SMB-COMP3	SMB1+	

Fig. 2–2: Pin assignment for PQFP128 package
Note 1 denotes pins that will not be available in future 88-pin versions.
Note 2 denotes pins that will not be available in future 104-pin versions.

2.3. Pin Function Description

(differing from document “CDC32xxG-C Automotive Controller - Family User Manual, CDC3205G-C Automotive Controller” (6251-579-1DS))

TEST2
For normal operation with internal code connect TEST2 to System Ground (no internal pull-down).

2.4. External Components

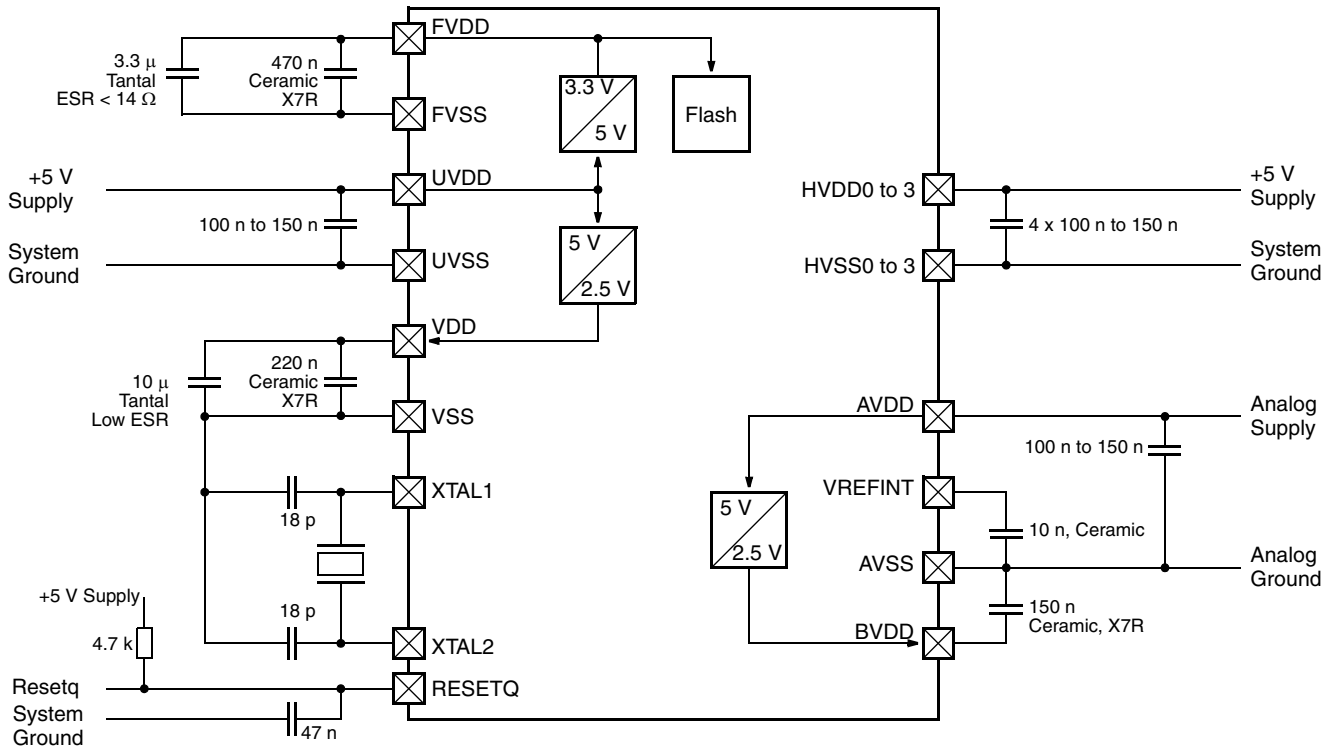


Fig. 2–3: CDC3207G-C: Recommended external supply and quartz connection.

To provide effective decoupling and to improve EMC behavior, the small decoupling capacitors must be located as close to the supply pins as possible. The self-inductance of these capacitors and the parasitic inductance and capacitance of the interconnecting traces determine the self-resonant frequency of the decoupling network. Too low a frequency will reduce decoupling effectiveness, will increase RF emissions and may adversely affect device operation.

XTAL1 and XTAL2 quartz connections are especially sensitive to capacitive coupling from other PC board signals. It is strongly recommended to place quartz and oscillation capacitors as close to the pins as possible and to shield the XTAL1 and XTAL2 traces from other signals by embedding them in a VSS trace.

The RESETQ pin adjacent to XTAL2 should be supplied with a 47 nF capacitor, to prevent fast RESETQ transients from being coupled into XTAL2, to prevent XTAL2 from coupling into RESETQ, and to guarantee a time constant of ≥200 µs sufficient for proper wake reset functionality.

3. Electrical Data

3.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum ratings conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

Table 3–1: All voltages listed are referenced to ground (UV_{SS} = HV_{SSn} = AV_{SS} = 0 V), except where noted. All ground pins except VSS must be connected to a low-resistive ground plane close to the IC.

Symbol	Parameter	Pin Name	Min.	Max.	Unit
V_{SUP}	Main supply voltage Analog supply voltage SM supply voltage	UVDD AVDD HVDD0 .. HVDD3	–0.3	6.0	V
V_{REG}	Flash supply voltage	FVDD	–0.3	4.0	V
	Core supply voltage PLL supply voltage	VDD BVDD	–0.3	3.0	V
I_{SUP}	Core supply current Main supply current	VDD, VSS, UVDD, UVSS	–100	100	mA
	Analog supply current	AVDD, AVSS	–20	20	mA
	SM supply current @T_{CASE} = 105 °C, duty factor = 0.71 [1)]	HVDD0 .. HVDD3 HVSS0 .. HVSS3	–250	250	mA
	Flash supply current	FVDD, FVSS	–50	50	mA
	PLL supply current	BVDD	–20	20	mA
V_{in}	Input voltage	U ports, XTAL,RESETQ, TEST, TEST2	UV_{SS} – 0.5	UV_{DD} + 0.7	V
		P ports VREF	UV_{SS} – 0.5	AV_{DD} + 0.7	V
		H ports	HV_{SS} – 0.5	HV_{DD} + 0.7	V
I_{in}	Input current	all inputs	0	2	mA
I_o	Output current	U ports, RESETQ, WAITH	–5	5	mA
		H ports	–60	60	mA
t_{oshsl}	Duration of short circuit to UVSS or UVDD, Port SLOW mode enabled	U ports, except in DP mode		indefinite	s
T_j	Junction temperature under bias		–45	115	°C
T_s	Storage temperature		–45	125	°C
P_{max}	Maximum power dissipation			0.8	W

[1)] This condition represents the worst case load with regard to the intended application.

3.2. Recommended Operating Conditions

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

Keep UV_{DD}=AV_{DD} during all power-up and power-down sequences.

Failure to comply with the above recommendations will result in unpredictable behavior of the device and may result in device destruction**.**

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions” of this specification is not implied, may result in unpredictable behavior of the device and may reduce reliability and lifetime.

Table 3–2: All voltages listed are referenced to ground (UV_{SS} = HV_{SSn} = AV_{SS} = 0 V), except where noted. All ground pins except VSS must be connected to a low-resistive ground plane close to the IC.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP}	Main supply voltage Analog supply voltage	UVDD = AVDD	3.5	5	5.5	V
HV_{SUP}	SM supply voltage	HVDDn	4.75	5	5.25	V
dV_{DD}	Ripple, peak-to-peak	UVDD AVDD BVDD FVDD VDD			200	mV
dV_{DD}/dt	Supply voltage up/down ramping rate	UVDD AVDD			20	V/µs
f_{XTAL}	XTAL clock frequency	XTAL1	4	4	5	MHz
f_{SYS}	CPU clock frequency, PLL on		For a list of available settings see Table 4–1.			
f_{BUS}	Program storage clock frequency, PLL on					
V_{il} [1)]	Automotive low input voltage	U ports H ports P ports			0.5 × xV_{DD}	V
	CMOS low input voltage	U ports, TEST, TEST2 H ports P ports			0.3 × xV_{DD}	V
V_{ih} [1)]	Automotive high input voltage	U ports H ports P ports	0.86 × xV_{DD}			V
	CMOS high input voltage	U ports,TEST, TEST2 H ports P ports	0.7 × xV_{DD}			V
RV_{il}	Reset active input voltage	RESETQ			0.75	V
WRV_{il}	Reset active input voltage during power-saving modes and wake reset	RESETQ			0.4	V
RV_{im}	Reset inactive and alarm active input voltage	RESETQ	1.5		2.3	V

[1)] For a list of input types and their supply voltages see Table 2-2 of document “CDC32xxG-C Automotive Controller - Family User Manual, CDC3205G-C Automotive Controller” (6251-579-1DS).

Table 3–2: All voltages listed are referenced to ground (UV_{SS} = HV_{SSn} = AV_{SS} = 0 V), except where noted. All ground pins except VSS must be connected to a low-resistive ground plane close to the IC.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
RV_{ih}	Reset inactive and alarm inactive input voltage	RESETQ	3.2			V
WRV_{ih}	Reset inactive input voltage during power-saving modes and wake reset	RESETQ	UV_{DD} – 0.4 V			V
V_{REFi}	Ext. ADC reference input voltage	VREF	2.56		AV_{DD}	V
PV_i	ADC port input voltage referenced to ext. VREF reference ADC port input voltage referenced to int. VREFINT reference	P ports	0 0		V_{REFi} V_{REFINT}	V

3.3. Characteristics

Listed are only those characteristics that differ from Chapter 3.3 of Document “CDC32xxG-C Automotive Controller - Family User Manual, CDC3205G-C Automotive Controller” (6251-579-1DS). All not differing characteristics, that are not listed here, apply, but in a T_{CASE} temperature range extended to –40 °C to +105 °C.

Table 3–3: UV_{SS} = FV_{SS} = HV_{SSn} = AV_{SS} = 0 V, 3.5 V < AV_{DD} = UV_{DD} < 5.5 V, 4.75 V < HV_{DDn} < 5.25 V, T_{CASE} = –40 °C to +105 °C, f_{XTAL} = 5 MHz, external components according to Fig. 2–3 (unless otherwise noted).

Symbol	Parameter	Pin Na.	Min.	Typ. [1]	Max.	Unit	Test Conditions
Package							
R_{thjc}	Thermal resistance from junction to case			9		K/W	measured on Micronas typical 2-layer board, 1s1p, described in document “Integrated Circuits - Thermal Characterization of Packages” (6200-266-1E) (modified JESD-51.3)
R_{thja}	Thermal resistance from junction to ambient			31		K/W	
Supply Currents (CMOS levels on all inputs, i.e., V_{il} = xV_{SS} ± 0.3 V and V_{ih} = xV_{DD} ± 0.3 V, no loads on outputs)							
UI_{DDp}	UVDD PLL mode supply current	UVDD			65 120	mA	f_{SYS} = 24 MHz f_{SYS} = 50 MHz
UI_{DDprog}	UVDD Flash program supply current	UVDD			45	mA	Flash Write/Erase, all modules off, [2]
UI_{DDf}	UVDD FAST mode supply current	UVDD			18	mA	all modules off, [2]
UI_{DDs}	UVDD SLOW mode supply current	UVDD		see Fig. 3–1	1.4	mA	all modules off, [2] [3]
[1] Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied, and are not 100% tested.							
[2] Value may be exceeded with unusual hardware option setting.							
[3] Measured with external clock. Add typically 120 µA for operation on quartz with SR0.XTAL=0 (Oscillator RUN mode).							

Table 3–3: $UV_{SS} = FV_{SS} = HV_{SSn} = AV_{SS} = 0$ V, 3.5 V < $AV_{DD} = UV_{DD}$ < 5.5 V, 4.75 V < HV_{DDn} < 5.25 V, T_{CASE} = −40 °C to +105 °C, f_{XTAL} = 5 MHz, external components according to Fig. 2–3 (unless otherwise noted).

Symbol	Parameter	Pin Na.	Min.	Typ. [1]	Max.	Unit	Test Conditions
UI_{DDd}	UVDD DEEP SLOW mode supply current	UVDD		see Fig. 3–1	0.9	mA	all modules off, [3]
UI_{DDw}	UVDD WAKE mode supply current	UVDD	0	20	50	µA	RC and XTAL oscillators off
UI_{DDst}	UVDD STANDBY mode supply current	UVDD		35	75	µA	RC oscillator on, XTAL off
		UVDD		60	100	µA	XTAL oscillator on, RC off [3]
UI_{DDi}	UVDD IDLE mode supply current	UVDD		50	475	µA	RC oscillator on, XTAL off
				see Fig. 3–1	500	µA	XTAL oscillator on, RC off [3]
AI_{DDa}	AVDD active supply current	AVDD		0.35	0.6	mA	ADC on, PLL off
					2	mA	ADC, buffer and PLL on
AI_{DDq}	Quiescent supply current	AVDD	0	1	10	µA	ADC and PLL off
HI_{DDq}		Sum of all HVDDn	0	1	40	µA	no output activity, SM module off
Inputs							
I_i	Input leakage current	TEST2	−1		1	µA	$0 < V_i < UV_{DD}$

[1] Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied, and are not 100% tested.

[2] Value may be exceeded with unusual hardware option setting.

[3] Measured with external clock. Add typically 120 µA for operation on quartz with SR0.XTAL=0 (Oscillator RUN mode).

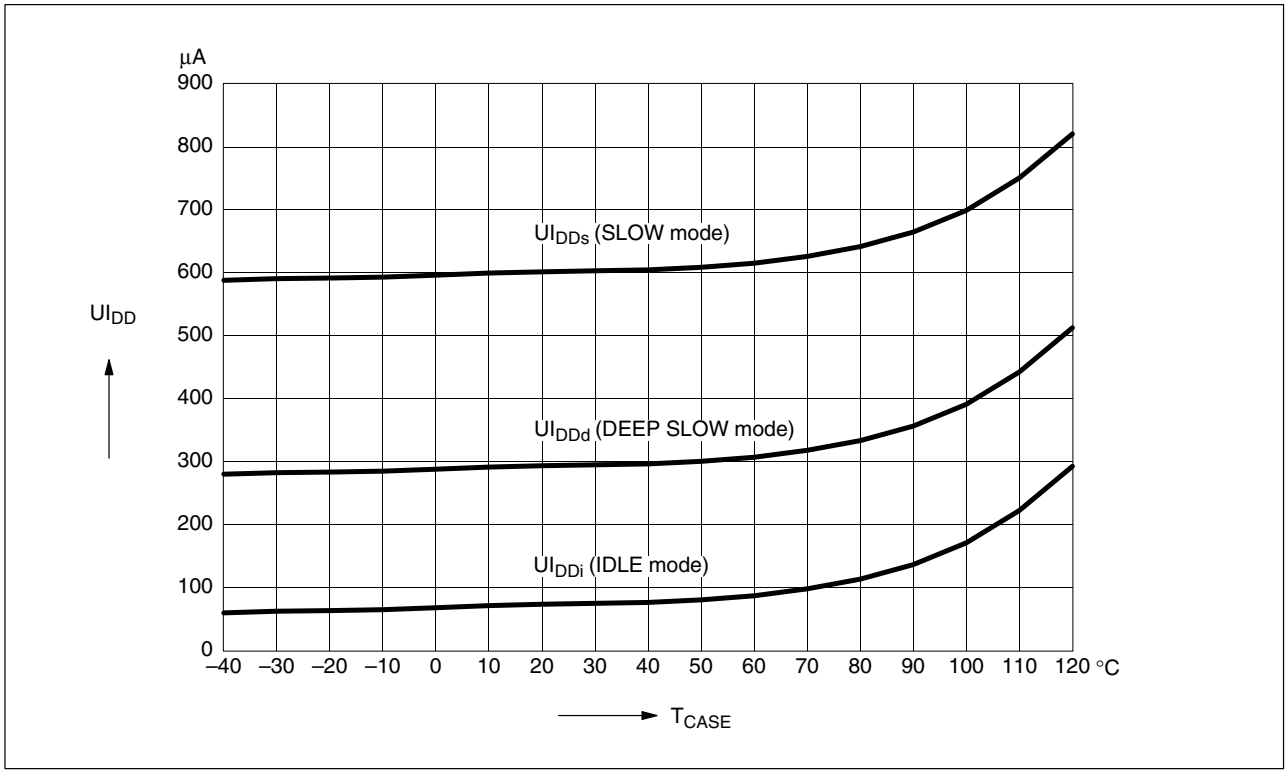


Fig. 3–1: Typical UI_{DD} characteristics over temperature @ f_{XTAL} = 4 MHz, 5 V

3.4. Recommended Quartz Crystal Characteristics

See Chapter 3.4 of document “CDC32xxG-C Automotive Controller - Family User Manual, CDC3205G-C Automotive Controller” (6251-579-1DS).

4. CPU and Clock System

4.1. Recommended Register Settings

Settings for PMF, IOP and WSR differing from those given in Table 4–1 must not be used and may result in undefined behavior. It is required not to operate I/O faster than Flash.

Suppression Strength (SUP) and Clock Tolerance (TOL) may be varied between zero and the values for strong settings according to the rules in Section 4.4.2 of the document “CDC32xxG-C Automotive Controller - Family User Manual, CDC3205G-C Automotive Controller” (6251-579-1DS). The given limits must not be exceeded.

Table 4–1: PLL and ERM modes: Recommended settings and resulting operating frequencies (MHz)

f_{XTAL}	CPU		Flash		I/O		ERMC.EOM = 1						ERMC.EOM = 2 or 3					
							Weak		Normal		Strong		Weak		Normal		Strong	
	f_{SYS}	PLLC. PMF	f_{BUS}	WSR	f_{IO}= f_0	IOC. IOP	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL
4	16	3	8	0x11	8	1	0	8	0	14	0	15	8	4	14	7	22	11
	24	5	8	0x22	8	2	0	12	0	15	0	15	12	6	21	11	31	12
			12	0x11			0	10	0	10	0	10	12	2	21	2	33	2
	32	7	8	0x33	8	3	0	12	0	12	0	12	16	8	28	12	31	12
			10.67	0x22			0	12	0	12	0	12	16	8	19 23 28	9 7 6	19 23 37	9 7 6
	40	9	10	0x33	8	4	0	6	0	6	0	6	21	6	35	6	37	6
	48	11	12	0x33	8	5	0	1	0	1	0	1	25	1	42	1	42	1
5	10	1	10	0x00	10	0	0	5	0	8	0	14	5	3	8	4	14	7
	20	3	10	0x11	10	1	0	10	0	15	0	15	10	5	17	8	28	8
	30	5	10	0x22	10	2	0	14	0	14	0	14	15	8	24 26	12 11	28 30 35	10 9 8
	40	7	10	0x33	10	3	0	6	0	6	0	6	21	6	35	6	37	6
	50	9	12.5	0x33	10	4	set ERMC.EOM=0						set ERMC.EOM=0					

5. Memory and Special Function ROM (SFR) System

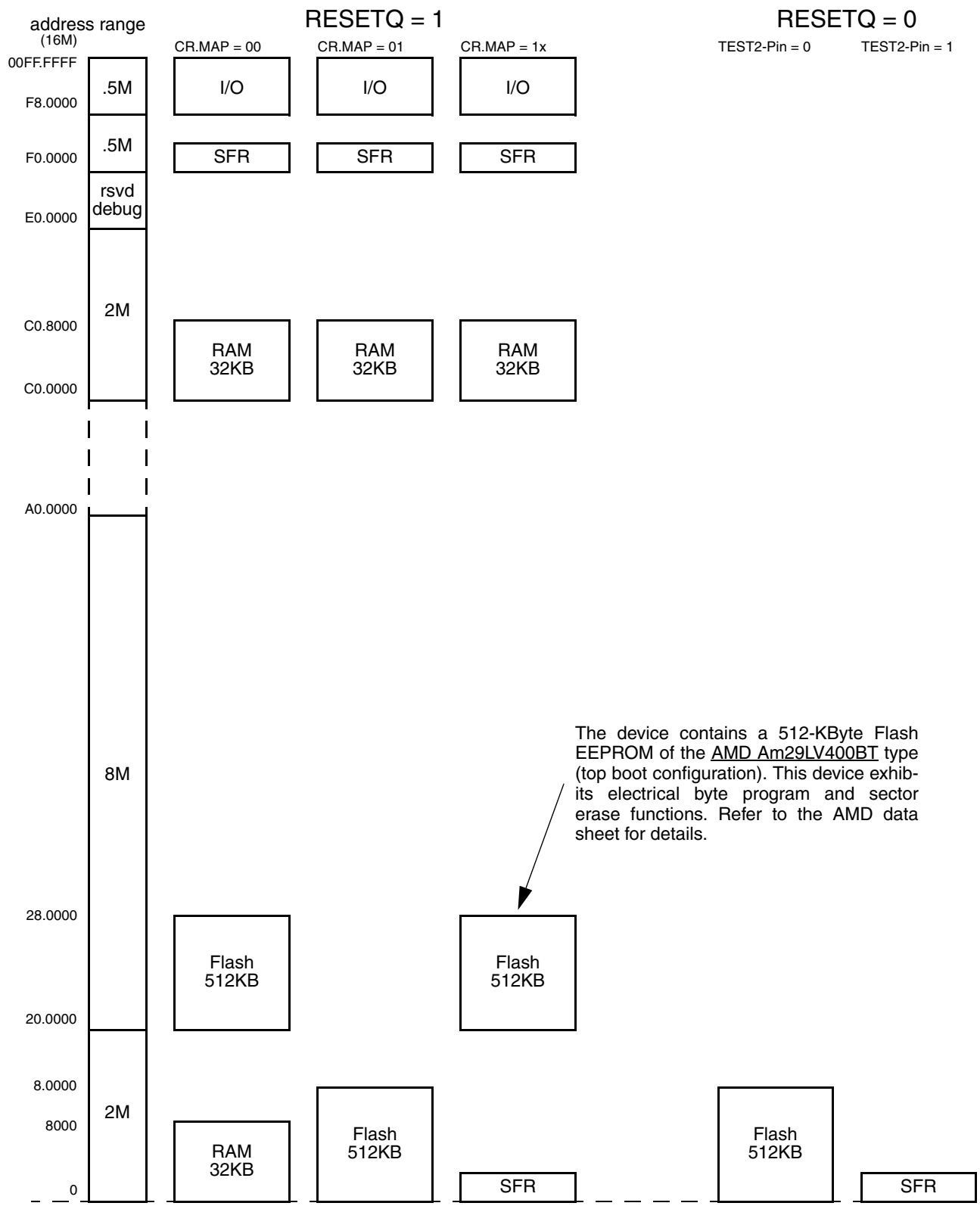


Fig. 5–1: Address map. Most common settings

Warning:

Since only a 24-bit address space is supported, do not use addresses outside this range when debugging this device.

6. Core Logic

6.1. Control Word (CW)

A number of important system configuration properties are selectable during device start-up by means of a unique control word (CW).

6.1.1. Reset Active

At the end of the reset period, the device fetches this CW from address locations 0x20 to 0x23 of a source that is determined by the state of pins TEST and TEST2 and flag MFPLR.MFPL, see Table 6–1 for MCM parts, Table 6–2 for ROM parts.

Table 6–1: CW fetch in MCM parts (QFP128)

"Control Word Fetch" desired from	Necessary Reset Configuration		
	TEST2	TEST	MFPL
Int. Flash	0	0	x
Int. Flash	0	1	1
Ext. via multifunction port			0 [1)]
Int. special-function ROM	1	x	x
[1)] Only available after a non-power-on RESET with MFPL = 0 set before			

As Table 6–1 shows, the device disables external access (through the multifunction port) to internal code, as long as MFPLR.MFPL is 1 (= state after UVDD power-up). Setting it to 0 requires internal SW. By this means, an effective device lock mechanism is implemented, which prevents unauthorized access to internal SW.

In ROM parts, flag MFPLR.MFPL is available, but does not lock the multifunction port. Thus Table 6–1 reduces to Table 6–2.

Table 6–2: CW fetch in ROM parts (QFP128)

"Control Word Fetch" desired from	Necessary Reset config. of pins	
	TEST2	TEST
Internal ROM	0	0
External via multifunction port	0	1
Int. special-function ROM	1	x

6.1.2. Reset Inactive

When exiting Reset, the CW is read and stored in the control register (CR) and the system will start up according to the configuration defined therein.

Normally the CW is fetched from the same memory that the system will start executing code from. Table 6–3 gives fixed CWs for a list of the most commonly used configurations.

Table 6–3: Some common system configurations and the corresponding CW setting

Part Type	"Program Start" desired from	Additional desired properties	Necessary CW	
			31:16	15:0
MCM	int. 16-bit Flash	-	Don't care	0x7F5F
ROM	int. 16-bit ROM	-	Don't care	0x7F5F

7. Hardware Options

7.1. Functional Description

Hardware options are available in several areas to adapt the IC function to the host system requirements. For details see the document “CDC32xxG-C Automotive Controller - Family User Manual, CDC3205G-C Automotive Controller” (6251-579-1DS).

Setting hardware options is carried out in two steps:

1. selection is effected by programming dedicated address locations in the HW options field with the desired options’ code.

2. activation is effected by copying the HW options field to the corresponding HW options’ registers at least once after each reset.

In EMU and MCM devices, all hardware options are software-progammable.

In mask ROM derivatives, the clock options and the watchdog, clock and supply monitors are hard-wired, according to the HW options field of the ROM code hex file. Those options can only be altered by changing a production mask.

To ensure compatible option settings in this IC and mask ROM derivatives when run with the same ROM code, it is mandatory to always write the HW options field to the HW option registers directly after reset.

8. Differences

This chapter describes differences between this document and predecessor document: “CDC3207G-C Automotive Controller Specification“ (6251-589-1PD).

Section	Description
1. Introduction	Table 1-1: devices added
2. Pins	Figure 2-3 changed.
3. Electrical Characteristics	Characteristics: Values changed: R_{thjc}, R_{thja}, UI_{DDp}, UI_{DDf}, UI_{DDi}, AI_{DDa}
4. CPU and Clock System	Table 4-1: entry for f_{XTAL} = 4 MHz, f_{SYS} = 8 MHz deleted Table 4-2: deleted
5. Memory and Special Function ROM System	Figure 5-1: Flash upper hex address corrected Precaution added

9. Data Sheet History

1. Advance Information: “CDC3207G-C V1.0 Automotive Controller Specification”, Feb. 21, 2002, 6251-589-1AI.
First release of the advance information.
Originally created for HW version CDC3207G-C1.

2. Advance Information: “CDC3207G-C V2.0 Automotive Controller Specification”, June 6, 2002, 6251-589-2AI.
Second release of the advance information.
Originally created for HW version CDC3207G-C2.

3. Advance Information: “CDC3207G-C Automotive Controller Specification”, April 15, 2003, 6251-589-3AI.
Third release of the advance information.
Originally created for HW version CDC3207G-C3.

4. Preliminary Data Sheet: “CDC3207G-C Automotive Controller Specification”, June 12, 2003, 6251-589-1PD.
First release of the preliminary data sheet.
Originally created for HW version CDC3207G-C3.

5. Data Sheet: “CDC3207G-C3 Automotive Controller Specification”, Feb. 10, 2005, 6251-589-1DS.
First release of the data sheet.
Originally created for HW version CDC3207G-C3.

Micronas GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@micronas.com
Internet: www.micronas.com

Printed in Germany
Order No. 6251-589-1DS