

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SSU40n01 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .

FEATURES

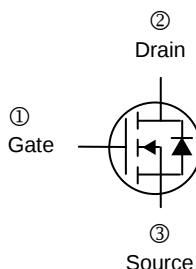
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS and 100% Rg Guaranteed
- Green Device Available

MARKING

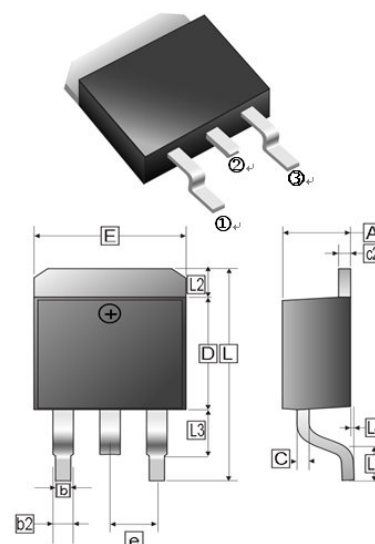


PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-263	0.8K	13 inch



TO-263



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.40	4.80	c2	1.17	1.45
b	0.76	1.00	b2	1.1	1.47
L4	0.00	0.30	D	8.5	9.0
c	0.36	0.5	e	2.54	REF
L3	1.50	REF	L	14.6	15.8
L1	2.29	2.79	θ	0°	8°
E	9.80	10.4	L2	1.27	REF

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C=25^\circ\text{C}$	I_D	149	A
	$T_C=70^\circ\text{C}$		119	
	$T_A=25^\circ\text{C}$		30	
	$T_A=70^\circ\text{C}$		24	
Pulsed Drain Current ¹		I_{DM}	480	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	83	W
	$T_A=25^\circ\text{C}$		2	
Single Pulse Avalanche Energy, $L=0.1\text{mH}$		E_{AS}	201	mJ
Single Pulse Avalanche Current, $L=0.1\text{mH}$		I_{AS}	63.5	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient ²		$R_{\theta JA}$	62	$^\circ\text{C} / \text{W}$
Maximum Thermal Resistance Junction-Case ²		$R_{\theta JC}$	1.5	$^\circ\text{C} / \text{W}$

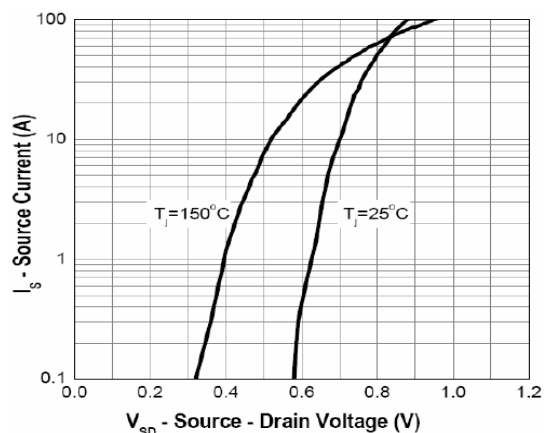
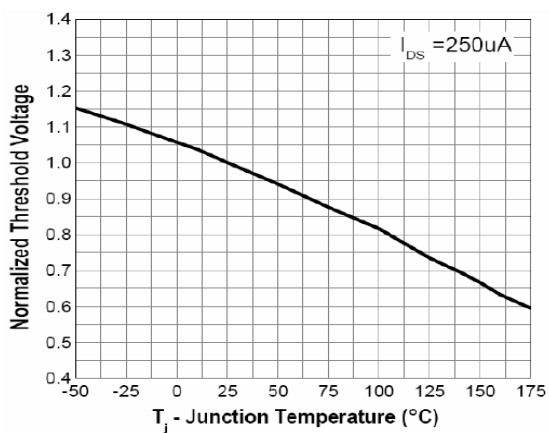
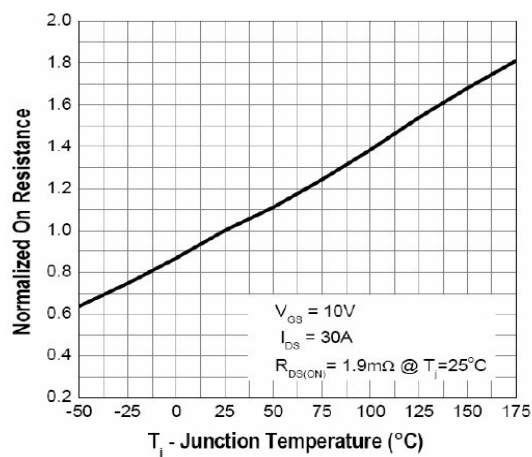
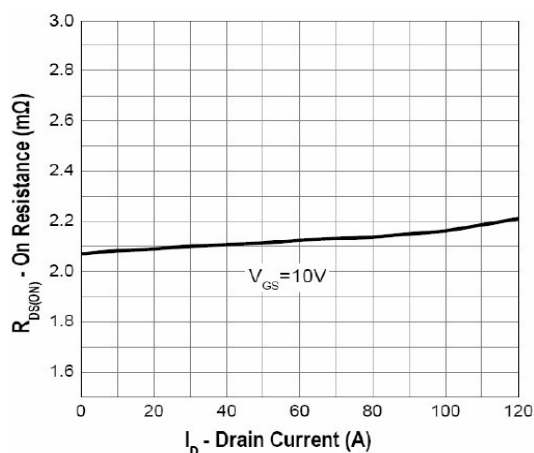
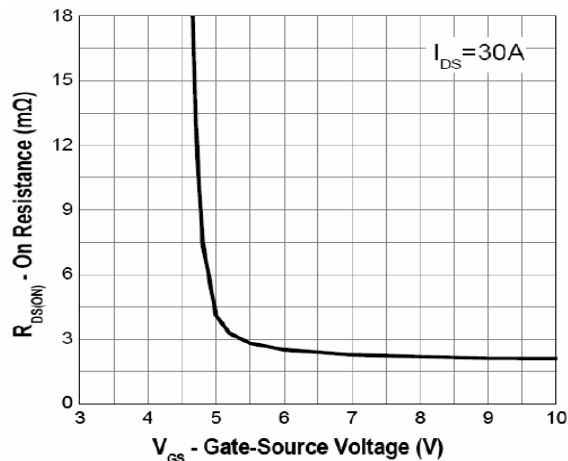
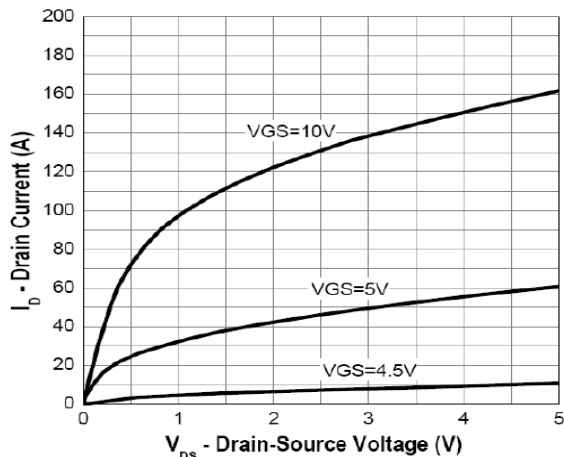
ELECTRICAL CHARACTERISTICS ($T_J=25^\circ C$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	40	-	-	V	V _{GS} =0, I _D =250μA
Gate-Threshold Voltage	V _{GS(th)}	2	3	4	V	V _{DS} =V _{GS} , I _D =250μA
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current	I _{DSS}	-	-	1	μA	V _{DS} =32V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	1.9	2.2	mΩ	V _{GS} =10V, I _D =30A
Total Gate Charge	Q _g	-	78.8	-	nC	I _D =30A V _{DS} =20V V _{GS} =10V
Gate-Source Charge	Q _{gs}	-	23	-		
Gate-Drain (“Miller”) Change	Q _{gd}	-	4.85	-		
Turn-on Delay Time	T _{d(on)}	-	21	-	nS	V _{DS} =20V I _D =30A V _{GS} =10V R _G =3Ω
Rise Time	T _r	-	6	-		
Turn-off Delay Time	T _{d(off)}	-	98	-		
Fall Time	T _f	-	17	-		
Input Capacitance	C _{iss}	-	4222	-	pF	V _{GS} =0 V _{DS} =20V f=1.0MHz
Output Capacitance	C _{oss}	-	889	-		
Reverse Transfer Capacitance	C _{rss}	-	398	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy ³	EAS	110	-	-	mJ	V _{DD} =20V,L=0.1mH , I _{AS} =47A
Source-Drain Diode						
Diode Forward Voltage	V _{SD}	-	-	1.3	V	I _S =30A, V _{GS} =0
Reverse Recovery Time	T _{rr}	-	32	-	ns	I _F =30A, T _J = 25℃
Reverse Recovery Charge	Q _{rr}	-	120	-	nC	dI/dt=100A/μs

Notes:

- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.
- The Min. value is 100% EAS tested guarantee

CHARACTERISTIC CURVES



CHARACTERISTIC CURVES

