



SPP2323

Dual P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2323 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss, and resistance to transients are needed.

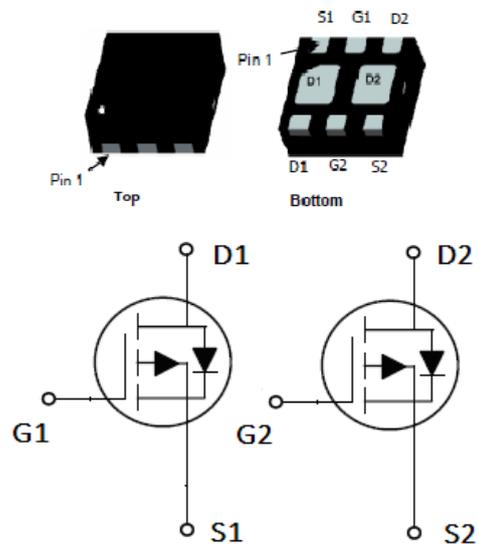
FEATURES

- -20V/-3.3A, $R_{DS(ON)}=65m\Omega @ V_{GS}=-4.5V$
- -20V/-2.8A, $R_{DS(ON)}=85m\Omega @ V_{GS}=-2.5V$
- -20V/-2.3A, $R_{DS(ON)}=130m\Omega @ V_{GS}=-1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TDFN2x2-6L package design

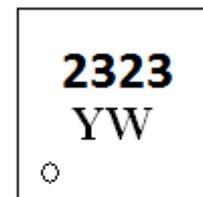
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION (TDFN2x2-6L)



PART MARKING



Y : Year Code
W: Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	D2	Drain 2
4	S2	Source 2
5	G2	Gate 2
6	D1	Drain1
Exposed Backside Metal	D1/D2	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2323TDN6RGB	TDFN2x2-6L	2323

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP2323TDN6RGB : Tape Reel ; Pb – Free ; Halogen -Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate –Source Voltage	V_{GSS}	± 10	V
Continuous Drain Current($T_J=150^{\circ}\text{C}$)	I_D	$T_A=25^{\circ}\text{C}$	-4.0
		$T_A=100^{\circ}\text{C}$	-2.8
Pulsed Drain Current	I_{DM}	-16	A
Continuous Source Current(Diode Conduction)	I_S	-1.6	A
Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	1.9
		$T_A=70^{\circ}\text{C}$	1.2
Operating Junction Temperature	T_J	-55/150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	$T \leq 5\text{sec}$	65
		Steady State	95



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.3		-1.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 10V$			-10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$			-1	μA
		$V_{DS}=-16V, V_{GS}=0V, T_J=125^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -4.5V, V_{GS}=-5V$	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-3.3A$		45	65	$m\Omega$
		$V_{GS}=-2.5V, I_D=-2.8A$		60	85	
		$V_{GS}=-1.8V, I_D=-2.3A$		90	130	
		$V_{GS}=-1.5V, I_D=-1A$		100	140	
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-1A$		2.2		S
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$			-1	V
Dynamic						
Input Capacitance	C_{iss}	$V_{DS}=-10V, V_{GS}=0V, F=1MHz$		515	745	pF
Output Capacitance	C_{oss}			55	80	
Reverse Transfer Capacitance	C_{rss}			20	30	
Total Gate Charge	Q_g	$V_{DS}=-10V, V_{GS}=-4.5V, I_D=-3A$		6.4		nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-1A$ $V_{GEN}=-4.5V, R_G=25\Omega$		5.0		nS
	t_r			17.4		
Turn-Off Time	$t_{d(off)}$			40.7		
	t_f			11.4		



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TYPICAL CHARACTERISTICS

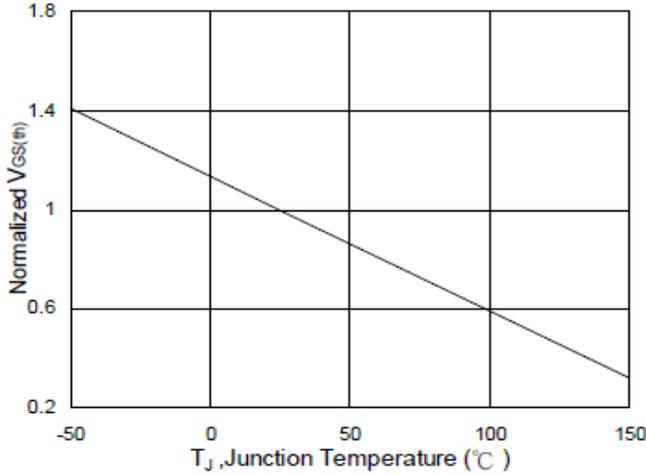


Fig. 1 Normalized $V_{GS(th)}$ vs. Temp

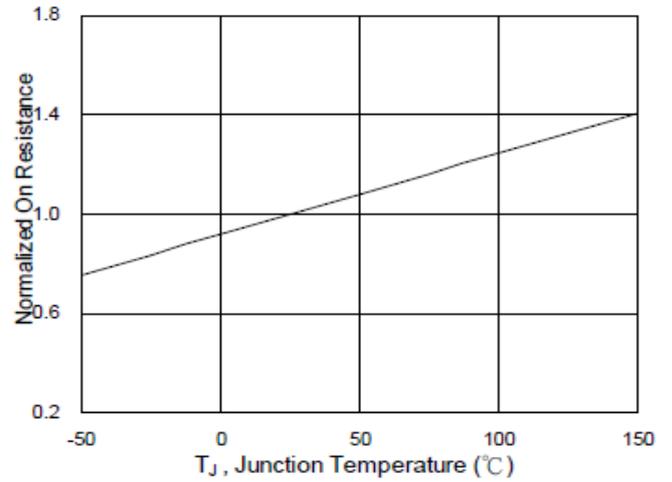


Fig. 2 Normalized On-Resistance vs. Temp

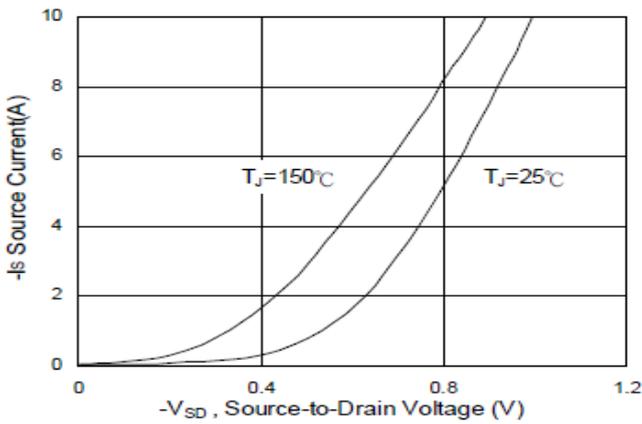


Fig. 3 Output Characteristics

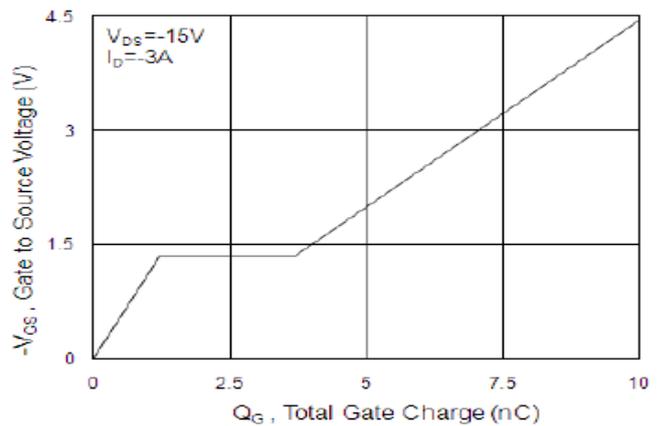


Fig. 4 Gate Charge Characteristics

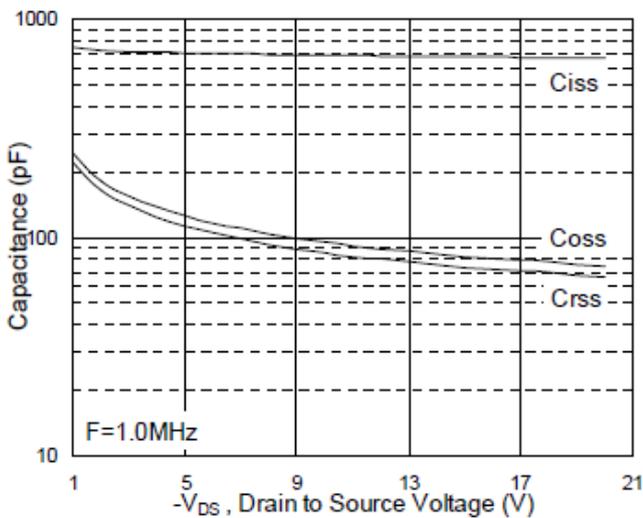


Fig 5 Capacitance vs. Drain Voltage

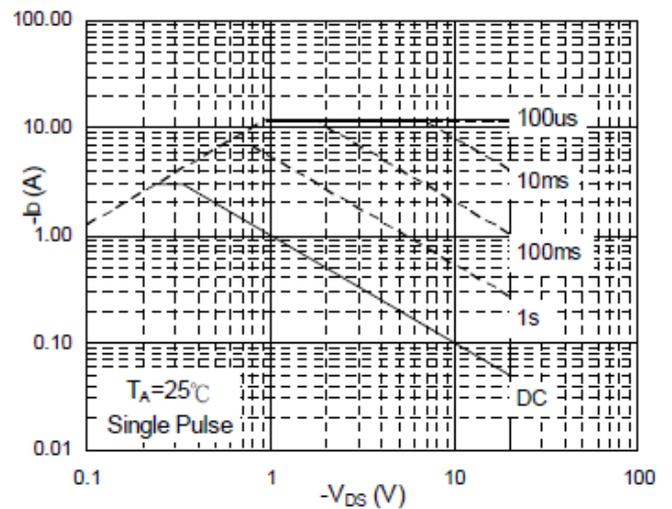


Fig. 6 Safe Operation Area



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