



SPP6241

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP6241 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

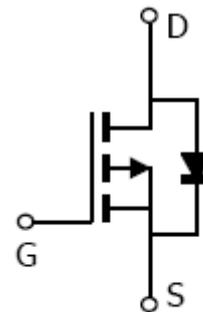
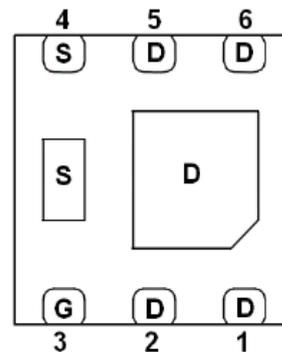
FEATURES

- ◆ -20V/-3.3A, $R_{DS(ON)}=45m\Omega@V_{GS}=-4.5V$
- ◆ -20V/-2.8A, $R_{DS(ON)}=55m\Omega@V_{GS}=-2.5V$
- ◆ -20V/-2.3A, $R_{DS(ON)}=65m\Omega@V_{GS}=-1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ UDFN2x2-6L package design

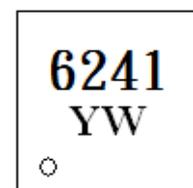
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(UDFN2x2-6L)



PART MARKING



Y : Year Code
W: Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP6241UDN6RGB	UDFN2x2-6L	6241

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPP6241UDN6RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-20	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-4.3	A
		TA=70°C	-3.8	
Pulsed Drain Current*	I _{DM}	-30	A	
Continuous Source Current(Diode Conduction)	I _S	-1.6	A	
Power Dissipation	P _D	TA=25°C	1.9	W
		TA=70°C	1.2	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	65	°C/W	

*Junction temperature limited.



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ELECTRICAL CHARACTERISTICS (T_A=25°C Unless otherwise noted)

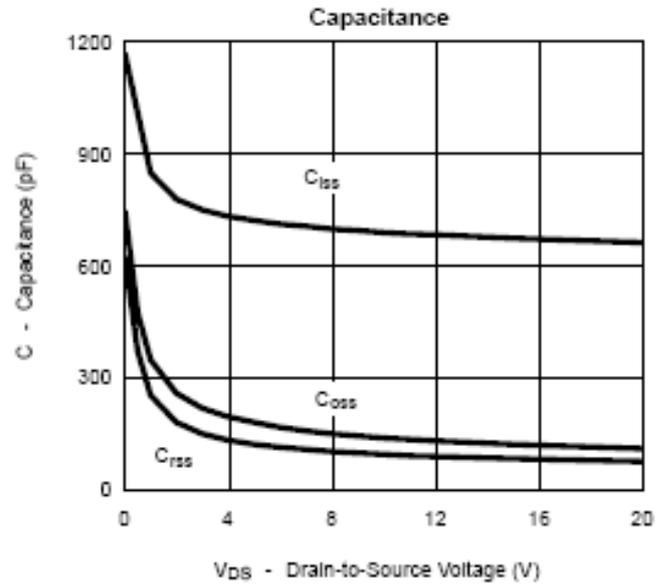
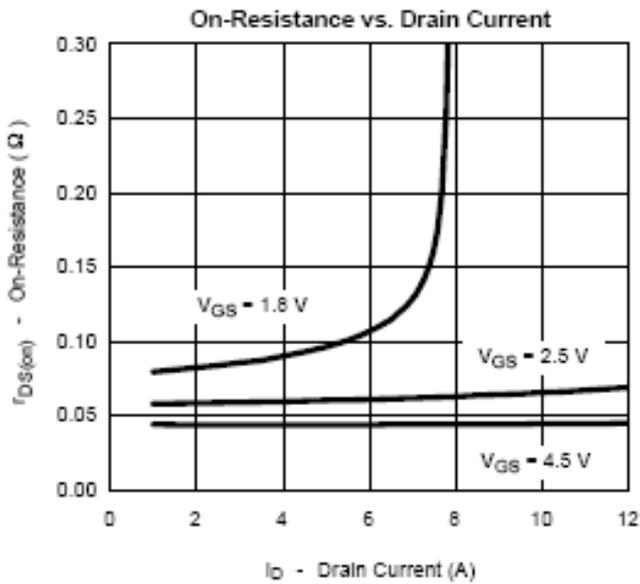
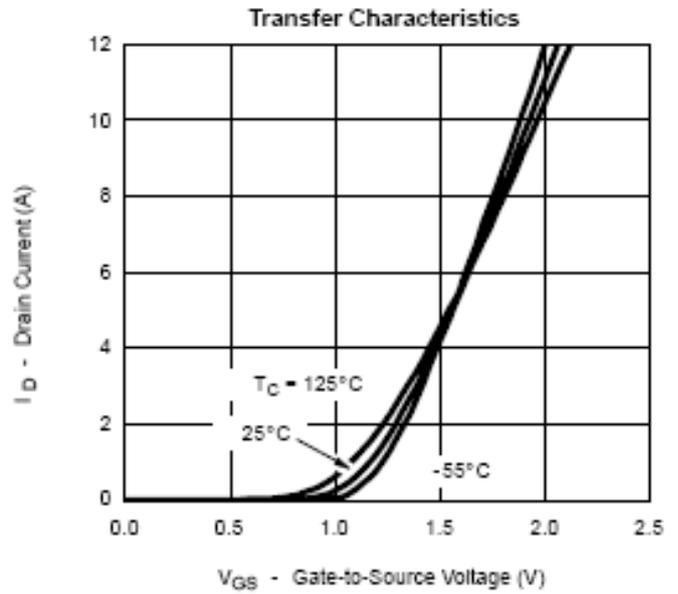
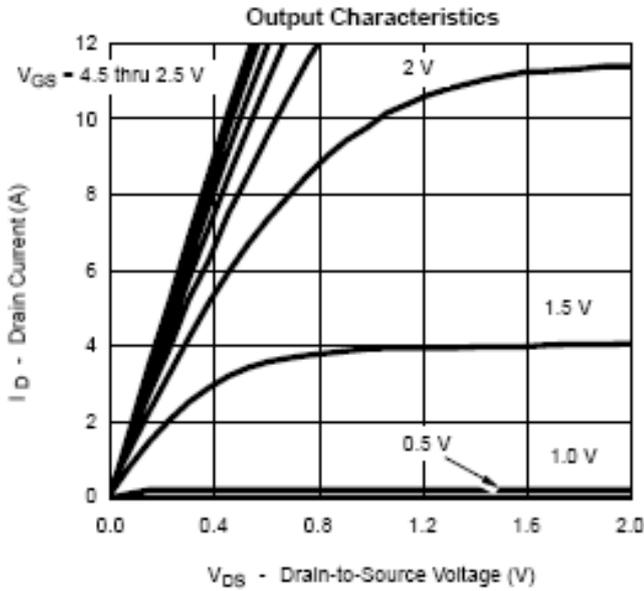
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.35		-0.9	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	uA
		V _{DS} =-20V, V _{GS} =0V T _J =55°C			-10	
On-State Drain Current	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} =-4.5V	-6			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-3.3A		0.036	0.045	Ω
		V _{GS} =-2.5V, I _D =-2.8A		0.045	0.055	
		V _{GS} =-1.8V, I _D =-2.3A		0.055	0.065	
Forward Transconductance	g _{fs}	V _{DS} =-5.0V, I _D =-3.3A		3		S
Diode Forward Voltage	V _{SD}	I _S =-1.6A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-6V, V _{GS} =-4.5V I _D =-3.3A		8	13	nC
Gate-Source Charge	Q _{gs}			1.2		
Gate-Drain Charge	Q _{gd}			2.2		
Input Capacitance	C _{iss}	V _{DS} =-6V, V _{GS} =0V f=1MHz		700		pF
Output Capacitance	C _{oss}			160		
Reverse Transfer Capacitance	C _{rss}			120		
Turn-On Time	t _{d(on)}	V _{DD} =-6V, R _L =6Ω I _D =-1.0A, V _{GEN} =-4.5V R _G =6Ω		15	25	nS
	t _r			35	55	
Turn-Off Time	t _{d(off)}			60	90	
	t _f			40	60	



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TYPICAL CHARACTERISTICS

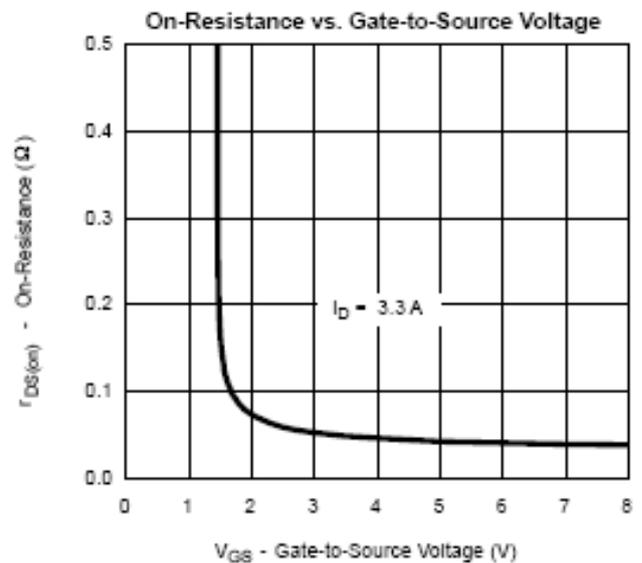
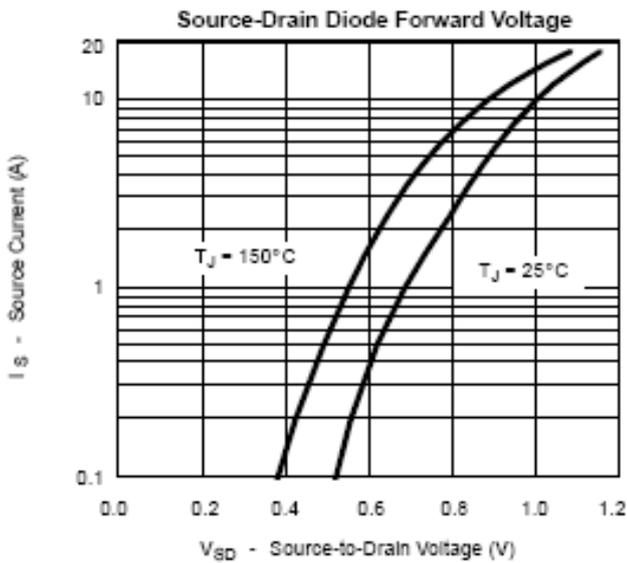
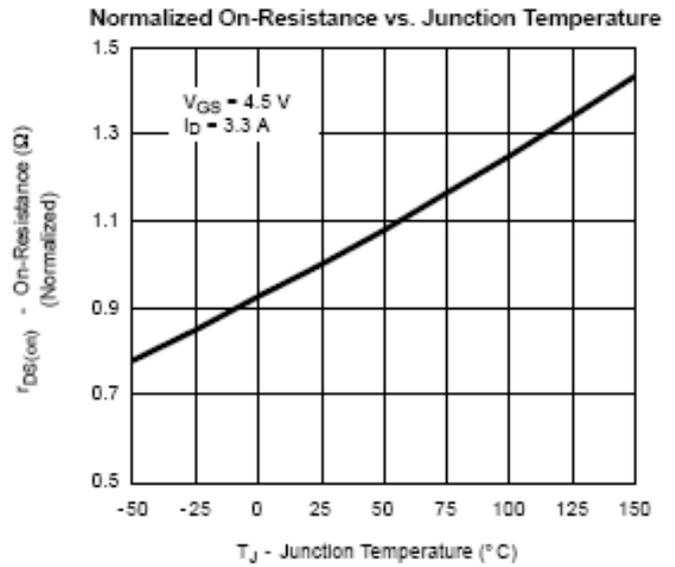
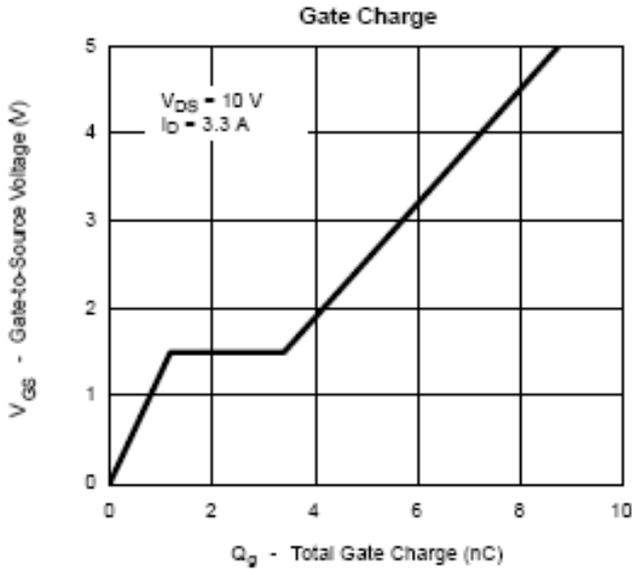




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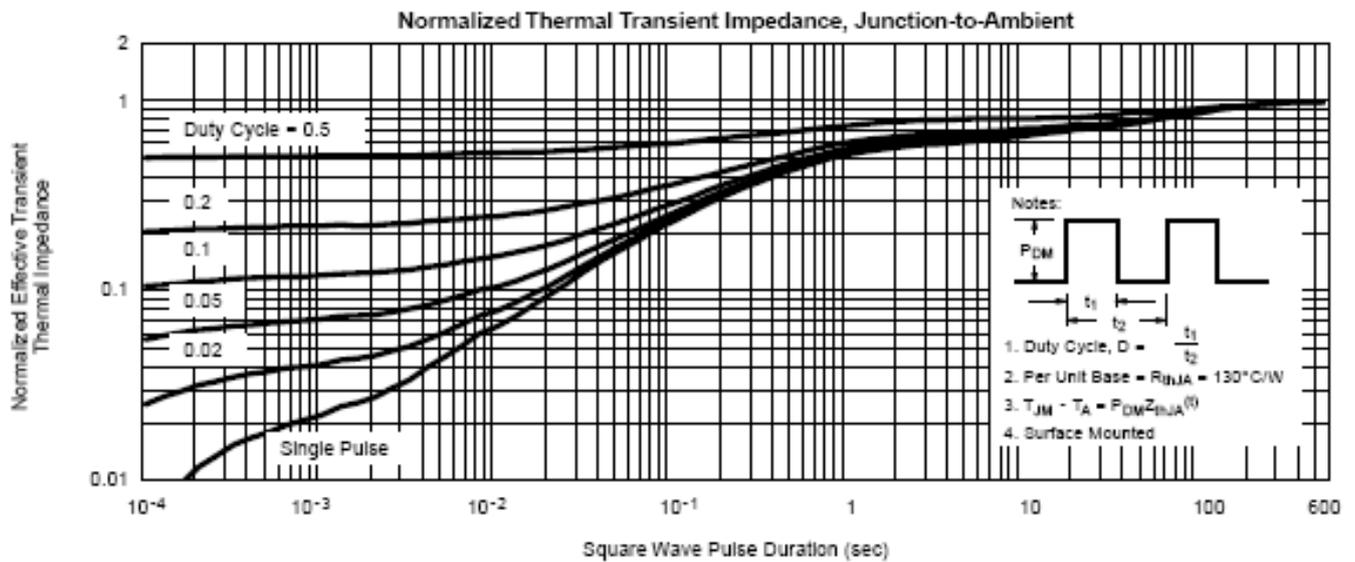
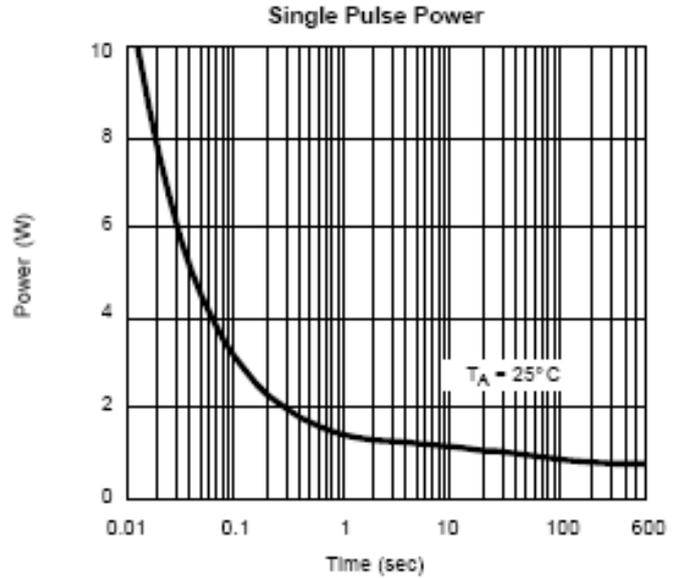
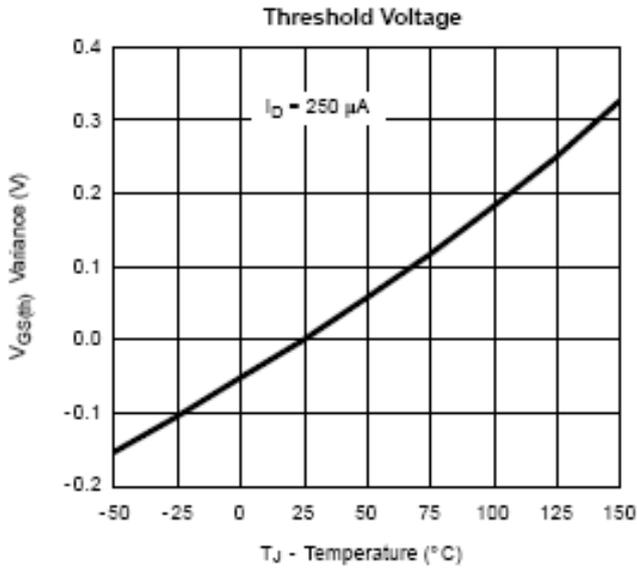
TYPICAL CHARACTERISTICS





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TYPICAL CHARACTERISTICS





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