

FEATURES

- ☐ 100% EAS Test
- ☐ Super high density cell design
- ☐ Extremely Low Intrinsic Capacitances
- ☐ Remarkable Switching Characteristics
- ☐ Extended Safe Operating Area
- ☐ Lower $R_{DS(on)}$: 8.2 mΩ (Typ.) @ $V_{GS}=10V$

APPLICATION

- ☐ DC Motor control for E-bike & Power tools
- ☐ Amplifier and car booster
- ☐ Load Switch
- ☐ DC-DC converters

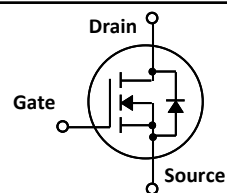
PFP15T110 / PFB15T110

150V N-Channel MOSFET

$$BV_{DSS} = 150\text{ V}$$

$$R_{DS(on)} = 8.2\text{ m}\Omega$$

$$I_D = 110\text{ A}$$



TO-220



1.Gate 2. Drain 3. Source

D2-PAK



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

$T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	150	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ($T_C = 25^\circ\text{C}$)	110	A
	Continuous Drain Current ($T_C = 100^\circ\text{C}$)	93	A
I_{DM}	Pulsed Drain Current	440	A
E_{AS}	Single Pulsed Avalanche Energy	1296	mJ
P_D	Maximum Power Dissipation ($T_C = 25^\circ\text{C}$)	320	W
	Maximum Power Dissipation ($T_C = 70^\circ\text{C}$)	223	W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.47	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Package Marking and Ordering Information

Marking	Device	Package	Remark
NCEP15T11	PFP15T110	TO-220	RoHS
NCEP15T11D	PFB15T110	TO-263(D2-PAK)	RoHS

Electrical Characteristics $T_c=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(ON)}$	Drain-Source On-Static Resistance	$V_{GS} = 10\text{ V}, I_D = 55\text{ A}, T_c = 25\text{ }^{\circ}\text{C}$	--	8.2	9.0	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 55\text{ A}$	70	-	-	V

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
V_{SD}	Diode Forward Voltage	$I_S = 110\text{ A}, V_{GS} = 0\text{ V}$	--	--	1.2	V

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}, f=1.0\text{ MHz}$	--	5500	--	pF
C_{oss}	Output Capacitance		--	540	--	pF
C_{rss}	Reverse Transfer Capacitance		--	5	--	pF

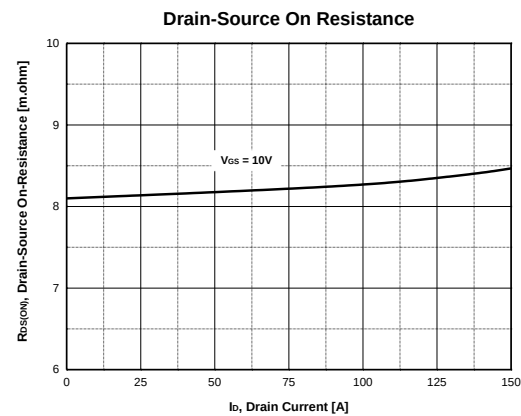
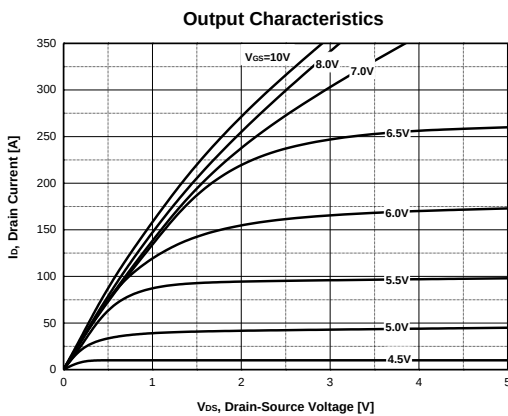
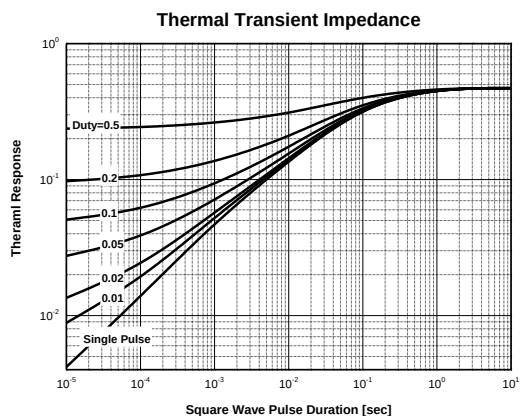
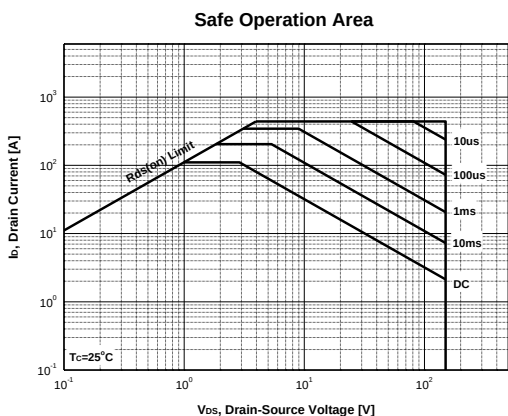
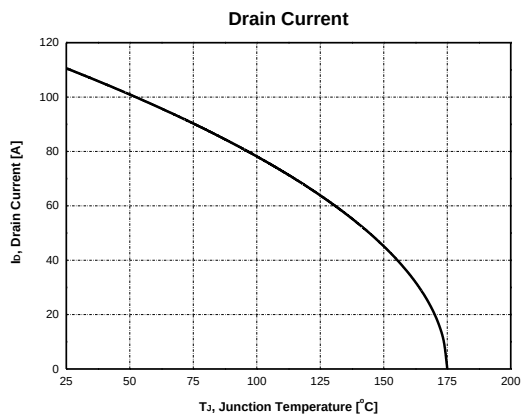
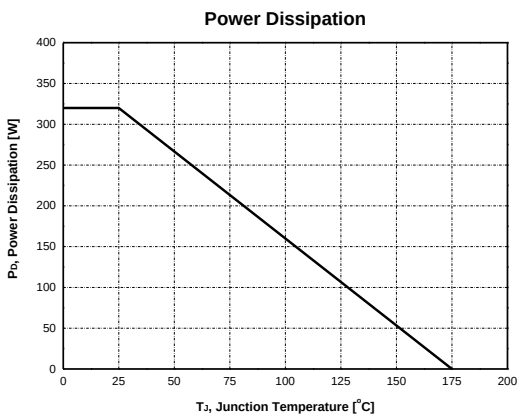
Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DD} = 75\text{ V}, I_D = 55\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 4.7\text{ }\Omega$	--	25	--	ns
t_r	Turn-On Rise Time		--	35	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	46	--	ns
t_f	Turn-Off Fall Time		--	14	--	ns
Q_g	Total Gate Charge	$V_{DS}=75\text{ V}, I_D=55\text{ A}, V_{GS}=10\text{ V}$	--	74	--	nC
Q_{gs}	Gate-Source Charge		--	32	--	nC
Q_{gd}	Gate-Drain Charge		--	7.3	--	nC

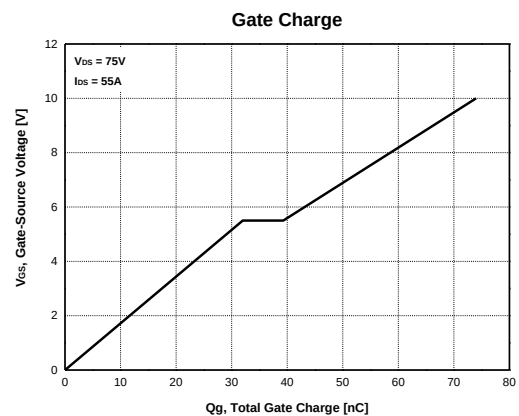
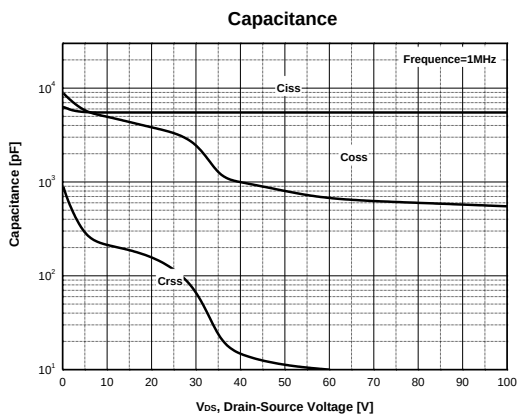
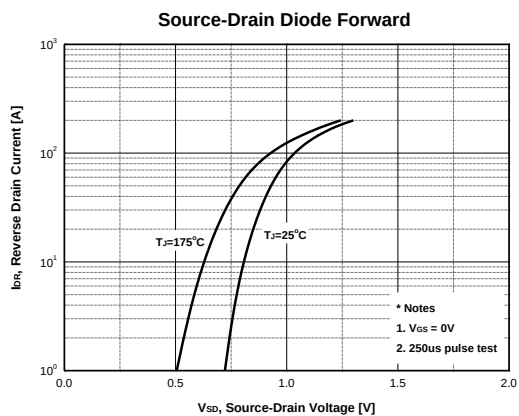
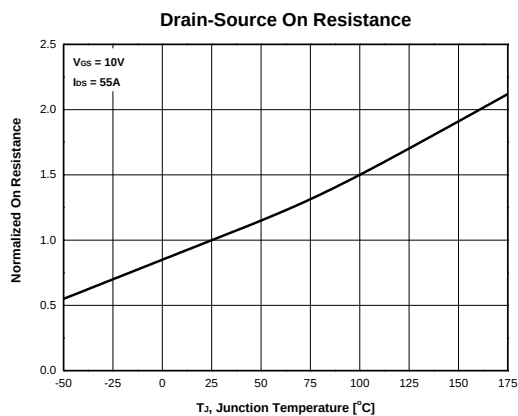
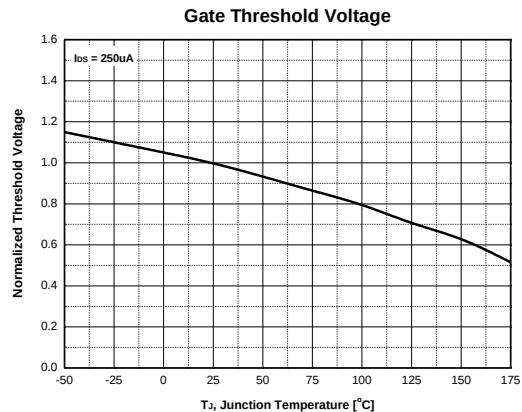
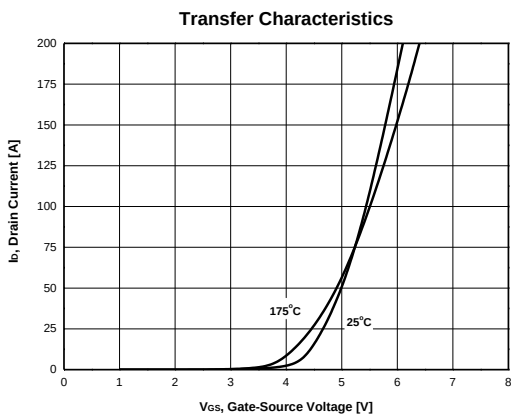
Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L=0.5\text{ mH}, I_{AS}=110, V_{DD}=50\text{ V}, R_G=25\text{ }\Omega$, Starting $T_J=25\text{ }^{\circ}\text{C}$
3. Pulse Test : Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature

Typical Characteristics



Typical Characteristics (continued)



Characteristics Test Circuit & Waveform

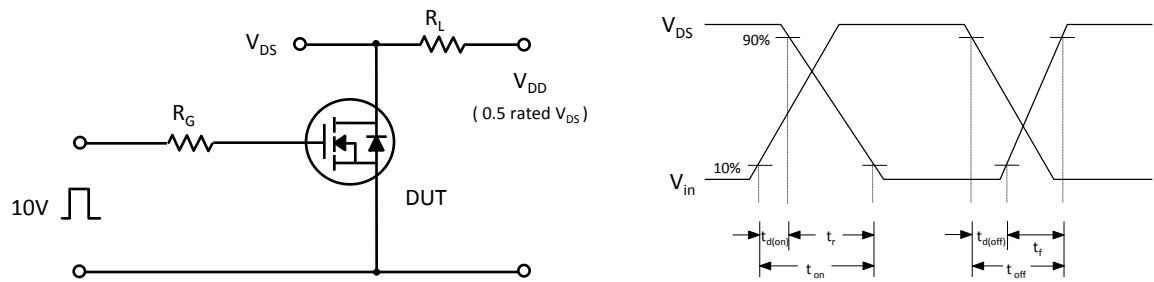


Fig 14. Resistive Switching Test Circuit & Waveforms

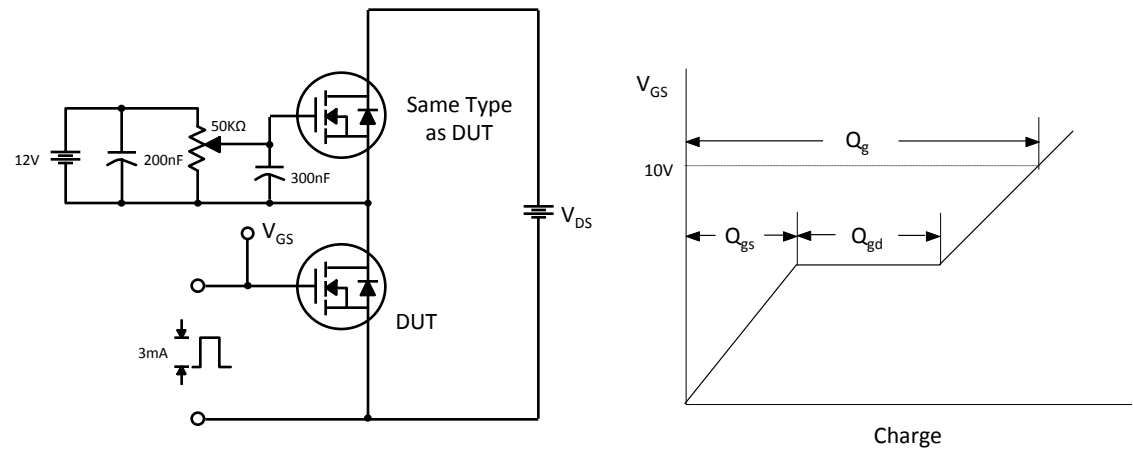


Fig 15. Gate Charge Test Circuit & Waveform

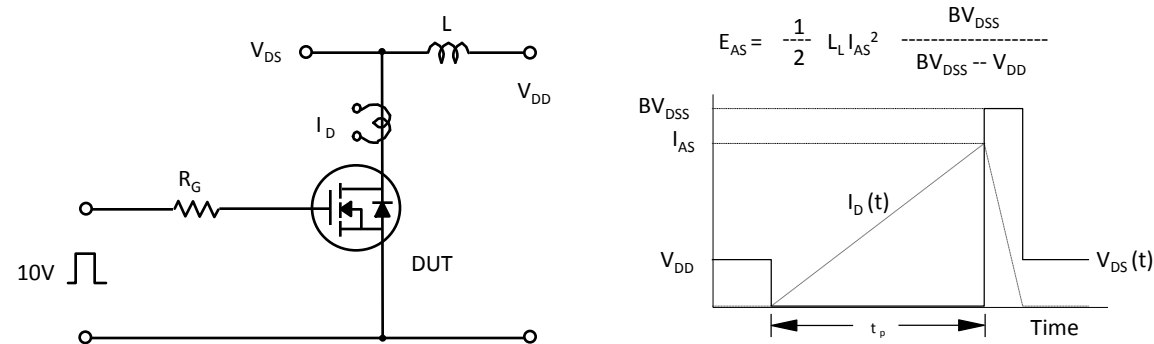


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms

Characteristics Test Circuit & Waveform (continued)

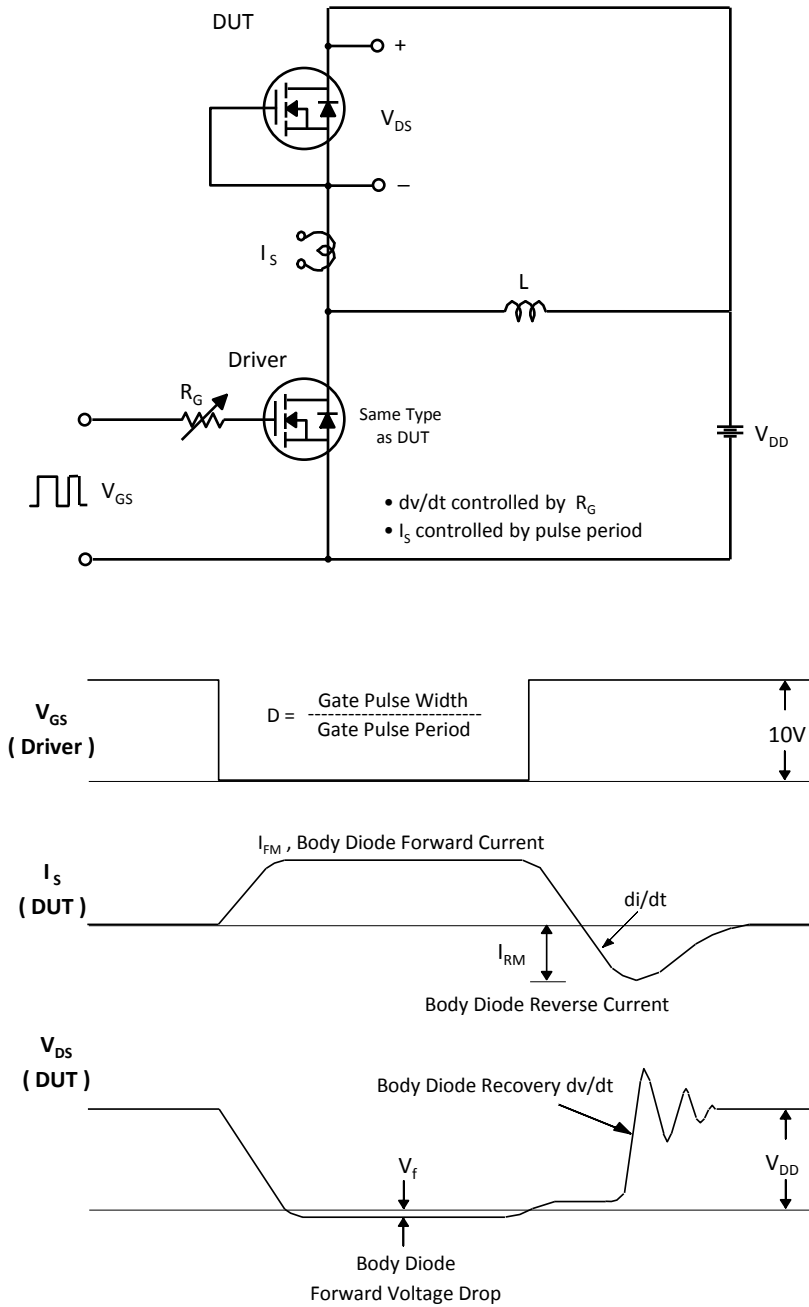


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms