

PFP110N10S/PFB110N10S 100V N-Channel MOSFET

FEATURES

- ❑ 100% EAS Test
- ❑ Super high density cell design
- ❑ Extremely Low Intrinsic Capacitances
- ❑ Remarkable Switching Characteristics
- ❑ Extended Safe Operating Area
- ❑ Lower $R_{DS(ON)}$: 6.5 m Ω (Typ.) @ $V_{GS}=10V$

APPLICATION

- ❑ DC Motor control for E-bike & Power tools
- ❑ Amplifier and car booster
- ❑ Load Switch
- ❑ DC-DC converters

$BV_{DSS} = 100\text{ V}$ $R_{DS(on)} = 6.5\text{ m}\Omega$ $I_D = 117\text{ A}$	
TO-220 1.Gate 2. Drain 3. Source	D2-PAK 1.Gate 2. Drain 3. Source

Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current ($T_C = 25^\circ\text{C}$)	117	A
	Continuous Drain Current ($T_C = 100^\circ\text{C}$)	83	A
I_{DM}	Pulsed Drain Current	468	A
E_{AS}	Single Pulsed Avalanche Energy	684	mJ
P_D	Maximum Power Dissipation ($T_C = 25^\circ\text{C}$)	217	W
	Maximum Power Dissipation ($T_C = 70^\circ\text{C}$)	152	W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.69	$^\circ\text{C/W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Electrical Characteristics $T_C=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}, T_C=25\text{ }^\circ\text{C}$ $T_C=125\text{ }^\circ\text{C}$	--	6.5 11.3	7.2 12.6	m Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
V_{SD}	Diode Forward Voltage	$I_S = 80\text{ A}, V_{GS} = 0\text{ V}$	--	--	1.3	V

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, f=1.0\text{ MHz}$	--	6140	--	pF
C_{oss}	Output Capacitance		--	940	--	pF
C_{riss}	Reverse Transfer Capacitance		--	450	--	pF
R_g	Gate Resistance	$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, f=1.0\text{ MHz}$	--	1.7	--	Ω

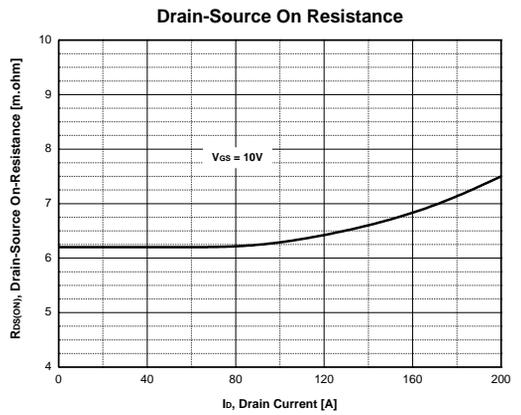
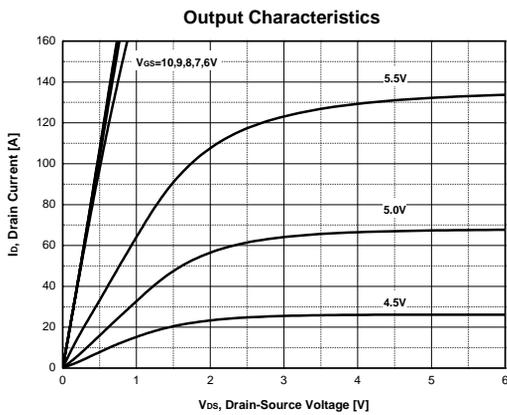
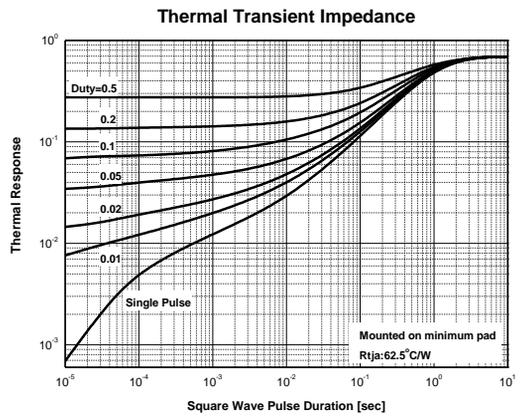
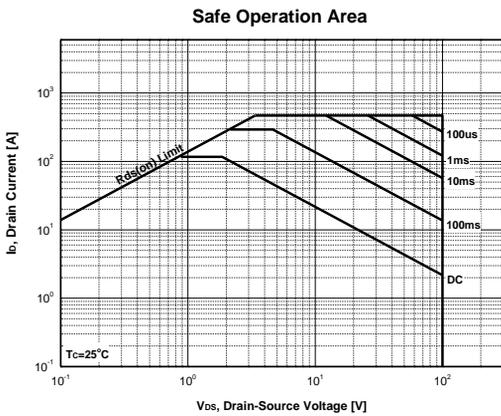
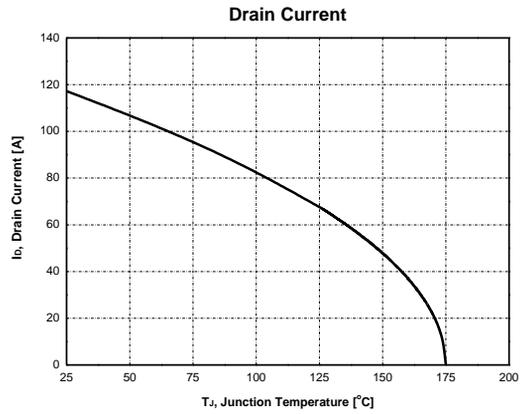
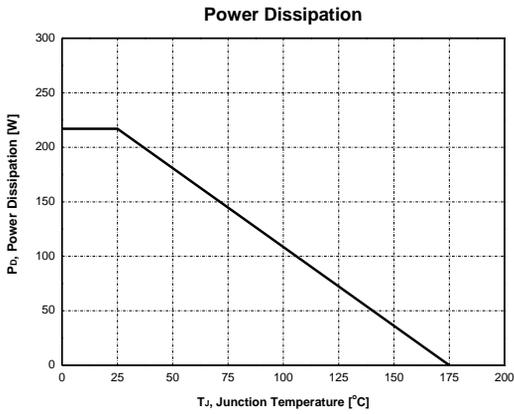
Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 50\text{ V}, R_G = 6\Omega$ $I_D = 80\text{ A}, V_{GS} = 10\text{ V}$	--	23	--	ns
t_r	Turn-On Rise Time		--	39	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	86	--	ns
t_f	Turn-Off Fall Time		--	46	--	ns
Q_g	Total Gate Charge	$V_{DS}=80\text{ V}, I_D=80\text{ A}, V_{GS}=10\text{ V}$	--	130	--	nC
Q_{gs}	Gate-Source Charge		--	25	--	nC
Q_{gd}	Gate-Drain Charge		--	32	--	nC

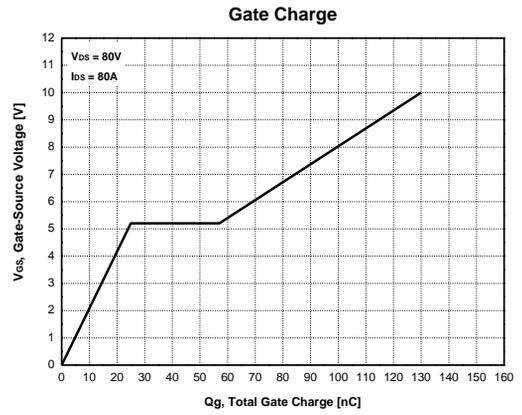
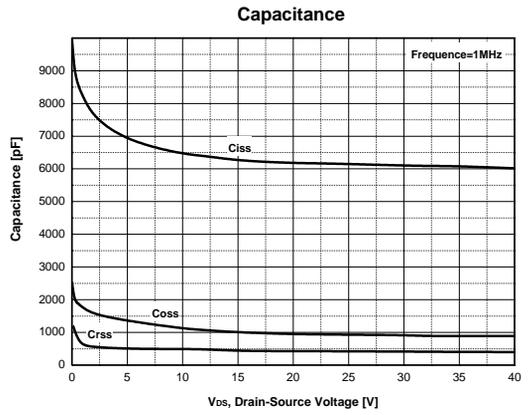
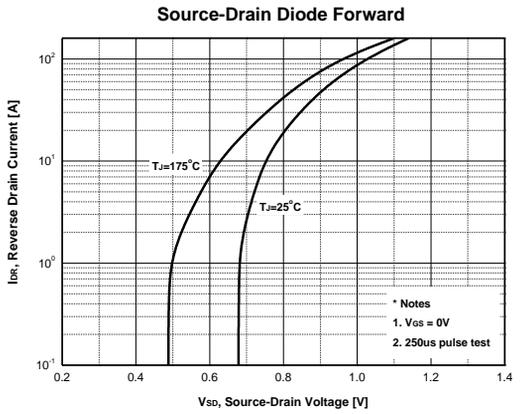
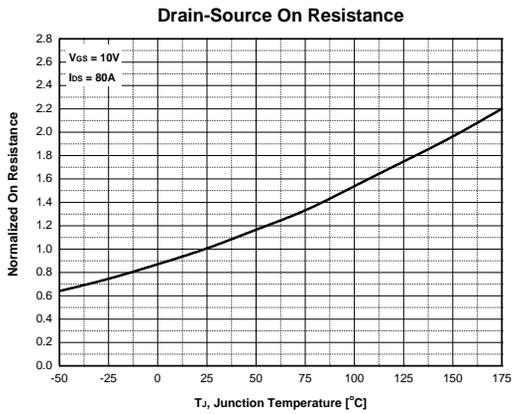
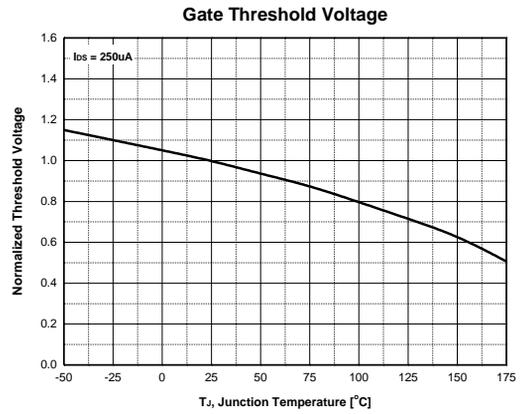
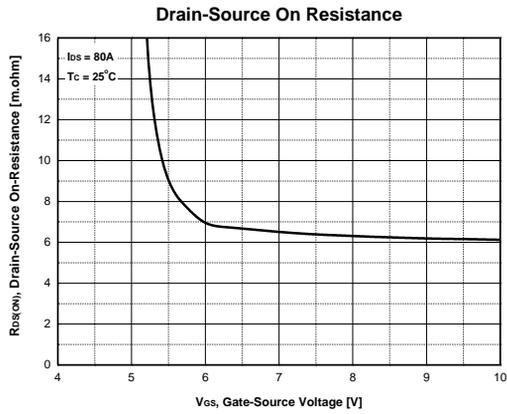
Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L=0.1\text{ mH}, I_{AS}=117, V_{DD}=50\text{ V}, R_G=25\Omega$, Starting $T_J=25\text{ }^\circ\text{C}$
3. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature

Typical Characteristics



Typical Characteristics (continued)



Characteristics Test Circuit & Waveform

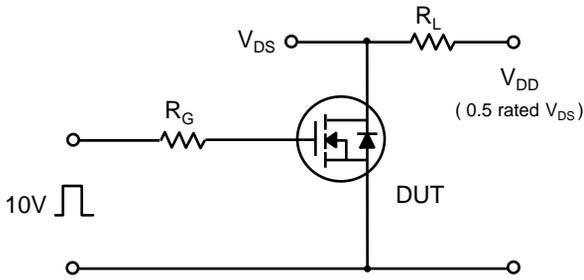


Fig 14. Resistive Switching Test Circuit & Waveforms

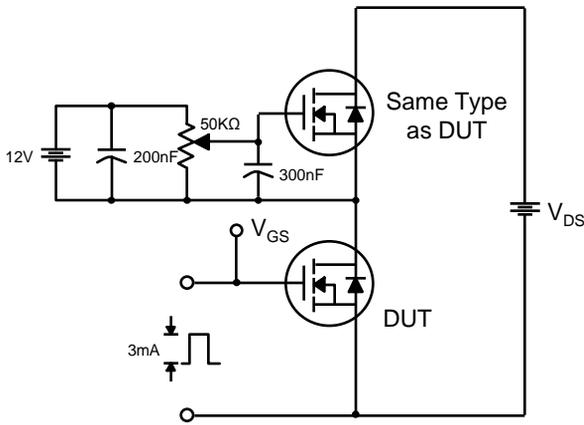


Fig 15. Gate Charge Test Circuit & Waveform

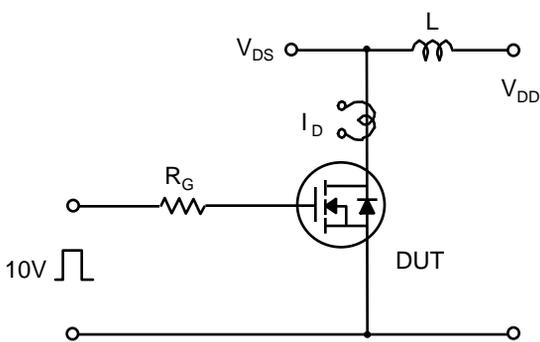
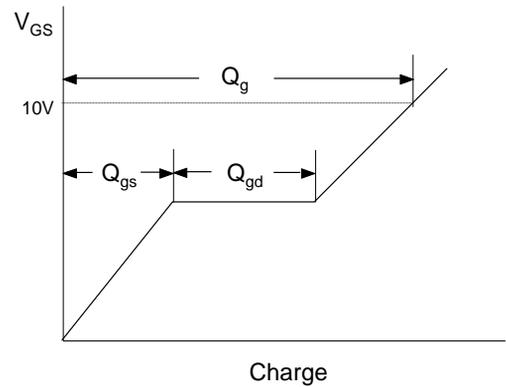
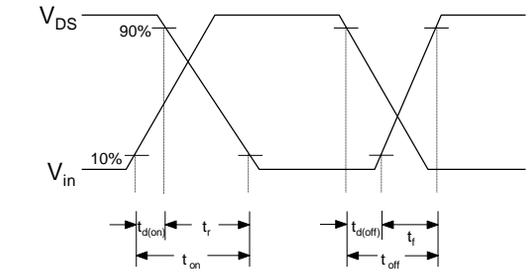
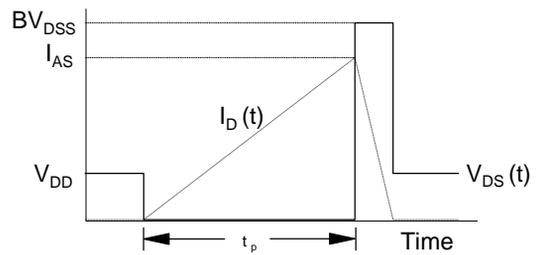


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Characteristics Test Circuit & Waveform (continued)

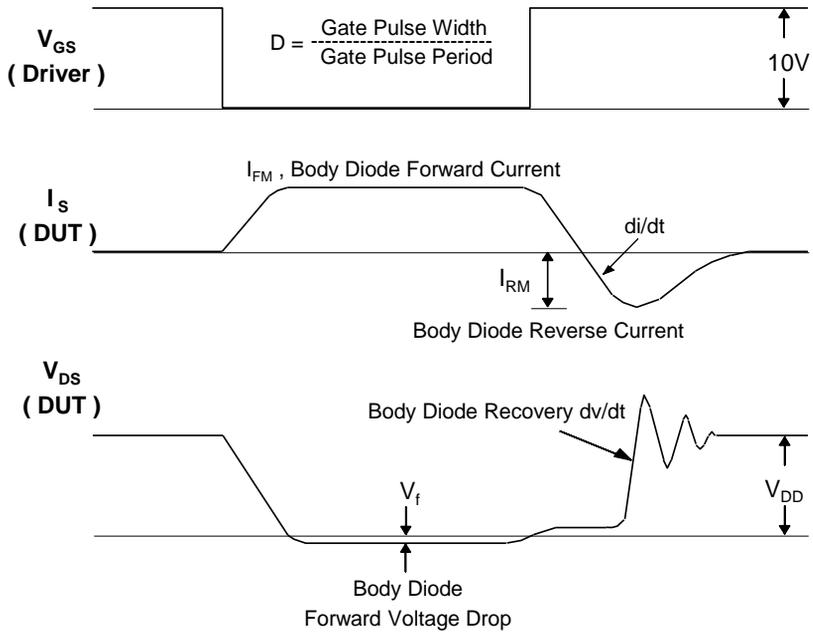
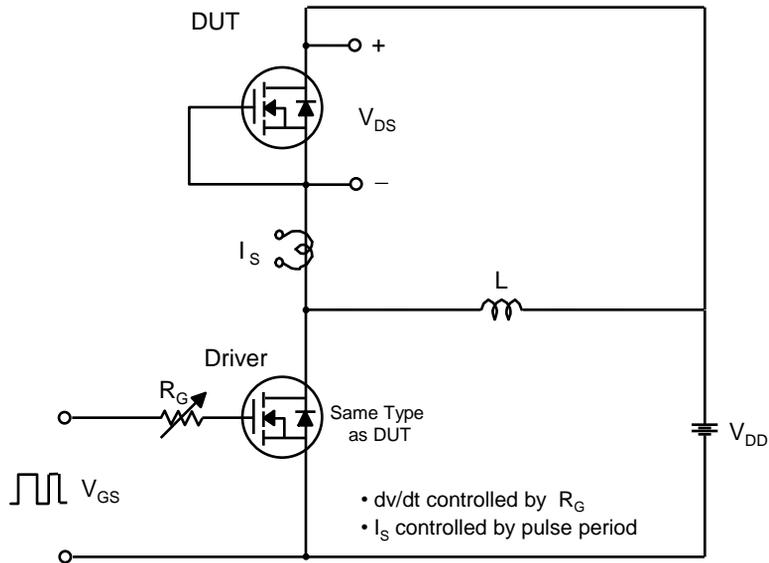
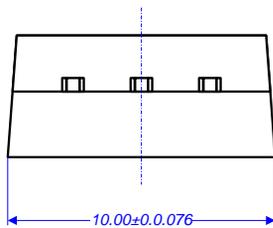
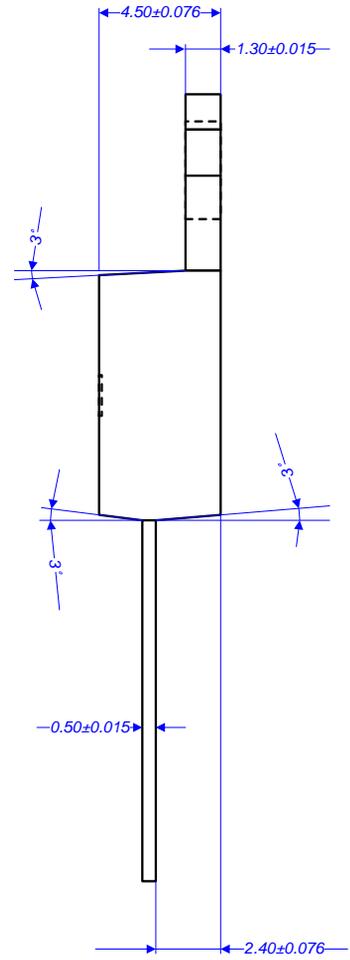
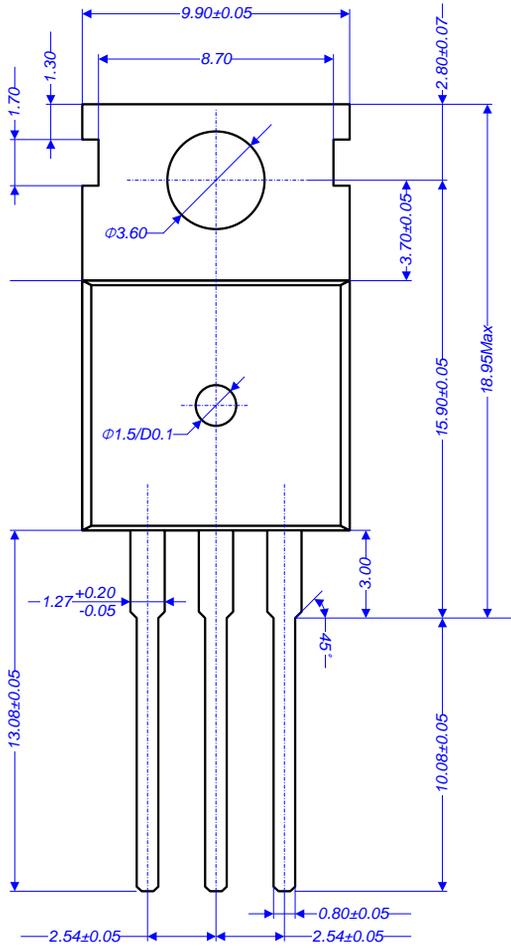


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Package Dimension

Z/H

TO-220

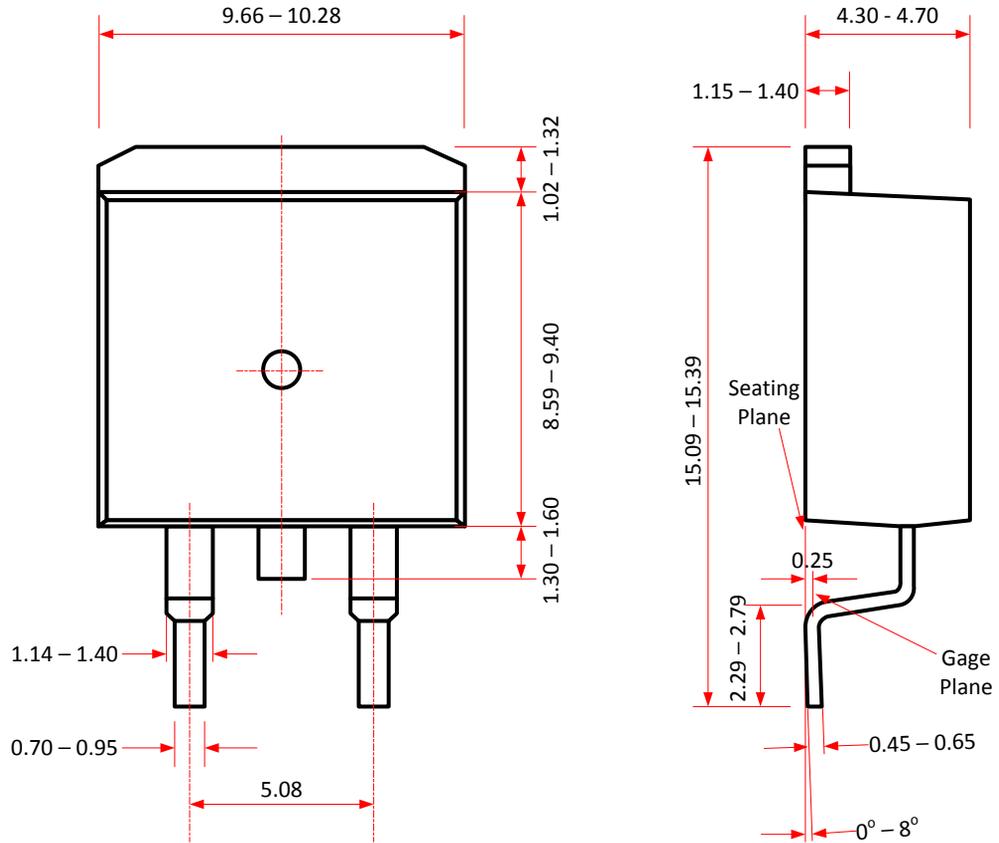


PFP110N10S / PFB110N10S

Package Dimension

H

TO-263 (D2-PAK)



PFP110N10S / PFB110N10S