

FEATURES

- ☐ 100% EAS Test
- ☐ Super high density cell design
- ☐ Extremely Low Intrinsic Capacitances
- ☐ Remarkable Switching Characteristics
- ☐ Extended Safe Operating Area
- ☐ Lower $R_{DS(ON)}$: 4.0 m Ω (Typ.) @ $V_{GS}=10V$

APPLICATION

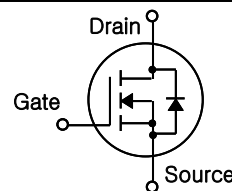
- ☐ DC Motor control for E-bike & Power tools
- ☐ Amplifier and car booster
- ☐ Load Switch
- ☐ DC-DC converters

PFP150N08S/PFB150N08S 80V N-Channel MOSFET

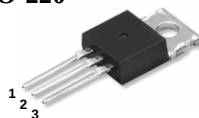
$$BV_{DSS} = 80 V$$

$$R_{DS(on)} = 4.0 m\Omega$$

$$I_D = 150 A$$



TO-220



1.Gate 2. Drain 3. Source

D2-PAK



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

$T_J=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	80	V
V_{GSS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current ($T_C = 25^{\circ}C$)	150	A
	Continuous Drain Current ($T_C = 100^{\circ}C$)	106	A
I_{DM}	Pulsed Drain Current	600	A
E_{AS}	Single Pulsed Avalanche Energy	625	mJ
P_D	Maximum Power Dissipation ($T_C = 25^{\circ}C$)	217	W
	Maximum Power Dissipation ($T_C = 100^{\circ}C$)	109	W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.69	$^{\circ}C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^{\circ}C$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^{\circ}C$

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}, T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$	--	4.0 5.6	5.0 7.0	m Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
V_{SD}	Diode Forward Voltage	$I_S = 40\text{ A}, V_{GS} = 0\text{ V}$	--	--	1.2	V

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, f=1.0\text{ MHz}$	--	6250	--	pF
C_{oss}	Output Capacitance		--	765	--	pF
C_{rss}	Reverse Transfer Capacitance		--	710	--	pF
R_g	Gate Resistance	$V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, f=1.0\text{ MHz}$	--	1.3	--	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 40\text{ V}, R_G = 3.3\Omega$ $I_D = 50\text{ A}, V_{GS} = 10\text{ V}$	--	23	--	ns
t_r	Turn-On Rise Time		--	39	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	86	--	ns
t_f	Turn-Off Fall Time		--	46	--	ns
Q_g	Total Gate Charge	$V_{DS}=64\text{ V}, I_D=50\text{ A}, V_{GS}=10\text{ V}$	--	130	--	nC
Q_{gs}	Gate-Source Charge		--	25	--	nC
Q_{gd}	Gate-Drain Charge		--	32	--	nC

Notes ;

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. EAS is tested at starting $T_J=25^\circ\text{C}$, $L=0.5\text{ mH}$, $I_{AS}=50\text{ A}$, $V_{GS}=10\text{ V}$
3. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature

Typical Characteristics

Fig. 1 Power Dissipation

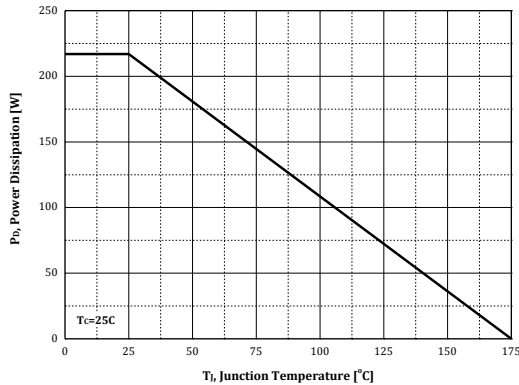


Fig. 2 Maximum Drain Current

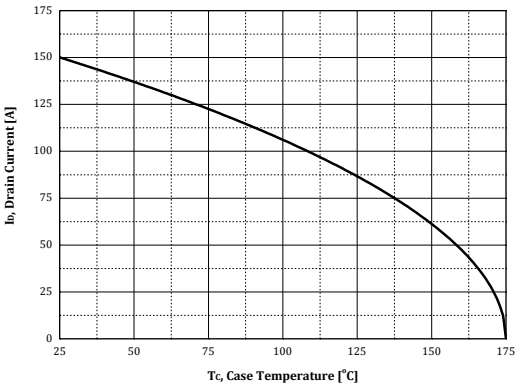


Fig. 3 Safe Operation Area

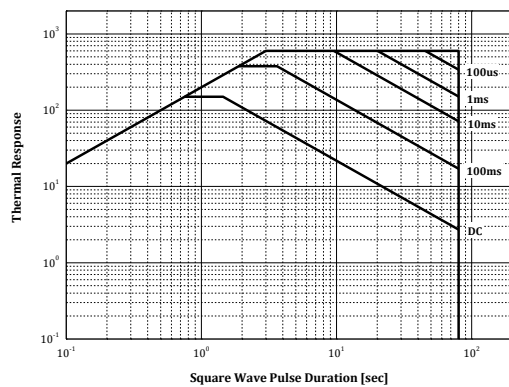


Fig. 4 Thermal Transient Impedance

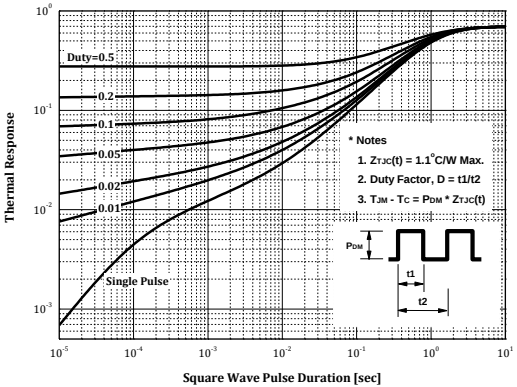


Fig. 5 Output Characteristics

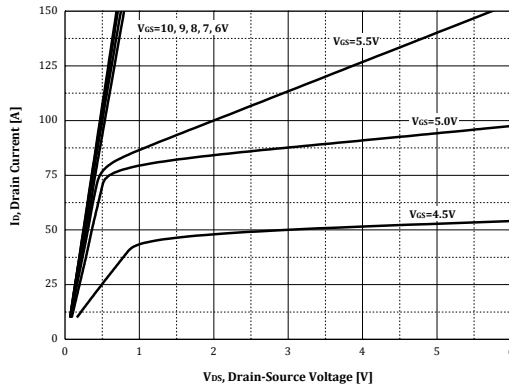
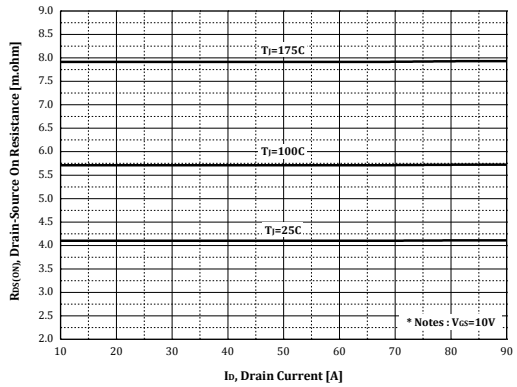


Fig. 6 Drain-Source On Resistance



Typical Characteristics (continued)

Fig. 7 Drain-Source on Resistance

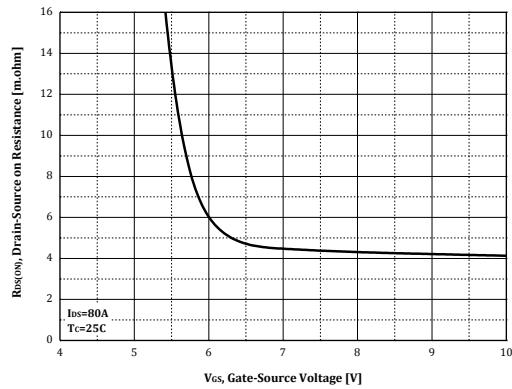


Fig. 8 $V_{GS(TH)}$ vs. Junction Temperature

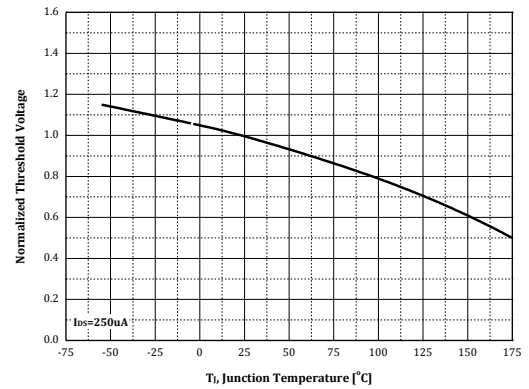


Fig. 9 $R_{DS(ON)}$ vs. Junction Temperature

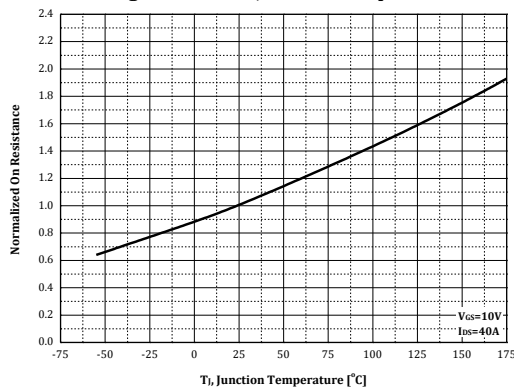


Fig. 10 Source-Drain Diode Voltage

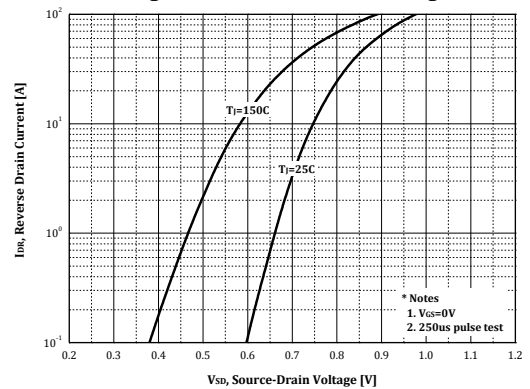


Fig. 11 Capacitance

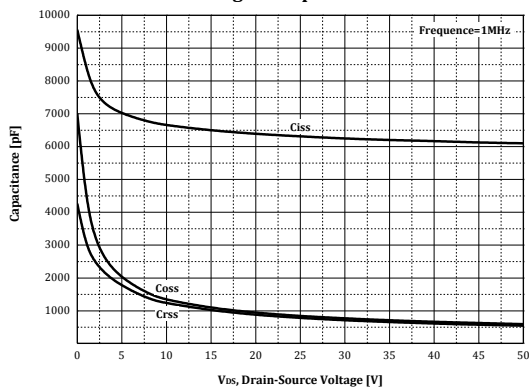
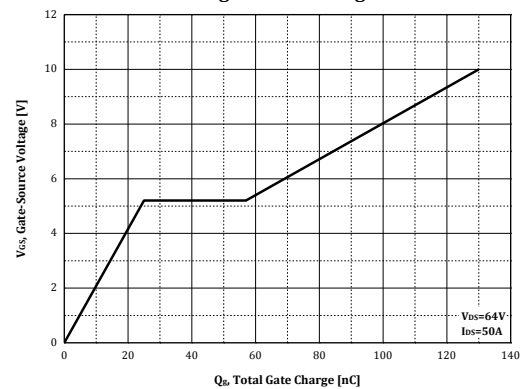


Fig. 12 Gate Charge



Characteristics Test Circuit & Waveform

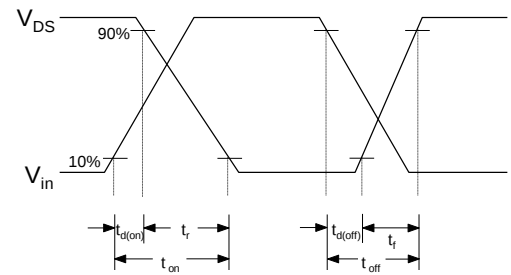
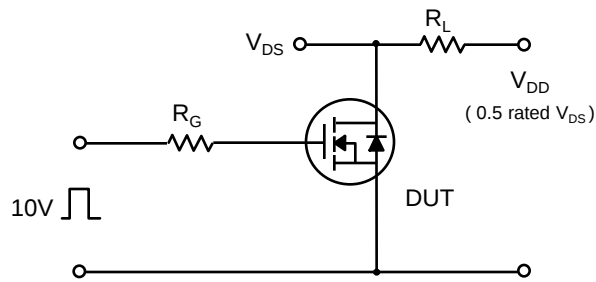


Fig 14. Resistive Switching Test Circuit & Waveforms

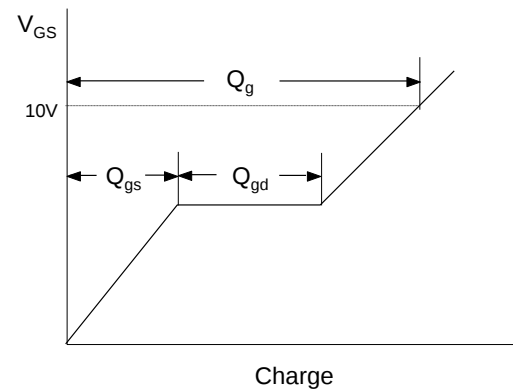
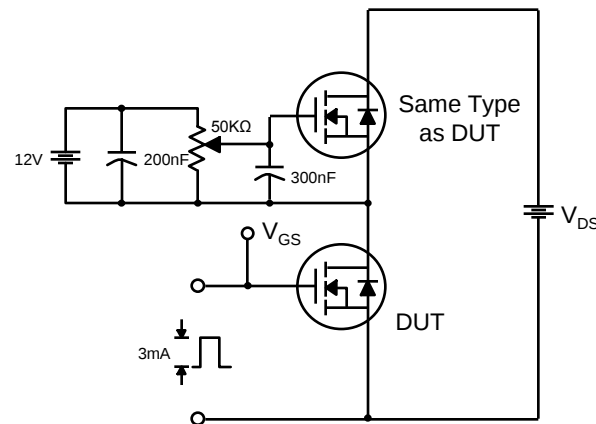


Fig 15. Gate Charge Test Circuit & Waveform

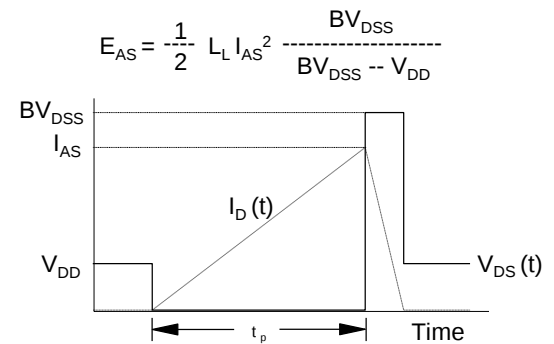
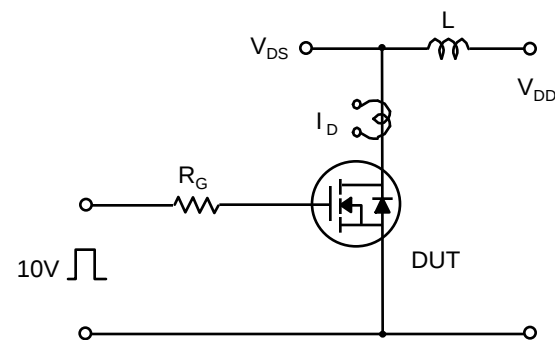


Fig 16. Unclamped Inductive Switching Test Circuit & Waveforms

Characteristics Test Circuit & Waveform (continued)

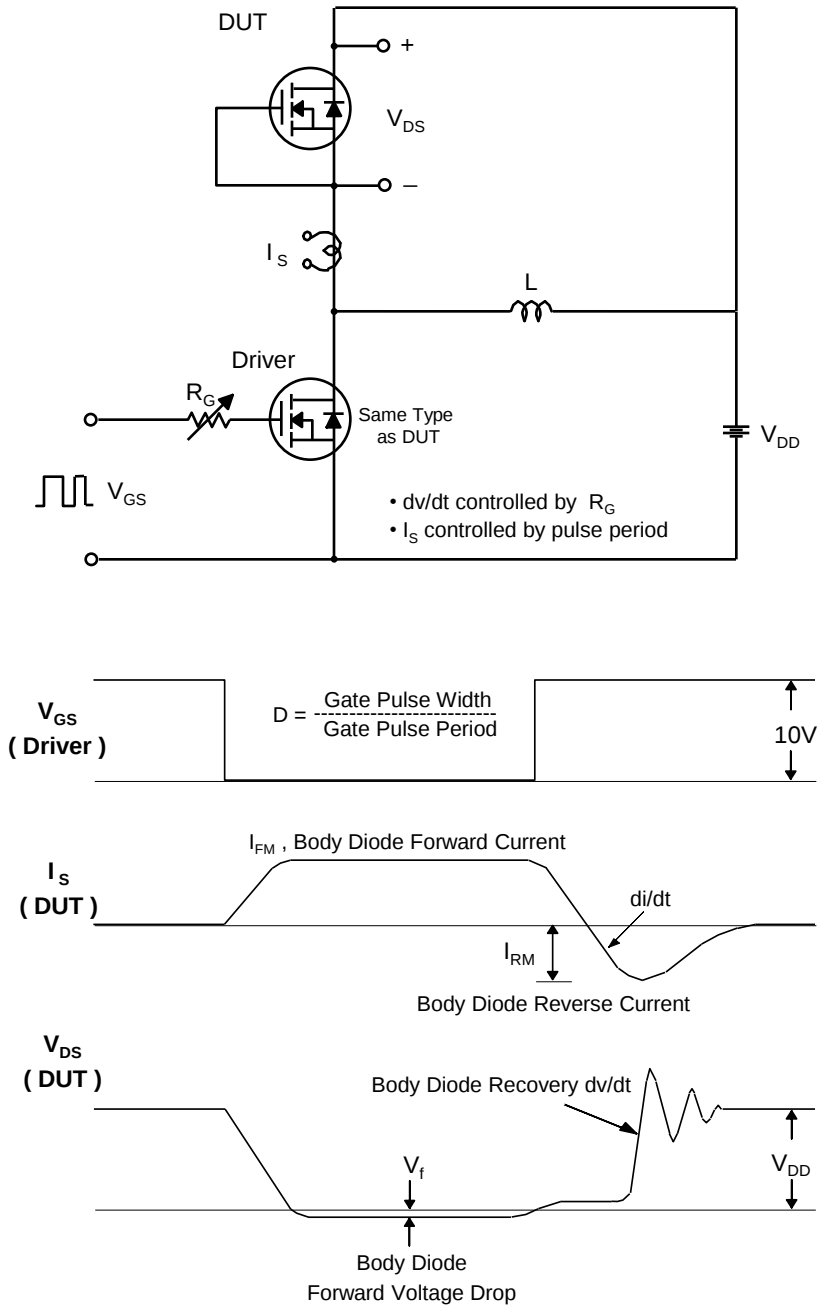
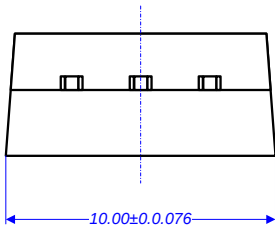
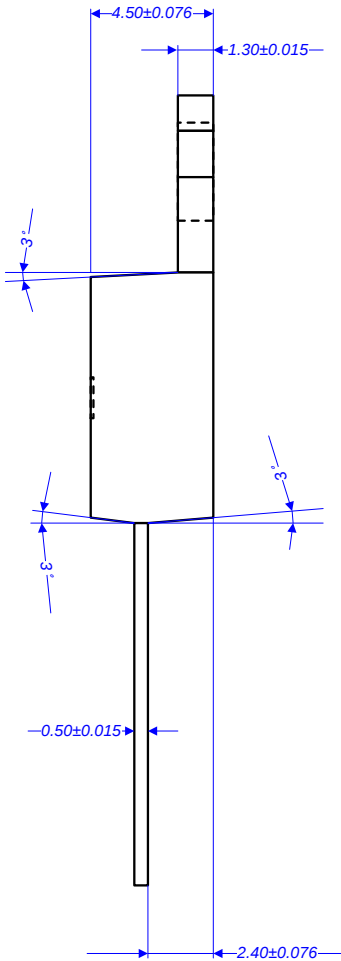
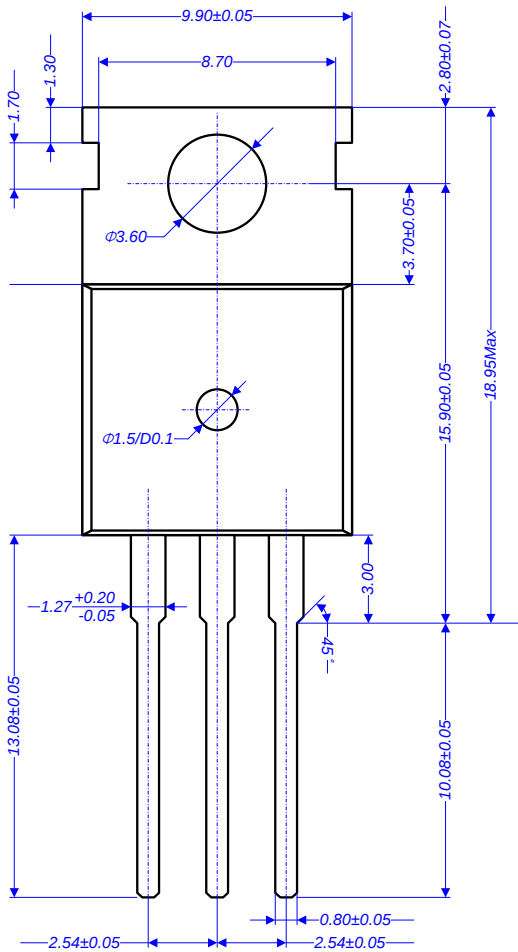


Fig 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Package Dimension

TO-220



Package Dimension

TO-263 (D2-PAK)

