

# I<sup>2</sup>C Bus Controlled 5-Input 2-Output AV Switch

## Monolithic IC MM1492

May 2, 2003

### Outline

This IC is an I<sup>2</sup>C bus controlled AV switch IC with 5-input 2-output developed for TVs. It supports 2-screen or PIP TVs as it provides two outputs, and support an external output (monitor) pin as well.

### Features

1. Serial control by I<sup>2</sup>C bus
2. 5 inputs and 2 outputs
3. 2 Y/C (S-pin) inputs and 2 outputs
4. Video and audio switches can be controlled independently.
5. Includes a 6dB amp in the video channel
6. Incorporates a Y/C mix circu
7. One of the two audio outputs has a built-in -6dB ON/OFF switch.
8. Slave address can be changed to 90H or 92H.
9. Enables audio mute with an external pin
10. I<sup>2</sup>C bus lines (SDA, SCL) maintain high impedance during power-off.
11. Includes a tri-stated detection function
12. Includes a power-on reset function
13. Supports 2-screen and PIP TVs. Also supports an external output (monitor) pin.

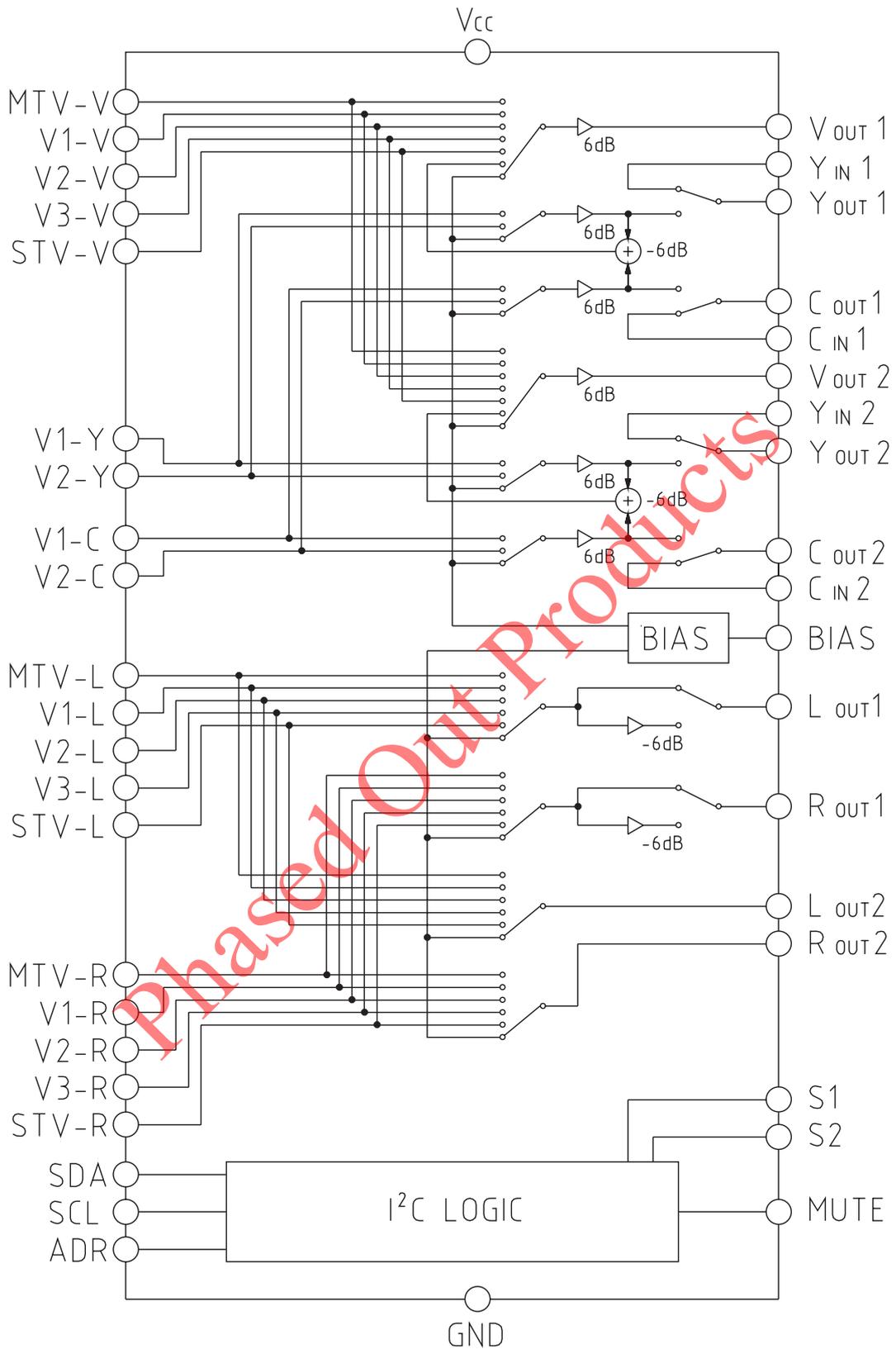
### Package

SOP-44A

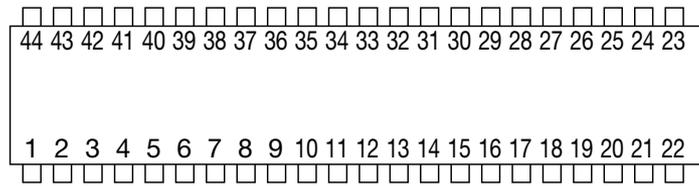
### Applications

- (1) TVs
- (2) Other video equipment

Block Diagram



Pin Assignment



SOP-44A

1	V1-V	12	S2	23	Vout2	34	YIN1
2	V1-L	13	V3-V	24	Rout2	35	Rout1
3	V1-Y	14	V3-L	25	Cout2	36	Lout1
4	V1-R	15	V3-R	26	Lout2	37	Vout1
5	V1-C	16	STV-V	27	Yout2	38	BIAS
6	S1	17	STV-L	28	GND	39	Yout1
7	V2-V	18	STV-R	29	SDA	40	Vcc
8	V2-L	19	YIN2	30	SCL	41	Cout1
9	V2-Y	20	ADR	31	MUTE	42	MTV-R
10	V2-R	21	CIN2	32	CIN1	43	MTV-V
11	V2-C	22	GND	33	GND	44	MTV-L

Pin Description

Pin No.	Pin name	Functions	Internal equivalent circuit diagram
1	V1-V	Video input terminal	
3	V1-Y	(Composite or Y)	
7	V2-V	*Sync chip clamp	
9	V2-Y		
13	V3-V		
16	STV-V		
19	YIN2		
34	YIN1		
43	MTV-V		
2	V1-L	Audio input terminal	
4	V1-R		
8	V2-L		
10	V2-R		
14	V3-L		
15	V3-R		
17	STV-L		
18	STV-R		
42	MTV-R		
44	MTV-L		

Pin No.	Pin name	Functions	Internal equivalent circuit diagram
5 11 21 32	V1-C V2-C C <sub>IN2</sub> C <sub>IN1</sub>	Video input terminal (Croma)	<p>* 1 5,11PIN=25kΩ、21,23PIN=12.5kΩ</p>
6 12	S1 S2	Distinction 3-effects input terminal DC Detect	
20 31	ADR Mute	Sleve address select Audio Mute terminal	
22 28 33	GND	GND	
23 37	V <sub>out2</sub> V <sub>out1</sub>	Composite video out	
24 26 35 36	R <sub>out2</sub> L <sub>out2</sub> R <sub>out1</sub> L <sub>out1</sub>	Audio out terminal	
25 27 39 41	C <sub>out2</sub> Y <sub>out2</sub> Y <sub>out1</sub> C <sub>out1</sub>	S-Video out terminal	

Pin No.	Pin name	Functions	Internal equivalent circuit diagram
29	SDA	Data input from I <sup>2</sup> C	
30	SCL	CLK input from I <sup>2</sup> C	
38	BIAS	Internal bias terminal	
40	Vcc	Vcc	

**Absolute Maximum Ratings** (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Power supply voltage	V <sub>CCmax.</sub>	12	V
Allowable loss	P <sub>d</sub>	1100	mW

**Recommended Operating Conditions**

Item	Symbol	Ratings	Units
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Operating voltage	V <sub>OP</sub>	+8~+10	V

**Electrical Characteristics** (Except where noted otherwise, V<sub>CC</sub>=9V, T<sub>a</sub>=25°C)

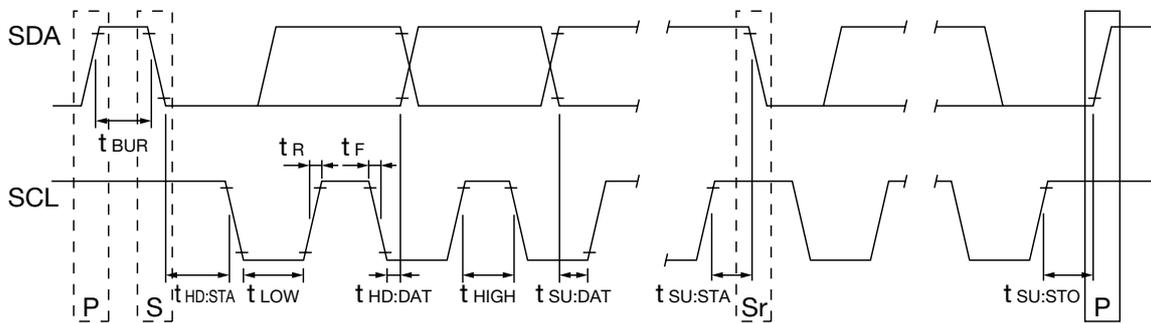
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption	I <sub>CC</sub>	No signal	39	55	71	mA
<b>V<sub>OUT1</sub></b>						
Voltage gain	G <sub>V1</sub>	SIN wave : 1V <sub>P-P</sub> 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	f <sub>V1</sub>	SIN wave : 1V <sub>P-P</sub> 10MHz/100kHz	-1.0	0.0	1.0	dB
Differential gain	DG <sub>V1</sub>	Staircase signal 1V <sub>P-P</sub>	-3	0	3	%
Differential phase	DP <sub>V1</sub>	Staircase signal 1V <sub>P-P</sub>	-3	0	3	deg
Input dynamic ranges	DV <sub>1</sub>	SIN wave : 100kHz THD=1.0%	1.4	1.5		V <sub>P-P</sub>
<b>V<sub>OUT2</sub></b>						
Voltage gain	G <sub>V2</sub>	SIN wave : 1V <sub>P-P</sub> 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	f <sub>V2</sub>	SIN wave : 1V <sub>P-P</sub> 10MHz/100kHz	-1.0	0.0	1.0	dB
Differential gain	DG <sub>V2</sub>	Staircase signal 1V <sub>P-P</sub>	-3	0	3	%
Differential phase	DP <sub>V2</sub>	Staircase signal 1V <sub>P-P</sub>	-3	0	3	deg
Input dynamic range	DV <sub>2</sub>	SIN wave : 100kHz THD=1.0%	1.4	1.5		V <sub>P-P</sub>
<b>Y<sub>OUT1</sub></b>						
Voltage gain	G <sub>Y1</sub>	V <sub>n-Y</sub> : SIN wave 1V <sub>P-P</sub> 100kHz	5.5	6.0	6.5	dB
	G <sub>Y2</sub>	Y <sub>IN1</sub> : SIN wave 2V <sub>P-P</sub> 100kHz	-0.5	0.0	0.5	dB
Frequency characteristics	f <sub>Y1</sub>	V <sub>n-Y</sub> : SIN wave 1V <sub>P-P</sub>	-1.0	0.0	1.0	dB
	f <sub>Y2</sub>	Y <sub>IN1</sub> : SIN wave 2V <sub>P-P</sub>	-1.0	0.0	1.0	dB
Differential gain	DG <sub>Y1</sub>	V <sub>n-Y</sub> : Staircase signal 1V <sub>P-P</sub>	-3	0	3	%
		Y <sub>IN1</sub> : Staircase signal 2V <sub>P-P</sub>	-3	0	3	%
Differential phase	DP <sub>Y1</sub>	V <sub>n-Y</sub> : Staircase signal 1V <sub>P-P</sub>	-3	0	3	deg
		Y <sub>IN1</sub> : Staircase signal 2V <sub>P-P</sub>	-3	0	3	deg
Input dynamic range	D <sub>Y1</sub>	V <sub>n-Y</sub> : SIN wave 100kHz THD=1.0%	1.4	1.5		V <sub>P-P</sub>
	D <sub>Y2</sub>	Y <sub>IN1</sub> : SIN wave 100kHz THD=1.0%	3.2	3.8		V <sub>P-P</sub>
Output impedance	Z <sub>OY1</sub>			(50)		Ω
<b>Y<sub>OUT2</sub></b>						
Voltage gain	G <sub>Y3</sub>	V <sub>n-Y</sub> : SIN wave 1V <sub>P-P</sub> 100kHz	5.5	6.0	6.5	dB
	G <sub>Y4</sub>	Y <sub>IN2</sub> : SIN wave 2V <sub>P-P</sub> 100kHz	-0.5	0.0	0.5	dB
Frequency characteristics	f <sub>Y3</sub>	V <sub>n-Y</sub> : SIN wave 1V <sub>P-P</sub>	-1.0	0.0	1.0	dB
	f <sub>Y4</sub>	Y <sub>IN2</sub> : SIN wave 2V <sub>P-P</sub>	-1.0	0.0	1.0	dB
Differential gain	DG <sub>Y2</sub>	V <sub>n-Y</sub> : Staircase signal 1V <sub>P-P</sub>	-3	0	3	%
		Y <sub>IN2</sub> : Staircase signal 2V <sub>P-P</sub>	-3	0	3	%
Differential phase	DP <sub>Y2</sub>	V <sub>n-Y</sub> : Staircase signal 1V <sub>P-P</sub>	-3	0	3	deg
		Y <sub>IN2</sub> : Staircase signal 2V <sub>P-P</sub>	-3	0	3	deg
Input dynamic range	D <sub>Y3</sub>	V <sub>n-Y</sub> : SIN wave 100kHz THD=1.0%	1.4	1.5		V <sub>P-P</sub>
	D <sub>Y4</sub>	Y <sub>IN2</sub> : SIN wave 100kHz THD=1.0%	3.2	3.8		V <sub>P-P</sub>
Output impedance	Z <sub>OY2</sub>			(50)		Ω
<b>C<sub>OUT1</sub></b>						
Voltage gain	G <sub>C1</sub>	V <sub>n-C</sub> : SIN wave 1V <sub>P-P</sub> 100kHz	5.5	6.0	6.5	dB
	G <sub>C2</sub>	C <sub>IN1</sub> : SIN wave 2V <sub>P-P</sub> 100kHz	-0.5	0.0	0.5	dB
Frequency characteristics	f <sub>C1</sub>	V <sub>n-C</sub> : SIN wave 1V <sub>P-P</sub>	-1.0	0.0	1.0	dB
	f <sub>C2</sub>	C <sub>IN1</sub> : SIN wave 2V <sub>P-P</sub>	-1.0	0.0	1.0	dB
Differential gain	DG <sub>C1</sub>	C <sub>IN1</sub> : Staircase signal 2V <sub>P-P</sub>	-3	0	3	%
Differential phase	DP <sub>C1</sub>	C <sub>IN1</sub> : Staircase signal 2V <sub>P-P</sub>	-3	0	3	deg
Input dynamic range	D <sub>C1</sub>	V <sub>n-Y</sub> : SIN wave 100kHz THD=1.0%	2.75	3.25		V <sub>P-P</sub>
	D <sub>C2</sub>	Y <sub>IN1</sub> : SIN wave 100kHz THD=1.0%	5.5	6.5		V <sub>P-P</sub>
Input impedance	Z <sub>IC1</sub>	V <sub>n-C</sub> and C <sub>IN1</sub>	10	15	20	kΩ
Output impedance	Z <sub>OC1</sub>			(50)		Ω

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
<b>C<sub>OUT2</sub></b>						
Voltage gain	G <sub>C3</sub>	V <sub>n-C</sub> : SIN wave 1V <sub>P-P</sub> 100kHz	5.5	6.0	6.5	dB
	G <sub>C4</sub>	C <sub>IN2</sub> : SIN wave 2V <sub>P-P</sub> 100kHz	-0.5	0.0	0.5	dB
Frequency characteristics	f <sub>C3</sub>	V <sub>n-C</sub> : SIN wave 1V <sub>P-P</sub>	-1.0	0.0	1.0	dB
	f <sub>C4</sub>	C <sub>IN2</sub> : SIN wave 2V <sub>P-P</sub>	-1.0	0.0	1.0	dB
Differential gain	DG <sub>C2</sub>	C <sub>IN1</sub> : Staircase signal 2V <sub>P-P</sub>	-3	0	3	%
Differential phase	DP <sub>C2</sub>	C <sub>IN2</sub> : Staircase signal 2V <sub>P-P</sub>	-3	0	3	deg
Input dynamic range	DC <sub>3</sub>	V <sub>n-Y</sub> : SIN wave 100kHz THD=1.0%	2.75	3.25		V <sub>P-P</sub>
	DC <sub>4</sub>	Y <sub>IN2</sub> : SIN wave 100kHz THD=1.0%	5.5	6.5		V <sub>P-P</sub>
Input impedance	Z <sub>IC2</sub>	C <sub>IN2</sub>	10	15	20	kΩ
Output impedance	Z <sub>OC2</sub>			(50)		Ω
<b>L<sub>OUT1</sub></b>						
Voltage gain	G <sub>L1</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz -6dB Select	-6.5	-6.0	-5.5	dB
	G <sub>L2</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz 0dB Select	-0.5	0.0	0.5	dB
Frequency characteristics	f <sub>L1</sub>	SIN wave 2.5V <sub>P-P</sub> 1MHz/1kHz	-3.0	0.0	1.0	dB
Total harmonic distortion	THD <sub>L1</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz		0.03	0.1	%
Input dynamic range	DL <sub>1</sub>	SIN wave 1kHz THD<0.5%	2.6	2.8		V <sub>rms</sub>
Output offset voltage	V <sub>OFFL1</sub>	DC offset at the switching time		0	±15	mV
Input impedance	Z <sub>IL1</sub>		42	60	78	kΩ
Output impedance	Z <sub>OL1</sub>			(120)		Ω
<b>L<sub>OUT2</sub></b>						
Voltage gain	G <sub>L3</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz -6dB Select	-6.5	-6.0	-5.5	dB
	G <sub>L4</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz 0dB Select	-0.5	0.0	0.5	dB
Frequency characteristics	f <sub>L2</sub>	SIN wave 2.5V <sub>P-P</sub> 1MHz/1kHz	-3.0	0.0	1.0	dB
Total harmonic distortion	THD <sub>L2</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz		0.03	0.1	%
Input dynamic range	DL <sub>2</sub>	SIN wave 1kHz THD<0.5%	2.6	2.8		V <sub>rms</sub>
Output offset voltage	V <sub>OFFL2</sub>	DC offset at the switching time		0	±15	mV
Output impedance	Z <sub>OL2</sub>			(120)		Ω
<b>R<sub>OUT1</sub></b>						
Voltage gain	G <sub>R1</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz -6dB Select	-6.5	-6.0	-5.5	dB
	G <sub>R2</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz 0dB Select	-0.5	0.0	0.5	dB
Frequency characteristic	f <sub>R1</sub>	SIN wave 2.5V <sub>P-P</sub> 1MHz/1kHz	-3.0	0.0	1.0	dB
Total harmonic distortion	THD <sub>R1</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz		0.03	0.1	%
Input dynamic range	DR <sub>1</sub>	SIN wave 1kHz THD<0.5%	2.6	2.8		V <sub>rms</sub>
Output offset voltage	V <sub>OFFR1</sub>	DC offset at the switching time		0	±15	mV
Input impedance	Z <sub>IR1</sub>		42	60	78	kΩ
Output impedance	Z <sub>OR1</sub>			(120)		Ω
<b>R<sub>OUT2</sub></b>						
Voltage gain	G <sub>R3</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz -6dB Select	-6.5	-6.0	-5.5	dB
	G <sub>R4</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz 0dB Select	-0.5	0.0	0.5	dB
Frequency characteristics	f <sub>R2</sub>	SIN wave 2.5V <sub>P-P</sub> 1MHz/1kHz	-3.0	0.0	1.0	dB
Total harmonic distortion	THD <sub>R2</sub>	SIN wave 2.5V <sub>P-P</sub> 1kHz		0.03	0.1	%
Input dynamic range	DR <sub>2</sub>	SIN wave 1kHz THD<0.5%	2.6	2.8		V <sub>rms</sub>
Output offset voltage	V <sub>OFFR2</sub>	DC offset at the switching time		0	±15	mV
Output impedance	Z <sub>OR2</sub>			(120)		Ω

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
<b>Crosstalk (★1)</b>						
V <sub>OUT1</sub>	CT <sub>V1</sub>	SG1 : 4.43MHz 1V <sub>P-P</sub> (At mix, SG2/3 input)		-60	-53	dB
V <sub>OUT2</sub>	CT <sub>V2</sub>	SG1 : 4.43MHz 1V <sub>P-P</sub> (At mix, SG2/3 input)		-60	-53	dB
Y <sub>OUT1</sub>	CT <sub>Y1</sub>	SG2 : 4.43MHz 1V <sub>P-P</sub>		-60	-53	dB
Y <sub>OUT2</sub>	CT <sub>Y2</sub>	SG2 : 4.43MHz 1V <sub>P-P</sub>		-60	-53	dB
C <sub>OUT1</sub>	CT <sub>C1</sub>	SG3 : 4.43MHz 1V <sub>P-P</sub>		-60	-53	dB
C <sub>OUT2</sub>	CT <sub>C2</sub>	SG3 : 4.43MHz 1V <sub>P-P</sub>		-60	-53	dB
L <sub>OUT1</sub>	CT <sub>L1</sub>	1kHz 2.5V <sub>P-P</sub>		-90	-80	dB
L <sub>OUT2</sub>	CT <sub>L2</sub>	1kHz 2.5V <sub>P-P</sub>		-90	-80	dB
R <sub>OUT1</sub>	CT <sub>R1</sub>	1kHz 2.5V <sub>P-P</sub>		-90	-80	dB
R <sub>OUT2</sub>	CT <sub>R2</sub>	1kHz 2.5V <sub>P-P</sub>		-90	-80	dB
<b>Terminal voltage</b>						
Video input terminal	V <sub>VIP</sub>	No signal, No load	4.6	4.9	5.2	V
V <sub>OUT1/2</sub> terminal	V <sub>VOP</sub>	No signal, No load	3.9	4.2	4.5	V
Y <sub>OUT1/2</sub> terminal	V <sub>YOP</sub>	No signal, No load	3.2	3.5	3.8	V
C <sub>OUT1/2</sub> terminal	V <sub>COP</sub>	No signal, No load	3.2	3.5	3.8	V
Audio input terminal	V <sub>AIP</sub>	No signal, No load	4.0	4.3	4.6	V
Audio output terminal	V <sub>AOP</sub>	No signal, No load	3.9	4.2	4.5	V
<b>I<sup>2</sup>C condition (Refer to figure below)</b>						
Input voltage L	V <sub>IL</sub>		0.0		1.5	V
Input voltage H	V <sub>IH</sub>		3.0		5.0	V
Low level output voltage	V <sub>OL</sub>	SDA sink 3mA	0.0		0.4	V
High level input current	I <sub>IH</sub>	SDA, SCL=4.5V	-10		10	V
Low level input current	I <sub>IL</sub>	SDA, SCL=0.4V	-10		10	V
Clock frequency	f <sub>SCL</sub>				100	kHz
Data transfer wait time	t <sub>BUF</sub>		4.7			μs
SCL start hold time	t <sub>HD:STA</sub>		4.0			μs
SCL low level hold time	t <sub>LOW</sub>		4.7			μs
SCL high level hold time	t <sub>HIGH</sub>		4.0			μs
SCL start setup time	t <sub>SU:STA</sub>		4.7			μs
SDA data hold time	t <sub>HD:DAT</sub>		200			ns
SDA data setup time	t <sub>SU:DAT</sub>		250			ns
SCL rise-time	t <sub>R</sub>				1000	ns
SCL fall-time	t <sub>F</sub>				300	ns
SCL stop setup time	t <sub>SU:STO</sub>		4.0			μs

(The inside of parentheses is design guarantee value.)

I<sup>2</sup>C condition



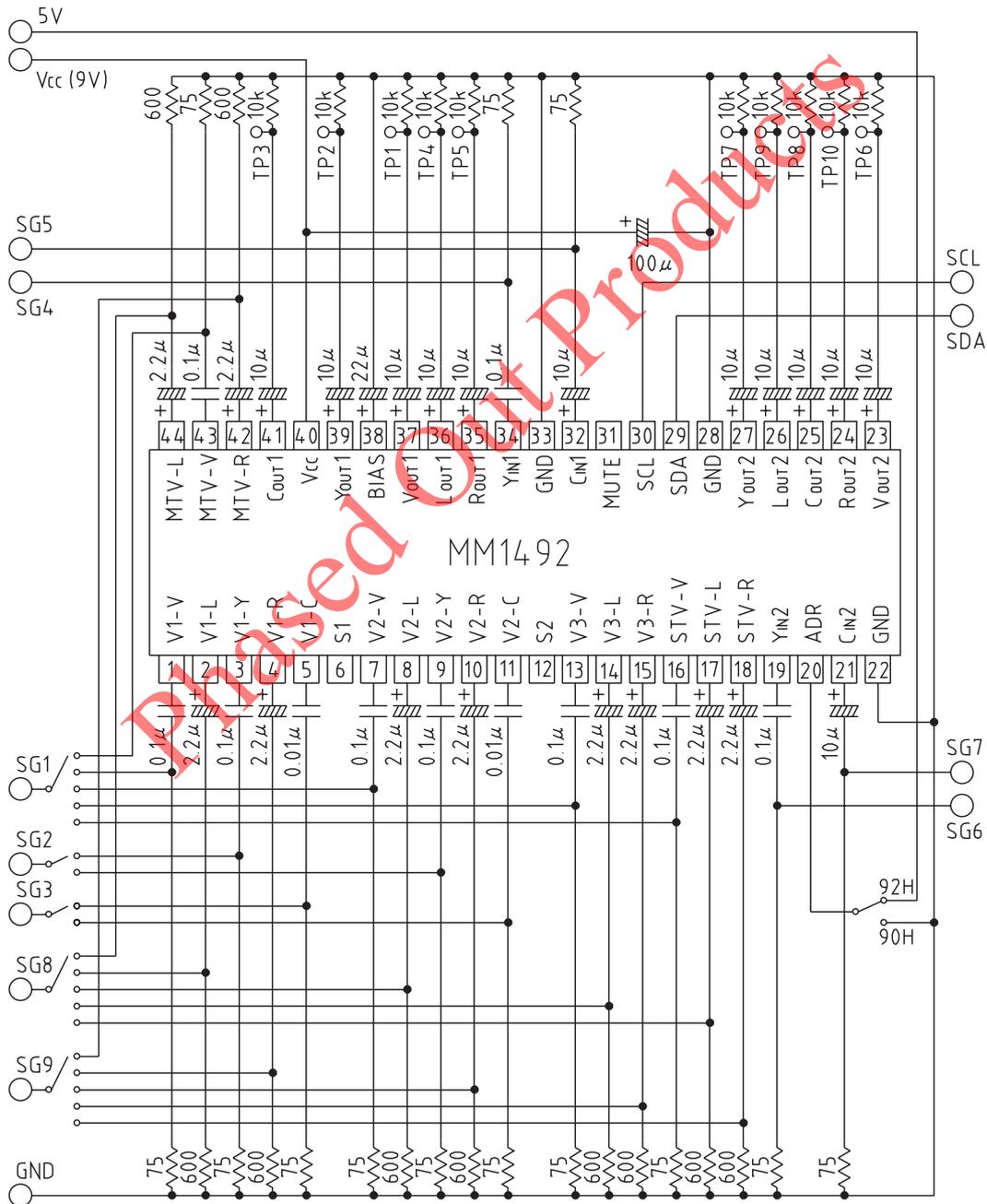
- (Note.1) : Input signal symbol  
 Vn-V=MTV-V, V1-V, V2-V,V3-V, STV-V  
 Vn-Y=V1-Y, V2-Y  
 Vn-C=V1-C, V2-C

- (Note.2) : \*1 Test Circuit of Crosstalk  
 See Test Circuit 2

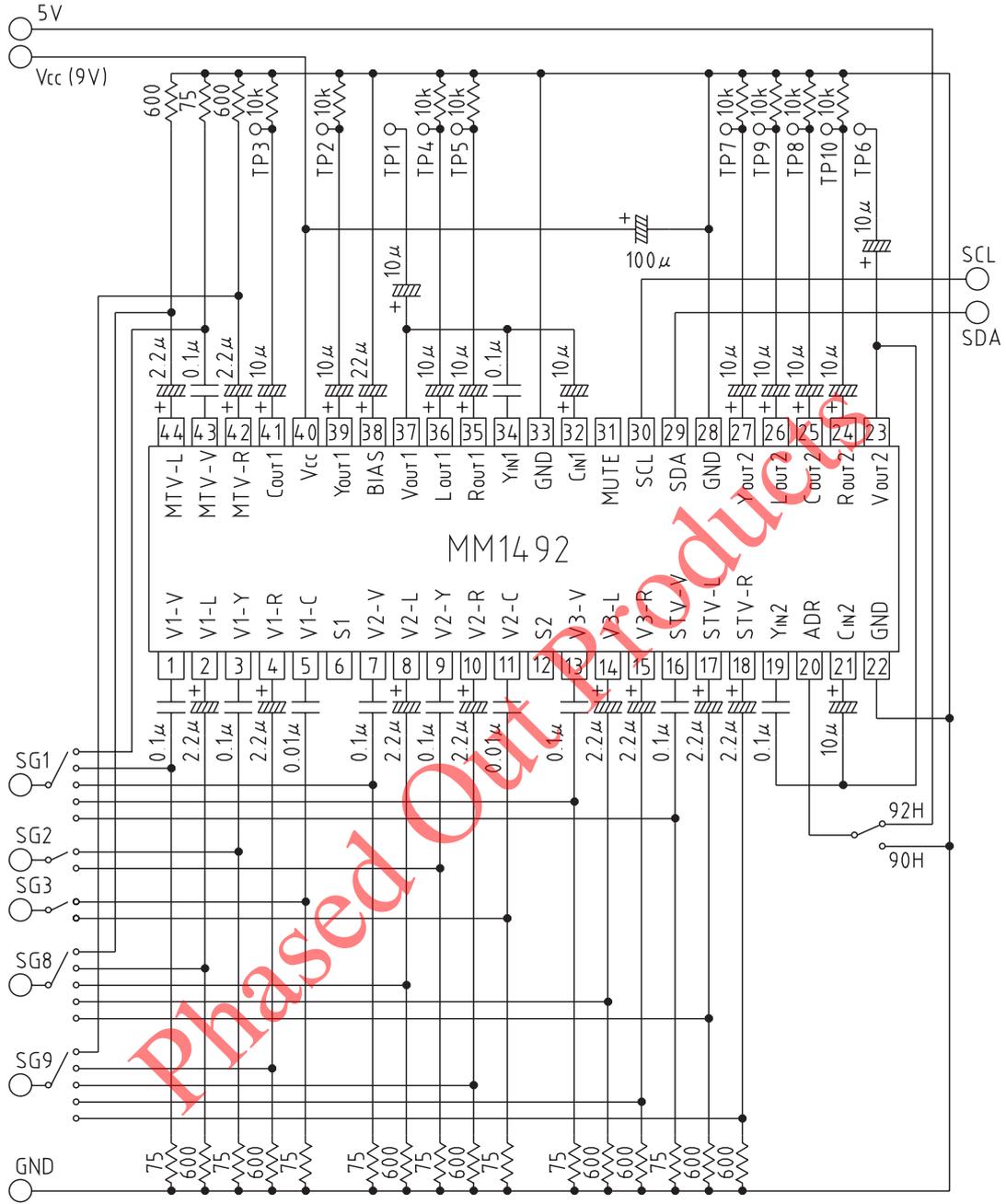
- (Note.3) : Video inputs  
 Vn-V, Vn-Y, and Y<sub>INN</sub> inputs are sync chip clamped, while Vn-C and C<sub>INN</sub> inputs are non-clamped.

## Measuring Circuit

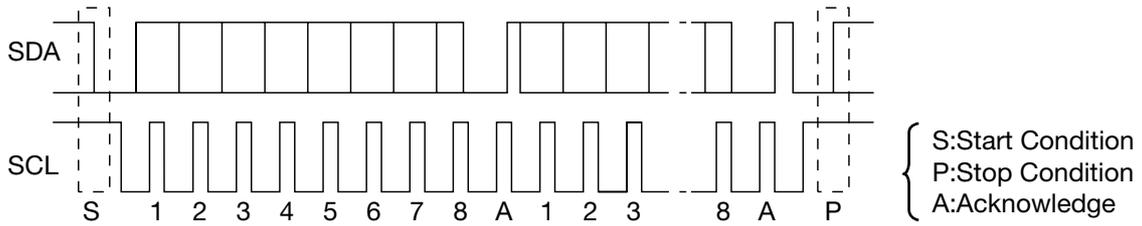
### Measuring Circuit 1



■ Measuring Circuit 2 (Crosstalk measurement)



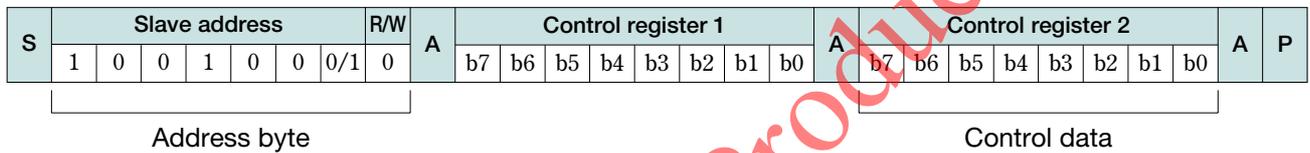
I<sup>2</sup>C BUS



I<sup>2</sup>C BUS is inter bus system controlled by 2 lines (SDA, SCL).  
 Data are transmitted and received in the units of byte and Acknowledge.  
 It is transmitted by MSB first from the Start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.  
 The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.

Set the R/W bit to 0 when data are used control registers.

As MM1492 slave address, either 90H or 92H can be selected according to the ADR terminal conditions.

When ADR terminal is L, 90H is selected.

The following figure indicates the control contents of control registers and switches.

Each bit of control registers is reset to 0, when power-on.

Register	b7	b6	b5	b4	b3	b2	b1	b0
1	Audio Gain 1	S/Comp select 1	Video out1 select		Audio out1 select			
2	Audio Gain 2	S/Comp select 2	Video out2 select		Audio out2 select			

MM1492 consists of one address byte and two control data bytes (3bytes in total).

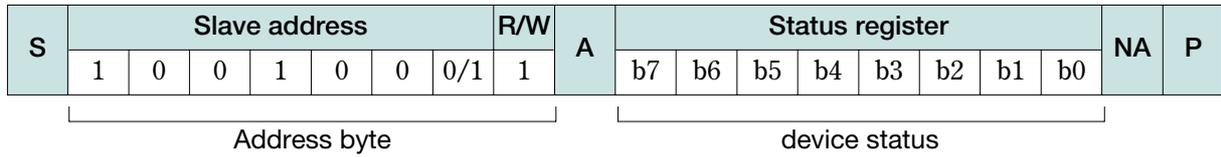
All data over the limited length (4th and subsequent bytes) are fully neglected.

For details of the control contents of switches, refer to the separate table.

**[Status registers]**

Status registers are data to inform the device status.

The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.

Set the R/W bit to 1 when data are used status registers.

As MM1492 slave address, either 91H or 93H can be selected according to the ADR terminal conditions.

When ADR terminal is L, 91H is selected.

Set the confirmation acknowledgement after the end of status register to non-acknowledgement.

The following figure shows the correspondence of the output data of status registers.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON	×	S1	S1	S2	S2	×	×
RESET		OPEN	SEL	OPEN	SEL		

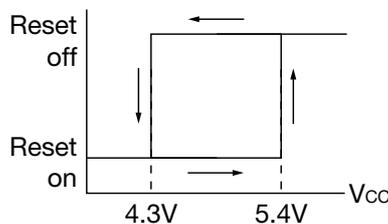
- P-on RESET : 1 returns when the power on reset is done, 0 returns after reading data once.
- S1/S2 OPEN : S1/S2 OPEN and SEL are identified by 3 values, and output according to the S1/S2 SEL combinations in the following table.

DC voltage of S1/S2	S1/S2 OPEN	S1/S2 SEL
DC ≤ 0.8V	0	1
1.3V ≤ DC ≤ 3.5V	0	0
4.5V ≤ DC	1	0

**[about power on reset]**

MM1492 is provided with a power on reset function to reset each control register to 0 when power supply is turned on.

The power on reset threshold has the hysteresis as shown in following figure.



**Switch Control Table**

(1) Video output 1

b6	b5	b4	b3	V <sub>out1</sub>	Y <sub>out1</sub>	C <sub>out1</sub>
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV-V	Y <sub>IN1</sub>	C <sub>IN1</sub>
0	0	1	0	V1-V	Y <sub>IN1</sub>	C <sub>IN1</sub>
0	0	1	1	V2-V	Y <sub>IN1</sub>	C <sub>IN1</sub>
0	1	0	0	V3-V	Y <sub>IN1</sub>	C <sub>IN1</sub>
0	1	0	1	STV-V	Y <sub>IN1</sub>	C <sub>IN1</sub>
0	1	1	0	Mute	Mute	Mute
0	1	1	1			
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV-V	Y <sub>IN1</sub>	C <sub>IN1</sub>
1	0	1	0	V1-(Y+C)	V1-Y	V1-C
1	0	1	1	V2-(Y+C)	V2-Y	V2-C
1	1	0	0	V3-V	Y <sub>IN1</sub>	C <sub>IN1</sub>
1	1	0	1	STV-V	Y <sub>IN1</sub>	C <sub>IN1</sub>
1	1	1	0	Mute	Mute	Mute
1	1	1	1			

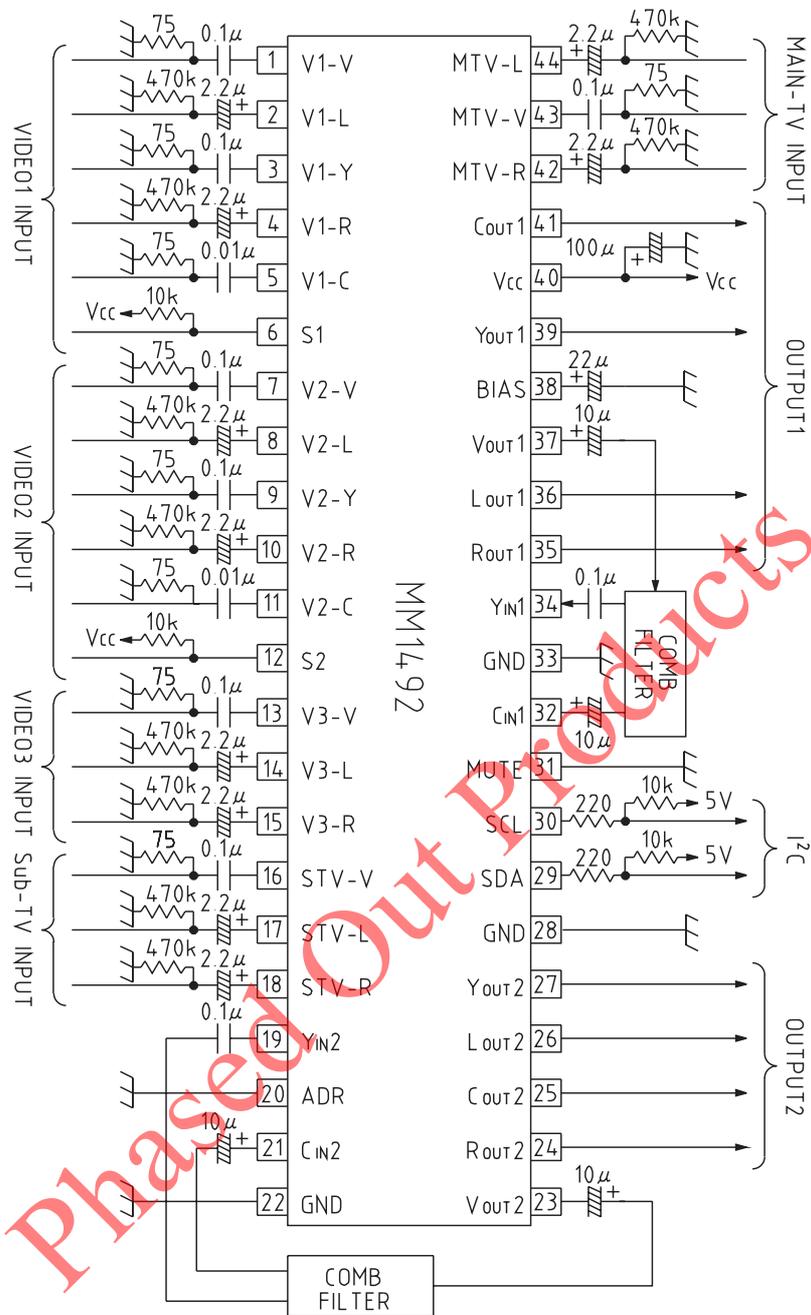
(2) Audio output 1

Mute terminal	b2	b1	b0	L <sub>out1</sub>	R <sub>out1</sub>
≤1.5V (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV-L	MTV-R
	0	1	0	V1-L	V1-R
	0	1	1	V2-L	V2-R
	1	0	0	V3-L	V3-R
	1	0	1	STV-L	STV-R
	1	1	0	Mute	Mute
	1	1	1		
≥3.0V				Mute	Mute

(3) Audio gain

b7	L <sub>out1</sub>	R <sub>out1</sub>
0	-6dB	-6dB
1	0dB	0dB

Application Circuit



Note.

(1) V<sub>OUT</sub> is set to 4.2V, While C<sub>IN</sub> is set to 4.9V.

Be careful since the capacity polarity may differ according to the comb filter bias.

(2) Each audio output can be set to myte by setting pin 31 to high. The mute is turned off in when pin 19 is open or low.