Protection for Lithium-Ion Batteries (4-serial cells)
Monolithic IC MM3114 Series

Outline

This IC integrates overcharge/overdischarge protection functions for lithium-ion/lithium polymer rechargeable batteries and the regulator functions into one chip by high voltage CMOS process. It can be used with other gas gauge IC, security IC, etc. as it includes a regulator. Overcharge/overdischarge can be detected to protect 4-cell lithium-ion/lithium polymer batteries. Charge/discharge control is perfomed using two external Pch MOS FETs.

Features

1. Overcharge detection voltage	Selectable between 4.0~4.5V by 5mV steps Accuracy ±25mV
2. Over-discharge detection voltage	Selectable between 2.0~3.0V by 100mV steps Accuracy ±80mV
3. No external capacitor for delay time required (delay time is set by the internal circuit)	
4. Regulator output voltage	Selectable between 2.0~4.0V by 0.2V steps Accuracy ±3%
5. Regulator load current	100mA max.
6. Operating temperature range	-40~85°C

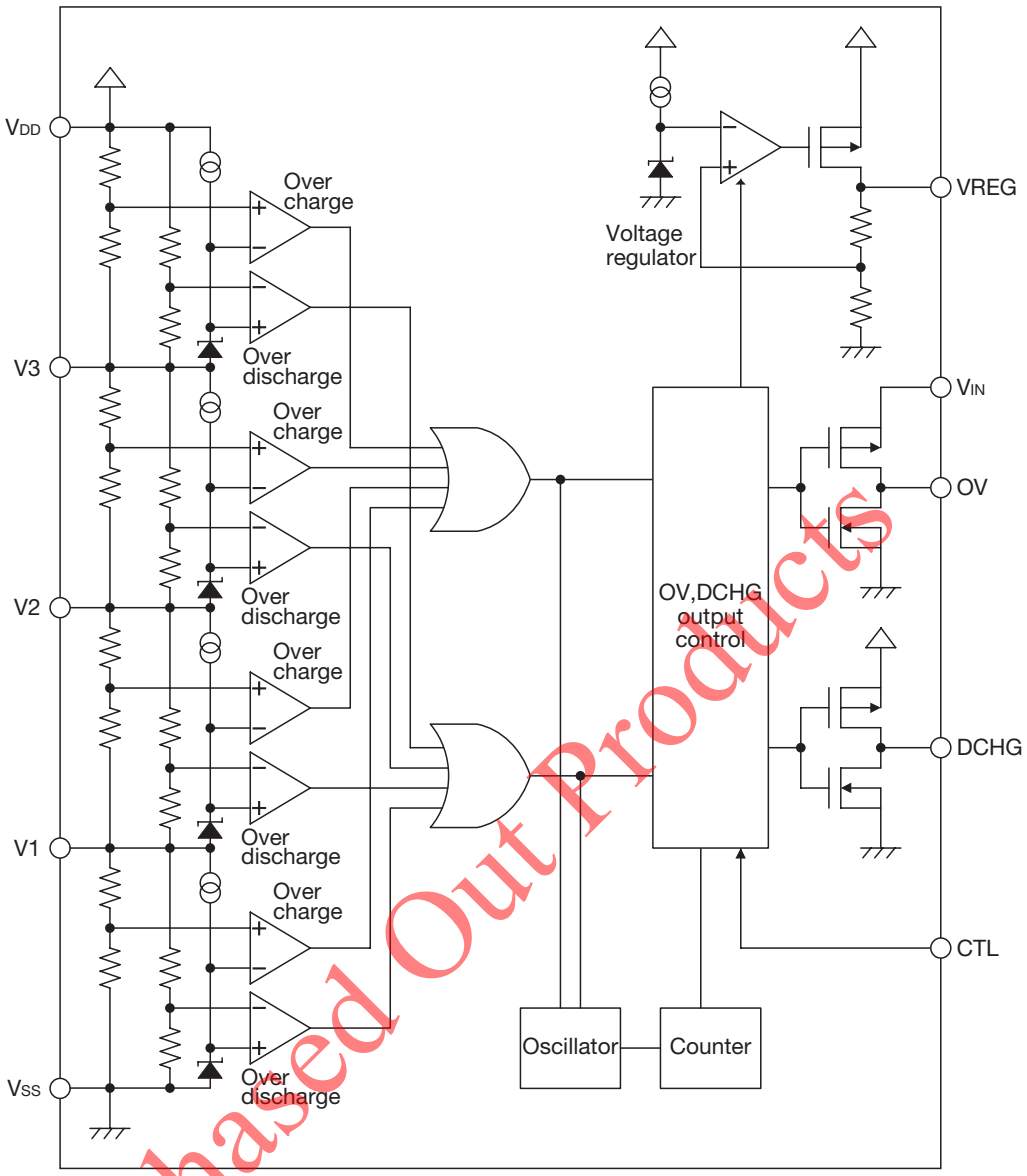
Package

VSOP-10A

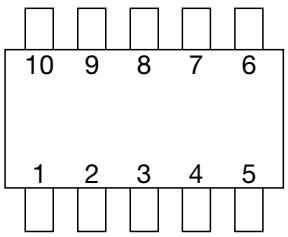
Applications

1. Lithium-ion battery pack (four cells).

Block Diagram



Pin Assignment



VSOP-10A
(TOP-VIEW)

1	DCHG
2	VDD
3	V3
4	V2
5	V1
6	VSS
7	VREG
8	CTL
9	VIN
10	OV

Pin Description

Pin No.	Symbol	I/O	Function
1	DCHG	Output	Output of over discharge detection. Output type is CMOS. ·Normal mode : "Low" ·Overdischarge mode : "High"
2	V_{DD}	Input	The input terminal of the power supply of IC, and the positive voltage of V4 cell.
3	V3	Input	The input terminal of the positive voltage of V3 cell, and the negative voltage of V4 cell.
4	V2	Input	The input terminal of the positive voltage of V2 cell, and the negative voltage of V3 cell.
5	V1	Input	The input terminal of the positive voltage of V1 cell, and the negative voltage of V2 cell.
6	V_{SS}	Input	The input terminal of the ground of IC, and the negative voltage of V1 cell.
7	VREG	Output	The output terminal of a voltage regulator. (3. 3V).
8	CTL	Input	The control terminal of FET for charge, and FET for discharge. ·CTL= "Low" : DCHG= "Low" Normal mode : OV= "Low" Normal mode ·CTL= "High" or "Open" : DCHG= "High" discharge prohibition : OV= "High" charge prohibition
9	V_{IN}	Input	The input terminal of the charger voltage.
10	OV	Output	Output of over charge detection. Output type is CMOS. ·Normal mode : "Low" ·Overcharge mode : "High"

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	–55~+125	°C
Operating temperature	T_{OPR}	–40~+85	°C
Supply voltage	$V_{DD\ max.}$	V_{SS}–0.3~V_{SS}+24	V
V_{IN} pin supply voltage	$V_{VIN\ max.}$	V_{SS}–0.3~V_{SS}+28	V
OV pin supply voltage	$V_{OV\ max.}$	V_{SS}–0.3~V_{IN}+0.3	V
DCHG pin supply voltage	$V_{DCHG\ max.}$	V_{SS}–0.3~V_{DD}+0.3	V
CTL pin supply voltage	$V_{CTL\ max.}$	V_{SS}–0.3~V_{DD}+0.3	V
Allowable loss	Pd	300	mW

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	–40~+85	°C
Supply voltage	V_{OPR}	V_{SS}+2.0~V_{SS}+18	V

Electrical Characteristics (Except where noted otherwise Ta=+25°C, $V_{IN}=V_{DD}$, V_{CELL}=3.5V)

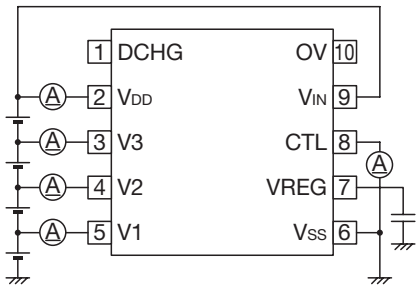
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	Circuit *2
Consumption current	I_{DD}	V_{CELL}=3.5V, I_{OUT}=0mA		10	20	µA	A
Current consumption at stand-by	I_S	V_{CELL}=1.8V, I_{OUT}=0mA $V_{IN}=V_{SS}$			0.1	µA	B
Pin3 (V3) nput current	I_{V3}	V_{CELL}=3.5V			±300	nA	A
Pin4 (V2) input current	I_{V2}	V_{CELL}=3.5V			±300	nA	A
Pin5 (V1) input current	I_{V1}	V_{CELL}=3.5V			±300	nA	A
Overcharge detection voltage	$V_{CELL}U$	Ta=0~+50°C *1 V_{CELL}=3.5V→4.5V	4.325	4.35	4.375	V	C
Overcharge release voltage	$V_{CELL}O$	V_{CELL}=4.5V→3.5V	$V_{CELL}U$ −260mV	$V_{CELL}U$ −200mV	$V_{CELL}U$ −140mV	V	C
Overcharge detection dead time	t_{OV}	V_{CELL}=3.5V→4.5V	50	100	150	ms	C
Overcharge release dead time	t_{OVREL}	V_{CELL}=4.5V→3.5V	10	20	40	ms	C
Overdischarge detection voltage	$V_{CELL}S$	V_{CELL}=3.5V→1.8V	2.22	2.3	2.38	V	D
Overdischarge release voltage	$V_{CELL}D$	$V_{IN}=V_{DD}$ V_{CELL}=1.8V→3.5V	2.7	2.8	2.9	V	D
Overdischarge detection dead time	t_{DC}	V_{CELL}=3.5V→1.8V	20	40	60	ms	D
Overdischarge release dead time	t_{DCREL}	V_{CELL}=1.8V→3.5V	10	20	40	ms	D
Pin1 (DCHG) source current	$I_{SO}D_{CH}$	V_{CELL} < $V_{CELL}S$ $V_{DCHG}=V_{DD}$−0.5V $V_{IN}=V_{SS}$	20			µA	E
Pin1 (DCHG) sink current	$I_{SI}D_{CH}$	V_{DCHG}=0.5V	20			µA	F
Pin1 (DCHG) output voltage H	$V_{TH}D_{CH}$	V_{CELL} < $V_{CELL}S$ $V_{DD}-V_{DCHG}$ I_{SO}=20µA $V_{IN}=V_{SS}$			0.5	V	E
Pin1 (DCHG) output voltage L	$V_{TH}D_{CL}$	$V_{DCHG}-V_{SS}$ I_{SI}=−20µA			0.5	V	F
Pin10 (OV) source current	$I_{SO}O_V$	V_{CELL} > $V_{CELL}U$ $V_{OV}=V_{IN}$−0.5V	20			µA	G
Pin10 (OV) sink current	$I_{SI}O_V$	V_{OV}=0.5V Ta=−40~85°C *1	20			µA	F
Pin10 (OV) output voltage H	$V_{TH}O_VH$	V_{CELL} > $V_{CELL}U$ $V_{IN}-V_{OV}$ I_{SO}=20µA			0.5	V	G
Pin10 (OV) output voltage L	$V_{TH}O_VL$	$V_{OV}-V_{SS}$ I_{SI}=−20µA Ta=−40~85°C *1			0.5	V	F
Pin7 (CTL) High current	I_{CTLH}	V_{CELL}=3.5V, $V_{CTL}=V_{DD}$			0.1	µA	H
Pin7 (CTL) Low current	I_{CTLL}	V_{CELL}=3.5V, $V_{CTL}=V_{SS}$	−1	−0.5		µA	A
Pin7 (CTL) High voltage	V_{CTLH}		V_{DD}×0.8			V	I
Pin7 (CTL) Low voltage	V_{CTLL}				V_{DD}×0.2	V	I
Pin8 (VREG) output voltage	V_{OUT}	V_{CELL}=3.5V, I_{OUT}=1mA	3.221	3.300	3.379	V	J
Pin8 (VREG) line regulation	ΔV_{OUT1}	V_{CELL}=2.4V→6V, I_{OUT}=1mA		5	15	mV	J
Pin8 (VREG) load regulation	ΔV_{OUT2}	V_{CELL}=3.5V, I_{OUT}=1→20mA		40	80	mV	J

*1 : The parameter is guaranteed by design.

*2 : The test circuit symbols on next page.

Measuring Circuit

A



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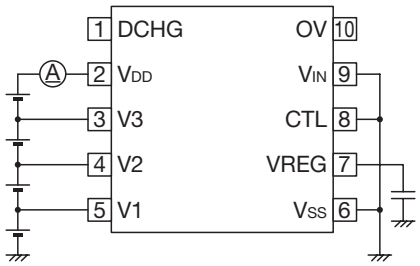

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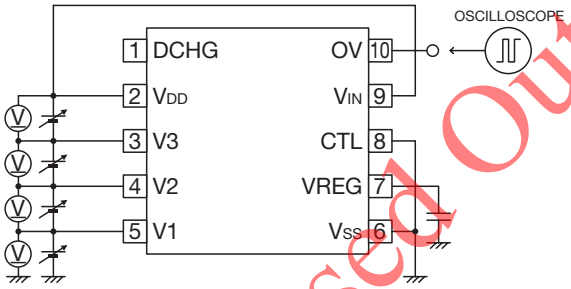

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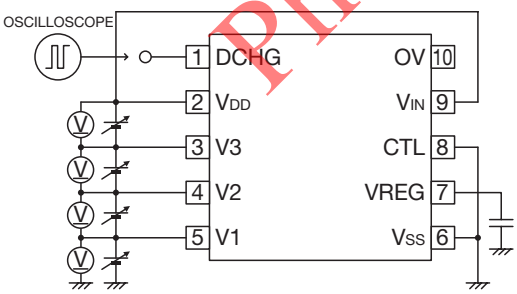

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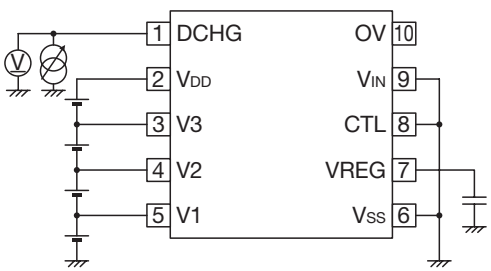

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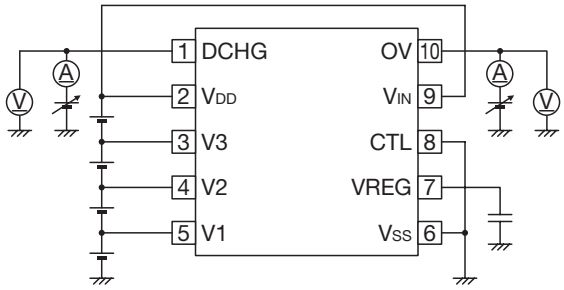

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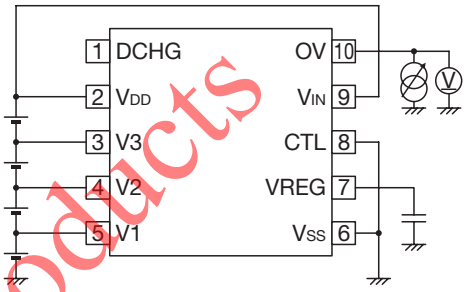

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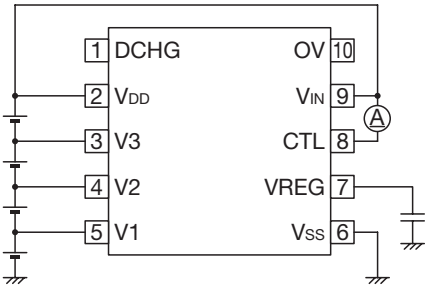

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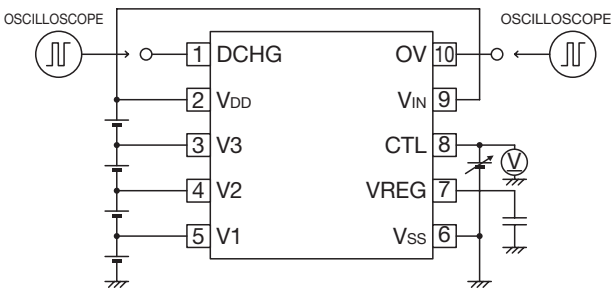

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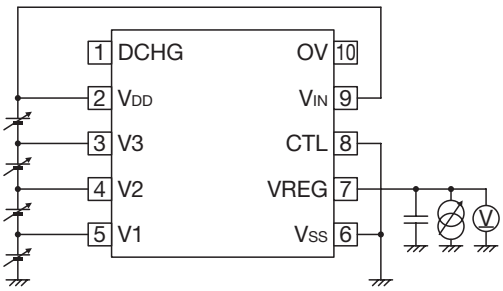
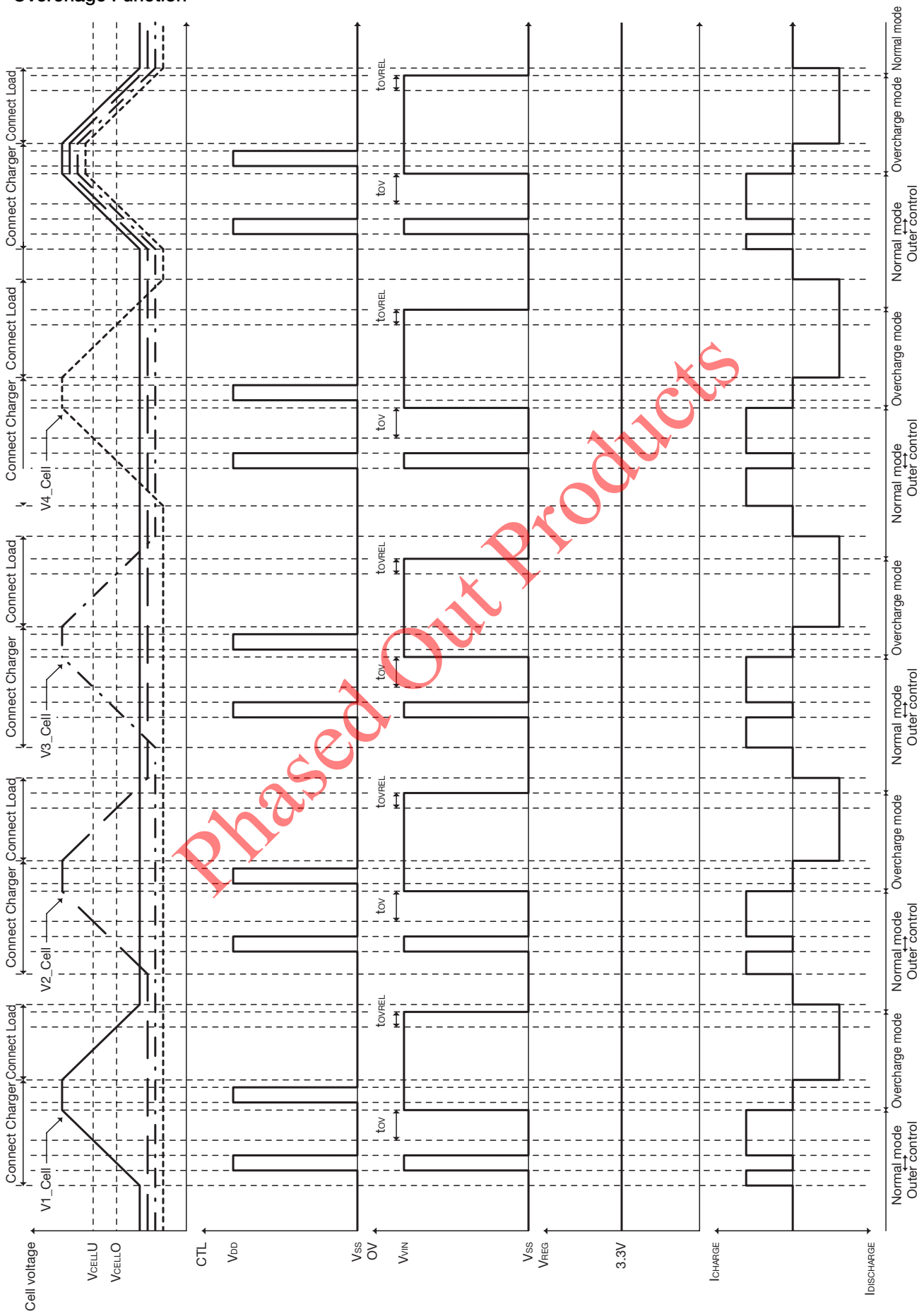
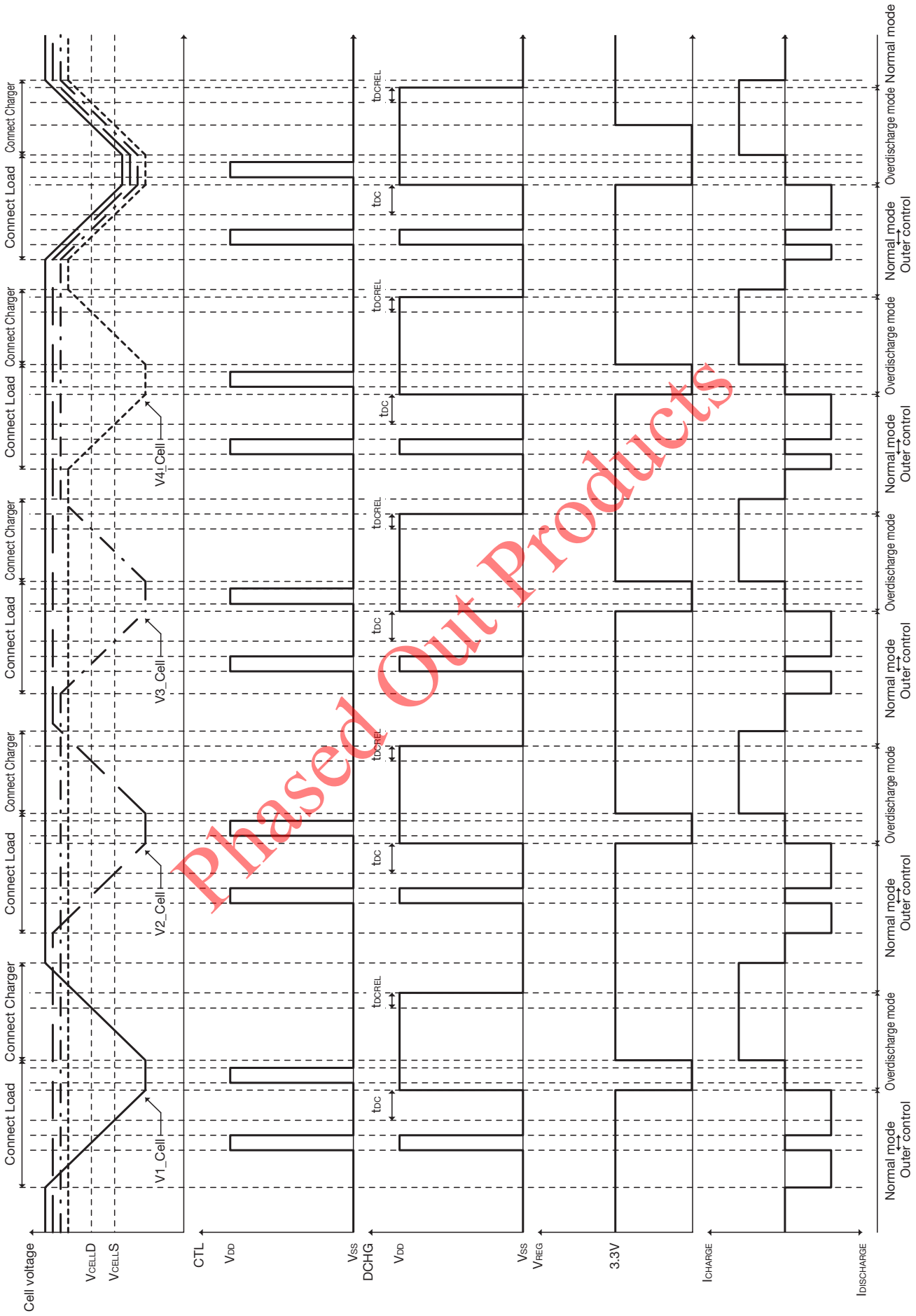


Timing chart

Overchage Function



Overdischage Function



Description

1. Over charge detector

· This IC monitors individual cell voltages. If any cell voltage exceeds the overcharge detection voltage (4.35V typ.) from a low value higher than the overcharge detection voltage, the IC sense a overcharging and external charging control Pch MOS FET turns to OFF with OV pin being high level.
· After detecting overcharge when the all cell voltages are coming down to a level lower than overcharge release voltage (4.15V typ.) external charging control Pch MOS FET turns to ON with OV pin being high level.
· After detecting overcharge in the cell voltage, connecting system load to the battery charger makes load current allowable supplied to parasitic diode of charging control FET. The OV pin level would be high when the cell voltage level is coming down to a level below the overcharge detection voltage by continuous sending a load current.
· There are delay time set in IC when the overcharge and the overcharge release are detected. When the V_{DD} level is going up to a higher level than overcharge detection voltage if the cell voltage would be back to a level lower than the overcharge detection voltage within a time period of the over charge release delay time (100ms typ). The overcharge detection does not release when returning to former state in the overcharge release dead time (20ms typ.) even if the load is connected after the charger is removed when the cell voltage is lower than the overcharge release voltage with the overcharge detected.
· A level shifter incorporated in a buffer drive for the OV to the V_{IN} pin voltage and the low level of OV is set to V_{SS} voltage with CMOS buffer.

2. Over discharge detector

· This IC monitors individual cell voltages. If any cell voltage crosses the overdischarge detection voltage (2.30V typ.) from high value to a value lower than the overdischarge detection voltage , this IC sense an overdischarge and an external discharging control Pch MOS FET turns to OFF with DCHG pin being at high level.
· The release from the overdischarge is done only by connecting the charger. Charging current is supplied through a parasitic diode of Pch MOS FET when the cell voltage is below the overdischarge detection voltage to the connection of the charger, and the DCHG pin enters the state which can be discharged by becoming low level, and turning on Pch MOS FET when the cell voltage rises more than the overdischarge detection voltage.
· The C_{OUT} pin becomes high level and charging current is supplied if the voltage of the charger is more than the maximum value of 0V charging lowest operating voltage when the voltage of the battery is 0V.
· An output delay time for the overdischarge detection is fixed internally (40m styp.). When cell voltage becomes lower the over discharge detection voltage if cell voltage higher more than the over discharge detection voltage in delay time even does not enter the over discharge detection mode. Moreover, when the over discharge release, delay time is set (20ms typ.).
· All the circuits are stopped, and after the overdischarge is detected, it is assumed the state of the standby, and decreases the current (standby current) which IC consumes as much as possible (The V_{CELL}=2V 0.1μA max.).
· The output type of DCHG pin is CMOS having high level of V_{DD} and low level of V_{SS}.

3. Discharging over current detector, Short detector (VD3, Short Detector)

· When the V- pin voltage is going up to a value during the short detection voltage (V_{DD}-0.9V typ.) and overdischarge current detection voltage (0.150V typ.) is overdischarge current detection mode, when the V- pin voltage higher than short detection voltage makes the short detection mode. This leads the external discharge control Nch MOS FET turns to OFF with the D_{OUT} pin being at low level.

· An output delay time for the overdischarge current detection is fixed internally (12ms typ.). When V- pin voltage becomes during the over discharge current detection voltage and the short circuit detection if V- pin lowers more than the over discharge current detection voltage in delay time even does not enter the over discharge current detection mode. Moreover, when the over discharge current release, delay time is set (4ms typ.).

· The delay time set in IC exists when the short circuit is detected (400ms typ.).

· The over discharge current release resistance (50kΩ typ.) is built into between V- pin and VSS pin. When the load opened after detecting the over discharge current or the short circuit, V- pin is pulled down to the V_{SS} through the over discharge current release resistance, And IC returns automatically from the over discharge current or the short circuit detection mode when V- pin voltage becomes below the over discharge current detection voltage. When the over discharge current or the short circuit is detected, the over discharge current release resistance is turned on. The over discharge current release resistance is usually turned off.

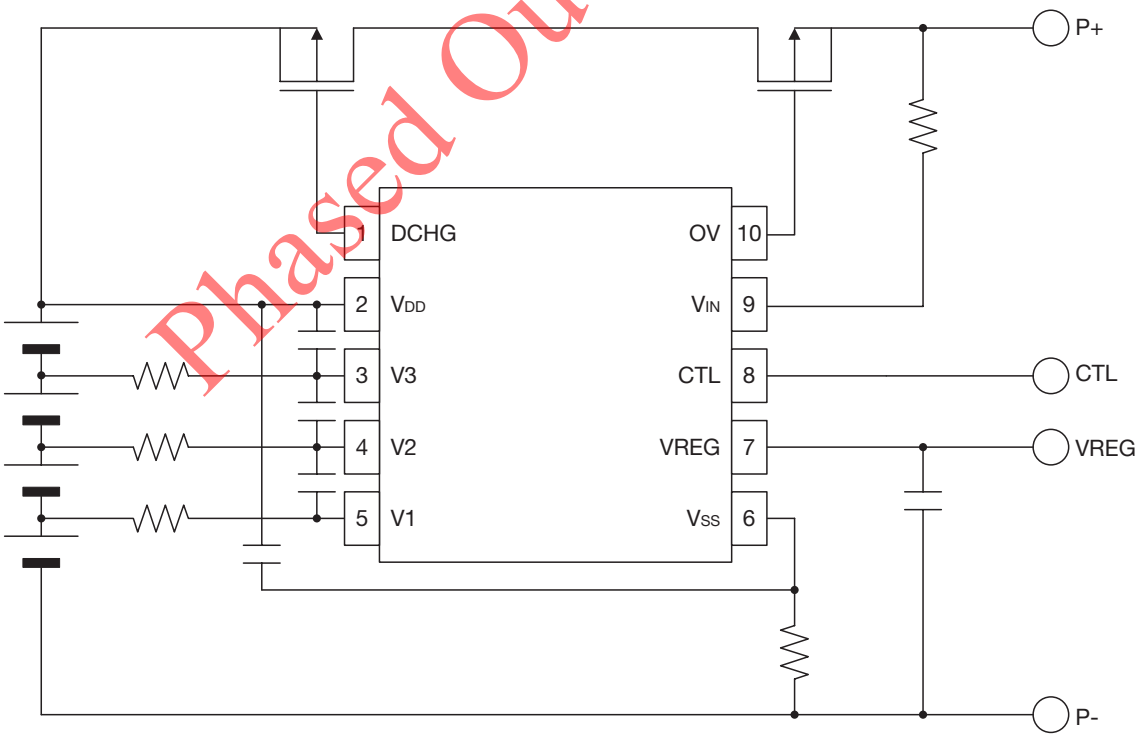
4. DS (Delay Shortening) function

· The overcharge, the over discharge, the over discharge current detection, and the delay time when returning can be shortened by impressing the V_{DD} voltage level to the terminal DS.

· In the DS pin, the pull-down resistance of 13kΩ is connected between V_{SS}.

· Please open the DS pin when using usually.

Application Circuit



· These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied.

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