I²C BUS AV-SW IC
Monolithic IC MM1783

Outline

This IC is a full HD compatible I²C BUS controlled audio video switch IC for LCD (middle-end to high-end), PDP, and rear-projection televisions.

· Operating supply voltage:
using two power supplies
Vcc1: 8.5V - 9.5V
Vcc2: 4.5V - 5.5V

· Input channels:
Composite video input: 7 channels
S Video input: 4 channels
Component input: 3 channels
Audio input: 10 channels

· Output channels
Video output: 3 channels
Audio input: 3 channels

Features

1. Full HD compatible (frequency response -3dB at 100MHz, for OUT1 only)
2. Integrates video and audio outputs into one chip
3. Enables RGB input (1600 x 1200 max. [UXGA])
4. Three type of LPF cutoff frequency can be selected.
   (OUT1, OUT2 fBW [=7MHz, 13MHz], fC [=24MHz])
5. Includes a 75Ω driver for monitor output (D1 resolution)
6. Supports S1/S2-terminal detection
7. Supports D-terminal detection
8. Detailed power saving function allows reduction in power consumption of unused circuits.
9. If D4 output is used, D4 mode function allows further reduction in power consumption.
10. Complies with the CENELEC SCART standard

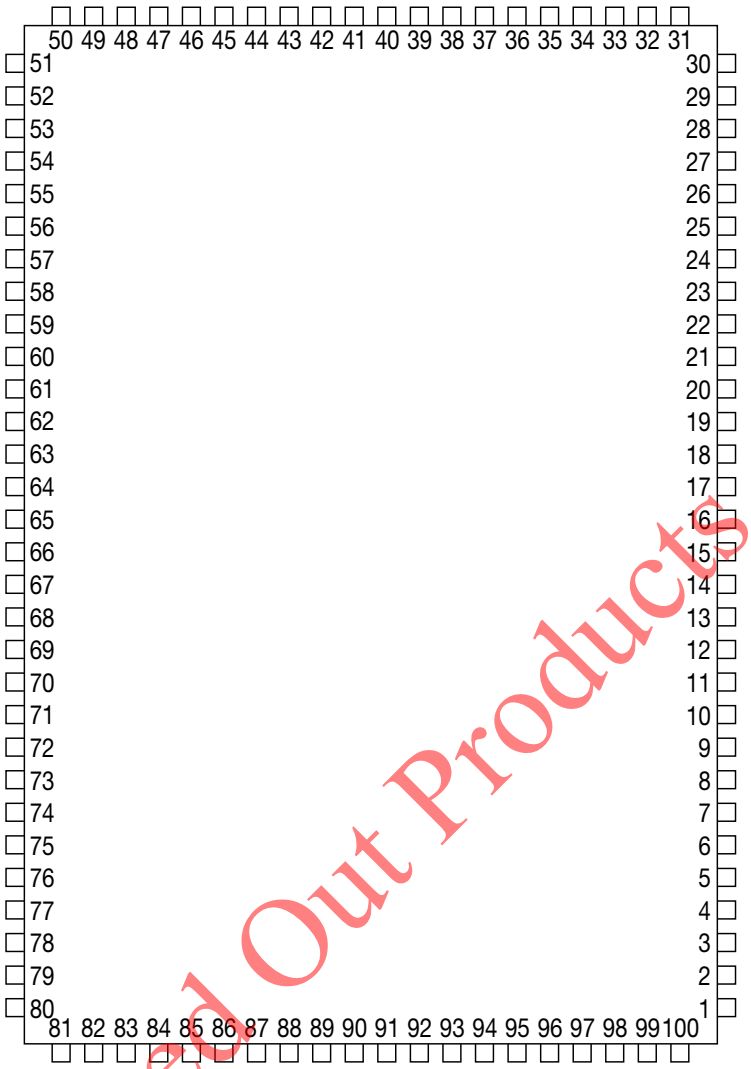
Package

QFP-100A

Applications

1. LCD TV (middle-end to high-end TV)
2. Plasma TV
3. Rear-projection TV
4. CRT TV

Pin Assignment

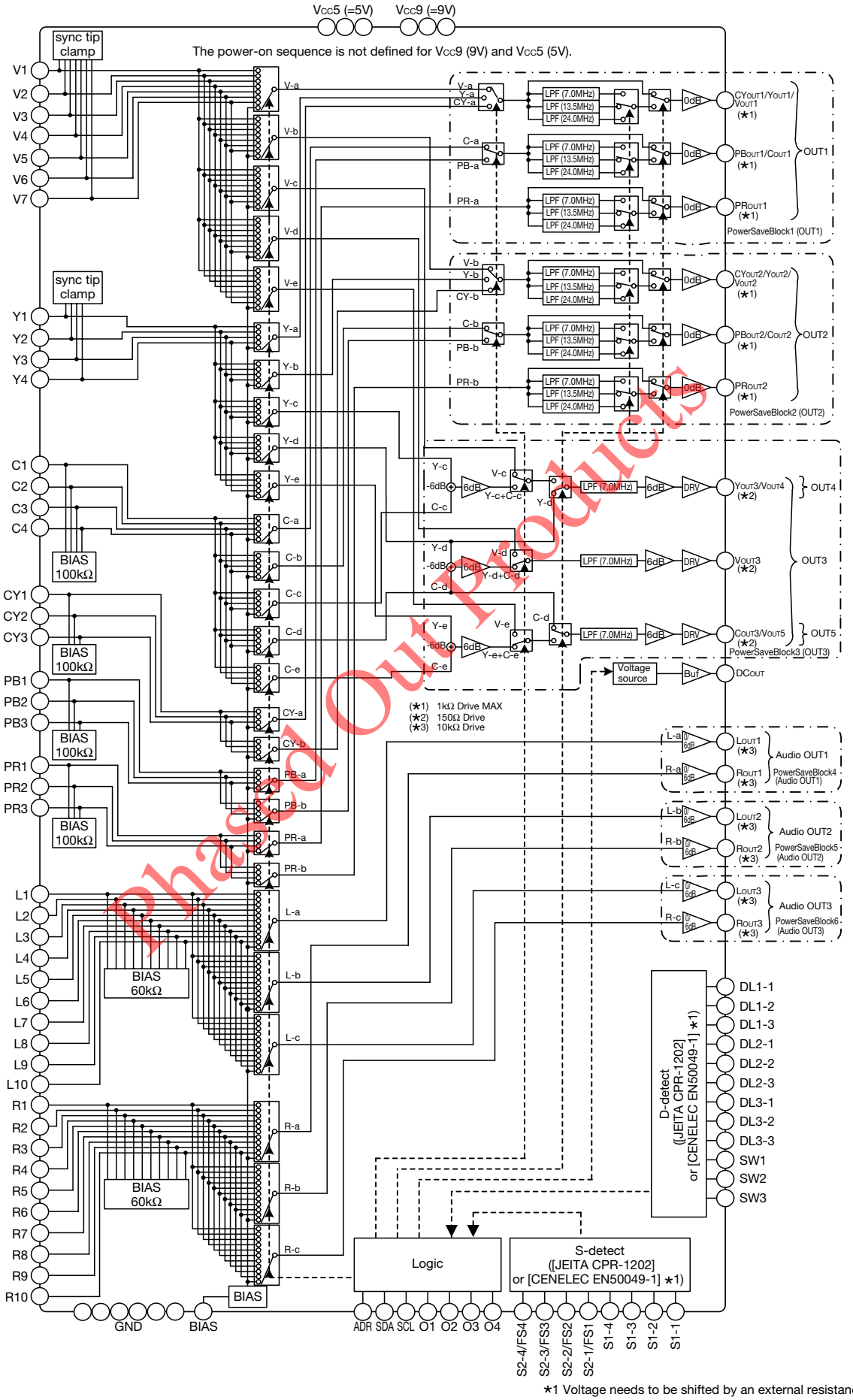


QFP-100A
(TOP VIEW)

1	S1-1	21	S2-4/FS4	41	R10	61	Vcc9	81	DL1-1
2	Y1	22	C4	42	L10	62	DCout	82	CY1
3	S2-1/FS1	23	O3	43	R9	63	Cout3	83	DL2-1
4	C1	24	V5	44	L9	64	GND	84	PB1
5	O1	25	GND	45	R8	65	Vout3	85	DL3-1
6	V2	26	V6	46	L8	66	Vcc5	86	PR1
7	S1-2	27	Vcc5	47	R7	67	Yout3	87	DL1-2
8	Y2	28	V7	48	L7	68	GND	88	CY2
9	S2-2/FS2	29	O4	49	R6	69	PRout2	89	DL2-2
10	C2	30	GND	50	L6	70	PBout2	90	PB2
11	BIAS	31	SCL	51	R5	71	CYout2	91	DL3-2
12	V3	32	SDA	52	L5	72	Vcc9	92	PR2
13	S1-3	33	Vcc9	53	R4	73	PRout1	93	DL1-3
14	Y3	34	Rout3	54	L4	74	PBout1	94	CY3
15	S2-3/FS3	35	Lout3	55	R3	75	CYout1	95	DL2-3
16	C3	36	Rout2	56	L3	76	ADR	96	PB3
17	O2	37	Lout2	57	R2	77	SW3	97	DL3-3
18	V4	38	Rout1	58	L2	78	SW2	98	PR3
19	S1-4	39	Lout1	59	R1	79	SW1	99	Vcc5
20	Y4	40	GND	60	L1	80	GND	100	V1

*: Vcc9=9V, Vcc5=5V

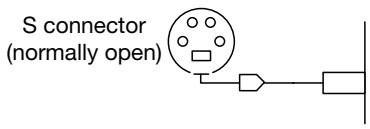
Block Diagram

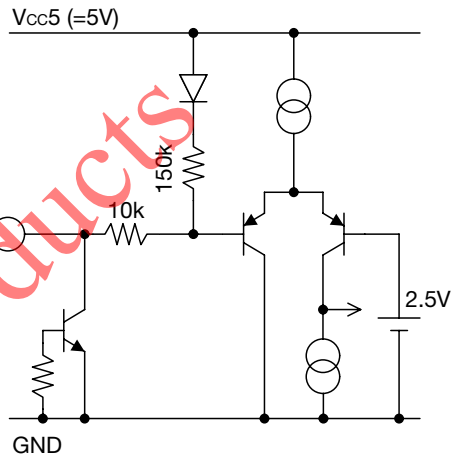


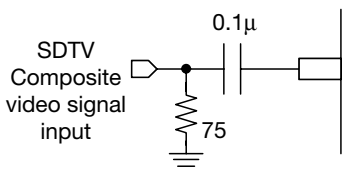
★1 Voltage needs to be shifted by an external resistance divider.

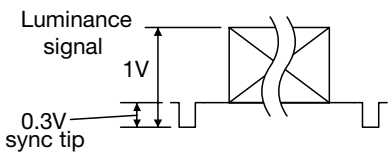
Pin Description

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">1
7
13
19</td><td rowspan="2">S1-1
S1-2
S1-3
S1-4</td><td>
Function
The terminal which detects the connection state of S connector
A detected result is reflected in a status register. (refer to [Status registers] [Output data of status registers & threshold])

Threshold: 2.4V typ.
Input impedance: 160kΩ typ.
External circuit


When not using it: open
Input signal
DC voltage:
0V (GND) or OPEN
Note:
When you impress voltage to a terminal, make it less than [6V].
</td><td>
Equivalent circuit diagram


</td></tr>
<tr><td rowspan="2">2
8
14
20</td><td rowspan="2">Y1
Y2
Y3
Y4</td><td>
Function
Luminance signal input
Input clamp
Pin voltage: 1.9V typ.
Input dynamic range: 1.3V_{P-P} min.
External circuit


When not using it: open
Input signal


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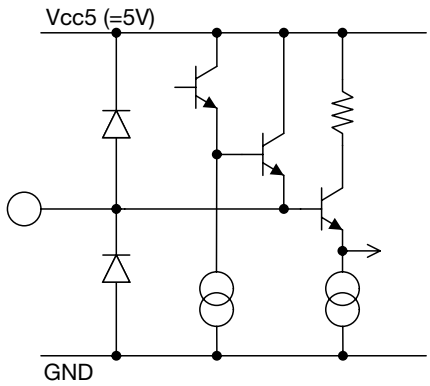
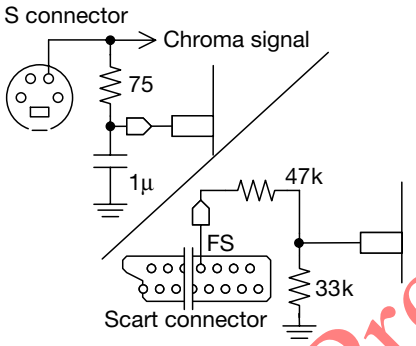
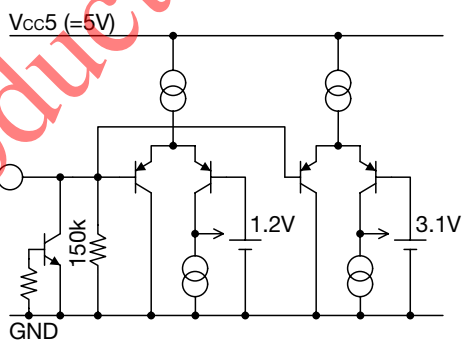
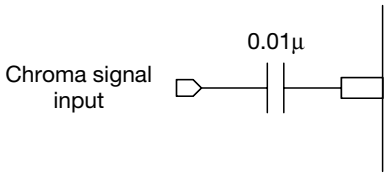
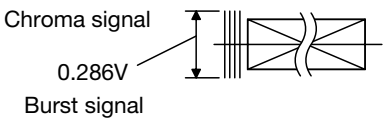
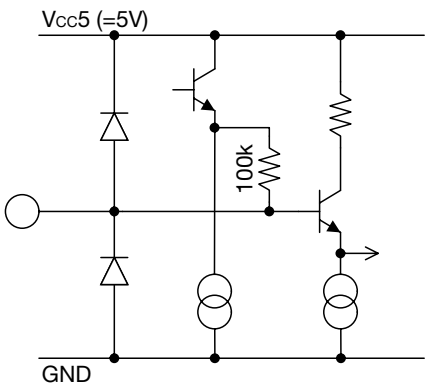
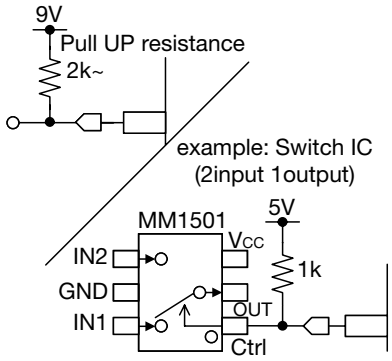
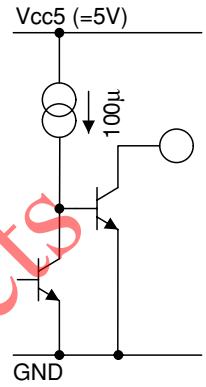
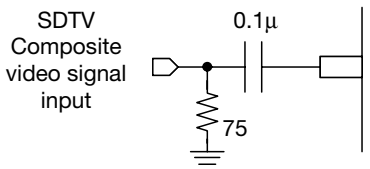
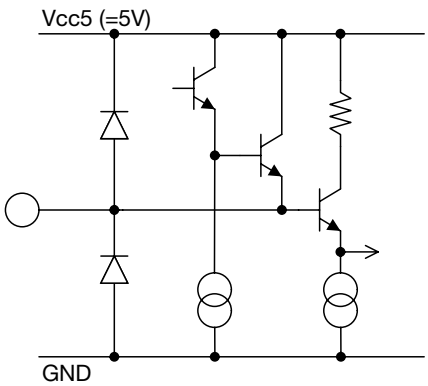
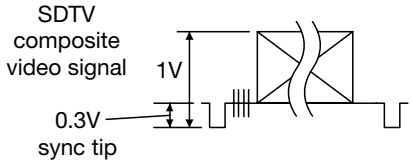
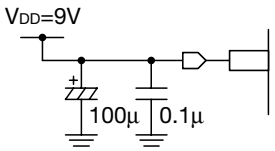
Equivalent circuit diagram


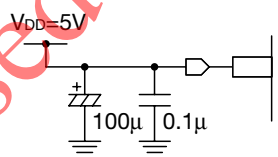
</td></tr>
</table>

Pin No.	Pin name	Pin description
3 9 15 21	S2-1/FS1 S2-2/FS2 S2-3/FS3 S2-4/FS4	**Function** The terminal which detects the aspect ratio information of S connector, or which detects the voltage of FS pin of a SCART interface. Note: When it is used for FS (Function Switching), connect outside circuit as the resistance division of 47kΩ and 33kΩ Threshold 1: 1.2V typ. Threshold 2: 3.1V typ. Input impedance: 150kΩ typ. **External circuit**  When not using it: open **Input signal** DC voltage: **Equivalent circuit diagram** 
4 10 16 22	C1 C2 C3 C4	**Function** Chroma signal input Input bias Pin voltage: 3.2V typ. Input impedance: 100kΩ typ. Input dynamic range: 1.3V_{P-P} min. **External circuit**  When not using it: open **Input signal**  **Equivalent circuit diagram** 

	S2	FS
L	0V	0–2V
M	1.4–2.4V	4.5–7V
H	3.5–5V	9.5–12V

Pin No.	Pin name	Pin description
5 17 23 29	O1 O2 O3 O4	**Function** Output port It is the open collector type general-purpose output port in which I²C control is possible. Sink current min.: 5mA **External circuit**  When not using it: open **Equivalent circuit diagram**  **Input signal** DC voltage: b53 / O1 (5pin): 0 Low; 1 Open (High) b52 / O2 (17pin): 0 Low; 1 Open (High) b51 / O3 (23pin): 0 Low; 1 Open (High) b50 / O4 (29pin): 0 Low; 1 Open (High)
6 12 18 24 26 28 100	V2 V3 V4 V5 V6 V7 V1	**Function** Composite signal input Input clamp Pin voltage: 1.9V typ. Input dynamic range: 1.3V_{P-P} min. **External circuit**  When not using it: open **Equivalent circuit diagram**  **Input signal** 

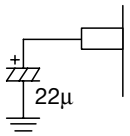
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>33
61
72</td><td>V_{CC9}</td><td>
Function
Voltage supply 1
It is a supply voltage impression terminal. Please impress 9V. 33 pin, 61 pin and 72 pin short-circuit inside IC. There is no regulation of the sequence of a power supply injection about V_{CC9} (9V) and V_{CC5} (5V).
Please arrange a bypass capacitor near the terminal.
External circuit


Equivalent circuit diagram
Input signal
DC Voltage:
+8.0~+10.0V
</td></tr>
<tr><td>27
66
99</td><td>V_{CC5}</td><td>
Function
Voltage supply 2
It is a supply voltage impression terminal. Please impress 5V. 27 pin, 66pin and 99 pin short-circuit inside IC. There is no regulation of the sequence of a power supply injection about V_{CC9} (9V) and V_{CC5} (5V).
Please arrange a bypass capacitor to the terminal latest as much as possible.
External circuit


Equivalent circuit diagram
Input signal
DC Voltage:
+4.5~+5.5V
</td></tr>
<tr><td>25
30
40
64
68
80</td><td>GND</td><td>
Function
Ground
It is a Ground terminal. 25pin, 30pin, 40pin, 64pin, 68pin and 80pin short-circuit inside IC.
External circuit
Equivalent circuit diagram
Input signal
</td></tr>
</table>

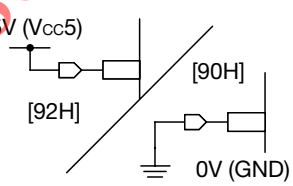
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">11</td><td rowspan="4">BIAS</td><td>Function

BIAS
All the reference voltage used inside IC is made based on resistance division of this terminal. It is the terminal which connects a filter capacitor to stabilize the reference voltage.

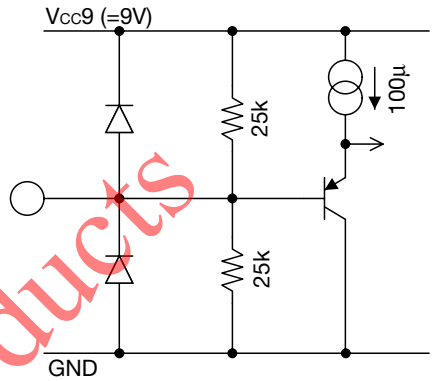
Input impedance: 12.6kΩ typ.</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

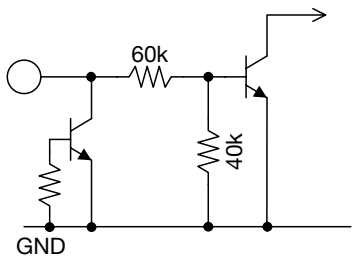
When not using it: open</td></tr>
<tr><td>Input signal</td></tr>
<tr><td rowspan="4">76</td><td rowspan="4">ADR</td><td>Function

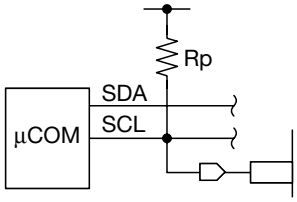
Slave address select pin
The I²C slave addresses 90H and 92H can be chosen with the voltage impressed to this terminal. It is set to 90H by Low, and is set to 92H by High.

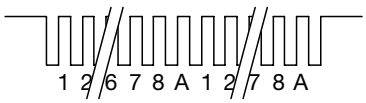
Threshold: 1.75V typ.
Input impedance: 100kΩ typ.</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

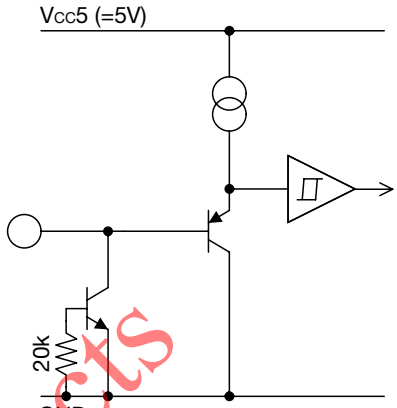
When not using it: open</td></tr>
<tr><td>Input signal

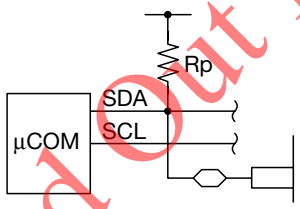
DC Voltage:
0V (GND) to 5V (Vcc5)</td></tr>
<tr><td colspan="2">Equivalent circuit diagram</td><td> 

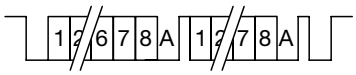

</td></tr>
</table>

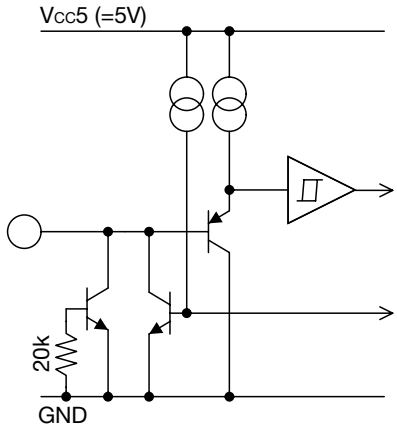
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">31</td><td rowspan="2">SCL</td><td>
Function
Clock input of I²C BUS
It is the terminal which connects the SCL line of I²C BUS.
External circuit


Input output signal
Input signal
Clock signal


Equivalent circuit diagram


</td></tr>
<tr><td>
Function
DATA I/O of I²C BUS
It is the terminal which connects the SDA line of I²C BUS.
External circuit


Input signal
Input signal
Control registers
Output signal
States registers


Equivalent circuit diagram


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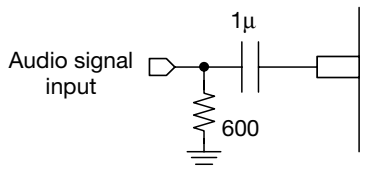
</table>

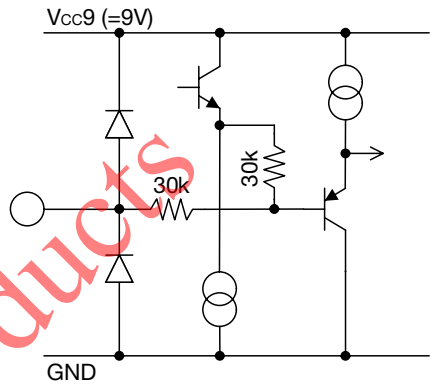
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">41~60</td><td rowspan="4">L1~L10
R1~R10</td><td>Function

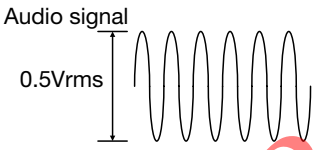
Audio line input
Pin to input audio signals. It includes 10 channels; L1-L10, R1-R10.

Pin voltage: 3.80V typ.
Input impedance: 60kΩ typ.
Input dynamic range: 3Vrms typ.</td></tr>
<tr><td>External circuit

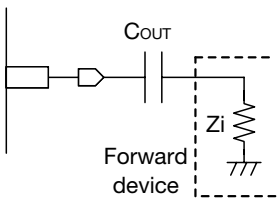
When not using it: connect to GND with 0.1µF</td><td>Equivalent circuit diagram

 
</td></tr>
<tr><td>Input signal

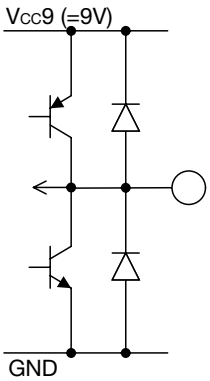
 
</td><td></td></tr>
<tr><td></td><td></td></tr>
<tr><td rowspan="4">34~39</td><td rowspan="4">LOUT1~3
ROUT1~3</td><td>Function

Audio line output
Pin to output audio signals
· Select voltage gain 0dB or 6dB with control registers b44 - b46.
Audio line output 1 (b46=0: 0dB mode, b46=1: 6dB mode)
Audio line output 2 (b45=0: 0dB mode, b45=1: 6dB mode)
Audio line output 3 (b44=0: 0dB mode, b44=1: 6dB mode)

Pin voltage: 4.50V typ.
Voltage gain: 0dB/6dB typ.
Frequency characteristic: –3dB at 50kHz min.</td></tr>
<tr><td>External circuit

$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$
*f_{CL}=1~10Hz
When not using it: open</td><td>Equivalent circuit diagram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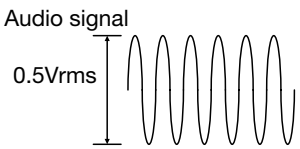
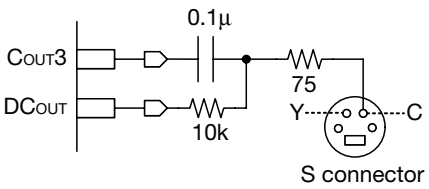
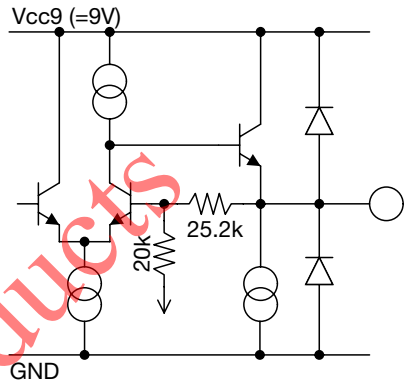
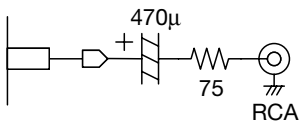
<tr><td>Input signal

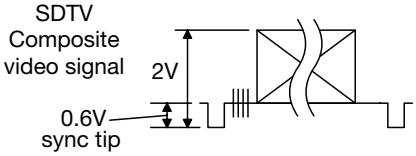
 
</td><td></td></tr>
<tr><td></td><td></td></tr>
</table>

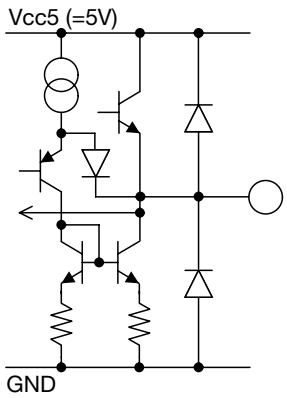
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">62</td><td rowspan="4">DCOUT</td><td>
Function
DC output for S terminal
It is the terminal which outputs S1/S2 signal of S terminal. The ternary output of L/M/H is controllable by I²C control. (refer to Table of status registers and Details of the contents of control)
</td></tr>
<tr><td>
External circuit


When not using it: open
</td></tr>
<tr><td>
Output signal
DC voltage:
<table>
<tr><th></th><th>b27</th><th>b26</th><th>DCOUT</th></tr>
<tr><td>L</td><td>0</td><td>0</td><td>0V</td></tr>
<tr><td>M</td><td>0</td><td>1</td><td>2.2V</td></tr>
<tr><td>H</td><td>1</td><td>0</td><td>5V</td></tr>
<tr><td></td><td>1</td><td>1</td><td>Hi-Imp</td></tr>
</table>
</td></tr>
<tr><td>
Equivalent circuit diagram


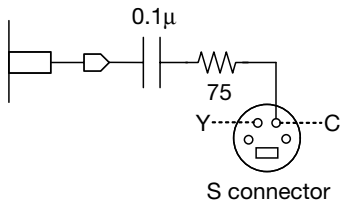
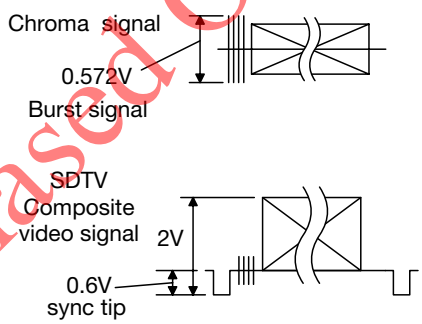
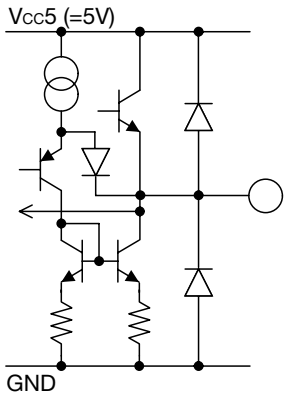
</td></tr>
<tr><td rowspan="4">65</td><td rowspan="4">VOUT3</td><td>
Function
Monitor output (composite signal)
It is a terminal for a composite signal external output. V or Y+C (MIX) can be chosen. (refer to Details of the contents of control)

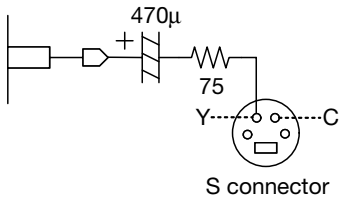
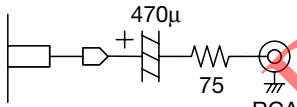
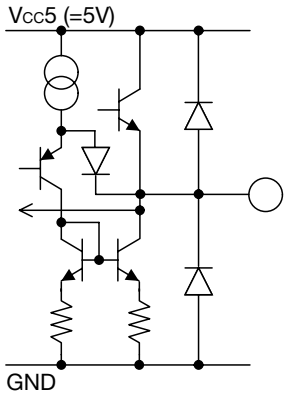
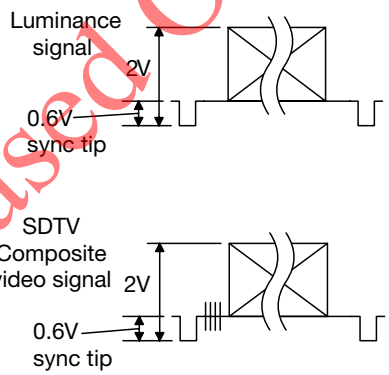
Pin voltage: 1.3V typ.
Load resistance: 150Ω
Stray capacitance max.: 20pF
</td></tr>
<tr><td>
External circuit


When not using it: open
</td></tr>
<tr><td>
Output signal


</td></tr>
<tr><td>
Equivalent circuit diagram


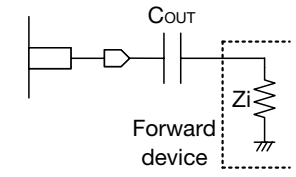
</td></tr>
</table>

Pin No.	Pin name	Pin description
63	COUT3/VOUT6	**Function** Monitor output (chroma or composite signal) It is a terminal for the chroma or composite signal external output. It becomes the chroma output terminal at the time of the separate switch OFF [b24=0], and becomes a composite output terminal at the time of the separate switch ON [b24=1]. C, V, and Y+C (MIX) can be chosen. (refer to Details of the contents of control) Pin voltage: 2.6V typ. [b24=0], 1.3V typ. [b24=1] Load resistance: 150Ω Stray capacitance max.: 20pF **External circuit**  When not using it: open **Output signal**  **Equivalent circuit diagram** 

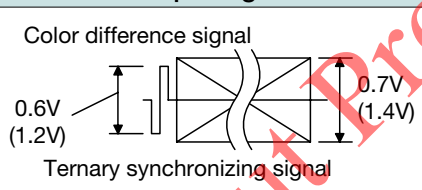
Pin No.	Pin name	Pin description
67	YOUT3/VOUT5	**Function** Monitor output (Luminance or composite signal) It is a terminal for a Luminance or composite signal external output. It becomes a Luminance output terminal at the time of the separate switch OFF [b24=0], and becomes a composite output terminal at the time of the separate switch ON [b24=1]. Y, V, or Y+C (MIX) can be chosen. (refer to Details of the contents of control) Pin voltage: 1.3V typ. Load resistance: 150Ω Stray capacitance max.: 20pF **External circuit** / **Equivalent circuit diagram**   When not using it: open  **Output signal** 

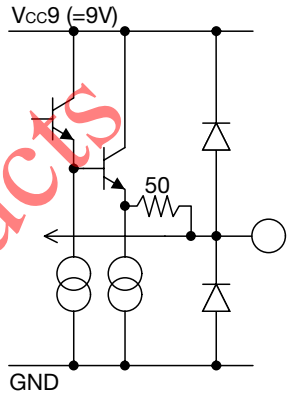
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>69</td><td>PROUT2</td><td>
Function
Color difference signal output
It is a terminal for a Color difference signal external output.

Pin voltage: 4.4V typ.
Load resistance min.: 1kΩ
Stray capacitance max.: 10pF

External circuit


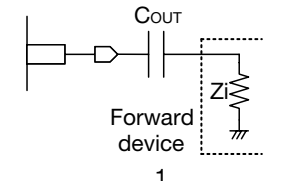
$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$
*fCL=1~10Hz
When not using it: open

Output signal


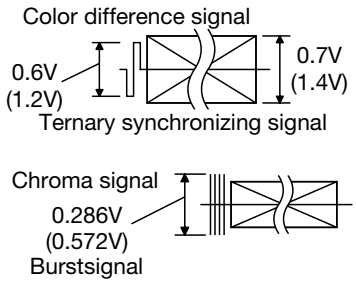
Equivalent circuit diagram


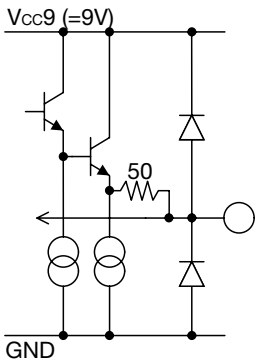
</td></tr>
<tr><td>70</td><td>PBOUT2/COUT2</td><td>
Function
Color difference signal or Chroma signal output
It is a terminal for a Color difference or Chroma signal external output.

Pin voltage: 4.4V typ.
Load resistance min.: 1kΩ
Stray capacitance max.: 10pF

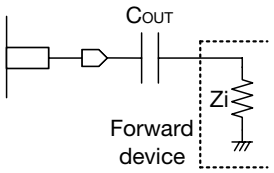
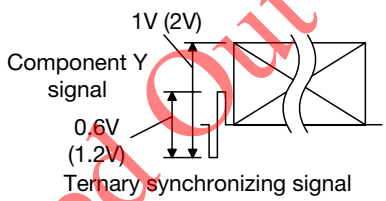
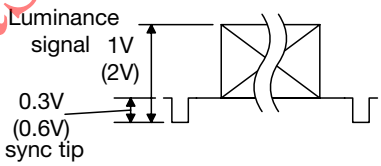
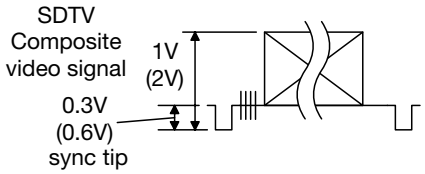
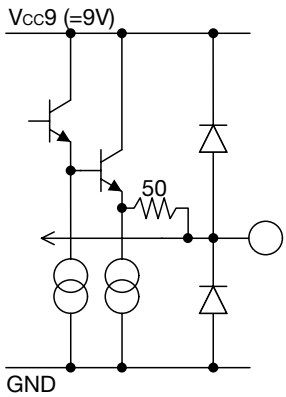
External circuit


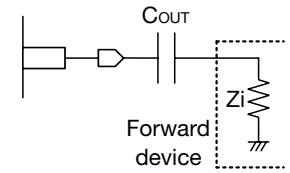
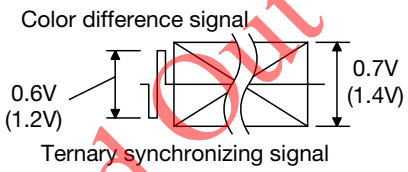
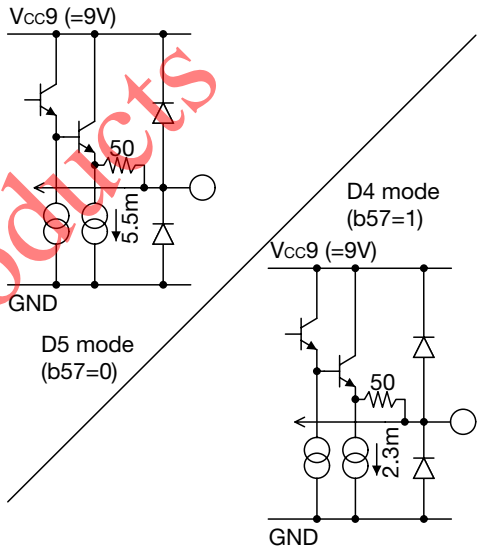
$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$
*fCL=1~10Hz
When not using it: open

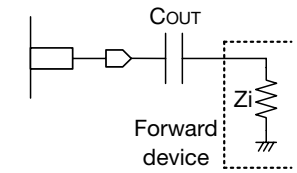
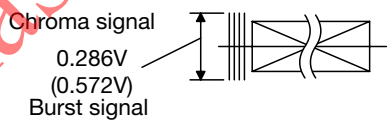
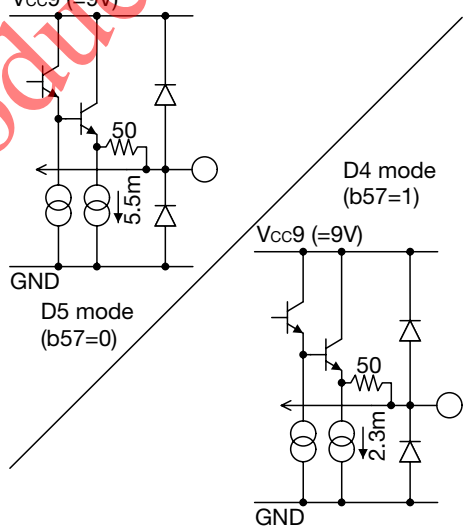
Output signal


Equivalent circuit diagram


</td></tr>
</table>

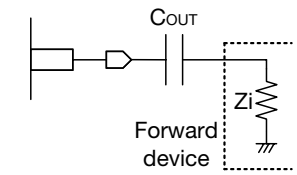
Pin No.	Pin name	Pin description
71	CYOUT2 /YOUT2 /VOUT2	**Function** Color difference signal , Luminance signal or Composite signal output It is a terminal for a Color difference or Luminance or Composite signal external output. Pin voltage: 2.2V typ. [V, Y] , 4.4V typ. [CY] Load resistance min.: 1kΩ Stray capacitance max.: 10pF **External circuit**  $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$ *f_{CL}=1~10Hz When not using it: open **Output signal**    **Equivalent circuit diagram** 

Pin No.	Pin name	Pin description
73	PROUT1	**Function** Color difference signal output It is a terminal for a Color difference signal external output. It can be switched with D5 mode or D4 mode. D4 mode is lower power than D5 mode. Pin voltage: 4.4V typ. Load resistance min.: 1kΩ Stray capacitance max.: 10pF **External circuit**  $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$ *f_{CL}=1~10Hz When not using it: open **Output signal**  **Equivalent circuit diagram** 

Pin No.	Pin name	Pin description
74	PBOUT1/COUT1	**Function** Color difference signal or Chroma signal output It is a terminal for a Color difference or Chroma signal external output. It can be switched with D5 mode or D4 mode. D4 mode is lower power than D5 mode. Pin voltage: 4.4V typ. Load resistance min.: 1kΩ Stray capacitance max.: 10pF **External circuit**  $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$ *f_{CL}=1~10Hz When not using it: open **Output signal**   **Equivalent circuit diagram** 

Pin No.	Pin name	Pin description
75	CYOUT1 /YOUT1 /VOUT1	**Function** Color difference signal , Luminance signal or Composite signal output It is a terminal for a Color difference or Luminance or Composite signal external output. It can be switched with D5 mode or D4 mode. D4 mode is lower power than D5 mode. Pin voltage: 2.2V typ. [V, Y] , 4.4V typ. [CY] Load resistance min.: 1kΩ Stray capacitance max.: 10pF

External circuit

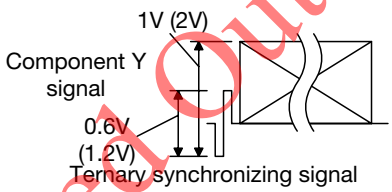


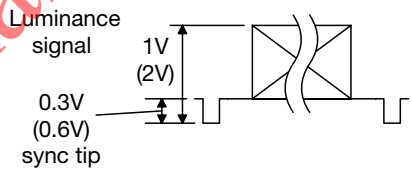
$$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$$

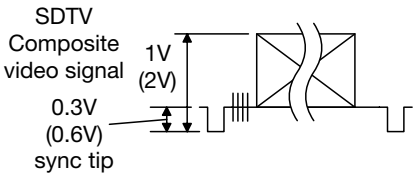
*f_{CL}=1~10Hz

When not using it: open

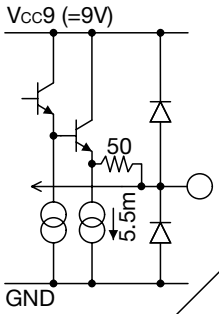
Output signal

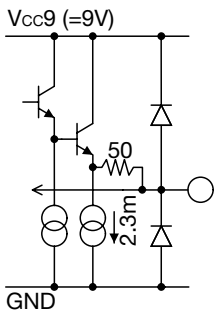




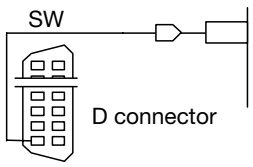


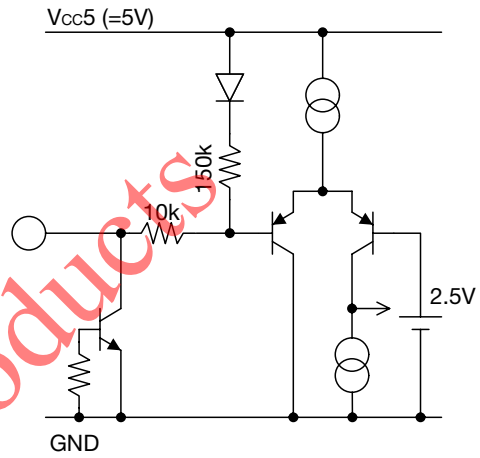
Equivalent circuit diagram



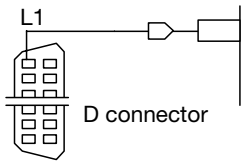


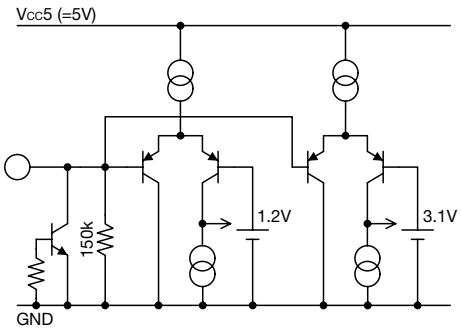
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">77
78
79</td><td rowspan="2">SW3
SW2
SW1</td><td>
Function
The terminal which detects the connection state of D connector.
A detected result is reflected in a status register.(refer to [Status registers] [Output data of status registers & threshold])

Threshold: 2.4V typ.
Input impedance: 160kΩ typ.
External circuit


When not using it: open
Input signal
DC voltage:
0V (GND) or OPEN
Note:
When you impress voltage to a terminal, make it less than [6V].
</td><td>
Equivalent circuit diagram


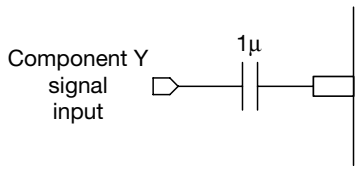
</td></tr>
<tr><td rowspan="2">81
87
93</td><td rowspan="2">DL1-1
DL1-2
DL1-3</td><td>
Function
The terminal which detects the number-of-scanning-lines information on D connector.
A detected result is reflected in a status register.(refer to [Status registers] [Output data of status registers & threshold])

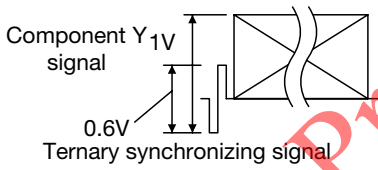
Threshold 1: 1.2V typ.
Threshold 2: 3.1V typ.
Input impedance: 150kΩ typ.
External circuit


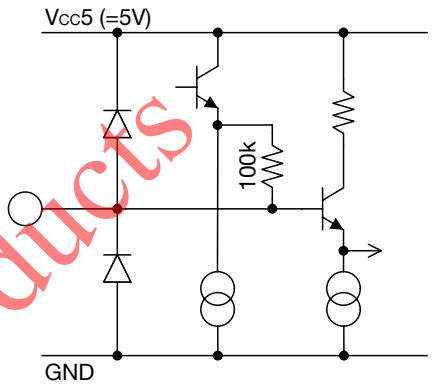
When not using it: open
Input signal
DC voltage:
<table>
<tr><td>L</td><td>0V</td></tr>
<tr><td>M</td><td>1.4–2.4V</td></tr>
<tr><td>H</td><td>3.5–5V</td></tr>
</table>
</td><td>
Equivalent circuit diagram


</td></tr>
</table>

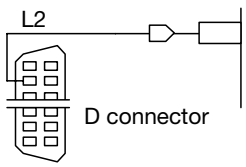
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">82
88
94</td><td rowspan="4">CY1
CY2
CY3</td><td>
Function
Component Y signal input
A RGB signal can also be inputted besides a component Y signal.

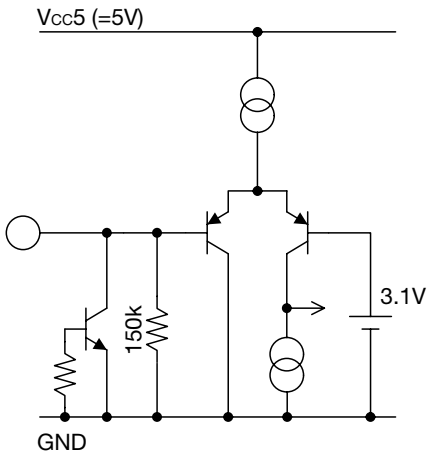
Input bias
Pin voltage: 3.2V typ.
Input impedance: 100kΩ typ.
Input dynamic range: 1.6V_{P-P} min.
External circuit


When not using it: open
Input signal


</td><td>
Equivalent circuit diagram


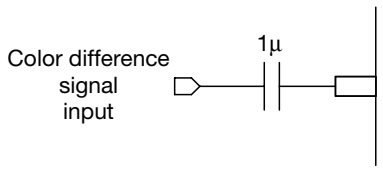
</td></tr>
<tr><td rowspan="3">83
89
95</td><td rowspan="3">DL2-1
DL2-2
DL2-3</td><td>
Function
The terminal which detects the I/P information of D connector.
A detected result is reflected in a status register. (refer to [Status registers] [Output data of status registers & threshold])

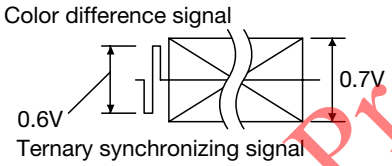
Threshold: 3.1V typ.
Input impedance: 150kΩ typ.
External circuit


When not using it: open
Input signal
DC voltage:
<table>
<tr><th></th><th>L2</th></tr>
<tr><td>M</td><td>0V</td></tr>
<tr><td>H</td><td>3.5–5V</td></tr>
</table>
</td><td>
Equivalent circuit diagram


</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">84
90
96</td><td rowspan="2">PB1
PB2
PB3</td><td>
Function
Color difference signal input
A RGB signal can also be inputted besides a color-difference signal.

Input bias
Pin voltage: 3.2V typ.
Input impedance: 100kΩ typ.
Input dynamic range: 1.6V_{P-P} typ.
External circuit


When not using it: open
Input signal


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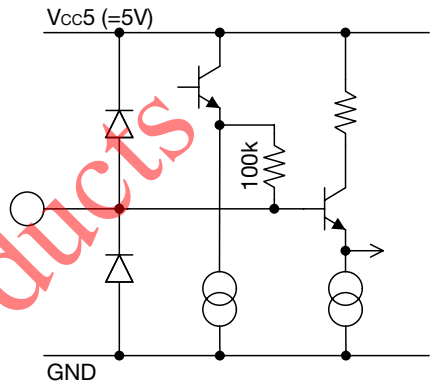
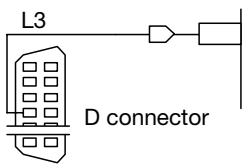
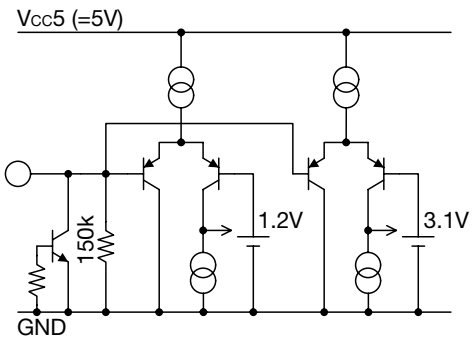
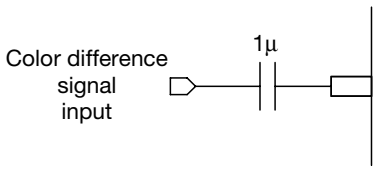
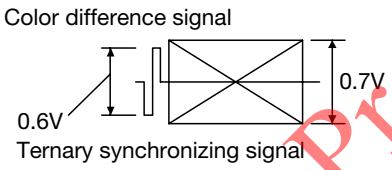
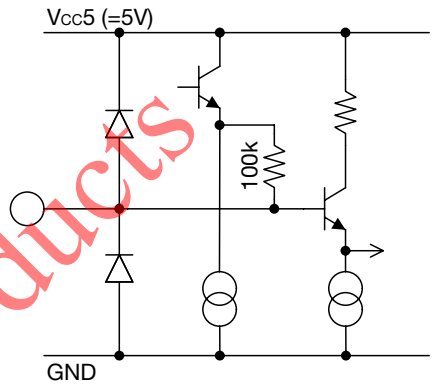
Equivalent circuit diagram


</td></tr>
<tr><td colspan="2"></td></tr>
<tr><td rowspan="2">85
91
97</td><td rowspan="2">DL3-1
DL3-2
DL3-3</td><td>
Function
The terminal which detects the aspect ratio information of D connector.
A detected result is reflected in a status register.(refer to [Status registers] [Output data of status registers & threshold])

Threshold 1: 1.2V typ.
Threshold 2: 3.1V typ.
Input impedance: 150kΩ typ.
External circuit


When not using it: open
Input signal
DC voltage:
<table>
<tr><th></th><th>L3</th></tr>
<tr><td>L</td><td>0V</td></tr>
<tr><td>M</td><td>1.4–2.4V</td></tr>
<tr><td>H</td><td>3.5–5V</td></tr>
</table>
</td><td>
Equivalent circuit diagram


</td></tr>
</table>

Pin No.	Pin name	Pin description
86 92 98	PR1 PR2 PR3	**Function** Color difference signal input A RGB signal can also be inputted besides a color-difference signal. Input bias Pin voltage: 3.2V typ. Input impedance: 100kΩ typ. Input dynamic range: 1.6V_{P-P} typ. **External circuit**  When not using it: open **Input signal**  **Equivalent circuit diagram** 

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	–65~+150	°C
Operating temperature	T_{OPR}	–40~+85	°C
Supply voltage 1	$V_{CC9max.}$	–0.2~+10.0	V
Supply voltage 2	$V_{CC5max.}$	–0.2~+6.0	V
Input voltage 1	$V_{IN1max.}$	–0.2~V_{CC9}+0.2	V
Input voltage 2	$V_{IN2max.}$	–0.2~V_{CC5}+0.2	V
Output voltage 1	$V_{OUT9max.}$	–0.2~V_{CC9}+0.2	V
Output voltage 2	$V_{OUT5max.}$	–0.2~V_{CC5}+0.2	V
Output current	$I_{OUTmax.}$	25	mA
Junction temperature	$T_{jmax.}$	150	°C
Thermal resistance	θ j–c	6.0	°C/W
Allowable loss (*1)	Pd	3.6	W

Note1: *1 Board mounting allowable loss. Board size 193×189×1.6mm

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	–40~+85	°C
Operating voltage 1	V_{CC9OP}	+8.0~+10.0	V
Operating voltage 2	V_{CC5OP}	+4.5~+5.5	V

Electrical Characteristics (Except where noted otherwise Ta=25°C, $V_{CC}9$=9V, $V_{CC}5$=5V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption							
Current consumption	$V_{CC}9$ (9V)	$I_{CC9\text{-}0}$	[b05, b15, b25, b57, b56, b55, b54=' 0, 0, 0, 0, 0, 0, 0 ']	42	70	98	mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}0}$		54	90	126	
All Power save current consumption							
All Power save current consumption	$V_{CC}9$ (9V)	$I_{CC9\text{-}0}$	[b05, b15, b25, b56, b55, b54=' 1, 1, 1, 1, 1, 1 ']	5	10	15	mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}0}$		27	45	63	
Block current consumption							
OUT1 Block current consumption (refer to block diagram)	$V_{CC}9$ (9V)	$I_{CC9\text{-}V1}$	Icc [b05=' 0 '] –Icc [b05=' 1 ']		30		mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}V1}$			8		
OUT2 Block current consumption (refer to block diagram)	$V_{CC}9$ (9V)	$I_{CC9\text{-}V2}$	Icc [b15=' 0 '] –Icc [b15=' 1 ']		20		mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}V2}$			8		
OUT3 Block current consumption (refer to block diagram)	$V_{CC}9$ (9V)	$I_{CC9\text{-}V3}$	Icc [b25=' 0 '] –Icc [b25=' 1 ']		0		mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}V3}$			30		
AUDIO OUT1 Block current consumption (refer to block diagram)	$V_{CC}9$ (9V)	$I_{CC9\text{-}A1}$	Icc [b56=' 0 '] –Icc [b56=' 1 ']		4		mA
AUDIO OUT2 Block current consumption (refer to block diagram)	$V_{CC}9$ (9V)	$I_{CC9\text{-}A2}$	Icc [b55=' 0 '] –Icc [b55=' 1 ']		4		mA
AUDIO OUT3 Block current consumption (refer to block diagram)	$V_{CC}9$ (9V)	$I_{CC9\text{-}A3}$	Icc [b54=' 0 '] –Icc [b54=' 1 ']		4		mA
Graphics Resolution current consumption	$V_{CC}9$ (9V)	$I_{CC9\text{-}GR}$	Icc [b57=' 0 '] –Icc [b57=' 1 ']		10		mA
Input pin voltage							
Input pin voltage 1(V, Y)		V_{IN1}	100, 6, 12, 18, 24, 26, 28, 2, 8, 14, 20 pin	1.4	1.9	2.4	V
Input pin voltage 2 (C, CY, PB, PR)		V_{IN2}	4, 10, 16, 22, 82, 84, 86, 88, 90, 92, 94, 96, 98 pin	2.6	3.2	3.8	V
Input pin voltage 3 (L, R)		V_{IN3}	41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60 pin	3.2	3.8	4.4	V
Output pin voltage (OUT1, 2)							
Output pin voltage 1 (V, Y)		V_{OUT1}	70, 71, 74, 75 pin	1.8	2.2	2.6	V
Output pin voltage 2 (C, CY, PB, PR)		V_{OUT2}	63, 69, 70, 71, 73, 74, 75 pin	4.0	4.4	4.8	V
Output pin voltage (OUT3, 4, 5)							
Output pin voltage 3 (V, Y)		V_{OUT3}	65, 67 pin	0.9	1.3	1.7	V
Output pin voltage 4 (C)		V_{OUT4}	63 pin	2.2	2.6	3.0	V
Audio output pin voltage (OUT1, 2, 3)							
Audio output pin voltage (L, R)		V_{OUT5}	34, 35, 36, 37, 38, 39 pin	4.1	4.5	4.9	V
S-DCOUT pin output voltage							
S-DCOUT pin output voltage	L	$V_{DCOUT\,L}$	62 pin R_L=10kΩ+100kΩ	GND	0.1	0.5	V
	M	$V_{DCOUT\,M}$	62 pin R_L=10kΩ+100kΩ	1.6	2.1	2.4	V
	H	$V_{DCOUT\,H}$	62 pin R_L=10kΩ+100kΩ	4.3	4.6	$V_{CC}5$	V

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Bias input impedance							
CIN input impedance		ZCIN	4, 10, 16, 22 pin	70	100	130	kΩ
CYIN input impedance		ZCYIN	82, 88, 94 pin	70	100	130	kΩ
PbIN input impedance		ZPbIN	84, 90, 96 pin	70	100	130	kΩ
PrIN input impedance		ZPrIN	86, 92, 98 pin	70	100	130	kΩ
LIN input impedance		ZLIN	60, 58, 56, 54, 52, 50, 48, 46, 44, 42 pin	47	60	73	kΩ
RIN input impedance		ZRIN	59, 57, 55, 53, 51, 49, 47, 45, 43, 41 pin	47	60	73	kΩ
VOUT3 (65pin) electrical characteristics							
VOUT3 Voltage gain		GvVOUT3	SIN wave: 1V f=100kHz	5.7	6.0	6.3	dB
VOUT3 Frequency characteristic	with filter	f1VOUT3	SIN wave: 1V 6.75MHz/100kHz	−1.0	0.0	1.0	dB
		f2VOUT3	SIN wave: 1V 27MHz/100kHz		−33.0	−24.0	dB
VOUT3 Input dynamic range		DRVOUT3	SIN wave: 100kHz THD=1.0%	1.3	1.4		V
VOUT3 Group delay	with filter	tGD VOUT3	at 100kHz		55		ns
VOUT3 Group delay deviation 1	with filter	⊿t1GD VOUT3	to 3.58MHz		4	20	ns
VOUT3 Group delay deviation 2	with filter	⊿t2GD VOUT3	to 4.43MHz		6	20	ns
VOUT3 Group delay deviation 3	with filter	⊿t3GD VOUT3	to 6MHz		13	20	ns
VOUT3 Crosstalk		CTVOUT3	SIN wave: 1V f=4.43MHz		−60	−55	dB
YOUT3/VOUT4 (67pin) electrical characteristics							
YOUT3 Voltage gain		GvYOUT3	SIN wave: 1V f=100kHz	5.7	6.0	6.3	dB
YOUT3 Frequency characteristic	with filter	f1YOUT3	SIN wave: 1V 6.75MHz/100kHz	−1.0	0.0	1.0	dB
		f2YOUT3	SIN wave: 1V 27MHz/100kHz		−33.0	−24.0	dB
YOUT3 Input dynamic range		DRYOUT3	SIN wave: 100kHz THD=1.0%	1.3	1.4		V
YOUT3 Group delay	with filter	tGD YOUT3	at 100kHz		55		ns
YOUT3 Group delay deviation 1	with filter	⊿t1GD YOUT3	to 3.58MHz		4	20	ns
YOUT3 Group delay deviation 2	with filter	⊿t2GD YOUT3	to 4.43MHz		6	20	ns
YOUT3 Group delay deviation 3	with filter	⊿t3GD YOUT3	to 6MHz		13	20	ns
YOUT3 Crosstalk		CTYOUT3	SIN wave: 1V f=4.43MHz		−60	−55	dB
COUT3/VOUT5 (63pin) electrical characteristics							
COUT3 Voltage gain		GvCOUT3	SIN wave: 1V f=100kHz	5.7	6.0	6.3	dB
COUT3 Frequency characteristic	with filter	f1COUT3	SIN wave: 1V 6.75MHz/100kHz	−1.0	0.0	1.0	dB
		f2COUT3	SIN wave: 1V 27MHz/100kHz		−33.0	−24.0	dB
COUT3 Input dynamic range		DRCOUT3	SIN wave: 100kHz THD=1.0%	1.3	1.4		V
COUT3 Group delay	with filter	tGD COUT3	at 100kHz		55		ns
COUT3 Group delay deviation 1	with filter	⊿t1GD COUT3	to 3.58MHz		4	20	ns
COUT3 Group delay deviation 2	with filter	⊿t2GD COUT3	to 4.43MHz		6	20	ns
COUT3 Group delay deviation 3	with filter	⊿t3GD COUT3	to 6MHz		13	20	ns
COUT3 Crosstalk		CTCOUT3	SIN wave: 1V f=4.43MHz		−60	−55	dB

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
CYOUT1 (75pin) electrical characteristics							
CYOUT1 Voltage gain		GvCYOUT1	SIN wave: 0.7V f=100kHz	–0.3	0.0	0.3	dB
CYOUT1 Frequency characteristic peak		fpeakCYOUT1	SIN wave: 0.7V f=100kHz~100MHz	0.0	0.5	1.0	dB
CYOUT1 Frequency characteristic	without filter	f1CYOUT1	SIN wave: 0.7V 100MHz/100kHz	–4.0	–3.0	–2.0	dB
	with filter1	f11CYOUT1	SIN wave: 0.7V 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		f12CYOUT1	SIN wave: 0.7V 27MHz/100kHz		–33.0	–24.0	dB
	with filter2	f21CYOUT1	SIN wave: 0.7V 13.5MHz/100kHz	–5.0	–3.0	–2.0	dB
		f22CYOUT1	SIN wave: 0.7V 54MHz/100kHz		–33.0	–24.0	dB
	with filter3	f31CYOUT1	SIN wave: 0.7V 24MHz/100kHz	–5.0	–3.0	1.0	dB
		f32CYOUT1	SIN wave: 0.7V 96MHz/100kHz		–33.0	–24.0	dB
CYOUT1 Input dynamic range		DRCYOUT1	SIN wave: 100kHz THD=1.0%	1.6	2.0		V
CYOUT1 Group delay	with filter1	t1GD CYOUT1	at 100kHz		30		ns
	with filter2	t2GD CYOUT1	at 100kHz		25		ns
	with filter3	t3GD CYOUT1	at 100kHz		25		ns
CYOUT1 Group delay deviation 11	with filter1	⊿t11GD CYOUT1	to 3.58MHz		4	20	ns
CYOUT1 Group delay deviation 12		⊿t12GD CYOUT1	to 4.43MHz		6	20	ns
CYOUT1 Group delay deviation 13		⊿t13GD CYOUT1	to 6MHz		12	20	ns
CYOUT1 Group delay deviation 21	with filter2	⊿t21GD CYOUT1	to 3.58MHz		3	20	ns
CYOUT1 Group delay deviation 22		⊿t22GD CYOUT1	to 4.43MHz		5	20	ns
CYOUT1 Group delay deviation 23		⊿t23GD CYOUT1	to 12MHz		8	20	ns
CYOUT1 Group delay deviation 31	with filter3	⊿t31GD CYOUT1	to 3.58MHz		1	20	ns
CYOUT1 Group delay deviation 32		⊿t32GD CYOUT1	to 4.43MHz		1	20	ns
CYOUT1 Group delay deviation 33		⊿t33GD CYOUT1	to 21MHz		5	20	ns
CYOUT1 Crosstalk		CTCYOUT1	SIN wave: 0.7V f=4.43MHz		–60	–55	dB
PbOUT1 (74pin) electrical characteristics							
PbOUT1 Voltage gain		GvPbOUT1	SIN wave: 0.7V f=100kHz	–0.3	0.0	0.3	dB
PbOUT1 Frequency characteristic peak		fpeakPbOUT1	SIN wave: 0.7V f=100kHz~100MHz	0.0	0.5	1.0	dB
PbOUT1 Frequency characteristic	without filter	f1PbOUT1	SIN wave: 0.7V 100MHz/100kHz	–4.0	–3.0	–2.0	dB
	with filter1	f11PbOUT1	SIN wave: 0.7V 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		f12PbOUT1	SIN wave: 0.7V 27MHz/100kHz		–33.0	–24.0	dB
	with filter2	f21PbOUT1	SIN wave: 0.7V 13.5MHz/100kHz	–5.0	–3.0	–2.0	dB
		f22PbOUT1	SIN wave: 0.7V 54MHz/100kHz		–33.0	–24.0	dB
	with filter3	f31PbOUT1	SIN wave: 0.7V 24MHz/100kHz	–5.0	–3.0	1.0	dB
		f32PbOUT1	SIN wave: 0.7V 96MHz/100kHz		–33.0	–24.0	dB
PbOUT1 Input dynamic range		DRPbOUT1	SIN wave: 100kHz THD=1.0%	1.6	2.0		V
PbOUT1 Group delay	with filter1	t1GD PbOUT1	at 100kHz		30		ns
	with filter2	t2GD PbOUT1	at 100kHz		25		ns
	with filter3	t3GD PbOUT1	at 100kHz		25		ns
PbOUT1 Group delay deviation 11	with filter1	⊿t11GD PbOUT1	to 3.58MHz		4	20	ns
PbOUT1 Group delay deviation 12		⊿t12GD PbOUT1	to 4.43MHz		6	20	ns
PbOUT1 Group delay deviation 13		⊿t13GD PbOUT1	to 6MHz		12	20	ns
PbOUT1 Group delay deviation 21	with filter2	⊿t21GD PbOUT1	to 3.58MHz		3	20	ns
PbOUT1 Group delay deviation 22		⊿t22GD PbOUT1	to 4.43MHz		5	20	ns
PbOUT1 Group delay deviation 23		⊿t23GD PbOUT1	to 12MHz		8	20	ns
PbOUT1 Group delay deviation 31	with filter3	⊿t31GD PbOUT1	to 3.58MHz		1	20	ns
PbOUT1 Group delay deviation 32		⊿t32GD PbOUT1	to 4.43MHz		1	20	ns
PbOUT1 Group delay deviation 33		⊿t33GD PbOUT1	to 21MHz		5	20	ns
PbOUT1 Crosstalk		CTPbOUT1	SIN wave: 0.7V f=4.43MHz		–60	–55	dB

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
PROUT1 (73pin) electrical characteristics							
PROUT1 Voltage gain		$G_{VPROUT1}$	SIN wave: 0.7V f=100kHz	–0.3	0.0	0.3	dB
PROUT1 Frequency characteristic peak		$f_{peakPROUT1}$	SIN wave: 0.7V f=100kHz~100MHz	0.0	0.5	1.0	dB
PROUT1 Frequency characteristic	without filter	$f1_{PROUT1}$	SIN wave: 0.7V 100MHz/100kHz	–4.0	–3.0	–2.0	dB
	With filter1	$f11_{PROUT1}$	SIN wave: 0.7V 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		$f12_{PROUT1}$	SIN wave: 0.7V 27MHz/100kHz		–33.0	–24.0	dB
	with filter2	$f21_{PROUT1}$	SIN wave: 0.7V 13.5MHz/100kHz	–5.0	–3.0	–2.0	dB
		$f22_{PROUT1}$	SIN wave: 0.7V 54MHz/100kHz		–33.0	–24.0	dB
	with filter3	$f31_{PROUT1}$	SIN wave: 0.7V 24MHz/100kHz	–5.0	–3.0	1.0	dB
		$f32_{PROUT1}$	SIN wave: 0.7V 96MHz/100kHz		–33.0	–24.0	dB
PROUT1 Input dynamic range		DR_{PROUT1}	SIN wave: 100kHz THD=1.0%	1.6	2.0		V
PROUT1 Crosstalk		CT_{PROUT1}	SIN wave: 0.7V f=4.43MHz		–60	–55	dB
PROUT1 Group delay	with filter1	$t1_{GD\ PROUT1}$	at 100kHz		30		ns
	with filter2	$t2_{GD\ PROUT1}$	at 100kHz		25		ns
	with filter3	$t3_{GD\ PROUT1}$	at 100kHz		25		ns
PROUT1 Group delay deviation 11	with filter1	$\Delta t11_{GD\ PROUT1}$	to 3.58MHz		4	20	ns
PROUT1 Group delay deviation 12		$\Delta t12_{GD\ PROUT1}$	to 4.43MHz		6	20	ns
PROUT1 Group delay deviation 13		$\Delta t13_{GD\ PROUT1}$	to 6MHz		12	20	ns
PROUT1 Group delay deviation 21	with filter2	$\Delta t21_{GD\ PROUT1}$	to 3.58MHz		3	20	ns
PROUT1 Group delay deviation 22		$\Delta t22_{GD\ PROUT1}$	to 4.43MHz		5	20	ns
PROUT1 Group delay deviation 23		$\Delta t23_{GD\ PROUT1}$	to 12MHz		8	20	ns
PROUT1 Group delay deviation 31	with filter3	$\Delta t31_{GD\ PROUT1}$	to 3.58MHz		1	20	ns
PROUT1 Group delay deviation 32		$\Delta t32_{GD\ PROUT1}$	to 4.43MHz		1	20	ns
PROUT1 Group delay deviation 33		$\Delta t33_{GD\ PROUT1}$	to 21MHz		5	20	ns
Group delay deviation between each channels							
Group delay deviation between C and Y		$\Delta t1_{chGD}$	between C and Y at 3.58MHz		0	10	ns
Group delay deviation between CY and Pb (Pr)		$\Delta t2_{chGD}$	between CY and Pb (Pr) at 8MHz		0	10	ns

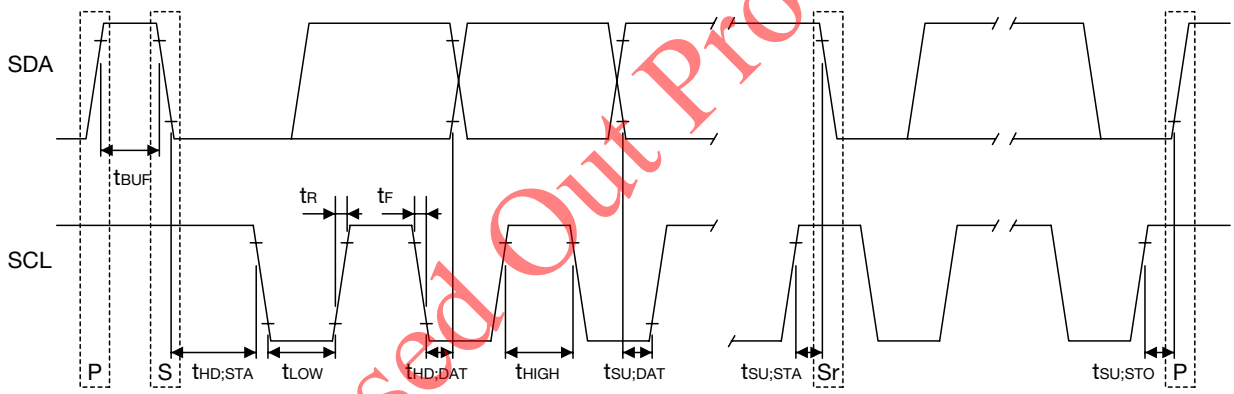
Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
CYOUT2 (71pin) electrical characteristics							
CYOUT2 Voltage gain		GvCYOUT2	SIN wave: 0.7V f=100kHz	–0.3	0.0	0.3	dB
CYOUT2 Frequency characteristic peak		fpeakCYOUT2	SIN wave: 0.7V f=100kHz~50MHz	0.0	0.5	1.0	dB
CYOUT2 Frequency characteristic	without filter	f1CYOUT2	SIN wave: 0.7V 50MHz/100kHz	–3.0	–1.0	0.0	dB
	with filter1	f11CYOUT2	SIN wave: 0.7V 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		f12CYOUT2	SIN wave: 0.7V 27MHz/100kHz		–33.0	–24.0	dB
	with filter2	f21CYOUT2	SIN wave: 0.7V 13.5MHz/100kHz	–5.0	–3.0	–2.0	dB
		f22CYOUT2	SIN wave: 0.7V 54MHz/100kHz		–33.0	–24.0	dB
	with filter3	f31CYOUT2	SIN wave: 0.7V 24MHz/100kHz	–5.0	–3.0	1.0	dB
		f32CYOUT2	SIN wave: 0.7V 96MHz/100kHz		–33.0	–24.0	dB
CYOUT2 Input dynamic range		DRCYOUT2	SIN wave: 100kHz THD=1.0%	1.6	2.0		V
CYOUT2 Group delay	with filter1	t1GD CYOUT2	at 100kHz		30		ns
	With filter2	t2GD CYOUT2	at 100kHz		25		ns
	With filter3	t3GD CYOUT2	at 100kHz		25		ns
CYOUT2 Group delay deviation 11	with filter1	⊿t11GD CYOUT2	to 3.58MHz		4	20	ns
CYOUT2 Group delay deviation 12		⊿t12GD CYOUT2	to 4.43MHz		6	20	ns
CYOUT2 Group delay deviation 13		⊿t13GD CYOUT2	to 6MHz		12	20	ns
CYOUT2 Group delay deviation 21	with filter2	⊿t21GD CYOUT2	to 3.58MHz		3	20	ns
CYOUT2 Group delay deviation 22		⊿t22GD CYOUT2	to 4.43MHz		5	20	ns
CYOUT2 Group delay deviation 23		⊿t23GD CYOUT2	to 12MHz		8	20	ns
CYOUT2 Group delay deviation 31	with filter3	⊿t31GD CYOUT2	to 3.58MHz		1	20	ns
CYOUT2 Group delay deviation 32		⊿t32GD CYOUT2	to 4.43MHz		1	20	ns
CYOUT2 Group delay deviation 33		⊿t33GD CYOUT2	to 21MHz		5	20	ns
CYOUT2 Crosstalk		CTCYOUT2	SIN wave: 0.7V f=4.43MHz		–60	–55	dB
PbOUT2 (70pin) electrical characteristics							
PbOUT2 Voltage gain		GvPbOUT2	SIN wave: 0.7V f=100kHz	–0.3	0.0	0.3	dB
PbOUT2 Frequency characteristic peak		fpeakPbOUT2	SIN wave: 0.7V f=100kHz~50MHz	0.0	0.5	1.0	dB
PbOUT2 Frequency characteristic	without filter	f1PbOUT2	SIN wave: 0.7V 50MHz/100kHz	–3.0	–1.0	0.0	dB
	With filter1	f11PbOUT2	SIN wave: 0.7V 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		f12PbOUT2	SIN wave: 0.7V 27MHz/100kHz		–33.0	–24.0	dB
	with filter2	f21PbOUT2	SIN wave: 0.7V 13.5MHz/100kHz	–5.0	–3.0	–2.0	dB
		f22PbOUT2	SIN wave: 0.7V 54MHz/100kHz		–33.0	–24.0	dB
	with filter3	f31PbOUT2	SIN wave: 0.7V 24MHz/100kHz	–5.0	–3.0	1.0	dB
		f32PbOUT2	SIN wave: 0.7V 96MHz/100kHz		–33.0	–24.0	dB
PbOUT2 Input dynamic range		DRPbOUT2	SIN wave: 100kHz THD=1.0%	1.6	2.0		V
PbOUT2 Group delay	with filter1	t1GD PbOUT2	at 100kHz		30		ns
	with filter2	t2GD PbOUT2	at 100kHz		25		ns
	with filter3	t3GD PbOUT2	at 100kHz		25		ns
PbOUT2 Group delay deviation 11	with filter1	⊿t11GD PbOUT2	to 3.58MHz		4	20	ns
PbOUT2 Group delay deviation 12		⊿t12GD PbOUT2	to 4.43MHz		6	20	ns
PbOUT2 Group delay deviation 13		⊿t13GD PbOUT2	to 6MHz		12	20	ns
PbOUT2 Group delay deviation 21	with filter2	⊿t21GD PbOUT2	to 3.58MHz		3	20	ns
PbOUT2 Group delay deviation 22		⊿t22GD PbOUT2	to 4.43MHz		5	20	ns
PbOUT2 Group delay deviation 23		⊿t23GD PbOUT2	to 12MHz		8	20	ns
PbOUT2 Group delay deviation 31	with filter3	⊿t31GD PbOUT2	to 3.58MHz		1	20	ns
PbOUT2 Group delay deviation 32		⊿t32GD PbOUT2	to 4.43MHz		1	20	ns
PbOUT2 Group delay deviation 33		⊿t33GD PbOUT2	to 21MHz		5	20	ns
PbOUT2 Crosstalk		CTPbOUT2	SIN wave: 0.7V f=4.43MHz		–60	–55	dB

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
PROUT2 (69pin) electrical characteristics							
PROUT2 Voltage gain		GvPROUT2	SIN wave: 0.7V f=100kHz	–0.3	0.0	0.3	dB
PROUT2 Frequency characteristicJ peak		fpeakPROUT2	SIN wave: 0.7V f=100kHz~50MHz	0.0	0.5	1.0	dB
PROUT2 Frequency characteristic	without filter	f1PROUT2	SIN wave: 0.7V 50MHz/100kHz	–3.0	–1.0	0.0	dB
	With filter1	f11PROUT2	SIN wave: 0.7V 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		f12PROUT2	SIN wave: 0.7V 27MHz/100kHz		–33.0	–24.0	dB
	with filter2	f21PROUT2	SIN wave: 0.7V 13.5MHz/100kHz	–5.0	–3.0	–2.0	dB
		f22PROUT2	SIN wave: 0.7V 54MHz/100kHz		–33.0	–24.0	dB
	with filter3	f31PROUT2	SIN wave: 0.7V 24MHz/100kHz	–5.0	–3.0	1.0	dB
		f32PROUT2	SIN wave: 0.7V 96MHz/100kHz		–33.0	–24.0	dB
PROUT2 Input dynamic range		DRPROUT2	SIN wave: 100kHz THD=1.0%	1.6	2.0		V
PROUT2 Crosstalk		CTPROUT2	SIN wave: 0.7V f=4.43MHz		–60	–55	dB
PROUT2 Group delay	with filter1	t1GD PROUT2	at 100kHz		30		ns
	with filter2	t2GD PROUT2	at 100kHz		25		ns
	with filter3	t3GD PROUT2	at 100kHz		25		ns
PROUT2 Group delay deviation 11	with filter1	⊿t11GD PROUT2	to 3.58MHz		4	20	ns
PROUT2 Group delay deviation 12		⊿t12GD PROUT2	to 4.43MHz		6	20	ns
PROUT2 Group delay deviation 13		⊿t13GD PROUT2	to 6MHz		12	20	ns
PROUT2 Group delay deviation 21	with filter2	⊿t21GD PROUT2	to 3.58MHz		3	20	ns
PROUT2 Group delay deviation 22		⊿t22GD PROUT2	to 4.43MHz		5	20	ns
PROUT2 Group delay deviation 23		⊿t23GD PROUT2	to 12MHz		8	20	ns
PROUT2 Group delay deviation 31	with filter3	⊿t31GD PROUT2	to 3.58MHz		1	20	ns
PROUT2 Group delay deviation 32		⊿t32GD PROUT2	to 4.43MHz		1	20	ns
PROUT2 Group delay deviation 33		⊿t33GD PROUT2	to 21MHz		5	20	ns
Group delay deviation between each channels							
Group delay deviation between C and Y		⊿t1chGD	between C and Y at 3.58MHz		0	10	ns
Group delay deviation between CY and Pb (Pr)		⊿t2chGD	between CY and Pb (Pr) at 8MHz		0	10	ns
L, ROUT (34~39pin) electrical characteristics							
L, ROUT Voltage gain	0dB	Gv1L, ROUT	SIN wave: 1Vrms f=1kHz	–0.3	0.0	0.3	dB
	6dB	Gv2L, ROUT	SIN wave: 1Vrms f=1kHz	5.7	6.0	6.3	dB
L, ROUT Frequency characteristic	0dB	f1L, ROUT	SIN wave: 1Vrms f=50kHz	–3.0			dB
	6dB	f2L, ROUT	SIN wave: 1Vrms f=50kHz	–3.0			dB
Total harmonic distortion		THD	SIN wave: 1Vrms f=1kHz, Gv=0dB		0.03	0.05	%
Input dynamic range		DR	f=1kHz, THD=0.5% Gv=0dB	2.8	3.0		Vrms
Crosstalk		CT	SIN wave: 1Vrms f=1kHz		–90	–80	dB
Ripple rejection		PSRR	VCC=9V+0.1Vrms (SIN wave)at 100Hz		–50	–40	dB
Output offset voltage		VOFF1	DC offset at the switching time, Gv=0dB	–15	0	15	mV
		VOFF2	DC offset at the switching time, Gv=6dB	–30	0	30	
S/N ratio		S/N1	1kHz, A curve, 1Vrms Gv=0dB		–90	–80	dB
		S/N2	1kHz, A curve, 1Vrms Gv=6dB		–80	–70	dB
O1 (5pin) electrical characteristics							
O1 pin low level output voltage		VO1	O1 pin sink 5mA	GND		0.4	V
O1 pin Leak current (at the time of OFF)		IO1		–10		10	µA
O2 (17pin) electrical characteristics							
O2 pin low level output voltage		VO2	O2 pin sink 5mA	GND		0.4	V
O2 pin Leak current (at the time of OFF)		IO2		–10		10	µA

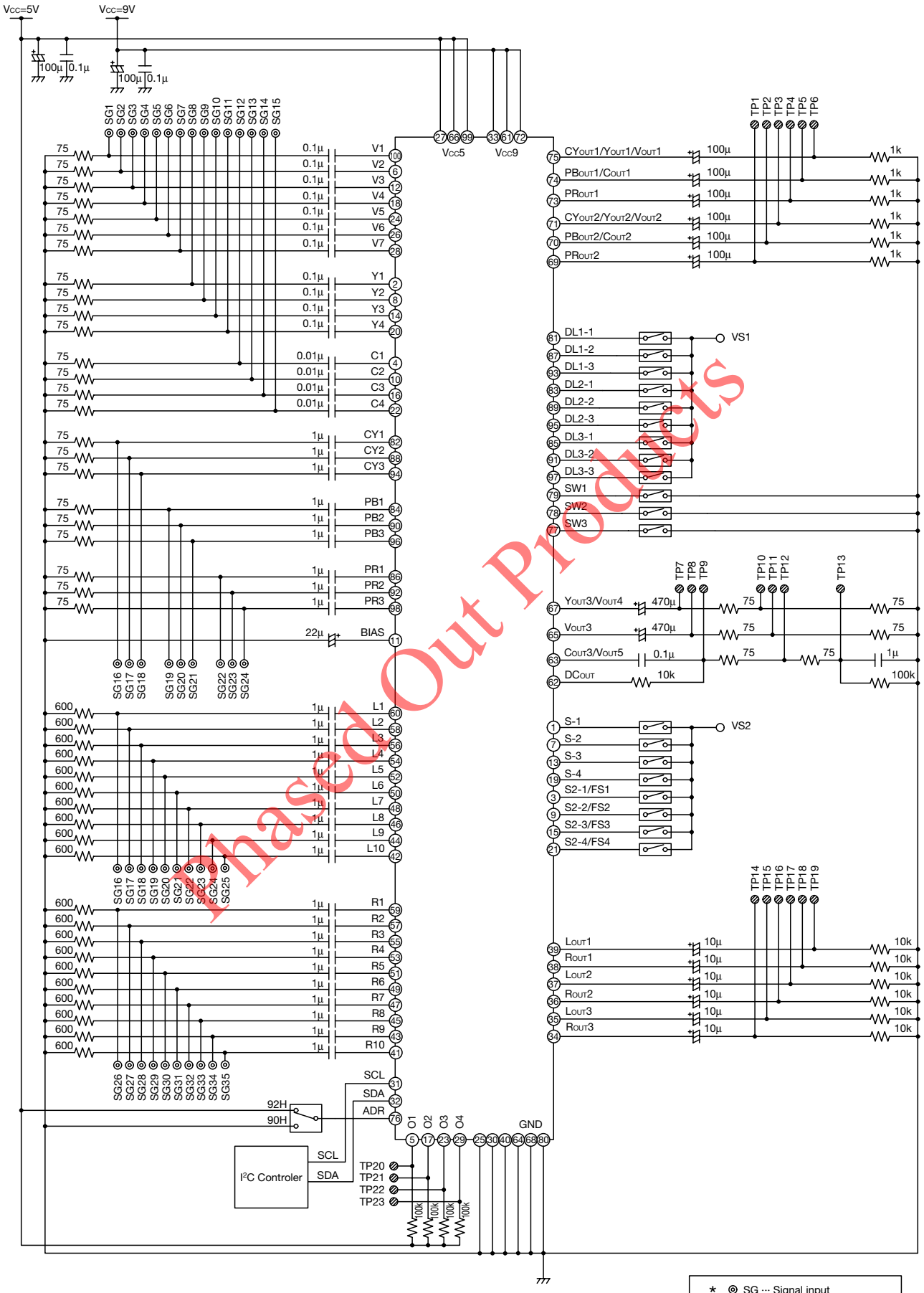
Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
O3 (23pin) electrical characteristics							
O3 pin low level output voltage		V_{O3}	O3 pin sink 5mA	GND		0.4	V
O3 pin Leak current (at the time of OFF)		I_{O3}		−10		10	µA
O4 (29pin) electrical characteristics							
O4 pin low level output voltage		V_{O4}	O4 pin sink 5mA	GND		0.4	V
O4 pin Leak current (at the time of OFF)		I_{O4}		−10		10	µA
DL1 (81, 87, 93pin) electrical characteristics							
DL1 Input voltage 1	Low	$V1_{L\ DL1}$		GND		1.0	V
	Middle	$V1_{M\ DL1}$		1.3		2.7	V
	High	$V1_{H\ DL1}$		3.5		$V_{CC}5$	V
DL2 (83, 89, 95pin) electrical characteristics							
DL2 Input voltage	Low	$V_{L\ DL2}$		GND		2.7	V
	High	$V_{H\ DL2}$		3.5		$V_{CC}5$	V
DL3 (85, 91, 97pin) electrical characteristics							
DL3 Input voltage	Low	$V_{L\ DL3}$		GND		1.0	V
	Middle	$V_{M\ DL3}$		1.3		2.7	V
	High	$V_{H\ DL3}$		3.5		$V_{CC}5$	V
SW (79, 78, 77pin) electrical characteristics							
SW Input voltage	Low	$V_{L\ SW}$		GND		2.0	V
	High	$V_{H\ SW}$		3.0		$V_{CC}5$	V
SW output current at terminal voltage Low		I_{SW}		19	27	35	µA
S2/FS (3, 9, 15, 21pin) electrical characteristics							
S2/FS Input voltage 1	Low	$V1_{L\ S2/FS}$	S, D-Detect Mode	GND		1.0	V
	Middle	$V1_{M\ S2/FS}$		1.3		2.7	V
	High	$V1_{H\ S2/FS}$		3.5		$V_{CC}5$	V
S2/FS Input voltage 2	Low	$V2_{L\ S2/FS}$	FS-Detect Mode	GND		1.0	V
	Middle	$V2_{M\ S2/FS}$		1.5		3.0	V
	High	$V2_{H\ S2/FS}$		3.5		$V_{CC}5$	V
S (1, 7, 13, 19pin) electrical characteristics							
S Input voltage	Low	$V_{L\ S1}$		GND		2.0	V
	High	$V_{H\ S1}$		3.0		$V_{CC}5$	V
S output current at terminal voltage Low		I_{S1}		19	27	35	µA
ADR (76pin) electrical characteristics							
ADR Input voltage	Low	$V_{L\ ADR}$	90H select	GND		0.8	V
	High	$V_{H\ ADR}$	92H select	2.5		$V_{CC}5$	V
ADR input current at terminal voltage High		I_{ADR}		50	70	90	µA

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I²C condition						
Input voltage L	V_{IL}		GND		0.8	V
Input voltage H	V_{IH}		2.2		$V_{CC}5$	V
SDA low level output voltage	V_{OL}	SDA sink 3mA	GND		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	−10		10	µA
Low level input current	I_{IL}	SDA, SCL=0.4V	−10		10	µA
Clock frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			µs
SCL start hold time	$t_{HD;STA}$		4.0			µs
SCL low level hold time	t_{LOW}		4.7			µs
SCL high level hold time	t_{HIGH}		4.0			µs
Start condition setup time	$t_{SU;STA}$		4.7			µs
SDA data hold time	$t_{HD;DAT}$		0			µs
SDA data setup time	$t_{SU;DAT}$		250			ns
SDA, SCL rise time	t_R				1000	ns
SDA, SCL fall time	t_F				300	ns
Stop condition setup time	$t_{SU;STO}$		4.0			µs

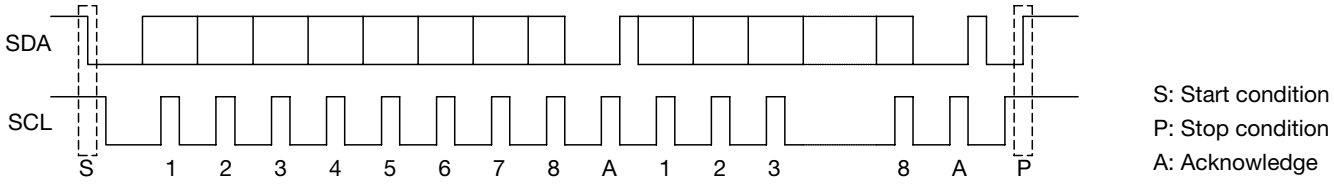
Note: I²C condition



Measuring Circuit



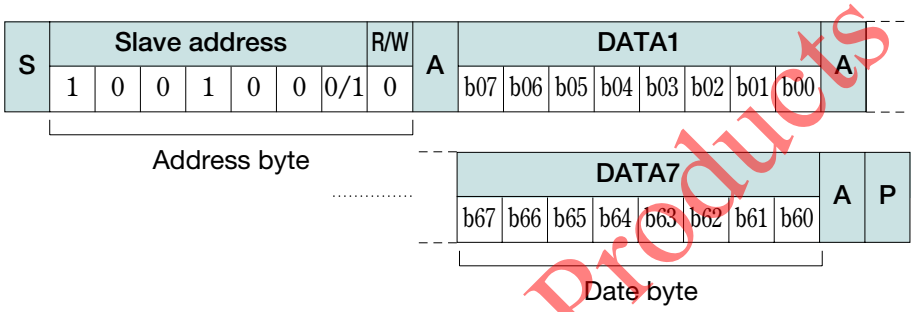
I²C BUS



I²C BUS is inter IC bus system controled by 2 lines (SDA, SCL). Data is transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start conditions.

[Control registers]

Control register is data sent from the master for determining the switch conditions. The data format is set as shown in the following figure.



Out of the Address byte, first 7bits are assigned to the slave address, while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 0 when data is used control register. As MM1783 slave address, either 90H or 92H can be selected according to the ADR terminal conditions. When ADR terminal is L, 90H is selected.
The following figure indicates the control contents of control registers and switches. Each bit of control registers is reset to 0, when the device is turned on.

MM1783 consists of one address byte and 7 control data bytes (8bytes in total). All data over the limited length (9th and subsequent bytes) is fully neglected. For details of the control contents of switches, refer to the another table.

The reset circuit in the MM1783 is configured with a 5V power supply.
The threshold voltage to operate the reset function is 2.5V±0.5V.

Even if a 9V power supply and 5V power supply are independently blacked out as a power sequence, I²C control is properly performed after power is recovered.

Table of control registers

No.	DATA condition							
DATA1 [00H]	b07	b06	b05	b04	b03	b02	b01	b00
	OUT1 LPF select		OUT1 power save		OUT1 line select			
DATA2 [00H]	b17	b16	b15	b14	b13	b12	b11	b10
	OUT2 LPF select		OUT2 power save		OUT2 line select			
DATA3 [00H]	b27	b26	b25	b24	b23	b22	b21	b20
	DC_{OUT} voltage		OUT3-5 power save	OUT3 separate	OUT3 line select			
DATA4 [00H]	b37	b36	b35	b34	b33	b32	b31	b30
	Audio OUT1 line select				Audio OUT2 line select			
DATA5 [00H]	b47	b46	b45	b44	b43	b42	b41	b40
		AO1 GAIN SW	AO2 GAIN SW	AO3 GAIN SW	Audio OUT3 line select			
DATA6 [00H]	b57	b56	b55	b54	b53	b52	b51	b50
	OUT1 graphics resolution	AO1 power save	AO2 power save	AO3 power save	O1	O2	O3	O4
DATA7 [00H]	b67	b66	b65	b64	b63	b62	b61	b60
	OUT4 line select				OUT5 line select			

*: [00H] is in the initial state of control registers.

Details of contents of control-1

OUT1 line select

b03	b02	b01	b00	CYOUT1 (75pin)	PbOUT1 (74pin)	ProUT1 (73pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	V1	Mute	Mute
0	0	1	0	V2	Mute	Mute
0	0	1	1	V3	Mute	Mute
0	1	0	0	V4	Mute	Mute
0	1	0	1	V5	Mute	Mute
0	1	1	0	V6	Mute	Mute
0	1	1	1	V7	Mute	Mute
1	0	0	0	Y1	C1	Mute
1	0	0	1	Y2	C2	Mute
1	0	1	0	Y3	C3	Mute
1	0	1	1	Y4	C4	Mute
1	1	0	0	CY1	PB1	PR1
1	1	0	1	CY2	PB2	PR2
1	1	1	0	CY3	PB3	PR3
1	1	1	1	Mute	Mute	Mute

OUT2 line select

b13	b12	b11	b10	CYOUT2 (71pin)	PbOUT2 (70pin)	ProUT2 (69pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	V1	Mute	Mute
0	0	1	0	V2	Mute	Mute
0	0	1	1	V3	Mute	Mute
0	1	0	0	V4	Mute	Mute
0	1	0	1	V5	Mute	Mute
0	1	1	0	V6	Mute	Mute
0	1	1	1	V7	Mute	Mute
1	0	0	0	Y1	C1	Mute
1	0	0	1	Y2	C2	Mute
1	0	1	0	Y3	C3	Mute
1	0	1	1	Y4	C4	Mute
1	1	0	0	CY1	PB1	PR1
1	1	0	1	CY2	PB2	PR2
1	1	1	0	CY3	PB3	PR3
1	1	1	1	Mute	Mute	Mute

Details of contents of control-2

OUT3 line select (OUT3 Separator SW OFF [b24=0]) *1

b24	b23	b22	b21	b20	VOUT3 (65pin)	YOUT3 (67pin)	COUT3 (63pin)
0	0	0	0	0	Mute	Mute	Mute
0	0	0	0	1	Y1+C1	Y1	C1
0	0	0	1	0	Y2+C2	Y2	C2
0	0	0	1	1	Y3+C3	Y3	C3
0	0	1	0	0	Y4+C4	Y4	C4
0	0	1	0	1	Mute	Mute	Mute
0	0	1	1	0	Mute	Mute	Mute
0	0	1	1	1	Mute	Mute	Mute
0	1	0	0	0	Mute	Mute	Mute
0	1	0	0	1	V1	Mute	Mute
0	1	0	1	0	V2	Mute	Mute
0	1	0	1	1	V3	Mute	Mute
0	1	1	0	0	V4	Mute	Mute
0	1	1	0	1	V5	Mute	Mute
0	1	1	1	0	V6	Mute	Mute
0	1	1	1	1	V7	Mute	Mute

OUT4 line select (OUT3 Separator SW ON [b24=1]) *1

b24	b67	b66	b65	b64	VOUT3 (65pin)	YOUT3 (67pin)	COUT3 (63pin)
1	0	0	0	0	Regardless of b24, It is controlled by the b23-b20. Refer to the upper table.	Mute	It is controlled by the b63-b60 at the time of b24=1. Refer to following table.
1	0	0	0	1		Y1+C1	
1	0	0	1	0		Y2+C2	
1	0	0	1	1		Y3+C3	
1	0	1	0	0		Y4+C4	
1	0	1	0	1		Mute	
1	0	1	1	0		Mute	
1	0	1	1	1		Mute	
1	1	0	0	0		Mute	
1	1	0	0	1		V1	
1	1	0	1	0		V2	
1	1	0	1	1		V3	
1	1	1	0	0		V4	
1	1	1	0	1		V5	
1	1	1	1	0		V6	
1	1	1	1	1		V7	

OUT5 line select (OUT3 Separator SW ON [b24=1]) *1

b24	b63	b62	b61	b60	VOUT3 (65pin)	YOUT3 (67pin)	COUT3 (63pin)
1	0	0	0	0	Regardless of b24, It is controlled by the b23-b20. Refer to the upper table.	It is controlled by the b67-b64 at the time of b24=1. Refer to the upper table.	Mute
1	0	0	0	1			Y1+C1
1	0	0	1	0			Y2+C2
1	0	0	1	1			Y3+C3
1	0	1	0	0			Y4+C4
1	0	1	0	1			Mute
1	0	1	1	0			Mute
1	0	1	1	1			Mute
1	1	0	0	0			Mute
1	1	0	0	1			V1
1	1	0	1	0			V2
1	1	0	1	1			V3
1	1	1	0	0			V4
1	1	1	0	1			V5
1	1	1	1	0			V6
1	1	1	1	1			V7

*1: When DCOUT is set to Hi-Impedance mode, OUT3 is automatically set to Mute mode.

Details of contents of control-3

LPF cutoff frequency select

OUT1 (73, 74, 75pin)

b07	b06	LPF fc
0	0	through
0	1	24.0MHz
1	0	13.5MHz
1	1	6.75MHz

OUT2 (69, 70, 71pin)

b17	b16	LPF fc
0	0	through
0	1	24.0MHz
1	0	13.5MHz
1	1	6.75MHz

Powersave

OUT1 (73, 74, 75pin)

b05	Conditions
0	Active
1	Powersave

OUT2 (69, 70, 71pin)

b15	Conditions
0	Active
1	Powersave

OUT3 (63, 65, 67pin)

b25	Conditions
0	Active
1	Powersave

Output PORT control

O1 (5pin)

b53	Conditions
0	Low
1	Open

O2 (17pin)

b52	Conditions
0	Low
1	Open

O3 (23pin)

b51	Conditions
0	Low
1	Open

O4 (29pin)

b50	Conditions
0	Low
1	Open

DCOUT (62pin) output voltage

b27	b26	Voltage
0	0	0V
0	1	2.2V
1	0	5V
1	1	Hi-Impedance *

*: When DCOUT is set to Hi-Impedance mode, OUT3 is automatically set to Mute mode.

Graphics resolution

OUT1 (73, 74, 75pin)

b57	Conditions
0	D5
1	D4

Details of contents of control-4

Audio OUT1 line select

b37	b36	b35	b34	LOUT1 (39pin)	ROUT1 (38pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	L9	R9
1	0	1	0	L10	R10
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Audio OUT2 line select

b33	b32	b31	b30	LOUT12 (37pin)	ROUT12 (36pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	L9	R9
1	0	1	0	L10	R10
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Audio OUT3 line select

b43	b42	b41	b40	LOUT3 (35pin)	ROUT3 (34pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	L9	R9
1	0	1	0	L10	R10
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Details of contents of control-5

Audio GAIN SW

OUT1 (38, 39pin)

b46	GAIN
0	0dB
1	6dB

OUT2 (36, 37pin)

b45	GAIN
0	0dB
1	6dB

OUT3 (34, 35pin)

b44	GAIN
0	0dB
1	6dB

Audio Powersave

OUT1 (38, 39pin)

b56	Conditions
0	Active
1	Powersave

OUT2 (36, 37pin)

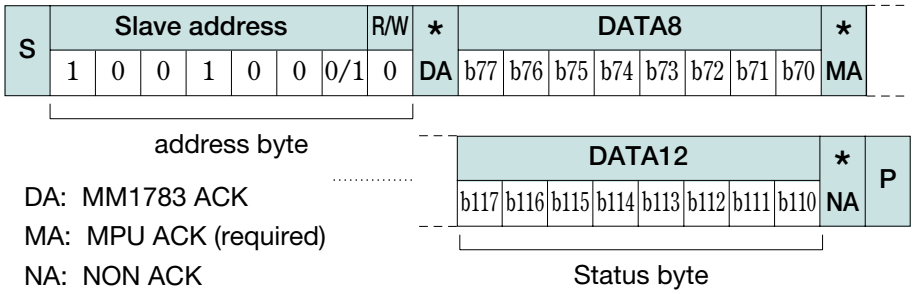
b55	Conditions
0	Active
1	Powersave

OUT3 (34, 35pin)

b54	Conditions
0	Active
1	Powersave

[Status register]

Status register is data to inform the master of the device status. The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 1 when data are used status registers. As MM1783 slave address, either 91H or 93H can be selected according to the ADR terminal conditions. When ADR terminal is L, 91H is selected. Set the confirmation acknowledgement after the end of status register to non-ACK. The following figure shows the correspondence of the output data of status register.

Table of status registers

No.	DATA condition							
DATA8	b77	b76	b75	b74	b73	b72	b71	b70
			SW1 detect	DL1-1 detect		DL2-1 detect	DL3-1 detect	
DATA9	b87	b86	b85	b84	b83	b82	b81	b80
			SW2 detect	DL1-2 detect		DL2-2 detect	DL3-2 detect	
DATA10	b97	b96	b95	b94	b93	b92	b91	b90
			SW3 detect	DL1-3 detect		DL2-3 detect	DL3-3 detect	
DATA11	b107	b106	b105	b104	b103	b102	b101	b100
			S-1 detect	S2-1/FS1 detect		S-2 detect	S2-2/FS2 detect	
DATA12	b117	b116	b115	b114	b113	b112	b111	b110
			S-3 detect	S2-3/FS3 detect		S-4 detect	S2-4/FS4 detect	

Output data of status register & threshold

It is based on CPR1202 which is the specification of JEITA.

(Except where noted otherwise Ta=25°C, Vcc9=9V, Vcc5=5V)

S1~S4 (1, 7, 13, 19pin) detect

S1~S4 voltage	Conditions	S4	S3	S2	S1
		b112	b115	b102	b105
GND ≦ VDC ≦ 2.0V	Connected	1	1	1	1
3.0V ≦ VDC ≦ Vcc5	Unconnected	0	0	0	0

S2-1~S2-4 (3, 9, 15, 21pin) detect (Aspect)

S2-1~S2-4 voltage	Aspect	S2-4		S2-3		S2-2		S2-11	
		b111	b110	b114	b113	b101	b100	b104	b103
GND ≦ VDC ≦ 1.0V	4 : 3	0	0	0	0	0	0	0	0
1.3V ≦ VDC ≦ 2.7V	Letterbox	0	1	0	1	0	1	0	1
3.5V ≦ VDC ≦ Vcc5	16 : 9	1	0	1	0	1	0	1	0

DL1-1, DL1-2, DL1-3 (81, 87, 93pin) detect (Scanning line)

DL1-1~DL1-3 voltage	Scanning line	DL1-3		DL1-2		DL1-1	
		b94	b93	b84	b83	b74	b73
GND ≦ VDC ≦ 1.0V	480	0	0	0	0	0	0
1.3V ≦ VDC ≦ 2.7V	720	0	1	0	1	0	1
3.5V ≦ VDC ≦ Vcc5	1080	1	0	1	0	1	0

DL2-1, DL2-2, DL2-3 (83, 89, 95pin) detect (I/P)

DL2-1~DL2-3 voltage	I/P	DL2-3	DL2-2	DL2-1
		b92	b82	b72
GND ≦ VDC ≦ 2.7V	Interlace	0	0	0
3.5V ≦ VDC ≦ Vcc5	Progressive	1	1	1

DL3-1, DL3-2, DL3-3 (85, 91, 97pin) detect (Aspect)

DL3-1~DL3-3 voltage	Aspect	DL3-3		DL3-2		DL3-1	
		b91	b90	b81	b80	b71	b70
GND ≦ VDC ≦ 1.0V	4 : 3	0	0	0	0	0	0
1.3V ≦ VDC ≦ 2.7V	Letterbox	0	1	0	1	0	1
3.5V ≦ VDC ≦ Vcc5	16 : 9	1	0	1	0	1	0

SW1~SW3 (79, 78, 77pin) detect

SW1~SW3 voltage	Conditions	SW3	SW2	SW1
		b95	b85	b75
GND ≦ VDC ≦ 2.0V	Connected	1	1	1
3.0V ≦ VDC ≦ Vcc5	Unconnected	0	0	0

It is based on EN50049-1 which is the specification of CENELEC. Please drop the voltage of FS terminal on resistance division(47kΩ&33kΩ), and input it.
(Except where noted otherwise Ta=25°C, Vcc9=9V, Vcc5=5V)

FS1~FS4 (3, 9, 15, 21pin) detect (Scanning Line)

FS1~FS3 voltage	Level	FS4		FS3		FS2		FS1	
		b111	b110	b114	b113	b101	b100	b104	b103
GND ≦ VDC ≦ 1.0V	0	0	0	0	0	0	0	0	0
1.5V ≦ VDC ≦ 3.0V	1A	0	1	0	1	0	1	0	1
3.5V ≦ VDC ≦ Vcc5	1B	1	0	1	0	1	0	1	0

*: Level 0 ···television broadcast reproduction
Level 1A ···repreduction of an external source with aspect ratio 16 : 9
Level 1B ···peritelevision reproduction

S1~S4 (1, 7, 13, 19pin) detect

S1~S4 voltage	Conditions	S4	S3	S2	S1
		b112	b115	b102	b105
GND ≦ VDC ≦ 2.0V	Connected	1	1	1	1
3.0V ≦ VDC ≦ Vcc5	Unconnected	0	0	0	0

S2-1~S2-4 (3, 9, 15, 21pin) detect (Aspect)

S2-1~S2-4 voltage	Aspect	S2-4 ↓ FS4	S2-3 ↓ FS3	S2-2 ↓ FS2	S2-1 ↓ FS1
GND ≦ VDC ≦ 1.0V	4 : 3				
1.3V ≦ VDC ≦ 2.7V	Letterbox				
3.5V ≦ VDC ≦ Vcc5	16 : 9				

DL1-1, DL1-2, DL1-3 (81, 87, 93pin) detect (Scanning Line)

DL1-1~DL1-3 voltage	Scanning line	DL1-3		DL1-2		DL1-1	
		b94	b93	b84	b83	b74	b73
GND ≦ VDC ≦ 1.0V	480	0	0	0	0	0	0
1.3V ≦ VDC ≦ 2.7V	720	0	1	0	1	0	1
3.5V ≦ VDC ≦ Vcc5	1080	1	0	1	0	1	0

DL2-1, DL2-2, DL2-3 (83, 89, 95pin) detect (I/P)

DL2-1~DL2-3 voltage	I/P	DL2-3	DL2-2	DL2-1
		b92	b82	b72
GND ≦ VDC ≦ 2.7V	Interlace	0	0	0
3.5V ≦ VDC ≦ Vcc5	Progressive	1	1	1

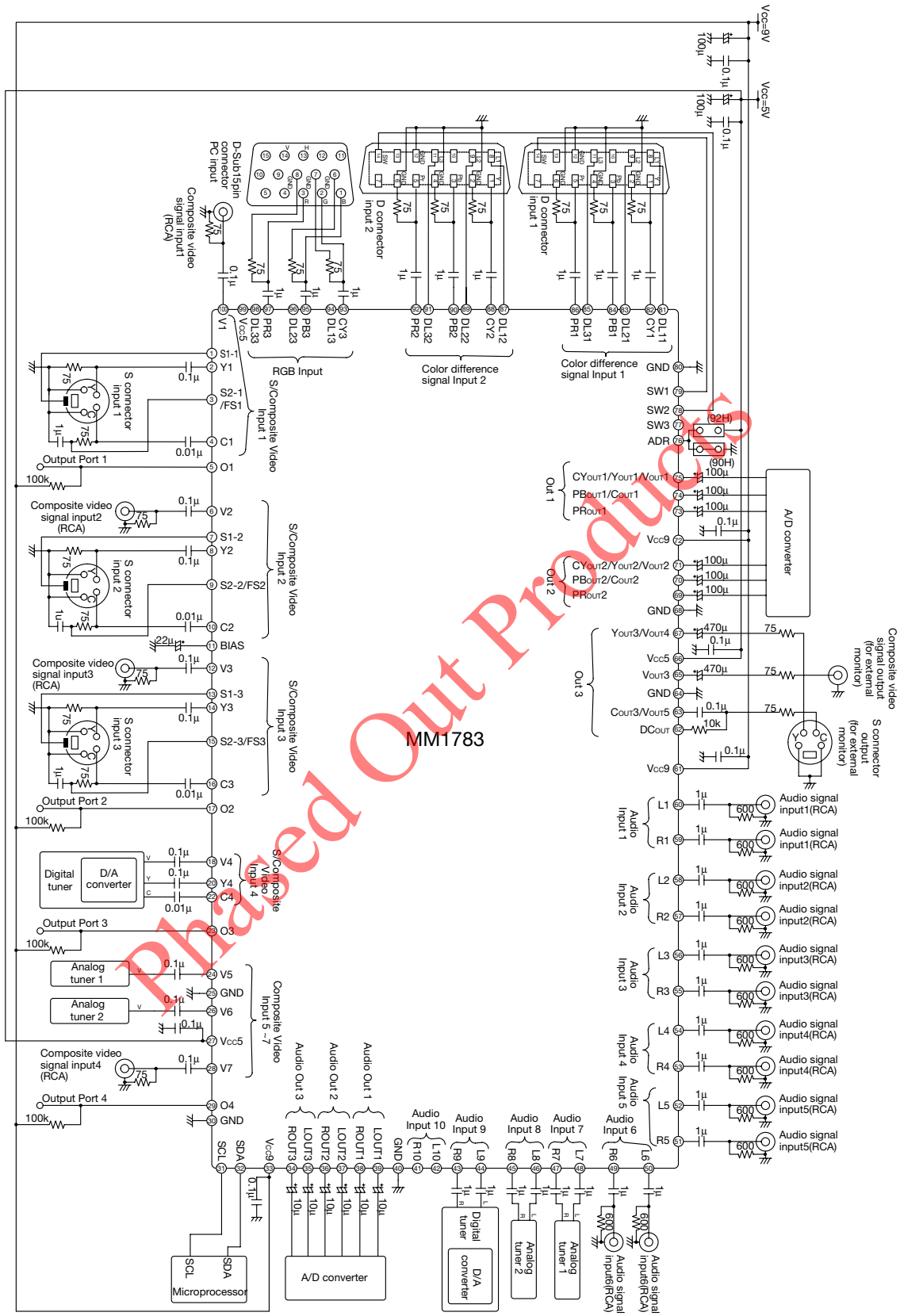
DL3-1, DL3-2, DL3-3 (85, 91, 97pin) detect (Aspect)

DL3-1~DL3-3 voltage	Aspect	DL3-3		DL3-2		DL3-1	
		b91	b90	b81	b80	b71	b70
GND ≦ VDC ≦ 1.0V	4 : 3	0	0	0	0	0	0
1.3V ≦ VDC ≦ 2.7V	Letterbox	0	1	0	1	0	1
3.5V ≦ VDC ≦ Vcc5	16 : 9	1	0	1	0	1	0

SW1~SW3 (79, 78, 77pin) detect

SW1~SW3 voltage	Conditions	SW3	SW2	SW1
		b95	b85	b75
GND ≦ VDC ≦ 2.0V	Connected	1	1	1
3.0V ≦ VDC ≦ Vcc5	Unconnected	0	0	0

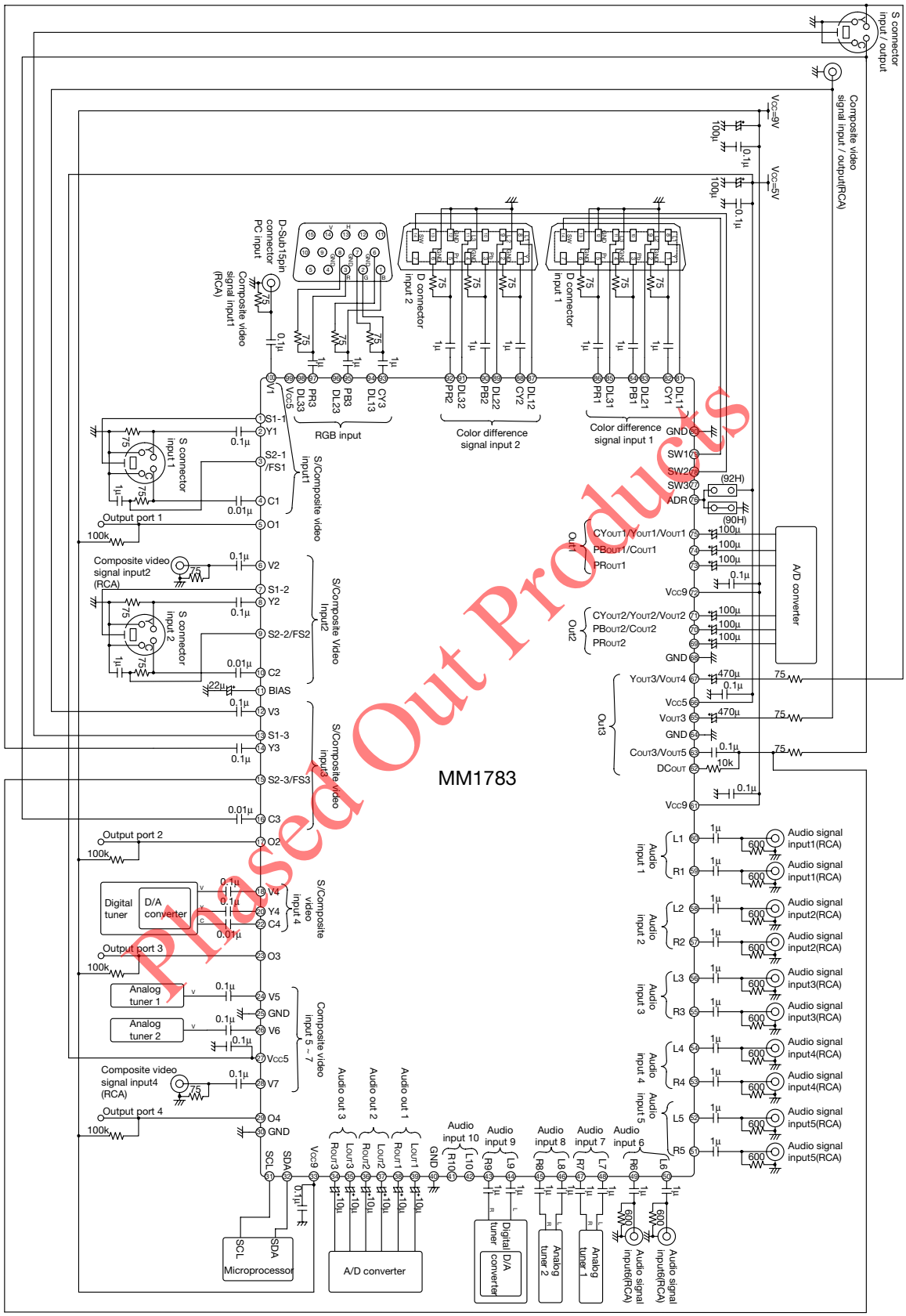
Application Circuit 1



Note: Be careful because a DC voltage changes when you short an adjoining terminal by the resistance.

- We shall not be liable for any trouble or damage caused by using this circuit.
- In the event a problem which may affect industrial property or any other rights of us or a third party happens during the use of information in these circuit, we shall not be liable for any problem, nor grant a license therefore.

Application Circuit 2



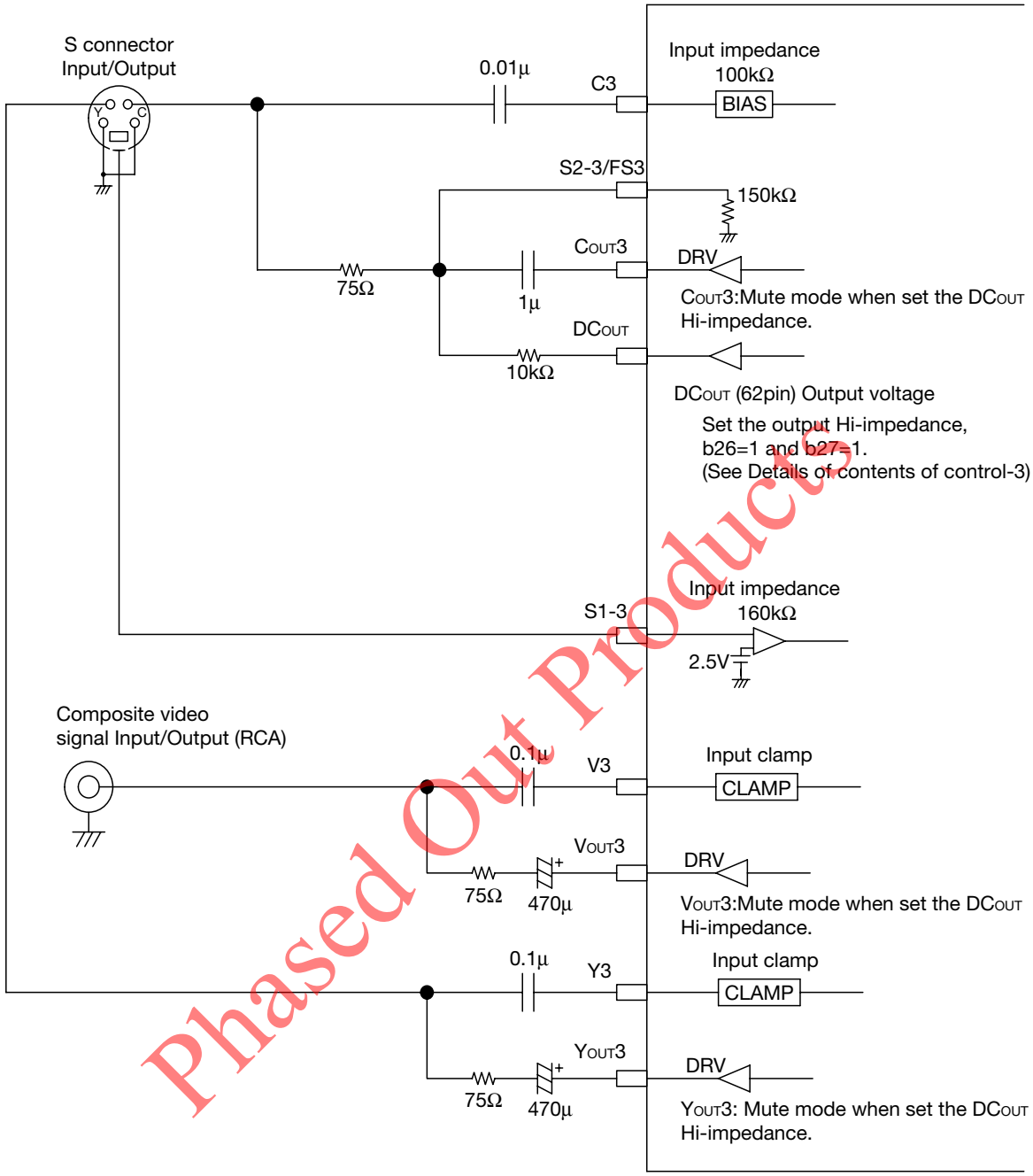
Note: Be careful because a DC voltage changes when you short an adjoining terminal by the resistance.

· We shall not be liable for any trouble or damage caused by using this circuit.

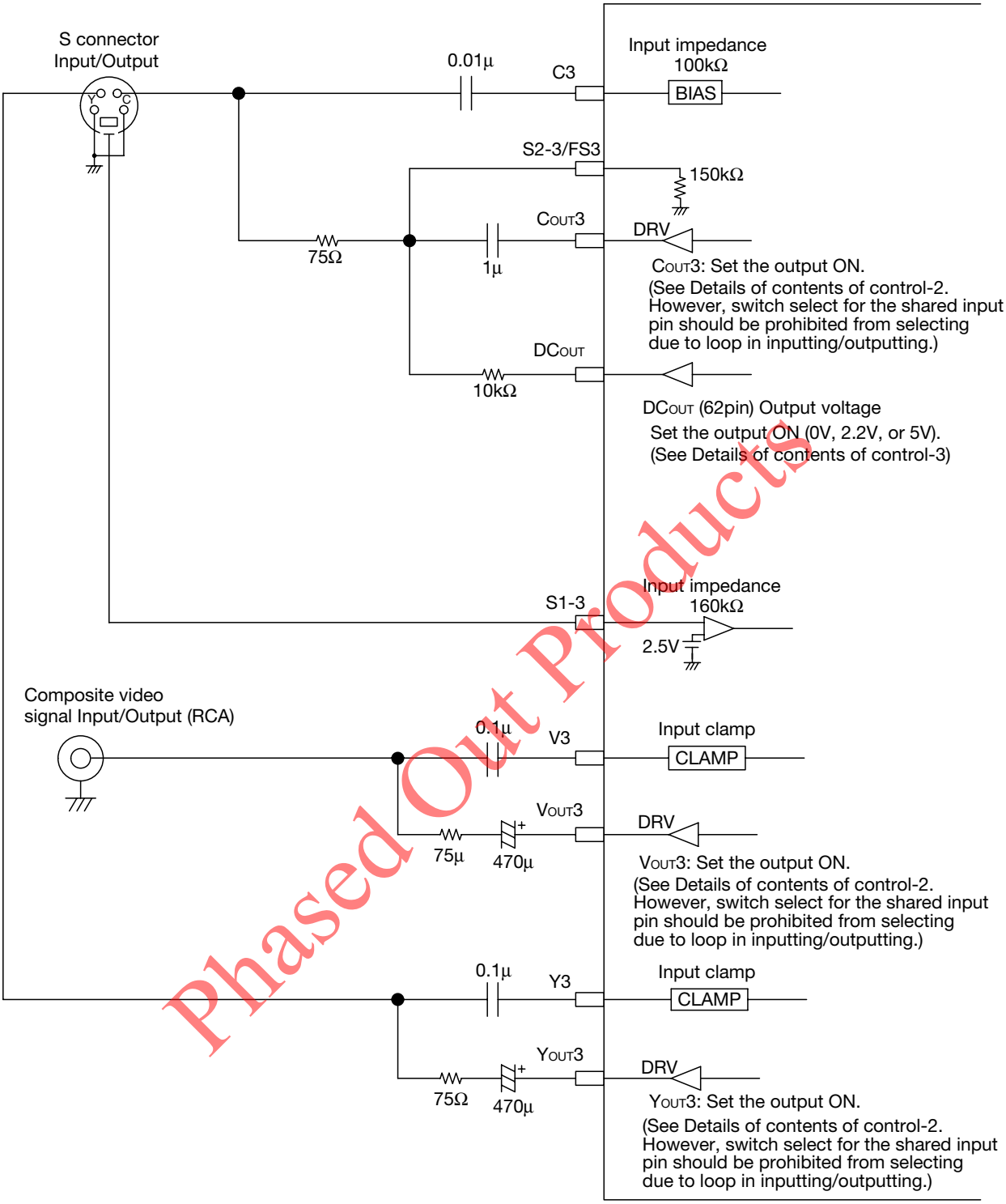
· In the event a problem which may affect industrial property or any other rights of us or a third party happens during the use of information in these circuit, we shall not be liable for any problem, nor grant a license therefore.

Application circuit as an output or an input pin

(1) Settings when used as an input pin

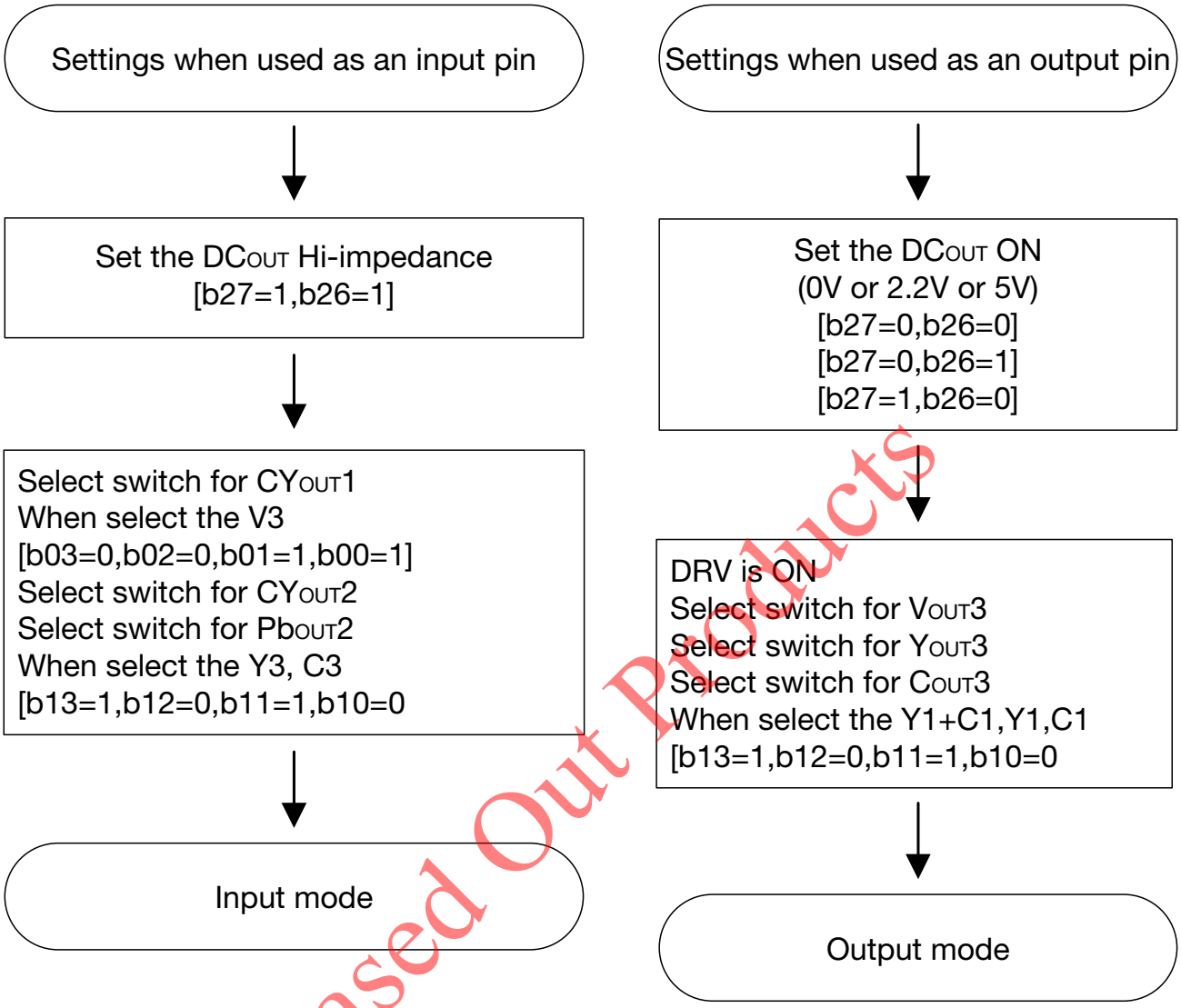


(2) Settings when used as an output pin



Flowchart for applications as an output or an input pin

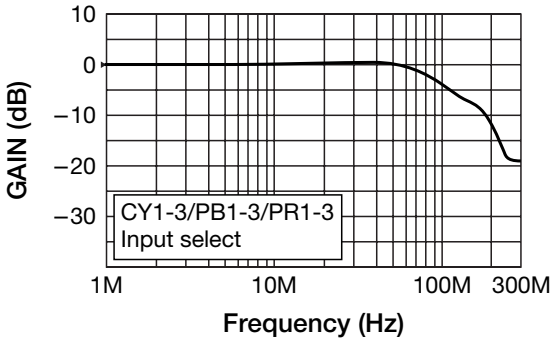
This is a flowchart applying to the Application Circuit2



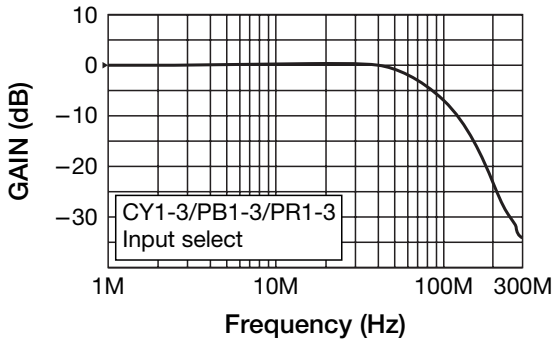
Characteristics

Frequency characteristic

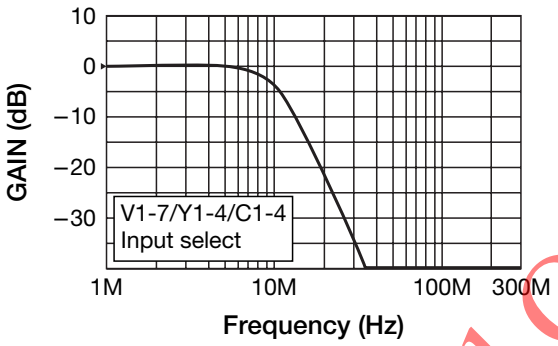
OUT1 THRU 0dB



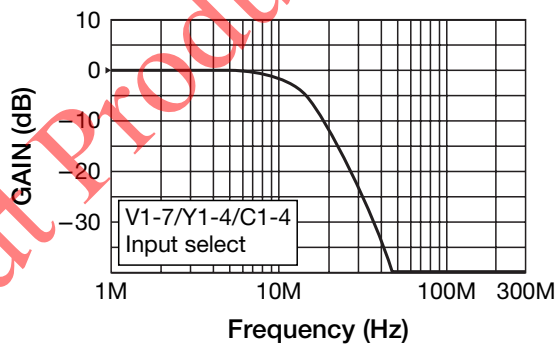
OUT2 THRU 0dB



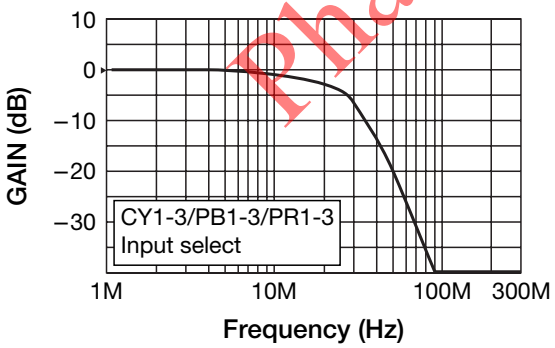
OUT1, 2 LPF1(fc=6.75MHz) 0dB



OUT1, 2 LPF2 (fc=13.5MHz) 0dB

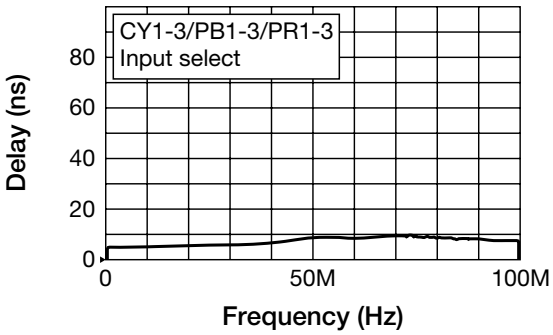


OUT1, 2 LPF3 (fc=24MHz) 0dB

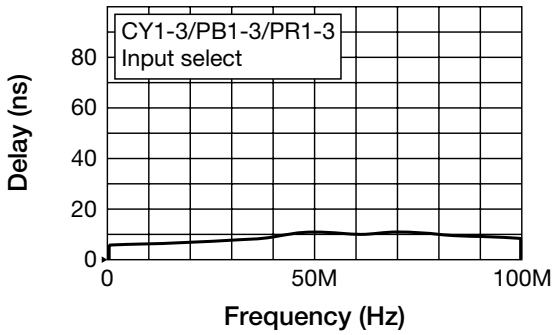


Group delay

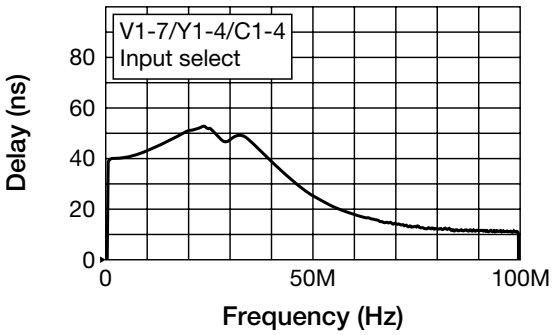
OUT1 THRU



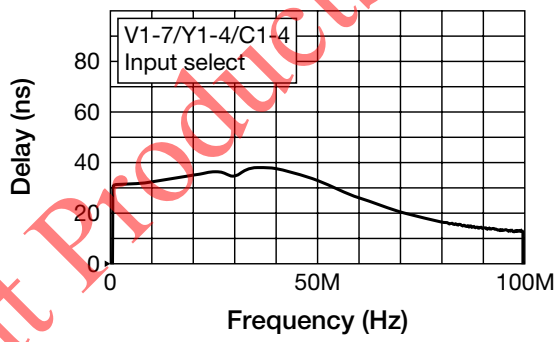
OUT2 THRU



OUT1, 2 LPF1 (fc=6.75MHz)



OUT1, 2 LPF2 (fc=13.5MHz)



OUT1, 2 LPF3 (fc=24MHz)