
MSM9563

IC for FM Multiplex Data Demodulation

GENERAL DESCRIPTION

The MSM9563 is an IC which demodulates FM character multiplex signals in the DARC (Data Radio Channel)*¹ format to acquire digital data. The MSM9563 operates at 3 V.

In the DARC format, baseband signals at ordinary FM broadcasting frequencies are multiplexed with 16 kbps digital data which is L-MSK-modulated at 76 kHz.

The MSM9563 has a bandpass filter consisting of an SCF, frame synchronization circuit, and error correction circuit on a single chip.

They allow a system for acquisition of digital data to be easily constructed by externally mounting an FM receiver tuner, microcontroller for control, and memory for temporary storage of data.

The MSM9563, a FM multiplex demodulator, has a simple configuration, and is equipped with only necessary functions. By making changes to software for the external microcontroller, the MSM9563 meets the various requirements of FM multiplex broadcasting services to be offered in future.

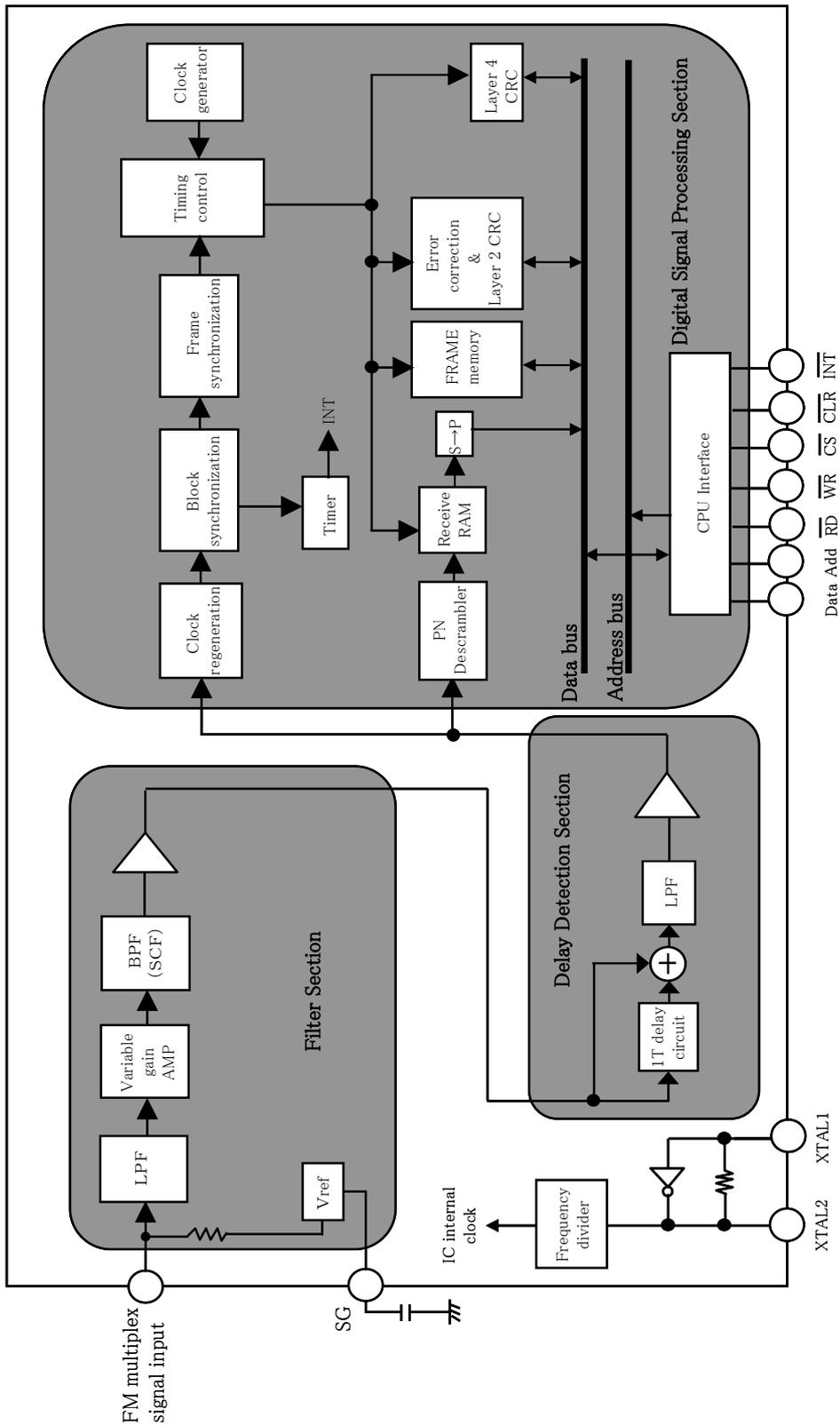
*1 DARC is a registered trademark of NHK Engineering Services.

Any manufacturer licensed by NHK Engineering Service can manufacture and sell products that utilize the DARC technology.

FEATURES

- Built-in two receive channels including main channel and sub-channel (one of two FM stations can be selected)
- Internal frame memory enables automatic error correction.
- Built-in bandpass filter (SCF)
- Built-in block synchronization circuit and frame synchronization circuit
- The number of synchronization protecting steps can be set
- Regeneration of data clocks by digital PLL
- 1T delay detector
- Built-in error correcting circuit (Vertical/Horizontal)
- Built-in layer-4 and layer-2 CRC processing circuit
- International frame formats A (supporting a real time block), B, and C available
- Microcontroller parallel interface
- Clock output for external devices (64 kHz to 8.192 MHz selectable)
- Power source: 3.0 to 3.6 V
- Package: 44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSM9563GA)

BLOCK DIAGRAM



PIN DESCRIPTIONS

Function	Symbol	Pin	Type	Description
Microcontroller interface	$\overline{\text{WR}}$	16	I	Write signal to internal register.
	$\overline{\text{RD}}$	18	I	Read signal to internal register.
	$\overline{\text{INT}}$	15	O	Interrupt signal to microcontroller. When set to “L”, an interrupt is generated.
	$\overline{\text{CS}}$	31	I	Chip select signal. When set “L”, the read, write, and data bus signals become effective.
	$\overline{\text{CLR}}$	40	I	When set “L”, the internal register is initialized, and the IC enters power down mode.
	A0 to A5	33 to 38	O	Address signal to internal register.
	DB0 to DB7	19 to 26	I/O	Data bus signal to internal register.
Tuner interface	AIN	6	I	FM multiple signal input.
	SG	5	O	Analog reference voltage pin. Connect a capacitor between this pin and the analog ground pin to prevent noise.
Analog section test	MON	1	O	Analog section waveform monitoring pin. The mode setting for the blocks in the analog section is specified by the analog section control register.
	ADETIN	2	I	Analog signal input pin for testing.
Digital section test	MOUT0 to MOUT6	8 to 14	O	Digital section test signal output and monitor output pins.
Clock	XTAL1	29	I	8.192 MHz crystal connection.
	XTAL2	30	O	8.192 MHz crystal connection.
	XOUT	32	O	Pin to supply variable clock (64 kHz to 8.192 MHz) to external devices.
	$\overline{\text{XOUTC}}$	7	I	XOUT control. “L” sets XOUT output, “H” sets XOUT output inhibit. This pin is pulled up internally.
Power supply	AV_{DD}	3	—	Analog power supply.
	AGND	4	—	Analog ground.
	DV_{DD}	28	—	Digital power supply.
	DGND	27	—	Digital ground.

ELECTRICAL CHARACTERISTICS

1. ABSOLUTE MAXIMUM RATINGS

No.	Parameter	Symbol	Condition	Rating	Unit
1	Power supply voltage	AVDD	AVDD = DVDD Ta = 25°C	-0.3 to +7.0	V
		DVDD			
2	Input voltage	Vi		-0.3 to AVDD + 0.3	
	Output voltage	Vo		-0.3 to DVDD + 0.3	
3	Maximum power dissipation	PD	Ta = 25°C, per package	400	mW
			Ta = 25°C, per output	50	
4	Storage temperature	TSTG	—	-55 to +150	°C

2. RECOMMENDED OPERATING CONDITIONS

No.	Parameter	Symbol	Condition	Range	Unit	Applied Pin
1	Power supply voltage	AVDD	AVDD = DVDD	3.0 to 3.6	V	AVDD
		DVDD				DVDD
2	Crystal oscillation frequency	fXTAL	—	8.192 MHz ±100 ppm	—	XTAL1, XTAL2
3	FM multiplex signal input voltage	VAIN*	Variable amplifier gain: × 1	0.6 to 0.9	V _{P-P}	AIN
			Variable amplifier gain: × 1.5	0.4 to 0.6		
			Variable amplifier gain: × 2	0.3 to 0.4		
			Variable amplifier gain: × 3	0.2 to 0.3		
4	Operating temperature	Ta	—	-40 to +85	°C	—

* Peak values (a total voltage of the following signals (a) to (c)) of composite signals including multiplex signals.

(a) Voice signals (100% modulated: voice max.)

(b) Pilot signal

(c) FM multiplex signals (10%: LMSK max.)

The maximum amplitude of an input signal is in the range of 0.9 V_{P-P} in which the internal IC circuit is not saturated.

Therefore, multiplex signals of up to 0.9 V_{P-P} can be input if only multiplex signals (excluding composite signals) are input from a signal generator.

3. DC CHARACTERISTICS

(DVDD = AVDD = 3.0 to 3.6 V, DGND = AGND = 0 V, Ta = -40 to +85°C)

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
1	Input voltage	V _{IH}	—	0.8 × DVDD	—	—	V	WR, RD, XOUTC, DB0 to DB7, CS, A0 to A5, CLR
		V _{IL}		—	—	0.2 × DVDD		
2	Output voltage	V _{OH}	I _{OH} = -1 mA	DVDD -0.5	—	—	V	MOUT0 to MOUT6, INT, DB0 to DB7, XOUT
		V _{OL}	I _{OL} = 2 mA	—	—	0.45		
3	Input current 1	I _{IH1}	V _{IH} = DVDD	—	—	2	μA	WR, RD, CS, DB0 to DB7, A0 to A5, CLR
		I _{IL1}	V _{IL} = DGND	-2	—	—		
4	Input current 2	I _{IH2}	V _{IH} = AVDD	—	—	2	μA	ADETIN
		I _{IL2}	V _{IL} = AGND	-2	—	—		
5	Input current 3	I _{IH3}	V _{IH} = DVDD	—	—	2	μA	XOUTC
6	Pull-up current	I _{pull}	DVDD = 3 V, V _{IL} = DGND	3	15	50	μA	
7	Output off-leakage current	I _{OH}	V _{OH} = AVDD During nonmonitoring (Hiz)	—	—	2	μA	MON
		I _{OL}	V _{OL} = AGND During nonmonitoring (Hiz)	-2	—	—		
8	Supply current	I _{DD}	During operation, no load f = 8.192 MHz	—	14	28	mA	AVDD, DVDD
			During power down, no load	—	—	50	μA	

4. AC CHARACTERISTICS

(DVDD = AVDD = 3.0 to 3.6 V, DGND = AGND = 0 V, Ta = -40 to +85°C)

No.	Parameter	Symbol*	Condition	Min.	Typ.	Max.	Unit	Applied Pin
1	Write setup time	t_{SWR1}	See figure 1	3	—	—	ns	\overline{WR} , \overline{CS} , A0 to A5, DB0 to DB7
		t_{SWR2}	See figure 1	90	—	—		
2	Write hold time	t_{HWR1}	See figure 1	-18	—	—	ns	\overline{WR} , \overline{CS} , A0 to A5, DB0 to DB7
		t_{HWR2}	See figure 1	10	—	—		
3	Write pulse width	t_{WWR}	See figure 1	90	—	—	ns	\overline{WR}
4	Read setup time	t_{SRD}	See figure 2	3	—	—	ns	\overline{RD} , \overline{CS} , A0 to A5
5	Read hold time	t_{HRD}	See figure 2	-18	—	—	ns	\overline{RD} , \overline{CS} , A0 to A5
6	Read pulse width	t_{WRD}	See figure 2	90	—	—	ns	\overline{RD}
7	Read data output delay (1)	t_{DRD1}	See figure 2	—	—	90	ns	\overline{RD} , DB0 to DB7
8	Read data output delay (2)	t_{DRD2}	See figure 2	—	—	20	ns	\overline{RD} , DB0 to DB7
9	Layer 4 data Interval between write and write	t_{IWRWR2}	Layer 4 CRC mode See figure 3	620	—	—	ns	\overline{WR}
10	Layer 4 data Interval between write and read	t_{IWRRD1}	Layer 4 CRC mode See figure 3	1.2	—	—	μ s	\overline{WR} , \overline{RD}
11	Interval between write and write	t_{IWRWR}	See figure 4	300	—	—	ns	\overline{WR}
12	Interval between write and write	t_{IWRWR1}	Continuously writing 0x3B to 0x3D to the same address See figure 5	550	—	—	ns	\overline{WR}
13	Interval between write and read	t_{IWRRD}	See figure 4	300	—	—	ns	\overline{WR} , \overline{RD}
14	Interval between read and read	$t_{IRD RD}$	See figure 6	300	—	—	ns	\overline{RD}
15	Interrupt CLR delay	$t_{DINTCLR}$	See figure 7	200	—	—	ns	\overline{INT} , \overline{WR}
16	CLR pulse width	t_{WCLR}	See figure 8	200	—	—	ns	\overline{CLR}

* See "TIMING DIAGRAM".

5. FILTER CHARACTERISTICS

(DV_{DD} = AV_{DD} = 3.0 to 3.6 V, DGND = AGND = 0 V, Ta = -40 to +85°C)

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied Pin
1	BPF pass band attenuation	GAIN1	72 to 80 kHz Variable gain amplifier gain: 0 dB	—	—	3.0	dB	MON
2	BPF block band attenuation (1)	GAIN2	0 to 53 kHz Variable gain amplifier gain: 0 dB	50	—	—	dB	MON
3	BPF block band attenuation (2)	GAIN3	100 to 500 kHz Variable gain amplifier gain: 0 dB	50	—	—	dB	MON

6. TIMING DIAGRAM

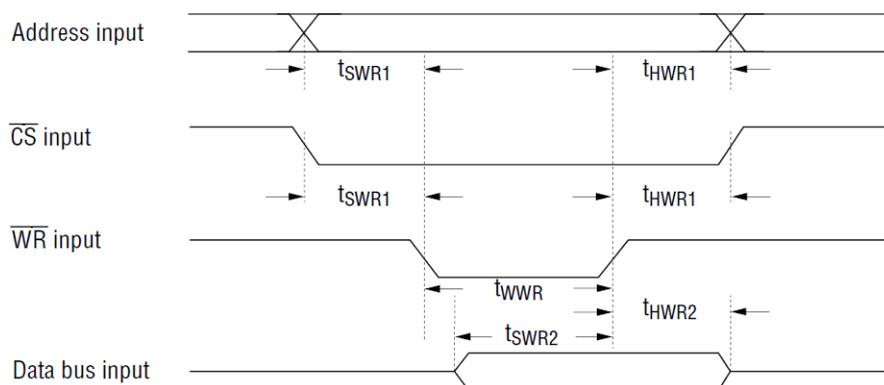


Figure 1 Write Timing

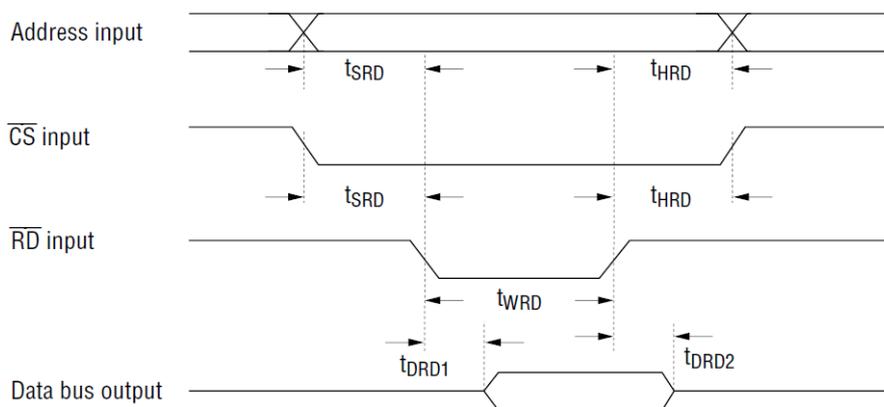


Figure 2 Read Timing

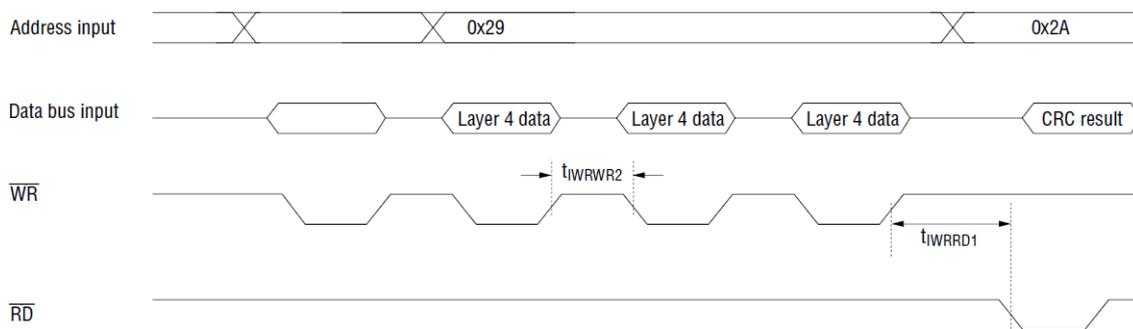


Figure 3 Layer 4 CRC mode and Layer 4 VICS mode Timing

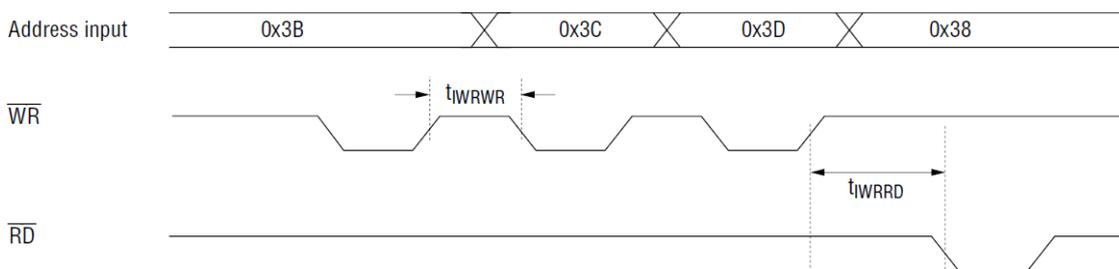


Figure 4 Interval between write and write or between write and read

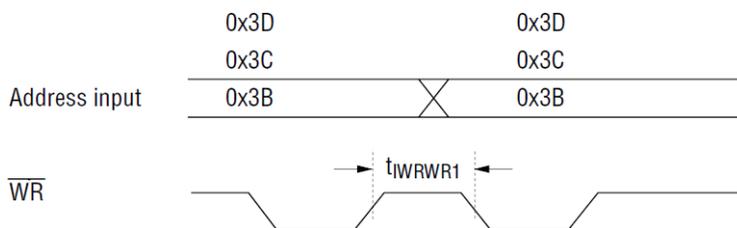


Figure 5 When 0x3B to 0x3D are continuously written at the same address (This is a rare case)

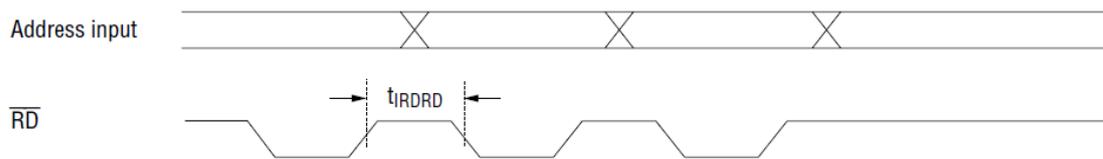


Figure 6 Interval between read and read

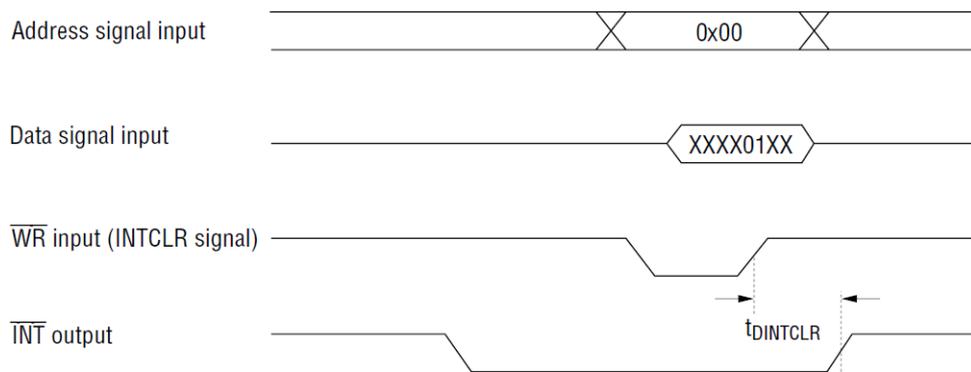


Figure 7 Interrupt CLR Timing

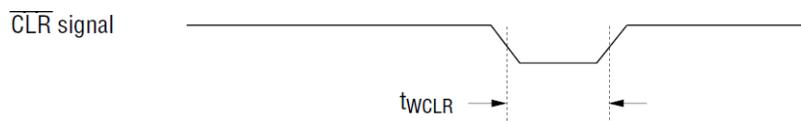
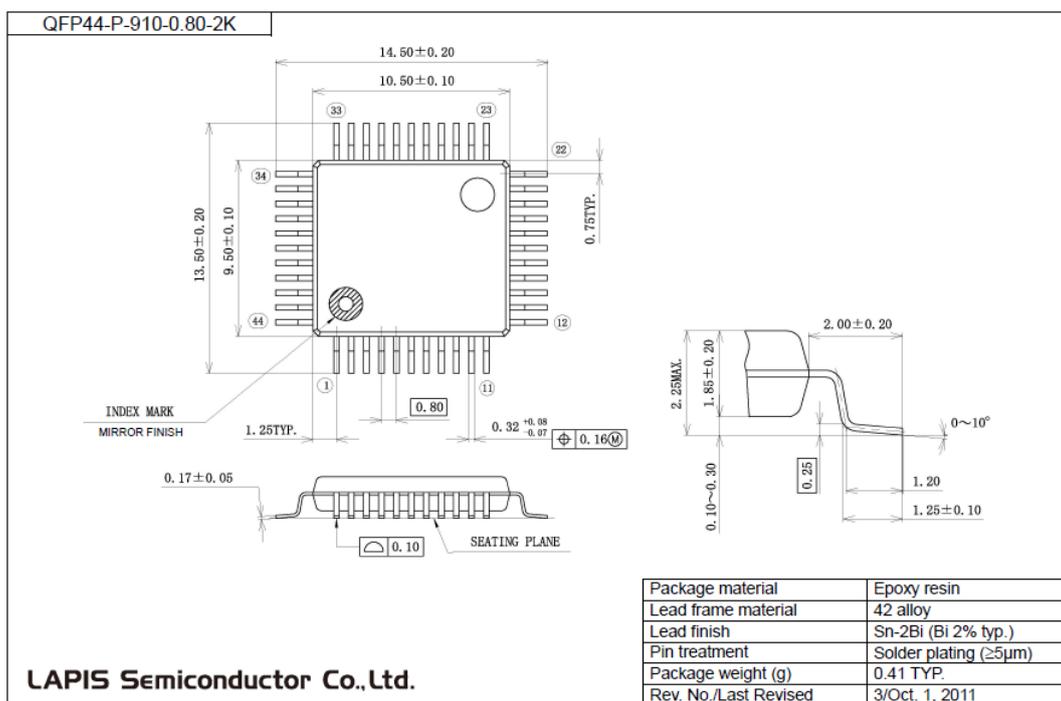


Figure 8 Clear pulse width

PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9563-01	Aug. 29, 2006	-	-	Final edition 1
FEDL9563-02	Nov. 1, 2011	-	2	BLOCK DIAGRAM is added.
		-	3	PIN CONFIGURATION is added.
		1	1	Power Source is corrected to "3.0 to 3.6V"
		2-5	4-7	Power supply voltage Range is corrected to "3.0 to 3.6V"
FEDL9563-03	Nov. 7, 2011	-	4	PIN DESCRIPTIONS is added.

NOTICE

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

Copyright 2010 - 2011 LAPIS Semiconductor Co., Ltd.