National Semiconductor

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MM54HC595/MM74HC595 8-Bit Shift Registers with Output Latches

General Description

This high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 TRI-STATE® outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

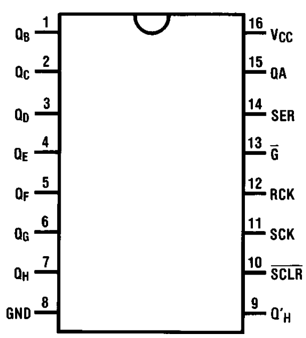
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

Connection Diagram

Dual-In-Line Package



TL/F/5342–1

Top View

Order Number MM54HC595 or MM74HC595

Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Function
X	X	X	H	Q_A thru Q_H = TRI-STATE
X	X	L	L	Shift Register cleared $Q'_H = 0$
X	↑	H	L	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	L	Contents of Shift Register transferred to output latches

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to $+7.0$V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC}+1.5$V
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC}+0.5$V
Clamp Diode Current (I_{IK}, I_{OK})	$\pm$20 mA
DC Output Current, per pin (I_{OUT})	$\pm$35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	$\pm$70 mA
Storage Temperature Range (T_{STG})	-65°C to $+150$°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	$+85$	°C
MM54HC	-55	$+125$	°C
Input Rise or Fall Times			
(t_r, t_f) $V_{CC}=2.0$V		1000	ns
$V_{CC}=4.5$V		500	ns
$V_{CC}=6.0$V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25$°C		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V 4.5V 6.0V		1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V V V
V_{IL}	Maximum Low Level Input Voltage**		2.0V 4.5V 6.0V		0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V V V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V 4.5V 6.0V	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V V V
	Q'$_H$	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA $\|I_{OUT}\|\leq 5.2$ mA	4.5V 6.0V	4.2 5.2	3.98 5.48	3.84 5.34	3.7 5.2	V V
	Q_A thru Q_H	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA $\|I_{OUT}\|\leq 7.8$ mA	4.5V 6.0V	4.2 5.7	3.98 5.48	3.84 5.34	3.7 5.2	V V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V 4.5V 6.0V	0 0 0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V V V
	Q'$_H$	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4$ mA $\|I_{OUT}\|\leq 5.2$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
	Q_A thru Q_H	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA $\|I_{OUT}\|\leq 7.8$ mA	4.5V 6.0V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		$\pm$0.1	$\pm$1.0	$\pm$1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	$V_{OUT}=V_{CC}$ or GND $\overline{G}=V_{IH}$	6.0V		$\pm$0.5	$\pm$5.0	$\pm$10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V $\pm$10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC}=5.5$V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to $Q_{H'}$	$C_L = 45$ pF	12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, RCK to Q_A thru Q_H	$C_L = 45$ pF	18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time from $\overline{G}$ to Q_A thru Q_H	$R_L = 1\ k\Omega$ $C_L = 45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q_H	$R_L =\ k\Omega$ $C_L = 5$ pF	15	25	ns
t_S	Minimum Setup Time from SER to SCK			20	ns
t_S	Minimum Setup Time from $\overline{SCLR}$ to SCK			20	ns
t_S	Minimum Setup Time from SCK to RCK (See Note 5)			40	ns
t_H	Minimum Hold Time from SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

Note 5: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

AC Electrical Characteristics $V_{CC} = 2.0–6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$ Typ	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L = 50$ pF	2.0V	10	6	4.8	4.0	MHz
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q'$_H$	$C_L = 50$ pF	2.0V	58	210	265	315	ns
		$C_L = 150$ pF	2.0V	83	294	367	441	ns
		$C_L = 50$ pF	4.5V	14	42	53	63	ns
		$C_L = 150$ pF	4.5V	17	58	74	88	ns
		$C_L = 50$ pF	6.0V	10	36	45	54	ns
		$C_L = 150$ pF	6.0V	14	50	63	76	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_A thru Q_H	$C_L = 50$ pF	2.0V	70	175	220	265	ns
		$C_L = 150$ pF	2.0V	105	245	306	368	ns
		$C_L = 50$ pF	4.5V	21	35	44	53	ns
		$C_L = 150$ pF	4.5V	28	49	61	74	ns
		$C_L = 50$ pF	6.0V	18	30	37	45	ns
		$C_L = 150$ pF	6.0V	26	42	53	63	ns

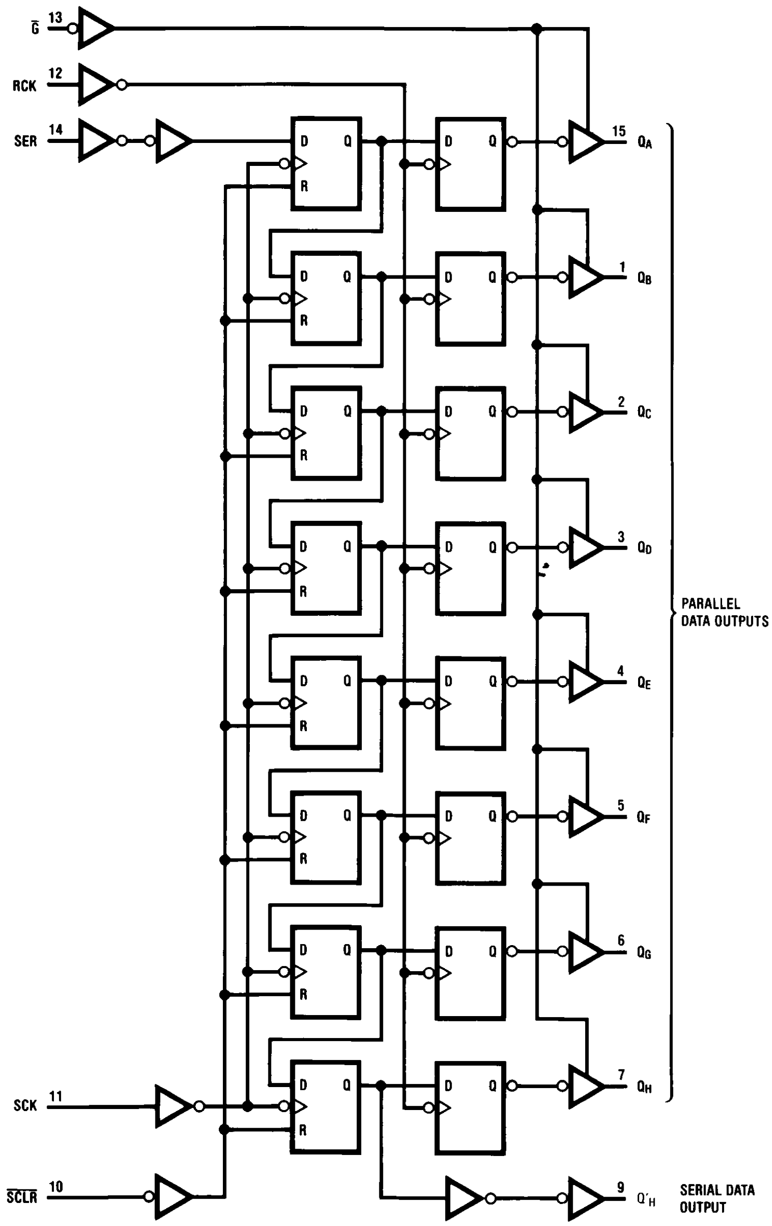
AC Electrical Characteristics

$V_{CC} = 2.0\text{–}6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified) (Continued)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SCLR}$ to Q'_H		2.0V 4.5V 6.0V		175 35 30	221 44 37	261 52 44	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable from $\overline{G}$ to Q_A thru Q_H	$R_L = 1\ k\Omega$ $C_L = 50$ pF $C_L = 150$ pF	 2.0V 2.0V	 75 100	 175 245	 220 306	 265 368	 ns ns
		$C_L = 50$ pF $C_L = 150$ pF	4.5V 4.5V	15 20	35 49	44 61	53 74	ns ns
		$C_L = 50$ pF $C_L = 150$ pF	6.0V 6.0V	13 17	30 42	37 53	45 63	ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q_H	$R_L = 1\ k\Omega$ $C_L = 50$ pF	2.0V 4.5V 6.0V	75 15 13	175 35 30	220 44 37	265 53 45	ns ns ns
t_S	Minimum Setup Time from SER to SCK		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_R	Minimum Removal Time from $\overline{SCLR}$ to SCK		2.0V 4.5V 6.0V		50 10 9	63 13 11	75 15 13	ns ns ns
t_S	Minimum Setup Time from SCK to RCK		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 26	ns ns ns
t_H	Minimum Hold Time SER to SCK		2.0V 4.5V 6.0V		5 5 5	5 5 5	5 5 5	ns ns ns
t_W	Minimum Pulse Width of SCK or $\overline{SCLR}$		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 22	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time Q_A–Q_H		2.0V 4.5V 6.0V	25 7 6	60 12 10	75 15 13	90 18 15	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time Q'_H		2.0V 4.5V 6.0V		75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 6)	$\overline{G} = V_{CC}$ $\overline{G} = GND$		90 150				pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Logic Diagram (positive logic)



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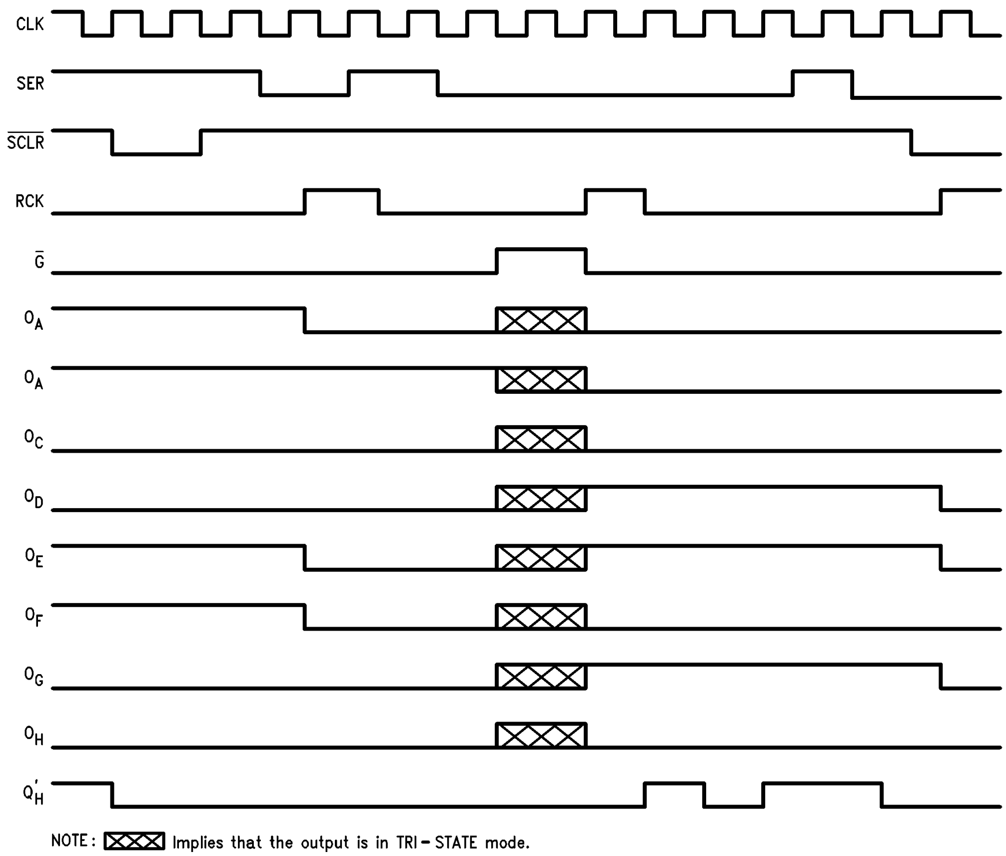
Timing Diagram

MM54HC595/MM74HC595



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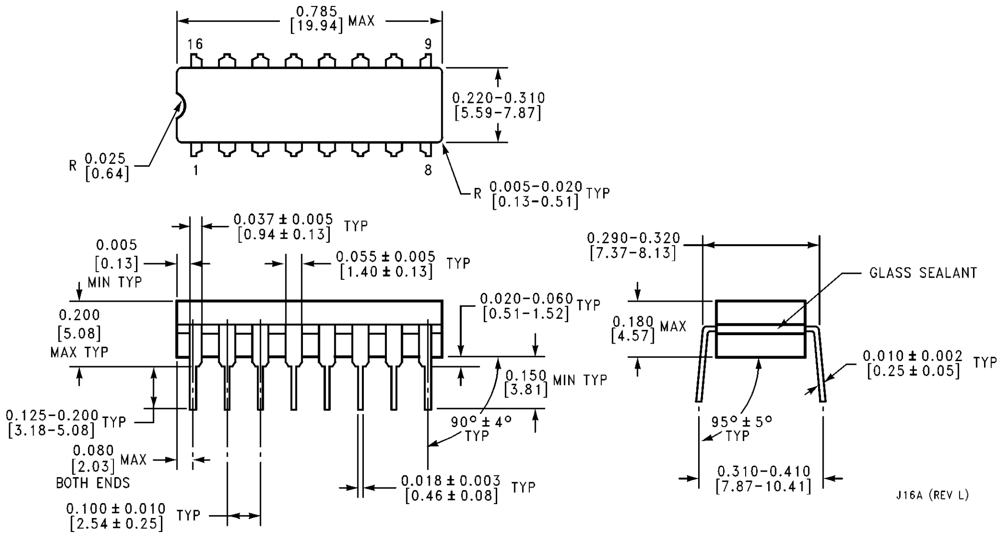
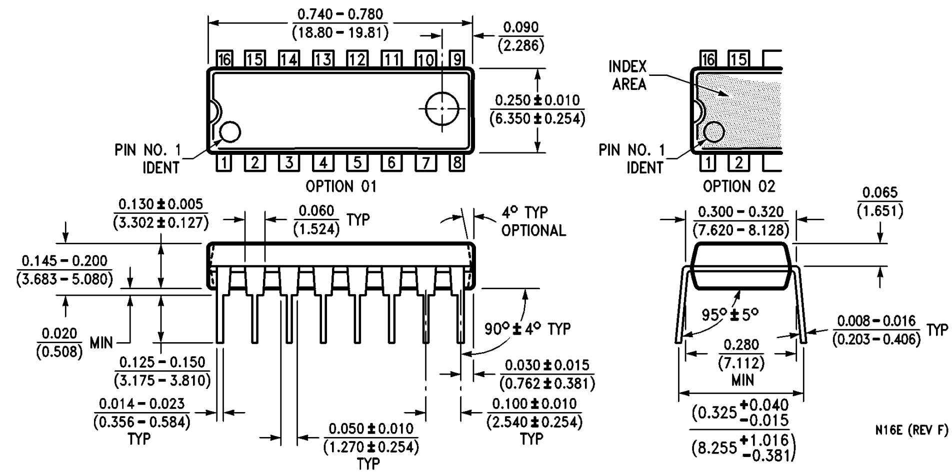
Physical Dimensions inches (millimeters)



Order Number MM54HC595J or MM54HC595J
NS Package J16A

Physical Dimensions inches (millimeters) (Continued)



Order Number MM54HC595N
NS Package N16E

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408