

Low Saturation PNP Epitaxial Planar Transistor

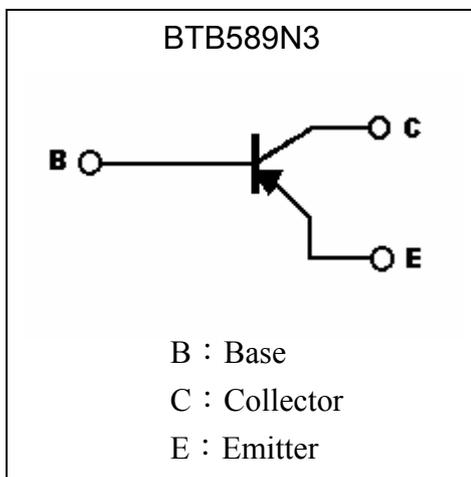
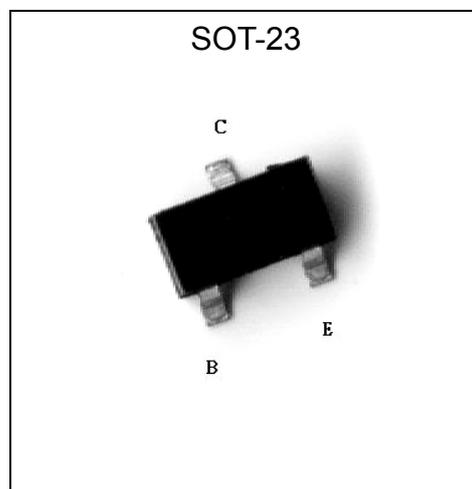
BTB589N3

Description

The BTB589N3 is designed with high current gain and low saturation voltage with collector current up to 1A continuous.

Features

- Low $V_{CE(SAT)}$, $V_{CE(SAT)} \leq -0.3V$ ($I_C / I_B = -1A / -100mA$)
- Large collector current, $I_C = -1A$
- Pb-free package

Symbol**Outline**

**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	-50	V
Collector-Emitter Voltage	V _{CEO}	-32	V
Emitter-Base Voltage	V _{EBO}	-5	V
Collector Current (DC)	I _C	-1	A
Collector Current (Pulse)	I _{CP}	-2	
Power Dissipation	P _d	310 (Note 1)	mW
		500 (Note 2)	
Thermal Resistance, Junction to Ambient	R _{θJA}	403 (Note 1)	°C/W
		250 (Note 2)	
Junction Temperature	T _j	-55~+150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note: 1. Device mounted on FR-4 PCB with minimum pad

2. Device mounted on FR-4 PCB with area of 4.5"x5", mounting pad 0.02 in² of 2 oz copper**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
B _V CBO	-40	-	-	V	I _C =-50μA
B _V CEO	-32	-	-	V	I _C =-1mA
B _V EBO	-5	-	-	V	I _E =-50μA
I _{CBO}	-	-	-100	nA	V _{CB} =-30V
I _{EBO}	-	-	-100	nA	V _{EB} =-4V
*V _{CE(sat)} 1	-	-	-0.25	V	I _C =-500mA, I _B =-50mA
*V _{CE(sat)} 2	-	-	-0.30	V	I _C =-1A, I _B =-100mA
*V _{CE(sat)} 3	-	-	-0.65	V	I _C =-2A, I _B =-200mA
*V _{BE(sat)}	-	-	-1.2	V	I _C =-1A, I _B =-100mA
*V _{BE(on)}	-	-	-1.1	V	V _{CE} =-2V, I _C =-1A
*h _{FE} 1	180	-	420	-	V _{CE} =-3V, I _C =-100mA
*h _{FE} 2	100	-	-	-	V _{CE} =-2V, I _C =-500mA
*h _{FE} 3	80	-	-	-	V _{CE} =-2V, I _C =-1A
*h _{FE} 4	30	-	-	-	V _{CE} =-2V, I _C =-2A
f _T	100	200	-	MHz	V _{CE} =-5V, I _C =-50mA, f=100MHz
C _{ob}	-	12	25	pF	V _{CB} =-10V, f=1MHz

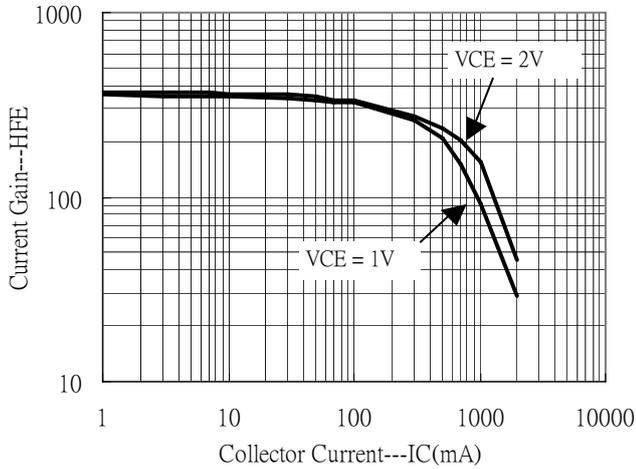
*Pulse Test: Pulse Width ≤380μs, Duty Cycle ≤2%

Ordering Information

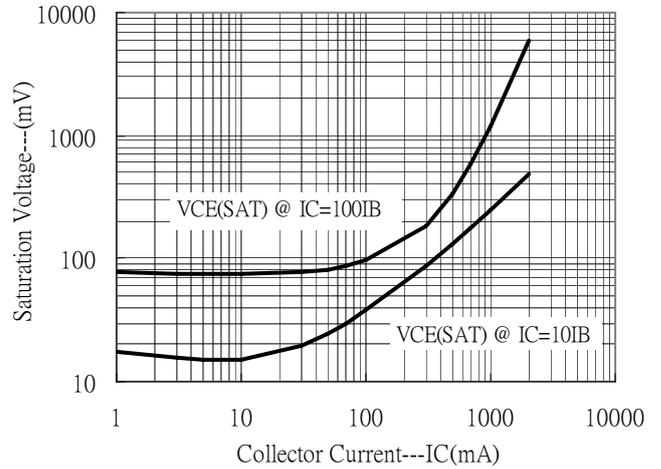
Device	Package	Shipping	Marking
BTB589N3	SOT-23 (Pb-free)	3000 pcs / Tape & Reel	AH

Characteristic Curves

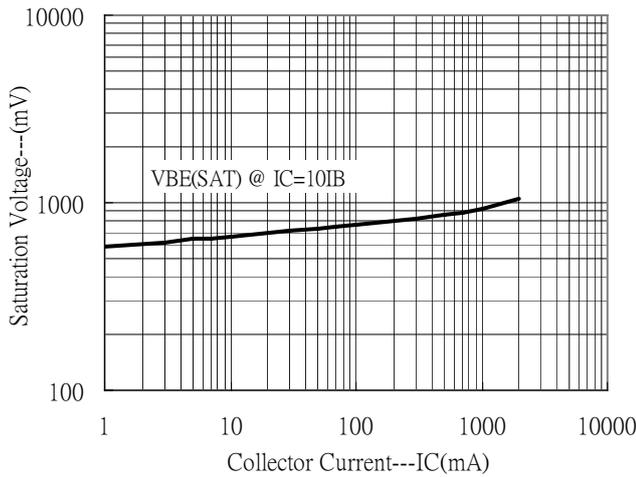
Current Gain vs Collector Current



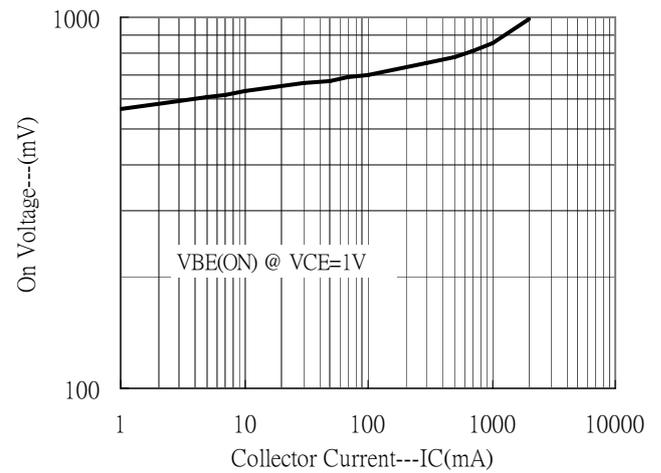
Saturation Voltage vs Collector Current



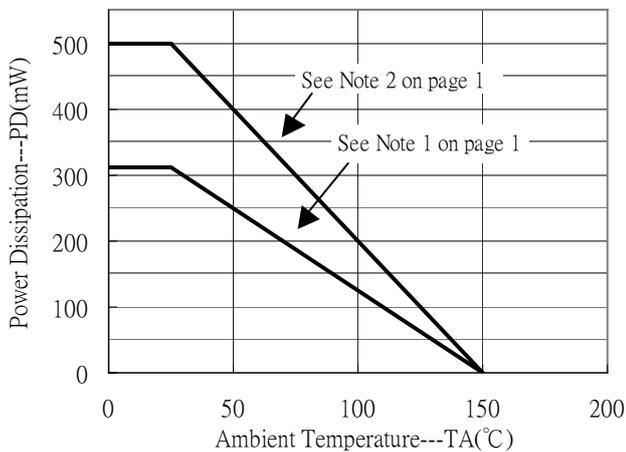
Saturation Voltage vs Collector Current



On Voltage vs Collector Current



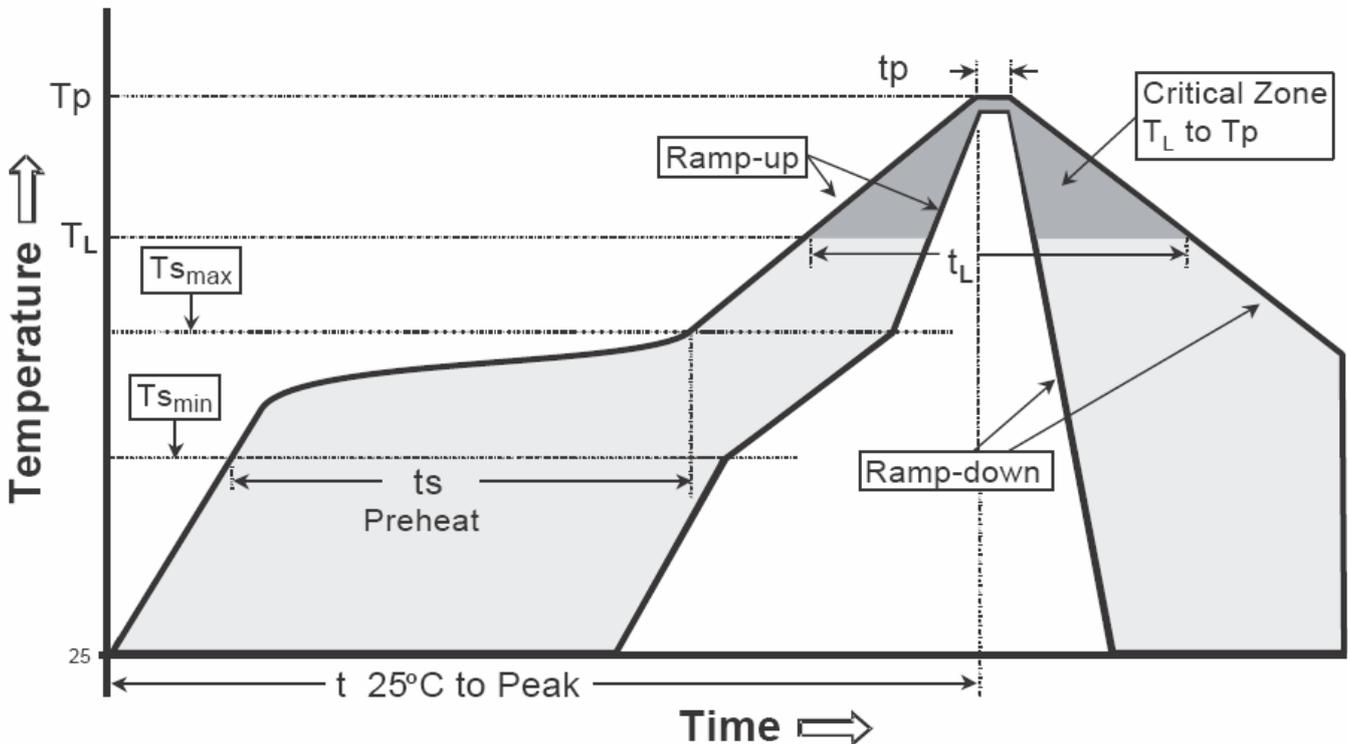
Power Derating Curves



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

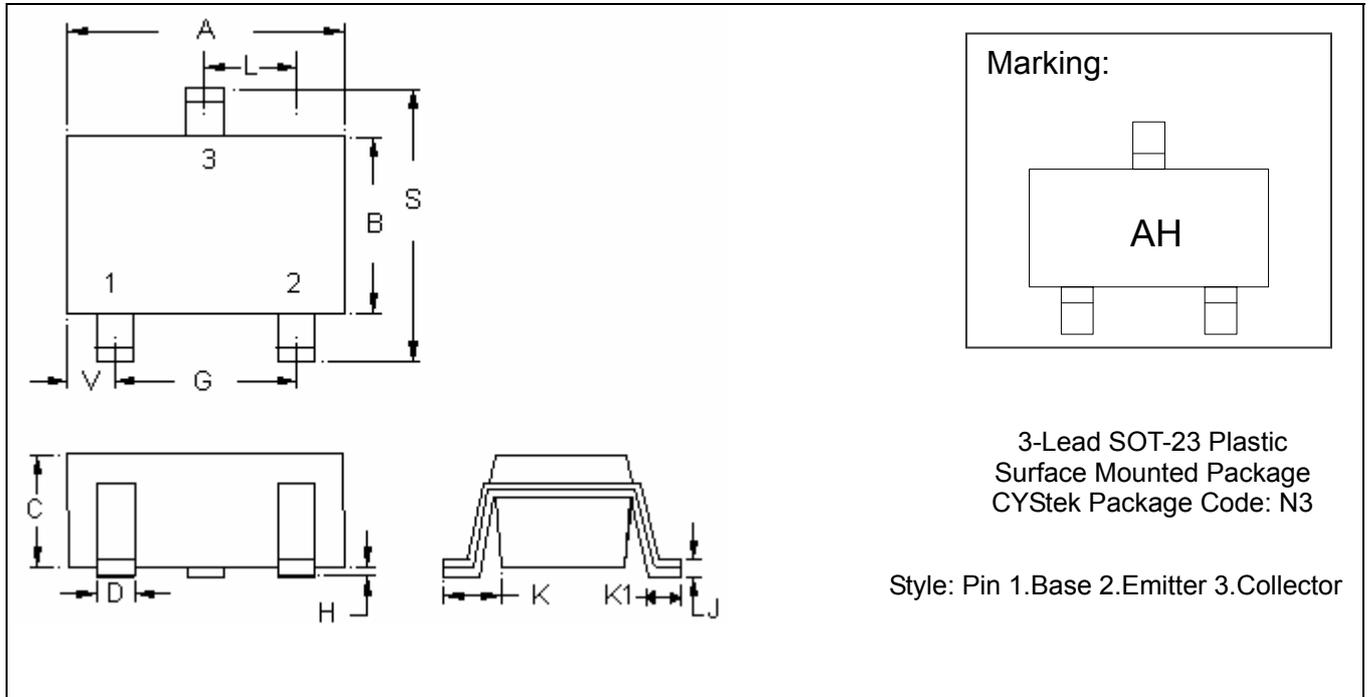
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Ts max to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _s min)	100°C	150°C
-Temperature Max(T _s max)	150°C	200°C
-Time(t _s min to t _s max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-23 Dimension



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0034	0.0070	0.085	0.177
B	0.0472	0.0630	1.20	1.60	K	0.0128	0.0266	0.32	0.67
C	0.0335	0.0512	0.89	1.30	K1	0.0118	0.0197	0.30	0.50
D	0.0118	0.0197	0.30	0.50	L	0.0335	0.0453	0.85	1.15
G	0.0669	0.0910	1.70	2.30	S	0.0830	0.1083	2.10	2.75
H	0.0005	0.0040	0.013	0.10	V	0.0098	0.0256	0.25	0.65

- Notes:**
- Controlling dimension: millimeters.
 - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy ; pure tin plated
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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