

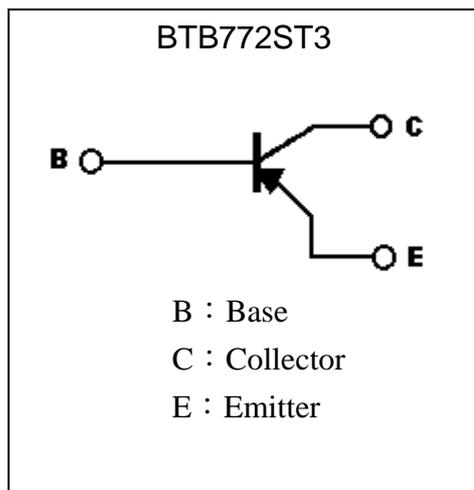
**Low Vcesat PNP Epitaxial Planar Transistor**

# BTB772ST3

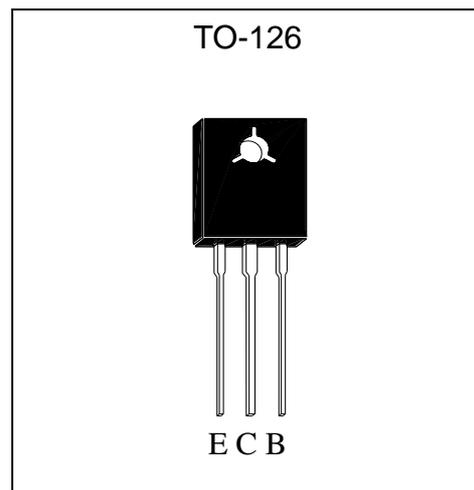
## Features

- Low  $V_{CE(sat)}$ , typically -0.45 V at  $I_C / I_B = -2A / -0.2A$
- Excellent current gain characteristics
- Pb-free lead plating and halogen-free package

## Symbol

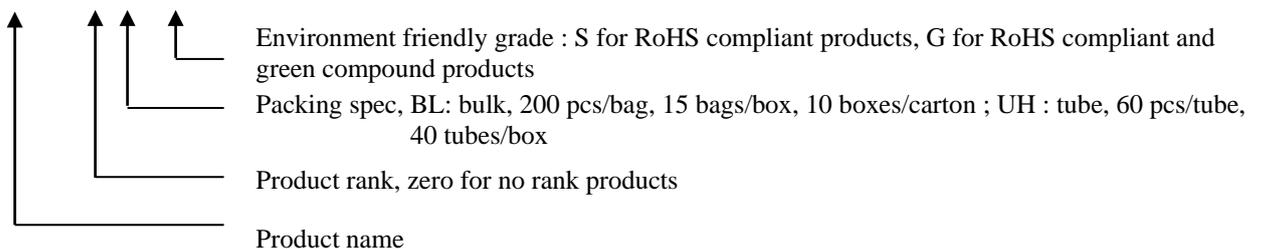


## Outline



## Ordering Information

Device	Package	Shipping
BTB772ST3-P-BL-X	TO-126 (Pb-free lead plating and halogen-free package)	200 pcs / bag, 3,000 pcs/box 30,000 pcs/carton
BTB772ST3-P-UH-X		60 pcs/ tube, 40 tubes/box



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V <sub>CBO</sub>	-40	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-30	V
Emitter-Base Voltage	V <sub>EBO</sub>	-5	V
Collector Current	I <sub>C</sub> (DC)	-2	A
	I <sub>C</sub> (pulse)	-5 *1	A
Power Dissipation	P <sub>d</sub> (Ta=25°C)	1	W
	P <sub>d</sub> (Tc=25°C)	10	
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

Note : \*1. Single Pulse Pw ≤ 300μs, Duty ≤ 2%.

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R <sub>th,j-c</sub>	12.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R <sub>th,j-a</sub>	125	°C/W

**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CBO</sub>	-40	-	-	V	I <sub>C</sub> =-50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	-30	-	-	V	I <sub>C</sub> =-1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	-5	-	-	V	I <sub>E</sub> =-50μA, I <sub>C</sub> =0
I <sub>CBO</sub>	-	-	-1	μA	V <sub>CB</sub> =-30V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	-1	μA	V <sub>EB</sub> =-5V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	-0.45	-0.6	V	I <sub>C</sub> =-2A, I <sub>B</sub> =-0.2A
*V <sub>BE(sat)</sub>	-	-1	-1.5	V	I <sub>C</sub> =-2A, I <sub>B</sub> =-0.2A
*h <sub>FE 1</sub>	120	-	-	-	V <sub>CE</sub> =-2V, I <sub>C</sub> =-20mA
*h <sub>FE 2</sub>	180	-	390	-	V <sub>CE</sub> =-2V, I <sub>C</sub> =-500mA
f <sub>T</sub>	-	80	-	MHz	V <sub>CE</sub> =-5V, I <sub>E</sub> =-0.1A, f=100MHz
C <sub>ob</sub>	-	55	-	pF	V <sub>CB</sub> =-10V, f=1MHz

\*Pulse Test : Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

**Classification Of h<sub>FE 2</sub>**

Rank	P
Range	180~390

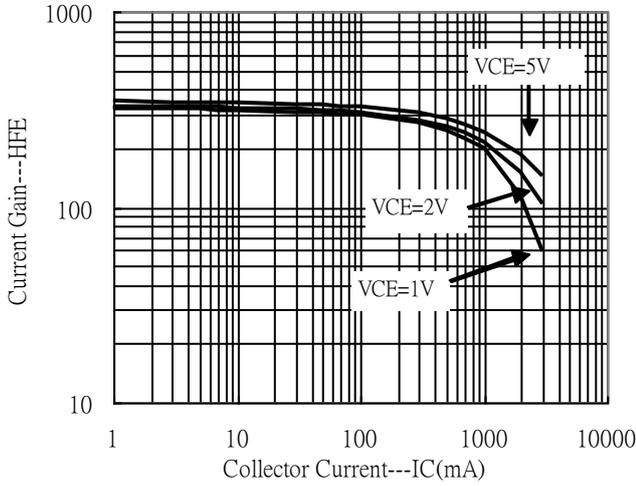
**Recommended Storage Condition:**

Temperature : 10~ 35 °C

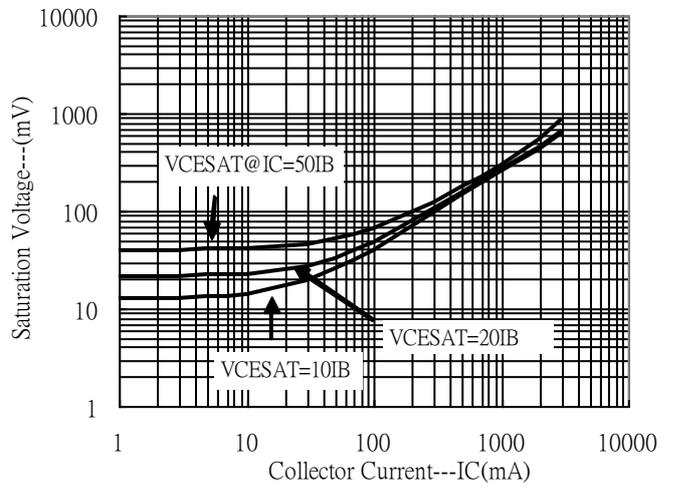
Humidity : 30~ 60% RH

**Typical Characteristics**

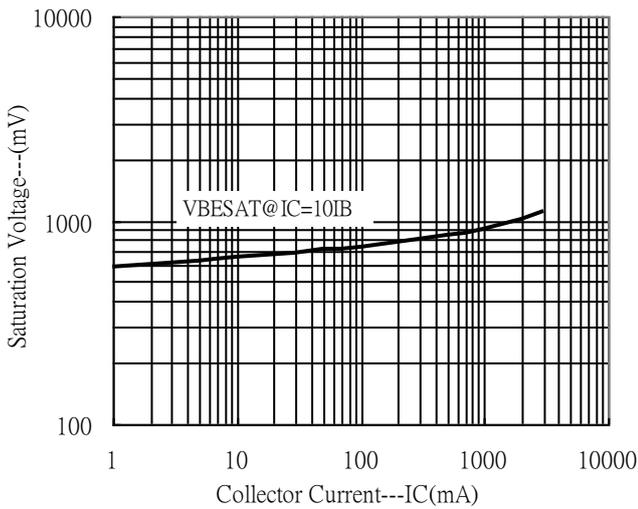
Current Gain vs Collector Current



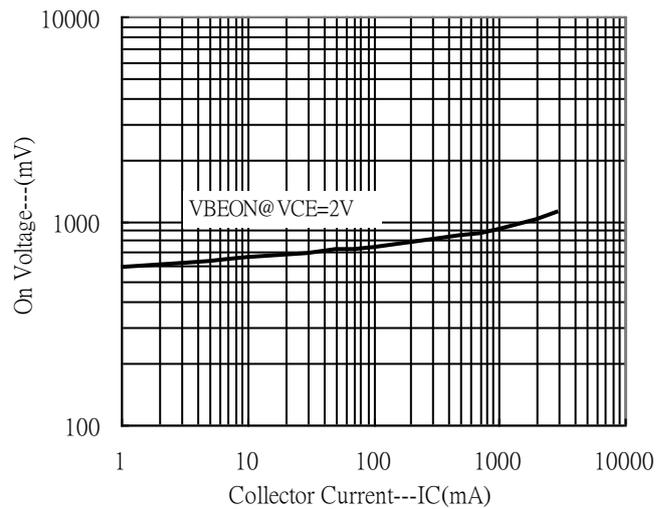
Saturation Voltage vs Collector Current



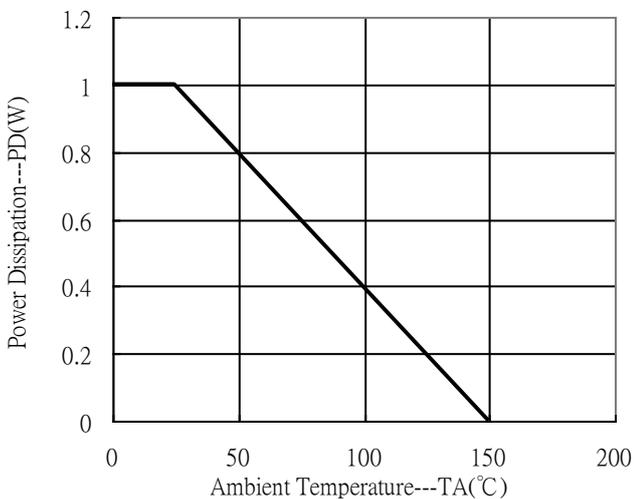
Saturation Voltage vs Collector Current



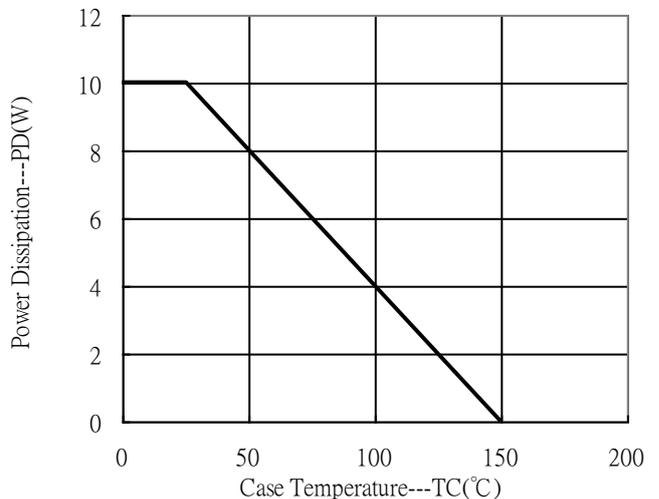
On Voltage vs Collector Current



Power Derating Curve



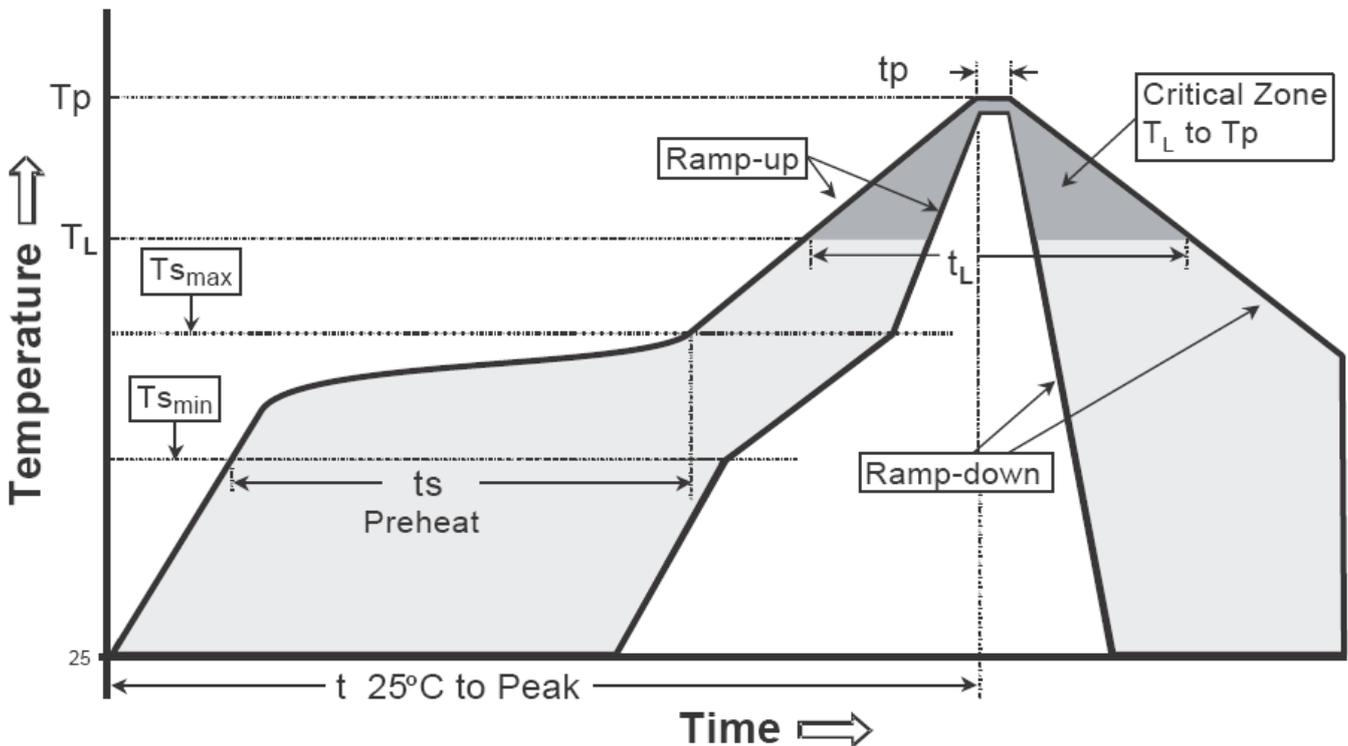
Power Derating Curve



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

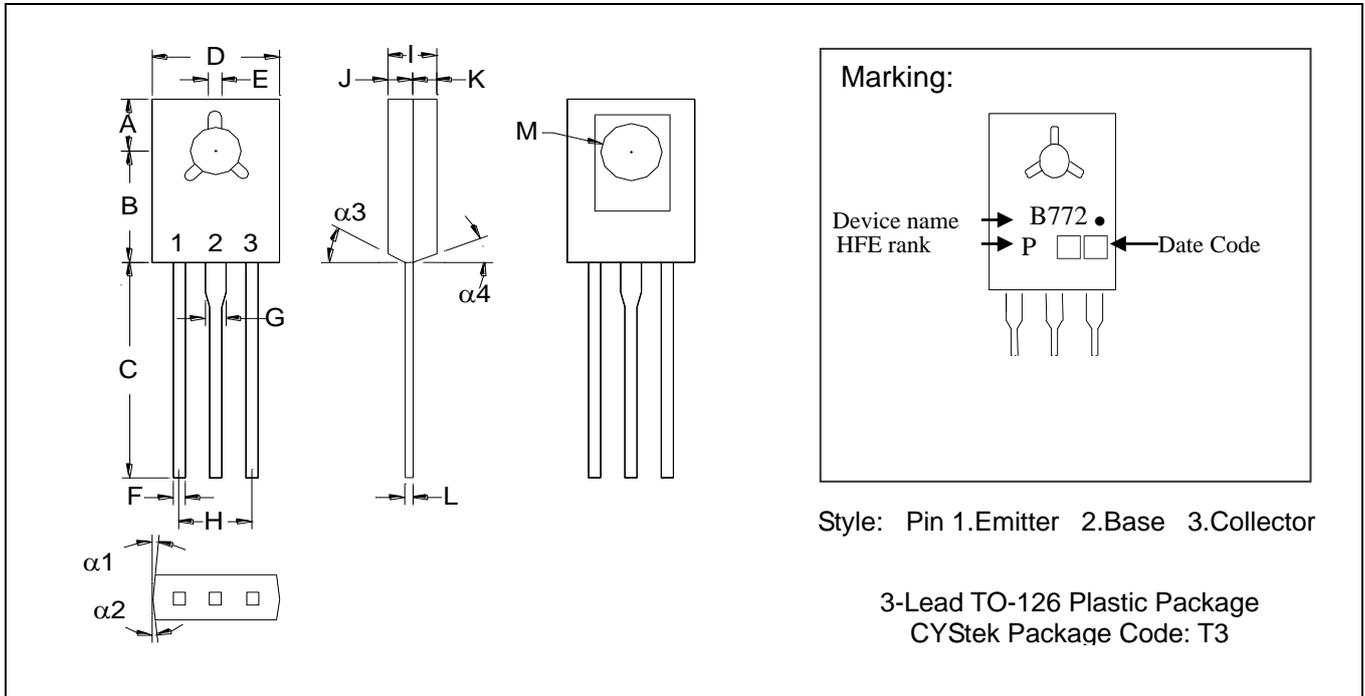
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-126 Dimension**



\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
$\alpha 1$	-	*3°	-	*3°	F	0.0280	0.0319	0.71	0.81
$\alpha 2$	-	*3°	-	*3°	G	0.0480	0.0520	1.22	1.32
$\alpha 3$	-	*3°	-	*3°	H	0.1709	0.1890	4.34	4.80
$\alpha 4$	-	*3°	-	*3°	I	0.0950	0.1050	2.41	2.66
A	0.1500	0.1539	3.81	3.91	J	0.0450	0.0550	1.14	1.39
B	0.2752	0.2791	6.99	7.09	K	0.0450	0.0550	1.14	1.39
C	0.5315	0.6102	13.50	15.50	L	-	*0.0217	-	*0.55
D	0.2854	0.3039	7.52	7.72	M	0.1378	0.1520	3.50	3.86
E	0.0374	0.0413	0.95	1.05					

- Notes:**
- Controlling dimension: millimeters.
  - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
  - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: KFC; tin plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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