HMC-C061

v02.0711

50 Gbps, DOUBLE-EDGE TRIGGERED D-TYPE FLIP-FLOP MODULE

Features

Supports data rates 50 Gbps

Half Rate Clock Input (1 MHz - 25 GHz)

Inputs Terminated Internally in 50 ohms

Supports Single-Ended or Differential Operation

Very Low Power Consumption: 690 mW

Less than 200 fs Additive RMS Jitter

Fast Rise and Fall Times: <10ps

Single -3.3 V Power Supply

Hermetically Sealed Module: 1.85mm connectors

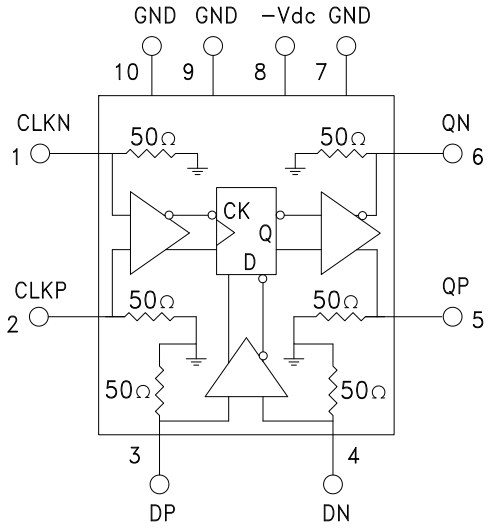
-40°C to +70°C Operating Temperature

Typical Applications

The HMC-C061 is ideal for:

- OC-768 and SDH STM-256 Equipment
- Serial Data Transmission up to 50 Gbps
- Short, intermediate, and long haul fiber optic applications
- Broadband Test and Measurement

Functional Diagram



General Description

The HMC-C061 is a double edge triggered D-type Flip-Flop (DETDFF) designed to support data transmission rates of up to 50 Gbps. The device operates at half the sampling frequency of the applied data rate. The maximum clock rate is 25 GHz for 50 Gbps input data. The clock input is broadband from DC to 25 GHz. During normal operation, data is transferred to the outputs on both the positive edge and the negative edge of the clock. All input signals to the HMC-C061 are terminated with 50 Ohms to ground on-chip, and may be either AC or DC coupled. The differential outputs of the HMC-C061 may be either AC or DC coupled. Outputs can be connected directly to a 50 Ohm to ground terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-ground DC voltage. The HMC-C061 operates from a single -3.3V DC supply, and is housed in a hermetically sealed module with 1.85mm connectors.

Electrical Specifications, T_A = +25°C, -Vdc = Vee = -3.3V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage	±5% Tolerance	-3.46	-3.3	-3.13	V
Power Supply Current			210	240	mA
Maximum Data Rate	NRZ Format	50			Gbps
Maximum Clock Frequency		25			GHz
Minimum Clock Frequency				0.001	GHz
Clock Input Duty Cycle	@ 25 GHz	45		55	%
Data Output Duty Cycle [1]	@ 50 Gbps	45		55	%
Deterministic Jitter [2]			1.5		ps p-p
Additive Random Jitter [3]			0.2		ps rms
Clock Phase Margin	Relative to data period @ 45 Gbps		270		degree

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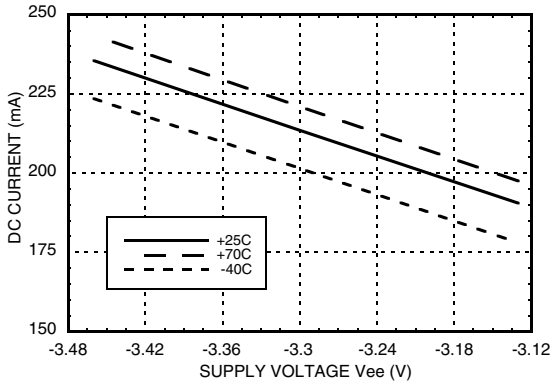
Electrical Specifications, (continued)

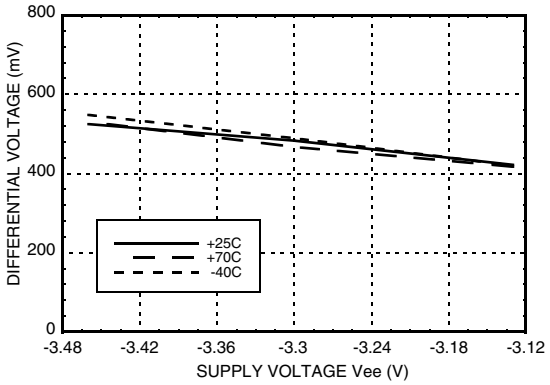
Parameter	Conditions	Min.	Typ.	Max	Units
Rise Time, tr	20% - 80%		8.5		ps
Fall Time, tf	20% - 80%		10		ps
Data Output Swing	Differential Output Swing	420	500		mV p-p
Input Return Loss	Data input up to 25 GHz		10		dB
	Clock input up to 40 GHz		10		dB
Output Return Loss	Data output up to 25 GHz		10		dB
Propagation Delay, td			200		ps
Input Amplitude (Data & Clock)	Single-Ended Amplitude	100		800	mV p-p
	Differential Amplitude	100		2000	mV p-p
Input High Voltage (Data & Clock)		-0.5		0.5	V
Input Low Voltage (Data & Clock)		-1		0	V
Output High Voltage			-10		mV
Output Low Voltage			-300		mV

[1] Data output bit interval variation with respect to ideal bit duration. Valid when clock to data phase margin is within the CPM window.
[2] Deterministic jitter measured at 45 Gbps with PRBS 2^{13}-1 pattern. It is the peak to peak deviation from the ideal time crossing
[3] Random jitter is measured with 45 Gbps 10101… pattern

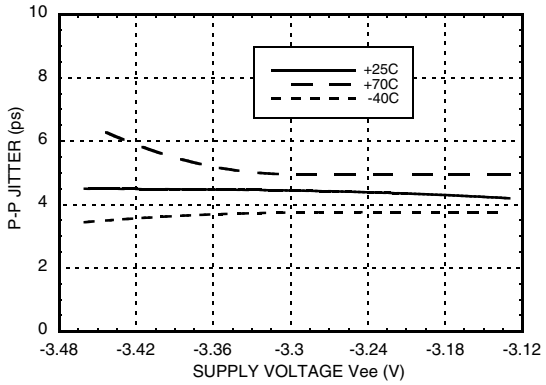
DC Current vs. Supply Voltage



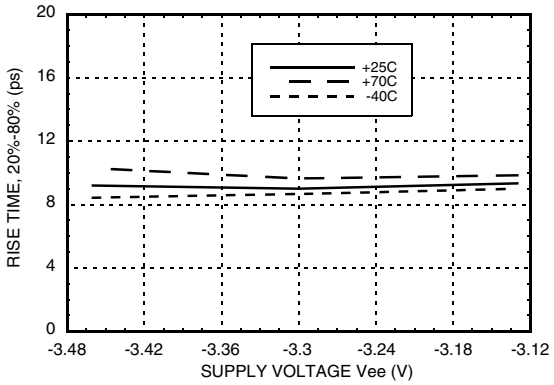
Differential Output vs. Supply Voltage



Peak-to-Peak Jitter vs. Supply Voltage [1] [2]



Rise Time vs. Supply Voltage [1]



[1] Data input = 45Gbps PRBS 2^{23}-1 [2] Source jitter was not deembedded.

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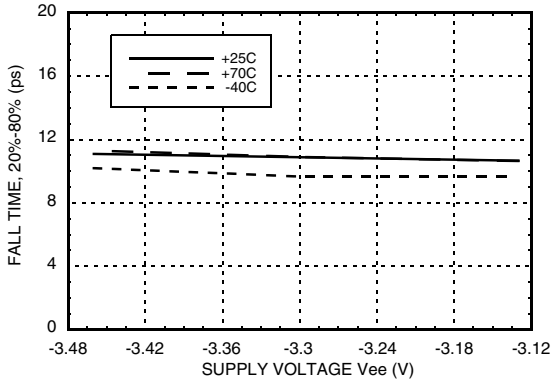
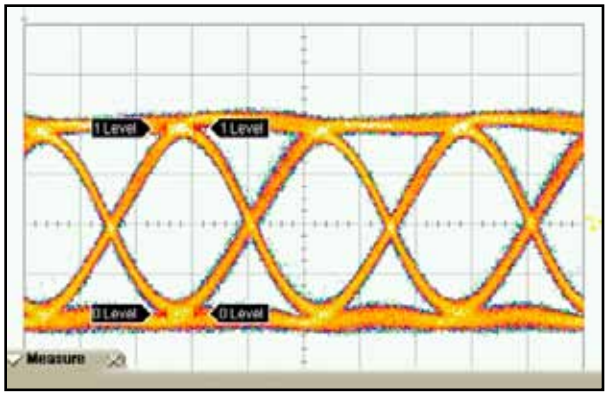
Fall Time vs. Supply Voltage [1]



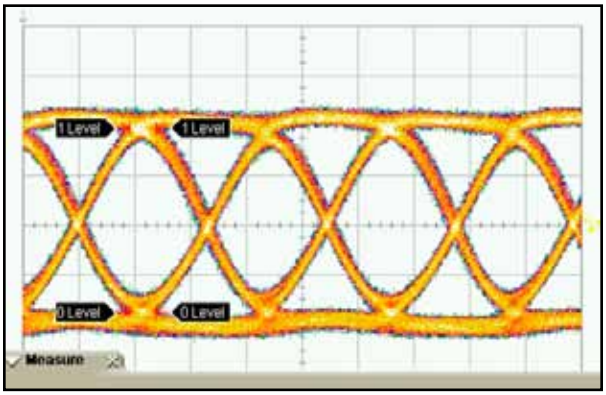
Eye Diagrams



	Current	Minimum	Maximum	Total Meas
Jitter p-p (f1)	3.111 ps	2.889 ps	3.333 ps	30
Rise Time (f1)	12.22 ps	12.00 ps	12.22 ps	30
Fall Time (f1)	10.67 ps	10.44 ps	10.67 ps	30
Differential Eye Ampliftude (f1)	523 mV	522 mV	523 mV	30

Vertical Scale	146 mV / div
Horizontal Scale	10.0 ps / div

[1] Test Conditions:
Eye diagram data presented on an Infinium DCA 86100A
Rate = 40 GB/s
Psuedo Random Code = 2^{23}-1
Vin = 500 mVpp Differential



	Current	Minimum	Maximum	Total Meas
Jitter p-p (f1)	3.333 ps	3.111 ps	3.333 ps	30
Rise Time (f1)	12.00 ps	12.00 ps	12.22 ps	30
Fall Time (f1)	11.11 ps	10.89 ps	11.11 ps	30
Differential Eye Ampliftude (f1)	483 mV	483 mV	484 mV	30

Vertical Scale	131 mV / div
Horizontal Scale	10.0 ps / div

[1] Test Conditions:
Eye diagram data presented on an Infinium DCA 86100A
Rate = 45 GB/s
Psuedo Random Code = 2^{23}-1
Vin = 500 mVpp Differential

[1] Data input = 45Gbps PRBS 2^{23}-1

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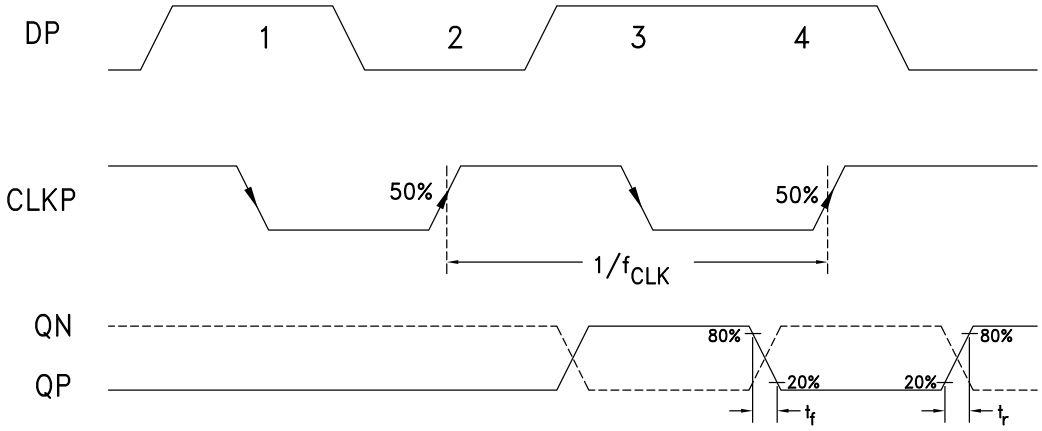
Timing Diagram



Truth Table

Input		Outputs
D	CLK	Q
L	L -> H	L
H	H -> L	H
Notes: D = DP - DN CLK = CLKP - CLKN Q = QP - QN	H - Negative voltage level L - Positive voltage level	

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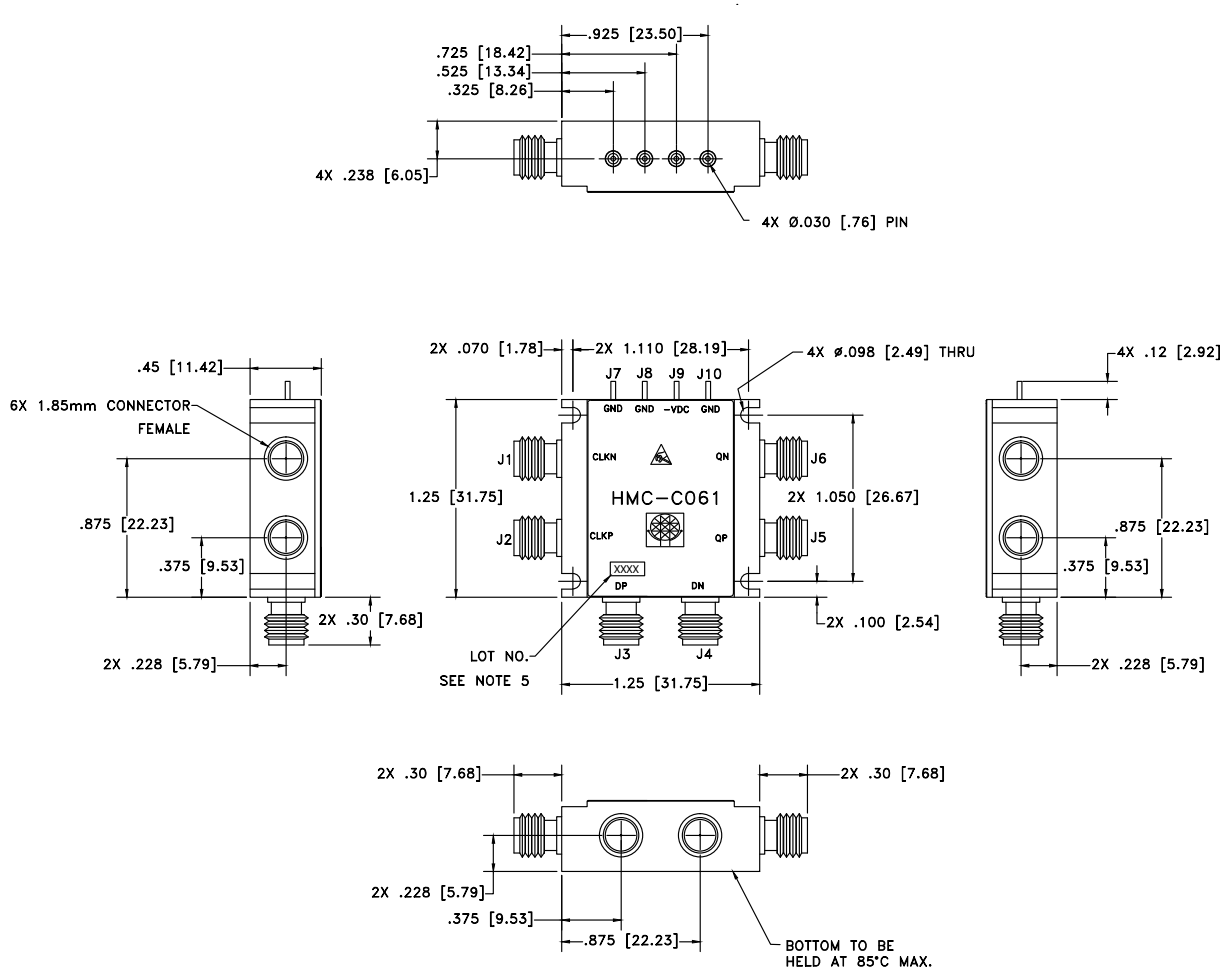
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.6 to +0.5V
Input Signals	-1.5V to +0.5V
Output Signals	-1.5V to +0.5V
Junction Temperature	125°C
Storage Temperature	-65°C to +125°C
Operating Temperature	-40°C to 70°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1 PACKAGE, LEADS, COVER MATERIAL: KOVAR
2 FINISH: GOLD PLATE OVER NICKEL PLATE.
3 ALL DIMENSIONS ARE IN INCHES [MILLIMETERS]
4 TOLERANCES:
4.1 .XX = ± .02
4.2 XXX = ±.010
5 MARK LOT NUMBER ON 0.080 X 0.250 LABEL WHERE SHOWN, WITH 0.030" MIN. TEXT HEIGHT.

Package Information

Package Type	C-13
Package Weight [1]	59.5 gms

[1] Includes the connectors

[2] ±1 gms Tolerance

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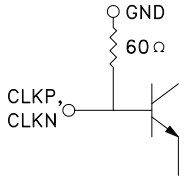
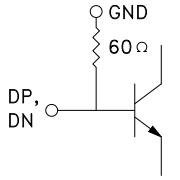
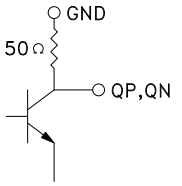
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2	CLKN, CLKP	Differential clock inputs.	
3, 4	DP, DN	Differential data inputs.	
5, 6	QP, QN	Differential data outputs.	
7, 9, 10	GND	Signal and supply ground.	
8	-Vdc (Vee)	Negative Supply	

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