



# PSMN2R2-40YSD

40 V standard level MOSFET

8 July 2019

Preliminary data sheet

## 1. General description

Standard level gate drive N-channel enhancement mode MOSFET.

## 2. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	166	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	1.9	2.2	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	6.1	12	nC
$Q_{G(tot)}$	total gate charge		-	45	63	nC

[1] 120A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 3. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	<p>LFPAK56; Power-SO8 (SOT669)</p>	<p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 4. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R2-40YSD	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 5. Limiting values

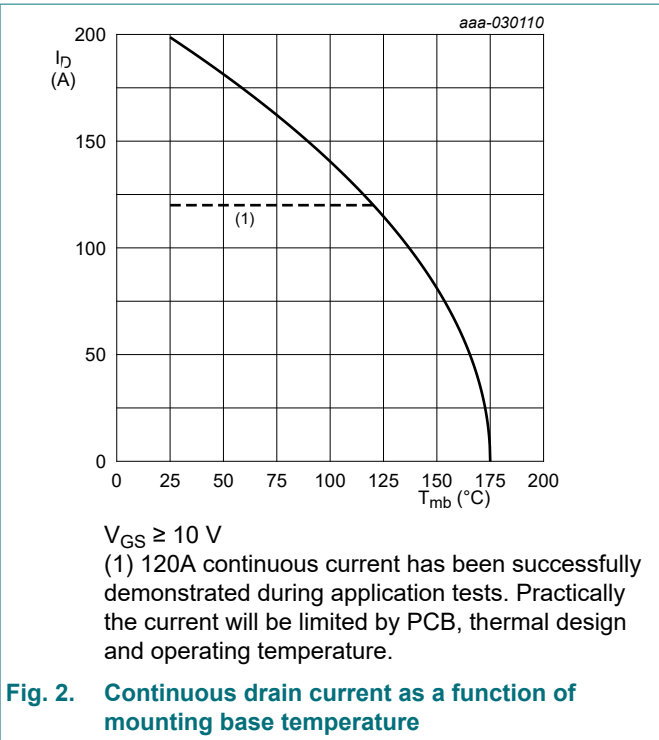
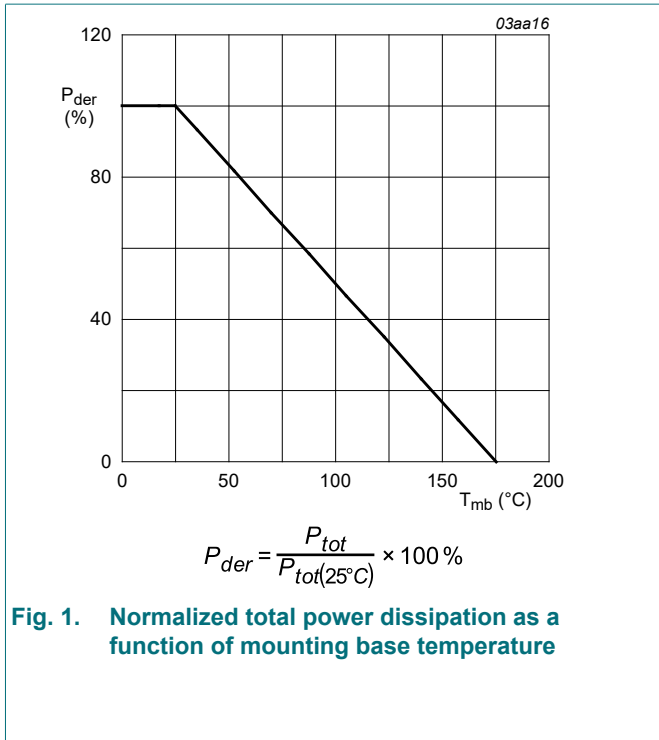
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
$V_{DSM}$	peak drain-source voltage	$t_p \leq 20\text{ ns}$ ; $f \leq 500\text{ kHz}$ ; $E_{DS(AL)} \leq 200\text{ nJ}$ ; pulsed		-	45	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$		-	40	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	166	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	120	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>		-	120	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	795	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
$T_{slid(M)}$	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	120	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	795	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 53.5\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 182\text{ }\mu\text{s}$	[2]	-	253	mJ
		$I_D = 25\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 937\text{ }\mu\text{s}$	[2]	-	609	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} = 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $R_{GS} = 50\text{ }\Omega$	[2]	-	120	A

[1] 120A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

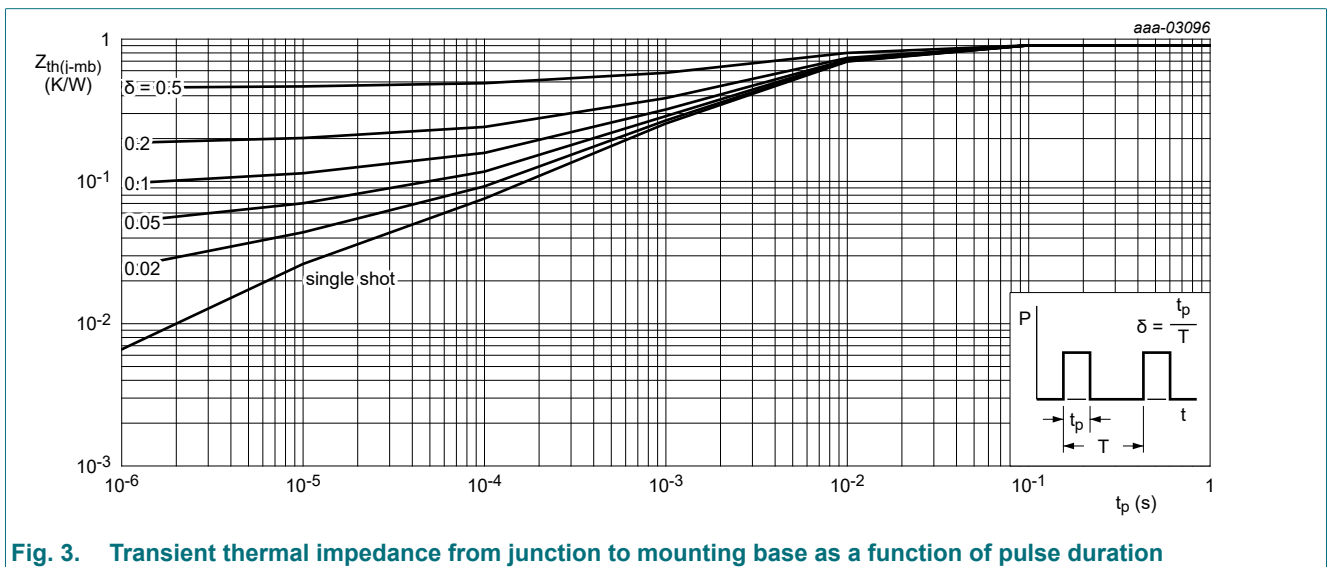
[2] Protected by 100% test

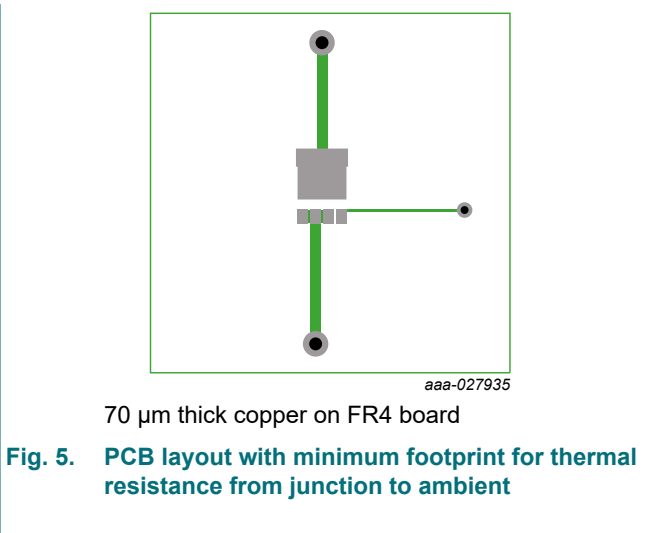
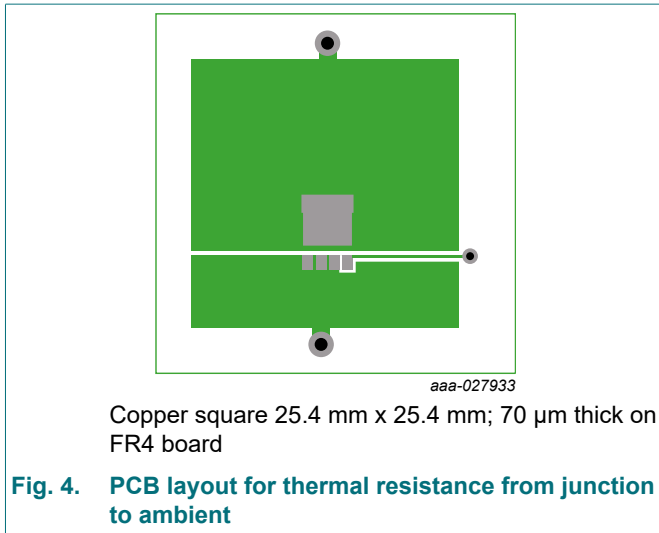


## 6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 3</a>	-	0.8	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 4</a>	-	42	-	K/W
		<a href="#">Fig. 5</a>	-	85	-	K/W





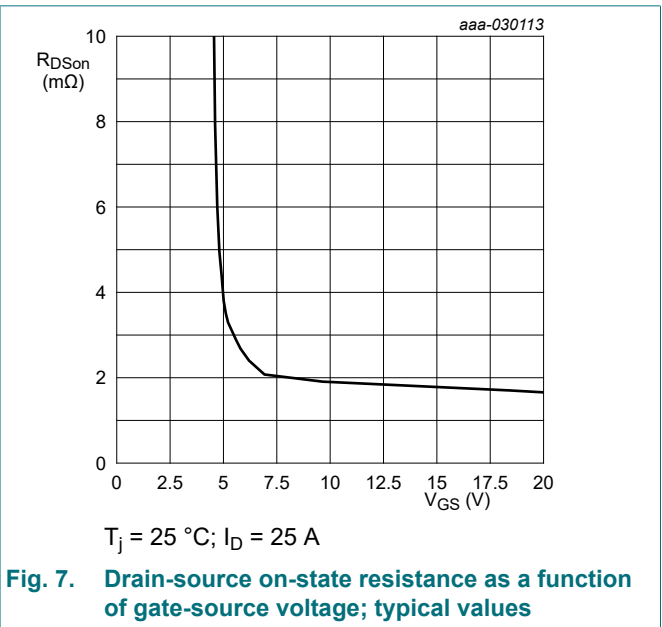
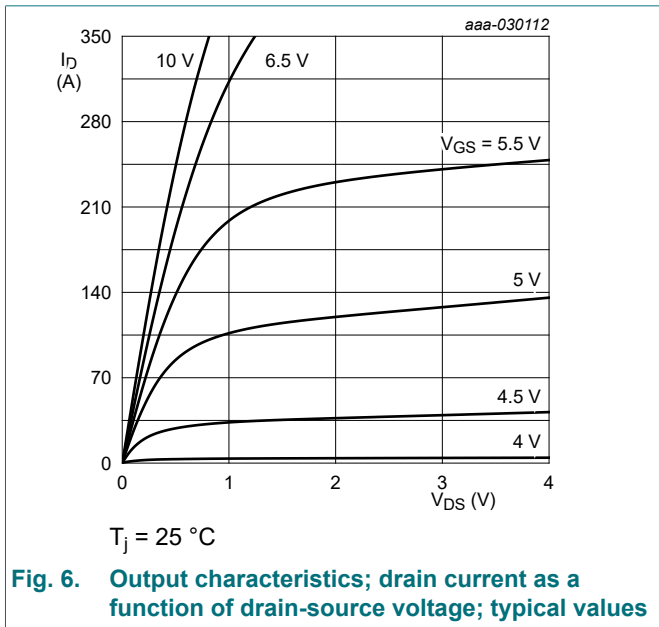
## 7. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	2.4	3	3.6	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-6.3	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	$\mu A$
		$V_{DS} = 32 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	[tbd]	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}$	-	1.9	2.2	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C; \text{ Fig. 10}$	-	-	4.3	m $\Omega$
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.4	0.9	2.3	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	-	45	63	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	[tbd]	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	-	14	21	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	10	15	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.8	7.2	nC
$Q_{GD}$	gate-drain charge		-	6.1	12	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; \text{ Fig. 11}; \text{ Fig. 12}$	-	4.4	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 13</a>	-	3664	5130	pF
$C_{oss}$	output capacitance		-	1068	1495	pF
$C_{rss}$	reverse transfer capacitance		-	193	425	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 0.8\ \Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\ \Omega$	-	13	-	ns
$t_r$	rise time		-	9	-	ns
$t_{d(off)}$	turn-off delay time		-	26	-	ns
$t_f$	fall time		-	10	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	33	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 14</a>	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V};$ <a href="#">Fig. 15</a>	-	29	-	ns
$Q_r$	recovered charge		[1]	21	-	nC
$t_a$	reverse recovery rise time		-	16	-	ns
$t_b$	reverse recovery fall time		-	13	-	ns

[1] includes capacitive recovery



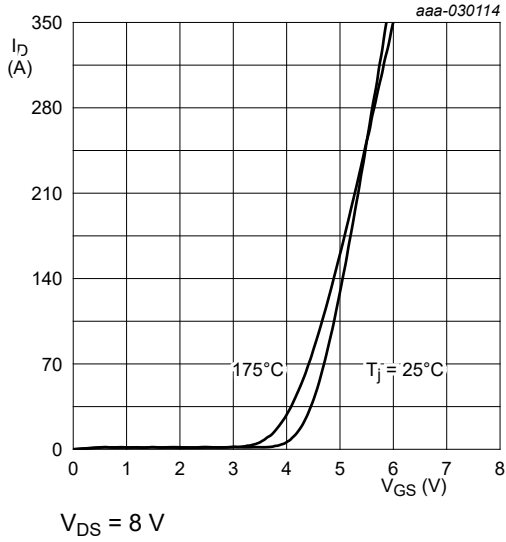


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

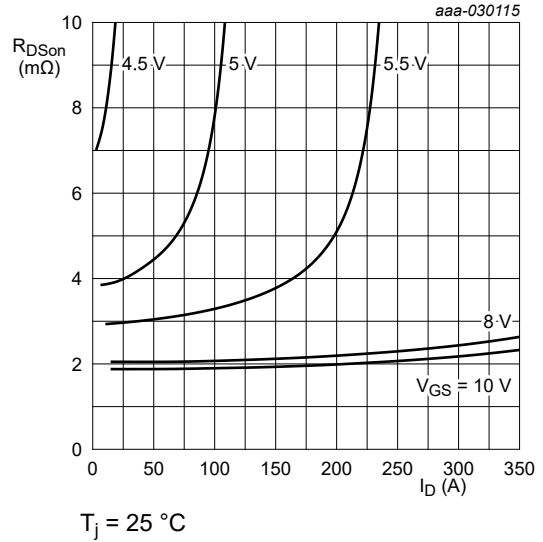


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

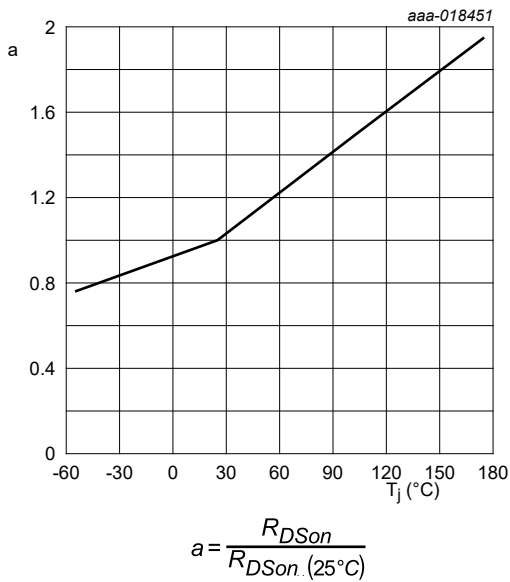


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

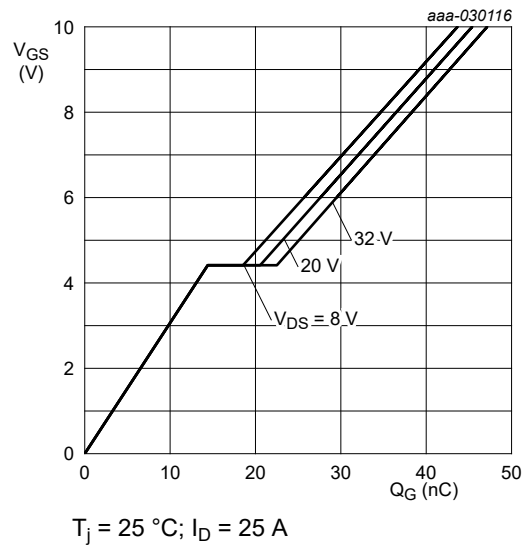


Fig. 11. Gate-source voltage as a function of gate charge; typical values

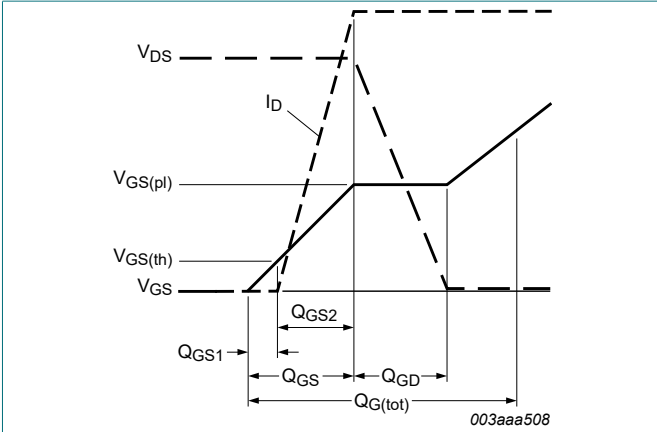
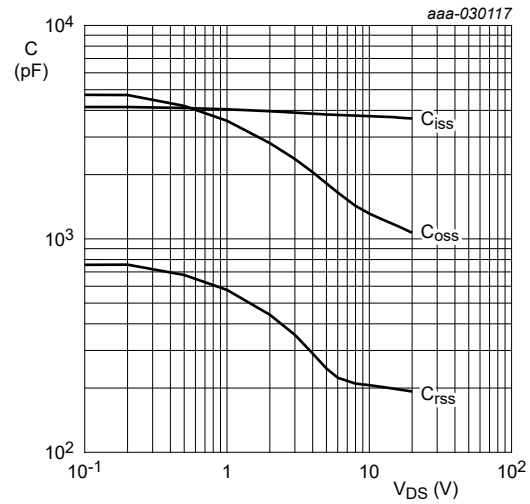
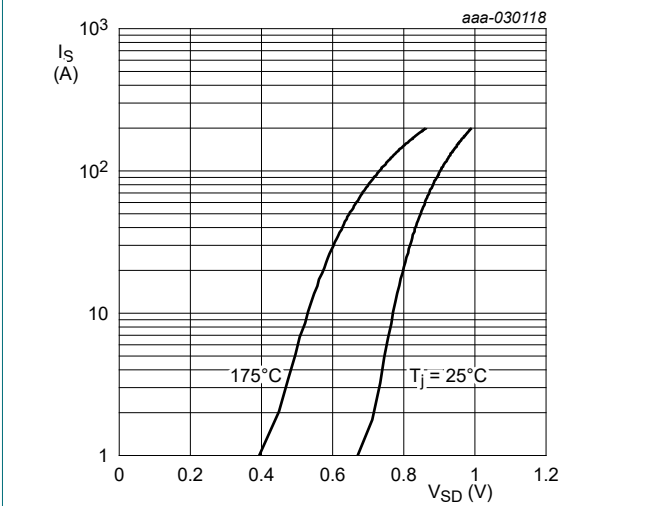


Fig. 12. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

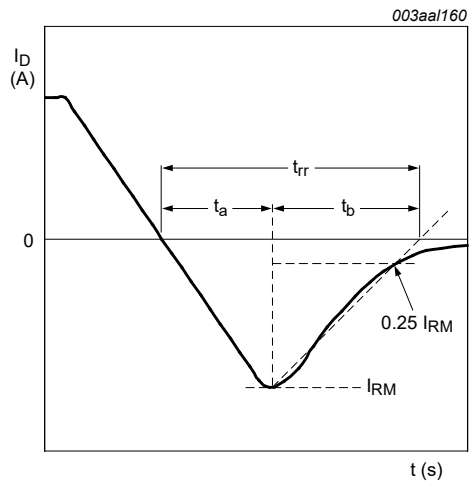


Fig. 15. Reverse recovery timing definition

### 8. Package outline

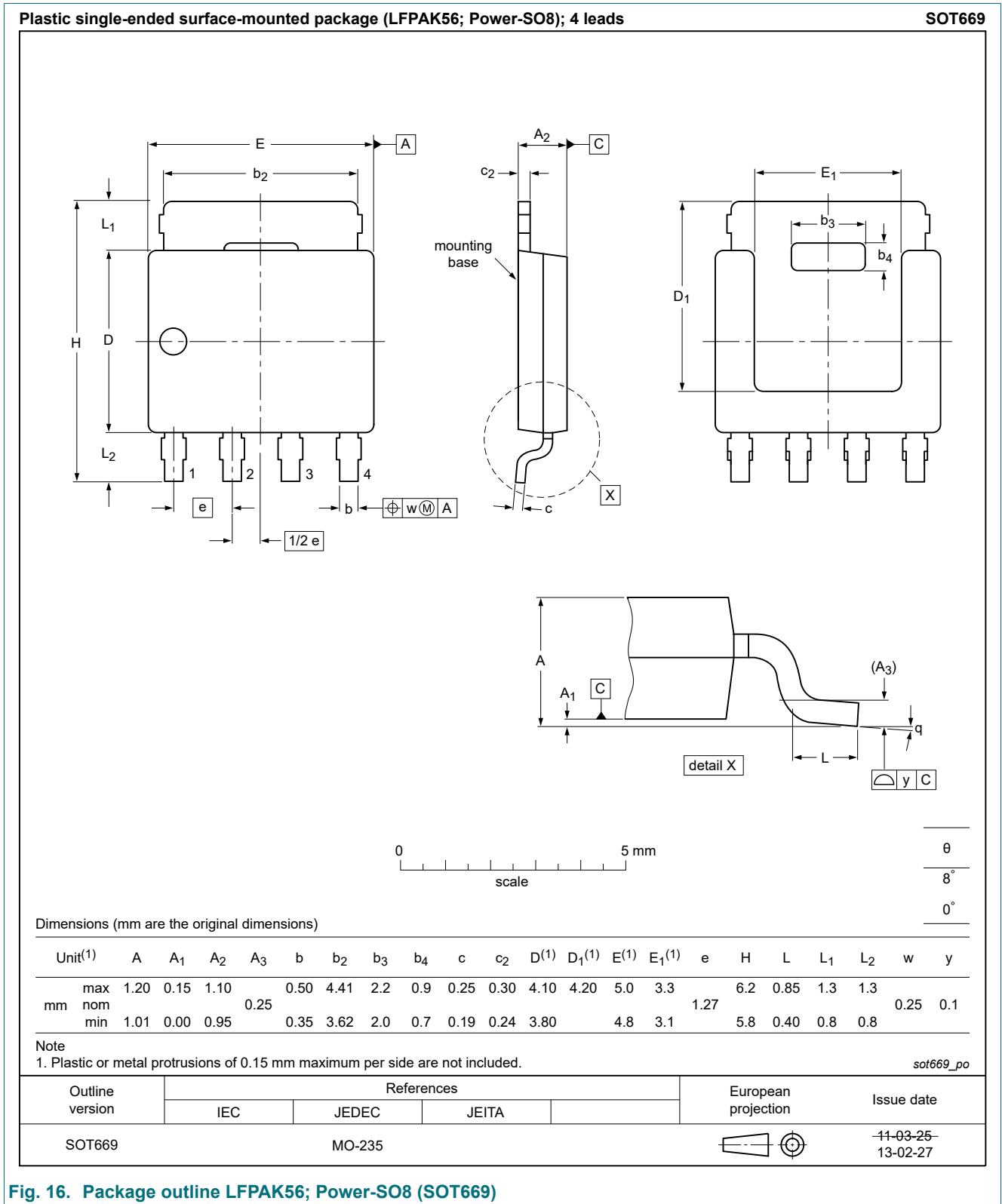


Fig. 16. Package outline LFAK56; Power-SO8 (SOT669)

### 9. Soldering

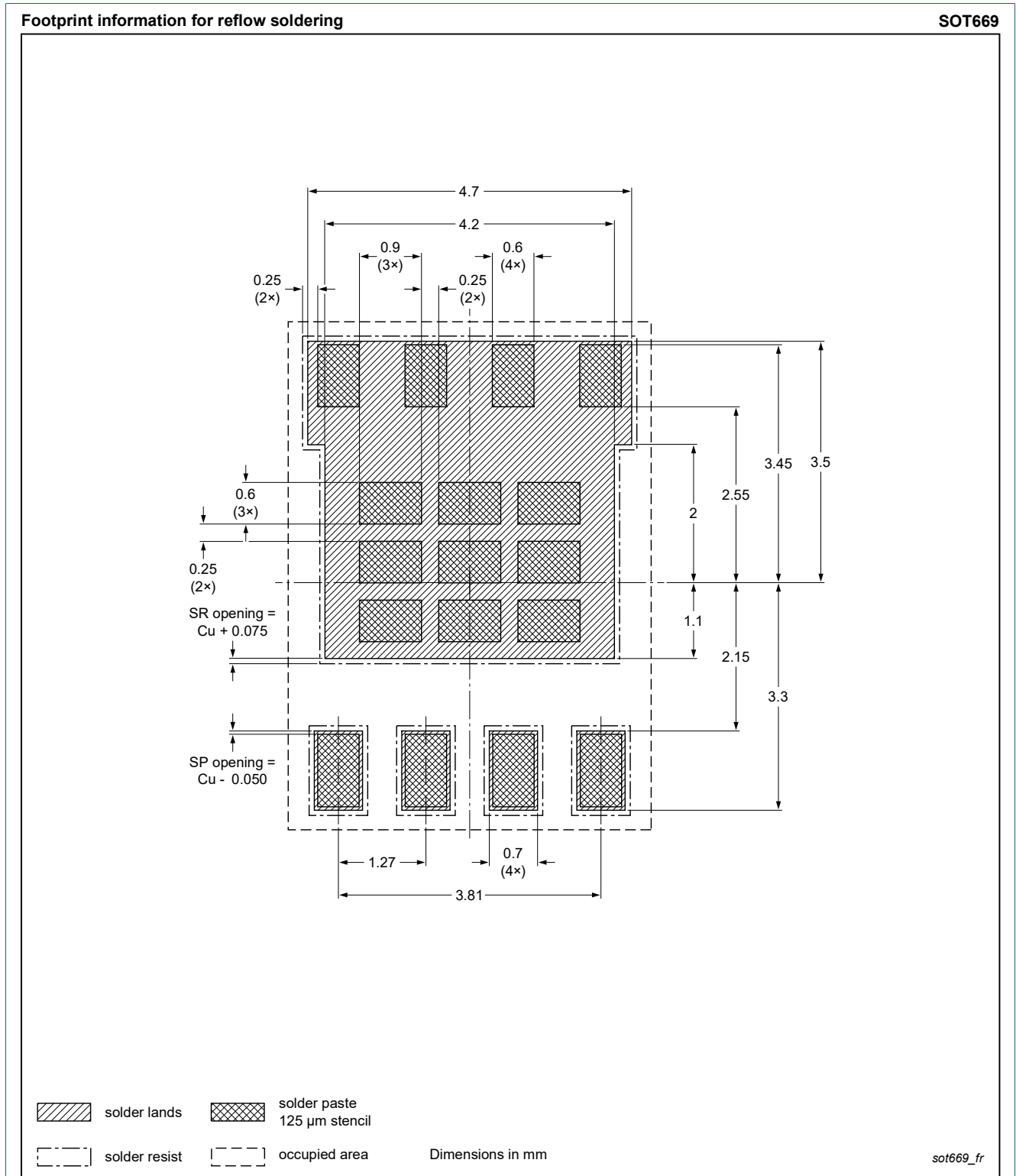
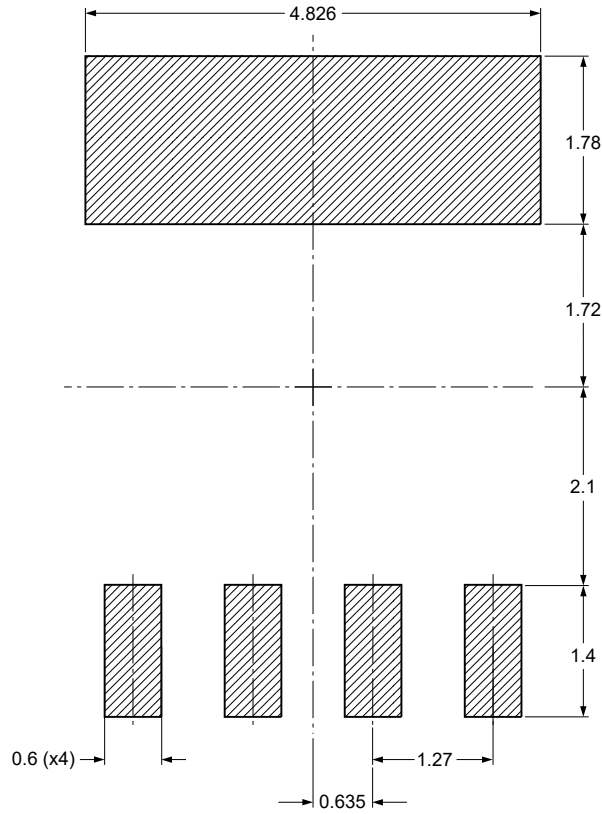


Fig. 17. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package

SOT669



 solder lands

Dimensions in mm

Issue date ~~15-04-13~~  
15-04-16

sot669\_fw

Fig. 18. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

## 10. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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