

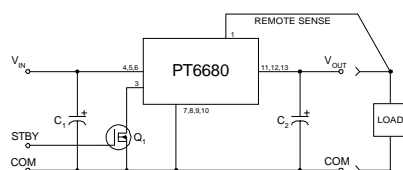
- Single Device: 5A Output
- Input Voltage Range: 18V to 36V
- Adjustable Output Voltage
- 80% Efficiency
- Remote Sense Capability
- Standby Function

trial applications requiring as much as 36V input and 5A of output current, the PT6680 is packaged in a 14-Pin SIP (Single In-line Package) and is available in a surface-mount configuration.

The PT6680 series is a new addition to Power Trends' line of 24V bus Integrated Switching Regulators (ISRs). Designed for general purpose indus-

Only two external capacitors are required for proper operation. Please note that this product does not include short circuit protection.

### Standard Application



$C_1$  = Required 560 $\mu$ F electrolytic (1)  
 $C_2$  = Required 330 $\mu$ F electrolytic  
 $Q_1$  = NFET-or Open Collector Gate

### Pin-Out Information

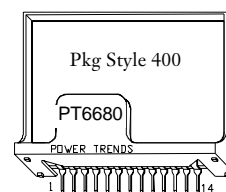
1	Remote Sense
2	Do Not Connect
3	STBY*- Standby
4	$V_{in}$
5	$V_{in}$
6	$V_{in}$
7	GND
8	GND
9	GND
10	GND
11	$V_{out}$
12	$V_{out}$
13	$V_{out}$
14	$V_{out}$ Adjust

### Ordering Information

PT6681	$\square$	= +3.3 Volts
PT6682	$\square$	= +2.5 Volts
PT6683	$\square$	= +5.0 Volts
PT6684	$\square$	= +9.0 Volts
PT6685	$\square$	= +15.0 Volts
PT6686	$\square$	= +12.0 Volts

### PT Series Suffix (PT1234X)

Case/Pin Configuration	Heat Spreader	Heat Spreader with Side Tabs
Vertical Through-Hole	P	R
Horizontal Through-Hole	D	G
Horizontal Surface Mount	E	B



Note: Back surface of product is conducting metal

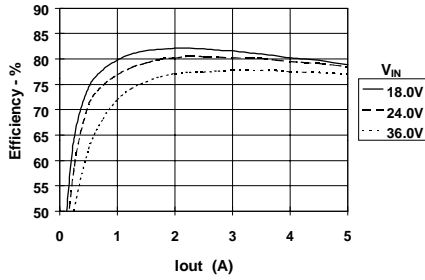
### Specifications

Characteristics ( $T_a = 25^\circ\text{C}$ unless noted)	Symbols	Conditions	PT6680 SERIES			Units	
			Min	Typ	Max		
Output Current	$I_o$	$T_a = 60^\circ\text{C}$ , 200 LFM, pkg P $T_a = 25^\circ\text{C}$ , natural convection	0.1 (2)	—	5.0	A	
Input Voltage Range	$V_{in}$	$0.1\text{A} \leq I_o \leq I_{o\text{max}}$	+18V	—	+36V	V	
Output Voltage Tolerance	$\Delta V_o$	Over $V_{in}$ range $T_a = -40^\circ\text{C}$ to $+65^\circ\text{C}$	$V_o - 0.1$	—	$V_o + 0.1$	V	
Output Voltage Adjust Range	$V_{\text{oadj}}$	Pin 14 to $V_o$ or ground	$V_o = +3.3\text{V}$ $V_o = +2.5\text{V}$ $V_o = +5.0\text{V}$ $V_o = +9.0\text{V}$ $V_o = +12\text{V}$ $V_o = +15\text{V}$	2.2 1.8 3.0 6.0 9.0 10.0	— — — — — —	4.7 4.3 6.5 10.2 13.6 17.0	V
Line Regulation	$\text{Reg}_{\text{line}}$	$+18\text{V} \leq V_{in} \leq +36\text{V}$ , $I_o = I_{o\text{max}}$	—	$\pm 0.5$	$\pm 1.0$	% $V_o$	
Load Regulation	$\text{Reg}_{\text{load}}$	$V_{in} = +28\text{V}$ , $0.1 \leq I_o \leq I_{o\text{max}}$	—	$\pm 0.5$	$\pm 1.0$	% $V_o$	
$V_o$ Ripple/Noise	$V_n$	$V_{in} = +28\text{V}$ , $I_o = I_{o\text{max}}$	—	50 1.0	—	mVpp % $V_o$	
Transient Response with $C_2 = 330\mu\text{F}$	$t_{\text{tr}}$ $V_{\text{os}}$	$I_o$ step between 2.5A and 5.0A $V_o$ over/undershoot	— —	100 100	— —	$\mu\text{Sec}$ mV	
Efficiency	$\eta$	$V_{in} = +28\text{V}$ , $I_o = I_{o\text{max}}$	$V_o = +3.3\text{V}$ $V_o = +2.5\text{V}$ $V_o = +5.0\text{V}$ $V_o = +9.0\text{V}$ $V_o = +12.0\text{V}$ $V_o = +15.0\text{V}$	— — — — — —	78 73 82 87 88 90	— — — — — —	%
Switching Frequency	$f_o$	$+18\text{V} \leq V_{in} \leq +36\text{V}$ Over $I_o$ range	500	550	600	kHz	
Maximum Operating Temperature Range	$T_a$	Over $V_{in}$ range	-40	—	+85 (3)	$^\circ\text{C}$	
Storage Temperature	$T_s$	—	-40	—	+125	$^\circ\text{C}$	
Mechanical Shock	—	Per Mil-STD-883D, Method 2002.3	—	500	—	G's	
Mechanical Vibration	—	Per Mil-STD-883D, Method 2007.2, 20-2000 Hz, soldered in a PC board	—	7.5	—	G's	
Weight	—	—	—	14	—	grams	

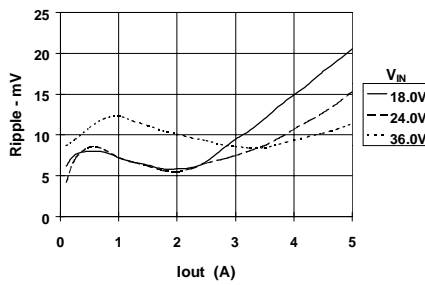
**Notes** (1) The 560 $\mu$ F electrolytic input capacitor must be rated for 1.5Arms ripple current. Both an input and output capacitor is required for proper operation.  
 (2) The ISR will operate down to no load with reduced specifications.  
 (3) Consult the SOA curves or contact the factory to determine the appropriate derating.

PT6681,  $V_{out} = 3.3V$  (Note A)

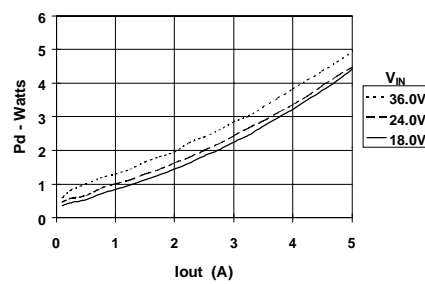
Efficiency vs Output Current



Ripple vs Output Current



Power Dissipation vs Output Current



Note A: Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical for the ISR.  
 Note B: SOA curves represent conditions at which internal components are at or below manufacturer's maximum operating temperatures.

## Adjusting the Output Voltage of the PT6680 5Amp 18-36V Bus Converter Series

The output voltage of the Power Trends PT6680 Series ISRs may be adjusted higher or lower than the factory trimmed pre-set voltage with the addition of a single external resistor<sup>1</sup>. Table 1 gives the respective allowable adjustment range for each model in the series as  $V_a$  (min) and  $V_a$  (max).

**Adjust Up:** An increase in the output voltage is obtained by adding a resistor R2, between pin 14 ( $V_o$  adjust) and pins 7-10 (GND).

**Adjust Down:** Add a resistor (R1), between pin 14 ( $V_o$  adjust) and pins 11-13 ( $V_{out}$ ).

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor, either (R1) or R2 as appropriate.

### Notes:

1. Use only a single 1% resistor in either the (R1) or R2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from  $V_o$  adjust to either GND,  $V_{out}$ , or the Remote Sense pin. Any capacitance added to the  $V_o$  adjust pin will affect the stability of the ISR.
3. If the Remote Sense feature is being used, connecting the resistor (R1) between pin 14 ( $V_o$  adjust) and pin 1 (Remote Sense) can benefit load regulation.
4. For output voltages above 10.0Vdc, the maximum output current must be limited to 4Adc.
5. Adjustments to the output voltage may place additional limits on the input voltage for the part. The revised limits must comply with the following requirements.

$$V_{in} \text{ (min)} = (V_{out} + 3)V \text{ or } 18V, \text{ whichever is higher.}$$

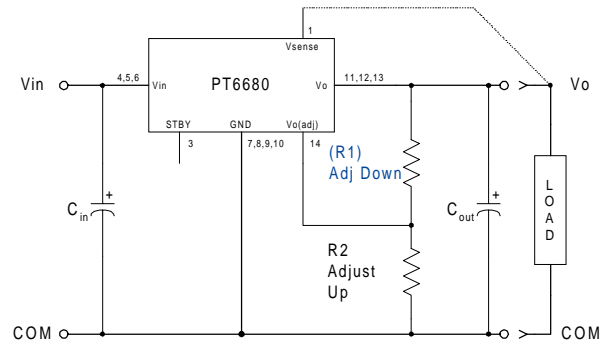
$$V_{in} \text{ (max)} = (10 \times V_{out})V \text{ or } 36V, \text{ whichever is less.}$$

**Table 1**

**PT6680 ADJUSTMENT AND FORMULA PARAMETERS**

Series Pt #	PT6682	PT6681	PT6683	PT6684	PT6686	PT6685
$V_o$ (nom)	2.5V	3.3V	5.0V	9.0V	12.0V	15.0V
$V_a$ (min)	1.8V	2.2V	3.0V	6.0V	9.0V	10.0V
$V_a$ (max)	4.3V	4.7V	6.5V	10.2V	13.6V	17.0V
$R_o$ (k $\Omega$ )	4.99	4.22	2.49	2.0	2.0	2.0
$R_s$ (k $\Omega$ )	2.49	4.99	4.99	12.7	12.7	12.7

**Figure 1**



The values of (R1) [adjust down], and R2 [adjust up], can also be calculated using the following formulae.

$$(R1) = \frac{R_o (V_o - 1.25)(V_a - 1.25)}{1.25 (V_o - V_a)} - R_s \quad k\Omega$$

$$R2 = \frac{R_o (V_o - 1.25)}{V_a - V_o} - R_s \quad k\Omega$$

Where:  $V_o$  = Original output voltage  
 $V_a$  = Adjusted output voltage  
 $R_o$  = The resistance value in Table 1  
 $R_s$  = The series resistance from Table 1

PT6680 Series

Table 2

PT6680 ADJUSTMENT RESISTOR VALUES

Series Pt #	PT6682	PT6681	PT6683	Series Pt #	PT6684	PT6686	PT6685
Current	5Adc	5Adc	5Adc	Current	5Adc	4Adc	4Adc
V <sub>o</sub> (nom)	2.5Vdc	3.3Vdc	5.0Vdc	V <sub>o</sub> (nom)	9.0Vdc	12.0Vdc	15.0Vdc
V <sub>a</sub> (req'd)				V <sub>a</sub> (req'd)			
1.8	(1.4)kΩ			6.0	(6.9)kΩ		
1.9	(2.9)kΩ			6.2	(9.2)kΩ		
2.0	(5.0)kΩ			6.4	(11.9)kΩ		
2.1	(8.1)kΩ			6.6	(14.0)kΩ		
2.2	(13.3)kΩ	(1.0)kΩ		6.8	(18.6)kΩ		
2.3	(23.7)kΩ	(2.3)kΩ		7.0	(23.0)kΩ		
2.4	(54.9)kΩ	(3.9)kΩ		7.2	(28.3)kΩ		
2.5		(5.8)kΩ		7.4	(35.0)kΩ		
2.6	59.9kΩ	(8.4)kΩ		7.6	(43.5)kΩ		
2.7	28.7kΩ	(11.7)kΩ		7.8	(55.0)kΩ		
2.8	18.3kΩ	(16.5)kΩ		8.0	(71.0)kΩ		
2.9	13.1kΩ	(23.6)kΩ		8.2	(95.0)kΩ		
3.0	10.0kΩ	(35.4)kΩ	(1.6)kΩ	8.4	(135.0)kΩ		
3.1	7.9kΩ	(59.0)kΩ	(2.3)kΩ	8.6	(215.0)kΩ		
3.2	6.4kΩ	(130.0)kΩ	(3.1)kΩ	8.8	(455.0)kΩ		
3.3	5.3kΩ		(4.0)kΩ	9.0		(31.7)kΩ	
3.4	4.4kΩ	81.5kΩ	(5.1)kΩ	9.2	64.8kΩ	(36.1)kΩ	
3.5	3.8kΩ	38.3kΩ	(6.2)kΩ	9.4	26.1kΩ	(41.2)kΩ	
3.6	3.2kΩ	23.8kΩ	(7.6)kΩ	9.6	13.1kΩ	(47.1)kΩ	
3.7	2.7kΩ	16.6kΩ	(9.1)kΩ	9.8	6.7kΩ	(54.1)kΩ	
3.8	2.3kΩ	12.3kΩ	(10.9)kΩ	10.0	2.8kΩ	(62.6)kΩ	(25.8)kΩ
3.9	2.0kΩ	9.4kΩ	(13.0)kΩ	10.2	0.2kΩ	(72.8)kΩ	(28.3)kΩ
4.0	1.7kΩ	7.4kΩ	(15.6)kΩ	10.4		(85.7)kΩ	(31.1)kΩ
4.1	1.4kΩ	5.8kΩ	(18.7)kΩ	10.6		(102.0)kΩ	(34.1)kΩ
4.2	1.2kΩ	4.6kΩ	(22.6)kΩ	10.8		(124.0)kΩ	(37.3)kΩ
4.3	1.0kΩ	3.7kΩ	(27.6)kΩ	11.0		(155.0)kΩ	(40.9)kΩ
4.4		2.9kΩ	(34.2)kΩ	11.2		(201.0)kΩ	(44.9)kΩ
4.5		2.2kΩ	(43.6)kΩ	11.4		(278.0)kΩ	(49.3)kΩ
4.6		1.7kΩ	(57.6)kΩ	11.6		(432.0)kΩ	(54.3)kΩ
4.7		1.2kΩ	(80.9)kΩ	11.8		(895.0)kΩ	(59.8)kΩ
4.8			(128.0)kΩ	12.0			(66.1)kΩ
4.9			(268.0)kΩ	12.2		94.8kΩ	(73.3)kΩ
5.0				12.4		41.1kΩ	(81.6)kΩ
5.1			88.4kΩ	12.6		23.1kΩ	(91.3)kΩ
5.2			41.7kΩ	12.8		14.2kΩ	(103.0)kΩ
5.3			26.1kΩ	13.0		8.8kΩ	(117.0)kΩ
5.4			18.4kΩ	13.2		5.2kΩ	(133.0)kΩ
5.5			13.7kΩ	13.4		2.7kΩ	(154.0)kΩ
5.6			10.6kΩ	13.6		0.7kΩ	(181.0)kΩ
5.7			8.4kΩ	13.8			(217.0)kΩ
5.8			6.7kΩ	14.0			(268.0)kΩ
5.9			5.4kΩ	14.2			(343.0)kΩ
6.0			4.4kΩ	14.5			(570.0)kΩ
6.1			3.5kΩ	15.0			
6.2			2.8kΩ	15.5			42.3kΩ
6.3			2.2kΩ	16.0			14.8kΩ
6.4			1.7kΩ	16.5			5.6kΩ
6.5			1.2kΩ	17.0			1.1kΩ

R1 = (Blue) R2 = Black

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PT6681B	OBSOLETE	SIP MODULE	EEK	14		TBD	Call TI	Call TI	-40 to 85		
PT6683P	OBSOLETE	SIP MODULE	EED	14		TBD	Call TI	Call TI	-40 to 85		
PT6685R	OBSOLETE	SIP MODULE	EEE	14		TBD	Call TI	Call TI	-40 to 85		
PT6686B	OBSOLETE	SIP MODULE	EEK	14		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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