

# CC3235S and CC3235SF SimpleLink™ Wi-Fi®, Dual-Band, Single-Chip Solution

## 1 Features

- Multiple-core architecture, system-on-chip (SoC)
- 802.11 a/b/g/n: 2.4GHz and 5GHz
- FIPS 140-2 Level 1 Certification
- Multilayered security features, help developers protect identities, data, and software IP
- Low-Power Modes for battery powered application
- Coexistence with 2.4GHz radios
- Industrial temperature: –40°C to +85°C
- Wi-Fi CERTIFIED® by the Wi-Fi Alliance®
- Application microcontroller subsystem:
  - Arm® Cortex®-M4 core at 80MHz
  - User-dedicated memory
    - 256KB RAM
    - Optional 1MB executable Flash
  - Rich set of peripherals and timers
  - 27 I/O pins with flexible multiplexing options
    - UART, I2S, I2C, SPI, SD, ADC, 8-bit parallel interface
    - Timers and PWM
- **Wi-Fi network processor subsystem:**
  - Wi-Fi® core:
    - 802.11 a/b/g/n 2.4GHz and 5GHz
    - Modes:
      - Access Point (AP)
      - Station (STA)
      - Wi-Fi Direct® (only supported on 2.4GHz)
    - Security:
      - WEP
      - WPA™/ WPA2™ PSK
      - WPA2 Enterprise
      - WPA3™ Personal
      - WPA3™ Enterprise
  - Internet and application protocols:
    - HTTPs server, mDNS, DNS-SD, DHCP
    - IPv4 and IPv6 TCP/IP stack
    - 16 BSD sockets (fully secured TLS v1.2 and SSL 3.0)
  - Built-in power management subsystem:
    - Configurable low-power profiles (always, intermittent, tag)
    - Advanced low-power modes
    - Integrated DC/DC regulators
- **Multilayered security features:**
  - Separate execution environments
  - Networking security
  - Device identity and key
  - Hardware accelerator cryptographic engines (AES, DES, SHA/MD5, CRC)
  - Application-level security (encryption, authentication, access control)
  - Initial secure programming
  - Software tamper detection
  - Secure boot
  - Certificate signing request (CSR)
  - Unique per device key pair
- Application throughput:
  - UDP: 16Mbps, TCP: 13 Mbps
  - Peak: 72Mbps
- **Power-Management Subsystem:**
  - Integrated DC/DC converters support a wide range of supply voltage:
    - VBAT wide-voltage mode: 2.1V to 3.6V
    - VIO is always tied with VBAT
  - Advanced low-power modes:
    - Shutdown: 1µA, hibernate: 4.5µA
    - Low-power deep sleep (LPDS): 120µA
    - Idle connected (MCU in LPDS): 710µA
    - RX traffic (MCU active): 59mA
    - TX traffic (MCU active): 223mA
- Wi-Fi TX power:
  - 2.4GHz: 18.0dBm at 1 DSSS
  - 5GHz: 18.1dBm at 6 OFDM
- Wi-Fi RX sensitivity:
  - 2.4GHz: –96dBm at 1 DSSS
  - 5GHz: –92dBm at 6 OFDM
- Clock source:
  - 40.0MHz crystal with internal oscillator
  - 32.768kHz crystal or external RTC
- RGK package
  - 64-pin, 9mm × 9mm very thin quad flat nonlead (VQFN) package, 0.5mm pitch
- Device supports **SimpleLink™ MCU Platform Developer's Ecosystem**



## 2 Applications

- For Internet of Things applications, such as:
  - [Building and home automation](#):
    - [HVAC systems and thermostat](#)
    - [Video surveillance, video doorbells, and low-power camera](#)
    - [Building security systems and E-locks](#)
  - [Appliances](#)
  - [Asset tracking](#)
  - [Factory automation](#)
  - [Medical and healthcare](#)
  - [Grid infrastructure](#)

## 3 Description

The dual-band wireless MCU CC3235x device comes in two variants, CC3235S and C3235SF.

- The [CC3235S](#) includes 256KB of RAM, IoT networking security, device identity/keys, as well as, MCU level security features such as file system encryption, user IP (MCU image) encryption, secure boot, and debug security.
- The [CC3235SF](#) builds on the CC3235S and integrates a user-dedicated 1MB of executable flash in addition to the 256KB of RAM.

Simplify your IoT design with a Wi-Fi CERTIFIED™ wireless microcontroller (MCU). The [SimpleLink™ Wi-Fi®](#) CC3235x device family is a dual-band system-on-chip (SoC) solution that integrates two processors within a single chip, including:

- Application processor: Arm® Cortex®-M4 MCU with a user-dedicated 256KB of RAM and an optional 1MB of executable flash
- Network processor to run all Wi-Fi and internet logical layers. This ROM-based subsystem completely offloads the host MCU and includes an 802.11 a/b/g/n dual-band 2.4GHz and 5GHz radio, baseband, and MAC with a powerful hardware cryptography engine

These devices introduce new capabilities that further simplify the connectivity of things to the Internet. The main new features include:

- 802.11a (5GHz) support
- BLE/2.4GHz radio coexistence
- Antenna selection
- Enhanced security with [FIPS](#) 140-2 Level 1 certification and more <sup>1</sup>
- Up to 16 concurrent secure sockets
- Certificate sign request (CSR)
- Online certificate status protocol (OCSP)
- Wi-Fi® Alliance certified IoT power-saving features (such as DMS, proxy ARP, and so forth)
- Hostless mode for offloading template packet transmissions
- Improved fast scan

The CC3235x device family is part of the SimpleLink™ MCU platform—a common, easy-to-use development environment based on a single-core software development kit (SDK) with a rich tool set and reference designs. The E2E™ community supports Wi-Fi®, Bluetooth® low energy, Sub-1GHz, and host MCUs. For more information, visit [www.ti.com/simplelink](http://www.ti.com/simplelink) or [www.ti.com/simplelinkwifi](http://www.ti.com/simplelinkwifi).

### Device Information <sup>(1)</sup>

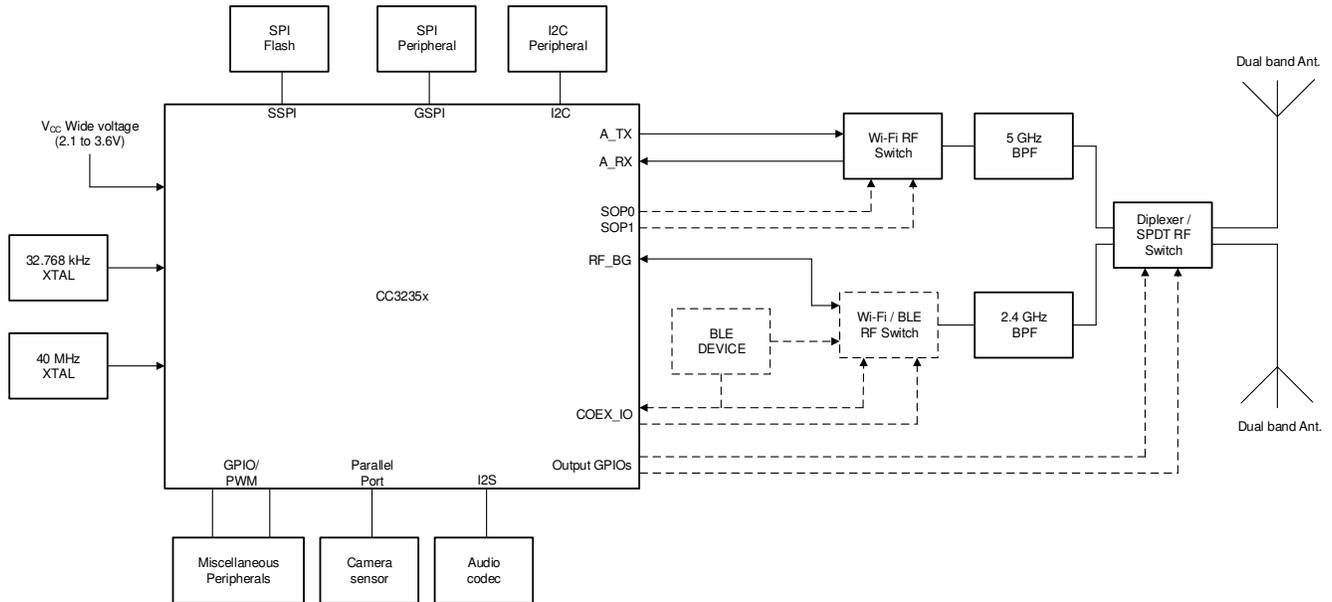
| PART NUMBER    | PACKAGE   | PACKAGE SIZE    |
|----------------|-----------|-----------------|
| CC3235SM2RGKR  | VQFN (64) | 9.00mm × 9.00mm |
| CC3235SF12RGKR | VQFN (64) | 9.00mm × 9.00mm |

(1) For more information, see [Section 12](#).

<sup>1</sup> For exact status of FIPS certification for a specific part number, please refer to <https://csrc.nist.gov/publications/fips>.

## 4 Functional Block Diagrams

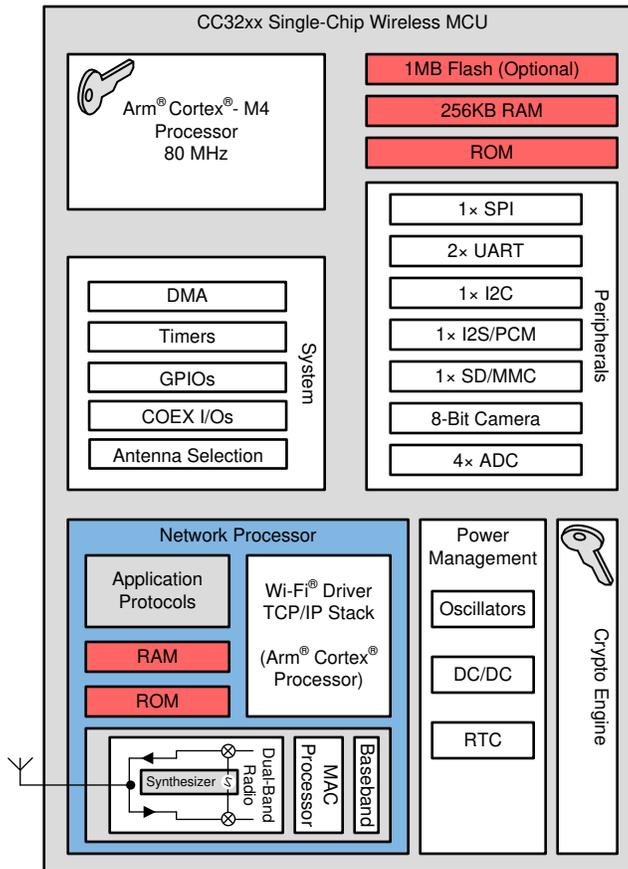
Figure 4-1 shows the functional block diagram of the CC3235x SimpleLink™ Wi-Fi® solution.



Note: The diplexer is used for the signal antenna solution. When using the antenna selection feature (dual antenna), an SPDT switch and two GPIO lines are required after the diplexer.

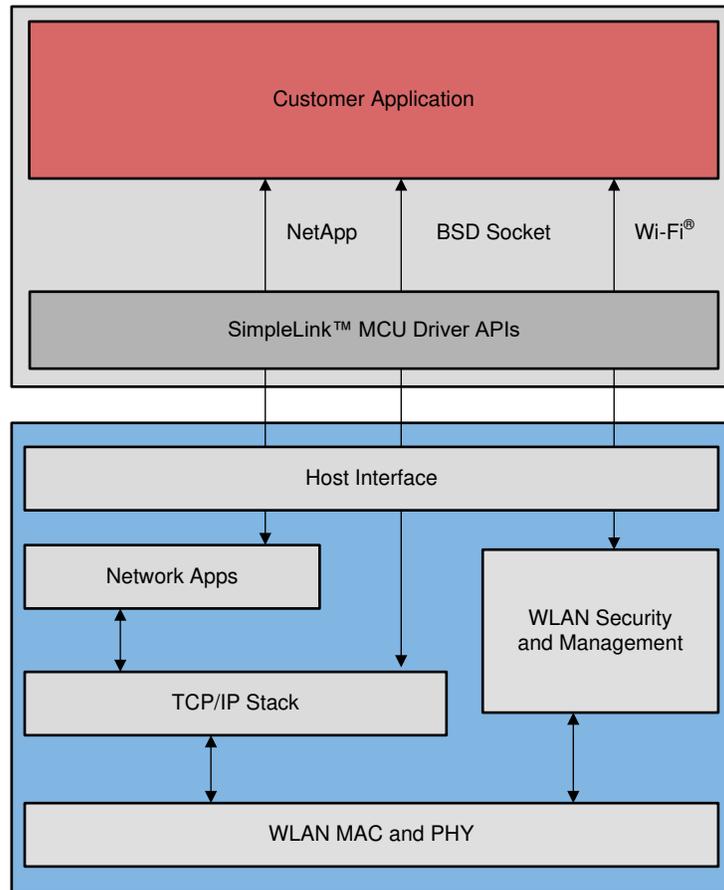
**Figure 4-1. Functional Block Diagram**

Figure 4-2 shows the hardware overview for the CC3235x device.



**Figure 4-2. CC3235x Hardware Overview**

Figure 4-3 shows an overview of the embedded software in the CC3235x device.



**Figure 4-3. CC3235x Embedded Software Overview**

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## 5 Device Comparison

Table 5-1 lists the features supported across different CC3x35 devices.

**Table 5-1. Comparison of Device Features**

| FEATURE   | DEVICE  |   |   |
|---|---|---|---|
|   | CC3135  | CC3235S   | CC3235SF  |
| Classification                                  | Network processor   | Wireless microcontroller  | Wireless microcontroller  |
| Standard  | 802.11a/b/g/n   | 802.11a/b/g/n   | 802.11a/b/g/n   |
| TCP/IP stack                                    | IPv4, IPv6  | IPv4, IPv6  | IPv4, IPv6  |
| Sockets   | 16  | 16  | 16  |
| Package   | 9mm × 9mm VQFN  | 9mm × 9mm VQFN  | 9mm × 9mm VQFN  |
| <b>ON-CHIP APPLICATION MEMORY</b>               |   |   |   |
| Flash   | —   | —   | 1MB   |
| RAM   | —   | 256KB   | 256KB   |
| <b>RF FEATURES</b>                              |   |   |   |
| Frequency                                       | 2.4GHz, 5GHz  | 2.4GHz, 5GHz  | 2.4GHz, 5GHz  |
| Coexistence with BLE Radio                      | Yes   | Yes   | Yes   |
| <b>SECURITY FEATURES</b>                        |   |   |   |
| Additional networking security                  | Unique device identity<br>Trusted root-certificate catalog<br>TI Root-of-trust public key<br>Online certificate status protocol (OCSP)<br>Certificate signing request (CSR)<br>Unique per-device key pair | Unique device identity<br>Trusted root-certificate catalog<br>TI Root-of-trust public key<br>Online certificate status protocol (OCSP)<br>Certificate signing request (CSR)<br>Unique per-device key pair | Unique device identity<br>Trusted root-certificate catalog<br>TI Root-of-trust public key<br>Online certificate status protocol (OCSP)<br>Certificate signing request (CSR)<br>Unique per-device key pair |
| Hardware acceleration                           | Hardware crypto engines   | Hardware crypto engines   | Hardware crypto engines   |
| Secure boot                                     | —   | Yes   | Yes   |
| Enhanced application level security             | —   | File system security<br>Secure key storage<br>Software tamper detection<br>Cloning protection<br>Initial secure programming   | File system security<br>Secure key storage<br>Software tamper detection<br>Cloning protection<br>Initial secure programming   |
| FIPS 140-2 Level 1 Certification <sup>(1)</sup> | Yes   | Yes   | Yes   |

(1) For exact status of FIPS certification for a specific part number, please refer to <https://csrc.nist.gov/publications/fips>.

## 5.1 Related Products

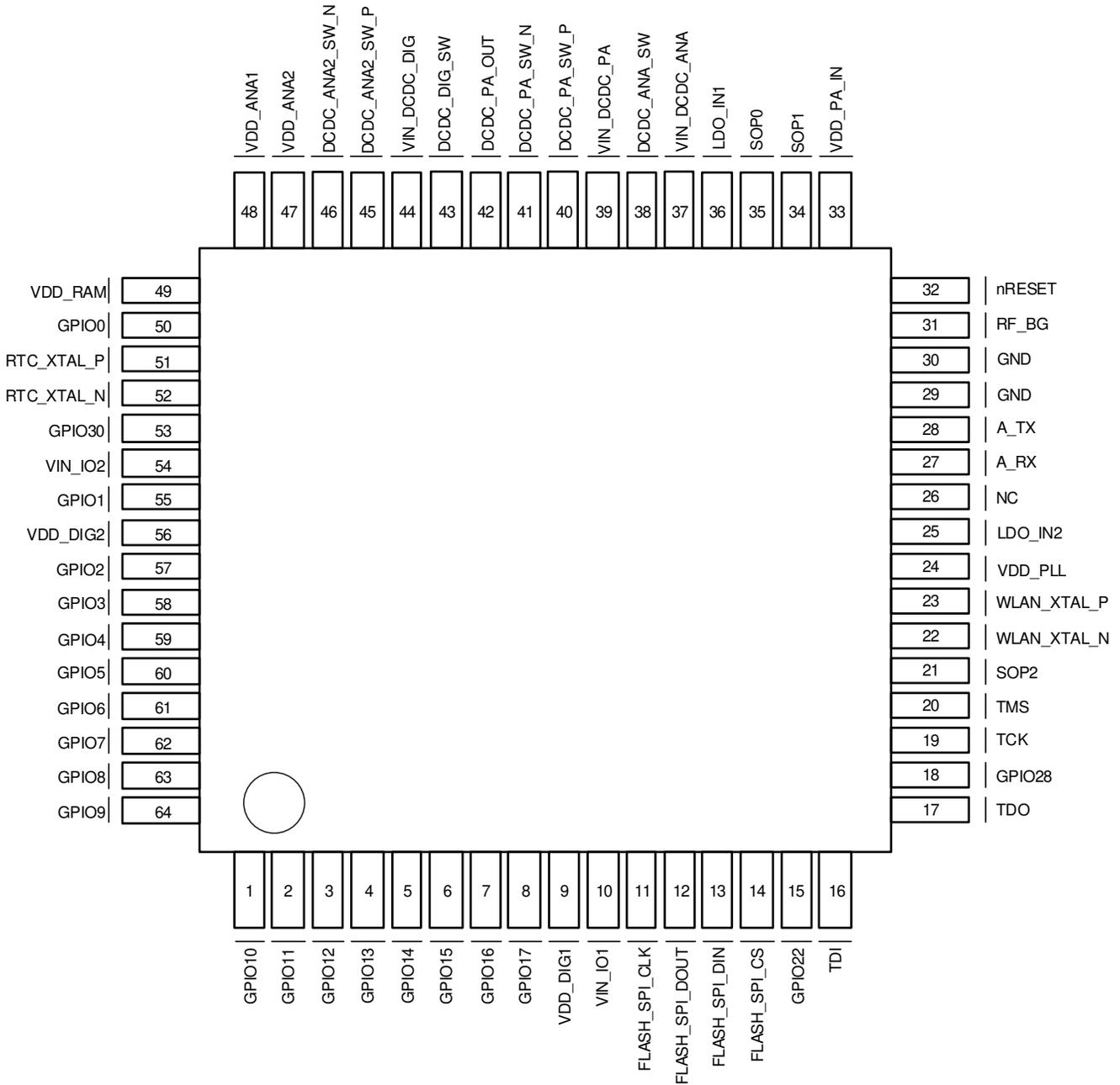
For information about other devices in this family of products or related products, see the links that follow.

|   |   |
|---|---|
| <a href="#">The SimpleLink™ MCU Portfolio</a>                           | This portfolio offers a single development environment that delivers flexible hardware, software, and tool options for customers developing wired and wireless applications. With 100 percent code reuse across host MCUs, Wi-Fi®, Bluetooth® low energy, Sub-1GHz devices and more, choose the MCU or connectivity standard that fits your design. A one-time investment with the SimpleLink™ software development kit (SDK) allows you to reuse often, opening the door to create unlimited applications. |
| <a href="#">SimpleLink™ Wi-Fi® Family</a>                               | This device platform offers several Internet-on-a chip™ solutions, which address the need of battery-operated, security-enabled products. Texas Instruments offers a single-chip wireless microcontroller and a wireless network processor that can be paired with any MCU, allowing developers to design new Wi-Fi® products or upgrade existing products with Wi-Fi® capabilities.  |
| <a href="#">BoosterPack™ Plug-in Module</a>                             | Extend the functionality of the TI LaunchPad™ Development Kit with the BoosterPack™ Plug-in Module. The application-specific BoosterPack Plug-in Module allows you to explore a broad range of applications, including capacitive touch, wireless sensing, LED Lighting control, and more. Stack multiple BoosterPack Plug-in Modules onto a single LaunchPad Development Kit to further enhance the functionality of your design.  |
| <a href="#">Reference Designs for CC3200, CC3220 and CC3235 Devices</a> | The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market.   |
| <a href="#">The SimpleLink™ Wi-Fi® SDK</a>                              | The SDK contains drivers for the CC3235 programmable MCU, sample applications, and documentation required to start development with CC3235x solutions.  |

## 6 Pin Configuration and Functions

### 6.1 Pin Diagram

Figure 6-1 shows pin assignments for the 64-pin VQFN package.



NC = No internal connection

**Figure 6-1. Top View Pin Assignment for 64-Pin VQFN**

## 6.2 Pin Attributes

The device makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at device reset) and register control.

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### Note

TI highly recommends using the [Pin Mux Tool](#) to obtain the desired pinout. In addition, refer to the user guide within the [SimpleLink™ CC32XX Software Development Kit \(SDK\)](#)

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The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used.

[Table 6-1](#) and [Table 6-2](#) list the pin descriptions and attributes. [Table 6-3](#) lists the signal descriptions. [Table 6-4](#) presents an overall view of pin multiplexing. All pin multiplexing options are configurable using the pin mux registers.

The following special considerations apply:

- All I/Os support drive strengths of 2mA, 4mA, and 6mA. The drive strength is individually configurable for each pin.
- All I/Os support 10µA pullup and pulldown resistors.
- The  $V_{IO}$  and  $V_{BAT}$  supply must be tied together at all times.
- By default, all I/Os float in the Hibernate state. However, the software can change the default state.
- All digital I/Os are non-fail-safe.

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### Note

If an external device drives a positive voltage to the signal pads and the CC3235x device is not powered, DC is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wake-up and boot of the CC3235x device can occur. To prevent current draw, TI recommends any one of the following conditions:

- All devices interfaced to the CC3235x device must be powered from the same power rail as the chip.
- Use level shifters between the device and any external devices fed from other independent rails.
- The nRESET pin of the CC3235x device must be held low until the  $V_{BAT}$  supply to the device is driven and stable.
- All GPIO pins default to high impedance unless programmed by the MCU. The bootloader sets the TDI, TDO, TCK, TMS, and Flash\_SPI pins to mode 1. All the other pins are left in the Hi-Z state.

The ADC inputs are tolerant up to 1.8V (see [Table 7-30](#) for more details about the usable range of the ADC). On the other hand, the digital pads can tolerate up to 3.6V. Hence, take care to prevent accidental damage to the ADC inputs. TI recommends first disabling the output buffers of the digital I/Os corresponding to the desired ADC channel (that is, converted to Hi-Z state), and thereafter disabling the respective pass switches (S7 [Pin 57], S8 [Pin 58], S9 [Pin 59], and S10 [Pin 60]). For more information, see [Section 6.5](#).

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**Table 6-1. Pin Descriptions**

| PINS              |                | TYPE   | DESCRIPTION   | SELECT AS WAKEUP SOURCE | CONFIGURE ADDITIONAL ANALOG MUX | MUXED WITH JTAG           |
|-------------------|----------------|--------|---|-------------------------|---------------------------------|---------------------------|
| NO.               | NAME           |        |   |                         |                                 |                           |
| 1                 | GPIO10         | I/O    | General-purpose input or output                       | No                      | No                              | No                        |
| 2                 | GPIO11         | I/O    | General-purpose input or output                       | Yes                     | No                              | No                        |
| 3                 | GPIO12         | I/O    | General-purpose input or output                       | No                      | No                              | No                        |
| 4                 | GPIO13         | I/O    | General-purpose input or output                       | Yes                     | No                              | No                        |
| 5                 | GPIO14         | I/O    | General-purpose input or output                       | No                      | No                              | No                        |
| 6                 | GPIO15         | I/O    | General-purpose input or output                       | No                      | No                              | No                        |
| 7                 | GPIO16         | I/O    | General-purpose input or output                       | No                      | No                              | No                        |
| 8                 | GPIO17         | I/O    | General-purpose input or output                       | Yes                     | No                              | No                        |
| 9                 | VDD_DIG1       | Power  | Internal digital core voltage                         | N/A                     | N/A                             | N/A                       |
| 10                | VIN_IO1        | Power  | I/O power supply (same as battery voltage)            | N/A                     | N/A                             | N/A                       |
| 11                | FLASH_SPI_CLK  | O      | Serial flash interface: SPI clock                     | N/A                     | N/A                             | N/A                       |
| 12                | FLASH_SPI_DOUT | O      | Serial flash interface: SPI data out                  | N/A                     | N/A                             | N/A                       |
| 13                | FLASH_SPI_DIN  | I      | Serial flash interface: SPI data in                   | N/A                     | N/A                             | N/A                       |
| 14                | FLASH_SPI_CS   | O      | Serial flash interface: SPI chip select               | N/A                     | N/A                             | N/A                       |
| 15                | GPIO22         | I/O    | General-purpose input or output                       | No                      | No                              | No                        |
| 16                | TDI            | I/O    | JTAG interface: data input                            | No                      | No                              | Muxed with JTAG TDI       |
| 17                | TDO            | I/O    | JTAG interface: data output                           | Yes                     | No                              | Muxed with JTAG TDO       |
| 18                | GPIO28         | I/O    | General-purpose input or output                       | No                      | No                              | No                        |
| 19                | TCK            | I/O    | JTAG / SWD interface: clock                           | No                      | No                              | Muxed with JTAG/ SWD-TCK  |
| 20                | TMS            | I/O    | JTAG / SWD interface: mode select or SWDIO            | No                      | No                              | Muxed with JTAG/ SWD-TMSC |
| 21 <sup>(1)</sup> | SOP2           | O      | Configuration sense-on-power                          | No                      | No                              | No                        |
| 22                | WLAN_XTAL_N    | Analog | 40-MHz XTAL   | N/A                     | N/A                             | N/A                       |
| 23                | WLAN_XTAL_P    | Analog | 40-MHz XTAL or TCXO clock input                       | N/A                     | N/A                             | N/A                       |
| 24                | VDD_PLL        | Power  | Internal analog voltage                               | N/A                     | N/A                             | N/A                       |
| 25                | LDO_IN2        | Power  | Analog RF supply from analog DCDC output              | N/A                     | N/A                             | N/A                       |
| 26                | NC             | —      | No Connect  | N/A                     | N/A                             | N/A                       |
| 27                | A_RX           | RF     | RF A band: 5 GHz A_RX                                 | N/A                     | N/A                             | N/A                       |
| 28                | A_TX           | RF     | RF A band: 5 GHz A_TX                                 | N/A                     | N/A                             | N/A                       |
| 29                | GND            | GND    | Ground  | N/A                     | N/A                             | N/A                       |
| 30                | GND            | GND    | Ground  | N/A                     | N/A                             | N/A                       |
| 31                | RF_BG          | RF     | RF BG band: 2.4 GHz TX, RX                            | N/A                     | N/A                             | N/A                       |
| 32                | nRESET         | I      | Master chip reset input. Active low input.            | N/A                     | N/A                             | N/A                       |
| 33                | VDD_PA_IN      | Power  | RF power amplifier (PA) input from PA DC-DC output    | N/A                     | N/A                             | N/A                       |
| 34                | SOP1           | O      | Configuration sense-on-power and 5 GHz switch control | N/A                     | N/A                             | N/A                       |

**Table 6-1. Pin Descriptions (continued)**

| PINS |                | TYPE   | DESCRIPTION  | SELECT AS WAKEUP SOURCE | CONFIGURE ADDITIONAL ANALOG MUX                    | MUXED WITH JTAG |
|------|----------------|--------|--|-------------------------|--|-----------------|
| NO.  | NAME           |        |  |                         |  |                 |
| 35   | SOP0           | O      | Configuration sense-on-power and 5 GHz switch control          | N/A                     | N/A  | N/A             |
| 36   | LDO_IN1        | Power  | Analog RF supply from analog DCDC output                       | N/A                     | N/A  | N/A             |
| 37   | VIN_DCDC_ANA   | Power  | Analog DC-DC supply input (same as battery voltage)            | N/A                     | N/A  | N/A             |
| 38   | DCDC_ANA_SW    | Power  | Analog DC/DC converter switching node                          | N/A                     | N/A  | N/A             |
| 39   | VIN_DCDC_PA    | Power  | PA DC/DC converter input supply (same as battery voltage)      | N/A                     | N/A  | N/A             |
| 40   | DCDC_PA_SW_P   | Power  | PA DC/DC converter +ve switching node                          | N/A                     | N/A  | N/A             |
| 41   | DCDC_PA_SW_N   | Power  | PA DC/DC converter –ve switching node                          | N/A                     | N/A  | N/A             |
| 42   | DCDC_PA_OUT    | Power  | PA DC/DC converter output.                                     | N/A                     | N/A  | N/A             |
| 43   | DCDC_DIG_SW    | Power  | Digital DC/DC converter switching node                         | N/A                     | N/A  | N/A             |
| 44   | VIN_DCDC_DIG   | Power  | Digital DC/DC converter supply input (same as battery voltage) | N/A                     | N/A  | N/A             |
| 45   | DCDC_ANA2_SW_P | I/O    | Analog2 DCDC converter +ve switching node                      | No                      | User configuration not required <sup>(2)</sup>     | No              |
| 46   | DCDC_ANA2_SW_N | Power  | Analog2 DC-DC converter -ve switching node                     | N/A                     | N/A  | N/A             |
| 47   | VDD_ANA2       | Power  | Analog2 DC-DC output   | N/A                     | N/A  | N/A             |
| 48   | VDD_ANA1       | Power  | Analog1 power supply fed by ANA2 DC-DC output                  | N/A                     | N/A  | N/A             |
| 49   | VDD_RAM        | Analog | SRAM LDO output  | N/A                     | N/A  | N/A             |
| 50   | GPIO0          | I/O    | General-purpose input or output                                | No                      | User configuration not required <sup>(2)</sup>     | No              |
| 51   | RTC_XTAL_P     | Analog | 32.768-kHz XTAL_P or external CMOS level clock input           | N/A                     | N/A  | N/A             |
| 52   | RTC_XTAL_N     | Analog | 32.768-kHz XTAL_N  | N/A                     | User configuration not required <sup>(2) (3)</sup> | No              |
| 53   | GPIO30         | I/O    | General-purpose input or output                                | No                      | User configuration not required <sup>(2)</sup>     | No              |
| 54   | VIN_IO2        | Analog | Chip supply voltage (VBAT)                                     | N/A                     | N/A  | N/A             |
| 55   | GPIO1          | I/O    | General-purpose input or output                                | No                      | No   | No              |
| 56   | VDD_DIG2       | Analog | Internal digital core voltage                                  | N/A                     | N/A  | N/A             |
| 57   | GPIO2          | I/O    | Analog input (1.5V max) or general-purpose input or output     | Wake-up source          | See <sup>(4)</sup>                                 | No              |
| 58   | GPIO3          | I/O    | Analog input (1.5V max) or general-purpose input or output     | No                      | See <sup>(4)</sup>                                 | No              |
| 59   | GPIO4          | I/O    | Analog input (1.5V max) or general-purpose input or output     | Wake-up source          | See <sup>(4)</sup>                                 | No              |
| 60   | GPIO5          | I/O    | Analog input (1.5V max) or general-purpose input or output     | No                      | See <sup>(4)</sup>                                 | No              |
| 61   | GPIO6          | I/O    | General-purpose input or output                                | No                      | No   | No              |
| 62   | GPIO7          | I/O    | General-purpose input or output                                | No                      | No   | No              |
| 63   | GPIO8          | I/O    | General-purpose input or output                                | No                      | No   | No              |
| 64   | GPIO9          | I/O    | General-purpose input or output                                | No                      | No   | No              |

**Table 6-1. Pin Descriptions (continued)**

| PINS    |      | TYPE | DESCRIPTION                       | SELECT AS WAKEUP SOURCE | CONFIGURE ADDITIONAL ANALOG MUX | MUXED WITH JTAG |
|---------|------|------|-----------------------------------|-------------------------|---------------------------------|-----------------|
| NO.     | NAME |      |                                   |                         |                                 |                 |
| GND_TAB |      | —    | Thermal pad and electrical ground | N/A                     | N/A                             | N/A             |

- (1) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TCXO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
- (2) Device firmware automatically enables the digital path during ROM boot.
- (3) To use the digital functions, RTC\_XTAL\_N must be pulled high to the supply voltage using a 100kΩ resistor.
- (4) Requires user configuration to enable the analog switch of the ADC channel (the switch is off by default.) The digital I/O is always connected and must be made Hi-Z before enabling the ADC switch.

**Table 6-2. Pin Attributes**

| PIN NO. | SIGNAL NAME <sup>(1)</sup> | SIGNAL TYPE <sup>(2)</sup> | PIN MUX ENCODING | SIGNAL DIRECTION | PAD STATES          |                    |            |
|---------|----------------------------|----------------------------|------------------|------------------|---------------------|--------------------|------------|
|         |                            |                            |                  |                  | LPDS <sup>(3)</sup> | Hib <sup>(4)</sup> | nRESET = 0 |
| 1       | GPIO10 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|         | I2C_SCL                    |                            | 1                | I/O (open drain) | Hi-Z, Pull, Drive   |                    |            |
|         | GT_PWM06                   |                            | 3                | O                | Hi-Z, Pull, Drive   |                    |            |
|         | UART1_TX                   |                            | 7                | O                | 1                   |                    |            |
|         | SDCARD_CLK                 |                            | 6                | O                | 0                   |                    |            |
|         | GT_CCP01                   |                            | 12               | I                | Hi-Z, Pull, Drive   |                    |            |
| 2       | GPIO11 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|         | I2C_SDA                    |                            | 1                | I/O (open drain) | Hi-Z, Pull, Drive   |                    |            |
|         | GT_PWM07                   |                            | 3                | O                | Hi-Z, Pull, Drive   |                    |            |
|         | pXCLK(XVCLK)               |                            | 4                | O                | 0                   |                    |            |
|         | SDCARD_CMD                 |                            | 6                | I/O (open drain) | Hi-Z, Pull, Drive   |                    |            |
|         | UART1_RX                   |                            | 7                | I                | Hi-Z, Pull, Drive   |                    |            |
|         | GT_CCP02                   |                            | 12               | I                | Hi-Z, Pull, Drive   |                    |            |
|         | MCAFSX                     |                            | 13               | O                | Hi-Z, Pull, Drive   |                    |            |
| 3       | GPIO12 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|         | McACLK                     |                            | 3                | O                | Hi-Z, Pull, Drive   |                    |            |
|         | pVS(VSYNC)                 |                            | 4                | I                | Hi-Z, Pull, Drive   |                    |            |
|         | I2C_SCL                    |                            | 5                | I/O (open drain) | Hi-Z, Pull, Drive   |                    |            |
|         | UART0_TX                   |                            | 7                | O                | 1                   |                    |            |
|         | GT_CCP03                   |                            | 12               | I                | Hi-Z, Pull, Drive   |                    |            |
| 4       | GPIO13 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|         | I2C_SDA                    |                            | 5                | I/O (open drain) |                     |                    |            |
|         | pHS(HSYNC)                 |                            | 4                | I                |                     |                    |            |
|         | UART0_RX                   |                            | 7                | I                |                     |                    |            |
|         | GT_CCP04                   |                            | 12               | I                |                     |                    |            |
| 5       | GPIO14 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|         | I2C_SCL                    |                            | 5                | I/O (open drain) |                     |                    |            |
|         | GSPI_CLK                   |                            | 7                | I/O              |                     |                    |            |
|         | pDATA8(CAM_D4)             |                            | 4                | I                |                     |                    |            |
|         | GT_CCP05                   |                            | 12               | I                |                     |                    |            |

**Table 6-2. Pin Attributes (continued)**

| PIN NO. | SIGNAL NAME <sup>(1)</sup> | SIGNAL TYPE <sup>(2)</sup> | PIN MUX ENCODING | SIGNAL DIRECTION | PAD STATES                       |   |            |
|---------|----------------------------|----------------------------|------------------|------------------|----------------------------------|---|------------|
|         |                            |                            |                  |                  | LPDS <sup>(3)</sup>              | Hib <sup>(4)</sup>                            | nRESET = 0 |
| 6       | GPIO15 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive                | Hi-Z, Pull, Drive                             | Hi-Z       |
|         | I2C_SDA                    |                            | 5                | I/O (open drain) |                                  |   |            |
|         | GSPI_MISO                  |                            | 7                | I/O              |                                  |   |            |
|         | pDATA9(CAM_D5)             |                            | 4                | I                |                                  |   |            |
|         | GT_CCP06                   |                            | 13               | I                |                                  |   |            |
|         | SDCARD_DATA0               |                            | 8                | I/O              |                                  |   |            |
| 7       | GPIO16 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive                | Hi-Z, Pull, Drive                             | Hi-Z       |
|         | GSPI_MOSI                  |                            | 7                | I/O              | Hi-Z, Pull, Drive                |   |            |
|         | pDATA10(CAM_D6)            |                            | 4                | I                | Hi-Z, Pull, Drive                |   |            |
|         | UART1_TX                   |                            | 5                | O                | 1                                |   |            |
|         | GT_CCP07                   |                            | 13               | I                | Hi-Z, Pull, Drive                |   |            |
|         | SDCARD_CLK                 |                            | 8                | O                | 0                                |   |            |
| 8       | GPIO17 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive                | Hi-Z, Pull, Drive                             | Hi-Z       |
|         | UART1_RX                   |                            | 5                | I                |                                  |   |            |
|         | GSPI_CS                    |                            | 7                | I/O              |                                  |   |            |
|         | pDATA11 (CAM_D7)           |                            | 4                | I                |                                  |   |            |
|         | SDCARD_CMD                 |                            | 8                | I/O              |                                  |   |            |
| 9       | VDD_DIG1 (PN)              | —                          | N/A              | N/A              | N/A                              | N/A   | N/A        |
| 10      | VIN_IO1                    | —                          | N/A              | N/A              | N/A                              | N/A   | N/A        |
| 11      | FLASH_SPI_CLK              | O                          | N/A              | O                | Hi-Z, Pull, Drive <sup>(5)</sup> | Hi-Z, Pull, Drive                             | Hi-Z       |
| 12      | FLASH_SPI_DOUT             | O                          | N/A              | O                | Hi-Z, Pull, Drive <sup>(5)</sup> | Hi-Z, Pull, Drive                             | Hi-Z       |
| 13      | FLASH_SPI_DIN              | I                          | N/A              | I                | Hi-Z, Pull, Drive <sup>(5)</sup> | Hi-Z  | Hi-Z       |
| 14      | FLASH_SPI_CS               | O                          | N/A              | O                | 1                                | Hi-Z, Pull, Drive                             | Hi-Z       |
| 15      | GPIO22 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive                | Hi-Z, Pull, Drive                             | Hi-Z       |
|         | McAFSX                     |                            | 7                | O                |                                  |   |            |
|         | GT_CCP04                   |                            | 5                | I                |                                  |   |            |
| 16      | TDI (PN)                   | I/O                        | 1                | I                | Hi-Z, Pull, Drive                | Hi-Z, Pull, Drive                             | Hi-Z       |
|         | GPIO23                     |                            | 0                | I/O              |                                  |   |            |
|         | UART1_TX                   |                            | 2                | O                | 1                                |   |            |
|         | I2C_SCL                    |                            | 9                | I/O (open drain) | Hi-Z, Pull, Drive                |   |            |
| 17      | TDO (PN)                   | I/O                        | 1                | O                | Hi-Z, Pull, Drive                | Driven high in SWD; driven low in 4-wire JTAG | Hi-Z       |
|         | GPIO24                     |                            | 0                | I/O              |                                  |   |            |
|         | PWM0                       |                            | 5                | O                |                                  |   |            |
|         | UART1_RX                   |                            | 2                | I                |                                  |   |            |
|         | I2C_SDA                    |                            | 9                | I/O (open drain) |                                  |   |            |
|         | GT_CCP06                   |                            | 4                | I                |                                  |   |            |
|         | McAFSX                     |                            | 6                | O                |                                  |   |            |
| 18      | GPIO28 (PN)                | I/O                        | 0                | I/O              | Hi-Z, Pull, Drive                | Hi-Z, Pull, Drive                             | Hi-Z       |
| 19      | TCK (PN)                   | I/O                        | 1                | I                | Hi-Z, Pull, Drive                | Hi-Z, Pull, Drive                             | Hi-Z       |
|         | GT_PWM03                   |                            | 8                | O                |                                  |   |            |

**Table 6-2. Pin Attributes (continued)**

| PIN NO.           | SIGNAL NAME <sup>(1)</sup> | SIGNAL TYPE <sup>(2)</sup> | PIN MUX ENCODING    | SIGNAL DIRECTION | PAD STATES          |                    |            |
|-------------------|----------------------------|----------------------------|---------------------|------------------|---------------------|--------------------|------------|
|                   |                            |                            |                     |                  | LPDS <sup>(3)</sup> | Hib <sup>(4)</sup> | nRESET = 0 |
| 20                | TMS (PN)                   | I/O                        | 1                   | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                   | GPIO29                     |                            | 0                   | I/O              |                     |                    |            |
| 21 <sup>(6)</sup> | GPIO25                     | O                          | 0                   | O                | Hi-Z, Pull, Drive   | Driven low         | Hi-Z       |
|                   | GT_PWM02                   |                            | 9                   | O                | Hi-Z, Pull, Drive   |                    |            |
|                   | McAFSX                     |                            | 2                   | O                | Hi-Z, Pull, Drive   |                    |            |
|                   | TCXO_EN                    |                            | N/A                 | O                | 0                   |                    |            |
|                   | SOP2 (PN)                  |                            | See <sup>(7)</sup>  | I                | Hi-Z, Pull, Drive   |                    |            |
| 22                | WLAN_XTAL_N                | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 23                | WLAN_XTAL_P                | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 24                | VDD_PLL                    | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 25                | LDO_IN2                    | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 26                | NC                         | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 27                | A_RX                       | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 28                | A_TX                       | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 29                | GND                        | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 30                | GND                        | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 31                | RF_BG                      | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 32                | nRESET                     | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 33                | VDD_PA_IN                  | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 34 <sup>(8)</sup> | SOP1 (PN)                  | I/O                        | N/A                 | N/A              | N/A                 | N/A                | N/A        |
|                   | A_SC1                      |                            | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 35 <sup>(8)</sup> | SOP0 (PN)                  | I/O                        | N/A                 | N/A              | N/A                 | N/A                | N/A        |
|                   | A_SC2                      |                            | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 36                | LDO_IN1                    | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 37                | VIN_DCDC_ANA               | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 38                | DCDC_ANA_SW                | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 39                | VIN_DCDC_PA                | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 40                | DCDC_PA_SW_P               | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 41                | DCDC_PA_SW_N               | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 42                | DCDC_PA_OUT                | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 43                | DCDC_DIG_SW                | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 44                | VIN_DCDC_DIG               | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 45 <sup>(9)</sup> | GPIO31                     | I/O                        | 0                   | I/O              | Hi-Z                | Hi-Z               | Hi-Z       |
|                   | UART0_RX                   |                            | 9                   | I                |                     |                    |            |
|                   | McAFSX                     |                            | 12                  | O                |                     |                    |            |
|                   | UART1_RX                   |                            | 2                   | I                |                     |                    |            |
|                   | McAXR0                     |                            | 6                   | I/O              |                     |                    |            |
|                   | GSPI_CLK                   |                            | 7                   | I/O              |                     |                    |            |
|                   | DCDC_ANA2_SW_P (PN)        | —                          | See <sup>(10)</sup> | N/A              | N/A                 | N/A                | N/A        |
| 46                | DCDC_ANA2_SW_N             | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 47                | VDD_ANA2                   | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 48                | VDD_ANA1                   | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 49                | VDD_RAM                    | —                          | N/A                 | N/A              | N/A                 | N/A                | N/A        |

**Table 6-2. Pin Attributes (continued)**

| PIN NO.            | SIGNAL NAME <sup>(1)</sup> | SIGNAL TYPE <sup>(2)</sup>               | PIN MUX ENCODING    | SIGNAL DIRECTION | PAD STATES          |                    |            |
|--------------------|----------------------------|--|---------------------|------------------|---------------------|--------------------|------------|
|                    |                            |  |                     |                  | LPDS <sup>(3)</sup> | Hib <sup>(4)</sup> | nRESET = 0 |
| 50                 | GPIO0 (PN)                 | I/O                                      | 0                   | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | UART0_CTS                  |  | 12                  | I                | Hi-Z, Pull, Drive   |                    |            |
|                    | McAXR1                     |  | 6                   | I/O              | Hi-Z, Pull, Drive   |                    |            |
|                    | GT_CCP00                   |  | 7                   | I                | Hi-Z, Pull, Drive   |                    |            |
|                    | GSPI_CS                    |  | 9                   | I/O              | Hi-Z, Pull, Drive   |                    |            |
|                    | UART1_RTS                  |  | 10                  | O                | 1                   |                    |            |
|                    | UART0_RTS                  |  | 3                   | O                | 1                   |                    |            |
|                    | McAXR0                     |  | 4                   | I/O              | Hi-Z, Pull, Drive   |                    |            |
| 51                 | RTC_XTAL_P                 | —  | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 52 <sup>(11)</sup> | RTC_XTAL_N (PN)            | O  | N/A                 | N/A              | N/A                 | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | GPIO32                     |  | 0                   | O                | Hi-Z, Pull, Drive   |                    |            |
|                    | McACLK                     |  | 2                   | O                |                     |                    |            |
|                    | McAXR0                     |  | 4                   | O                | 1                   |                    |            |
|                    | UART0_RTS                  |  | 6                   | O                |                     |                    |            |
|                    | GSPI_MOSI                  |  | 8                   | O                | Hi-Z, Pull, Drive   |                    |            |
| 53                 | GPIO30 (PN)                | I/O                                      | 0                   | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | UART0_TX                   |  | 9                   | O                | 1                   |                    |            |
|                    | McACLK                     |  | 2                   | O                | Hi-Z, Pull, Drive   |                    |            |
|                    | McAFSX                     |  | 3                   | O                |                     |                    |            |
|                    | GT_CCP05                   |  | 4                   | I                |                     |                    |            |
|                    | GSPI_MISO                  |  | 7                   | I/O              |                     |                    |            |
| 54                 | VIN_IO2                    | —  | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 55                 | GPIO1 (PN)                 | I/O                                      | 0                   | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | UART0_TX                   |  | 3                   | O                | 1                   |                    |            |
|                    | pCLK (PIXCLK)              |  | 4                   | I                | Hi-Z, Pull, Drive   |                    |            |
|                    | UART1_TX                   |  | 6                   | O                | 1                   |                    |            |
|                    | GT_CCP01                   |  | 7                   | I                | Hi-Z, Pull, Drive   |                    |            |
| 56                 | VDD_DIG2                   | —  | N/A                 | N/A              | N/A                 | N/A                | N/A        |
| 57 <sup>(12)</sup> | ADC_CH0                    | Analog input (up to 1.5V) or digital I/O | See <sup>(10)</sup> | I                | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | GPIO2 (PN)                 |  | 0                   | I/O              |                     |                    |            |
|                    | UART0_RX                   |  | 3                   | I                |                     |                    |            |
|                    | UART1_RX                   |  | 6                   | I                |                     |                    |            |
|                    | GT_CCP02                   |  | 7                   | I                |                     |                    |            |
| 58 <sup>(12)</sup> | ADC_CH1                    | Analog input (up to 1.5V) or digital I/O | See <sup>(10)</sup> | I                | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | GPIO3 (PN)                 |  | 0                   | I/O              |                     |                    |            |
|                    | UART1_TX                   |  | 6                   | O                | 1                   |                    |            |
|                    | pDATA7 (CAM_D3)            |  | 4                   | I                | Hi-Z, Pull, Drive   |                    |            |
| 59 <sup>(12)</sup> | ADC_CH2                    | Analog input (up to 1.5V) or digital I/O | See <sup>(10)</sup> | I                | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | GPIO4 (PN)                 |  | 0                   | I/O              |                     |                    |            |
|                    | UART1_RX                   |  | 6                   | I                |                     |                    |            |
|                    | pDATA6 (CAM_D2)            |  | 4                   | I                |                     |                    |            |

**Table 6-2. Pin Attributes (continued)**

| PIN NO.            | SIGNAL NAME <sup>(1)</sup> | SIGNAL TYPE <sup>(2)</sup>               | PIN MUX ENCODING    | SIGNAL DIRECTION | PAD STATES          |                    |            |
|--------------------|----------------------------|--|---------------------|------------------|---------------------|--------------------|------------|
|                    |                            |  |                     |                  | LPDS <sup>(3)</sup> | Hib <sup>(4)</sup> | nRESET = 0 |
| 60 <sup>(12)</sup> | ADC_CH3                    | Analog input (up to 1.5V) or digital I/O | See <sup>(10)</sup> | I                | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | GPIO5 (PN)                 |  | 0                   | I/O              |                     |                    |            |
|                    | pDATA5 (CAM_D1)            |  | 4                   | I                |                     |                    |            |
|                    | McAXR1                     |  | 6                   | I/O              |                     |                    |            |
|                    | GT_CCP05                   |  | 7                   | I                |                     |                    |            |
| 61                 | GPIO6 (PN)                 | I/O                                      | 0                   | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | UART0_RTS                  |  | 5                   | O                | 1                   |                    |            |
|                    | pDATA4 (CAM_D0)            |  | 4                   | I                | Hi-Z, Pull, Drive   |                    |            |
|                    | UART1_CTS                  |  | 3                   | I                |                     |                    |            |
|                    | UART0_CTS                  |  | 6                   | I                |                     |                    |            |
|                    | GT_CCP06                   |  | 7                   | I                |                     |                    |            |
| 62                 | GPIO7 (PN)                 | I/O                                      | 0                   | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | McACLKX                    |  | 13                  | O                | 1                   |                    |            |
|                    | UART1_RTS                  |  | 3                   | O                |                     |                    |            |
|                    | UART0_RTS                  |  | 10                  | O                |                     |                    |            |
|                    | UART0_TX                   |  | 11                  | O                |                     |                    |            |
| 63                 | GPIO8 (PN)                 | I/O                                      | 0                   | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | SDCARD_IRQ                 |  | 6                   | I                |                     |                    |            |
|                    | McAFSX                     |  | 7                   | O                |                     |                    |            |
|                    | GT_CCP06                   |  | 12                  | I                |                     |                    |            |
| 64                 | GPIO9 (PN)                 | I/O                                      | 0                   | I/O              | Hi-Z, Pull, Drive   | Hi-Z, Pull, Drive  | Hi-Z       |
|                    | GT_PWM05                   |  | 3                   | O                |                     |                    |            |
|                    | SDCARD_DATA0               |  | 6                   | I/O              |                     |                    |            |
|                    | McAXR0                     |  | 7                   | I/O              |                     |                    |            |
|                    | GT_CCP00                   |  | 12                  | I                |                     |                    |            |
| GND_TAB            | —                          | —  | N/A                 | N/A              | N/A                 | N/A                | N/A        |

- (1) Signals names with (PN) denote the default pin name.
- (2) Signal Types: I = Input, O = Output, I/O = Input or Output.
- (3) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.
- (4) Hibernate mode: The I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.
- (5) To minimize leakage in some serial flash vendors during LPDS, TI recommends that the user application always enables internal weak pulldown resistors on the FLASH\_SPI\_DIN, FLASH\_SPI\_DOUT, and FLASH\_SPI\_CLK pins.
- (6) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
- (7) This pin is one of three that must have a passive pullup or pulldown resistor onboard to configure the device hardware power-up mode. For this reason, the pin must be output only when used for digital functions.
- (8) This pin has dual functions: as a SOP (device operation mode) input pin during boot up, and as the 5GHz switch control (output) pin on power up.
- (9) Pin 45 is used by an internal DC/DC (ANA2\_DCDC). For the CC3235S device, pin 45 can be used as GPIO\_31 if a supply is provided on pin 47.
- (10) For details on proper use, see [Section 6.5](#).
- (11) Pin 52 is used by the RTC crystal oscillator. These devices use automatic configuration sensing. Therefore, some board-level configuration is required to use pin 52 as a digital pad. Pin 52 is used for RTC crystal in most applications. However, in some applications, a 32.768kHz square-wave clock might always be available onboard. When a 32.768kHz square-wave clock is available, the crystal can be removed to free pin 52 for digital functions. The external clock must then be applied at pin 51. For the chip to automatically detect this configuration, a 100kΩ pullup resistor must be connected between pin 52 and the supply line. To prevent false detection, TI recommends using pin 52 for output-only functions.
- (12) This pin is shared by the ADC inputs and digital I/O pad cells.

### 6.3 Signal Descriptions

**Table 6-3. Signal Descriptions**

| FUNCTION          | SIGNAL NAME | PIN NO.               | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                            |
|-------------------|-------------|-----------------------|----------|------------------|--|
| ADC               | ADC_CH0     | 57                    | I/O      | I                | ADC channel 0 input (maximum of 1.5 V) |
|                   | ADC_CH1     | 58                    | I/O      | I                | ADC channel 1 input (maximum of 1.5 V) |
|                   | ADC_CH2     | 59                    | I/O      | I                | ADC channel 2 input (maximum of 1.5 V) |
|                   | ADC_CH3     | 60                    | I        | I                | ADC channel 3 input (maximum of 1.5 V) |
| Antenna selection | GPIO10      | 1                     | I/O      | O                | Antenna selection control              |
|                   | GPIO11      | 2                     | I/O      | O                |  |
|                   | GPIO12      | 3                     | I/O      | O                |  |
|                   | GPIO13      | 4                     | I/O      | O                |  |
|                   | GPIO14      | 5                     | I/O      | O                |  |
|                   | GPIO15      | 6                     | I/O      | O                |  |
|                   | GPIO16      | 7                     | I/O      | O                |  |
|                   | GPIO17      | 8                     | I/O      | O                |  |
|                   | GPIO22      | 15                    | I/O      | O                |  |
|                   | GPIO28      | 18 <sup>(1)</sup>     | I/O      | O                |  |
|                   | GPIO25      | 21                    | O        | O                |  |
|                   | GPIO31      | 45 <sup>(1) (2)</sup> | I/O      | O                |  |
|                   | GPIO0       | 50                    | I/O      | O                |  |
|                   | GPIO32      | 52 <sup>(1)</sup>     | I/O      | O                |  |
|                   | GPIO30      | 53 <sup>(1)</sup>     | I/O      | O                |  |
|                   | GPIO3       | 58                    | I/O      | O                |  |
|                   | GPIO4       | 59                    | I/O      | O                |  |
|                   | GPIO5       | 60                    | I/O      | O                |  |
| GPIO6             | 61          | I/O                   | O        |                  |  |
| GPIO8             | 63          | I/O                   | O        |                  |  |
| GPIO9             | 64          | I/O                   | O        |                  |  |

**Table 6-3. Signal Descriptions (continued)**

| FUNCTION                      | SIGNAL NAME | PIN NO.               | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION   |
|-------------------------------|-------------|-----------------------|----------|------------------|---|
| BLE/2.4 GHz radio coexistence | GPIO10      | 1                     | I/O      | I/O              | Coexistence inputs and outputs  |
|                               | GPIO11      | 2                     | I/O      | O                |   |
|                               | GPIO12      | 3                     | I/O      | I/O              |   |
|                               | GPIO13      | 4                     | I/O      | I/O              |   |
|                               | GPIO14      | 5                     | I/O      | I/O              |   |
|                               | GPIO15      | 6                     | I/O      | I/O              |   |
|                               | GPIO16      | 7                     | I/O      | I/O              |   |
|                               | GPIO17      | 8                     | I/O      | O                |   |
|                               | GPIO22      | 15                    | I/O      | I/O              |   |
|                               | GPIO28      | 18 <sup>(1)</sup>     | I/O      | I/O              |   |
|                               | GPIO25      | 21                    | O        | O                |   |
|                               | GPIO31      | 45 <sup>(1) (2)</sup> | I/O      | I/O              |   |
|                               | GPIO0       | 50                    | I/O      | I/O              |   |
|                               | GPIO32      | 52 <sup>(1)</sup>     | I/O      | I/O              |   |
|                               | GPIO30      | 53 <sup>(1)</sup>     | I/O      | I/O              |   |
|                               | GPIO3       | 58                    | I/O      | O                |   |
|                               | GPIO4       | 59                    | I/O      | O                |   |
|                               | GPIO5       | 60                    | I/O      | I/O              |   |
| GPIO6                         | 61          | I/O                   | I/O      |                  |   |
| GPIO8                         | 63          | I/O                   | I/O      |                  |   |
| GPIO9                         | 64          | I/O                   | I/O      |                  |   |
| Clock                         | WLAN_XTAL_N | 22                    | —        | —                | 40-MHz crystal; pull down if external TCXO is used                      |
|                               | WLAN_XTAL_P | 23                    | —        | —                | 40-MHz crystal or TCXO clock input                                      |
|                               | RTC_XTAL_P  | 51                    | —        | —                | Connect 32.768-kHz crystal or force external CMOS level clock           |
|                               | RTC_XTAL_N  | 52                    | —        | —                | Connect 32.768-kHz crystal or connect 100-kΩ resistor to supply voltage |

**Table 6-3. Signal Descriptions (continued)**

| FUNCTION         | SIGNAL NAME | PIN NO.               | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                         |
|------------------|-------------|-----------------------|----------|------------------|-------------------------------------|
| Hostless mode    | HM_IO       | 1                     | I/O      | I/O              | Hostless mode inputs and outputs    |
|                  |             | 2                     | I/O      | O                |                                     |
|                  |             | 3                     | I/O      | I/O              |                                     |
|                  |             | 4                     | I/O      | I/O              |                                     |
|                  |             | 5                     | I/O      | I/O              |                                     |
|                  |             | 6                     | I/O      | I/O              |                                     |
|                  |             | 7                     | I/O      | I/O              |                                     |
|                  |             | 8                     | I/O      | O                |                                     |
|                  |             | 15                    | I/O      | I/O              |                                     |
|                  |             | 18 <sup>(1)</sup>     | I/O      | I/O              |                                     |
|                  |             | 21                    | O        | O                |                                     |
|                  |             | 45 <sup>(1) (2)</sup> | I/O      | I/O              |                                     |
|                  |             | 50                    | I/O      | I/O              |                                     |
|                  |             | 52 <sup>(1)</sup>     | I/O      | I/O              |                                     |
|                  |             | 53 <sup>(1)</sup>     | I/O      | I/O              |                                     |
|                  |             | 58                    | O        | O                |                                     |
|                  |             | 59                    | O        | O                |                                     |
| 60               | I/O         | I/O                   |          |                  |                                     |
| 61               | I/O         | I/O                   |          |                  |                                     |
| 63               | I/O         | I/O                   |          |                  |                                     |
| 64               | I/O         | I/O                   |          |                  |                                     |
| JTAG / SWD       | TDI         | 16                    | I/O      | I                | JTAG TDI. Reset default pinout.     |
|                  | TDO         | 17                    | I/O      | O                | JTAG TDO. Reset default pinout.     |
|                  | TCK         | 19                    | I/O      | I                | JTAG/SWD TCK. Reset default pinout. |
|                  | TMS         | 20                    | I/O      | I/O              | JTAG/SWD TMS. Reset default pinout. |
| I <sup>2</sup> C | I2C_SCL     | 1                     | I/O      | I/O (open drain) | I <sup>2</sup> C clock data         |
|                  |             | 3                     |          |                  |                                     |
|                  |             | 5                     |          |                  |                                     |
|                  |             | 16                    |          |                  |                                     |
|                  | I2C_SDA     | 2                     | I/O      | I/O (open drain) | I <sup>2</sup> C data               |
|                  |             | 4                     |          |                  |                                     |
|                  |             | 6                     |          |                  |                                     |
|                  |             | 17                    |          |                  |                                     |

**Table 6-3. Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | PIN NO. | PIN TYPE | SIGNAL DIRECTION             | DESCRIPTION                   |                     |
|----------|-------------|---------|----------|------------------------------|-------------------------------|---------------------|
| Timers   | GT_PWM06    | 1       | I/O      | O                            | Pulse-width modulated O/P     |                     |
|          | GT_CCP01    | 1       | I/O      | I                            | Timer capture port            |                     |
|          | GT_PWM07    | 2       | I/O      | O                            | Pulse-width modulated O/P     |                     |
|          | GT_CCP02    | 2       | I/O      | I                            | Timer capture ports           |                     |
|          | GT_CCP03    | 3       | I/O      | I                            |                               |                     |
|          | GT_CCP04    | 4       | I/O      | I                            |                               |                     |
|          |             | 15      | I/O      | I                            |                               |                     |
|          | GT_CCP05    | 5       | I/O      | I                            |                               |                     |
|          |             | 6       | I/O      | I                            |                               |                     |
|          | GT_CCP06    |         | 17       | I/O                          |                               | I                   |
|          |             |         | 61       | I/O                          |                               | I                   |
|          |             |         | 63       | I/O                          |                               | I                   |
|          | GT_CCP07    | 7       | I/O      | I                            |                               |                     |
|          | PWM0        | 17      | I/O      | O                            | Pulse-width modulated outputs |                     |
|          | GT_PWM03    | 19      | I/O      | O                            |                               |                     |
|          | GT_PWM02    | 21      | O        | O                            |                               |                     |
|          | GT_CCP00    |         | 50       | I/O                          | I                             | Timer capture ports |
|          |             |         | 64       | I/O                          | I                             |                     |
|          | GT_CCP05    | 53      | I/O      | I                            |                               |                     |
|          | GT_CCP01    | 55      | I/O      | I                            |                               |                     |
| GT_CCP02 | 57          | I/O     | I        |                              |                               |                     |
| GT_CCP05 | 60          | I       | I        | Timer capture port Input     |                               |                     |
| GT_PWM05 | 64          | I/O     | O        | Pulse-width modulated output |                               |                     |

**Table 6-3. Signal Descriptions (continued)**

| FUNCTION                         | SIGNAL NAME | PIN NO.           | PIN TYPE | SIGNAL DIRECTION                  | DESCRIPTION  |
|----------------------------------|-------------|-------------------|----------|-----------------------------------|--|
| GPIO                             | GPIO10      | 1                 | I/O      | I/O                               | General-purpose inputs or outputs  |
|                                  | GPIO11      | 2                 | I/O      | I/O                               |  |
|                                  | GPIO12      | 3                 | I/O      | I/O                               |  |
|                                  | GPIO13      | 4                 | I/O      | I/O                               |  |
|                                  | GPIO14      | 5                 | I/O      | I/O                               |  |
|                                  | GPIO15      | 6                 | I/O      | I/O                               |  |
|                                  | GPIO16      | 7                 | I/O      | I/O                               |  |
|                                  | GPIO17      | 8                 | I/O      | I/O                               |  |
|                                  | GPIO22      | 15                | I/O      | I/O                               |  |
|                                  | GPIO23      | 16                | I/O      | I/O                               |  |
|                                  | GPIO24      | 17                | I/O      | I/O                               |  |
|                                  | GPIO28      | 18                | I/O      | I/O                               |  |
|                                  | GPIO29      | 20                | I/O      | I/O                               |  |
|                                  | GPIO25      | 21                | O        | O                                 |  |
|                                  | GPIO31      | 45 <sup>(2)</sup> | I/O      | I/O                               |  |
|                                  | GPIO0       | 50                | I/O      | I/O                               |  |
|                                  | GPIO32      | 52                | I/O      | O                                 |  |
|                                  | GPIO30      | 53                | I/O      | I/O                               |  |
|                                  | GPIO1       | 55                | I/O      | I/O                               |  |
|                                  | GPIO2       | 57                | I/O      | I/O                               |  |
|                                  | GPIO3       | 58                | I/O      | I/O                               |  |
|                                  | GPIO4       | 59                | I/O      | I/O                               |  |
|                                  | GPIO5       | 60                | I/O      | I/O                               |  |
| GPIO6                            | 61          | I/O               | I/O      |                                   |  |
| GPIO7                            | 62          | I/O               | I/O      |                                   |  |
| GPIO8                            | 63          | I/O               | I/O      |                                   |  |
| GPIO9                            | 64          | I/O               | I/O      |                                   |  |
| McASP<br>I <sup>2</sup> S or PCM | MCAFSX      | 2                 | I/O      | O                                 | I <sup>2</sup> S audio port frame sync                                     |
|                                  |             | 15                |          |                                   |  |
|                                  |             | 17                |          |                                   |  |
|                                  |             | 21                |          |                                   |  |
|                                  |             | 45 <sup>(2)</sup> |          |                                   |  |
|                                  |             | 53                |          |                                   |  |
|                                  | McACLK      | 3                 | I/O      | O                                 | I <sup>2</sup> S audio port clock outputs                                  |
|                                  |             | 52                | O        | O                                 |  |
|                                  |             | 53                | I/O      | O                                 |  |
|                                  | McAXR1      | 50                | I/O      | I/O                               | I <sup>2</sup> S audio port data 1 (RX/TX)                                 |
|                                  |             | 60                | I        | I/O                               | I <sup>2</sup> S audio port data 1 (RX and TX)                             |
|                                  | McAXR0      | 45 <sup>(2)</sup> | I/O      | I/O                               | I <sup>2</sup> S audio port data 0 (RX and TX)                             |
|                                  |             | 50                | I/O      | I/O                               |  |
|                                  |             | 52                | O        | O                                 | I <sup>2</sup> S audio port data (only output mode is supported on pin 52) |
|                                  |             | 64                | I/O      | I/O                               | I <sup>2</sup> S audio port data (RX and TX)                               |
| McACLKX                          | 62          | I/O               | O        | I <sup>2</sup> S audio port clock |  |

**Table 6-3. Signal Descriptions (continued)**

| FUNCTION                          | SIGNAL NAME      | PIN NO.           | PIN TYPE | SIGNAL DIRECTION                      | DESCRIPTION  |
|-----------------------------------|------------------|-------------------|----------|---------------------------------------|--|
| Multimedia card (MMC or SD)       | SDCARD_CLK       | 1                 | I/O      | O                                     | SD card clock data   |
|                                   |                  | 7                 |          |                                       |  |
|                                   | SDCARD_CMD       | 2                 | I/O      | I/O (open drain)                      | SD card command line   |
|                                   |                  | 8                 | I/O      | I/O                                   |  |
|                                   | SDCARD_DATA0     | 6                 | I/O      | I/O                                   | SD card data   |
| 64                                |                  |                   |          |                                       |  |
| SDCARD_IRQ                        | 63               | I/O               | I        | Interrupt from SD card <sup>(3)</sup> |  |
| Parallel interface (8-bit $\pi$ ) | pXCLK (XVCLK)    | 2                 | I/O      | O                                     | Free clock to parallel camera  |
|                                   | pVS (VSYNC)      | 3                 | I/O      | I                                     | Parallel camera vertical sync  |
|                                   | pHS (HSYNC)      | 4                 | I/O      | I                                     | Parallel camera horizontal sync                                      |
|                                   | pDATA8 (CAM_D4)  | 5                 | I/O      | I                                     | Parallel camera data bit 4   |
|                                   | pDATA9 (CAM_D5)  | 6                 | I/O      | I                                     | Parallel camera data bit 5   |
|                                   | pDATA10 (CAM_D6) | 7                 | I/O      | I                                     | Parallel camera data bit 6   |
|                                   | pDATA11 (CAM_D7) | 8                 | I/O      | I                                     | Parallel camera data bit 7   |
|                                   | pCLK (PIXCLK)    | 55                | I/O      | I                                     | Pixel clock from parallel camera sensor                              |
|                                   | pDATA7 (CAM_D3)  | 58                | I/O      | I                                     | Parallel camera data bit 3   |
|                                   | pDATA6 (CAM_D2)  | 59                | I/O      | I                                     | Parallel camera data bit 2   |
|                                   | pDATA5 (CAM_D1)  | 60                | I        | I                                     | Parallel camera data bit 1   |
| pDATA4 (CAM_D0)                   | 61               | I/O               | I        | Parallel camera data bit 0            |  |
| Power                             | VDD_DIG1         | 9                 | —        | —                                     | Internal digital core voltage  |
|                                   | VIN_IO1          | 10                | —        | —                                     | Device supply voltage ( $V_{BAT}$ )                                  |
|                                   | VDD_PLL          | 24                | —        | —                                     | Internal analog voltage  |
|                                   | LDO_IN2          | 25                | —        | —                                     | Internal analog RF supply from analog DC/DC output                   |
|                                   | VDD_PA_IN        | 33                | —        | —                                     | Internal PA supply voltage from PA DC/DC output                      |
|                                   | LDO_IN1          | 36                | —        | —                                     | Internal analog RF supply from analog DC/DC output                   |
|                                   | VIN_DCDC_ANA     | 37                | —        | —                                     | Analog DC/DC input (connected to device input supply [ $V_{BAT}$ ])  |
|                                   | DCDC_ANA_SW      | 38                | —        | —                                     | Internal analog DC/DC switching node                                 |
|                                   | VIN_DCDC_PA      | 39                | —        | —                                     | PA DC/DC input (connected to device input supply [ $V_{BAT}$ ])      |
|                                   | DCDC_PA_SW_P     | 40                | —        | —                                     | Internal PA DC/DC switching node                                     |
|                                   | DCDC_PA_SW_N     | 41                | —        | —                                     | Internal PA DC/DC switching node                                     |
|                                   | DCDC_PA_OUT      | 42                | —        | —                                     | Internal PA buck converter output                                    |
|                                   | DCDC_DIG_SW      | 43                | —        | —                                     | Internal digital DC/DC switching node                                |
|                                   | VIN_DCDC_DIG     | 44                | —        | —                                     | Digital DC/DC input (connected to device input supply [ $V_{BAT}$ ]) |
|                                   | DCDC_ANA2_SW_P   | 45 <sup>(2)</sup> | —        | —                                     | Analog to DC/DC converter +ve switching node                         |
|                                   | DCDC_ANA2_SW_N   | 46                | —        | —                                     | Internal analog to DC/DC converter –ve switching node                |
|                                   | VDD_ANA2         | 47                | —        | —                                     | Internal analog to DC/DC output                                      |
|                                   | VDD_ANA1         | 48                | —        | —                                     | Internal analog supply fed by ANA2 DC/DC output                      |
| VDD_RAM                           | 49               | —                 | —        | Internal SRAM LDO output              |  |
| VIN_IO2                           | 54               | —                 | —        | Device supply voltage ( $V_{BAT}$ )   |  |
| VDD_DIG2                          | 56               | —                 | —        | Internal digital core voltage         |  |
| Reset                             | nRESET           | 32                | I        | I                                     | Global master device reset (active low)                              |

**Table 6-3. Signal Descriptions (continued)**

| FUNCTION  | SIGNAL NAME    | PIN NO.           | PIN TYPE          | SIGNAL DIRECTION | DESCRIPTION                                       |  |
|-----------|----------------|-------------------|-------------------|------------------|---|--|
| RF        | A_RX           | 27                | I                 | I                | WLAN analog A-band receive                        |  |
|           | A_TX           | 28                | O                 | O                | WLAN analog A-band transmit                       |  |
|           | RF_BG          | 31                | I/O               | I/O              | WLAN analog RF 802.11 b/g bands                   |  |
| SPI       | GSPI_CLK       | 5                 | I/O               | I/O              | General SPI clock                                 |  |
|           |                | 45 <sup>(2)</sup> | I/O               | I/O              |   |  |
|           | GSPI_MISO      | 6                 | I/O               | I/O              | General SPI MISO                                  |  |
|           |                | 53                | I/O               | I/O              |   |  |
|           | GSPI_CS        | 8                 | I/O               | I/O              | General SPI device select                         |  |
|           |                | 50                | I/O               | I/O              |   |  |
|           | GSPI_MOSI      | 7                 | I/O               | I/O              | General SPI MOSI                                  |  |
| 52        |                | O                 | O                 |                  |   |  |
| FLASH SPI | FLASH_SPI_CLK  | 11                | O                 | O                | Clock to SPI serial flash (fixed default)         |  |
|           | FLASH_SPI_DOUT | 12                | O                 | O                | Data to SPI serial flash (fixed default)          |  |
|           | FLASH_SPI_DIN  | 13                | I                 | I                | Data from SPI serial flash (fixed default)        |  |
|           | FLASH_SPI_CS   | 14                | O                 | O                | Device select to SPI serial flash (fixed default) |  |
| UART      | UART1_TX       | 1                 | I/O               | O                | UART TX data                                      |  |
|           |                | 7                 | I/O               | O                |   |  |
|           |                | 16                | I/O               | O                |   |  |
|           |                | 55                | I/O               | O                |   |  |
|           |                | 58                | I/O               | O                |   |  |
|           | UART1_RX       | 2                 | I/O               | I                | UART RX data                                      |  |
|           |                | 8                 | I/O               | I                |   |  |
|           |                | 17                | I/O               | I                |   |  |
|           |                | 45 <sup>(2)</sup> | I/O               | I                | UART1 RX data                                     |  |
|           |                | 57                | I/O               | I                |   |  |
|           |                | 59                | I/O               | I                |   |  |
|           | UART1_RTS      | 50                | I/O               | O                | UART1 request-to-send (active low)                |  |
|           |                | 62                | I/O               | O                |   |  |
|           | UART1_CTS      | 61                | I/O               | I                | UART1 clear-to-send (active low)                  |  |
|           | UART0_TX       | UART0_TX          | 3                 | I/O              | O   | UART0 TX data                          |
|           |                |                   | 53                | I/O              | O   |  |
|           |                |                   | 55                | I/O              | O   |  |
|           |                |                   | 62                | I/O              | O   |  |
|           | UART0_RX       | UART0_RX          | 4                 | I/O              | I   | UART0 RX data                          |
|           |                |                   | 45 <sup>(2)</sup> | I/O              | I   | UART0 RX data                          |
|           |                |                   | 57                | I/O              | I   | UART0 RX data                          |
|           | UART0_CTS      | UART0_CTS         | 50                | I/O              | I   | UART0 clear-to-send input (active low) |
|           |                |                   | 61                |                  |   |  |
|           | UART0_RTS      | UART0_RTS         | 50                | I/O              | O   | UART0 request-to-send (active low)     |
| 52        |                |                   | O                 | O                |   |  |
| 61        |                |                   | I/O               | O                |   |  |
| 62        |                |                   | I/O               | O                |   |  |

**Table 6-3. Signal Descriptions (continued)**

| FUNCTION       | SIGNAL NAME | PIN NO.           | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                    |
|----------------|-------------|-------------------|----------|------------------|--------------------------------|
| Sense-On-Power | SOP2        | 21 <sup>(4)</sup> | O        | I                | Sense-on-power 2               |
|                | SOP1        | 34                | I        | I                | Configuration sense-on-power 1 |
|                | SOP0        | 35                | I        | I                | Configuration sense-on-power 0 |

- (1) LPDS retention unavailable.
- (2) Pin 45 is used by an internal DC/DC (ANA2\_DCDC). For CC3235S device, pin 45 can be used as GPIO\_31 if a supply is provided on pin 47.
- (3) Future support.
- (4) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TCXO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

## 6.4 Pin Multiplexing

**Table 6-4. Pin Multiplexing**

| Register Address | Register Name      | Pin                                 | ANALOG OR SPECIAL FUNCTION     |                  |                  |                  | Digital Function (XXX Field Encoding) <sup>(1)</sup> |         |          |          |                  |          |            |           |              |          |    |    |          |          |
|------------------|--------------------|-------------------------------------|--------------------------------|------------------|------------------|------------------|--|---------|----------|----------|------------------|----------|------------|-----------|--------------|----------|----|----|----------|----------|
|                  |                    |                                     | JTAG                           | Hostless Mode    | BLE COEX         |                  | 0  | 1       | 2        | 3        | 4                | 5        | 6          | 7         | 8            | 9        | 10 | 11 | 12       | 13       |
|                  |                    |                                     |                                |                  | CC_COEX_SW_OUT   | CC_COEX_BLE_IN   |  |         |          |          |                  |          |            |           |              |          |    |    |          |          |
| 0x4402E0C8       | GPIO_PAD_CONFIG_10 | 1                                   | —                              | Y                | Y                | Y                | GPIO10   | I2C_SCL | —        | GT_PWM06 | —                | —        | SDCARD_CLK | UART1_TX  | —            | —        | —  | —  | GT_CCP01 | —        |
| 0x4402E0CC       | GPIO_PAD_CONFIG_11 | 2                                   | —                              | Y <sup>(2)</sup> | Y                | —                | GPIO11   | I2C_SDA | —        | GT_PWM07 | pXCLK (XVCLK)    | —        | SDCARD_CMD | UART1_RX  | —            | —        | —  | —  | GT_CCP02 | McAFSX   |
| 0x4402E0D0       | GPIO_PAD_CONFIG_12 | 3                                   | —                              | Y                | Y                | Y                | GPIO12   | —       | —        | McACLK   | pVS (VSYNC)      | I2C_SCL  | —          | UART0_TX  | —            | —        | —  | —  | GT_CCP03 | —        |
| 0x4402E0D4       | GPIO_PAD_CONFIG_13 | 4                                   | —                              | Y                | Y                | Y                | GPIO13   | —       | —        | —        | pHS (HSYNC)      | I2C_SDA  | —          | UART0_RX  | —            | —        | —  | —  | GT_CCP04 | —        |
| 0x4402E0D8       | GPIO_PAD_CONFIG_14 | 5                                   | —                              | Y                | Y                | Y                | GPIO14   | —       | —        | —        | pDATA8 (CAM_D4)  | I2C_SCL  | —          | GSPI_CLK  | —            | —        | —  | —  | GT_CCP05 | —        |
| 0x4402E0DC       | GPIO_PAD_CONFIG_15 | 6                                   | —                              | Y                | Y                | Y                | GPIO15   | —       | —        | —        | pDATA9 (CAM_D5)  | I2C_SDA  | —          | GSPI_MISO | SDCARD_DATA0 | —        | —  | —  | —        | GT_CCP06 |
| 0x4402E0E0       | GPIO_PAD_CONFIG_16 | 7                                   | —                              | Y                | Y                | Y                | GPIO16   | —       | —        | —        | pDATA10 (CAM_D6) | UART1_TX | —          | GSPI_MOSI | SDCARD_CLK   | —        | —  | —  | —        | GT_CCP07 |
| 0x4402E0E4       | GPIO_PAD_CONFIG_17 | 8                                   | —                              | Y <sup>(2)</sup> | Y                | —                | GPIO17   | —       | —        | —        | pDATA11 (CAM_D7) | UART1_RX | —          | GSPI_CS   | SDCARD_CMD   | —        | —  | —  | —        | —        |
| 0x4402E0F8       | GPIO_PAD_CONFIG_22 | 15                                  | —                              | Y                | Y                | Y                | GPIO22   | —       | —        | —        | —                | GT_CCP04 | —          | McAFSX    | —            | —        | —  | —  | —        | —        |
| 0x4402E0FC       | GPIO_PAD_CONFIG_23 | 16                                  | Muxed with JTAG                | —                | —                | —                | GPIO23   | TDI     | UART1_TX | —        | —                | —        | —          | —         | —            | I2C_SCL  | —  | —  | —        | —        |
| 0x4402E100       | GPIO_PAD_CONFIG_24 | 17                                  | Muxed with JTAG TDO            | —                | —                | —                | GPIO24   | TDO     | UART1_RX | —        | GT_CCP06         | PWM0     | McAFSX     | —         | —            | I2C_SDA  | —  | —  | —        | —        |
| 0x4402E140       | GPIO_PAD_CONFIG_40 | 18                                  | —                              | Y <sup>(3)</sup> | Y <sup>(3)</sup> | Y <sup>(3)</sup> | GPIO28   | —       | —        | —        | —                | —        | —          | —         | —            | —        | —  | —  | —        | —        |
| 0x4402E110       | GPIO_PAD_CONFIG_28 | 19                                  | Muxed with JTAG or SWD and TCK | —                | —                | —                | —  | TCK     | —        | —        | —                | —        | —          | —         | GT_PWM03     | —        | —  | —  | —        | —        |
| 0x4402E114       | GPIO_PAD_CONFIG_29 | 20                                  | Muxed with JTAG or SWD and TMS | —                | —                | —                | GPIO29   | TMS     | —        | —        | —                | —        | —          | —         | —            | —        | —  | —  | —        | —        |
| 0x4402E104       | GPIO_PAD_CONFIG_25 | 21 <sup>(4)</sup>                   | —                              | Y <sup>(2)</sup> | Y                | —                | GPIO25   | —       | McAFSX   | —        | —                | —        | —          | —         | —            | GT_PWM02 | —  | —  | —        | —        |
| 0x4402E11C       | GPIO_PAD_CONFIG_31 | 45 <sup>(3)</sup><br><sup>(5)</sup> | —                              | Y                | Y                | Y                | GPIO31   | —       | UART1_RX | —        | —                | —        | McAXR0     | GSPI_CLK  | —            | UART0_RX | —  | —  | McAFSX   | —        |

**Table 6-4. Pin Multiplexing (continued)**

| Register Address | Register Name      | Pin | ANALOG OR SPECIAL FUNCTION |                  |                  |                  | Digital Function (XXX Field Encoding) <sup>(1)</sup> |   |        |           |                 |           |              |           |           |          |           |          |           |          |
|------------------|--------------------|-----|----------------------------|------------------|------------------|------------------|--|---|--------|-----------|-----------------|-----------|--------------|-----------|-----------|----------|-----------|----------|-----------|----------|
|                  |                    |     | JTAG                       | Hostless Mode    | BLE COEX         |                  | 0  | 1 | 2      | 3         | 4               | 5         | 6            | 7         | 8         | 9        | 10        | 11       | 12        | 13       |
|                  |                    |     |                            |                  | CC_COEX_SW_OUT   | CC_COEX_BLE_IN   |  |   |        |           |                 |           |              |           |           |          |           |          |           |          |
| 0x4402E0A0       | GPIO_PAD_CONFIG_0  | 50  | —                          | Y                | Y                | Y                | GPIO0  | — | —      | UART0_RTS | McAXR0          | —         | McAXR1       | GT_CCP00  | —         | GSPI_CS  | UART1_RTS | —        | UART0_CTS | —        |
| 0x4402E120       | GPIO_PAD_CONFIG_32 | 52  | —                          | Y <sup>(3)</sup> | Y <sup>(3)</sup> | Y <sup>(3)</sup> | GPIO32   | — | McACLK | —         | McAXR0          | —         | UART0_RTS    | —         | GSPI_MOSI | —        | —         | —        | —         | —        |
| 0x4402E118       | GPIO_PAD_CONFIG_30 | 53  | —                          | Y <sup>(3)</sup> | Y <sup>(3)</sup> | Y <sup>(3)</sup> | GPIO30   | — | McACLK | McAFSX    | GT_CCP05        | —         | —            | GSPI_MISO | —         | UART0_TX | —         | —        | —         | —        |
| 0x4402E0A4       | GPIO_PAD_CONFIG_1  | 55  | —                          | —                | —                | —                | GPIO1  | — | —      | UART0_TX  | pCLK (PIXCLK)   | —         | UART1_TX     | GT_CCP01  | —         | —        | —         | —        | —         | —        |
| 0x4402E0A8       | GPIO_PAD_CONFIG_2  | 57  | —                          | —                | —                | —                | GPIO2  | — | —      | UART0_RX  | —               | —         | UART1_RX     | GT_CCP02  | —         | —        | —         | —        | —         | —        |
| 0x4402E0AC       | GPIO_PAD_CONFIG_3  | 58  | —                          | Y <sup>(2)</sup> | Y                | —                | GPIO3  | — | —      | —         | pDATA7 (CAM_D3) | —         | UART1_TX     | —         | —         | —        | —         | —        | —         | —        |
| 0x4402E0B0       | GPIO_PAD_CONFIG_4  | 59  | —                          | Y <sup>(2)</sup> | Y                | —                | GPIO4  | — | —      | —         | pDATA6 (CAM_D2) | —         | UART1_RX     | —         | —         | —        | —         | —        | —         | —        |
| 0x4402E0B4       | GPIO_PAD_CONFIG_5  | 60  | —                          | Y                | Y                | Y                | GPIO5  | — | —      | —         | pDATA5 (CAM_D1) | —         | McAXR1       | GT_CCP05  | —         | —        | —         | —        | —         | —        |
| 0x4402E0B8       | GPIO_PAD_CONFIG_6  | 61  | —                          | Y                | Y                | Y                | GPIO6  | — | —      | UART1_CTS | pDATA4 (CAM_D0) | UART0_RTS | UART0_CTS    | GT_CCP06  | —         | —        | —         | —        | —         | —        |
| 0x4402E0BC       | GPIO_PAD_CONFIG_7  | 62  | —                          | —                | —                | —                | GPIO7  | — | —      | UART1_RTS | —               | —         | —            | —         | —         | —        | UART0_RTS | UART0_TX | —         | McACLKX  |
| 0x4402E0C0       | GPIO_PAD_CONFIG_8  | 63  | —                          | Y                | Y                | Y                | GPIO8  | — | —      | —         | —               | —         | SDCARD_IRQ   | McAFSX    | —         | —        | —         | —        | —         | GT_CCP06 |
| 0x4402E0C4       | GPIO_PAD_CONFIG_9  | 64  | —                          | Y                | Y                | Y                | GPIO9  | — | —      | GT_PWM05  | —               | —         | SDCARD_DATA0 | McAXR0    | —         | —        | —         | —        | —         | GT_CCP00 |

- (1) Pin mux encodings with (RD) denote the default encoding after reset release.
- (2) Output Only
- (3) LPDS retention unavailable.
- (4) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TCXO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
- (5) Pin 45 is used by an internal DC/DC (ANA2\_DCDC). For CC3235S device, pin 45 can be used as GPIO\_31 if a supply is provided on pin 47.

## 6.5 Drive Strength and Reset States for Analog and Digital Multiplexed Pins

Table 6-5 describes the use, drive strength, and default state of analog and digital multiplexed pins at first-time power up and reset (nRESET pulled low).

**Table 6-5. Drive Strength and Reset States for Analog and Digital Multiplexed Pins**

| Pin | Board-Level Configuration and Use   | Default State at First Power Up or Forced Reset            | State After Configuration of Analog Switches (ACTIVE, LPDS, and HIB Power Modes) | Maximum Effective Drive Strength (mA) |
|-----|---|--|--|---------------------------------------|
| 45  | VDD_ANA2 (pin 47) must be shorted to the input supply rail. Otherwise, the pin is driven by the ANA2 DC/DC. | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os.                          | 4                                     |
| 50  | Generic I/O   | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os.                          | 4                                     |
| 52  | The pin must have an external pullup of 100 kΩ to the supply rail and must be used in output signals only.  | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os.                          | 4                                     |
| 53  | Generic I/O   | Analog is isolated. The digital I/O cell is also isolated. | Determined by the I/O state, as are other digital I/Os.                          | 4                                     |
| 57  | Analog signal (1.8-V absolute, 1.46-V full scale)   | ADC is isolated. The digital I/O cell is also isolated.    | Determined by the I/O state, as are other digital I/Os.                          | 4                                     |
| 58  | Analog signal (1.8-V absolute, 1.46-V full scale)   | ADC is isolated. The digital I/O cell is also isolated.    | Determined by the I/O state, as are other digital I/Os.                          | 4                                     |
| 59  | Analog signal (1.8-V absolute, 1.46-V full scale)   | ADC is isolated. The digital I/O cell is also isolated.    | Determined by the I/O state, as are other digital I/Os.                          | 4                                     |
| 60  | Analog signal (1.8-V absolute, 1.46-V full scale)   | ADC is isolated. The digital I/O cell is also isolated.    | Determined by the I/O state, as are other digital I/Os.                          | 4                                     |

## 6.6 Pad State After Application of Power to Device, Before Reset Release

When a stable power is applied to the CC3235x device for the first time or when supply voltage is restored to the proper value following a period with supply voltage less than 1.5 V, the level of each digital pad is undefined in the period starting from the release of nRESET and until DIG\_DCDC powers up. This period is less than approximately 10 ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins is required to have a definite value during this pre-reset period, an appropriate pullup or pulldown resistor must be used at the board level. The recommended value of this external pull is 2.7 kΩ.

## 6.7 Connections for Unused Pins

All unused pin should be configured as stated in [Table 6-6](#).

**Table 6-6. Connections for Unused Pins**

| FUNCTION   | SIGNAL DESCRIPTION              | PIN NUMBER | ACCEPTABLE PRACTICE   | PREFERRED PRACTICE  |
|------------|---------------------------------|------------|---|---|
| GPIO       | General-purpose input or output |            | Wake up I/O source should not be floating during hibernate. All the I/O pins will float while in Hibernate and Reset states. Ensure pullup and pulldown resistors are available on board to maintain the state of the I/O. Leave unused GPIOs as NC |   |
| No Connect | NC                              | 26         | Unused pin, leave as NC.  | Unused pin, leave as NC   |
| SOP        | Configuration sense-on-power    |            | Ensure pulldown resistors are available on unused SOP pins  | 69.8K Pull down resistor on SOP0 and SOP1 used as switch control pins, 100K pull down on SOP2 |
| Reset      | RESET input for the device      |            | Never leave the reset pin floating  |   |
| Clock      | RTC_XTAL_N                      |            | When using an external oscillator, add a 100-kΩ pullup resistor to VIO  |   |
|            | WLAN_XTAL_N                     |            | When using an external oscillator, connect to ground if unused  |   |
| JTAG       | JTAG interface                  |            | Leave as NC if unused   |   |

## 7 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

### 7.1 Absolute Maximum Ratings

All measurements are referenced at the device pins unless otherwise indicated. All specifications are over process and overvoltage unless otherwise indicated.

Over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                                |                                   |                      | MIN  | MAX            | UNIT |
|--------------------------------|-----------------------------------|----------------------|--|----------------|------|
| Supply voltage                 | $V_{BAT}$ and $V_{IO}$            | Pins: 37, 39, 44     | -0.5   | 3.8            | V    |
|                                | $V_{IO} - V_{BAT}$ (differential) | Pins: 10, 54         | $V_{BAT}$ and $V_{IO}$ should be tied together |                | V    |
| Digital inputs                 |                                   |                      | -0.5   | $V_{IO} + 0.5$ | V    |
| RF pins                        |                                   |                      | -0.5   | 2.1            | V    |
| Analog pins, Crystal           |                                   | Pins: 22, 23, 51, 52 | -0.5   | 2.1            | V    |
| Operating temperature, $T_A$   |                                   |                      | -40  | 85             | °C   |
| Storage temperature, $T_{stg}$ |                                   |                      | -55  | 125            | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to  $V_{SS}$ , unless otherwise noted.

### 7.2 ESD Ratings

|           |                         | VALUE   | UNIT  |
|-----------|-------------------------|---|-------|
| $V_{ESD}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±2000 |
|           |                         | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±500  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Power-On Hours (POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

| OPERATING CONDITION             | POWER-ON HOURS [POH]<br>(hours) |
|---------------------------------|---------------------------------|
| $T_A$ up to 85°C <sup>(1)</sup> | 87,600                          |

- (1) The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

### 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                      |   |                          |  | MIN                | TYP | MAX | UNIT      |
|----------------------|---|--------------------------|--|--------------------|-----|-----|-----------|
| Supply voltage       | $V_{BAT}$ , $V_{IO}$<br>(shorted to $V_{BAT}$ ) | Pins: 10, 37, 39, 44, 54 | Direct battery connection <sup>(3)</sup> | 2.1 <sup>(4)</sup> | 3.3 | 3.6 | V         |
| Ambient thermal slew |   |                          |  | -20                |     | 20  | °C/minute |

- (1) Operating temperature is limited by crystal frequency variation.
- (2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
- (3) To ensure WLAN performance, ripple on the supply must be less than ±300 mV.
- (4) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1 V, and care must be taken when operating at the minimum specified voltage.

## 7.5 Current Consumption Summary (CC3235S)

**Table 7-1. Current Consumption Summary (CC3235S) 2.4 GHz RF Band**

T<sub>A</sub> = 25°C, V<sub>BAT</sub> = 3.6 V

| PARAMETER                               |                          | TEST CONDITIONS <sup>(1) (2)</sup> |         | MIN                | TYP <sup>(3)</sup> | MAX  | UNIT |
|---|--------------------------|------------------------------------|---------|--------------------|--------------------|------|------|
| MCU ACTIVE                              | NWP ACTIVE               | TX                                 | 1 DSSS  | TX power level = 0 |                    | 272  | mA   |
|   |                          |                                    |         | TX power level = 4 |                    | 190  |      |
|   |                          |                                    | 6 OFDM  | TX power level = 0 |                    | 248  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 182  |      |
|   |                          |                                    | 54 OFDM | TX power level = 0 |                    | 223  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 160  |      |
|   |                          | RX                                 | 1 DSSS  |                    | 59                 |      |      |
|   |                          |                                    | 54 OFDM |                    | 59                 |      |      |
| NWP idle connected <sup>(4)</sup>       |                          |                                    |         |                    |                    | 15.3 |      |
| MCU SLEEP                               | NWP ACTIVE               | TX                                 | 1 DSSS  | TX power level = 0 |                    | 269  | mA   |
|   |                          |                                    |         | TX power level = 4 |                    | 187  |      |
|   |                          |                                    | 6 OFDM  | TX power level = 0 |                    | 245  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 179  |      |
|   |                          |                                    | 54 OFDM | TX power level = 0 |                    | 220  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 157  |      |
|   |                          | RX                                 | 1 DSSS  |                    | 56                 |      |      |
|   |                          |                                    | 54 OFDM |                    | 56                 |      |      |
| NWP idle connected <sup>(4)</sup>       |                          |                                    |         |                    |                    | 12.2 |      |
| MCU LPDS                                | NWP ACTIVE               | TX                                 | 1 DSSS  | TX power level = 0 |                    | 266  | mA   |
|   |                          |                                    |         | TX power level = 4 |                    | 184  |      |
|   |                          |                                    | 6 OFDM  | TX power level = 0 |                    | 242  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 176  |      |
|   |                          |                                    | 54 OFDM | TX power level = 0 |                    | 217  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 154  |      |
|   |                          | RX                                 | 1 DSSS  |                    | 53                 |      |      |
|   |                          |                                    | 54 OFDM |                    | 53                 |      |      |
| NWP LPDS <sup>(5)</sup>                 |                          | 120 µA at 64KB<br>135 µA at 256KB  |         |                    | 135                | µA   |      |
| NWP idle connected <sup>(4)</sup>       |                          |                                    |         |                    |                    | 710  |      |
| MCU SHUTDOWN                            | MCU shutdown             |                                    |         |                    | 1                  | µA   |      |
| MCU HIBERNATE                           | MCU hibernate            |                                    |         |                    | 4.5                | µA   |      |
| Peak calibration current <sup>(6)</sup> | V <sub>BAT</sub> = 3.6 V |                                    |         |                    | 420                | mA   |      |
|   | V <sub>BAT</sub> = 3.3 V |                                    |         |                    | 450                |      |      |
|   | V <sub>BAT</sub> = 2.1 V |                                    |         |                    | 670                |      |      |

- (1) TX power level = 0 implies maximum power (see [Figure 7-1](#), [Figure 7-2](#), and [Figure 7-3](#)). TX power level = 4 implies output power backed off approximately 4 dB.
- (2) The CC3235x system is a constant power-source system. The active current numbers scale based on the V<sub>BAT</sub> voltage supplied.
- (3) Typical numbers assume a VSWR of 1.5:1.
- (4) DTIM = 1
- (5) LPDS current does not include the external serial flash. The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3235x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.
- (6) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see [CC31xx, CC32xx SimpleLink™ Wi-Fi® and IoT Network Processor Programmer's Guide](#).

**Table 7-2. Current Consumption Summary (CC3235S) 5 GHz RF Band** $T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ 

| PARAMETER                               |                                   | TEST CONDITIONS <sup>(1) (2)</sup> |   | MIN  | TYP <sup>(3)</sup> | MAX | UNIT          |
|---|-----------------------------------|------------------------------------|---|------|--------------------|-----|---------------|
| MCU ACTIVE                              | NWP ACTIVE                        | TX                                 | 6 OFDM  |      | 318                |     | mA            |
|   |                                   |                                    | 54 OFDM   |      | 293                |     |               |
|   | RX                                | 54 OFDM                            |   | 67   |                    |     |               |
|   | NWP idle connected <sup>(4)</sup> |                                    |   | 15.3 |                    |     |               |
| MCU SLEEP                               | NWP ACTIVE                        | TX                                 | 6 OFDM  |      | 315                |     | mA            |
|   |                                   |                                    | 54 OFDM   |      | 290                |     |               |
|   | RX                                | 54 OFDM                            |   | 64   |                    |     |               |
|   | NWP idle connected <sup>(4)</sup> |                                    |   | 12.2 |                    |     |               |
| MCU LPDS                                | NWP ACTIVE                        | TX                                 | 6 OFDM  |      | 312                |     | mA            |
|   |                                   |                                    | 54 OFDM   |      | 287                |     |               |
|   |                                   | RX                                 | 54 OFDM   |      | 61                 |     |               |
|   | NWP LPDS <sup>(5)</sup>           |                                    | 120 $\mu\text{A}$ at 64KB<br>135 $\mu\text{A}$ at 256KB |      | 135                |     | $\mu\text{A}$ |
|   | NWP idle connected <sup>(4)</sup> |                                    |   | 710  |                    |     |               |
| MCU SHUTDOWN                            | MCU shutdown                      |                                    |   |      | 1                  |     | $\mu\text{A}$ |
| MCU HIBERNATE                           | MCU hibernate                     |                                    |   |      | 4.5                |     | $\mu\text{A}$ |
| Peak calibration current <sup>(6)</sup> | $V_{BAT} = 3.6\text{ V}$          |                                    |   |      | 290                |     | mA            |
|   | $V_{BAT} = 3.3\text{ V}$          |                                    |   |      | 310                |     |               |
|   | $V_{BAT} = 2.7\text{ V}$          |                                    |   |      | 310                |     |               |
|   | $V_{BAT} = 2.1\text{ V}$          |                                    |   |      | 400                |     |               |

(1) Measurements taken at maximum TX power

(2) The CC3235x system is a constant power-source system. The active current numbers scale based on the  $V_{BAT}$  voltage supplied.

(3) Typical numbers assume a VSWR of 1.5:1.

(4) DTIM = 1

(5) LPDS current does not include the external serial flash. The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3235x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4  $\mu\text{A}$ .(6) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see [CC31xx](#), [CC32xx SimpleLink™ Wi-Fi® and IoT Network Processor Programmer's Guide](#).

## 7.6 Current Consumption Summary (CC3235SF)

**Table 7-3. Current Consumption Summary (CC3235SF) 2.4 GHz RF Band**

T<sub>A</sub> = 25°C, V<sub>BAT</sub> = 3.6 V

| PARAMETER                               |                          | TEST CONDITIONS <sup>(1) (2)</sup> |         | MIN                | TYP <sup>(3)</sup> | MAX  | UNIT |
|---|--------------------------|------------------------------------|---------|--------------------|--------------------|------|------|
| MCU ACTIVE                              | NWP ACTIVE               | TX                                 | 1 DSSS  | TX power level = 0 |                    | 286  | mA   |
|   |                          |                                    |         | TX power level = 4 |                    | 202  |      |
|   |                          |                                    | 6 OFDM  | TX power level = 0 |                    | 255  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 192  |      |
|   |                          |                                    | 54 OFDM | TX power level = 0 |                    | 232  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 174  |      |
|   |                          | RX                                 | 1 DSSS  |                    | 74                 |      |      |
|   |                          |                                    | 54 OFDM |                    | 74                 |      |      |
| NWP idle connected <sup>(4)</sup>       |                          |                                    |         |                    |                    | 25.2 |      |
| MCU SLEEP                               | NWP ACTIVE               | TX                                 | 1 DSSS  | TX power level = 0 |                    | 282  | mA   |
|   |                          |                                    |         | TX power level = 4 |                    | 198  |      |
|   |                          |                                    | 6 OFDM  | TX power level = 0 |                    | 251  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 188  |      |
|   |                          |                                    | 54 OFDM | TX power level = 0 |                    | 228  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 170  |      |
|   |                          | RX                                 | 1 DSSS  |                    | 70                 |      |      |
|   |                          |                                    | 54 OFDM |                    | 70                 |      |      |
| NWP idle connected <sup>(4)</sup>       |                          |                                    |         |                    |                    | 21.2 |      |
| MCU LPDS                                | NWP active               | TX                                 | 1 DSSS  | TX power level = 0 |                    | 266  | mA   |
|   |                          |                                    |         | TX power level = 4 |                    | 184  |      |
|   |                          |                                    | 6 OFDM  | TX power level = 0 |                    | 242  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 176  |      |
|   |                          |                                    | 54 OFDM | TX power level = 0 |                    | 217  |      |
|   |                          |                                    |         | TX power level = 4 |                    | 154  |      |
|   |                          | RX                                 | 1 DSSS  |                    | 53                 |      |      |
|   |                          |                                    | 54 OFDM |                    | 53                 |      |      |
| NWP LPDS <sup>(5)</sup>                 |                          | 120 µA at 64KB<br>135 µA at 256KB  |         |                    | 135                | µA   |      |
| NWP idle connected <sup>(4)</sup>       |                          |                                    |         |                    |                    | 710  |      |
| MCU SHUTDOWN                            | MCU shutdown             |                                    |         |                    | 1                  | µA   |      |
| MCU HIBERNATE                           | MCU hibernate            |                                    |         |                    | 4.5                | µA   |      |
| Peak calibration current <sup>(6)</sup> | V <sub>BAT</sub> = 3.6 V |                                    |         |                    | 420                | mA   |      |
|   | V <sub>BAT</sub> = 3.3 V |                                    |         |                    | 450                |      |      |
|   | V <sub>BAT</sub> = 2.1 V |                                    |         |                    | 670                |      |      |

- (1) TX power level = 0 implies maximum power (see [Figure 7-1](#), [Figure 7-2](#), and [Figure 7-3](#)). TX power level = 4 implies output power backed off approximately 4 dB.
- (2) The CC3235x system is a constant power-source system. The active current numbers scale based on the V<sub>BAT</sub> voltage supplied.
- (3) Typical numbers assume a VSWR of 1.5:1.
- (4) DTIM = 1
- (5) LPDS current does not include the external serial flash. The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3235x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.

- (6) The complete calibration can take up to 17 mJ of energy from the battery over a period of 24 ms. Calibration is performed sparingly, typically when coming out of HIBERNATE and only if temperature has changed by more than 20°C. The calibration event can be controlled by a configuration file in the serial flash.

**Table 7-4. Current Consumption Summary (CC3235SF) 5 GHz RF Band**

T<sub>A</sub> = 25°C, V<sub>BAT</sub> = 3.6 V

| PARAMETER                               |                                   | TEST CONDITIONS <sup>(1) (2)</sup> |         | MIN                               | TYP <sup>(3)</sup> | MAX | UNIT |
|---|-----------------------------------|------------------------------------|---------|-----------------------------------|--------------------|-----|------|
| MCU ACTIVE                              | NWP ACTIVE                        | TX                                 | 6 OFDM  |                                   | 329                |     | mA   |
|   |                                   |                                    | 54 OFDM |                                   | 306                |     |      |
|   |                                   | RX                                 | 54 OFDM |                                   | 80                 |     |      |
|   | NWP idle connected <sup>(4)</sup> |                                    |         |                                   | 25.2               |     |      |
| MCU SLEEP                               | NWP ACTIVE                        | TX                                 | 6 OFDM  |                                   | 325                |     | mA   |
|   |                                   |                                    | 54 OFDM |                                   | 302                |     |      |
|   |                                   | RX                                 | 54 OFDM |                                   | 76                 |     |      |
|   | NWP idle connected <sup>(4)</sup> |                                    |         |                                   | 21.2               |     |      |
| MCU LPDS                                | NWP active                        | TX                                 | 6 OFDM  |                                   | 312                |     | mA   |
|   |                                   |                                    | 54 OFDM |                                   | 289                |     |      |
|   |                                   | RX                                 | 54 OFDM |                                   | 63                 |     |      |
|   | NWP LPDS <sup>(5)</sup>           |                                    |         | 120 µA at 64KB<br>135 µA at 256KB |                    | 135 |      |
| NWP idle connected <sup>(4)</sup>       |                                   |                                    |         |                                   | 710                |     |      |
| MCU SHUTDOWN                            | MCU shutdown                      |                                    |         |                                   | 1                  |     | µA   |
| MCU HIBERNATE                           | MCU hibernate                     |                                    |         |                                   | 4.5                |     | µA   |
| Peak calibration current <sup>(6)</sup> | V <sub>BAT</sub> = 3.6 V          |                                    |         |                                   | 290                |     | mA   |
|   | V <sub>BAT</sub> = 3.3 V          |                                    |         |                                   | 310                |     |      |
|   | V <sub>BAT</sub> = 2.7 V          |                                    |         |                                   | 310                |     |      |
|   | V <sub>BAT</sub> = 2.1 V          |                                    |         |                                   | 400                |     |      |

- (1) Measurements taken at maximum TX power  
 (2) The CC3235x system is a constant power-source system. The active current numbers scale based on the V<sub>BAT</sub> voltage supplied.  
 (3) Typical numbers assume a VSWR of 1.5:1.  
 (4) DTIM = 1  
 (5) LPDS current does not include the external serial flash. The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3235x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.  
 (6) The complete calibration can take up to 17 mJ of energy from the battery over a period of 24 ms. Calibration is performed sparingly, typically when coming out of HIBERNATE and only if temperature has changed by more than 20°C. The calibration event can be controlled by a configuration file in the serial flash.

### 7.7 TX Power Control for 2.4 GHz Band

The CC3235x has several options for modifying the output power of the device when required. For the 2.4 GHz band it is possible to lower the overall output power at a global level using the global TX power level setting. In addition, the 2.4 GHz band allows the user to enter additional back-offs<sup>2</sup>, per channel, region<sup>3</sup> and modulation rates<sup>4</sup>, via Image creator (see the [Uniflash with Image Creator User Guide](#) for more details).

Figure 7-1, Figure 7-2, and Figure 7-3 show TX power and IBAT versus TX power level settings for the CC3235S device at modulations of 1 DSSS, 6 OFDM, and 54 OFDM, respectively. For the CC3235SF device, the IBAT

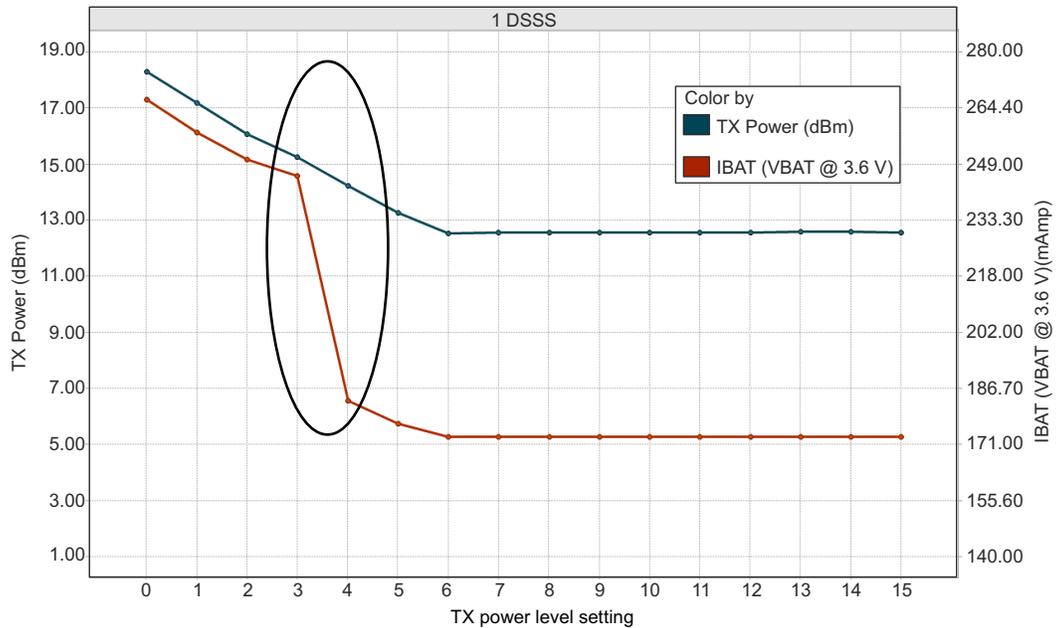
<sup>2</sup> The back-off range is between -6 dB to +6 dB in 0.25dB increments.

<sup>3</sup> FCC/ISED, ETSI (Europe), and Japan are supported.

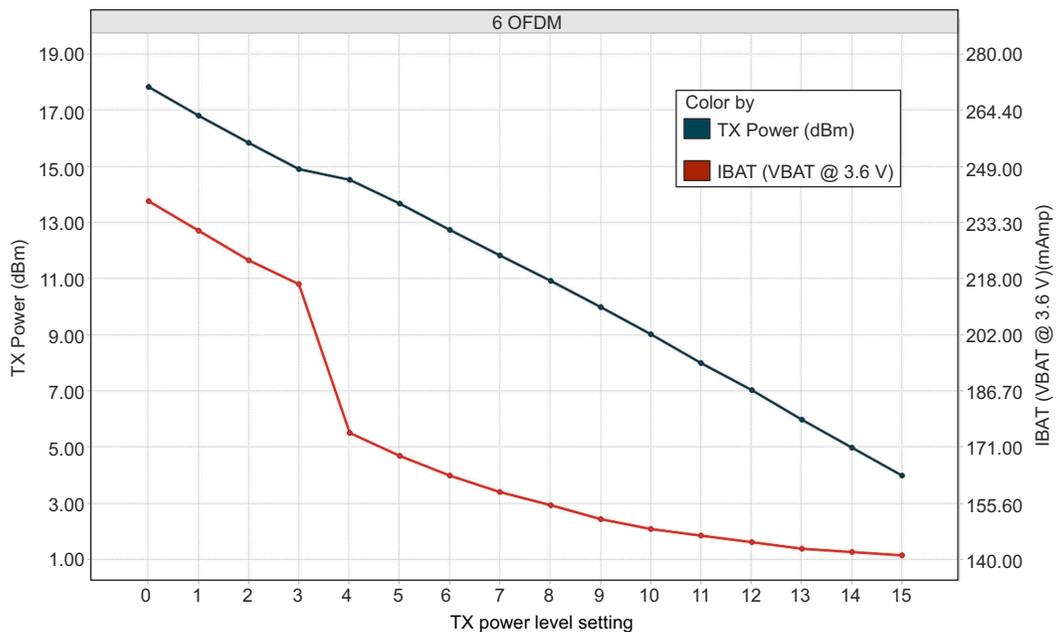
<sup>4</sup> Back-off rates are grouped into 11b rates, high modulation rates (MCS7, 54 OFDM and 48 OFDM), and lower modulation rates (all other rates).

current has an increase of approximately 10 mA to 15 mA depending on the transmitted rate. The TX power level will remain the same.

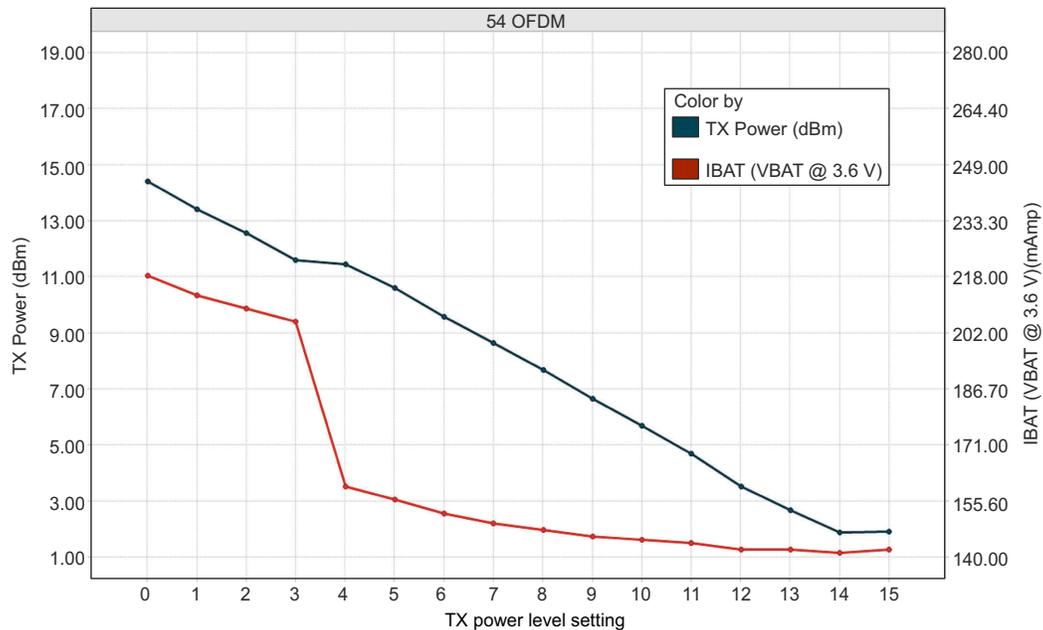
In Figure 7-1, the area enclosed in the circle represents a significant reduction in current during transition from TX power level 3 to level 4. In the case of lower range requirements (14-dBm output power), TI recommends using TX power level 4 to reduce the current.



**Figure 7-1. TX Power and IBAT vs TX Power Level Settings (1 DSSS)**



**Figure 7-2. TX Power and IBAT vs TX Power Level Settings (6 OFDM)**



**Figure 7-3. TX Power and IBAT vs TX Power Level Settings (54 OFDM)**

## 7.8 TX Power Control for 5 GHz

5 GHz power control is done via Image Creator where the maximum transmit power is provided <sup>5</sup>. Within Image Creator power control is possible per channel, region <sup>6</sup>, and modulation rates <sup>7</sup>. In addition, it is possible to enter an additional back-off <sup>8</sup> factor per channel and modulation rate for further margin to regulatory requirements.

Finally, it is also possible to set the TX and RX trace losses to the antenna per band <sup>9</sup>. The peak antenna gain <sup>10</sup> can also be provided, thus allowing further control. For a full description of options and capabilities see [Uniflash with Image Creator User Guide](#).

<sup>5</sup> The maximum transmit power range is 18dBm to 0.125dBm in 0.125dBm decrements.

<sup>6</sup> FCC/ISED, ETSI (Europe), and Japan are supported.

<sup>7</sup> Rates are grouped into high modulation rates (MCS7, 54 OFDM and 48 OFDM) and lower modulation rates (all other rates).

<sup>8</sup> The back-off range is 0 dBm to 18 dBm in 0.125 dBm increments, with the maximum back-off not exceed that of the maximum transmit power.

<sup>9</sup> The range of losses if from 0 dBm to 7.75 dBm in 0.125 dBm increments.

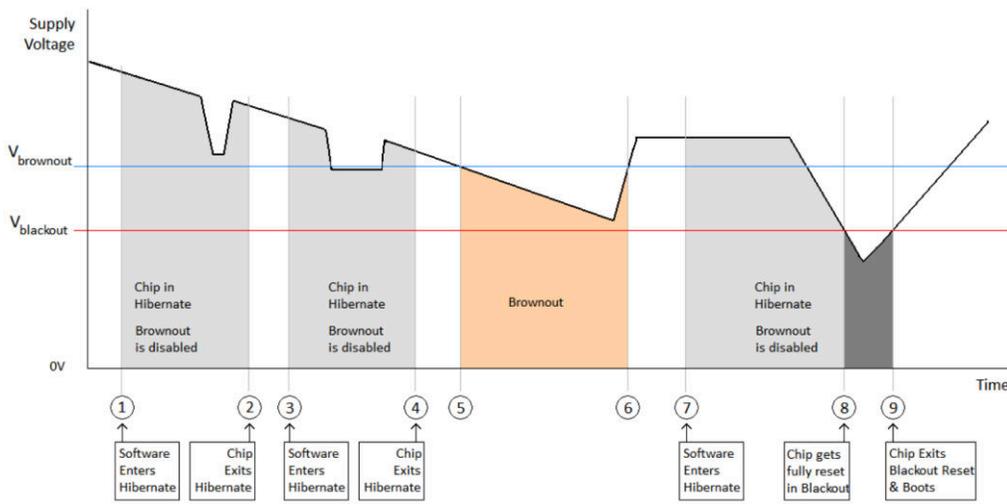
<sup>10</sup> The antenna gain has a range of -2 dBi to 5.75 dBi in 0.125 dBi increments.

### 7.9 Brownout and Blackout Conditions

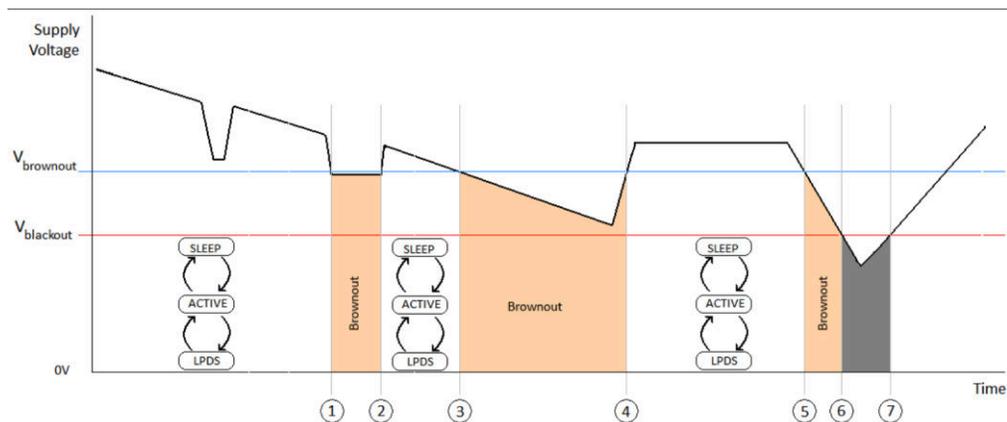
The device enters a brownout condition when the input voltage drops below  $V_{\text{brownout}}$  (see Figure 7-4 and Figure 7-5). This condition must be considered during design of the power supply routing, especially when operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout condition. The resistance includes the internal resistance of the battery, the contact resistance of the battery holder (four contacts for 2x AA batteries), and the wiring and PCB routing resistance.

**Note**

When the device is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.



**Figure 7-4. Brownout and Blackout Levels (1 of 2)**



**Figure 7-5. Brownout and Blackout Levels (2 of 2)**

In the brownout condition, all sections of the device (including the 32-kHz RTC) shut down except for the Hibernate module, which remains on. The current in this state can reach approximately 400  $\mu$ A. The blackout condition is equivalent to a hardware reset event in which all states within the device are lost.

Table 7-5 lists the brownout and blackout voltage levels.

**Table 7-5. Brownout and Blackout Voltage Levels**

| CONDITION             | VOLTAGE LEVEL | UNIT |
|-----------------------|---------------|------|
| V <sub>brownout</sub> | 2.1           | V    |
| V <sub>blackout</sub> | 1.67          | V    |

## 7.10 Electrical Characteristics for GPIO Pins

**Table 7-6. Electrical Characteristics: GPIO Pins Except 50, 52, and 53**

T<sub>A</sub> = 25°C, V<sub>BAT</sub> = 2.1 V to 3.3 V.<sup>(1)</sup>

| PARAMETER       |                           | TEST CONDITIONS  | MIN                    | TYP | MAX                     | UNIT |
|-----------------|---------------------------|--|------------------------|-----|-------------------------|------|
| C <sub>IN</sub> | Pin capacitance           |  |                        | 4   |                         | pF   |
| V <sub>IH</sub> | High-level input voltage  |  | 0.65 × V <sub>DD</sub> |     | V <sub>DD</sub> + 0.5 V | V    |
| V <sub>IL</sub> | Low-level input voltage   |  | -0.5                   |     | 0.35 × V <sub>DD</sub>  | V    |
| I <sub>IH</sub> | High-level input current  |  |                        | 5   |                         | nA   |
| I <sub>IL</sub> | Low-level input current   |  |                        | 5   |                         | nA   |
| V <sub>OH</sub> | High-level output voltage | IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V <sub>DD</sub> < 3.6 V |                        |     | V <sub>DD</sub> × 0.8   | V    |
|                 |                           | IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V <sub>DD</sub> < 3.6 V |                        |     | V <sub>DD</sub> × 0.7   |      |
|                 |                           | IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V <sub>DD</sub> < 3.6 V |                        |     | V <sub>DD</sub> × 0.7   |      |
|                 |                           | IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V <sub>DD</sub> < 2.4 V |                        |     | V <sub>DD</sub> × 0.75  |      |
| V <sub>OL</sub> | Low-level output voltage  | IL = 2 mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V <sub>DD</sub> < 3.6 V | V <sub>DD</sub> × 0.2  |     |                         | V    |
|                 |                           | IL = 4 mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V <sub>DD</sub> < 3.6 V | V <sub>DD</sub> × 0.2  |     |                         |      |
|                 |                           | IL = 6 mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V <sub>DD</sub> < 3.6 V | V <sub>DD</sub> × 0.2  |     |                         |      |
|                 |                           | IL = 2 mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V <sub>DD</sub> < 2.4 V | V <sub>DD</sub> × 0.25 |     |                         |      |
| I <sub>OH</sub> | High-level source current | 2-mA drive   | 2                      |     |                         | mA   |
|                 |                           | 4-mA drive   | 4                      |     |                         |      |
|                 |                           | 6-mA drive   | 6                      |     |                         |      |
| I <sub>OL</sub> | Low-level sink current    | 2-mA drive   | 2                      |     |                         | mA   |
|                 |                           | 4-mA drive   | 4                      |     |                         |      |
|                 |                           | 6-mA drive   | 6                      |     |                         |      |

- (1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

**Table 7-7. Electrical Characteristics: GPIO Pins 50, 52, and 53**
 $T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 2.1\text{ V to }3.6\text{ V}$ .<sup>(1)</sup>

| PARAMETER |   | TEST CONDITIONS  | MIN                  | TYP                  | MAX                     | UNIT |
|-----------|---|--|----------------------|----------------------|-------------------------|------|
| $C_{IN}$  | Pin capacitance                           |  |                      | 7                    |                         | pF   |
| $V_{IH}$  | High-level input voltage                  |  | $0.65 \times V_{DD}$ |                      | $V_{DD} + 0.5\text{ V}$ | V    |
| $V_{IL}$  | Low-level input voltage                   |  | -0.5                 |                      | $0.35 \times V_{DD}$    | V    |
| $I_{IH}$  | High-level input current                  |  |                      | 50                   |                         | nA   |
| $I_{IL}$  | Low-level input current                   |  |                      | 50                   |                         | nA   |
| $V_{OH}$  | High-level output voltage                 | IL = 2 mA; configured I/O drive strength = 2 mA; $2.4\text{ V} \leq V_{DD} < 3.6\text{ V}$ |                      |                      | $V_{DD} \times 0.8$     | V    |
|           |   | IL = 4 mA; configured I/O drive strength = 4 mA; $2.4\text{ V} \leq V_{DD} < 3.6\text{ V}$ |                      |                      | $V_{DD} \times 0.7$     |      |
|           |   | IL = 6 mA; configured I/O drive strength = 6 mA; $2.4\text{ V} \leq V_{DD} < 3.6\text{ V}$ |                      |                      | $V_{DD} \times 0.7$     |      |
|           |   | IL = 2 mA; configured I/O drive strength = 2 mA; $2.1\text{ V} \leq V_{DD} < 2.4\text{ V}$ |                      |                      | $V_{DD} \times 0.75$    |      |
| $V_{OL}$  | Low-level output voltage                  | IL = 2 mA; configured I/O drive strength = 2 mA; $2.4\text{ V} \leq V_{DD} < 3.6\text{ V}$ |                      | $V_{DD} \times 0.2$  |                         | V    |
|           |   | IL = 4 mA; configured I/O drive strength = 4 mA; $2.4\text{ V} \leq V_{DD} < 3.6\text{ V}$ |                      | $V_{DD} \times 0.2$  |                         |      |
|           |   | IL = 6 mA; configured I/O drive strength = 6 mA; $2.4\text{ V} \leq V_{DD} < 3.6\text{ V}$ |                      | $V_{DD} \times 0.2$  |                         |      |
|           |   | IL = 2 mA; configured I/O drive strength = 2 mA; $2.1\text{ V} \leq V_{DD} < 2.4\text{ V}$ |                      | $V_{DD} \times 0.25$ |                         |      |
| $I_{OH}$  | High-level source current, $V_{OH} = 2.4$ | 2-mA drive   |                      | 1.5                  |                         | mA   |
|           |   | 4-mA drive   |                      | 2.5                  |                         |      |
|           |   | 6-mA drive   |                      | 3.5                  |                         |      |
| $I_{OL}$  | Low-level sink current                    | 2-mA drive   |                      | 1.5                  |                         | mA   |
|           |   | 4-mA drive   |                      | 2.5                  |                         |      |
|           |   | 6-mA drive   |                      | 3.5                  |                         |      |
| $V_{IL}$  | nRESET                                    |  |                      | 0.6                  |                         | V    |

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6 mA.

## 7.11 Electrical Characteristics for Pin Internal Pullup and Pulldown

$T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 3.0\text{ V}$ .

| PARAMETER | TEST CONDITIONS  | MIN | TYP | MAX | UNIT          |
|-----------|--|-----|-----|-----|---------------|
| $I_{OH}$  | Pullup current, $V_{OH} = 2.4$ ( $V_{DD} = 3.0\text{ V}$ )   | 5   |     | 10  | $\mu\text{A}$ |
| $I_{OL}$  | Pulldown current, $V_{OL} = 0.4$ ( $V_{DD} = 3.0\text{ V}$ ) | 5   |     |     | $\mu\text{A}$ |

## 7.12 WLAN Receiver Characteristics

**Table 7-8. WLAN Receiver Characteristics: 2.4 GHz Band**

$T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 2.1\text{ V}$  to  $3.6\text{ V}$ . Parameters are measured at the SoC pin on channel 6 (2437 MHz).

| PARAMETER   | TEST CONDITIONS (Mbps)   | MIN | TYP   | MAX | UNIT |
|---|--------------------------|-----|-------|-----|------|
| Sensitivity<br>(8% PER for 11b rates, 10% PER for 11g/11n rates) <sup>(1)</sup> | 1 DSSS                   |     | -96.0 |     | dBm  |
|   | 2 DSSS                   |     | -94.0 |     |      |
|   | 11 CCK                   |     | -88.0 |     |      |
|   | 6 OFDM                   |     | -90.5 |     |      |
|   | 9 OFDM                   |     | -90.0 |     |      |
|   | 18 OFDM                  |     | -86.5 |     |      |
|   | 36 OFDM                  |     | -80.5 |     |      |
|   | 54 OFDM                  |     | -74.5 |     |      |
|   | MCS7 (GF) <sup>(2)</sup> |     | -71.5 |     |      |
| Maximum input level<br>(10% PER)  | 802.11b                  |     | -4.0  |     | dBm  |
|   | 802.11g                  |     | -10.0 |     |      |

(1) Sensitivity is 1-dB worse on channel 13 (2472 MHz).

(2) Sensitivity for mixed mode is 1-dB worse.

**Table 7-9. WLAN Receiver Characteristics: 5 GHz Band**

$T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 2.1\text{ V}$  to  $3.6\text{ V}$ . Parameters measured at SoC pin are the average of channels 40, 56, 120, and 157.

| PARAMETER                                  | TEST CONDITIONS (Mbps)   | MIN | TYP   | MAX | UNIT |
|--|--------------------------|-----|-------|-----|------|
| Sensitivity<br>(10% PER for 11g/11n rates) | 6 OFDM                   |     | -92.0 |     | dBm  |
|  | 9 OFDM                   |     | -91.0 |     |      |
|  | 18 OFDM                  |     | -88.0 |     |      |
|  | 36 OFDM                  |     | -81.5 |     |      |
|  | 54 OFDM                  |     | -75.0 |     |      |
|  | MCS7 (GF) <sup>(1)</sup> |     | -71.0 |     |      |
| Maximum input level                        | 802.11a                  |     | -20   |     | dBm  |

(1) Sensitivity for mixed mode is 1-dB worse.

## 7.13 WLAN Transmitter Characteristics

**Table 7-10. WLAN Transmitter Characteristics: 2.4 GHz Band**

$T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 2.1\text{ V to }3.6\text{ V}$ . Parameters measured at SoC pin on channel 6 (2437 MHz).<sup>(1) (2)</sup>

| PARAMETER  | TEST CONDITIONS | MIN  | TYP  | MAX  | UNIT |
|--|-----------------|------|------|------|------|
| Operating frequency range <sup>(3) (4)</sup>                             |                 | 2412 |      | 2472 | MHz  |
| Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM | 1 DSSS          |      | 18.0 |      | dBm  |
|  | 2 DSSS          |      | 18.0 |      |      |
|  | 11 CCK          |      | 18.3 |      |      |
|  | 6 OFDM          |      | 17.3 |      |      |
|  | 9 OFDM          |      | 17.3 |      |      |
|  | 18 OFDM         |      | 17.0 |      |      |
|  | 36 OFDM         |      | 16.0 |      |      |
|  | 54 OFDM         |      | 14.5 |      |      |
|  | MCS7            |      | 13.0 |      |      |
| Transmit center frequency accuracy                                       |                 | -25  |      | 25   | ppm  |

- (1) The OFDM and MCS7 edge channels (2412 and 2462 MHz) have reduced TX power to meet FCC emission limits.
- (2) Power of 802.11b rates are reduced to meet ETSI requirements in Europe.
- (3) Channels 1 (2142 MHz) through 11 (2462 MHz) are supported for FCC.
- (4) Channels 1 (2142 MHz) through 13 (2472MHz) are supported for Europe and Japan. Note that channel 14 is not supported for Japan.

**Table 7-11. WLAN Transmitter Characteristics: 5 GHz Band**

$T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 2.1\text{ V to }3.6\text{ V}$ .<sup>(1)</sup> Parameters measured at SoC pin are the average of channels 40, 56, 120, and 157.<sup>(2)</sup>

| PARAMETER  | TEST CONDITIONS | MIN  | TYP  | MAX  | UNIT |
|--|-----------------|------|------|------|------|
| Operating frequency range <sup>(3) (4) (5)</sup>                         |                 | 5180 |      | 5825 | MHz  |
| Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM | 6 OFDM          |      | 18.1 |      | dBm  |
|  | 9 OFDM          |      | 18.1 |      |      |
|  | 18 OFDM         |      | 18.1 |      |      |
|  | 36 OFDM         |      | 16.6 |      |      |
|  | 54 OFDM         |      | 15.0 |      |      |
|  | MCS7            |      | 14.0 |      |      |
| Transmit center frequency accuracy                                       |                 | -20  |      | 20   | ppm  |

- (1) Transmit power will be reduced by 1.5dB for  $V_{BAT} < 2.8\text{V}$
- (2) FCC, Europe, and Japan channel power limits per modulation rates can be found in the [Uniflash with Image Creator User Guide](#).
- (3) FCC band covers U-NII-1, U-NII-2A, U-NII-2C, and U-NII-3 20-MHz BW modulations.
- (4) Europe bands 1, 2 and 3, 20-MHz BW modulations are supported.
- (5) For Japan, W52, W53 and W56, 20-MHz BW modulations are supported.

### 7.14 WLAN Transmitter Out-of-Band Emissions

Both the 2.4 GHz and the 5 GHz RF paths require an external band-pass filter to meet the various emission standards, including FCC. [Table 7-12](#) and [Table 7-13](#) presents the minimum attenuation requirements for the 2.4 GHz and 5 GHz band-pass filter, respectively. TI recommends using the same filter, switch, diplexer, and so on, used in the reference design to ease the process of certification.

**Table 7-12. WLAN 2.4 GHz Filter Requirements**

| PARAMETER                     | FREQUENCY (MHz) | MIN | TYP | MAX | UNIT |
|-------------------------------|-----------------|-----|-----|-----|------|
| Return loss                   | 2412 to 2484    | 10  |     |     | dB   |
| Insertion loss <sup>(1)</sup> | 2412 to 2484    |     | 1   | 1.5 | dB   |
| Attenuation                   | 804 to 828      | 30  | 42  |     | dB   |
|                               | 1608 to 1656    | 20  | 23  |     |      |
|                               | 3216 to 3312    | 30  | 49  |     |      |
|                               | 4020 to 4140    | 40  | 52  |     |      |
|                               | 4824 to 4968    | 20  | 30  |     |      |
|                               | 5628 to 5796    | 20  | 27  |     |      |
|                               | 6432 to 6624    | 20  | 42  |     |      |
|                               | 7200 to 7500    | 35  | 44  |     |      |
|                               | 7500 to 10000   | 20  | 30  |     |      |
| Reference impedance           | 2412 to 2484    |     | 50  |     | Ω    |
| Filter type                   | Bandpass        |     |     |     |      |

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

**Table 7-13. WLAN 5 GHz Filter Requirements**

| PARAMETER                     | FREQUENCY (MHz) | MIN | TYP | MAX | UNIT |
|-------------------------------|-----------------|-----|-----|-----|------|
| Return loss                   | 5150 to 5925    | 10  |     |     | dB   |
| Insertion loss <sup>(1)</sup> | 5150 to 5925    |     | 1   | 2   | dB   |
| Attenuation                   | 600 to 2700     | 41  | 42  |     | dB   |
|                               | 2950 to 3850    | 27  | 31  |     |      |
|                               | 4400 to 4600    | 20  | 27  |     |      |
|                               | 6600 to 6900    | 20  | 28  |     |      |
|                               | 7000 to 7775    | 20  | 27  |     |      |
|                               | 10300 to 11850  | 25  | 37  |     |      |
| Reference impedance           | 5150 to 5925    |     | 50  |     | Ω    |
| Filter type                   | Bandpass        |     |     |     |      |

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

## 7.15 BLE/2.4 GHz Radio Coexistence and WLAN Coexistence Requirements

For proper BLE/2.4 GHz radio coexistence, the following requirements needs to met:

**Table 7-14. COEX Isolation Requirement**

| PARAMETER              | Band                       | MIN               | TYP | MAX | UNIT |
|------------------------|----------------------------|-------------------|-----|-----|------|
| Port-to-port isolation | Single antenna             | 20 <sup>(1)</sup> |     |     | dB   |
|                        | Dual antenna Configuration | 20 <sup>(2)</sup> |     |     |      |

(1) WLAN/BLE switch used must provide a minimum of 20 dB isolation between ports.

(2) For dual antenna configuration antenna placement must be such that isolation between the BLE and WLAN ports is at least 20 dB.

## 7.16 Thermal Resistance Characteristics for RGK Package

| THERMAL METRICS <sup>(1)</sup> |                         | °C/W <sup>(2) (3)</sup> | AIR FLOW (m/s) <sup>(4)</sup> |
|--------------------------------|-------------------------|-------------------------|-------------------------------|
| RO <sub>JC</sub>               | Junction-to-case        | 6.3                     | 0.0051                        |
| RO <sub>JB</sub>               | Junction-to-board       | 2.4                     | 0.0051                        |
| RO <sub>JA</sub>               | Junction-to-free air    | 23                      | 0.0051                        |
| RO <sub>JMA</sub>              | Junction-to-moving air  | 14.6                    | 0.765                         |
|                                |                         | 12.4                    | 1.275                         |
|                                |                         | 10.8                    | 2.55                          |
| Psi <sub>JT</sub>              | Junction-to-package top | 0.2                     | 0.0051                        |
|                                |                         | 0.2                     | 0.765                         |
|                                |                         | 0.3                     | 1.275                         |
|                                |                         | 0.1                     | 2.55                          |
| Psi <sub>JB</sub>              | Junction-to-board       | 2.3                     | 0.0051                        |
|                                |                         | 2.3                     | 0.765                         |
|                                |                         | 2.2                     | 1.275                         |
|                                |                         | 2.4                     | 2.55                          |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) °C/W = degrees Celsius per watt.

(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RO<sub>JC</sub>] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

(4) m/s = meters per second.

## 7.17 Timing and Switching Characteristics

### 7.17.1 Power Supply Sequencing

For proper operation of the CC3235x device, perform the recommended power-up sequencing as follows:

1. Tie the following pins together on the board:
  - V<sub>BAT</sub> (pins 37, 39, and 44)
  - V<sub>IO</sub> (pins 54 and 10)
2. Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100K ||, 0.01µF, RC = 1ms).
3. For an external RTC, ensure that the clock is stable before RESET is deasserted (high).

For timing diagrams, see [Section 7.17.3](#).

### 7.17.2 Device Reset

When a device restart is required, the user may issue a negative pulse to the nRESET pin. The user must follow one of the following alternatives to ensure the reset is properly applied:

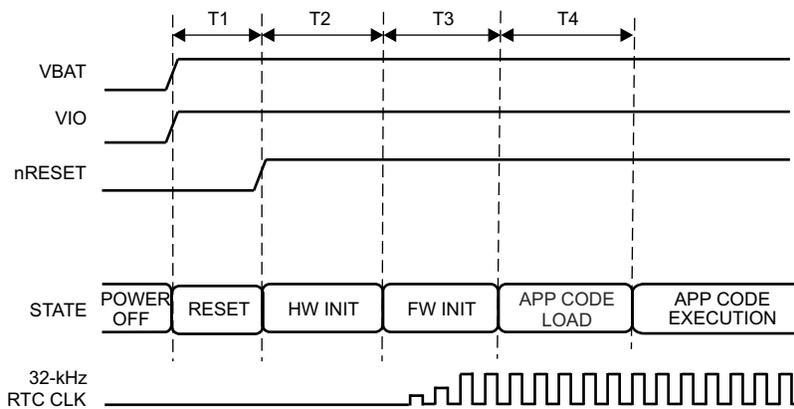
- A negative reset pulse (on pin 32) of at least 200ms duration
- If the 200ms pulse duration cannot be ensured, a pulldown resistor of 2MΩ must be connected to pin 52 (RTC\_XTAL\_N). If implemented, a shorter pulse of at least 100μs can be used.

To ensure a proper reset sequence, the user must call the sl\_stop function prior to toggling the reset. When a reset is required, it is preferable to use the software reset instead of an external trigger.

### 7.17.3 Reset Timing

#### 7.17.3.1 nRESET (32kHz Crystal)

Figure 7-6 shows the reset timing diagram for the 32kHz crystal first-time power-up and reset removal.



**Figure 7-6. First-Time Power-Up and Reset Removal Timing Diagram (32kHz Crystal)**

Table 7-15 describes the timing requirements for the 32kHz clock crystal first-time power-up and reset removal.

**Table 7-15. First-Time Power-Up and Reset Removal Timing Requirements (32kHz Crystal)**

| ITEM | NAME  | DESCRIPTION  | MIN                       | NOM | MAX | UNIT |
|------|---|--|---------------------------|-----|-----|------|
| T1   | nReset timing                                     | nReset timing after VBAT and VIO supply are stable |                           | 1   |     | ms   |
| T2   | Hardware wake-up time                             |  |                           | 25  |     | ms   |
| T3   | Time taken by ROM firmware to initialize hardware | Includes 32.768kHz XOSC settling time              |                           | 1.1 |     | s    |
| T4   | App code load time for CC3235S                    | CC3235S  | Image size (KB) × 1.7 ms  |     |     |      |
|      | App code integrity check time for CC3235SF        | CC3235SF   | Image size (KB) × 0.06 ms |     |     |      |

### 7.17.3.2 nRESET (External 32kHz Clock)

Figure 7-7 shows the reset timing diagram for the external 32kHz clock first-time power-up and reset removal.

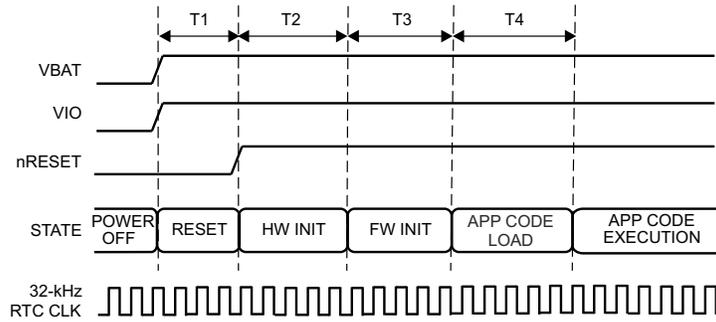


Figure 7-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32kHz Clock)

Table 7-16 describes the timing requirements for the external 32kHz clock first-time power-up and reset removal.

Table 7-16. First-Time Power-Up and Reset Removal Timing Requirements (External 32kHz Clock)

| ITEM | NAME  | DESCRIPTION  | MIN | NOM                      | MAX | UNIT |
|------|---|--|-----|--------------------------|-----|------|
| T1   | nReset time                                       | nReset timing after VBAT and VIO supply are stable |     | 1                        |     | ms   |
| T2   | Hardware wake-up time                             |  |     | 25                       |     | ms   |
| T3   | Time taken by ROM firmware to initialize hardware | CC3235S  |     | 10.3                     |     | ms   |
|      |   | CC3235SF   |     | 17.3                     |     |      |
| T4   | App code load time for CC3235R and CC3235S        | CC3235S  |     | Image size (KB) × 1.7ms  |     |      |
|      | App code integrity check time for CC3235SF        | CC3235SF   |     | Image size (KB) × 0.06ms |     |      |

### 7.17.4 Wakeup From HIBERNATE Mode

#### Note

The 32.768kHz crystal is enabled by default when the chip goes into HIBERNATE mode.

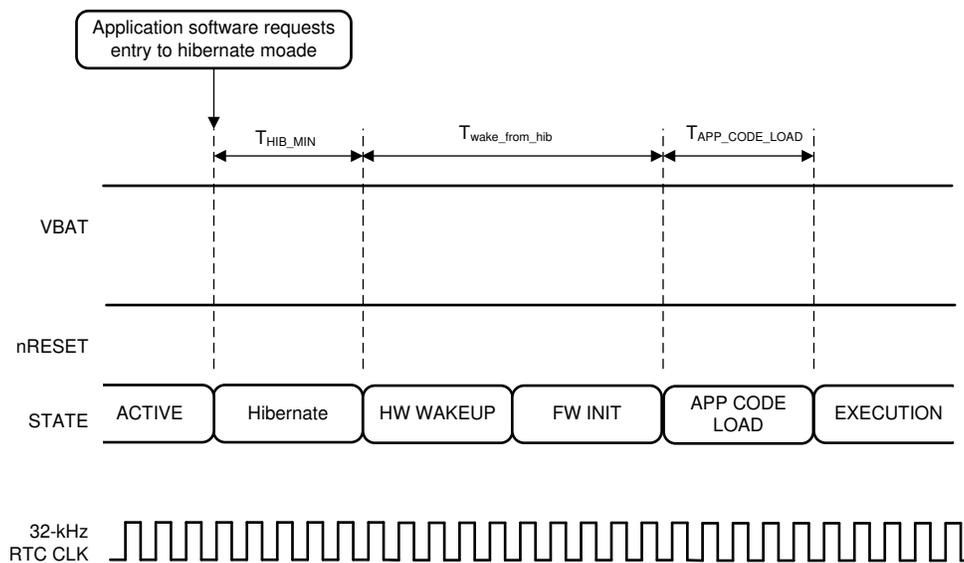
Table 7-17 lists the software hibernate timing requirements.

**Table 7-17. Software Hibernate Timing Requirements**

| ITEM                                      | NAME   | DESCRIPTION | MIN                      | TYP               | MAX | UNIT |
|---|--|-------------|--------------------------|-------------------|-----|------|
| T <sub>HIB_MIN</sub>                      | Minimum hibernate time                                 |             | 10                       |                   |     | ms   |
| T <sub>wake_from_hib</sub> <sup>(1)</sup> | Hardware wakeup time plus firmware initialization time |             |                          | 50 <sup>(2)</sup> |     | ms   |
| T <sub>APP_CODE_LOAD</sub>                | App code load time for CC3235S                         | CC3235S     | Image size (KB) × 1.7ms  |                   |     | ms   |
|   | App code load time for CC3235SF                        | CC3235SF    | Image size (KB) × 0.06ms |                   |     |      |

- (1) T<sub>wake\_from\_hib</sub> can be 200ms on rare occasions when calibration is performed. Calibration is performed sparingly, typically when exiting Hibernate and only if temperature has changed by more than 20°C or more than 24 hours have elapsed since a prior calibration.
- (2) Wake-up time can extend to 75ms if a patch is downloaded from the serial Flash.

Figure 7-8 shows the timing diagram for wakeup from HIBERNATE mode.



**Figure 7-8. Wakeup From HIBERNATE Timing Diagram**

### 7.17.5 Clock Specifications

The CC3235x device requires two separate clocks for operation:

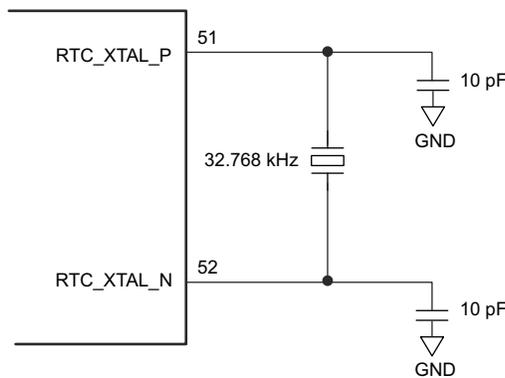
- A slow clock running at 32.768kHz is used for the RTC.
- A fast clock running at 40MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators that enable the use of less-expensive crystals rather than dedicated TCXOs for these clocks. The RTC can also be fed externally to provide reuse of an existing clock on the system and to reduce overall cost.

#### 7.17.5.1 Slow Clock Using Internal Oscillator

The RTC crystal connected to the device supplies the free-running slow clock. The accuracy of the slow clock frequency must be 32.768kHz ±150ppm. In this mode of operation, the crystal is tied between RTC\_XTAL\_P (pin 51) and RTC\_XTAL\_N (pin 52) with a suitable load capacitance to meet the ppm requirement.

Figure 7-9 shows the crystal connections for the slow clock.



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**Figure 7-9. RTC Crystal Connections**

Table 7-18 lists the RTC crystal requirements.

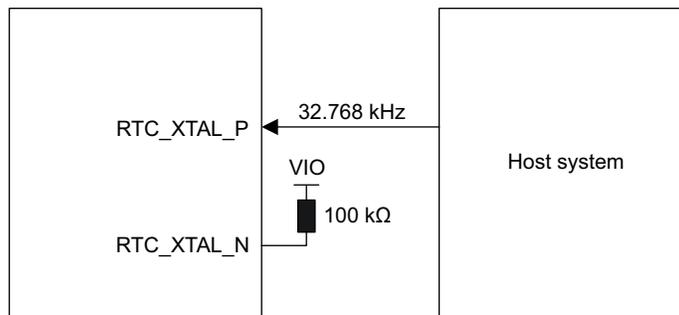
**Table 7-18. RTC Crystal Requirements**

| CHARACTERISTICS    | TEST CONDITIONS                     | MIN | TYP    | MAX  | UNIT |
|--------------------|-------------------------------------|-----|--------|------|------|
| Frequency          |                                     |     | 32.768 |      | kHz  |
| Frequency accuracy | Initial plus temperature plus aging |     |        | ±150 | ppm  |
| Crystal ESR        | 32.768kHz                           |     |        | 70   | kΩ   |

### 7.17.5.2 Slow Clock Using an External Clock

When an RTC oscillator is present in the system, the CC3235x device can accept this clock directly as an input. The clock is fed on the RTC\_XTAL\_P line, and the RTC\_XTAL\_N line is held to  $V_{IO}$ . The clock must be a CMOS-level clock compatible with  $V_{IO}$  fed to the device.

Figure 7-10 shows the external RTC input connection.



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**Figure 7-10. External RTC Input**

Table 7-19 lists the external RTC digital clock requirements.

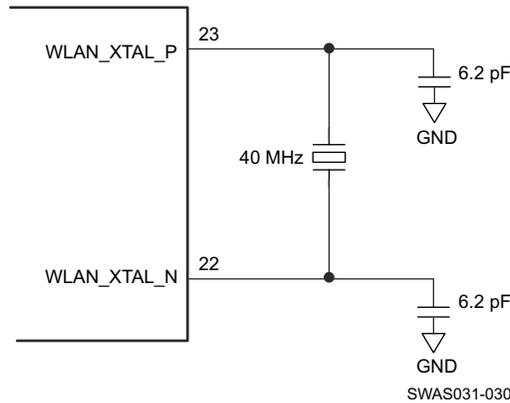
**Table 7-19. External RTC Digital Clock Requirements**

| CHARACTERISTICS   |   | TEST CONDITIONS         | MIN                  | TYP   | MAX                  | UNIT       |
|---|---|-------------------------|----------------------|-------|----------------------|------------|
| Frequency   |   |                         |                      | 32768 |                      | Hz         |
| Frequency accuracy<br>(Initial plus temperature plus aging) |   |                         |                      | ±150  |                      | ppm        |
| $t_r, t_f$  | Input transition time $t_r, t_f$ (10% to 90%) |                         |                      |       | 100                  | ns         |
| Frequency input duty cycle                                  |   |                         | 20%                  | 50%   | 80%                  |            |
| $V_{ih}$  | Slow clock input voltage limits               | Square wave, DC coupled | $0.65 \times V_{IO}$ |       | $V_{IO}$             | V          |
| $V_{il}$  |   |                         | 0                    |       | $0.35 \times V_{IO}$ | $V_{peak}$ |
| Input impedance   |   |                         | 1                    |       |                      | MΩ         |
|   |   |                         |                      |       | 5                    | pF         |

### 7.17.5.3 Fast Clock ( $F_{ref}$ ) Using an External Crystal

The CC3235x device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The crystal is fed directly between WLAN\_XTAL\_P (pin 23) and WLAN\_XTAL\_N (pin 22) with suitable loading capacitors.

Figure 7-11 shows the crystal connections for the fast clock.



- A. The crystal capacitance must be tuned to ensure that the PPM requirement is met. See [CC31xx & CC32xx Frequency Tuning](#) for information on frequency tuning.

**Figure 7-11. Fast Clock Crystal Connections**

Table 7-20 lists the WLAN fast-clock crystal requirements.

**Table 7-20. WLAN Fast-Clock Crystal Requirements**

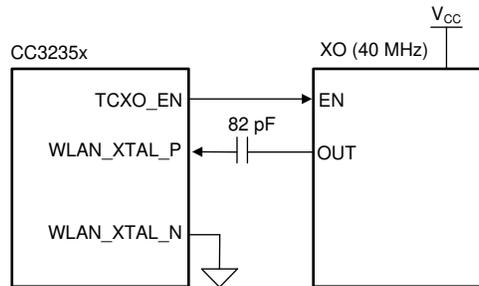
| CHARACTERISTICS    | TEST CONDITIONS                     | MIN | TYP | MAX | UNIT |
|--------------------|-------------------------------------|-----|-----|-----|------|
| Frequency          |                                     |     | 40  |     | MHz  |
| Frequency accuracy | Initial plus temperature plus aging |     |     | ±20 | ppm  |
| Crystal ESR        | 40MHz                               |     |     | 60  | Ω    |

### 7.17.5.4 Fast Clock (F<sub>ref</sub>) Using an External Oscillator

The CC3235x device can accept an external TCXO/XO for the 40MHz clock. In this mode of operation, the clock is connected to WLAN\_XTAL\_P (pin 23). WLAN\_XTAL\_N (pin 22) is connected to GND. The external TCXO/XO can be enabled by TCXO\_EN (pin 21) from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

Figure 7-12 shows the connection.



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**Figure 7-12. External TCXO Input**

Table 7-21 lists the external F<sub>ref</sub> clock requirements.

**Table 7-21. External F<sub>ref</sub> Clock Requirements (–40°C to +85°C)**

| CHARACTERISTICS  |                      | TEST CONDITIONS                       | MIN | TYP   | MAX    | UNIT            |
|--|----------------------|---------------------------------------|-----|-------|--------|-----------------|
| Frequency  |                      |                                       |     | 40.00 |        | MHz             |
| Frequency accuracy (initial plus temperature plus aging) |                      |                                       |     |       | ±20    | ppm             |
| Frequency input duty cycle                               |                      |                                       | 45% | 50%   | 55%    |                 |
| V <sub>pp</sub>  | Clock voltage limits | Sine or clipped sine wave, AC coupled | 0.7 |       | 1.2    | V <sub>pp</sub> |
| Phase noise at 40 MHz                                    |                      | at 1kHz                               |     |       | –125   | dBc/Hz          |
|  |                      | at 10kHz                              |     |       | –138.5 |                 |
|  |                      | at 100kHz                             |     |       | –143   |                 |
| Input impedance  | Resistance           |                                       | 12  |       |        | kΩ              |
|  | Capacitance          |                                       |     |       | 7      | pF              |

### 7.17.6 Peripherals Timing

This section describes the peripherals that are supported by the CC3235x device:

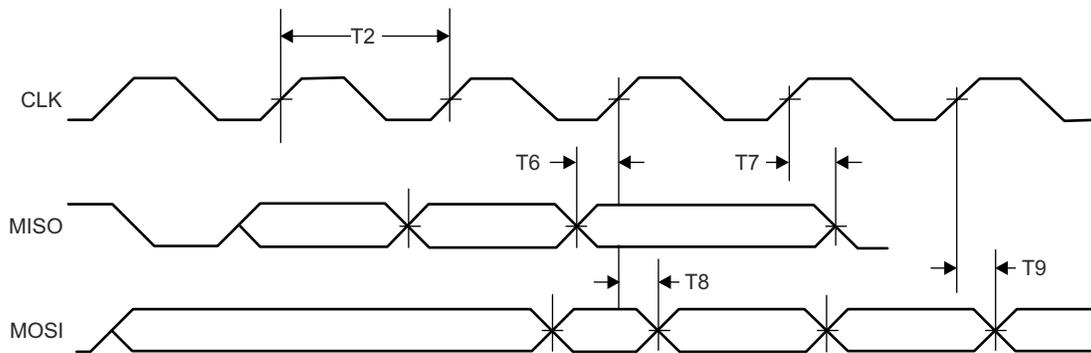
- SPI
- I<sup>2</sup>S
- GPIOs
- I<sup>2</sup>C
- IEEE 1149.1 JTAG
- ADC
- Camera Parallel Port
- UART
- SD Host
- Timers

#### 7.17.6.1 SPI

##### 7.17.6.1.1 SPI Master

The CC3235x microcontroller includes one SPI module that can be configured as a master or slave device. The SPI includes a serial clock with programmable frequency, polarity, and phase; a programmable timing control between chip select and external clock generation; and a programmable delay before the first SPI word is transmitted. Slave mode does not include a dead cycle between two successive words.

Figure 7-13 shows the timing diagram for the SPI master.



**Figure 7-13. SPI Master Timing Diagram**

Table 7-22 lists the timing parameters for the SPI master.

**Table 7-22. SPI Master Timing Parameters**

| PARAMETER NUMBER |                                 |                      | MIN  | MAX | UNIT |
|------------------|---------------------------------|----------------------|------|-----|------|
|                  | F <sup>(1)</sup>                | Clock frequency      |      | 30  | MHz  |
| T2               | T <sub>clk</sub> <sup>(1)</sup> | Clock period         | 33.3 |     | ns   |
|                  | D <sup>(1)</sup>                | Duty cycle           | 45%  | 55% |      |
| T6               | t <sub>IS</sub> <sup>(1)</sup>  | RX data setup time   | 1    |     | ns   |
| T7               | t <sub>IH</sub> <sup>(1)</sup>  | RX data hold time    | 2    |     | ns   |
| T8               | t <sub>OD</sub> <sup>(1)</sup>  | TX data output delay |      | 8.5 | ns   |
| T9               | t <sub>OH</sub> <sup>(1)</sup>  | TX data hold time    |      | 8   | ns   |

(1) Timing parameter assumes a maximum load of 20pF.

7.17.6.1.2 SPI Slave

Figure 7-14 shows the timing diagram for the SPI slave.

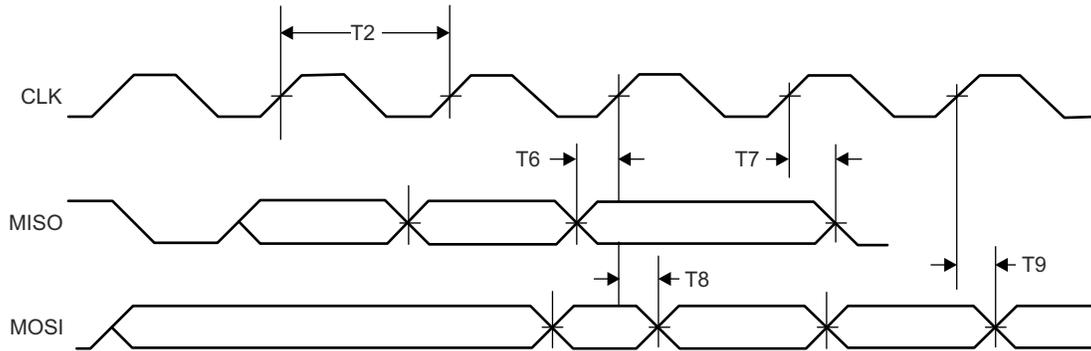


Figure 7-14. SPI Slave Timing Diagram

Table 7-23 lists the timing parameters for the SPI slave.

Table 7-23. SPI Slave Timing Parameters

| PARAMETER NUMBER |                                 |  | MIN | MAX | UNIT |
|------------------|---------------------------------|--|-----|-----|------|
|                  | F <sup>(1)</sup>                | Clock frequency at V <sub>BAT</sub> = 3.3V |     | 20  | MHz  |
|                  |                                 | Clock frequency at V <sub>BAT</sub> ≤ 2.1V |     | 12  |      |
| T2               | T <sub>clk</sub> <sup>(1)</sup> | Clock period                               | 50  |     | ns   |
|                  | D <sup>(1)</sup>                | Duty cycle                                 | 45% | 55% |      |
| T6               | t <sub>IS</sub> <sup>(1)</sup>  | RX data setup time                         | 4   |     | ns   |
| T7               | t <sub>IH</sub> <sup>(1)</sup>  | RX data hold time                          | 4   |     | ns   |
| T8               | t <sub>OD</sub> <sup>(1)</sup>  | TX data output delay                       |     | 20  | ns   |
| T9               | t <sub>OH</sub> <sup>(1)</sup>  | TX data hold time                          |     | 24  | ns   |

(1) Timing parameter assumes a maximum load of 20pF at 3.3V.

7.17.6.2 I<sup>2</sup>S

The McASP interface functions as a general-purpose audio serial port optimized for multichannel audio applications and supports transfer of two stereo channels over two data pins. The McASP consists of transmit and receive sections that operate synchronously and have programmable clock and frame-sync polarity. A fractional divider is available for bit-clock generation.

7.17.6.2.1 I<sup>2</sup>S Transmit Mode

Figure 7-15 shows the timing diagram for the I<sup>2</sup>S transmit mode.

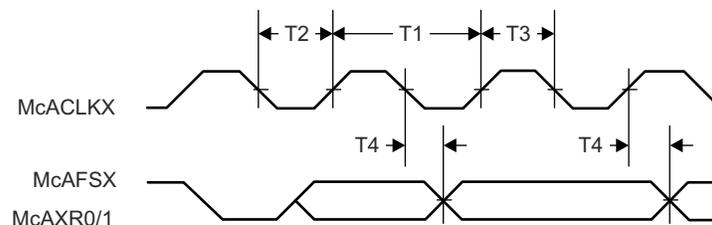


Figure 7-15. I<sup>2</sup>S Transmit Mode Timing Diagram

Table 7-24 lists the timing parameters for the I<sup>2</sup>S transmit mode.

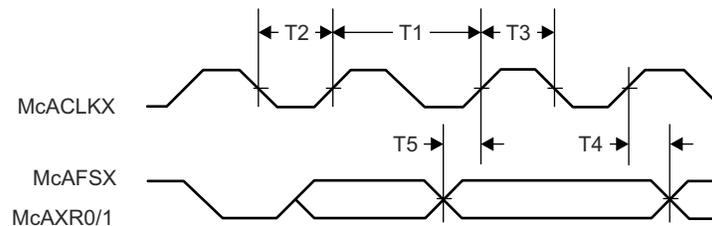
**Table 7-24. I<sup>2</sup>S Transmit Mode Timing Parameters**

| PARAMETER NUMBER |                                 |                   | MIN | MAX                  | UNIT |
|------------------|---------------------------------|-------------------|-----|----------------------|------|
| T1               | f <sub>clk</sub> <sup>(1)</sup> | Clock frequency   |     | 9.216                | MHz  |
| T2               | t <sup>LP</sup> <sup>(1)</sup>  | Clock low period  |     | 1/2 f <sub>clk</sub> | ns   |
| T3               | t <sup>HT</sup> <sup>(1)</sup>  | Clock high period |     | 1/2 f <sub>clk</sub> | ns   |
| T4               | t <sub>OH</sub> <sup>(1)</sup>  | TX data hold time |     | 22                   | ns   |

(1) Timing parameter assumes a maximum load of 20pF.

### 7.17.6.2.2 I<sup>2</sup>S Receive Mode

Figure 7-16 shows the timing diagram for the I<sup>2</sup>S receive mode.



**Figure 7-16. I<sup>2</sup>S Receive Mode Timing Diagram**

Table 7-25 lists the timing parameters for the I<sup>2</sup>S receive mode.

**Table 7-25. I<sup>2</sup>S Receive Mode Timing Parameters**

| PARAMETER NUMBER |                                 |                    | MIN | MAX                  | UNIT |
|------------------|---------------------------------|--------------------|-----|----------------------|------|
| T1               | f <sub>clk</sub> <sup>(1)</sup> | Clock frequency    |     | 9.216                | MHz  |
| T2               | t <sup>LP</sup> <sup>(1)</sup>  | Clock low period   |     | 1/2 f <sub>clk</sub> | ns   |
| T3               | t <sup>HT</sup> <sup>(1)</sup>  | Clock high period  |     | 1/2 f <sub>clk</sub> | ns   |
| T4               | t <sub>OH</sub> <sup>(1)</sup>  | RX data hold time  |     | 0                    | ns   |
| T5               | t <sub>OS</sub> <sup>(1)</sup>  | RX data setup time |     | 15                   | ns   |

(1) Timing parameter assumes a maximum load of 20pF.

### 7.17.6.3 GPIOs

All digital pins of the device can be used as general-purpose input/output (GPIO) pins. The GPIO module consists of four GPIO blocks, each of which provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used. Each GPIO has configurable pullup and pulldown strength (weak 10μA), configurable drive strength (2, 4, and 6mA), and open-drain enable.

#### Note

Unless otherwise stated, GPIO specifications also apply to pins configured as COEX IOs and network scripter interface

Figure 7-17 shows the GPIO timing diagram.

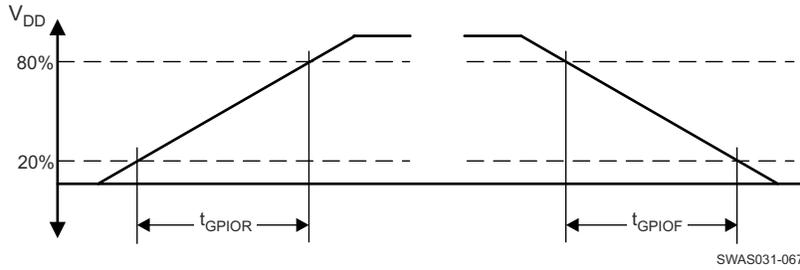


Figure 7-17. GPIO Timing Diagram

**7.17.6.3.1 GPIO Output Transition Time Parameters ( $V_{supply} = 3.3V$ )**

Table 7-26 lists the GPIO output transition times for  $V_{supply} = 3.3V$ .

**Table 7-26. GPIO Output Transition Times ( $V_{supply} = 3.3V$ ) (1) (2)**

| DRIVE STRENGTH (mA) | DRIVE STRENGTH CONTROL BITS | $t_r$ |     |      | $t_f$ |     |      | UNIT |
|---------------------|-----------------------------|-------|-----|------|-------|-----|------|------|
|                     |                             | MIN   | NOM | MAX  | MIN   | NOM | MAX  |      |
| 2 <sup>(3)</sup>    | 2MA_EN=1                    | 8.0   | 9.3 | 10.7 | 8.2   | 9.5 | 11.0 | ns   |
|                     | 4MA_EN=0                    |       |     |      |       |     |      |      |
| 4 <sup>(3)</sup>    | 2MA_EN=0                    | 6.6   | 7.1 | 7.6  | 4.7   | 5.2 | 5.8  | ns   |
|                     | 4MA_EN=1                    |       |     |      |       |     |      |      |
| 6                   | 2MA_EN=1                    | 3.2   | 3.5 | 3.7  | 2.3   | 2.6 | 2.9  | ns   |
|                     | 4MA_EN=1                    |       |     |      |       |     |      |      |

(1)  $V_{supply} = 3.3V$ ,  $T = 25^\circ C$ , total pin load = 30pF

(2) The transition data applies to the pins except the multiplexed analog-digital pins 29, 30, 45, 50, 52, and 53.

(3) The 2mA and 4mA drive strength does not apply to the COEX I/O pins. Pins configured as COEX lines are invariably driven at 6mA.

**7.17.6.3.2 GPIO Input Transition Time Parameters**

Table 7-27 lists the input transition time parameters.

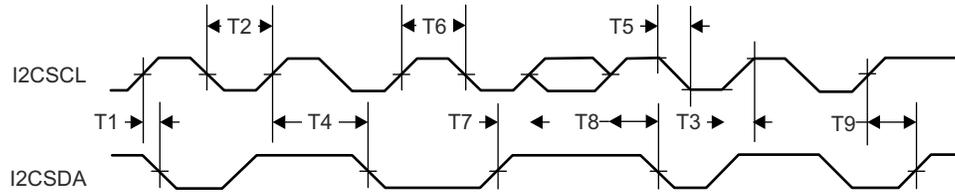
**Table 7-27. GPIO Input Transition Time Parameters**

|       |  | MIN | MAX | UNIT |
|-------|--|-----|-----|------|
| $t_r$ | Input transition time ( $t_r, t_f$ ), 10% to 90% | 1   | 3   | ns   |
| $t_f$ |  | 1   | 3   | ns   |

### 7.17.6.4 I<sup>2</sup>C

The CC3235x microcontroller includes one I<sup>2</sup>C module operating with standard (100kbps) or fast (400kbps) transmission speeds.

Figure 7-18 shows the I<sup>2</sup>C timing diagram.



**Figure 7-18. I<sup>2</sup>C Timing Diagram**

Table 7-28 lists the I<sup>2</sup>C timing parameters.

**Table 7-28. I<sup>2</sup>C Timing Parameters <sup>(1)</sup>**

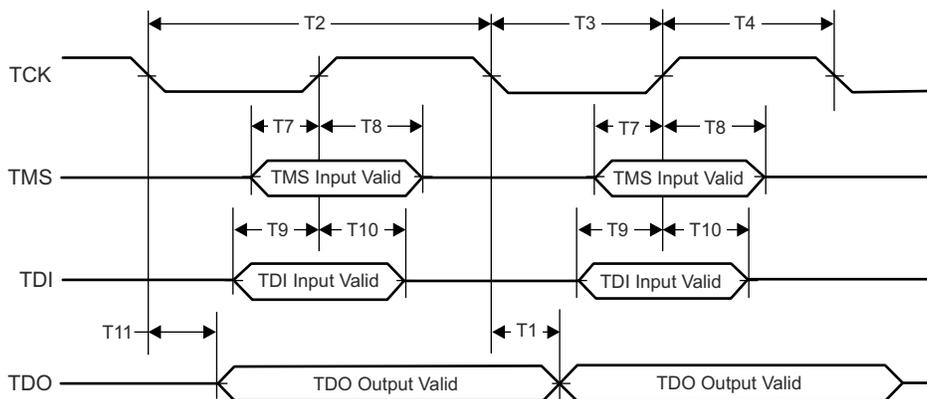
| PARAMETER NUMBER |                   |                            | MIN                | MAX                | UNIT         |
|------------------|-------------------|----------------------------|--------------------|--------------------|--------------|
| T2               | t <sub>LP</sub>   | Clock low period           | See <sup>(2)</sup> |                    | System clock |
| T3               | t <sub>SRT</sub>  | SCL/SDA rise time          |                    | See <sup>(3)</sup> | ns           |
| T4               | t <sub>DH</sub>   | Data hold time             | N/A                |                    |              |
| T5               | t <sub>SFT</sub>  | SCL/SDA fall time          | 3                  |                    | ns           |
| T6               | t <sub>HT</sub>   | Clock high time            | See <sup>(2)</sup> |                    | System clock |
| T7               | t <sub>DS</sub>   | Data setup time            | t <sub>LP</sub> /2 |                    | System clock |
| T8               | t <sub>SCSR</sub> | Start condition setup time | 36                 |                    | System clock |
| T9               | t <sub>SCS</sub>  | Stop condition setup time  | 24                 |                    | System clock |

- (1) All timing is with a 6mA drive and 20pF load.
- (2) This value depends on the value programmed in the clock period register of I<sup>2</sup>C. Maximum output frequency is the result of the minimal value programmed in this register.
- (3) Because I<sup>2</sup>C is an open-drain interface, the controller can drive logic 0 only. Logic is the result of an external pullup resistor. Rise time depends on the value of the external signal capacitance and external pullup register.

### 7.17.6.5 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1, *Test Access Port and Boundary-Scan Architecture*.

Figure 7-19 shows the JTAG timing diagram.



**Figure 7-19. JTAG Timing Diagram**

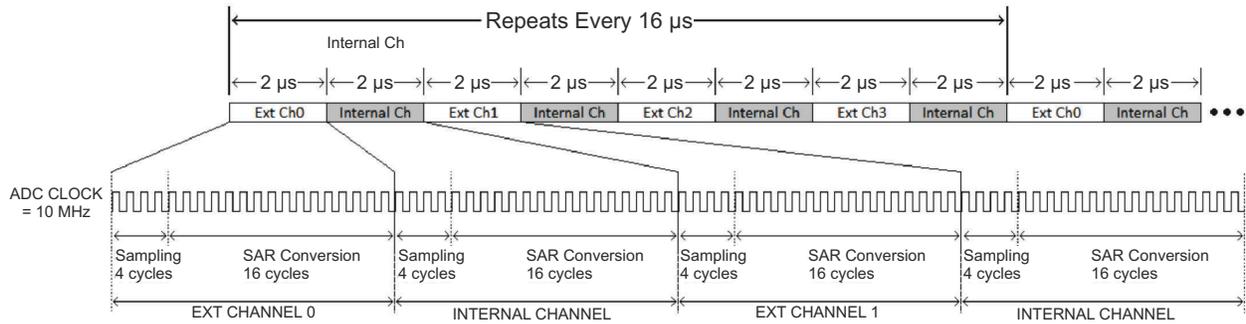
Table 7-29 lists the JTAG timing parameters.

**Table 7-29. JTAG Timing Parameters**

| PARAMETER NUMBER |               |                   | MIN | MAX           | UNIT |
|------------------|---------------|-------------------|-----|---------------|------|
| T1               | $f_{TCK}$     | Clock frequency   |     | 15            | MHz  |
| T2               | $t_{TCK}$     | Clock period      |     | $1 / f_{TCK}$ | ns   |
| T3               | $t_{CL}$      | Clock low period  |     | $t_{TCK} / 2$ | ns   |
| T4               | $t_{CH}$      | Clock high period |     | $t_{TCK} / 2$ | ns   |
| T7               | $t_{TMS\_SU}$ | TMS setup time    | 1   |               | ns   |
| T8               | $t_{TMS\_HO}$ | TMS hold time     | 16  |               | ns   |
| T9               | $t_{TDI\_SU}$ | TDI setup time    | 1   |               | ns   |
| T10              | $t_{TDI\_HO}$ | TDI hold time     | 16  |               | ns   |
| T11              | $t_{TDO\_HO}$ | TDO hold time     |     | 15            | ns   |

**7.17.6.6 ADC**

Figure 7-20 shows the ADC clock timing diagram.



**Figure 7-20. ADC Clock Timing Diagram**

Table 7-30 lists the ADC electrical specifications. See [CC32xx ADC Appnote](#) for further information on using the ADC and for application-specific examples.

**Table 7-30. ADC Electrical Specifications**

| PARAMETER                | DESCRIPTION                               | TEST CONDITIONS and ASSUMPTIONS  | MIN  | TYP   | MAX | UNIT |
|--------------------------|---|--|------|-------|-----|------|
| Nbits                    | Number of bits                            |  |      | 12    |     | Bits |
| INL                      | Integral nonlinearity                     | Worst-case deviation from histogram method over full scale (not including first and last three LSB levels) | -2.5 |       | 2.5 | LSB  |
| DNL                      | Differential nonlinearity                 | Worst-case deviation of any step from ideal  | -1   |       | 4   | LSB  |
| Input range              |   |  | 0    |       | 1.4 | V    |
| Driving source impedance |   |  |      |       | 100 | Ω    |
| FCLK                     | Clock rate                                | Successive approximation input clock rate  |      | 10    |     | MHz  |
| Input capacitance        |   |  |      | 12    |     | pF   |
| Input impedance          |   | ADC Pin 57   |      | 2.15  |     | kΩ   |
|                          |   | ADC Pin 58   |      | 0.7   |     |      |
|                          |   | ADC Pin 59   |      | 2.12  |     |      |
|                          |   | ADC Pin 60   |      | 1.17  |     |      |
| Number of channels       |   |  | 4    |       |     |      |
| F <sub>sample</sub>      | Sampling rate of each pin                 |  |      | 62.5  |     | KSPS |
| F <sub>input_max</sub>   | Maximum input signal frequency            |  |      |       | 31  | kHz  |
| SINAD                    | Signal-to-noise and distortion            | Input frequency DC to 300 Hz and 1.4 V <sub>pp</sub> sine wave input                                       | 55   | 60    |     | dB   |
| I <sub>active</sub>      | Active supply current                     | Average for analog-to-digital during conversion without reference current                                  |      | 1.5   |     | mA   |
| I <sub>PD</sub>          | Power-down supply current for core supply | Total for analog-to-digital when not active (this must be the SoC level test)                              |      | 1     |     | μA   |
| Absolute offset error    |   | FCLK = 10 MHz  |      | ±2    |     | mV   |
| Gain error               |   |  |      | ±2%   |     |      |
| V <sub>ref</sub>         | ADC reference voltage                     |  |      | 1.467 |     | V    |

### 7.17.6.7 Camera Parallel Port

The fast camera parallel port interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The camera parallel port supports 8 bits.

Figure 7-21 shows the timing diagram for the camera parallel port.

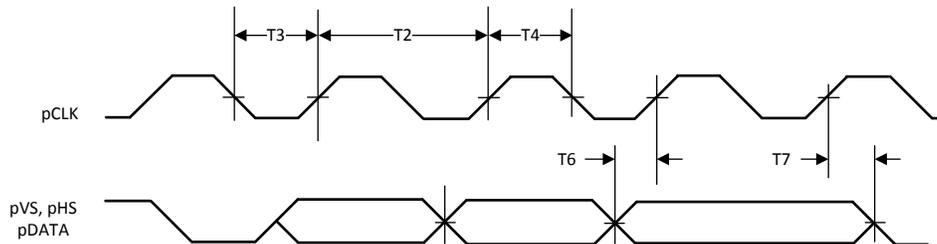


Figure 7-21. Camera Parallel Port Timing Diagram

Table 7-31 lists the timing parameters for the camera parallel port.

Table 7-31. Camera Parallel Port Timing Parameters

| PARAMETER NUMBER |           |                    | MIN | MAX         | UNIT |
|------------------|-----------|--------------------|-----|-------------|------|
|                  | pCLK      | Clock frequency    |     | 2           | MHz  |
| T2               | $T_{clk}$ | Clock period       |     | $1/pCLK$    | ns   |
| T3               | $t_{LP}$  | Clock low period   |     | $T_{clk}/2$ | ns   |
| T4               | $t_{HT}$  | Clock high period  |     | $T_{clk}/2$ | ns   |
| T6               | $t_{IS}$  | RX data setup time |     | 2           | ns   |
| T7               | $t_{IH}$  | RX data hold time  |     | 2           | ns   |
|                  | D         | Duty cycle         | 45% | 55%         |      |

### 7.17.6.8 UART

The CC3235x device includes two UARTs with the following features:

- Programmable baud-rate generator allows speeds up to 3Mbps
- Separate 16-bit × 8-bit TX and RX FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including a 1-byte-deep operation providing a conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Generation and detection of line-breaks
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Generation and detection of even, odd, stick, or no-parity bits
  - Generation of 1 or 2 stop-bits
- RTS and CTS hardware flow support
- Standard FIFO-level and End-of-Transmission interrupts

- Efficient transfers using  $\mu$ DMA:
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- The system clock is used to generate the baud clock.

#### 7.17.6.9 SD Host

The CC3235x device provides an interface between a local host (LH), such as an MCU and an SD memory card, and handles SD transactions with minimal LH intervention.

The SD host does the following:

- Provides SD card access in 1-bit mode
- Deals with SD protocol at the transmission level
- Handles data packing
- Adds cyclic redundancy checks (CRC)
- Start and end bit
- Checks for syntactical correctness

The application interface sends every SD command and either polls for the status of the adapter or waits for an interrupt request. The result is then sent back to the application interface in case of exceptions or to warn of end-of-operation. The controller can be configured to generate DMA requests and work with minimum CPU intervention. Given the nature of integration of this peripheral on the CC3235x platform, TI recommends that developers use peripheral library APIs to control and operate the block. This section emphasizes understanding the SD host APIs provided in the peripheral library of the CC3235x Software Development Kit (SDK).

The SD Host features are as follows:

- Full compliance with SD command and response sets, as defined in the SD memory card
  - Specifications, v2.0
  - Includes high-capacity (size >2GB) HC and SD cards
- Flexible architecture allows support for new command structure
- 1-bit transfer mode specifications for SD cards
- Built-in 1024-byte buffer for read or write
  - 512-byte buffer for both transmit and receive
  - Each buffer is 32-bits wide by 128-words deep
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Programmable clock generation
- Integrates an internal transceiver that allows a direct connection to the SD card without an external transceiver
- Supports configurable busy and response timeout
- Support for a wide range of card clock frequency with odd and even clock ratio
- Maximum frequency supported is 24MHz.

#### 7.17.6.10 Timers

Programmable timers can be used to count or time external events that drive the timer input pins. The CC3235x general-purpose timer module (GPTM) contains 16- or 32-bit GPTM blocks. Each 16- or 32-bit GPTM block provides two 16-bit timers or counters (referred to as Timer A and Timer B) that can be configured to operate independently as timers or event counters, or they can be concatenated to operate as one 32-bit timer. Timers can also be used to trigger  $\mu$ DMA transfers.

The GPTM contains four 16- or 32-bit GPTM blocks with the following functional options:

- Operating modes:
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 16-bit input-edge count or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal
- Counts up or counts down
- Sixteen 16- or 32-bit capture compare pins (CCP)
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine
- Efficient transfers using micro direct memory access controller ( $\mu$ DMA):
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt
- Runs from system clock (80MHz)

## 8 Detailed Description

### 8.1 Overview

The CC3235x wireless MCU family has a rich set of peripherals for diverse application requirements. This section briefly highlights the internal details of the CC3235x devices and offers suggestions for application configurations.

### 8.2 Arm® Cortex®-M4 Processor Core Subsystem

The high-performance Arm® Cortex®-M4 processor provides a cost-conscious platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The Arm Cortex-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit Arm® Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for Armv6 unaligned accesses
- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low-latency interrupt processing. The NVIC includes the following features:
  - Bits of priority configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  - Wake-up interrupt controller (WIC) providing ultra-low-power sleep mode support
- Bus interfaces:
  - Advanced high-performance bus (AHB-Lite) interfaces: system bus interfaces
  - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Cost-conscious debug solution featuring:
  - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted
  - Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
  - Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

### 8.3 Wi-Fi® Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated Arm MCU to completely offload the host MCU along with an 802.11a/b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3235x devices support station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security, WPS 2.0, and WPA3 personal and enterprise<sup>11</sup>. The Wi-Fi network processor includes an embedded IPv6, IPv4 TCP/IP stack, TLS stack and network applications such as HTTPS server.

<sup>11</sup> See CC3235 SDK v3.40 or later for details. Limited to STA mode only.

### 8.3.1 WLAN

The WLAN features are as follows:

- 802.11a/b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, Wi-Fi Direct client, and group owner with CCK and OFDM rates in the 2.4 GHz band (channels 1 through 13), and the 5GHz 20-MHz BW U-NII bands (U-NII-1, U-NII-2A, U-NII-2C, and U-NII-3).

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#### Note

802.11n is supported only in Wi-Fi station and Wi-Fi direct.

- The automatically calibrated radio with a single-ended 50Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in serial flash allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators, including: WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x), WPA3 Personal, and WPA3 Enterprise.

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#### Note

When using WPA Enterprise security modes, the TLS socket used to communicate with the Radius server is limited to TLSv1.0.

- Smart provisioning options deeply integrated within the device providing a comprehensive end-to-end solution. With elaborate events notification to the host, enabling the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point with HTTP server
  - WPS - Wi-Fi Protected Setup, supporting both push button and pin code options.
  - SmartConfig™ Technology: TI proprietary, easy-to-use, one-step, one-time process used to connect a CC3235x-enabled device to the home wireless network.
- 802.11 transceiver mode allows transmitting and receiving of proprietary data through a socket. The 802.11 transceiver mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works with the filtering options.
- Antenna selection for best connection
- BLE/2.4GHz radio coexistence mechanism to avoid interference

### 8.3.2 Network Stack

The Network Stack features are as follows:

- Integrated IPv4, IPv6 TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

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#### Note

Not all APIs are 100% BSD compliant. Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, RAW, SSL/TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 with DAD and stateless autoconfiguration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet
- Built-in network applications and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial flash
    - RESTful APIs for setting and configuring application content
    - Dynamic user callbacks

- Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3235x device provides critical information, such as device name, IP, vendor, and port number.
- DHCP server
- Ping

Table 8-1 describes the NWP features.

**Table 8-1. NWP Features**

| Feature                            | Description  |
|------------------------------------|--|
| Wi-Fi standards                    | 802.11a/b/g/n station<br>802.11a/b/g AP supporting up to four stations<br>Wi-Fi Direct client and group owner  |
| Wi-Fi channels                     | 2.4 GHz ISM and 5 GHz U-NII Channels   |
| Channel Bandwidth                  | 20 MHz   |
| Wi-Fi security                     | WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x), WPA3 personal and enterprise <sup>(1)</sup>   |
| Wi-Fi provisioning                 | SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP web server  |
| IP protocols                       | IPv4/IPv6  |
| IP addressing                      | Static IP, LLA, DHCPv4, DHCPv6 with DAD  |
| Cross layer                        | ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP  |
| Transport                          | UDP, TCP<br>SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2<br>RAW   |
| Network applications and utilities | Ping<br>HTTP/HTTPS web server<br>mDNS<br>DNS-SD<br>DHCP server   |
| Host interface                     | UART/SPI   |
| Security                           | Device identity<br>Trusted root-certificate catalog<br>TI root-of-trust public key<br>The CC3235S and CC3235SF variants also support: <ul style="list-style-type: none"> <li>• Secure key storage</li> <li>• Online certificate status protocol (OCSP)</li> <li>• Certificate signing request (CSR)</li> <li>• Unique per device Key-Pair</li> <li>• File system security</li> <li>• Software tamper detection</li> <li>• Cloning protection</li> <li>• Secure boot</li> <li>• Validate the integrity and authenticity of the run-time binary during boot</li> <li>• Initial secure programming</li> <li>• Debug security</li> <li>• JTAG and debug</li> </ul> |
| Power management                   | Enhanced power policy management uses 802.11 power save and deep-sleep power modes   |
| Other                              | Transceiver<br>Programmable RX filters with event-trigger mechanism<br>Rx Metrics for tracking the surrounding RF environment  |

(1) See CC3235 SDK v3.40 or newer for details. Limited to STA mode only.

## 8.4 Security

The SimpleLink™ Wi-Fi® CC3235x Internet-on-a-chip device enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

### Wi-Fi and Internet Security:

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0/1
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TLS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2
- Secure sockets
  - Protocol versions: OCSP, SSL v3, TLS 1.0, TLS 1.1, TLS 1.2
  - Powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections
  - Ciphers suites
    - SL\_SEC\_MASK\_SSL\_RSA\_WITH\_RC4\_128\_SHA
    - SL\_SEC\_MASK\_SSL\_RSA\_WITH\_RC4\_128\_MD5
    - SL\_SEC\_MASK\_TLS\_RSA\_WITH\_AES\_256\_CBC\_SHA
    - SL\_SEC\_MASK\_TLS\_DHE\_RSA\_WITH\_AES\_256\_CBC\_SHA
    - SL\_SEC\_MASK\_TLS\_ECDHE\_RSA\_WITH\_AES\_256\_CBC\_SHA
    - SL\_SEC\_MASK\_TLS\_ECDHE\_RSA\_WITH\_RC4\_128\_SHA
    - SL\_SEC\_MASK\_TLS\_RSA\_WITH\_AES\_128\_CBC\_SHA256
    - SL\_SEC\_MASK\_TLS\_RSA\_WITH\_AES\_256\_CBC\_SHA256
    - SL\_SEC\_MASK\_TLS\_ECDHE\_RSA\_WITH\_AES\_128\_CBC\_SHA256
    - SL\_SEC\_MASK\_TLS\_ECDHE\_ECDSA\_WITH\_AES\_128\_CBC\_SHA256
    - SL\_SEC\_MASK\_TLS\_ECDHE\_ECDSA\_WITH\_AES\_128\_CBC\_SHA
    - SL\_SEC\_MASK\_TLS\_ECDHE\_ECDSA\_WITH\_AES\_256\_CBC\_SHA
    - SL\_SEC\_MASK\_TLS\_RSA\_WITH\_AES\_128\_GCM\_SHA256
    - SL\_SEC\_MASK\_TLS\_RSA\_WITH\_AES\_256\_GCM\_SHA384
    - SL\_SEC\_MASK\_TLS\_DHE\_RSA\_WITH\_AES\_128\_GCM\_SHA256
    - SL\_SEC\_MASK\_TLS\_DHE\_RSA\_WITH\_AES\_256\_GCM\_SHA384
    - SL\_SEC\_MASK\_TLS\_ECDHE\_RSA\_WITH\_AES\_128\_GCM\_SHA256
    - SL\_SEC\_MASK\_TLS\_ECDHE\_RSA\_WITH\_AES\_256\_GCM\_SHA384
    - SL\_SEC\_MASK\_TLS\_ECDHE\_ECDSA\_WITH\_AES\_128\_GCM\_SHA256
    - SL\_SEC\_MASK\_TLS\_ECDHE\_ECDSA\_WITH\_AES\_256\_GCM\_SHA384
    - SL\_SEC\_MASK\_TLS\_ECDHE\_ECDSA\_WITH\_CHACHA20\_POLY1305\_SHA256
    - SL\_SEC\_MASK\_TLS\_ECDHE\_RSA\_WITH\_CHACHA20\_POLY1305\_SHA256
    - SL\_SEC\_MASK\_TLS\_DHE\_RSA\_WITH\_CHACHA20\_POLY1305\_SHA256
  - Server authentication
  - Client authentication
  - Domain name verification
  - Runtime socket upgrade to secure socket – STARTTLS

- Secure HTTP server (HTTPS)
- Trusted root-certificate catalog – Verifies that the CA used by the application is trusted and known secure content delivery
- TI root-of-trust public key – Hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery – Allows encrypted file transfer to the system using asymmetric keys created by the device

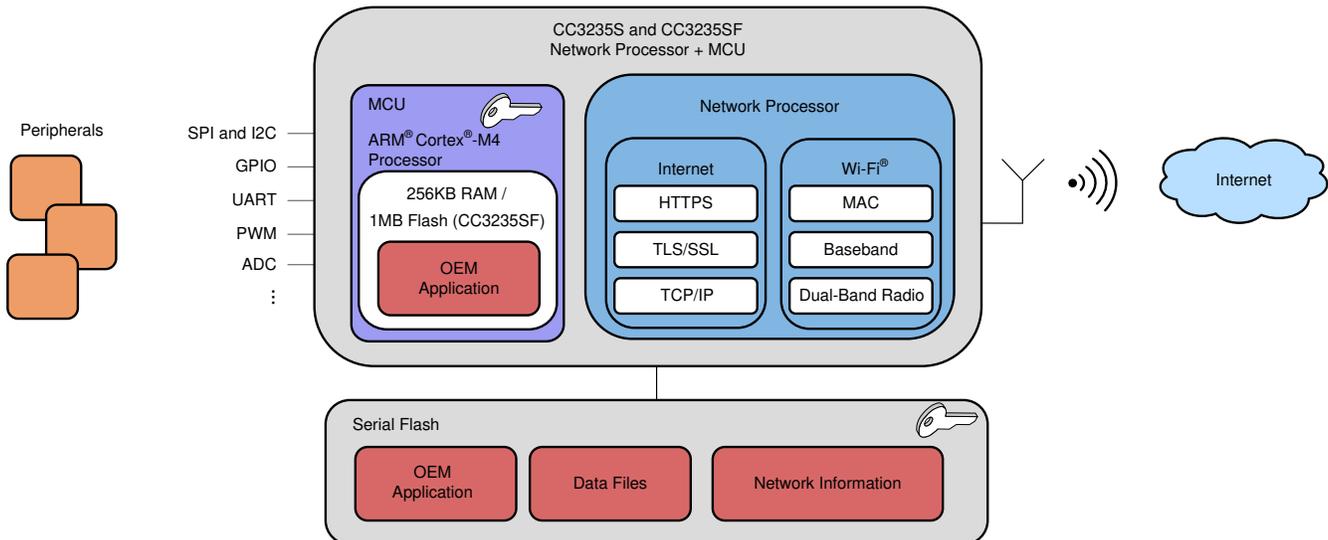
**Code and Data Security:**

- Network passwords and certificates are encrypted and signed.
- Cloning protection – Application and data files are encrypted by a unique key per device.
- Access control – Access to application and data files only by using a token provided in file creation time. If an unauthorized access is detected, a tamper protection lock down mechanism takes effect.
- Secured boot – Authentication of the application image on every boot
- Code and data encryption – User application and data files can be encrypted in the serial flash
- Code and data authentication – User Application and data files are authenticated with a public key certificate
- Offloaded crypto library for asymmetric keys, including the ability to create key-pair, sign and verify data buffer
- Recovery mechanism

**Device Security:**

- Separate execution environments – Application processor and network processor run on separate Arm cores
- Initial secure programming – Allows for keeping the content confidential on the production line
- Debug security
  - JTAG lock
  - Debug ports lock
- True random number generator

Figure 8-1 shows the high-level structure of the CC3235S and CC3235SF devices. The application image, user data, and network information files (passwords, certificates) are encrypted using a device-specific key.



**Figure 8-1. CC3235S and CC3235SF High-Level Structure**

## 8.5 FIPS 140-2 Level 1 Certification

The Federal Information Processing Standard (FIPS) Publication 140-2 is a U.S. government computer security standard. It is commonly referred to as FIPS 140-2 and is used to accredit the design and implementation of cryptographic modules. A cryptographic module within a security system is necessary to maintain the confidentiality and integrity of the information protected by the device.

The security engines of the CC3235x device are FIPS validated for FIPS 140-2 level 1 certification <sup>12</sup>. This certification involves testing the device for all areas related to the secure design and implementation of the cryptographic modules and covers topics such as: cryptographic specifications, ports and interfaces, a finite state model for the cryptographic module, the operational environment of the module, and how cryptographic keys are managed.

## 8.6 Power-Management Subsystem

The CC3235x power-management subsystem contains DC/DC converters to accommodate the different voltage or current requirements of the system.

- Digital DC/DC (Pin 44)
  - Input:  $V_{BAT}$  wide voltage (2.1V to 3.6V)
- ANA1 DC/DC (Pin 37)
  - Input:  $V_{BAT}$  wide voltage (2.1V to 3.6V)
- PA DC/DC (Pin 39)
  - Input:  $V_{BAT}$  wide voltage (2.1V to 3.6V)
- ANA2 DC/DC (Pin 47, CC3235SF only)
  - Input:  $V_{BAT}$  wide voltage (2.1V to 3.6V)

The CC3235x device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the device to operate from a wide variety of input sources.

## 8.7 Low-Power Operating Mode

From a power-management perspective, the CC3235x device comprises the following two independent subsystems:

- Arm<sup>®</sup> Cortex<sup>®</sup>-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Arm<sup>®</sup> Cortex<sup>®</sup>-M4 application processor runs the user application loaded from an external serial flash or internal flash (in CC3235SF). The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

<sup>12</sup> For exact status of FIPS certification for a specific part number, please refer to <https://csrc.nist.gov/publications/fips>.

The user program controls the power state of the application processor subsystem. The application processor can be in one of the five modes described in [Table 8-2](#).

**Table 8-2. User Program Modes**

| APPLICATION PROCESSOR (MCU) MODE <sup>(1)</sup> | DESCRIPTION  |
|---|--|
| MCU active mode                                 | MCU executing code at a state rate of 80MHz  |
| MCU sleep mode                                  | The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.   |
| MCU LPDS mode                                   | State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs as the wake-up source. |
| MCU hibernate mode                              | The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The RTC continues running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15ms plus the time to load the application from serial flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO.       |
| MCU shutdown mode                               | The lowest power mode system-wide. All device logics are off, including the RTC. The wake-up time in this mode is longer than hibernate at about 1.1s. To enter or exit the shutdown mode, the state of the nRESET line is changed (low to shut down, high to turn on).  |

(1) Modes are listed in order of power consumption, with the highest power modes listed first.

The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception (see [Table 8-3](#)).

**Table 8-3. Networking Subsystem Modes**

| NETWORK PROCESSOR MODE                             | DESCRIPTION  |
|--|--|
| Network active mode (processing layer 3, 2, and 1) | Transmitting or receiving IP protocol packets  |
| Network active mode (processing layer 2 and 1)     | Transmitting or receiving MAC management frames; IP processing is not required.  |
| Network active listen mode                         | Special power-optimized active mode for receiving beacon frames (no other frames are supported)  |
| Network connected Idle                             | A composite mode that implements 802.11 infrastructure power-save operation. The CC3235x NWP automatically enters LPDS mode between beacons and then wakes into active listen mode to receive a beacon and determine if there is pending traffic at the AP. If not, the NWP returns to LPDS mode and the cycle repeats.<br><br>Advanced features of long sleep interval and IoT low power for extending LPDS time for up to 22 seconds while maintaining Wi-Fi connection is supported in this mode. |
| Network LPDS mode                                  | Low-power state between beacons in which the state is retained by the NWP, allowing for a rapid wake-up.   |
| Network disabled                                   | The network is disabled.   |

The operation of the application and network processor ensures that the device remains in the lowest power mode most of the time to preserve battery life.

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of receiving a beacon frame and waiting for the next beacon.
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data, spends most of the time in hibernate mode, jumping briefly to active mode to transmit data.

## 8.8 Memory

### 8.8.1 External Memory Requirements

The CC3235x device maintains a proprietary file system on the serial flash. The CC3235x file system stores the MCU binary, service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always at the beginning of the serial flash. The applications microcontroller must access the serial flash memory area allocated to the file system directly through the CC3235x file system. The applications microcontroller must not access the serial flash memory area directly.

The file system manages the allocation of serial flash blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on serial flash using human-readable filenames rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system.

All file types can have a maximum of 100 supported files in the file system. All files are stored in 4KB blocks and thus use a minimum of 4KB of flash space. Fail-safe files require twice the original size and use a minimum of 8KB. Encrypted files are counted as fail-safe in terms of space. The maximum file size is 1MB.

Table 8-4 lists the minimum required memory consumption under the following assumptions:

- System files in use consume 64 blocks (256KB).
- Vendor files are not taken into account.
- MCU code is taken as the maximal possible size for the CC3235 with fail-safe enabled to account for future updates, such as through OTA.
- Gang image:
  - Storage for the gang image is rounded up to 32 blocks (meaning 128KB resolution).
  - Gang image size depends on the actual content size of all components. Additionally, the image should be 128KB aligned so unaligned memory is considered lost. Service pack, system files, and the 128KB aligned memory are assumed to occupy 256KB.
- All calculations consider that the restore-to-default is enabled.

**Table 8-4. Recommended Flash Size**

| ITEM  | CC3235S (KB) | CC3235SF (KB) |
|---|--------------|---------------|
| File system allocation table                  | 20           | 20            |
| System and configuration files <sup>(1)</sup> | 256          | 256           |
| Service pack <sup>(1)</sup>                   | 264          | 264           |
| MCU Code <sup>(1)</sup>                       | 512          | 2048          |
| Gang image size                               | 256 + MCU    | 256 + MCU     |
| Total   | 1308 + MCU   | 2844 + MCU    |
| Minimal flash size <sup>(2)</sup>             | 16MBit       | 32MBit        |
| Recommended flash size <sup>(2)</sup>         | 16MBit       | 32MBit        |

(1) Including fail-safe.

(2) For maximum MCU size.

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**Note**

The maximum supported serial flash size is 32MB (256Mb) (see [Using Serial Flash on CC3135/CC3235 SimpleLink™ Wi-Fi® and Internet-of-Things Devices](#)).

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**8.8.2 Internal Memory**

The CC3235x device includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. The micro direct memory access ( $\mu$ DMA) controller can transfer data to and from SRAM and various peripherals. The CC3235x ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3235x API list.

**8.8.2.1 SRAM**

The CC3235x family provides 256KB of on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is at offset 0x2000 0000 of the device memory map.

Use the  $\mu$ DMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide.

**8.8.2.2 ROM**

The internal zero-wait-state ROM of the CC3235x device is at address 0x0000 0000 of the device memory and is programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial flash memory is empty). The CC3235x DriverLib software library controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce flash memory requirements and free the flash memory for other purposes.

**8.8.2.3 Flash Memory**

The CC3235SF device comes with an on-chip flash memory of 1MB that allows application code to execute in place while freeing SRAM exclusively for read-write data. The flash memory is used for code and constant data sections and is directly attached to the icode/dcode bus of the Arm Cortex-M4 core. A 128-bit-wide instruction prefetch buffer allows maintenance of maximum performance for linear code or loops that fit inside the buffer.

The flash memory is organized as 2KB sectors that can be independently erased. Reads and writes can be performed at word (32-bit) level.

### 8.8.2.4 Memory Map

Table 8-5 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

**Table 8-5. Memory Map**

| START ADDRESS | END ADDRESS | DESCRIPTION  | COMMENT                        |
|---------------|-------------|--|--------------------------------|
| 0x0000 0000   | 0x0007 FFFF | On-chip ROM (bootloader + DriverLib)                                       |                                |
| 0x0100 0000   | 0x010F FFFF | On-chip flash (for user application code)                                  | CC3235SF device only           |
| 0x2000 0000   | 0x2003 FFFF | Bit-banded on-chip SRAM  |                                |
| 0x2200 0000   | 0x23FF FFFF | Bit-band alias of 0x2000 0000 to 0x200F FFFF                               |                                |
| 0x4000 0000   | 0x4000 0FFF | Watchdog timer A0  |                                |
| 0x4000 4000   | 0x4000 4FFF | GPIO port A0   |                                |
| 0x4000 5000   | 0x4000 5FFF | GPIO port A1   |                                |
| 0x4000 6000   | 0x4000 6FFF | GPIO port A2   |                                |
| 0x4000 7000   | 0x4000 7FFF | GPIO port A3   |                                |
| 0x4000 C000   | 0x4000 CFFF | UART A0  |                                |
| 0x4000 D000   | 0x4000 DFFF | UART A1  |                                |
| 0x4002 0000   | 0x4000 07FF | I <sup>2</sup> C A0 (master)   |                                |
| 0x4002 0800   | 0x4002 0FFF | I <sup>2</sup> C A0 (slave)  |                                |
| 0x4002 4000   | 0x4002 4FFF | GPIO group 4   |                                |
| 0x4003 0000   | 0x4003 0FFF | General-purpose timer A0   |                                |
| 0x4003 1000   | 0x4003 1FFF | General-purpose timer A1   |                                |
| 0x4003 2000   | 0x4003 2FFF | General-purpose timer A2   |                                |
| 0x4003 3000   | 0x4003 3FFF | General-purpose timer A3   |                                |
| 0x400F 7000   | 0x400F 7FFF | Configuration registers  |                                |
| 0x400F E000   | 0x400F EFFF | System control   |                                |
| 0x400F F000   | 0x400F FFFF | μDMA   |                                |
| 0x4200 0000   | 0x43FF FFFF | Bit band alias of 0x4000 0000 to 0x400F FFFF                               |                                |
| 0x4401 0000   | 0x4401 0FFF | SDIO master  |                                |
| 0x4401 8000   | 0x4401 8FFF | Camera Interface   |                                |
| 0x4401 C000   | 0x4401 DFFF | McASP  |                                |
| 0x4402 0000   | 0x4402 1FFF | SSPI   | Used for external serial flash |
| 0x4402 1000   | 0x4402 2FFF | GSPI   | Used by application processor  |
| 0x4402 5000   | 0x4402 5FFF | MCU reset clock manager  |                                |
| 0x4402 6000   | 0x4402 6FFF | MCU configuration space  |                                |
| 0x4402 D000   | 0x4402 DFFF | Global power, reset, and clock manager (GPRCM)                             |                                |
| 0x4402 E000   | 0x4402 EFFF | MCU shared configuration   |                                |
| 0x4402 F000   | 0x4402 FFFF | Hibernate configuration  |                                |
| 0x4403 0000   | 0x4403 FFFF | Crypto range (includes apertures for all crypto-related blocks as follows) |                                |
| 0x4403 0000   | 0x4403 0FFF | DTHE registers and TCP checksum  |                                |
| 0x4403 5000   | 0x4403 5FFF | MD5/SHA  |                                |
| 0x4403 7000   | 0x4403 7FFF | AES  |                                |
| 0x4403 9000   | 0x4403 9FFF | DES  |                                |
| 0xE000 0000   | 0xE000 0FFF | Instrumentation trace Macrocell™   |                                |
| 0xE000 1000   | 0xE000 1FFF | Data watchpoint and trace (DWT)  |                                |
| 0xE000 2000   | 0xE000 2FFF | Flash patch and breakpoint (FPB)   |                                |
| 0xE000 E000   | 0xE000 EFFF | NVIC   |                                |

**Table 8-5. Memory Map (continued)**

| START ADDRESS | END ADDRESS | DESCRIPTION                                 | COMMENT |
|---------------|-------------|---|---------|
| 0xE004 0000   | 0xE004 0FFF | Trace port interface unit (TPIU)            |         |
| 0xE004 1000   | 0xE004 1FFF | Reserved for embedded trace macrocell (ETM) |         |
| 0xE004 2000   | 0xE00F FFFF | Reserved                                    |         |

## 8.9 Restoring Factory Default Configuration

The device has an internal recovery mechanism that allows rolling back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the serial flash in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None – no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by calling software APIs, or by pulling or forcing SOP[2:0] = 110 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial flash vendor.

## 8.10 Boot Modes

### 8.10.1 Boot Mode List

The CC3235x device implements a sense-on-power (SOP) scheme to determine the device operation mode.

SOP values are sensed from the device pin during power-up. This encoding determines the boot flow. Before the device is taken out of reset, the SOP values are copied to a register and used to determine the device operation mode while powering up. These values determine the boot flow as well as the default mapping (to JTAG, SWD, UART0) for some of the pins. [Table 8-6](#) lists the pull configurations.

**Table 8-6. CC3235x Functional Configurations**

| BOOT MODE NAME          | SOP[2]   | SOP[1]   | SOP[0]   | SOP MODE       | COMMENT   |
|-------------------------|----------|----------|----------|----------------|---|
| UARTLOAD                | Pullup   | Pulldown | Pulldown | LDfrUART       | Factory, lab flash, and SRAM loads through the UART. The device waits indefinitely for the UART to load code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode.  |
| FUNCTIONAL_2WJ          | Pulldown | Pulldown | Pullup   | Fn2WJ          | Functional development mode. In this mode, 2-pin SWD is available to the developer. TMS and TCK are available for debugger connection.  |
| FUNCTIONAL_4WJ          | Pulldown | Pulldown | Pulldown | Fn4WJ          | Functional development mode. In this mode, 4-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection.  |
| UARTLOAD_FUNCTIONAL_4WJ | Pulldown | Pullup   | Pulldown | LDfrUART_Fn4WJ | Supports flash and SRAM load through UART and functional mode. The MCU bootloader tries to detect a UART break on UART receive line. If the break signal is present, the device enters the UARTLOAD mode, otherwise, the device enters the functional mode. TDI, TMS, TCK, and TDO are available for debugger connection. |

**Table 8-6. CC3235x Functional Configurations (continued)**

| BOOT MODE NAME    | SOP[2]   | SOP[1] | SOP[0] | SOP MODE   | COMMENT   |
|-------------------|----------|--------|--------|------------|---|
| RET_FACTORY_IMAGE | Pulldown | Pullup | Pullup | RetFactDef | When the device reset is toggled, the MCU bootloader kick-starts the procedure to restore factory default images. |

The recommended values of pulldown resistors are 69.8kΩ for SOP0 and SOP1 and 100kΩ for SOP2. The application can use SOP2 for other functions after the device has powered up. To avoid spurious SOP values from being sensed at power up, TI strongly recommends using the SOP2 pin only for output signals. The SOP0 and SOP1 pins are used as 5GHz control switch and are not available for other functions. Ensure the SOP pins are configured as shown in [Figure 9-7](#), this is the recommended configuration to ensure the RF Switch, SOP boot modes, and factory restore process operate optimally without conflict.

## 8.11 Hostless Mode

The SimpleLink Wi-Fi CC3235 device incorporates a scripting ability that enables offloading of simple tasks from the host processor. Using simple and conditional scripts, repetitive tasks can be handled internally, which allows the host processor to remain in a low-power state. In some cases where the scripter is being used to send packets, it reduces code footprint and memory consumption. The *if-this-then-that* style conditioning can include anything from GPIO toggling to transmitting packets.

The conditional scripting abilities can be divided into conditions and actions. The conditions define when to trigger actions. Only one action can be defined per condition, but multiple instances of the same condition may be used, so in effect multiple actions can be defined for a single condition. In total, 16 condition and action pairs can be defined. The conditions can be simple, or complex using sub-conditions (using a combinatorial AND condition between them). The actions are divided into two types, those that can occur during runtime and those that can occur only during the initialization phase.

The following actions can only be performed when triggered by the pre-initialization condition:

- Set roles AP, station, P2P, and Tag modes
- Delete all stored profiles
- Set connection policy
- Hardware GPIO indication allows an I/O to be driven directly from the WLAN core hardware to indicate internal signaling

The following actions may be activated during runtime:

- Send transceiver packet
- Send UDP packet
- Send TCP packet
- Increment counter increments one of the user counters by 1
- Set counter allows setting a specific value to a counter
- Timer control
- Set GPIO allows GPIO output from the device using the internal networking core
- Enter Hibernate state

---

### Note

Consider the following limitations:

- Timing cannot be ensured when using the network scripter because some variable latency will apply depending on the utilization of the networking core.
  - The scripter is limited to 16 pairs of conditions and reactions.
  - Both timers and counters are limited to 8 instances each. Timers are limited to a resolution of 1 second. Counters are 32 bits wide.
  - Packet length is limited to the size of one packet and the number of possible packet tokens is limited to 8.
-

## 9 Applications, Implementation, and Layout

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 9.1 Application Information

#### 9.1.1 BLE/2.4GHz Radio Coexistence

The CC3235x device is designed to support BLE/2.4GHz radio coexistence. Because WLAN is inherently more tolerant to time-domain disturbances, the coexistence mechanism gives priority to the Bluetooth® low energy entity over the WLAN. Bluetooth® low energy operates in the 2.4GHz band, therefore the coexistence mechanism does not affect the 5GHz band. The CC3235x device can operate normally on the 5GHz band, while the Bluetooth® low energy works on the 2.4GHz band without mutual interference.

The following coexistence modes can be configured by the user:

- Off mode or intrinsic mode
  - No BLE/2.4GHz radio coexistence, or no synchronization between WLAN and Bluetooth® low energy—in case Bluetooth® low energy exists in this mode, collisions can randomly occur.
- Time Division Multiplexing (TDM, Single Antenna)
  - 2.4GHz Wi-Fi band (see [Figure 9-1](#))

In this mode, the two entities share the antenna through an RF switch using two GPIOs (one input and one output from the WLAN perspective).

- 5GHz Wi-Fi band (see [Figure 9-2](#))

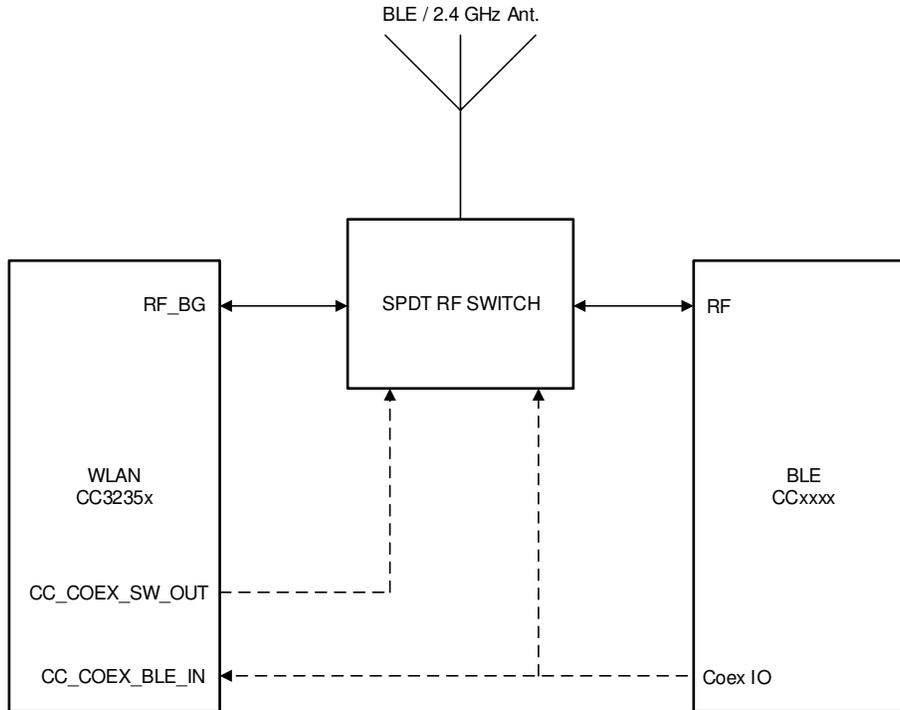
In this mode, the WLAN operates on the 5GHz band and Bluetooth® low energy operates on the 2.4GHz band. A 2.4- or 5GHz diplexer is required for sharing the single antenna.

- Time Division Multiplexing (TDM, Dual Antenna)
  - 2.4GHz Wi-Fi Band (see [Figure 9-3](#))

In this mode, the two entities have separate antennas. No RF switch is required and only a single GPIO (one input from the WLAN perspective).

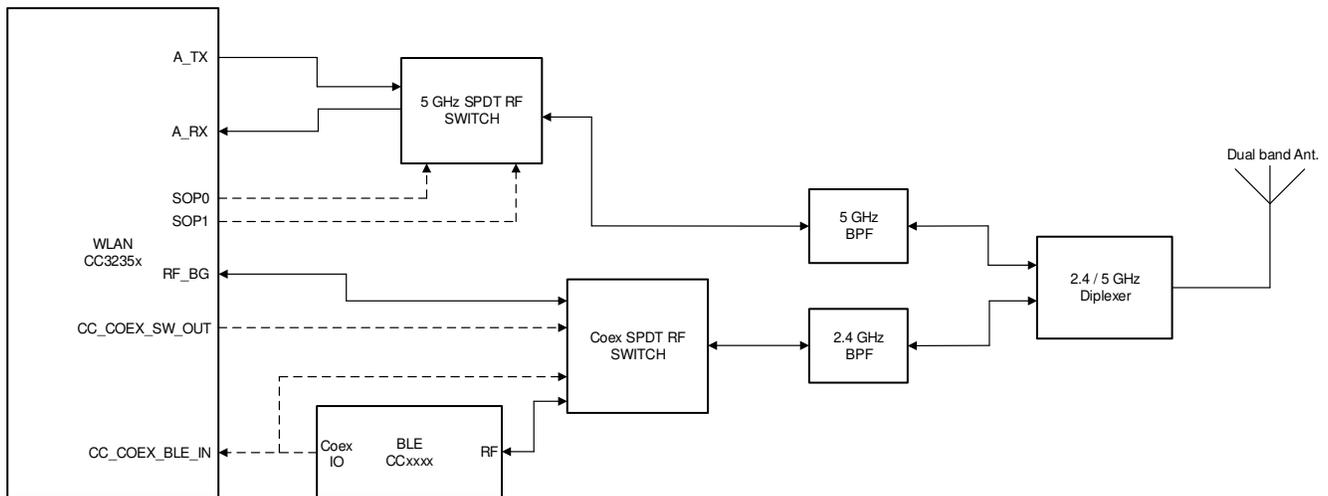
- 5GHz Wi-Fi band (see [Figure 9-4](#))

In this mode, the WLAN operates on the 5GHz band and Bluetooth® low energy operates on the 2.4GHz band. No diplexer is required for the dual-antenna solution.



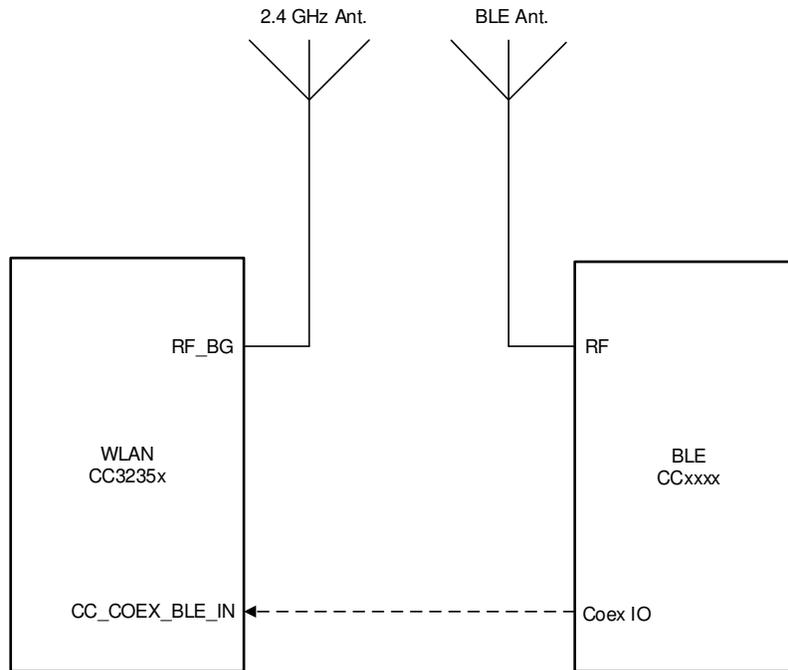
**Figure 9-1. 2.4GHz, Single-Antenna Coexistence Mode Block Diagram**

Figure 9-2 shows the single antenna implementation of a complete Bluetooth® low energy and WLAN coexistence network with the WLAN operating on either a 2.4- or a 5GHz band. The SOP lines control the 5GHz switch. The Coex switch is controlled by a GPIO signal from the BLE device and a GPIO signal from the CC3235x device.



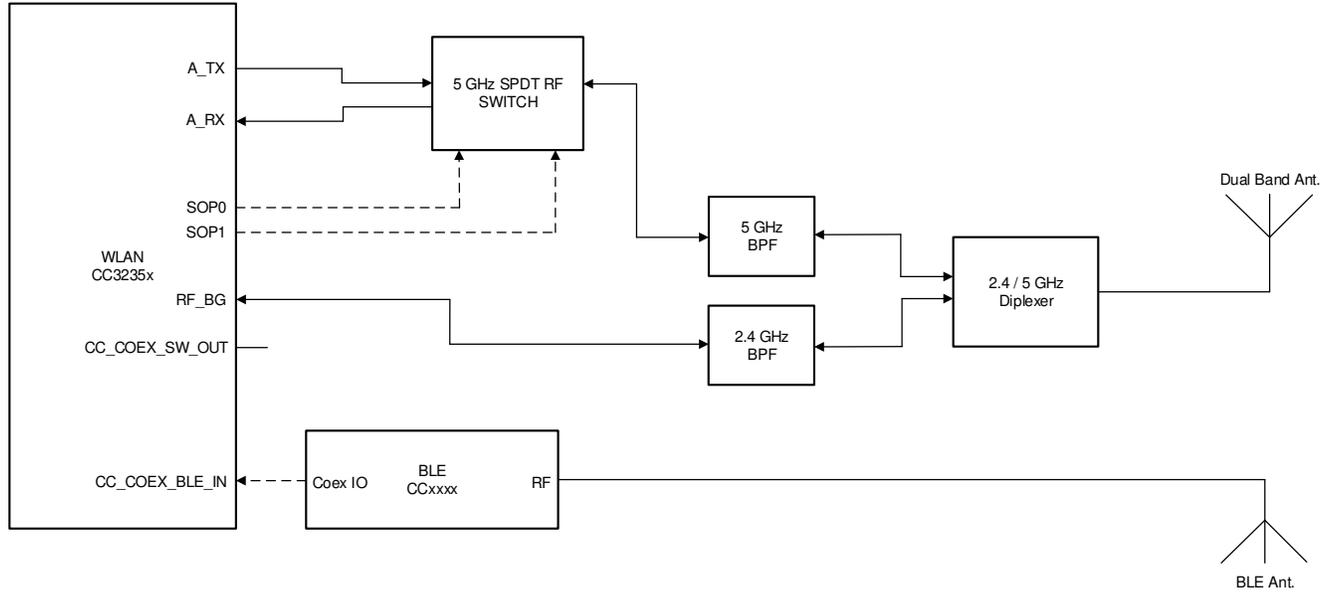
**Figure 9-2. Single Antenna Coexistence Solution with 5GHz Wi-Fi**

Figure 9-3 shows the dual antenna implementation of a complete Bluetooth® low energy and WLAN coexistence network with the WLAN operating on either a 2.4- or a 5GHz band. Note in this implementation no Coex switch is required and only a single GPIO from the BLE device to the CC3235x device is required.



**Figure 9-3. Dual-Antenna Coexistence Mode Block Diagram**

Figure 9-4 shows the dual antenna implementation of a complete Bluetooth® low energy and WLAN coexistence network with the WLAN operating on either a 2.4- or a 5GHz band. In this case, the 2.4GHz and 5GHz Wi-Fi share an antenna and the BLE has its own dedicated antenna. The SOP lines control the 5GHz switch. Note that in this implementation, no Coex switch is required and only a single GPIO from the BLE device to the CC3235x device is required.



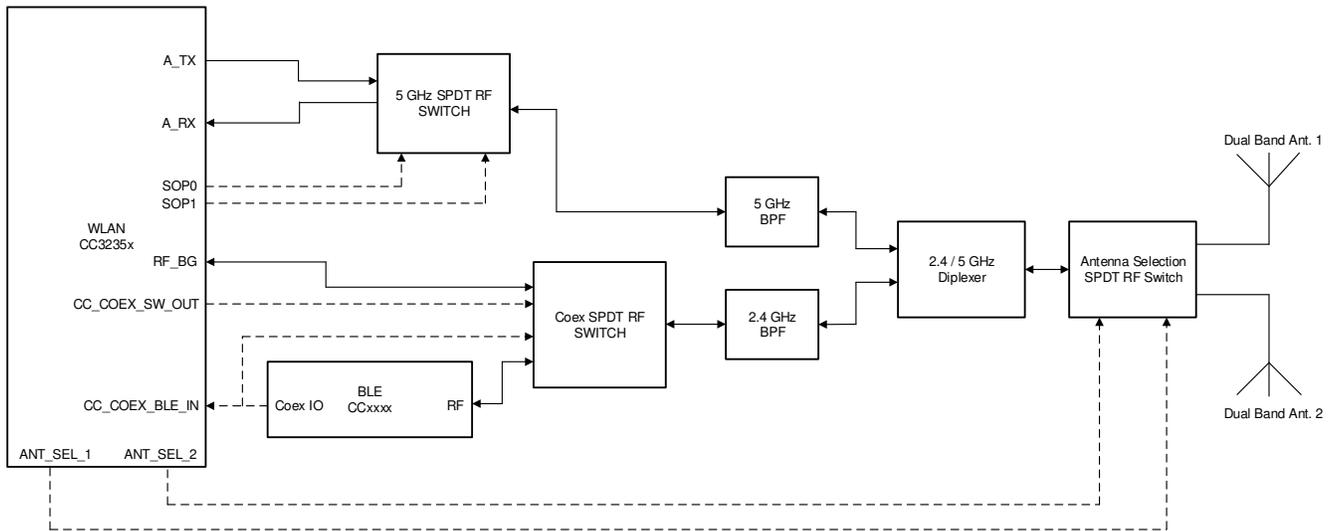
**Figure 9-4. Dual Antenna Coexistence Solution with 5GHz Wi-Fi**

### 9.1.2 Antenna Selection

The CC3235x device is designed to also support antenna selection and is controlled by Image Creator. When enabled, there are three options possible options:

- ANT 1: When selected, the GPIOs that are defined for antenna selection will set the RF path for antenna 1.
- ANT 2: When selected, the GPIOs that are defined for antenna selection will set the RF path for antenna 2.
- Autoselect: When selected, during a scan and prior to connecting to an AP, CC3235x device will determine the best RF path and select the appropriate antenna <sup>13 14</sup>. The result is saved as the port of the profile.

Figure 9-5 shows the implementation of a complete Bluetooth® low energy and WLAN coexistence network with the WLAN operating on either a 2.4- or a 5GHz band with antenna selection. The SOP lines control the 5GHz switch. The Coex switch is controlled by a GPIO signal from the BLE device and a GPIO signal from the CC3235x device. The Antenna switch is controlled by two GPIO lines from the CC3235x device.

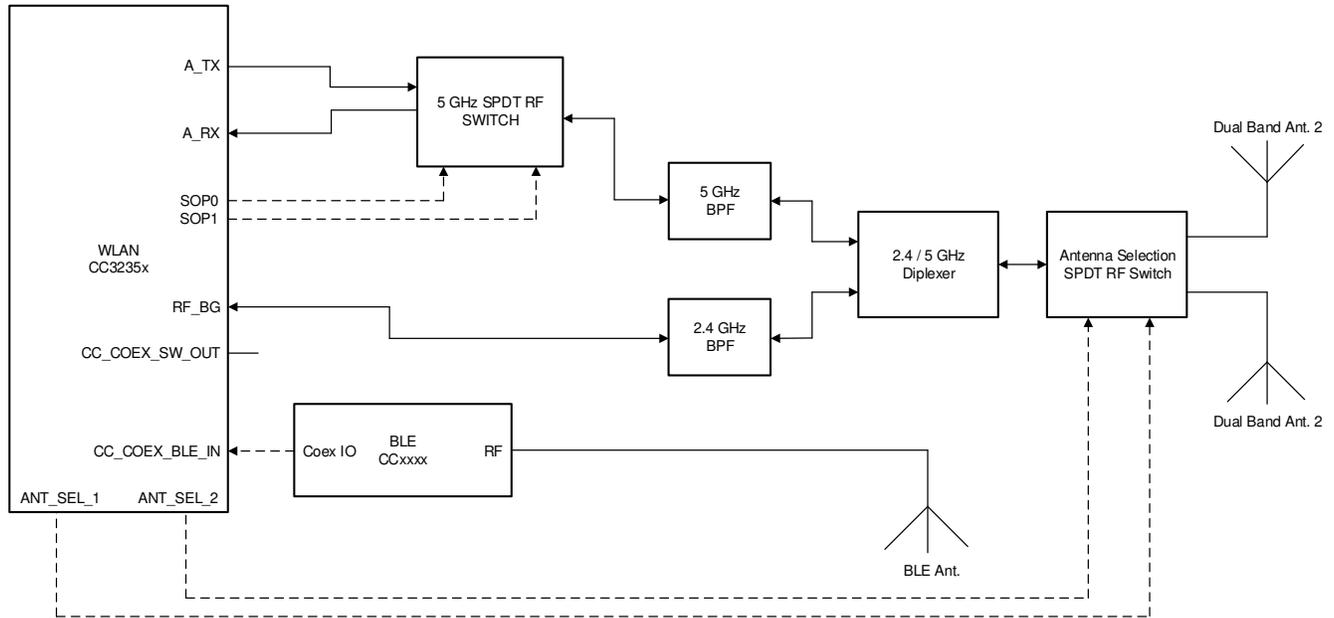


**Figure 9-5. Antenna Selection Solution with Coexistence Solution and 5GHz Wi-Fi**

<sup>13</sup> When selecting Autoselect via the API, a reset is required in order for the CC3235x device to determine the best antenna for use.

<sup>14</sup> Refer to the [Uniflash with Image Creator User Guide](#) for more information.

Figure 9-6 shows the antenna selection implementation for Wi-Fi, with BLE operating on its own antenna. The SOP lines control the 5GHz switch. Note in this implementation no Coex switch is required and only a single GPIO from the BLE device to the CC3235x device is required. The antenna switch is controlled by two GPIO lines from the CC3235x device.



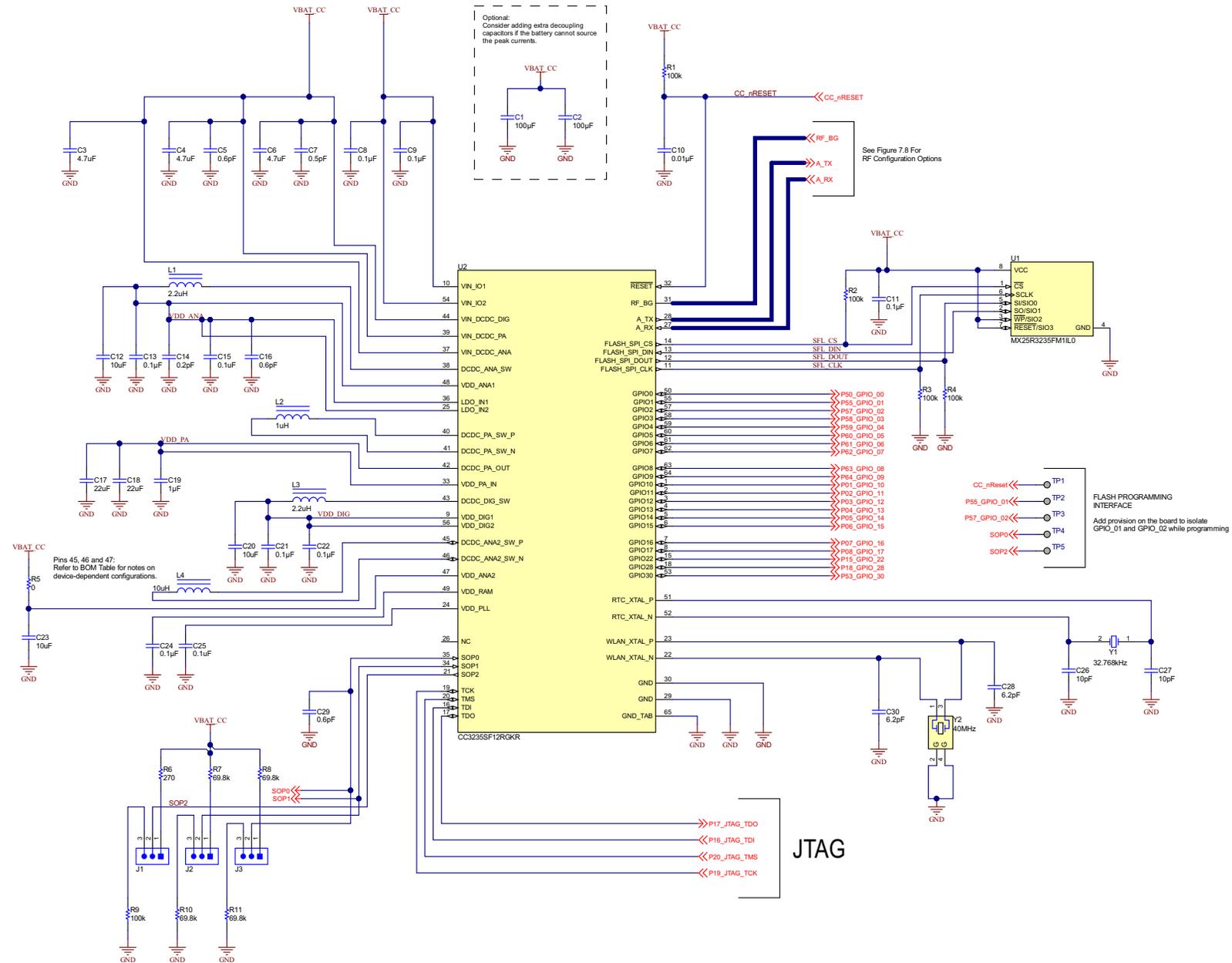
**Figure 9-6. Coexistence Solution with Wi-Fi Antenna Selection and dedicated BLE antenna**

### 9.1.3 Typical Application

Figure 9-7 shows the schematic of the engine area for the CC3235x device in the wide-voltage mode of operation, with the corresponding bill of materials show in Table 9-1. Figure 9-8 provides the schematic for the RF implementation with and without BLE/2.4GHz coexistence, with the corresponding bill of materials shown in Table 9-2. For a full operation reference design, see the [CC3235x SimpleLink™ and Internet of Things Hardware Design Files](#).

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**Figure 9-7. CC3235x Engine Area**

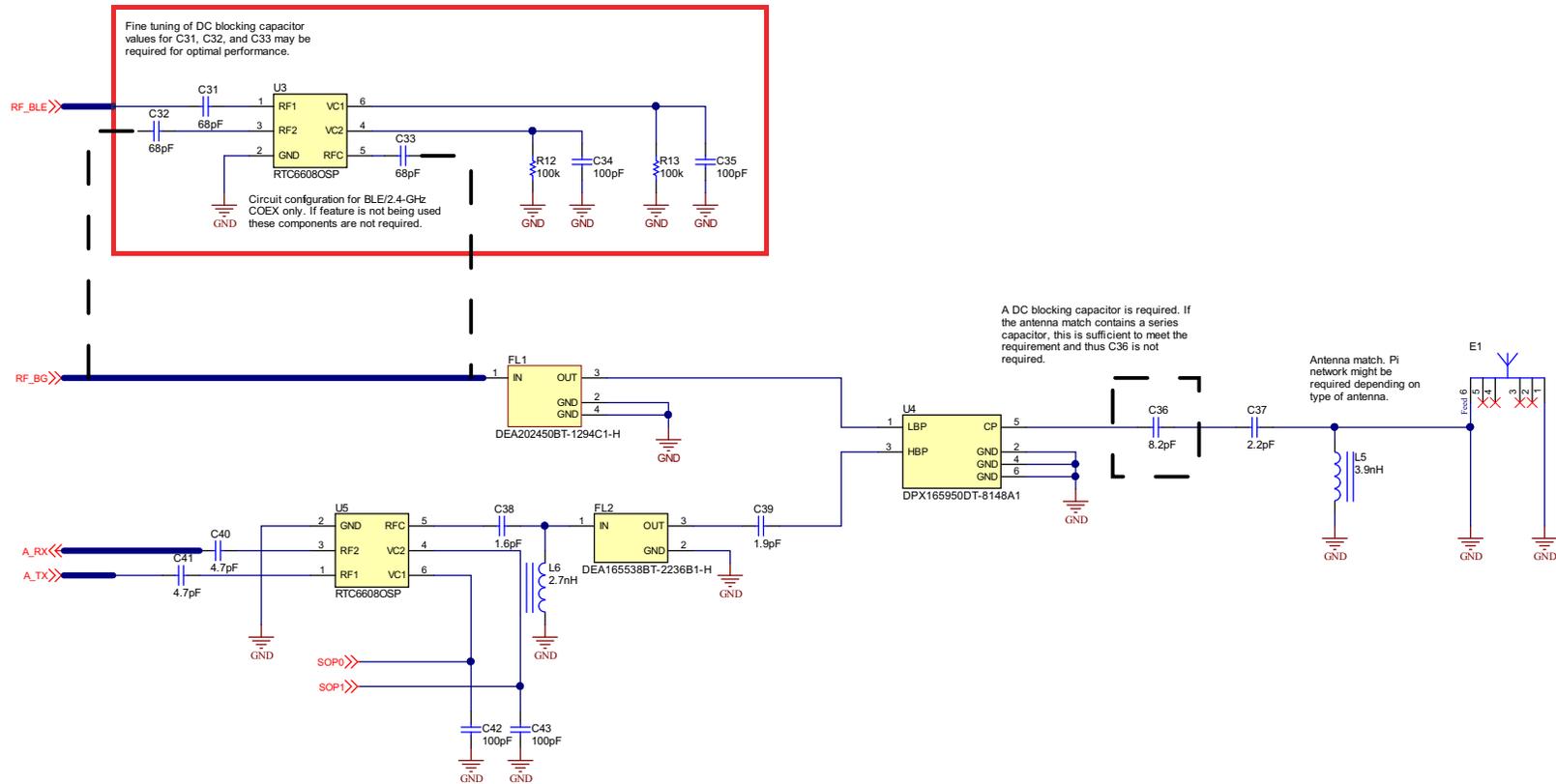
**Table 9-1. Bill of Materials for CC3235x Engine Area**

| Quantity | Designator                      | Value        | Manufacturer              | Part Number        | Description  |
|----------|---------------------------------|--------------|---------------------------|--------------------|--|
| 2        | C1, C2                          | 100 $\mu$ F  | Taiyo Yuden               | LMK325ABJ107MMHT   | CAP, CERM, 100 $\mu$ F, 10 V, +/- 20%, X5R, AEC-Q200 Grade 3, 1210 |
| 3        | C3, C4, C6                      | 4.7 $\mu$ F  | Taiyo Yuden               | JMK105BC6475MV-F   | CAP, CERM, 4.7 $\mu$ F, 6.3 V, +/- 20%, X6S, 0402                  |
| 3        | C5, C16, C29                    | 0.6 pF       | MuRata                    | GJM0335C1ER60BB01D | CAP, CERM, 0.6pF, 25 V, +/- 16%, C0G/NP0, 0201                     |
| 1        | C7                              | 0.5 pF       | Murata                    | GJM0335C1ER50BB01D | CAP, CERM, 0.5 pF, 25 V, +/- 20%, C0G/NP0, 0201                    |
| 7        | C8, C9, C11, C13, C21, C22, C24 | 0.1 $\mu$ F  | Walsin                    | CL05B104KO5NNNC    | CAP, CERM, 0.1 $\mu$ F, 16 V, +/- 10%, X7R, 0402                   |
| 1        | C10                             | 0.01 $\mu$ F | Walsin                    | 0402B103K500CT     | CAP, CERM, 0.01 $\mu$ F, 50 V, +/- 10%, X7R, 0402                  |
| 3        | C12, C20, C23                   | 10 $\mu$ F   | Taiyo Yuden               | LMK107BC6106MA-T   | CAP, CERM, 10 $\mu$ F, 10 V, +/- 20%, X6S, 0603                    |
| 1        | C14                             | 0.2 pF       | MuRata                    | GJM0335C1ER20BB01D | CAP, CERM, 0.2pF, 25 V, +/- 50%, C0G/NP0, 0201                     |
| 2        | C15, C25                        | 0.1 $\mu$ F  | Samsung Electro-Mechanics | CL03A104KP3NNNC    | CAP, CERM, 0.1 $\mu$ F, 10 V, +/- 10%, X5R, 0201                   |
| 2        | C17, C18                        | 22 $\mu$ F   | MuRata                    | GRM188C80G226ME15J | CAP, CERM, 22 $\mu$ F, 4 V, +/- 20%, X6S, 0603                     |
| 1        | C19                             | 1 $\mu$ F    | Walsin                    | CL05A105MP5NNNC    | CAP, CERM, 1 $\mu$ F, 10 V, +/- 20%, X5R, 0402                     |
| 2        | C26, C27                        | 10 pF        | Walsin                    | 0402N100J500CT     | CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0402                      |
| 2        | C28, C30                        | 6.2 pF       | Walsin                    | 0402N6R2C500CT     | CAP, CERM, 6.2 pF, 50 V, +/- 4%, C0G/NP0, 0402                     |
| 3        | J1, J2, J3                      |              | Würth Elektronik          | 61300311121        | Header, 2.54 mm, 3x1, Gold, TH                                     |
| 2        | L1, L3                          | 2.2 $\mu$ H  | MuRata                    | LQM2MPN2R2NG0      | Inductor, Multilayer, Ferrite, 2.2 $\mu$ H, 1.2 A, 0.11 ohm, SMD   |
| 1        | L2                              | 1 $\mu$ H    | MuRata                    | LQM2HPN1R0MG0L     | Inductor, Multilayer, Ferrite, 1 $\mu$ H, 1.6 A, 0.055 ohm, SMD    |
| 1        | L4 <sup>(1)</sup>               | 10 $\mu$ H   | TDK                       | MLP2520S100MT0S1   | Inductor, Multilayer, Ferrite, 10 $\mu$ H, 0.7 A, 0.364 ohm, SMD   |
| 5        | R1, R2, R3, R4, R9              | 100k         | Vishay-Dale               | CRCW0402100KJNED   | RES, 100 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402                    |
| 1        | R5 <sup>(2)</sup>               | 0            | Panasonic                 | ERJ-2GE0R00X       | RES, 0, 5%, 0.063 W, 0402  |
| 1        | R6                              | 270          | Vishay-Dale               | CRCW0402270RJNED   | RES, 270, 5%, 0.063 W, AEC-Q200 Grade 0, 0402                      |

**Table 9-1. Bill of Materials for CC3235x Engine Area (continued)**

| Quantity | Designator       | Value | Manufacturer                    | Part Number         | Description  |
|----------|------------------|-------|---------------------------------|---------------------|--|
| 4        | R7, R8, R10, R11 | 69.8k | Vishay-Dale                     | CRCW040269K8FKED    | RES, 69.8 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402   |
| 1        | U1               |       | Macronix International Co., LTD | MX25R3235FM1I0      | Ultra low power, 32M-bit [x 1/x 2/x 4] CMOS MXSMIO(serial multi I/O) Flash memory, SOP-8         |
| 1        | U2               |       | Texas Instruments               | CC3235SF12RGKR      | SimpleLink Wi-Fi and Internet-of-Things Solution, a Single-Chip Wireless MCU, RGK0064B (VQFN-64) |
| 1        | Y1               |       | Abrakon Corporation             | ABS07-32.768KHZ-9-T | Crystal, 32.768KHz, 9PF, SMD   |
| 1        | Y2               |       | TXC Corporation                 | 8Y40072002          | Crystal, 40 MHz, 8 pF, SMD   |

- (1) For the CC3235SF device, L4 is populated. For the CC3235S device, L4 is not populated.
- (2) For the CC3220SF device, R5 is not populated. For the CC3235S device if R5 is populated, Pin 45 can be used as GPIO\_31.



**Figure 9-8. CC3235x RF Schematic Implementation with and without Coexistence**

**Note**

The Following guidelines are recommended for implementation of the RF design:

- Ensure an RF path is designed with an impedance of 50Ω.
- Tuning of the antenna impedance π matching network is recommended after manufacturing of the PCB to account for PCB parasitics.
- π or L matching and tuning may be required between cascaded passive components on the RF path.

Table 9-2. Bill of Materials For CC3235x RF Section

| Quantity | Designator   | Value  | Manufacturer | Part Number          | Description  |
|----------|--|--------|--------------|----------------------|--|
| 3        | C31 <sup>(1)</sup> , C32 <sup>(1)</sup> , C33 <sup>(1)</sup> | 68 pF  | Murata       | GRM0335C1H680JA1D    | CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0201                                  |
| 4        | C34 <sup>(1)</sup> , C35 <sup>(1)</sup> , C42, C43           | 100 pF | Yageo        | CC0201JRNPO8BN101    | CAP, CERM, 100 pF, 25 V, +/- 5%, C0G/NP0, 0201                                 |
| 1        | C36  | 8.2 pF | Walsin       | 0402N8R2C500CT       | CAP, CERM, 8.2 pF, 50 V, +/- 3%, C0G/NP0, 0402                                 |
| 1        | C37  | 2.2 pF | MuRata       | GJM1555C1H2R2BB01D   | CAP, CERM, 2.2 pF, 50 V, +/- 4.5%, C0G/NP0, 0402                               |
| 1        | C38  | 1.6 pF | MuRata       | GRM0335C1H1R6BA01D   | CAP, CERM, 1.6 pF, 50 V, +/- 7%, C0G/NP0, 0201                                 |
| 1        | C39  | 1.9 pF | MuRata       | GJM1555C1H1R9WB01D   | CAP, CERM, 1.9 pF, 50 V, +/- 2.6%, C0G/NP0, 0402                               |
| 2        | C40, C41   | 4.7 pF | MuRata       | GRM0335C1H4R7BA01D   | CAP, CERM, 4.7 pF, 50 V, +/- 3%, C0G/NP0, 0201                                 |
| 1        | E1   |        | Ethertronics | M830520              | WLAN Antenna 802.11, SMD   |
| 1        | FL1  |        | TDK          | DEA202450BT-1294C1-H | Multilayer Chip Band Pass Filter For 2.4 GHz W-LAN/Bluetooth, SMD              |
| 1        | FL2  |        | TDK          | DEA165538BT-2236B1-H | Multilayer Band Pass Filter For 5 GHz W-LAN/LTE-U                              |
| 1        | L5   | 3.9 nH | MuRata       | LQG15HS3N9S02D       | Inductor, Multilayer, Air Core, 3.9 nH, 0.75 A, 0.14 ohm, SMD                  |
| 1        | L6   | 2.7 nH | MuRata       | LQG15WH2N7C02D       | Inductor, Multilayer, Air Core, 2.7 nH, 0.9 A, 0.07 ohm, AEC-Q200 Grade 1, SMD |
| 2        | R12 <sup>(1)</sup> , R13 <sup>(1)</sup>                      | 100k   | Vishay-Dale  | CRCW0402100KJNED     | RES, 100 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402                                |
| 2        | U3 <sup>(1)</sup> , U5                                       |        | Richwave     | RTC6608OSP           | 0.03 GHz-6 GHz SPDT Switch   |
| 1        | U4   |        | TDK          | DPX165950DT-8148A1   | Multilayer Diplexer for 2.4 GHz W-LAN & Bluetooth / 5 GHz W-LAN                |

(1) If the BLE/2.4GHz coexistence features is not used, these components are not required.

## 9.2 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC3235x VQFN device. Following these guidelines ensures that the design will minimize the risk with regulatory certifications including FCC, ETSI, and CE. For more information, see [CC3135 and CC3235 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines](#).

### 9.2.1 General PCB Guidelines

Use the following PCB guidelines:

- Verify the recommended PCB stackup in the PCB design guidelines, as well as the recommended layers for signals and ground.
- Ensure that the VQFN PCB footprint follows the information in [Section 12](#).
- Ensure that the VQFN PCB GND and solder paste follow the recommendations provided in [CC3135 and CC3235 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines](#).
- Decoupling capacitors must be as close as possible to the VQFN device.

### 9.2.2 Power Layout and Routing

Three critical DC/DC converters must be considered for the CC3235x device.

- Analog DC/DC converter
- PA DC/DC converter
- Digital DC/DC converter

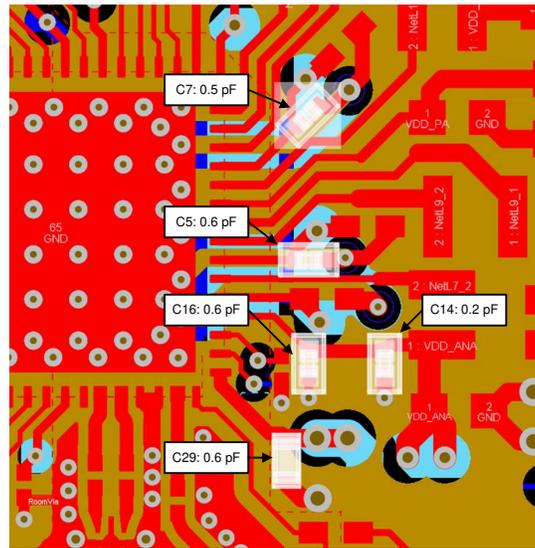
Each converter requires an external inductor and capacitor that must be laid out with care. DC current loops are formed when laying out the power components.

#### 9.2.2.1 Design Considerations

The following design guidelines must be followed when laying out the CC3235x device:

- Ground returns of the input decoupling capacitors (C13, C15, and C22) should be routed on Layer 2 using thick traces to isolate the RF ground from the noisy supply ground. This step is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be greater than 12 mils. Take special consideration for power amplifier supply lines (pins 33, 40, 41, and 42), and all input supply pins (pins 37, 39, and 44).
- Ensure the shortest grounding loop for the PLL supply decoupling capacitor (pin 24).
- Place all decoupling capacitors as close to the respective pins as possible.
- Power budget—the CC3235x device can consume up to 450mA for 3.3V, 670mA for 2.1V, for 24ms during the calibration cycle.
- Ensure the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24ms.
- The CC3235x device contains many high-current input pins. Ensure the trace feeding these pins can handle the following currents:
  - VIN\_DCDC\_PA input (pin 39) maximum 1A
  - VIN\_DCDC\_ANA input (pin 37) maximum 600mA
  - VIN\_DCDC\_DIG input (pin 44) maximum 500mA
  - DCDC\_PA\_SW\_P (pin 40) and DCDC\_PA\_SW\_N (pin 41) switching nodes maximum 1A
  - DCDC\_PA\_OUT output node (pin 42) maximum 1A
  - DCDC\_ANA\_SW switching node (pin 38) maximum 600mA
  - DCDC\_DIG\_SW switching node (pin 43) maximum 500mA
  - VDD\_PA\_IN supply (pin 33) maximum 500mA

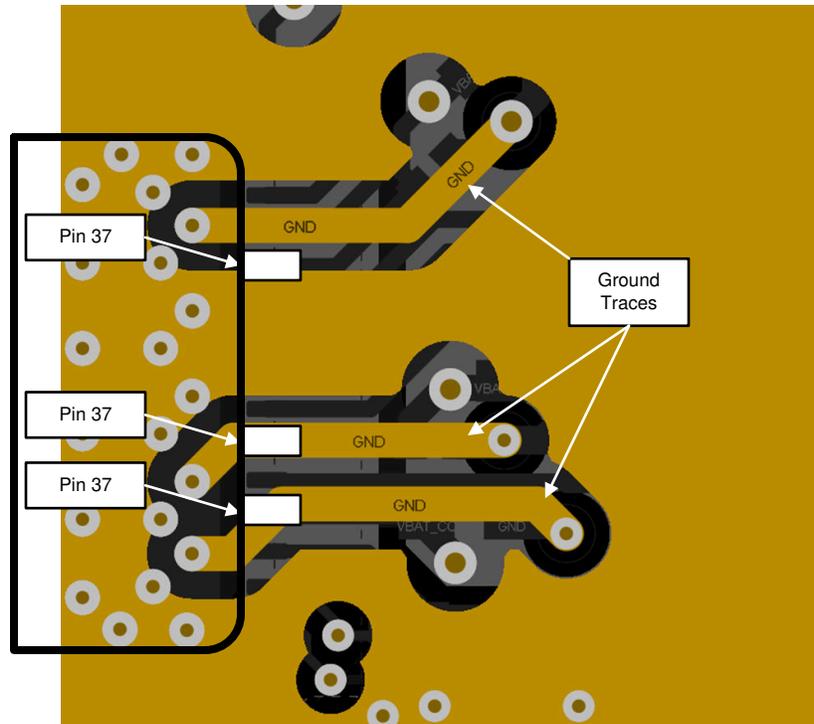
Figure 9-9 shows the ground routing for the input decoupling capacitors.



**Figure 9-9. Ground Routing for Input Decoupling Capacitors**

**Note**

The ground returns for the input capacitors are routed on layer two to reduce the EMI and improve the spectral mask. This routing must be strictly followed because it is critical for the overall performance of the device.



**Figure 9-10. Ground Returns for Input Capacitors**

### 9.2.3 Clock Interface Guidelines

The following guidelines are for the slow clock:

- The 32.768kHz crystal must be placed close to the VQFN package.
- Ensure the load capacitance is tuned according to the board parasitics to the frequency tolerance within  $\pm 150$ ppm.
- The ground plane on layer two is solid below the trace lanes, and there is ground around these traces on the top layer.

The following guidelines are for the fast clock:

- The 40MHz crystal must be placed close to the VQFN package.
- Ensure the load capacitance is tuned according to the board parasitics to the frequency tolerance within  $\pm 10$ ppm at room temperature. The total frequency across parts, temperature, and aging must be  $\pm 20$ ppm to meet the WLAN specification.
- To avoid noise degradation, ensure that no high-frequency lines are routed close to the routing of the crystal pins.
- Ensure that crystal tuning capacitors are close to the crystal pads.
- Both traces (XTAL\_N and XTAL\_P) should be as close as possible to parallel and approximately the same length.
- The ground plane on layer two is solid below the trace lines, and there should be ground around these traces on the top layer.
- For frequency tuning, see [CC31xx and CC32xx Frequency Tuning](#).

### 9.2.4 Digital Input and Output Guidelines

The following guidelines are for the digital I/Os:

- Route SPI and UART lines away from any RF traces.
- Keep the length of the high-speed lines as short as possible to avoid transmission line effects.
- Keep the line lower than 1/10 of the rise time of the signal to ignore transmission line effects (required if the traces cannot be kept short). Place the resistor at the source end closer to the device that is driving the signal.
- Add a series-terminating resistor for each high-speed line (for example, SPI\_CLK or SPI\_DATA) to match the driver impedance to the line. Typical terminating-resistor values range from  $27\Omega$  to  $36\Omega$  for a  $50\Omega$  line impedance.
- Route high-speed lines with a continuous ground reference plane below it to offer good impedance throughout. This routing also helps shield the trace against EMI.
- Avoid stubs on high-speed lines to minimize the reflections. If the line must be routed to multiple locations, use a separate line driver for each line.
- If the lines are longer compared to the rise time, add series-terminating resistors near the driver for each high-speed line to match the driver impedance to the line. Typical terminating-resistor values range from  $27\Omega$  to  $36\Omega$  for a  $50\Omega$  line impedance.

### 9.2.5 RF Interface Guidelines

The following guidelines are for the RF interface. Follow guidelines specified in the vendor-specific antenna design guides (including placement of the antenna). Also, see [CC3135 and CC3235 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines](#) for general antenna guidelines.

- Ensure that the antenna is matched for 50Ω. A  $\pi$ -matching network is recommended. Ensure that the  $\pi$  pad is available for tuning the matching network after PCB manufacture.
- A DC-blocking capacitor is required before the antenna. If the antenna matching network contains a series capacitor, this is sufficient to meet the requirement.
- Ensure that the area underneath the BPFs pads have a solid plane on layer 2 and that the minimum filter requirements are met.
- Ensure that the area underneath the RF switch pads have a solid plane on layer 2 and that the minimum switch isolation requirements are met.
- Ensure that the area underneath the diplexer pads have a solid plane on layer 2 and that the minimum diplexer requirements are met.
- Verify that the Wi-Fi RF trace is a 50Ω, impedance-controlled trace with a reference to solid ground.
- The RF trace bends must be made with gradual curves. Avoid 90-degree bends.
- The RF traces must not have sharp corners.
- There must be no traces or ground under the antenna section.
- The RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- For optimal antenna performance, ensure adequate ground plane around the antenna on all layers.
- Ensure RF connectors for conducted testing are isolated from the top layer ground using vias.
- Maintain a controlled pad to trace shapes using filleted edges if necessary to avoid mismatch.
- Diplexers, switches, BPF, and other elements on the RF route should be isolated from the top layer ground using vias.

## 10 Device and Documentation Support

### 10.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 10.2 Tools and Software

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

For the most up-to-date list of development tools and software, see the [CC3235 Tools & Software](#) product page. Users can also click the "Alert Me" button on the top right corner of the [CC3235 Tools & Software](#) page to stay informed about updates related to the CC3235x device.

#### Development Tools

##### [Pin Mux Tool](#)

The supported devices are: CC3200, CC3220x, and CC3235x.

The Pin Mux Tool is a software tool that provides a graphical user interface (GUI) for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for MPUs from TI. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customers' custom software. Version 3 of the Pin Mux Tool adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

##### [SimpleLink™ Wi-Fi® Starter Pro](#)

The supported devices are: CC3100, CC3200, CC3120R, CC3220x, CC3135 and CC3235x.

The SimpleLink™ Wi-Fi® Starter Pro mobile App is a new mobile application for SimpleLink™ provisioning. The app goes along with the embedded provisioning library and example that runs on the device side (see [SimpleLink™ Wi-Fi® SDK plugin](#) and [TI SimpleLink™ CC32XX Software Development Kit \(SDK\)](#)). The new provisioning release is a TI recommendation for Wi-Fi® provisioning using SimpleLink™ Wi-Fi® products. The provisioning release implements advanced AP mode and SmartConfig™ technology provisioning with feedback and fallback options to ensure successful process has been accomplished. Customers can use both embedded library and the mobile library for integration to their end products.

##### [SimpleLink™ CC32XX Software Development Kit \(SDK\)](#)

The CC3235x devices are supported.

The SimpleLink™ CC32XX SDK contains drivers for the CC3235 programmable MCU, more than 30 sample applications, and documentation needed to use the solution. It also contains the flash programmer, a command line tool for flashing software, configuring network and software parameters (SSID, access point channel, network profile, BS NIEW), system files, and user files (certificates, web pages, and more). This SDK can be used with TI's SimpleLink™ Wi-Fi® CC3235 LaunchPad™ development kits.

##### [Uniflash Standalone Flash Tool for TI Microcontrollers \(MCU\), Sitara Processors & SimpleLink Devices](#)

The supported devices are: CC3120R, CC3220x, CC3135 and CC3235x.

CCS Uniflash is a standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara™ processors. Uniflash has a GUI, command line, and scripting interface. CCS Uniflash is available free of charge.

**SimpleLink™ Wi-Fi®  
Radio Testing Tool**

The supported devices are: CC3100, CC3200, CC3120R, CC3220, CC3135 and CC3235x.

The SimpleLink™ Wi-Fi® Radio Testing Tool is a Windows-based software tool for RF evaluation and testing of SimpleLink™ Wi-Fi® CC3x20 and CC3x35 designs during development and certification. The tool enables low-level radio testing capabilities by manually setting the radio into transmit or receive modes. Using the tool requires familiarity and knowledge of radio circuit theory and radio test methods.

Created for the internet-of-things (IoT), the SimpleLink™ Wi-Fi® CC31xx and CC32xx family of devices include on-chip Wi-Fi®, Internet, and robust security protocols with no prior Wi-Fi® experience needed for faster development. For more information on these devices, visit [SimpleLink™ Wi-Fi® family](#), [Internet-on-a chip™ solutions](#).

**UniFlash Standalone  
Flash Tool for TI  
Microcontrollers (MCU),  
Sitara™ Processors  
and SimpleLink™  
Devices**

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara™ processors. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

**TI Designs and Reference Designs**

The [TI Designs Reference Design Library](#) is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jumpstart your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

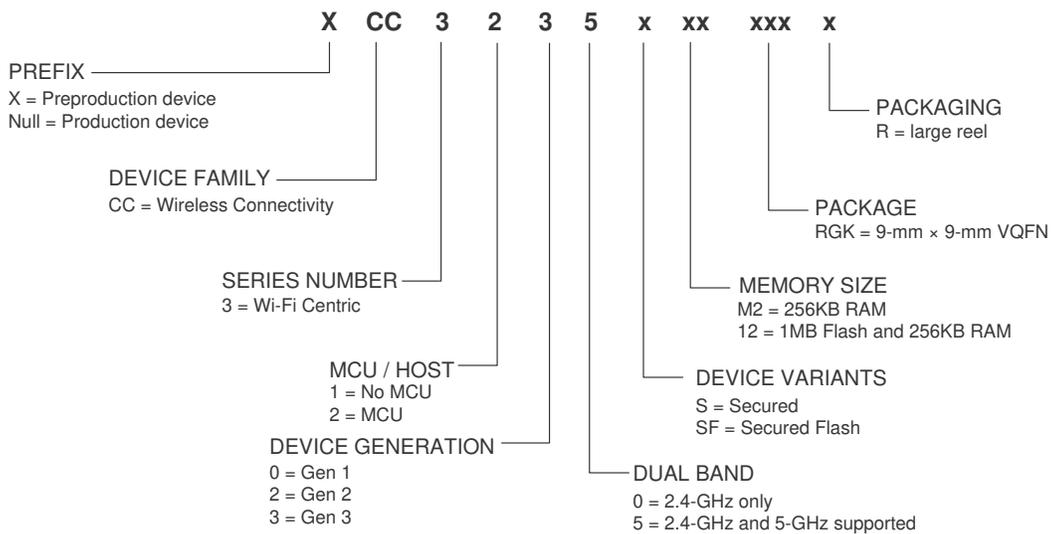
**10.3 Firmware Updates**

TI updates features in the service pack for this module with no published schedule. Due to the ongoing changes, TI recommends that the user has the latest service pack in their module for production.

To stay informed, click the SDK “Alert me” button the top right corner of the product page, or visit [SimpleLink™ CC32XX SDK](#).

**10.4 Device Nomenclature**

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3235x device and support tools (see [Figure 10-1](#)).



**Figure 10-1. CC3235x Device Nomenclature**

## 10.5 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](http://ti.com) (CC3235). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document. The current documentation that describes the processor, related peripherals, and other technical collateral follows.

The following documents provide support for the CC3235 device.

### Application Reports

- [CC3135 and CC3235 SimpleLink™ Wi-Fi® Embedded Programming User Guide](#) CC3135 and CC3235 SimpleLink Wi-Fi Embedded Programming User Guide
- [SimpleLink™ CC3135, CC3235 Wi-Fi® Internet-on-a chip™ Networking Sub-System Power Management](#) This application report describes the best practices for power management and extended battery life for embedded low-power Wi-Fi devices such as the SimpleLink Wi-Fi Internet-on-a chip solution from Texas Instruments.
- [SimpleLink™ CC31xx, CC32xx Wi-Fi® Internet-on-a chip™ Solution Built-In Security Features](#) The SimpleLink Wi-Fi CC31xx and CC32xx Internet-on-a chip family of devices from Texas Instruments offer a wide range of built-in security features to help developers address a variety of security needs, which is achieved without any processing burden on the main microcontroller (MCU). This document describes these security-related features and provides recommendations for leveraging each in the context of practical system implementation.
- [SimpleLink™ CC3135, CC3235 Wi-Fi® and Internet-of-Things Over-the-Air Update](#) This document describes the OTA library for the SimpleLink Wi-Fi CC3x35 family of devices from Texas Instruments and explains how to prepare a new cloud-ready update to be downloaded by the OTA library.
- [SimpleLink™ CC3135, CC3235 Wi-Fi® Internet-on-a chip™ Solution Device Provisioning](#) This guide describes the provisioning process, which provides the SimpleLink Wi-Fi device with the information (network name, password, and so forth) needed to connect to a wireless network.
- [Transfer of TI's Wi-Fi® Alliance Certifications to Products Based on SimpleLink™](#) This document explains how to employ the Wi-Fi® Alliance (WFA) derivative certification transfer policy to transfer a WFA certification, already obtained by Texas Instruments, to a system you have developed.
- [Using Serial Flash on SimpleLink™ CC3135 and CC3235 Wi-Fi® and Internet-of-Things Devices](#) This application note is divided into two parts. The first part provides important guidelines and best-practice design techniques to consider when choosing and embedding a serial Flash paired with the CC3135 and CC3235 (CC3x35) devices. The second part describes the file system, along with guidelines and considerations for system designers working with the CC3x35 devices.

## User's Guides

[SimpleLink™ Wi-Fi® and Internet-of-Things CC31xx and CC32xx Network Processor](#) This document provides software (SW) programmers with all of the required knowledge for working with the networking subsystem of the SimpleLink Wi-Fi devices. This guide provides basic guidelines for writing robust, optimized networking host applications, and describes the capabilities of the networking subsystem. The guide contains some example code snapshots, to give users an idea of how to work with the host driver. More comprehensive code examples can be found in the formal software development kit (SDK). This guide does not provide a detailed description of the host driver APIs.

[SimpleLink™ CC3135 and CC3235 Wi-Fi® and IoT Solution Layout Guidelines](#) This document provides the design guidelines of the 4-layer PCB used for the CC3135 and CC3235 SimpleLink Wi-Fi family of devices from Texas Instruments. The CC3135 and CC3235 devices are easy to lay out and are available in quad flat no-leads (QFNS) packages. When designing the board, follow the suggestions in this document to optimize performance of the board.

[SimpleLink™ CC3235 Wi-Fi® LaunchPad™ Development Kit Hardware](#) The CC3235 SimpleLink LaunchPad Development Kit (LAUNCHXL-CC3235) is a cost-conscious evaluation platform for Arm Cortex-M4-based MCUs. The LaunchPad design highlights the CC3235 Internet-on-a chip solution and Wi-Fi capabilities. The CC3235 LaunchPad also features temperature and accelerometer sensors, programmable user buttons, three LEDs for custom applications, and onboard emulation for debugging. The stackable headers of the CC3235 LaunchPad XL interface demonstrate how easy it is to expand the functionality of the LaunchPad when interfacing with other peripherals on many existing BoosterPack™ Plug-in Module add-on boards, such as graphical displays, audio codecs, antenna selection, environmental sensing, and more.

[SimpleLink™ Wi-Fi® and Internet-on-a chip™ CC3135 and CC3235 Solution Radio Tool](#) The Radio Tool serves as a control panel for direct access to the radio, and can be used for both the radio frequency (RF) evaluation and for certification purposes. This guide describes how to have the tool work seamlessly on Texas Instruments evaluation platforms such as the BoosterPack™ plus FTDI emulation board for CC3235 devices, and the LaunchPad™ for CC3235 devices.

[SimpleLink™ Wi-Fi® CC3135 and CC3235 Provisioning for Mobile Applications](#) This guide describes TI's SimpleLink Wi-Fi provisioning solution for mobile applications, specifically on the usage of the Android™ and IOS® building blocks for UI requirements, networking, and provisioning APIs required for building the mobile application.

## More Literature

[CC3235 SimpleLink™ Wi-Fi® and Internet of Things Technical Reference Manual](#) This technical reference manual details the modules and peripherals of the CC3235 SimpleLink™ Wi-Fi® MCU. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals may be present on all devices. Pin functions, internal signal connections, and operational parameters differ from device to device. The user should consult the device-specific data sheet for these details.

[CC3x35 SimpleLink™ Wi-Fi® Hardware Design Checklist](#)

[CC3235S/CC3235SF SimpleLink™ Wi-Fi® LaunchPad™ Design Files](#)

## 10.6 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 10-1. Related Links**

| PARTS    | PRODUCT FOLDER             | ORDER NOW                  | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| CC3235S  | <a href="#">Click here</a> |
| CC3235SF | <a href="#">Click here</a> |

## 10.7 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 10.9 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.10 Export Control Notice

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## 10.11 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

**Changes from May 13, 2021 to December 11, 2024 (from Revision D (May 2021) to Revision E (December 2024))**

|   | Page |
|---|------|
| • Added the note on the TLS socket for WPA Enterprise security modes in <a href="#">Section 8.3.1</a> ..... | 62   |

**Changes from May 5, 2020 to May 13, 2021 (from Revision C (May 2020) to Revision D (May 2021))**

**Page**

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- Added "WPA3 Enterprise" to [Section 1](#) ..... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added "WPA3 personal and enterprise" to [Section 8.3](#) .....61
- Changed footnote in [Section 8.3](#) ..... 61
- Added WPA3 Enterprise to [Section 8.3.1](#) .....62
- Added WPA3 enterprise to Wi-Fi security Feature in [Table 8-1](#) ..... 62
- Changed tablenote for [Table 8-1](#) ..... 62

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## **12 Mechanical, Packaging, and Orderable Information**

### **12.1 Packaging Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 12.1.1 Packaging Option Addendum

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish <sup>(3)</sup> | MSL Peak Temp <sup>(4)</sup> | Op Temp (°C) | Device Marking <sup>(5) (6)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|---------------------------------|------------------------------|--------------|-----------------------------------|
| CC3235SM2RGKR    | ACTIVE                | VQFN         | RGK             | 64   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU NIPDAUAG         | Level-3-260C-168 HR          | -40 to 85    | CC3235SM2                         |
| CC3235SF12RGKR   | ACTIVE                | VQFN         | RGK             | 64   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU NIPDAUAG         | Level-3-260C-168 HR          | -40 to 85    | CC3235SF12                        |

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD:** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.  
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## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CC3235SF12RGKR</a> | Active        | Production           | VQFN (RGK)   64 | 2500   LARGE T&R      | Yes         | NIPDAU   NIPDAUAG                    | Level-3-260C-168 HR               | -40 to 85    | CC3235SF<br>12      |
| <a href="#">CC3235SM2RGKR</a>  | Active        | Production           | VQFN (RGK)   64 | 2500   LARGE T&R      | Yes         | NIPDAU   NIPDAUAG                    | Level-3-260C-168 HR               | -40 to 85    | CC3235S<br>M2       |
| CC3235SM2RGKR.B                | Active        | Production           | VQFN (RGK)   64 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | CC3235S<br>M2       |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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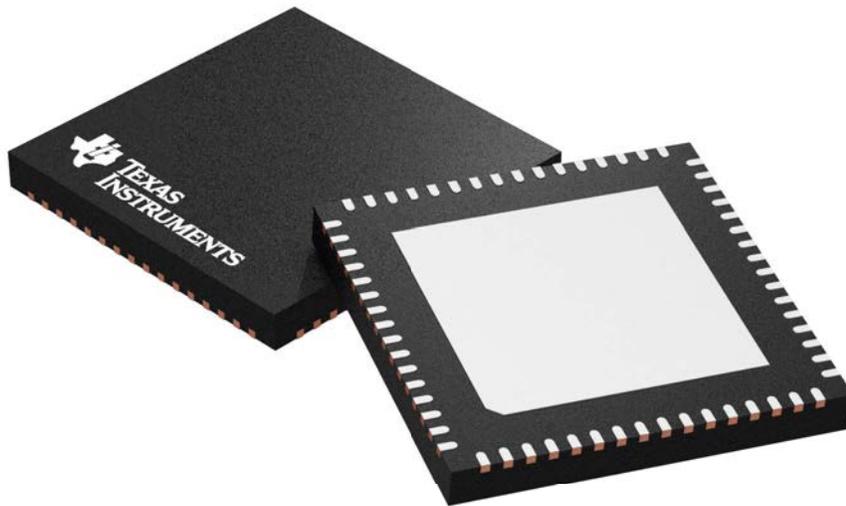
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**RGK 64**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

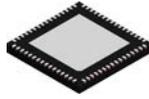
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211520/D

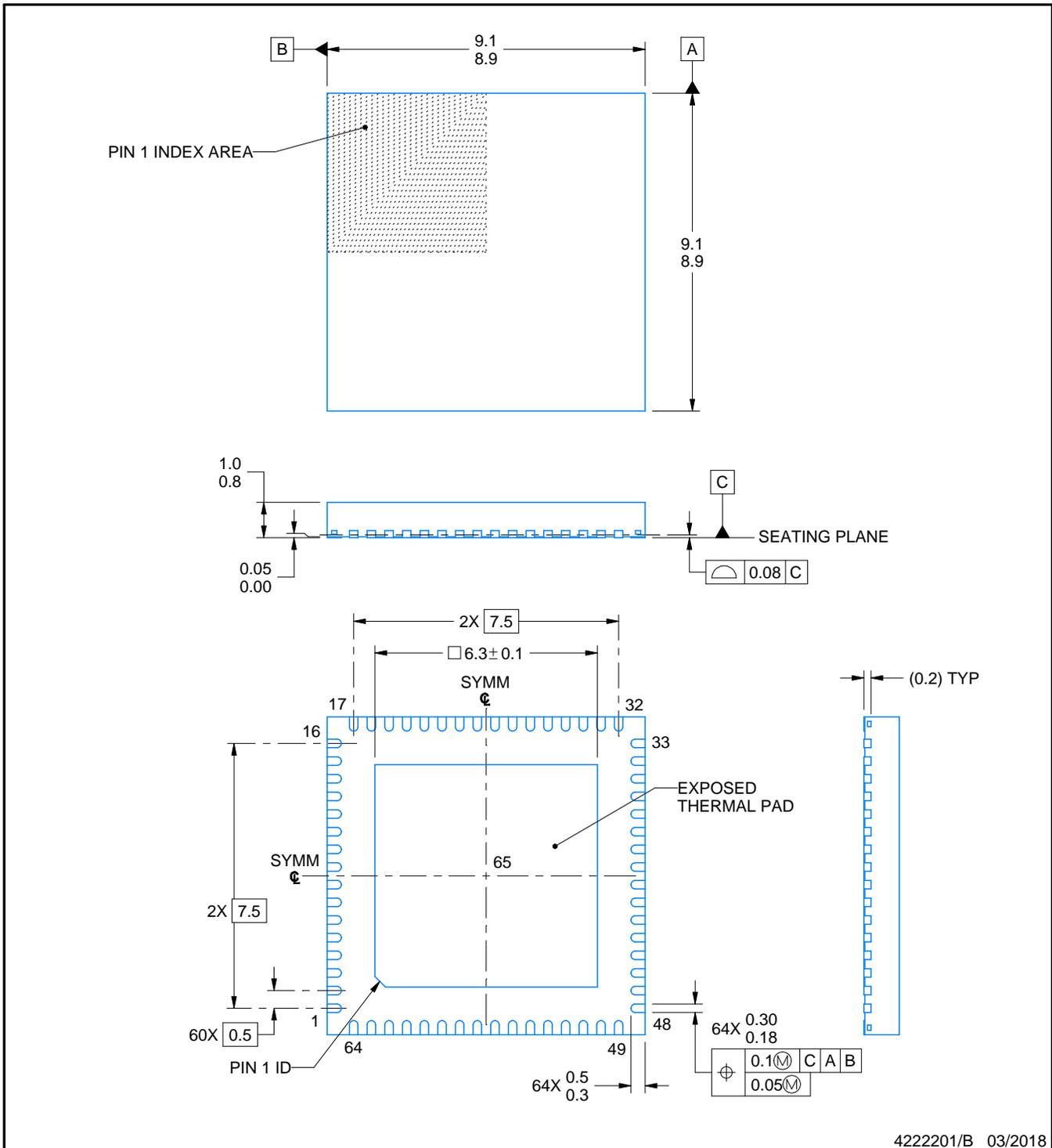
# RGK0064B



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4222201/B 03/2018

### NOTES:

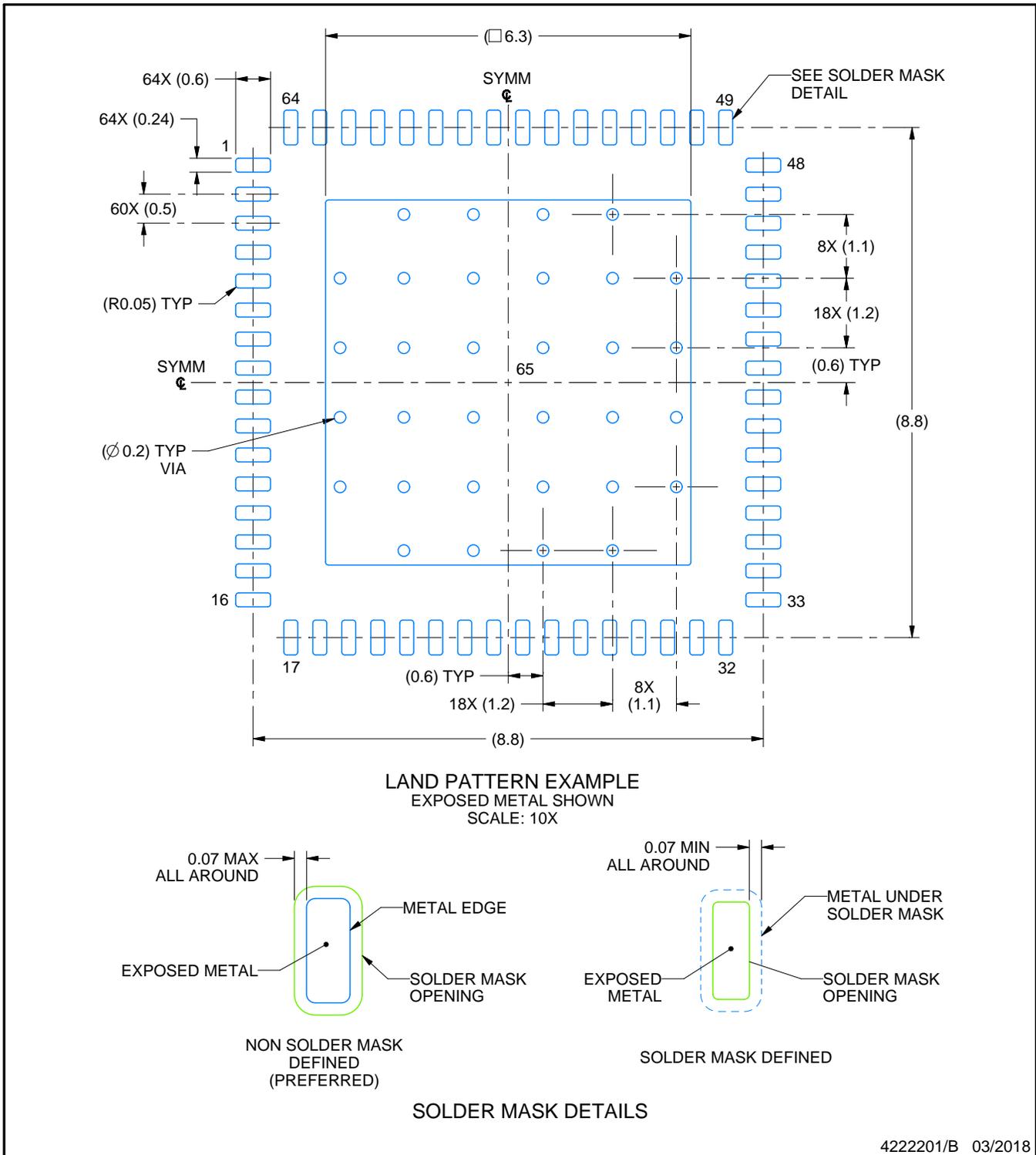
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

**RGK0064B**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES: (continued)

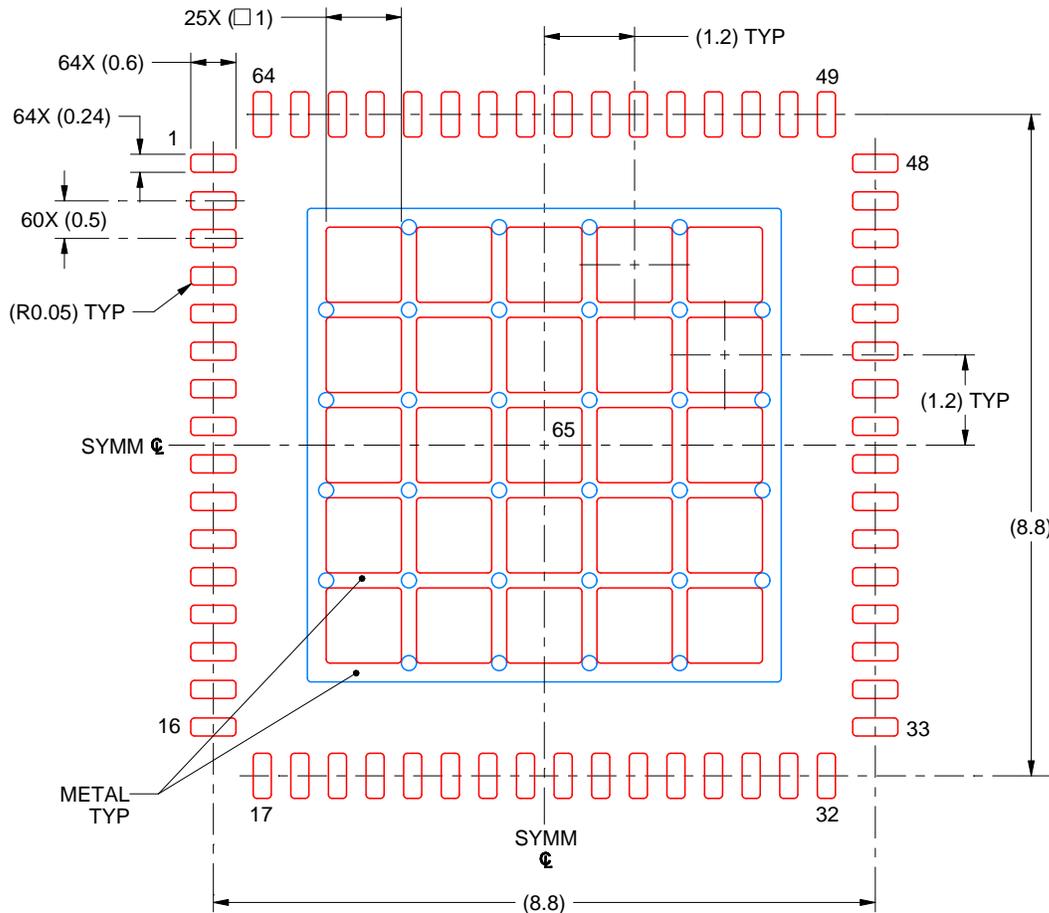
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGK0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.1 MM THICK STENCIL  
 SCALE: 10X

EXPOSED PAD 65  
 63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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