

ADC34J2x Quad-Channel, 12-Bit, 50-MSPS to 160-MSPS, Analog-to-Digital Converter with JESD204B Interface

1 Features

- Quad Channel
- 12-Bit Resolution
- Single 1.8-V Supply
- Flexible Input Clock Buffer with Divide-by-1, -2, -4
- SNR = 69.6 dBFS, SFDR = 86 dBc at $f_{IN} = 70$ MHz
- Ultra-Low Power Consumption:
 - 203 mW/Ch at 160 MSPS
- Channel Isolation: 105 dB
- Internal Dither
- JESD204B Serial Interface:
 - Subclass 0, 1, 2 Compliant up to 3.2 Gbps
 - Supports One Lane per ADC up to 160 MSPS
- Support for Multi-Chip Synchronization
- Pin-to-Pin Compatible with 14-Bit Version
- Package: VQFN-48 (7 mm x 7 mm)

2 Applications

- Multi-Carrier, Multi-Mode Cellular Base Stations
- Radar and Smart Antenna Arrays
- Munitions Guidance
- Motor Control Feedback
- Network and Vector Analyzers
- Communications Test Equipment
- Nondestructive Testing
- Microwave Receivers
- Software Defined Radios (SDRs)
- Quadrature and Diversity Radio Receivers

3 Description

The ADC34J2x are a high-linearity, ultra-low power, dual-channel, 12-bit, 50-MSPS to 160-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. A clock input divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The devices support JESD204B interfaces in order to reduce the number of interface lines, thus allowing for high system integration density. The JESD204B interface is a serial interface, where the data of each ADC are serialized and output over only one differential pair. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock by 20 to derive the bit clock that is used to serialize the 12-bit data from each channel. The devices support subclass 1 with interface speeds up to 3.2 Gbps.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	SAMPLING RATE (MSPS)
ADC34J22	VQFN (48)	50
ADC34J23		80
ADC34J24		125
ADC34J25		160

(1) For all available packages, see the orderable addendum at the end of the datasheet.

FFT with Dither On
($f_s = 160$ MSPS, $f_{IN} = 10$ MHz, SNR = 70.3 dBFS, SFDR = 84 dBc)

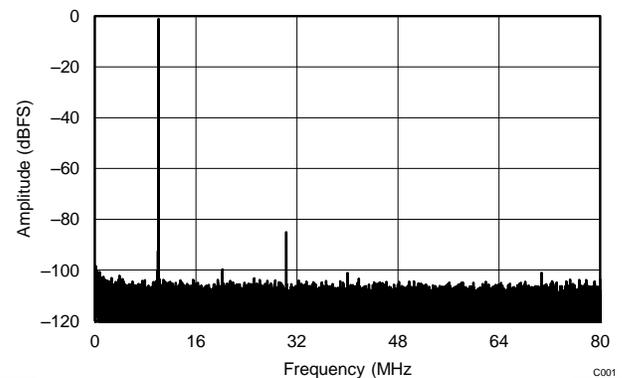


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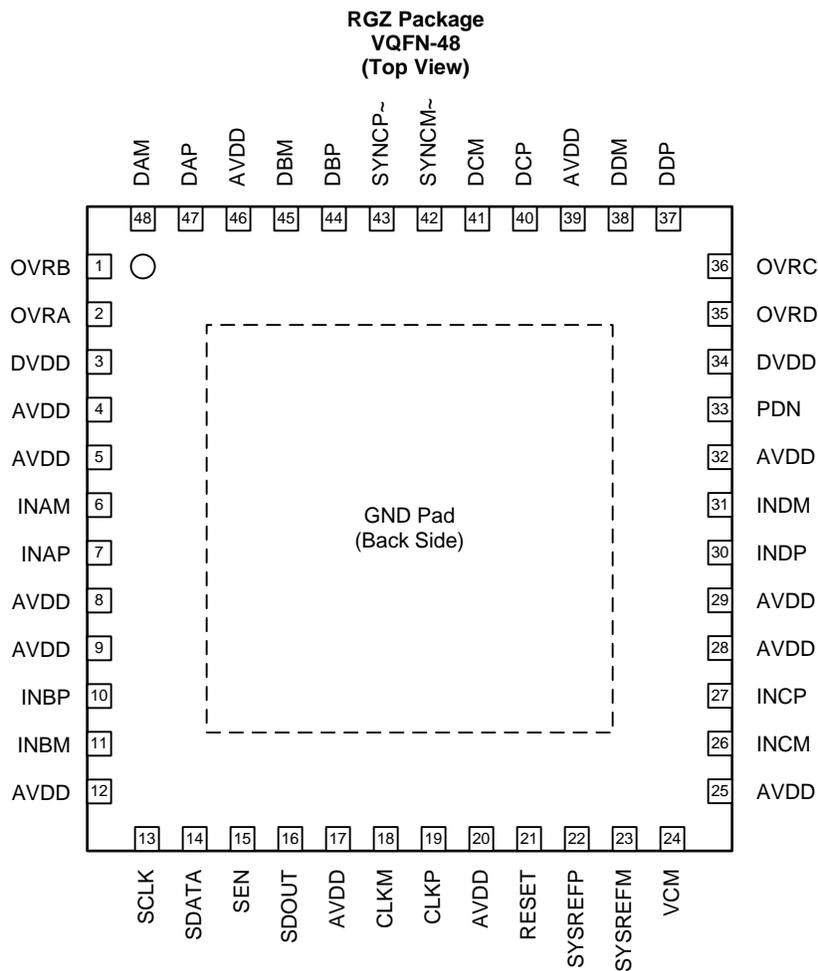
4 Revision History

Changes from Original (May 2014) to Revision A	Page
• Changed document status from product preview to production data.....	1

5 Device Comparison Table

INTERFACE	RESOLUTION (Bits)	25 MSPS	50 MSPS	80 MSPS	125 MSPS	160 MSPS
Serial LVDS	12	ADC3421	ADC3422	ADC3423	ADC3424	—
	14	ADC3441	ADC3442	ADC3443	ADC3444	—
JESD204B	12	—	ADC34J22	ADC34J23	ADC34J24	ADC34J25
	14	—	ADC34J42	ADC34J43	ADC34J44	ADC34J45

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	4, 5, 8, 9, 12, 17, 20, 25, 28, 29, 32, 39, 46	I	Analog 1.8-V power supply
CLKM	18	I	Negative differential clock input for the ADC
CLKP	19	I	Positive differential clock input for the ADC
DAM	48	O	Negative serial JESD204B output for channel A
DAP	47	O	Positive serial JESD204B output for channel A
DBM	45	O	Negative serial JESD204B output for channel B
DBP	44	O	Positive serial JESD204B output for channel B
DCM	41	O	Negative serial JESD204B output for channel C
DCP	40	O	Positive serial JESD204B output for channel C
DDM	38	O	Negative serial JESD204B output for channel D
DDP	37	O	Positive serial JESD204B output for channel D
DVDD	3, 34	I	Digital 1.8-V power supply
GND	PowerPAD™	I	Ground, 0 V
INAM	6	I	Negative differential analog input for channel A
INAP	7	I	Positive differential analog input for channel A
INBM	11	I	Negative differential analog input for channel B
INBP	10	I	Positive differential analog input for channel B
INCM	26	I	Negative differential analog input for channel C
INCP	27	I	Positive differential analog input for channel C
INDM	31	I	Negative differential analog input for channel D
INDP	30	I	Positive differential analog input for channel D
OVRA	2	O	Overrange indicator for channel A
OVRB	1	O	Overrange indicator for channel B
OVRC	36	O	Overrange indicator for channel C
OVRD	35	O	Overrange indicator for channel D
PDN	33	I	Power-down control. This pin has an internal 150-kΩ pull-down resistor.
RESET	21	I	Hardware reset; active high. This pin has an internal 150-kΩ, pull-down resistor.
SCLK	13	I	Serial interface clock input. This pin has an internal 150-kΩ pull-down resistor.
SDATA	14	I	Serial interface data input. This pin has an internal 150-kΩ pull-down resistor.
SDOUT	16	O	Serial interface data output
SEN	15	I	Serial interface enable. Active low. This pin has an internal 150-kΩ pull-up resistor to AVDD.
SYNCM~	42	I	Negative JESD204B synch input
SYNCP~	43	I	Positive JESD204B synch input
SYSREFM	23	I	Negative external SYSREF input
SYSREFP	22	I	Positive external SYSREF input
VCM	24	O	Common-mode voltage output for the analog inputs

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Supply voltage range, AVDD		-0.3	2.1	V
Supply voltage range, DVDD		-0.3	2.1	V
Voltage applied to input pins:	INAP, INBP, INCP, INDP, INAM, INBM, INCM, INDM	-0.3	Minimum (AVDD + 0.3, 2.1)	V
	CLKP, CLKM ⁽²⁾	-0.3	Minimum (AVDD + 0.3, 2.1)	V
	SYSREFP, SYSREFM, SYNCP~, SYNCM~	-0.3	Minimum (AVDD + 0.3, 2.1)	V
	SCLK, SEN, SDATA, RESET, PDN	-0.3	3.6	V
Temperature	Operating free-air, T _A	-40	85	°C
	Operating junction, T _J		125	°C
	Storage, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP, CLKM is less than |0.3 V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLIES					
AVDD	Analog supply voltage range	1.7	1.8	1.9	V
DVDD	Digital supply voltage range	1.7	1.8	1.9	V
ANALOG INPUT					
V _{ID}	Differential input voltage	For input frequencies < 450 MHz		2	V _{PP}
		For input frequencies < 600 MHz		1	V _{PP}
V _{IC}	Input common-mode voltage	VCM ± 0.025			V
CLOCK INPUT					
Input clock frequency		Sampling clock frequency		25	160 ⁽²⁾ MSPS
Input clock amplitude (differential)	Sine wave, ac-coupled		0.2	1.5	V
	LPECL, ac-coupled			1.6	V
	LVDS, ac-coupled			0.7	V
Input clock duty cycle		35	50	65	%
Input clock common-mode voltage			0.95		V
DIGITAL OUTPUTS					
C _{LOAD}	Maximum external load capacitance from each output pin to GND		3.3		pF
R _{LOAD}	Single-ended load resistance		100		Ω

- (1) After power-up, to reset the device for the first time, only use the RESET pin; see the Register Initialization section.
- (2) With the clock divider enabled by default for divide-by-1. Maximum sampling clock frequency for the divide-by-4 option is 640 MSPS.

7.4 Summary of Special Mode Registers

Table 1 lists the location, value, and functions of special mode registers in the device.

Table 1. Special Modes Summary

MODE		LOCATION	VALUE AND FUNCTION
Dither mode	DIS DITH CHA	01h [7:6], 134h[5,3]	Creates a noise floor cleaner and improves SFDR; see the Internal Dither Algorithm section. 0000 = Dither disabled 1111 = Dither enabled
	DIS DITH CHB	01h [5:4], 434h[5,3]	
	DIS DITH CHC	01h [3:2], 534h[5,3]	
	DIS DITH CHD	01h [1:0], 234h[5,3]	
Special mode 1	SPECIAL MODE 1 CHA	06h[4:2]	Use for better HD3. 000 = Default after reset 010 = Use for frequency < 120 MHz 111 = Use for frequency > 120 MHz
	SPECIAL MODE 1 CHB	07h[4:2]	
	SPECIAL MODE 1 CHC	08h[4:2]	
	SPECIAL MODE 1 CHD	09h[4:2]	
Special mode 2	SPECIAL MODE 2 CHA	122h[1:0]	Helps improve HD2. 00 = Default after reset 11 = Improves HD2
	SPECIAL MODE 2 CHB	422h[1:0]	
	SPECIAL MODE 2 CHC	522h[1:0]	
	SPECIAL MODE 2 CHD	222h[1:0]	

7.5 Thermal Information

THERMAL METRIC ⁽¹⁾		ADC34J2x	UNIT
		RGZ (VQFN)	
		48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.0	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.6 Electrical Characteristics: ADC34J24, ADC34J25

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, maximum sampling rate, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	ADC34J24			ADC34J25			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			125			160	MSPS
Resolution	12			12			Bits
1.8-V analog supply (AVDD) current		318	490		354	490	mA
1.8-V digital supply current		79	150		97	150	mA
Total power dissipation		715	1010		812	1010	mW
Global power-down dissipation		22			22		mW
Wake-up time from global power-down		85	100		85	100	μs
Standby power-down dissipation		177			185		mW
Wake-up time from standby power-down		35	300		35	300	μs

7.7 Electrical Characteristics: ADC34J22, ADC34J23

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, maximum sampling rate, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	ADC34J22			ADC34J23			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
ADC clock frequency			50			80	MSPS
Resolution	12			12			Bits
1.8-V analog supply current		233	490		269	490	mA
1.8-V digital supply current		39	150		56	150	mA
Total power dissipation		491	1010		584	1010	mW
Global power-down dissipation		22			22		mW
Wake-up time from global power-down		85	100		85	100	μs
Standby power-down dissipation		155			166		mW
Wake-up time from standby power-down		35	300		35	300	μs

7.8 Electrical Characteristics: General

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, Maximum sampling rate, 50% clock duty cycle, $AV_{\text{DD}} = DV_{\text{DD}} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Differential input full-scale			2.0		V_{PP}
r_i	Input resistance	Differential at dc		6.5		$\text{k}\Omega$
c_i	Input capacitance	Differential at dc		5.2		pF
$V_{\text{OC(VCM)}}$	VCM common-mode voltage output			0.95		V
	VCM output current capability			10		mA
	Input common-mode current	Per analog input pin		1.5		$\mu\text{A/MSPS}$
	Analog input bandwidth (3 dB)	50- Ω differential source driving 50- Ω termination across INP and INM		450		MHz
DC ACCURACY						
E_{O}	Offset error		-20		20	mV
$E_{\text{G(REF)}}$	Gain error as a result of internal reference inaccuracy alone		-3		3	%FS
$E_{\text{G(CHAN)}}$	Gain error of channel alone			± 1		%FS
CHANNEL-TO-CHANNEL ISOLATION						
Crosstalk ⁽¹⁾	$f_{\text{IN}} = 10\text{ MHz}$	Near channel		105		dB
		Far channel		105		dB
	$f_{\text{IN}} = 100\text{ MHz}$	Near channel		95		dB
		Far channel		105		dB
	$f_{\text{IN}} = 200\text{ MHz}$	Near channel		94		dB
		Far channel		105		dB
	$f_{\text{IN}} = 230\text{ MHz}$	Near channel		93		dB
		Far channel		105		dB
	$f_{\text{IN}} = 300\text{ MHz}$	Near channel		85		dB
		Far channel		105		dB

(1) Crosstalk is measured with a -1-dBFS input signal on aggressor channel and no input on victim channel.

7.9 AC Performance: ADC34J25

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC34J25 ($f_s = 160\text{ MSPS}$)						UNIT	
		DITHER ON			DITHER OFF				
		MIN	TYP	MAX	MIN	TYP	MAX		
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	$f_{\text{IN}} = 10\text{ MHz}$	70.2			70.4			dBFS
		$f_{\text{IN}} = 70\text{ MHz}$	68.5	69.6		69.9			
		$f_{\text{IN}} = 100\text{ MHz}$	69.3			69.6			
		$f_{\text{IN}} = 170\text{ MHz}$	68.4			68.9			
		$f_{\text{IN}} = 230\text{ MHz}$	67.5			68.1			
NSD	Noise spectral density (averaged across Nyquist zone)	$f_{\text{IN}} = 10\text{ MHz}$	149.2			149.4			dBFS/Hz
		$f_{\text{IN}} = 70\text{ MHz}$	147.5	148.6		148.9			
		$f_{\text{IN}} = 100\text{ MHz}$	148.3			148.6			
		$f_{\text{IN}} = 170\text{ MHz}$	147.4			147.9			
		$f_{\text{IN}} = 230\text{ MHz}$	146.5			147.1			
SINAD	Signal-to-noise and distortion ratio	$f_{\text{IN}} = 10\text{ MHz}$	70.1			70.3			dBFS
		$f_{\text{IN}} = 70\text{ MHz}$	67.6	69.5		69.7			
		$f_{\text{IN}} = 100\text{ MHz}$	69.2			69.4			
		$f_{\text{IN}} = 170\text{ MHz}$	68.2			68.6			
		$f_{\text{IN}} = 230\text{ MHz}$	67.2			67.5			
ENOB	Effective number of bits	$f_{\text{IN}} = 10\text{ MHz}$	11.4			11.4			Bits
		$f_{\text{IN}} = 70\text{ MHz}$	10.9	11.3		11.3			
		$f_{\text{IN}} = 100\text{ MHz}$	11.2			11.3			
		$f_{\text{IN}} = 170\text{ MHz}$	11.1			11.1			
		$f_{\text{IN}} = 230\text{ MHz}$	10.9			10.9			
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 10\text{ MHz}$	85			86			dBc
		$f_{\text{IN}} = 70\text{ MHz}$	81	86		85			
		$f_{\text{IN}} = 100\text{ MHz}$	86			87			
		$f_{\text{IN}} = 170\text{ MHz}$	85			84			
		$f_{\text{IN}} = 230\text{ MHz}$	81			80			
HD2	Second harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$	91			92			dBc
		$f_{\text{IN}} = 70\text{ MHz}$	81	94		93			
		$f_{\text{IN}} = 100\text{ MHz}$	93			91			
		$f_{\text{IN}} = 170\text{ MHz}$	83			83			
		$f_{\text{IN}} = 230\text{ MHz}$	81			79			
HD3	Third harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$	85			86			dBc
		$f_{\text{IN}} = 70\text{ MHz}$	81	85		85			
		$f_{\text{IN}} = 100\text{ MHz}$	86			87			
		$f_{\text{IN}} = 170\text{ MHz}$	93			87			
		$f_{\text{IN}} = 230\text{ MHz}$	85			82			
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	$f_{\text{IN}} = 10\text{ MHz}$	98			94			dBc
		$f_{\text{IN}} = 70\text{ MHz}$	87	97		94			
		$f_{\text{IN}} = 100\text{ MHz}$	96			93			
		$f_{\text{IN}} = 170\text{ MHz}$	92			92			
		$f_{\text{IN}} = 230\text{ MHz}$	90			89			

AC Performance: ADC34J25 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC34J25 ($f_S = 160\text{ MSPS}$)						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
THD Total harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		84			83		dBc
	$f_{\text{IN}} = 70\text{ MHz}$	76.5	84			83		
	$f_{\text{IN}} = 100\text{ MHz}$		84			84		
	$f_{\text{IN}} = 170\text{ MHz}$		82			80		
	$f_{\text{IN}} = 230\text{ MHz}$		78			76		
IMD3 Third-order intermodulation distortion	$f_{\text{IN1}} = 45\text{ MHz},$ $f_{\text{IN2}} = 50\text{ MHz}$		92			92		dBFS
	$f_{\text{IN1}} = 185\text{ MHz},$ $f_{\text{IN2}} = 190\text{ MHz}$		87			87		

7.10 AC Performance: ADC34J24

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC34J24 ($f_s = 125 \text{ MSPS}$)						UNIT	
		DITHER ON			DITHER OFF				
		MIN	TYP	MAX	MIN	TYP	MAX		
DYNAMIC AC CHARACTERISTICS									
SNR	Signal-to-noise ratio	$f_{\text{IN}} = 10 \text{ MHz}$	70.3			70.6			dBFS
		$f_{\text{IN}} = 70 \text{ MHz}$	68.8	70.1		70.4			
		$f_{\text{IN}} = 100 \text{ MHz}$	69.9			70.2			
		$f_{\text{IN}} = 170 \text{ MHz}$	69.1			69.7			
		$f_{\text{IN}} = 230 \text{ MHz}$	68.6			69.1			
NSD	Noise spectral density (averaged across Nyquist zone)	$f_{\text{IN}} = 10 \text{ MHz}$	148.3			148.6			dBFS/Hz
		$f_{\text{IN}} = 70 \text{ MHz}$	146.8	148.1		148.4			
		$f_{\text{IN}} = 100 \text{ MHz}$	147.9			148.2			
		$f_{\text{IN}} = 170 \text{ MHz}$	147.1			147.7			
		$f_{\text{IN}} = 230 \text{ MHz}$	146.6			147.1			
SINAD	Signal-to-noise and distortion ratio	$f_{\text{IN}} = 10 \text{ MHz}$	70.3			70.5			dBFS
		$f_{\text{IN}} = 70 \text{ MHz}$	67.6	70		70.3			
		$f_{\text{IN}} = 100 \text{ MHz}$	69.8			70.1			
		$f_{\text{IN}} = 170 \text{ MHz}$	68.9			69.3			
		$f_{\text{IN}} = 230 \text{ MHz}$	68.4			68.8			
ENOB	Effective number of bits	$f_{\text{IN}} = 10 \text{ MHz}$	11.4			11.4			Bits
		$f_{\text{IN}} = 70 \text{ MHz}$	10.9	11.4		11.4			
		$f_{\text{IN}} = 100 \text{ MHz}$	11.3			11.4			
		$f_{\text{IN}} = 170 \text{ MHz}$	11.2			11.3			
		$f_{\text{IN}} = 230 \text{ MHz}$	11.1			11.1			
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 10 \text{ MHz}$	94			92			dBc
		$f_{\text{IN}} = 70 \text{ MHz}$	81	93		91			
		$f_{\text{IN}} = 100 \text{ MHz}$	93			92			
		$f_{\text{IN}} = 170 \text{ MHz}$	85			83			
		$f_{\text{IN}} = 230 \text{ MHz}$	83			82			
HD2	Second harmonic distortion	$f_{\text{IN}} = 10 \text{ MHz}$	93			93			dBc
		$f_{\text{IN}} = 70 \text{ MHz}$	81	94		94			
		$f_{\text{IN}} = 100 \text{ MHz}$	92			92			
		$f_{\text{IN}} = 170 \text{ MHz}$	83			83			
		$f_{\text{IN}} = 230 \text{ MHz}$	82			82			
HD3	Third harmonic distortion	$f_{\text{IN}} = 10 \text{ MHz}$	96			93			dBc
		$f_{\text{IN}} = 70 \text{ MHz}$	83	94		91			
		$f_{\text{IN}} = 100 \text{ MHz}$	95			93			
		$f_{\text{IN}} = 170 \text{ MHz}$	88			86			
		$f_{\text{IN}} = 230 \text{ MHz}$	87			88			
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	$f_{\text{IN}} = 10 \text{ MHz}$	99			95			dBc
		$f_{\text{IN}} = 70 \text{ MHz}$	87	98		95			
		$f_{\text{IN}} = 100 \text{ MHz}$	97			95			
		$f_{\text{IN}} = 170 \text{ MHz}$	97			92			
		$f_{\text{IN}} = 230 \text{ MHz}$	95			92			

AC Performance: ADC34J24 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC34J24 ($f_S = 125\text{ MSPS}$)						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
THD Total harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		89			87		dBc
	$f_{\text{IN}} = 70\text{ MHz}$	76.5	89			87		
	$f_{\text{IN}} = 100\text{ MHz}$		89			87		
	$f_{\text{IN}} = 170\text{ MHz}$		82			80		
	$f_{\text{IN}} = 230\text{ MHz}$		81			80		
IMD3 Third-order intermodulation distortion	$f_{\text{IN1}} = 45\text{ MHz},$ $f_{\text{IN2}} = 50\text{ MHz}$		97			97		dBFS
	$f_{\text{IN1}} = 185\text{ MHz},$ $f_{\text{IN2}} = 190\text{ MHz}$		89			89		

7.11 AC Performance: ADC34J23

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $AV_{\text{DD}} = DV_{\text{DD}} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC34J23 ($f_s = 80\text{ MSPS}$)						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS								
SNR	Signal-to-noise ratio	$f_{\text{IN}} = 10\text{ MHz}$	70.2		70.4		dBFS	
		$f_{\text{IN}} = 70\text{ MHz}$	68.7	70	70.3			
		$f_{\text{IN}} = 100\text{ MHz}$	69.9		70.1			
		$f_{\text{IN}} = 170\text{ MHz}$	69.3		69.6			
		$f_{\text{IN}} = 230\text{ MHz}$	68.7		68.9			
NSD	Noise spectral density (averaged across Nyquist zone)	$f_{\text{IN}} = 10\text{ MHz}$	146.1		146.3		dBFS/Hz	
		$f_{\text{IN}} = 70\text{ MHz}$	144.8	145.9	146.2			
		$f_{\text{IN}} = 100\text{ MHz}$	145.8		146.0			
		$f_{\text{IN}} = 170\text{ MHz}$	145.2		145.5			
		$f_{\text{IN}} = 230\text{ MHz}$	144.6		144.8			
SINAD	Signal-to-noise and distortion ratio	$f_{\text{IN}} = 10\text{ MHz}$	70.2		70.3		dBFS	
		$f_{\text{IN}} = 70\text{ MHz}$	67.6	70	70.2			
		$f_{\text{IN}} = 100\text{ MHz}$	69.8		69.9			
		$f_{\text{IN}} = 170\text{ MHz}$	69.1		69.3			
		$f_{\text{IN}} = 230\text{ MHz}$	68.2		68.4			
ENOB	Effective number of bits	$f_{\text{IN}} = 10\text{ MHz}$	11.4		11.4		Bits	
		$f_{\text{IN}} = 70\text{ MHz}$	10.9	11.4	11.4			
		$f_{\text{IN}} = 100\text{ MHz}$	11.3		11.3			
		$f_{\text{IN}} = 170\text{ MHz}$	11.2		11.3			
		$f_{\text{IN}} = 230\text{ MHz}$	11.1		11.1			
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 10\text{ MHz}$	95		91		dBc	
		$f_{\text{IN}} = 70\text{ MHz}$	82	95	90			
		$f_{\text{IN}} = 100\text{ MHz}$	90		89			
		$f_{\text{IN}} = 170\text{ MHz}$	87		84			
		$f_{\text{IN}} = 230\text{ MHz}$	80		80			
HD2	Second harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$	95		95		dBc	
		$f_{\text{IN}} = 70\text{ MHz}$	82	95	94			
		$f_{\text{IN}} = 100\text{ MHz}$	91		92			
		$f_{\text{IN}} = 170\text{ MHz}$	83		83			
		$f_{\text{IN}} = 230\text{ MHz}$	81		82			
HD3	Third harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$	99		94		dBc	
		$f_{\text{IN}} = 70\text{ MHz}$	83	101	94			
		$f_{\text{IN}} = 100\text{ MHz}$	91		90			
		$f_{\text{IN}} = 170\text{ MHz}$	92		90			
		$f_{\text{IN}} = 230\text{ MHz}$	80		80			
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	$f_{\text{IN}} = 10\text{ MHz}$	98		92		dBc	
		$f_{\text{IN}} = 70\text{ MHz}$	87	98	92			
		$f_{\text{IN}} = 100\text{ MHz}$	97		91			
		$f_{\text{IN}} = 170\text{ MHz}$	96		91			
		$f_{\text{IN}} = 230\text{ MHz}$	93		91			

AC Performance: ADC34J23 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC34J23 ($f_s = 80\text{ MSPS}$)						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
THD Total harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$		91			86		dBc
	$f_{\text{IN}} = 70\text{ MHz}$	76.5	91			86		
	$f_{\text{IN}} = 100\text{ MHz}$		87			84		
	$f_{\text{IN}} = 170\text{ MHz}$		82			81		
	$f_{\text{IN}} = 230\text{ MHz}$		77			77		
IMD3 Third-order intermodulation distortion	$f_{\text{IN1}} = 45\text{ MHz},$ $f_{\text{IN2}} = 50\text{ MHz}$		95			95		dBFS
	$f_{\text{IN1}} = 185\text{ MHz},$ $f_{\text{IN2}} = 190\text{ MHz}$		88			88		

7.12 AC Performance: ADC34J22

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $AV_{\text{DD}} = DV_{\text{DD}} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC34J22 ($f_s = 50\text{ MSPS}$)						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS								
SNR	Signal-to-noise ratio	$f_{\text{IN}} = 10\text{ MHz}$	69.3	70.2		70.5		dBFS
		$f_{\text{IN}} = 70\text{ MHz}$		70		70.3		
		$f_{\text{IN}} = 100\text{ MHz}$		69.9		70.2		
		$f_{\text{IN}} = 170\text{ MHz}$		69.3		69.5		
		$f_{\text{IN}} = 230\text{ MHz}$		67.9		68		
NSD	Noise spectral density (averaged across Nyquist zone)	$f_{\text{IN}} = 10\text{ MHz}$	143.3	144.2		144.5		dBFS/Hz
		$f_{\text{IN}} = 70\text{ MHz}$		144		144.3		
		$f_{\text{IN}} = 100\text{ MHz}$		143.9		144.2		
		$f_{\text{IN}} = 170\text{ MHz}$		143.3		143.5		
		$f_{\text{IN}} = 230\text{ MHz}$		141.9		142		
SINAD	Signal-to-noise and distortion ratio	$f_{\text{IN}} = 10\text{ MHz}$	67.6	70.2		70.4		dBFS
		$f_{\text{IN}} = 70\text{ MHz}$		69.9		70.1		
		$f_{\text{IN}} = 100\text{ MHz}$		69.8		70		
		$f_{\text{IN}} = 170\text{ MHz}$		69.1		69.3		
		$f_{\text{IN}} = 230\text{ MHz}$		67.5		67.6		
ENOB	Effective number of bits	$f_{\text{IN}} = 10\text{ MHz}$	10.9	11.4		11.4		Bits
		$f_{\text{IN}} = 70\text{ MHz}$		11.3		11.3		
		$f_{\text{IN}} = 100\text{ MHz}$		11.3		11.3		
		$f_{\text{IN}} = 170\text{ MHz}$		11.2		11.2		
		$f_{\text{IN}} = 230\text{ MHz}$		10.9		10.9		
SFDR	Spurious-free dynamic range	$f_{\text{IN}} = 10\text{ MHz}$	84.5	95		91		dBc
		$f_{\text{IN}} = 70\text{ MHz}$		93		90		
		$f_{\text{IN}} = 100\text{ MHz}$		90		89		
		$f_{\text{IN}} = 170\text{ MHz}$		85		84		
		$f_{\text{IN}} = 230\text{ MHz}$		80		80		
HD2	Second harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$	84.5	94		93		dBc
		$f_{\text{IN}} = 70\text{ MHz}$		93		93		
		$f_{\text{IN}} = 100\text{ MHz}$		90		90		
		$f_{\text{IN}} = 170\text{ MHz}$		83		83		
		$f_{\text{IN}} = 230\text{ MHz}$		81		81		
HD3	Third harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$	84.5	102		96		dBc
		$f_{\text{IN}} = 70\text{ MHz}$		94		92		
		$f_{\text{IN}} = 100\text{ MHz}$		90		89		
		$f_{\text{IN}} = 170\text{ MHz}$		91		90		
		$f_{\text{IN}} = 230\text{ MHz}$		80		80		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	$f_{\text{IN}} = 10\text{ MHz}$	87	98		92		dBc
		$f_{\text{IN}} = 70\text{ MHz}$		97		92		
		$f_{\text{IN}} = 100\text{ MHz}$		96		92		
		$f_{\text{IN}} = 170\text{ MHz}$		95		91		
		$f_{\text{IN}} = 230\text{ MHz}$		93		91		

AC Performance: ADC34J22 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADC34J22 ($f_s = 50\text{ MSPS}$)						UNIT
		DITHER ON			DITHER OFF			
		MIN	TYP	MAX	MIN	TYP	MAX	
THD Total harmonic distortion	$f_{\text{IN}} = 10\text{ MHz}$	76.5	91		86			dBc
	$f_{\text{IN}} = 70\text{ MHz}$		89		85			
	$f_{\text{IN}} = 100\text{ MHz}$		86		84			
	$f_{\text{IN}} = 170\text{ MHz}$		82		81			
	$f_{\text{IN}} = 230\text{ MHz}$		77		77			
IMD3 Third-order intermodulation distortion	$f_{\text{IN1}} = 45\text{ MHz}$, $f_{\text{IN2}} = 50\text{ MHz}$		93		93			dBFS
	$f_{\text{IN1}} = 185\text{ MHz}$, $f_{\text{IN2}} = 190\text{ MHz}$		86		86			

7.13 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$ and -1-dBFS differential input, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
DIGITAL INPUTS (RESET, SCLK, SEN, SDATA, PDN)⁽¹⁾							
V_{IH}	High-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels			1.2	V	
V_{IL}	Low-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels			0.4	V	
I_{IH}	High-level input current	SEN			0	μA	
		RESET, SCLK, SDATA, PDN			10	μA	
I_{IL}	Low-level input current	SEN			10	μA	
		RESET, SCLK, SDATA, PDN			0	μA	
DIGITAL INPUTS (SYNCP~, SYNCM~, SYSREFP, SYSREFM)							
V_{IH}	High-level input voltage				1.3	V	
V_{IL}	Low-level input voltage				0.5	V	
$V_{\text{CM_DIG}}$	Common-mode voltage for SYNCP~ and SYSREF				0.9	V	
DIGITAL OUTPUTS (SDOUT, OVRA, OVRB, OVRC, OVRD)							
V_{OH}	High-level output voltage				$\text{DVDD} - 0.1$	DVDD	V
V_{OL}	Low-level output voltage					0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)⁽²⁾							
V_{OH}	High-level output voltage				DVDD	V	
V_{OL}	Low-level output voltage				$\text{DVDD} - 0.4$	V	
V_{OD}	Output differential voltage				0.4	V	
V_{OC}	Output common-mode voltage				$\text{DVDD} - 0.2$	V	
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between -0.25 V and 1.45 V			-100	100	mA
Z_{os}	Single-ended output impedance				50	Ω	
	Output capacitance	Output capacitance inside the device, from either output to ground			2	pF	

(1) RESET, SCLK, SDATA, and PDN pins have 150-k Ω (typical) internal pull-down resistor to ground, while SEN pin has 150-k Ω (typical) pull-up resistor to AVDD.

(2) 50- Ω , single-ended external termination to 1.8 V.

7.14 Timing Characteristics

Typical values are at 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C. See [Figure 143](#).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLE TIMING CHARACTERISTICS					
Aperture delay		0.85	1.25	1.65	ns
Aperture delay matching	Between two channels on the same device		±70		ps
	Between two devices at the same temperature and supply voltage		±150		ps
Aperture jitter			200		f _S rms
Wake-up time	Time to valid data after coming out of STANDBY mode		35	100	μs
	Time to valid data after coming out of global power-down		85	300	μs
t _{SU_SYNC~}	Setup time for SYNC~	Referenced to input clock rising edge	1		ns
t _{H_SYNC~}	Hold time for SYNC~	Referenced to input clock rising edge	100		ps
t _{SU_SYSREF}	Setup time for SYSREF	Referenced to input clock rising edge	1		ns
t _{H_SYSREF}	Hold time for SYSREF	Referenced to input clock rising edge	100		ps
CML OUTPUT TIMING CHARACTERISTICS					
Unit interval		312.5		1667	ps
Serial output data rate				3.2	Gbps
Total jitter	3.125 Gbps (20x mode, f _S = 156.25 MSPS)		0.3		p-pUI
t _R , t _F	Data rise time, data fall time	Rise and fall times measured from 20% to 80%, differential output waveform, 600 Mbps ≤ bit rate ≤ 3.125 Gbps	105		ps

Table 2. Latency in Different Modes⁽¹⁾⁽²⁾

MODE	PARAMETER	LATENCY (N Cycles)	TYPICAL DATA DELAY (t _D , ns)
20x	ADC latency	17	0.29 × t _S + 3
	Normal OVR latency	9	0.5 × t _S + 2
	Fast OVR latency	7	0.5 × t _S + 2
	From SYNC~ falling edge to CGS phase ⁽³⁾	15	0.3 × t _S + 4
	From SYNC~ rising edge to ILA sequence ⁽⁴⁾	17	0.3 × t _S + 4
40x	ADC latency	16	0.85 × t _S + 3.9
	Normal OVR latency	9	0.5 × t _S + 2
	Fast OVR latency	7	0.5 × t _S + 2
	From SYNC~ falling edge to CGS phase ⁽³⁾	14	0.9 × t _S + 4
	From SYNC~ rising edge to ILA sequence ⁽⁴⁾	12	0.9 × t _S + 4

(1) Overall latency = latency + t_D.

(2) t_S is the time period of the ADC conversion clock.

(3) Latency is specified for subclass 2. In subclass 0, the SYNC~ falling edge to CGS phase latency is 16 clock cycles in 10x mode and 15 clock cycles in 20x mode.

(4) Latency is specified for subclass 2. In subclass 0, the SYNC~ rising edge to ILA sequence latency is 11 clock cycles in 10x mode and 11 clock cycles in 20x mode.

7.15 Typical Characteristics: ADC34J25

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.

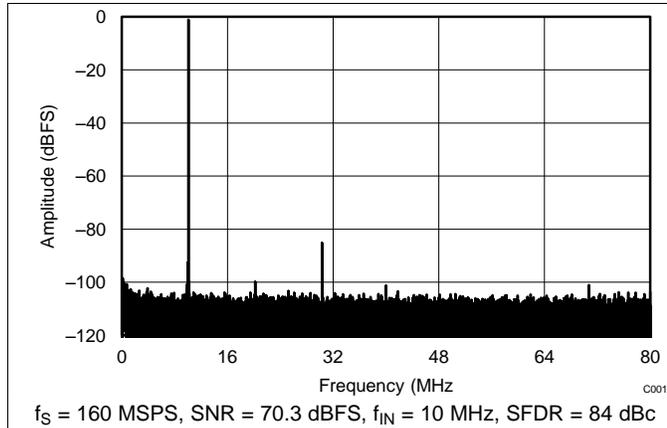


Figure 1. FFT for 10-MHz Input Signal (Dither On)

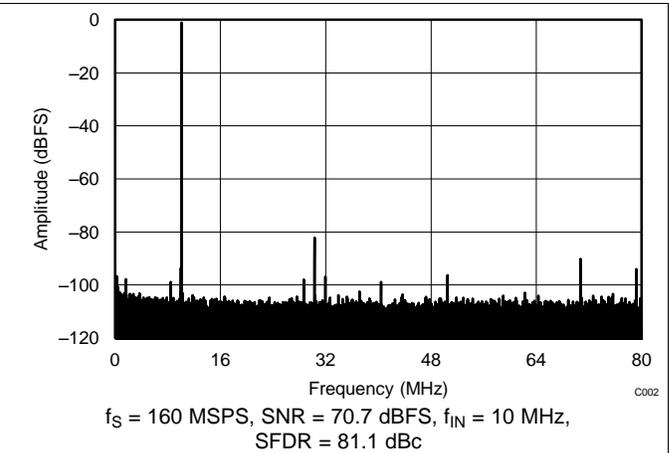


Figure 2. FFT for 10-MHz Input Signal (Dither Off)

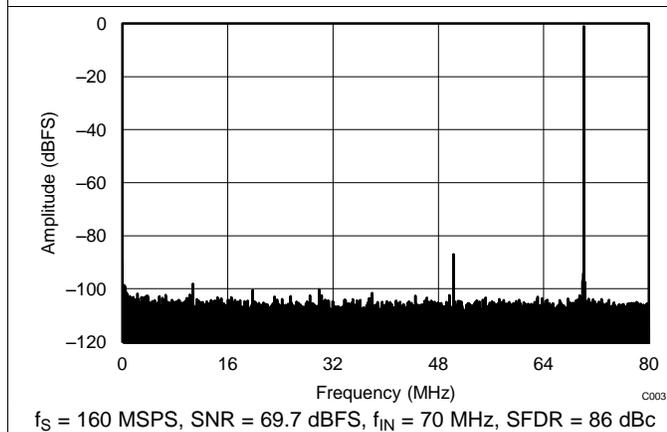


Figure 3. FFT for 70-MHz Input Signal (Dither On)

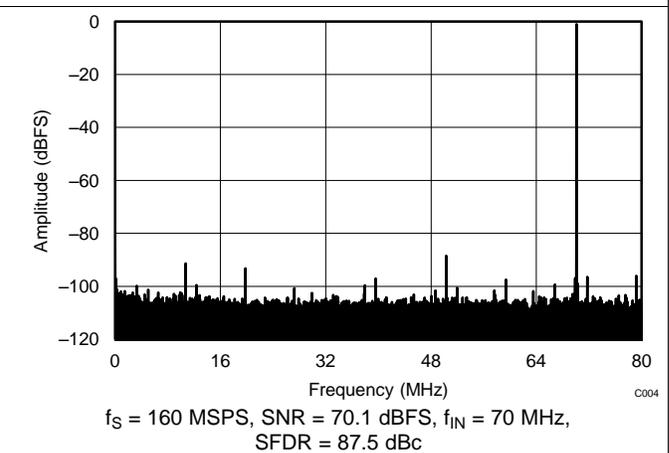


Figure 4. FFT for 70-MHz Input Signal (Dither Off)

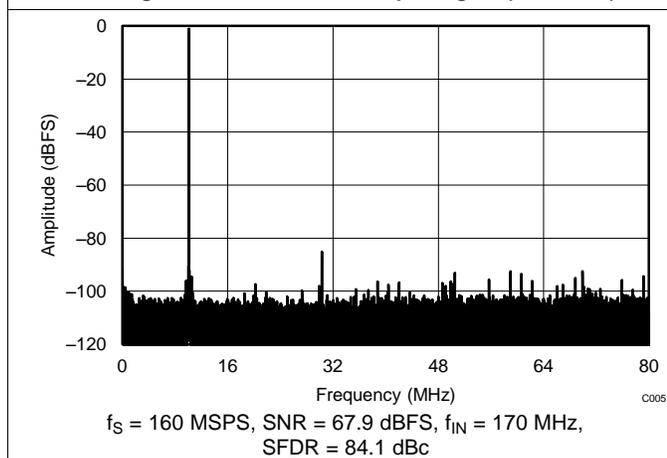


Figure 5. FFT for 170-MHz Input Signal (Dither On)

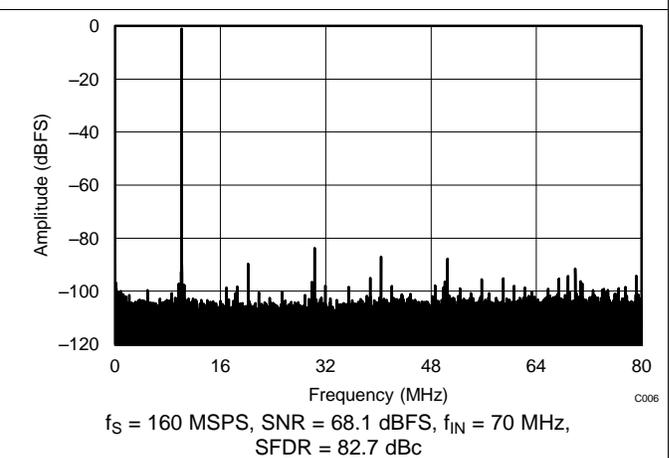
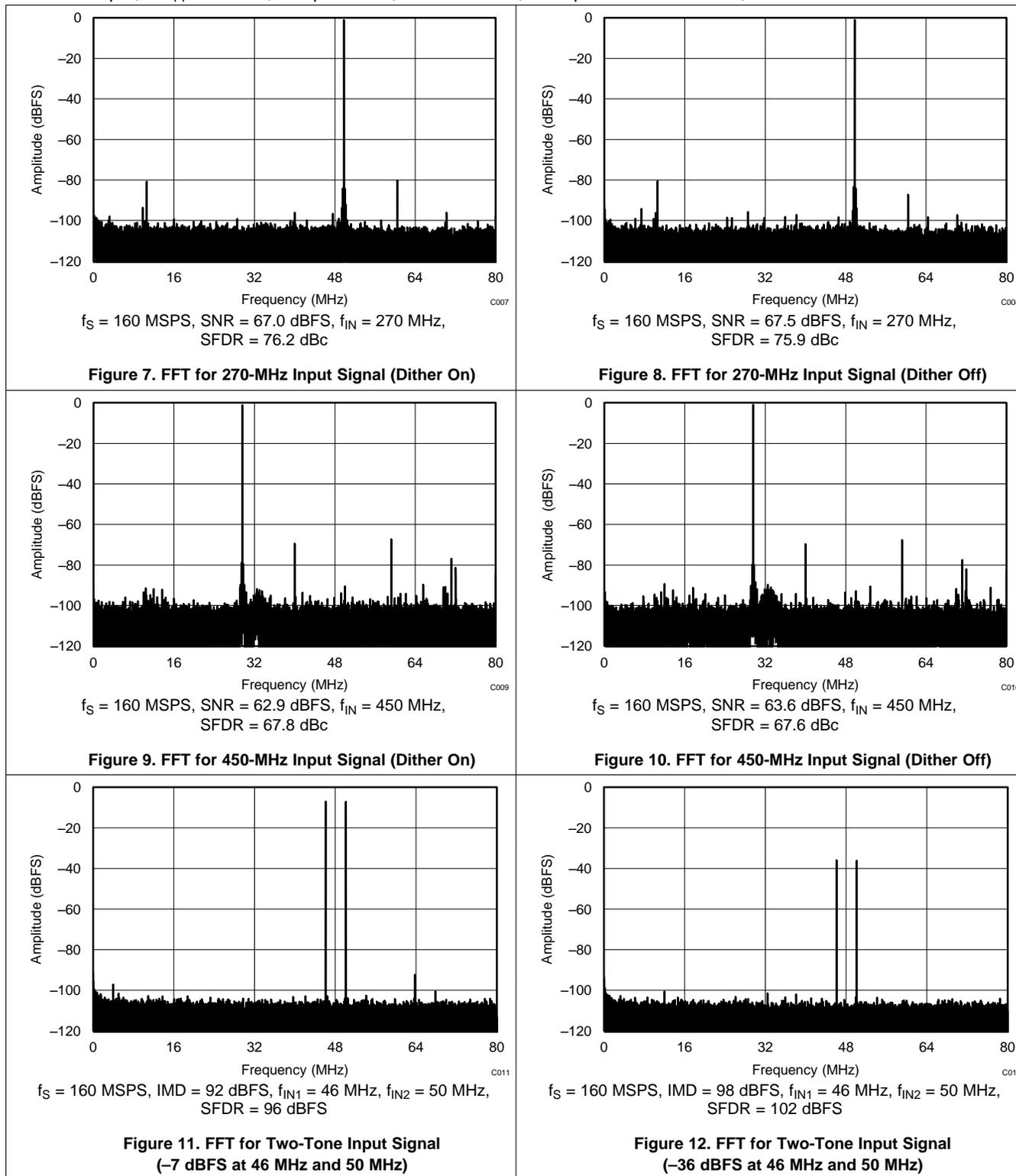


Figure 6. FFT for 170-MHz Input Signal (Dither Off)

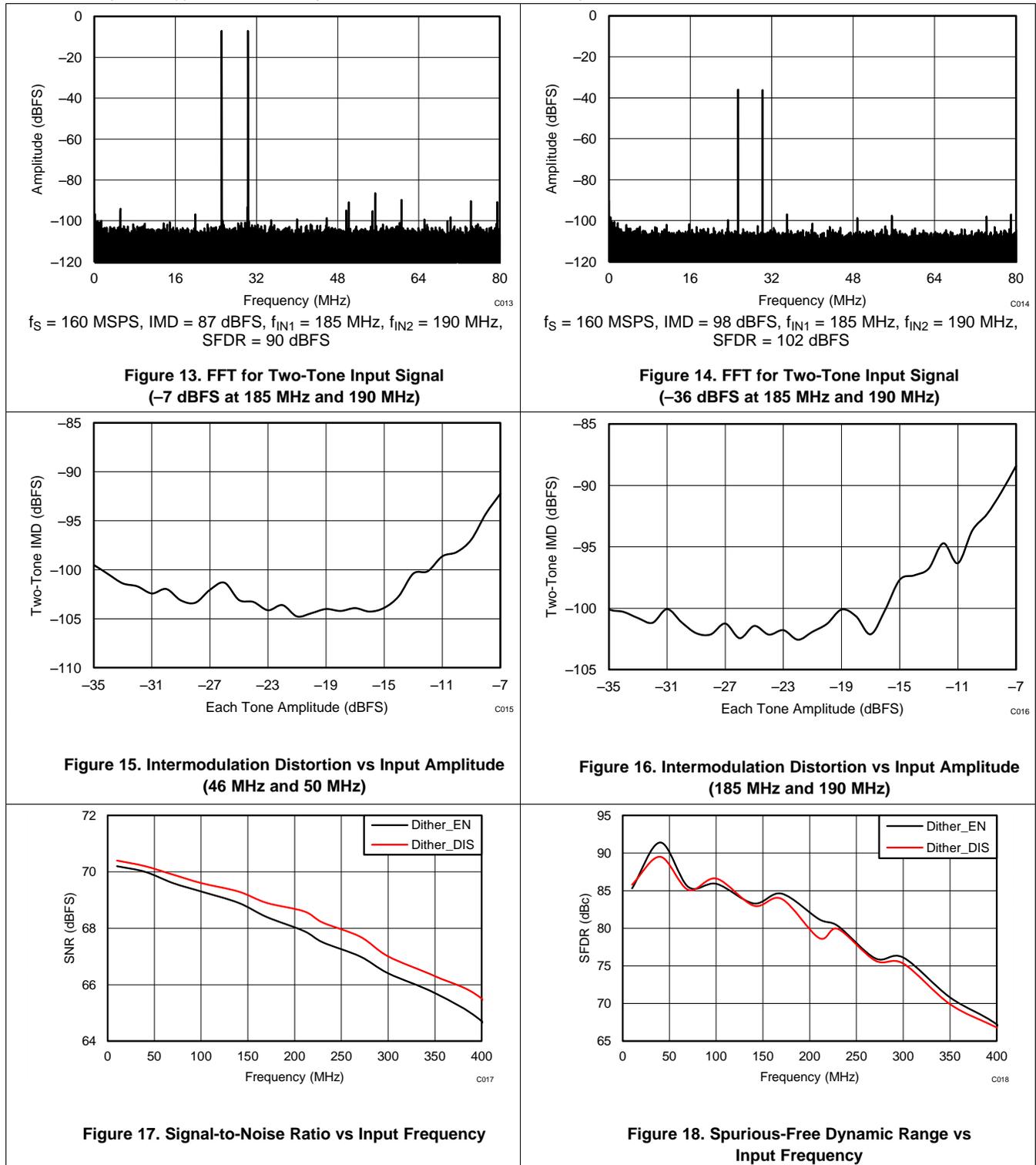
Typical Characteristics: ADC34J25 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.



Typical Characteristics: ADC34J25 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.



Typical Characteristics: ADC34J25 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.

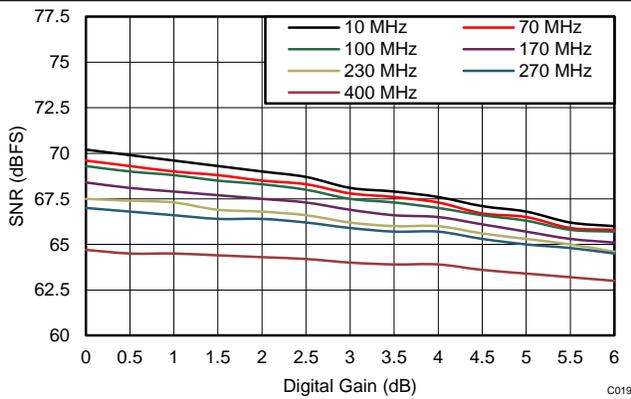


Figure 19. Signal-to-Noise Ratio vs Digital Gain and Input Frequency

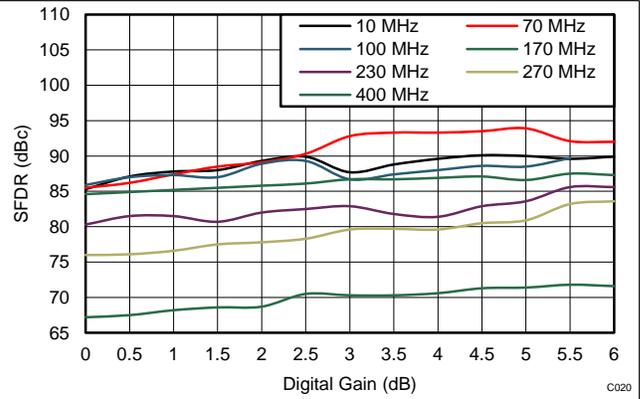


Figure 20. Spurious-Free Dynamic Range vs Digital Gain and Input Frequency

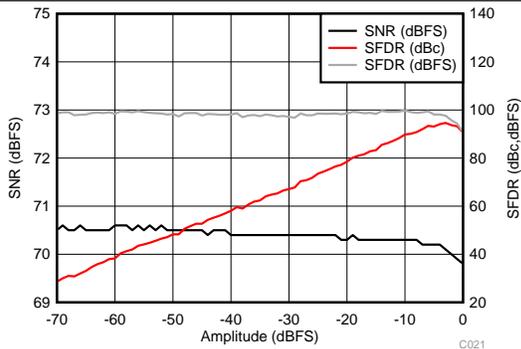


Figure 21. Performance vs Input Amplitude (30 MHz)

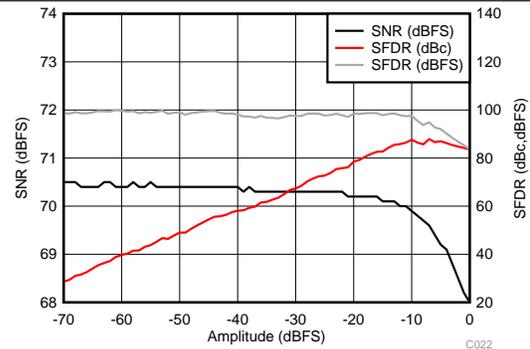


Figure 22. Performance vs Input Amplitude (170 MHz)

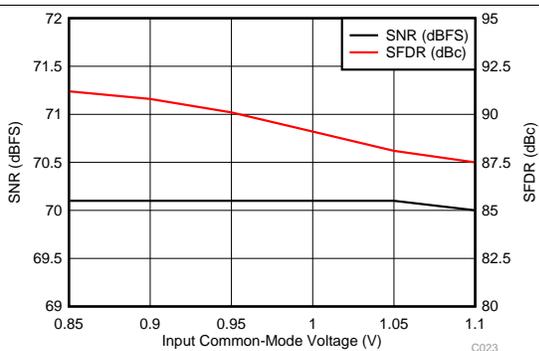


Figure 23. Performance vs Input Common-Mode Voltage (30 MHz)

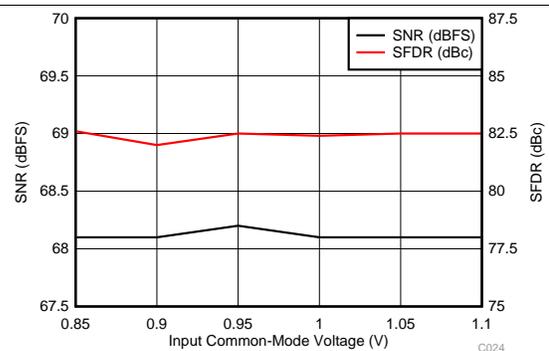


Figure 24. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADC34J25 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.

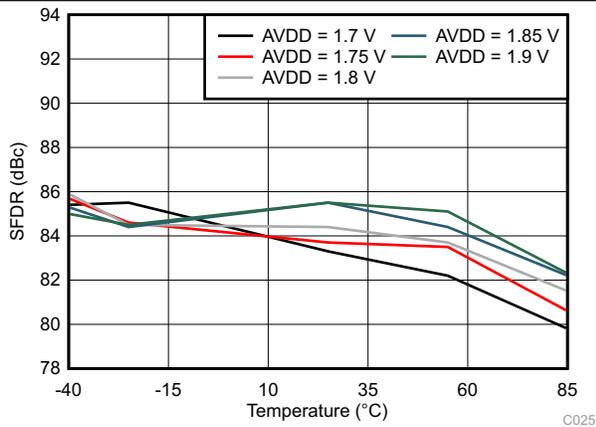


Figure 25. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

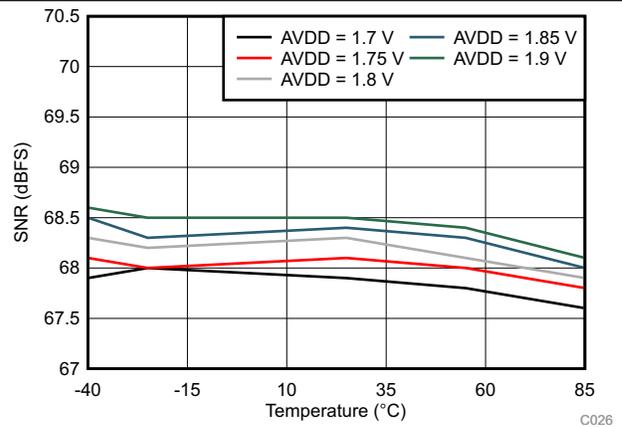


Figure 26. Signal-to-Noise Ratio vs AVDD Supply and Temperature

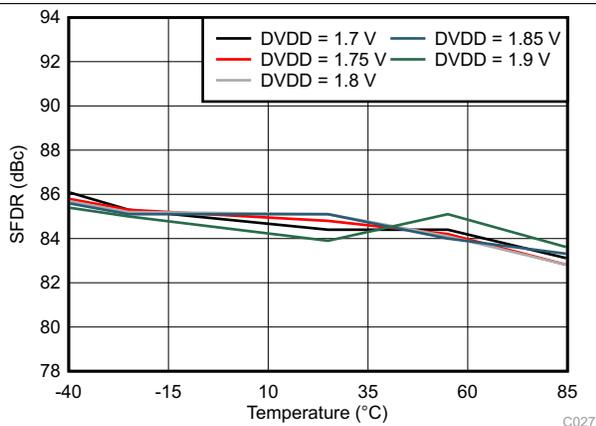


Figure 27. Spurious-Free Dynamic Range vs DVDD Supply and Temperature

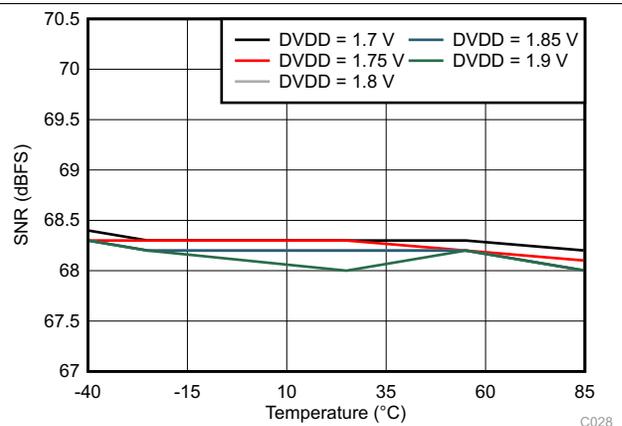


Figure 28. Signal-to-Noise Ratio vs DVDD Supply and Temperature

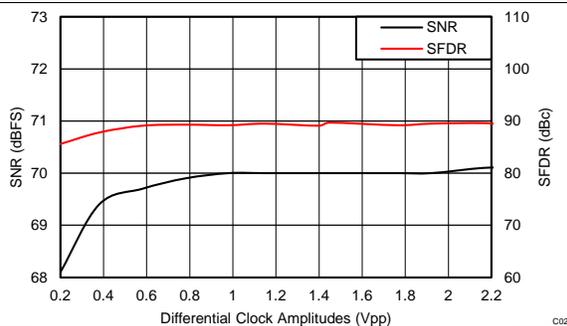


Figure 29. Performance vs Clock Amplitude (40 MHz)

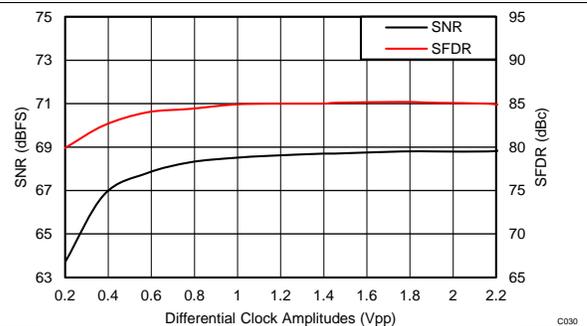


Figure 30. Performance vs Clock Amplitude (150 MHz)

Typical Characteristics: ADC34J25 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, dither enabled, and special modes written, unless otherwise noted.

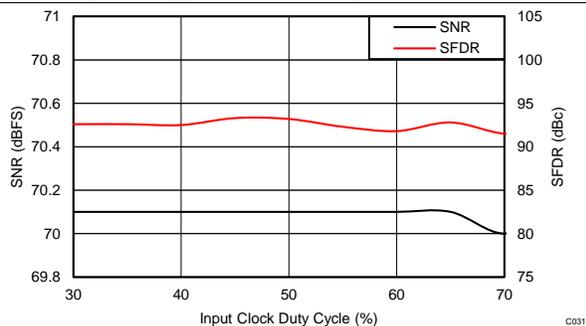


Figure 31. Performance vs Clock Duty Cycle (40 MHz)

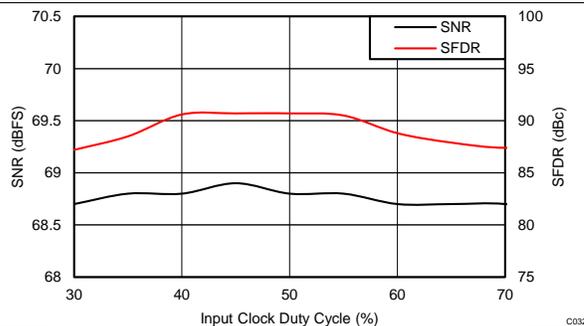


Figure 32. Performance vs Clock Duty Cycle (150 MHz)

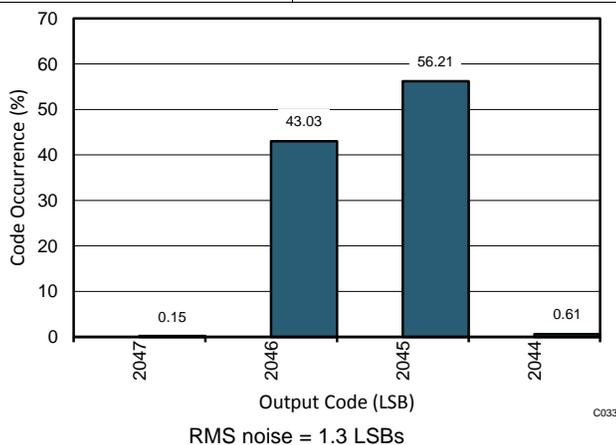
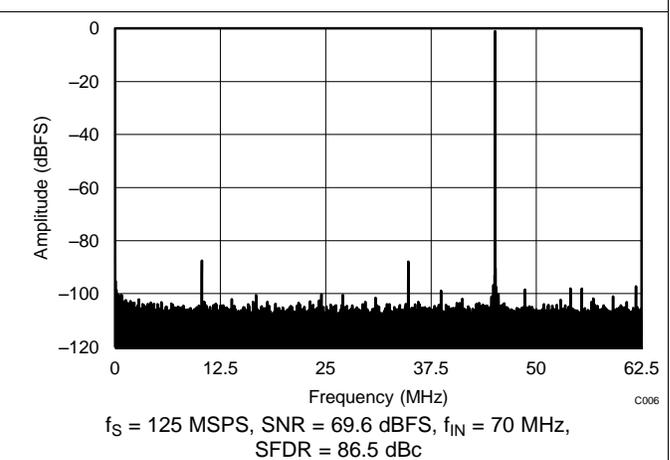
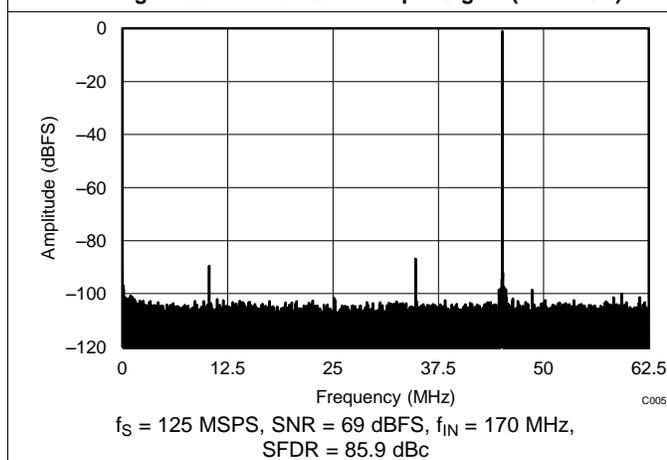
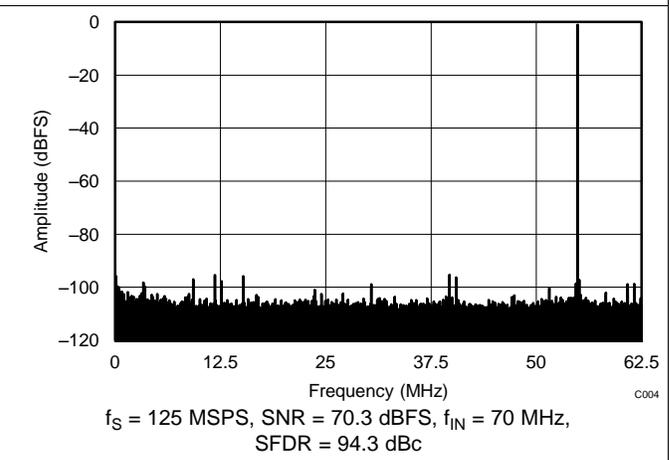
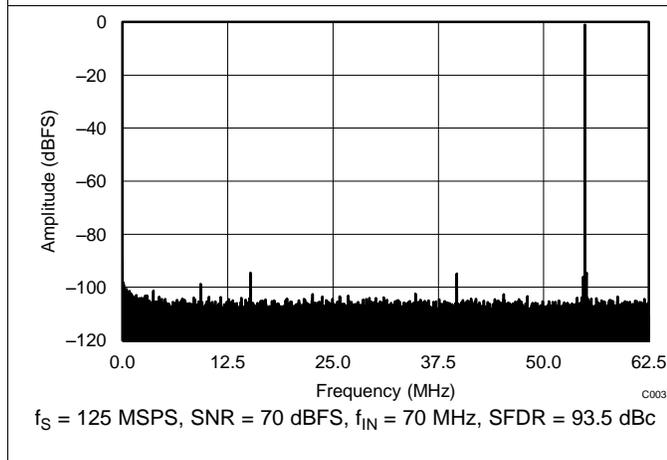
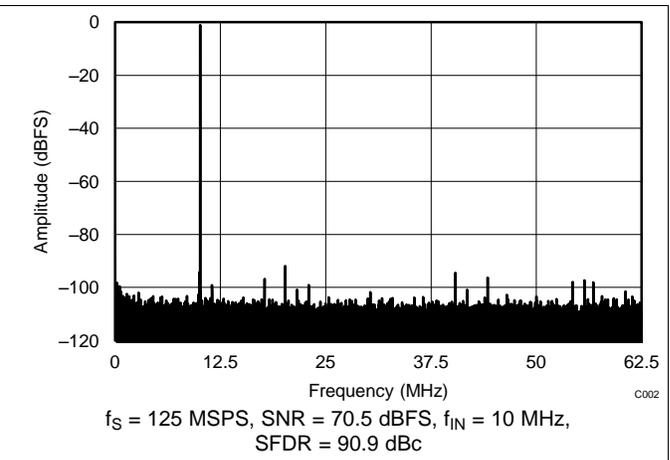
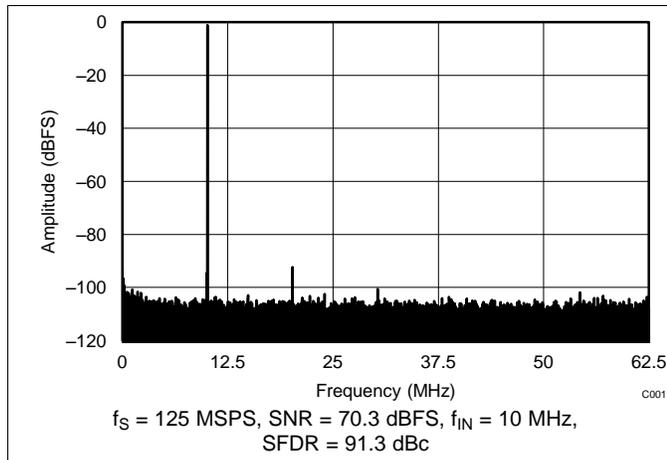


Figure 33. Idle Channel Histogram

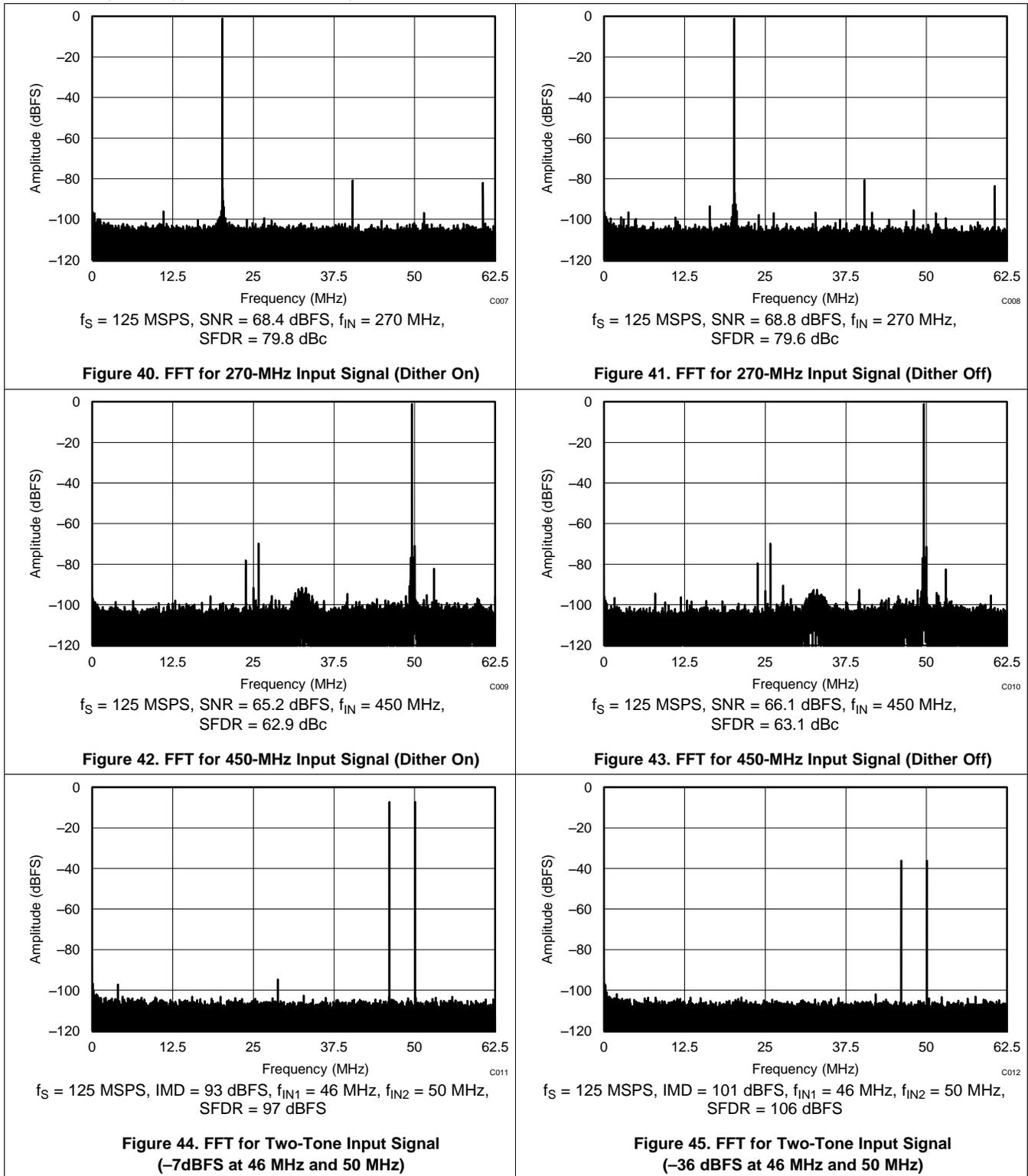
7.16 Typical Characteristics: ADC34J24

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



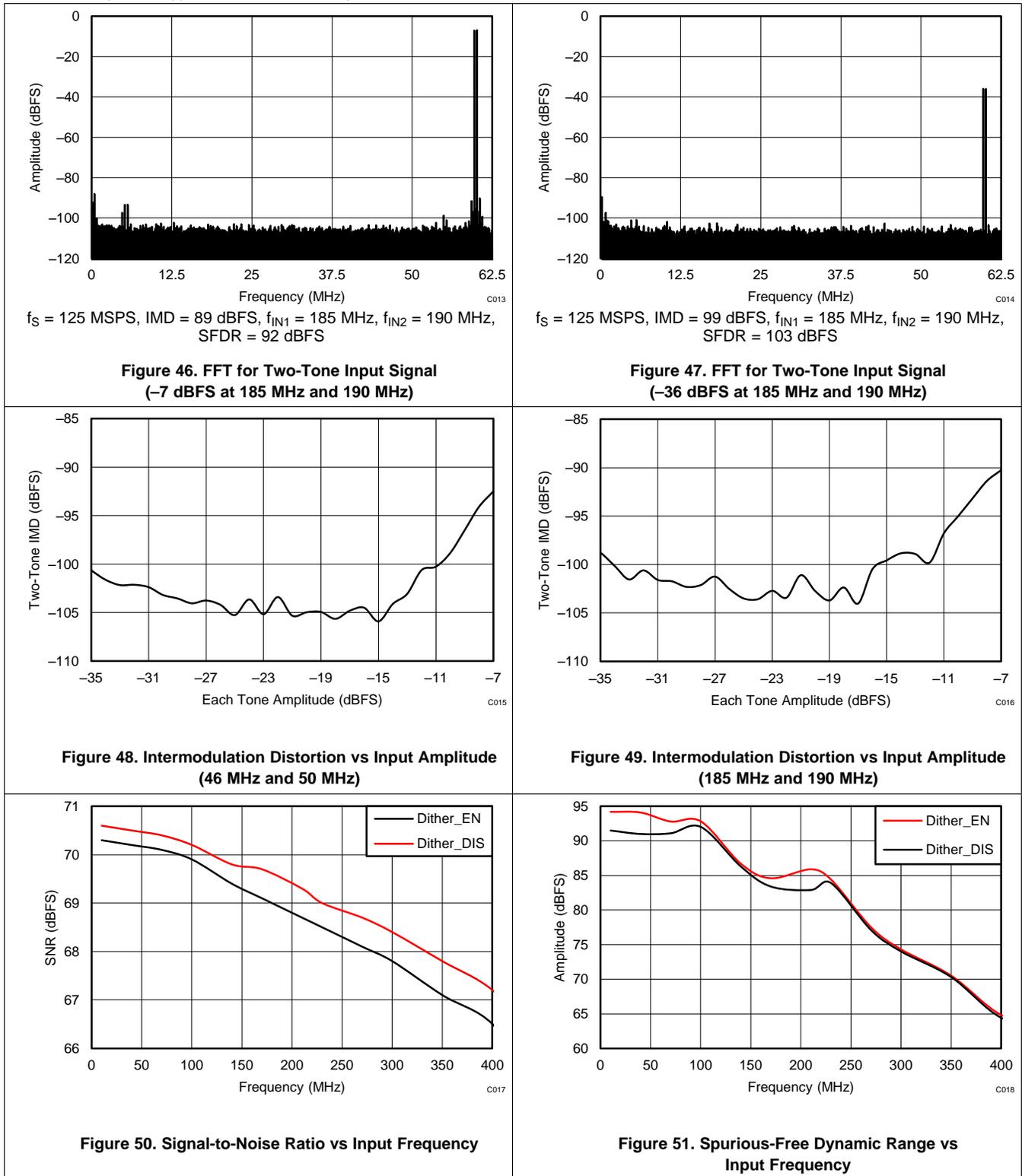
Typical Characteristics: ADC34J24 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J24 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J24 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.

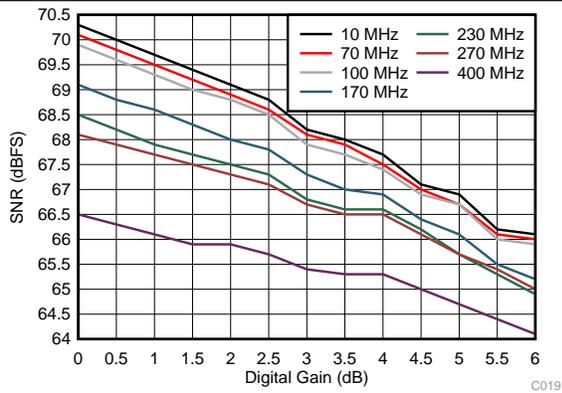


Figure 52. Signal-to-Noise Ratio vs Digital Gain and Input Frequency

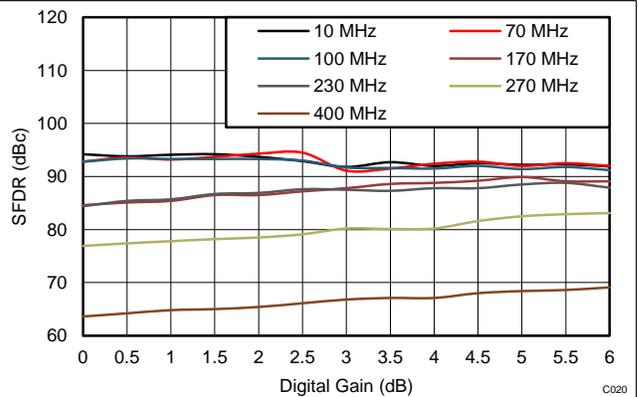


Figure 53. Spurious-Free Dynamic Range vs Digital Gain and Input Frequency

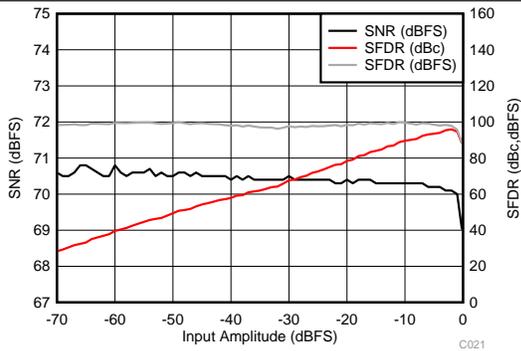


Figure 54. Performance vs Input Amplitude (30 MHz)

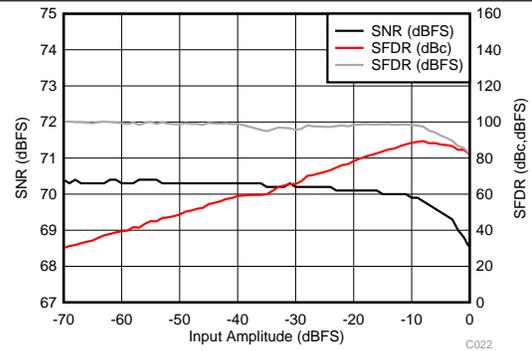


Figure 55. Performance vs Input Amplitude (170 MHz)

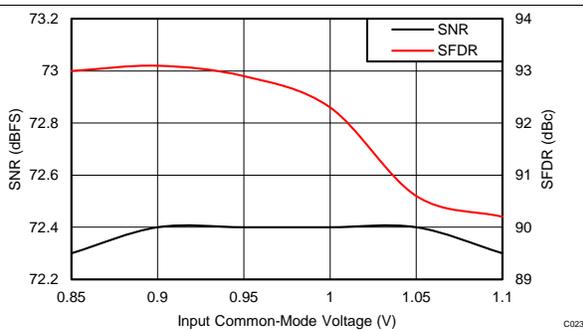


Figure 56. Performance vs Input Common-Mode Voltage (30 MHz)

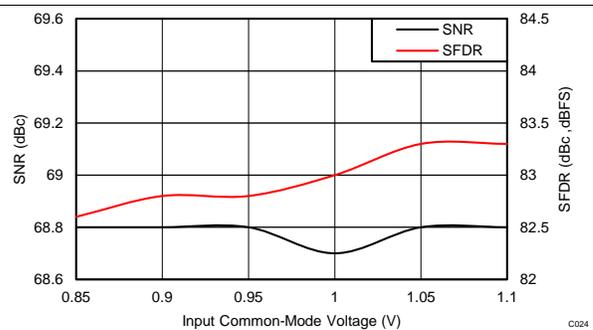
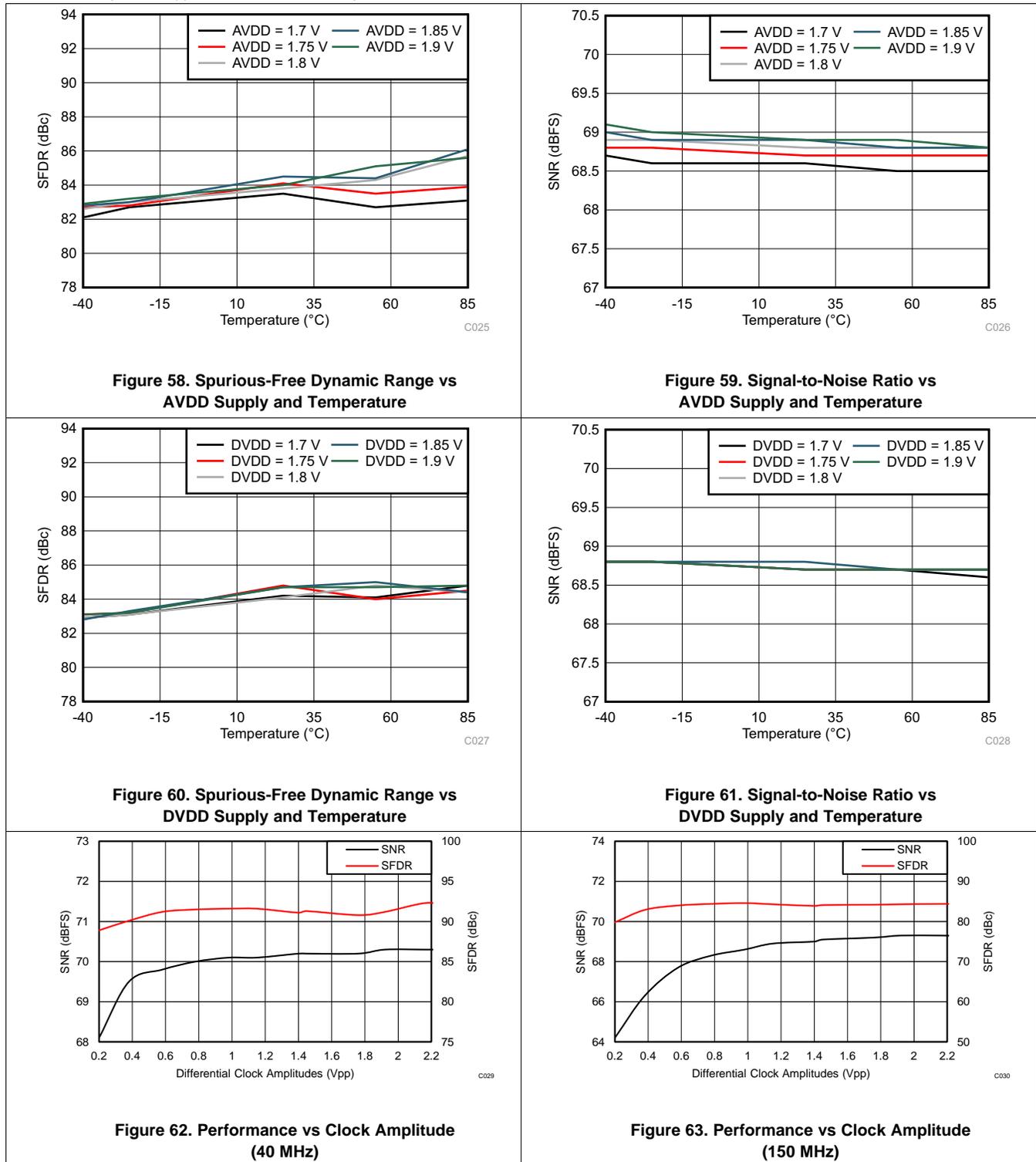


Figure 57. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADC34J24 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, -1-dBFS differential input, 2-V_{pp} full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J24 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.

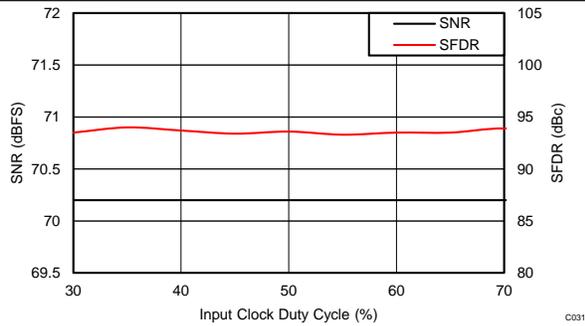


Figure 64. Performance vs Clock Duty Cycle (40 MHz)

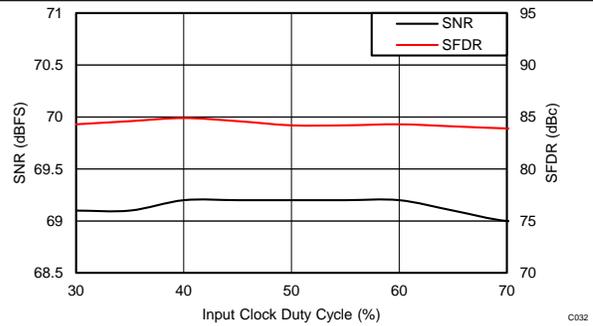


Figure 65. Performance vs Clock Duty Cycle (150 MHz)

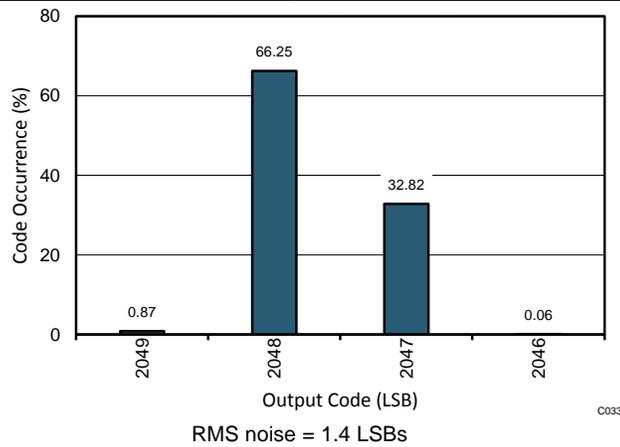
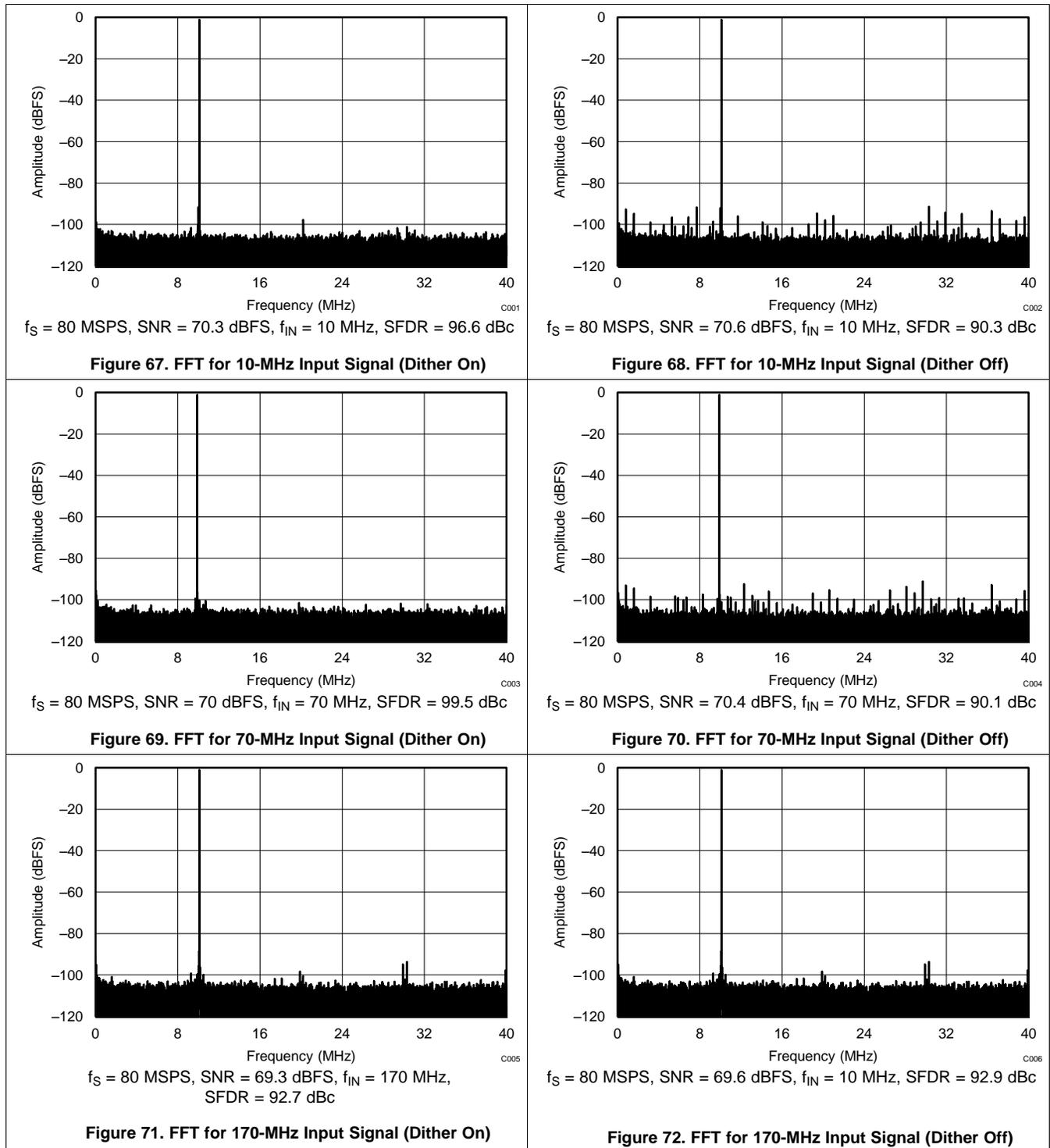


Figure 66. Idle Channel Histogram

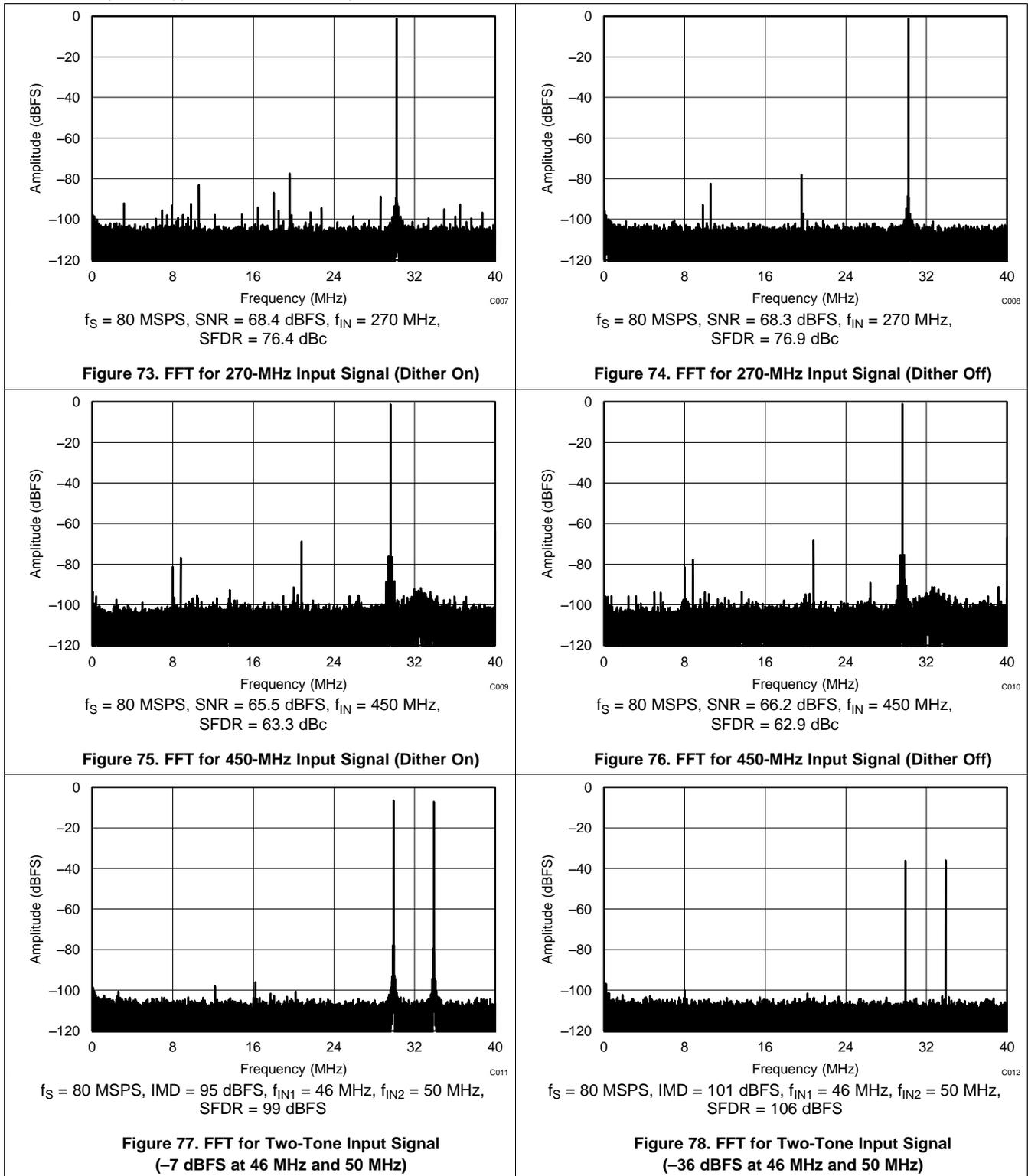
7.17 Typical Characteristics: ADC34J23

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



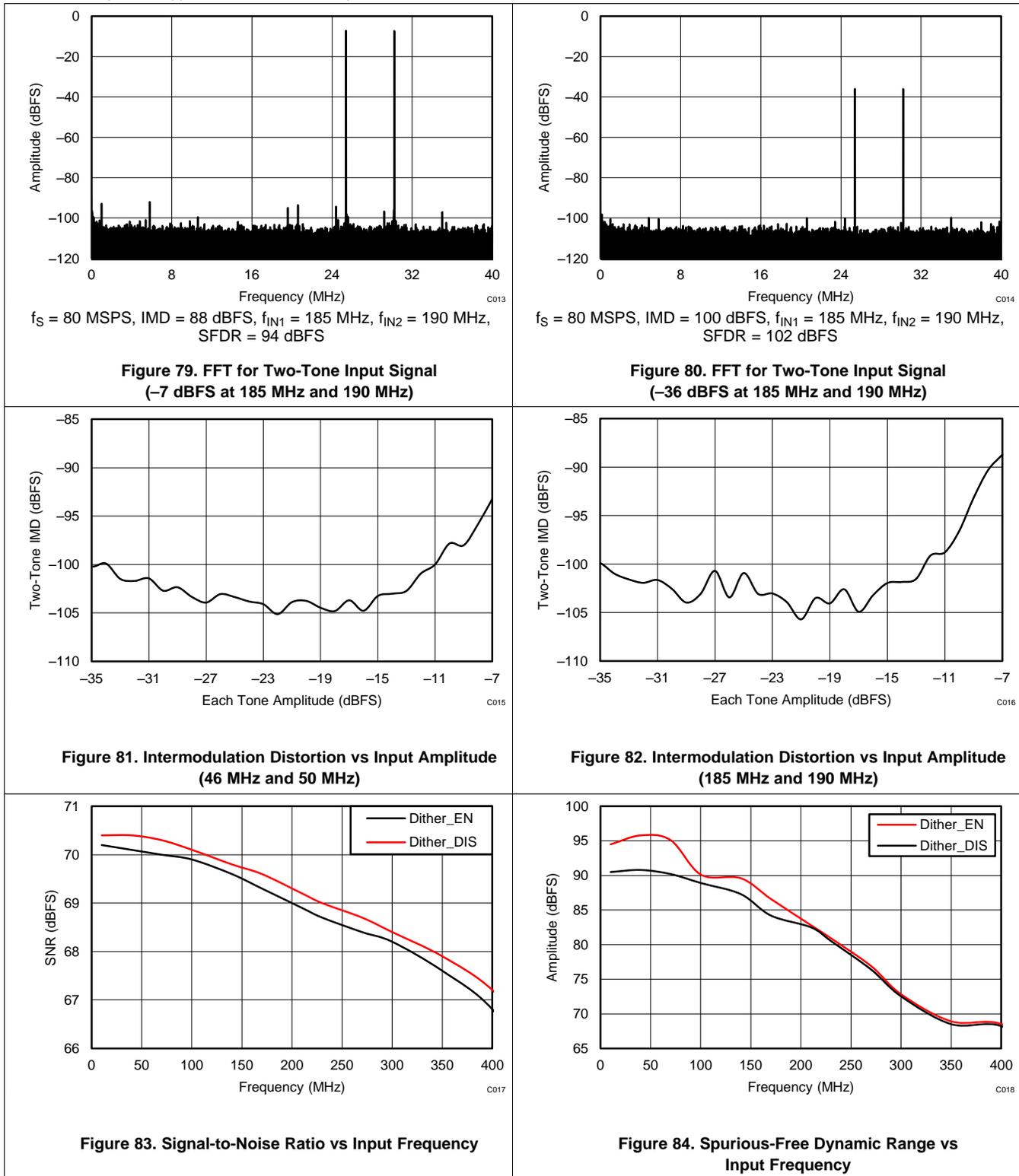
Typical Characteristics: ADC34J23 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J23 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J23 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.

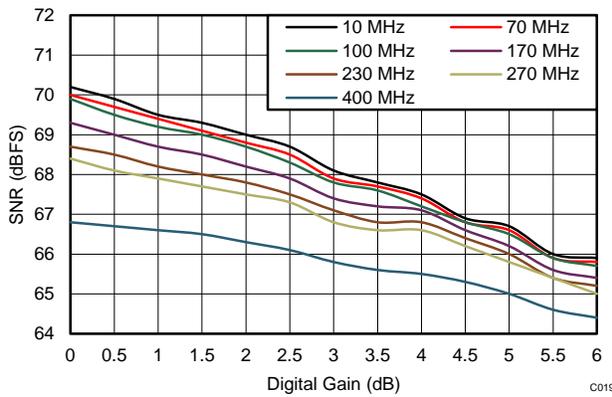


Figure 85. Signal-to-Noise Ratio vs Digital Gain and Input Frequency

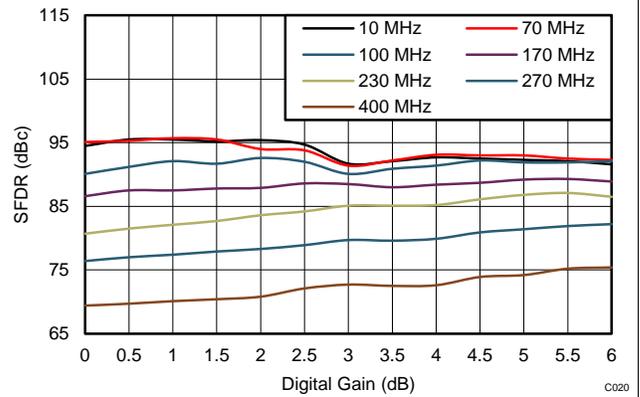


Figure 86. Spurious-Free Dynamic Range vs Digital Gain and Input Frequency

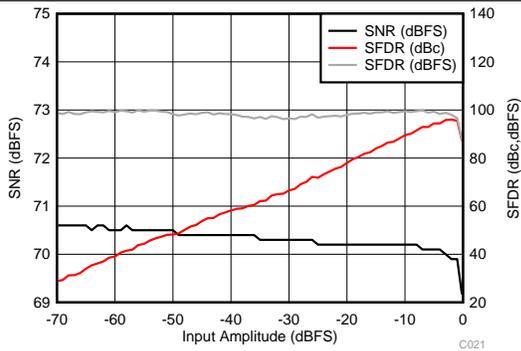


Figure 87. Performance vs Input Amplitude (30 MHz)

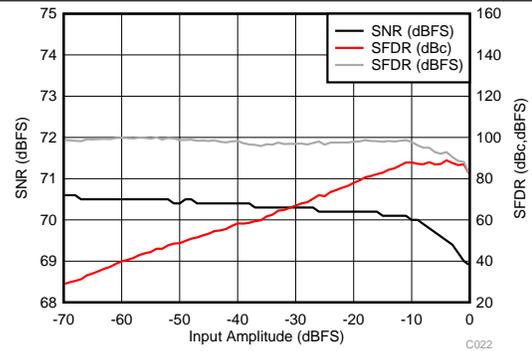


Figure 88. Performance vs Input Amplitude (170 MHz)

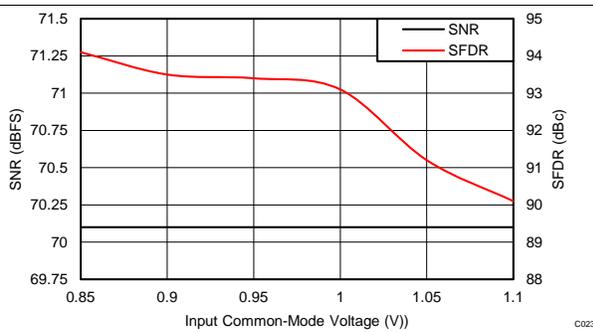


Figure 89. Performance vs Input Common-Mode Voltage (30 MHz)

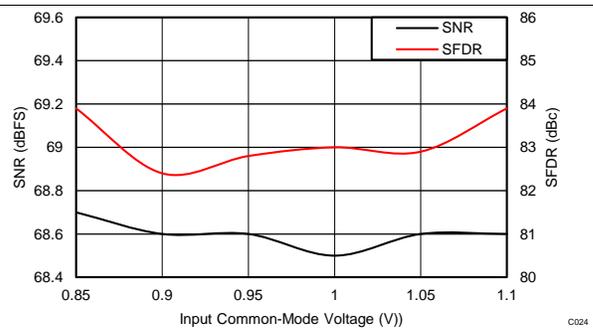
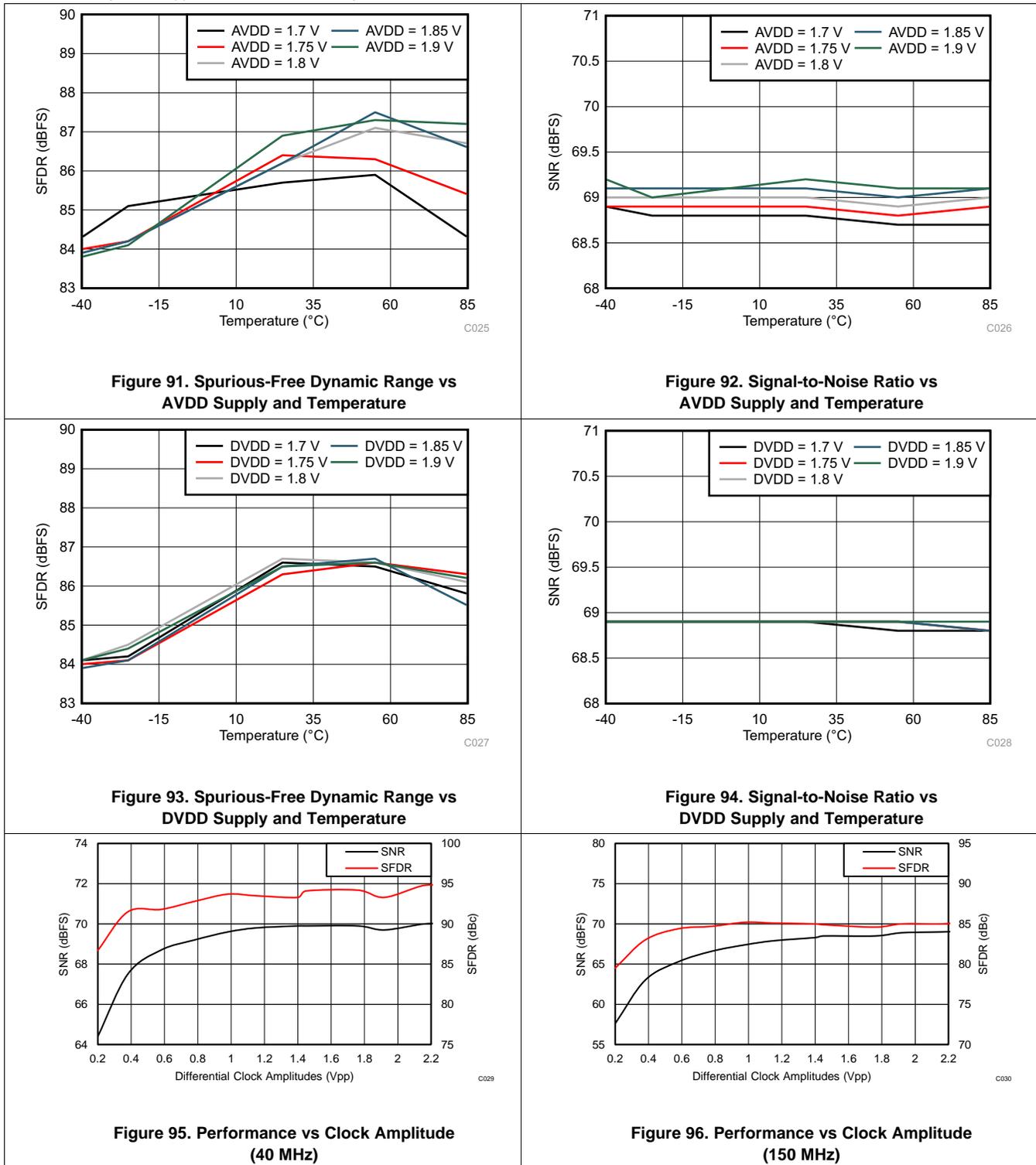


Figure 90. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADC34J23 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, -1-dBFS differential input, 2-V_{pp} full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J23 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.

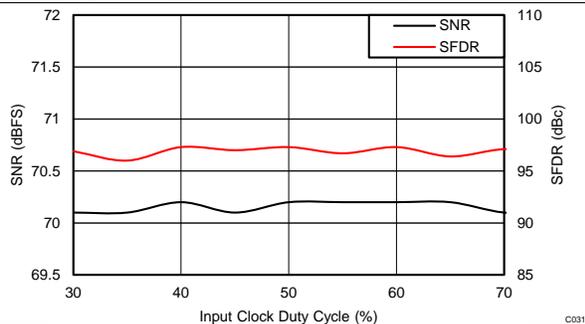


Figure 97. Performance vs Clock Duty Cycle (40 MHz)

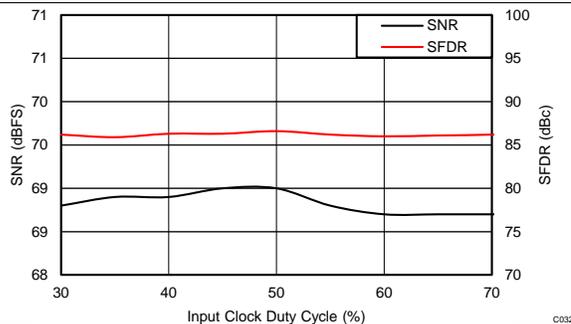


Figure 98. Performance vs Clock Duty Cycle (150 MHz)

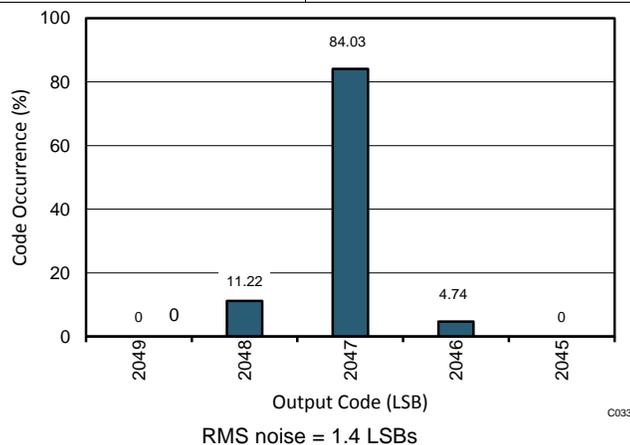
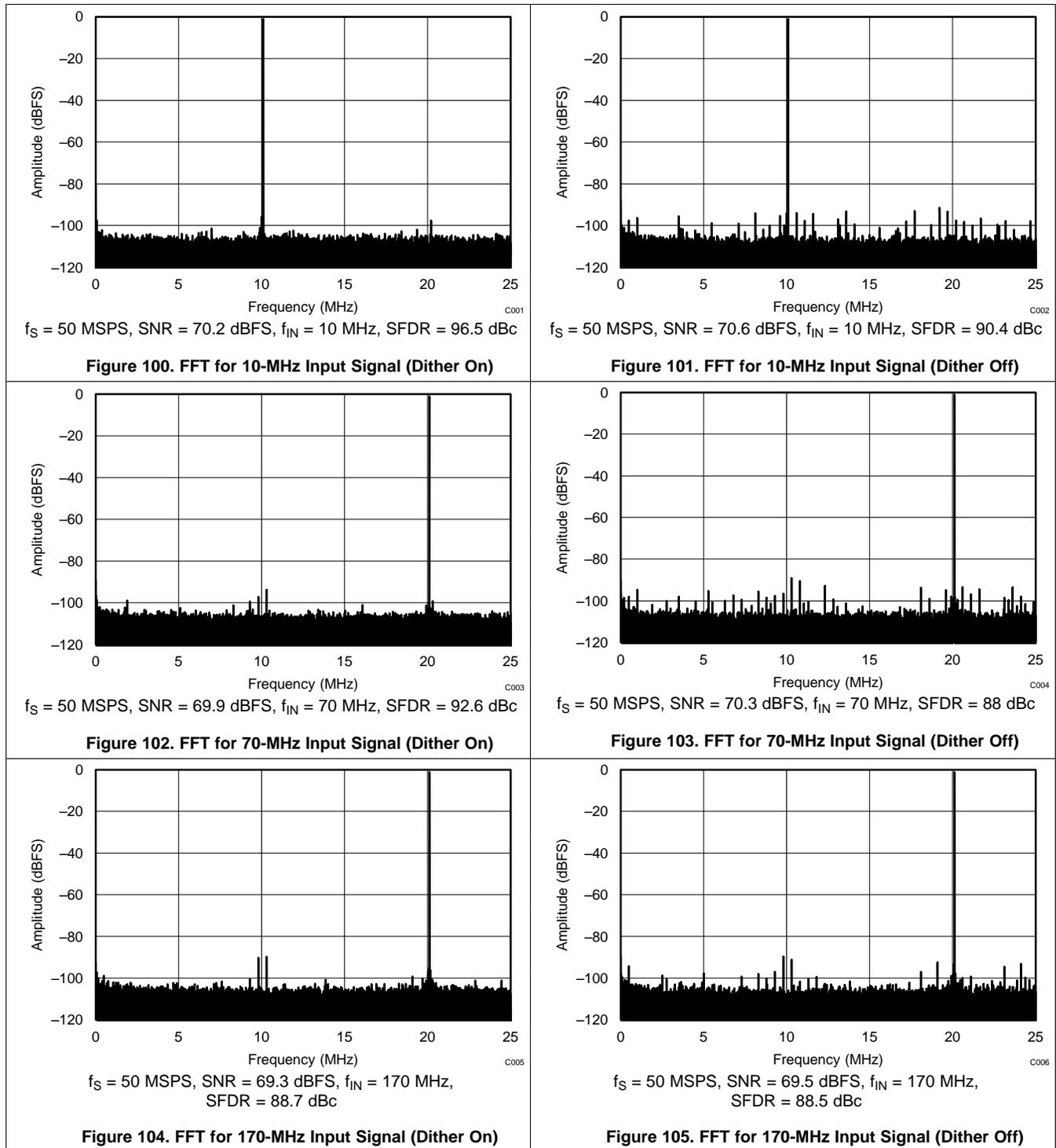


Figure 99. Idle Channel Histogram

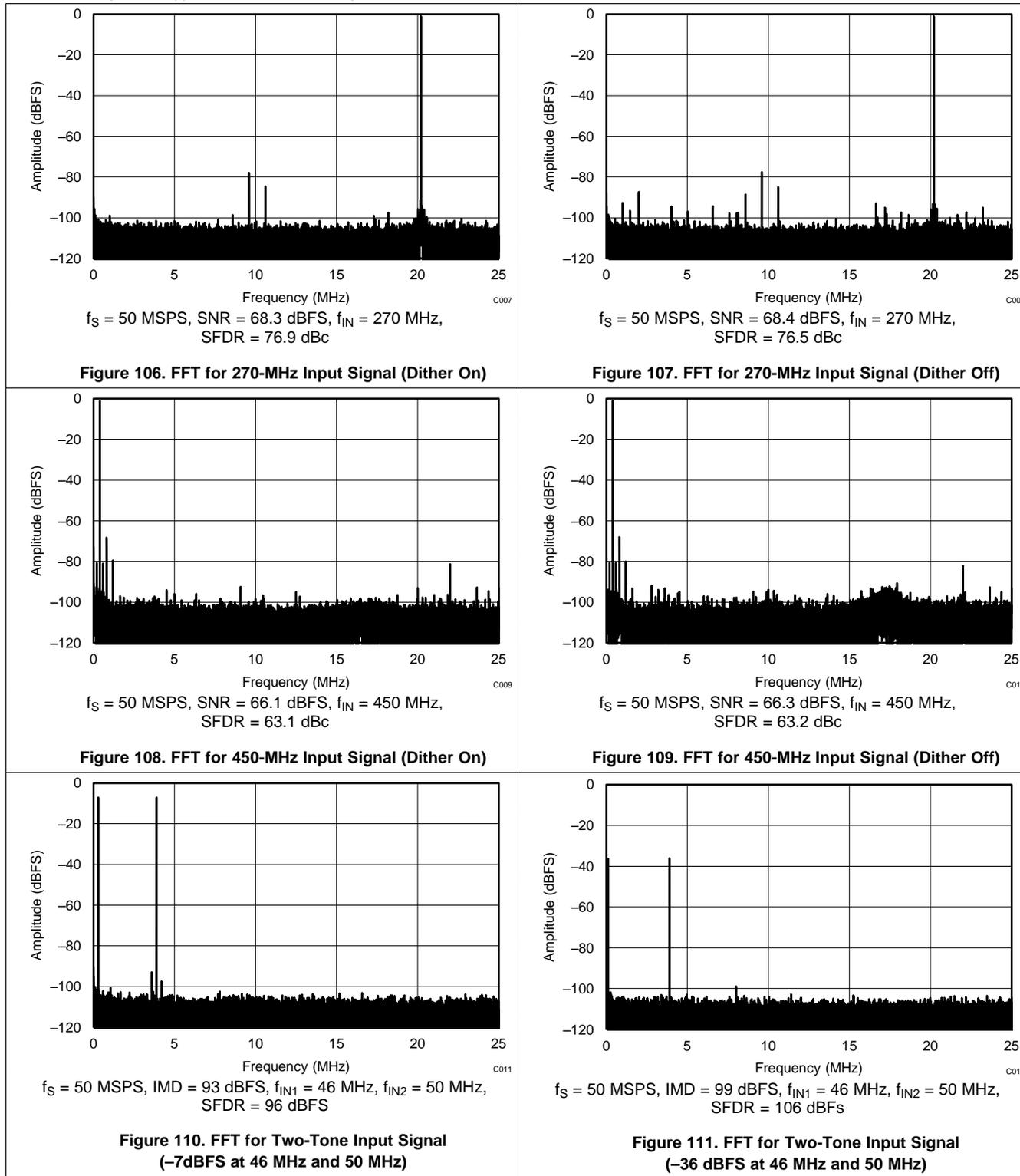
7.18 Typical Characteristics: ADC34J22

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



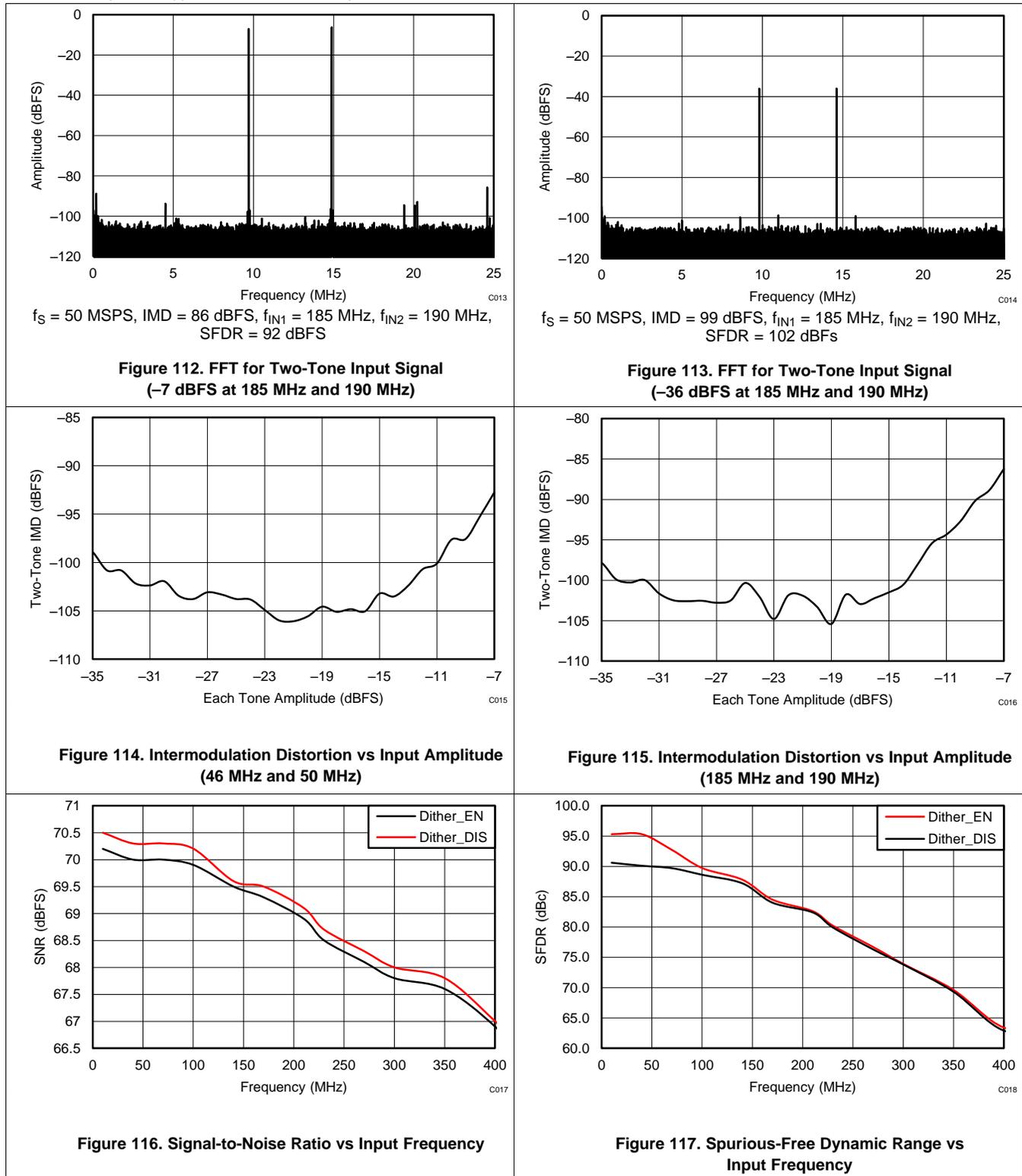
Typical Characteristics: ADC34J22 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J22 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J22 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.

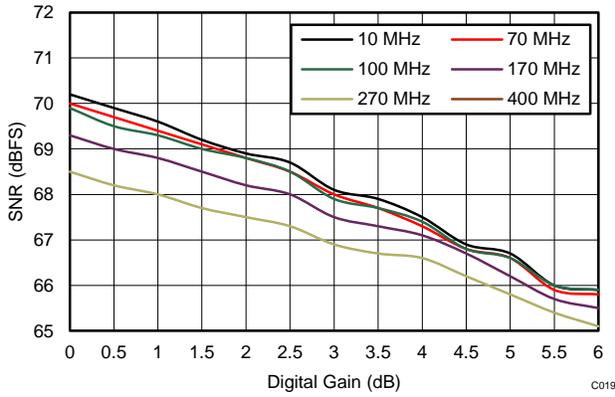


Figure 118. Signal-to-Noise Ratio vs Digital Gain and Input Frequency

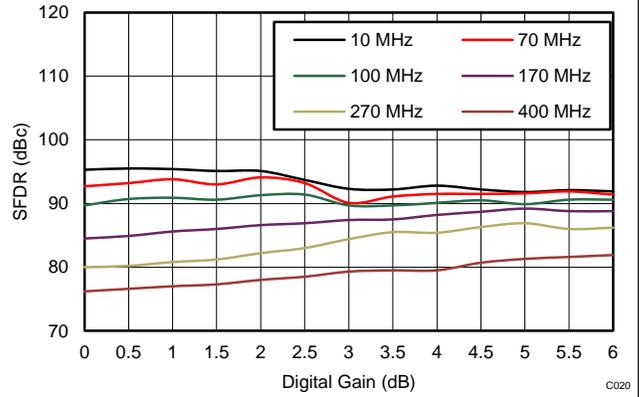


Figure 119. Spurious-Free Dynamic Range vs Digital Gain and Input Frequency

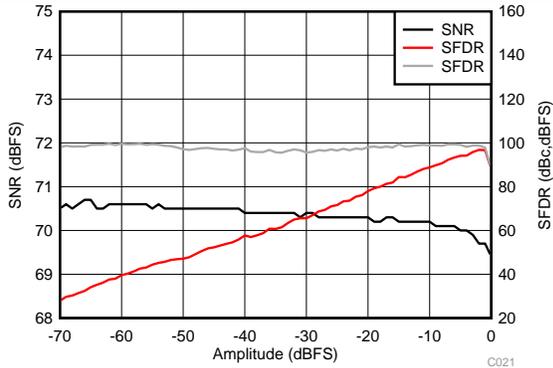


Figure 120. Performance vs Input Amplitude (30 MHz)

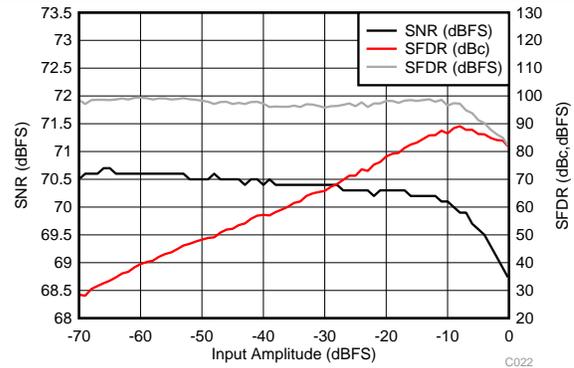


Figure 121. Performance vs Input Amplitude (170 MHz)

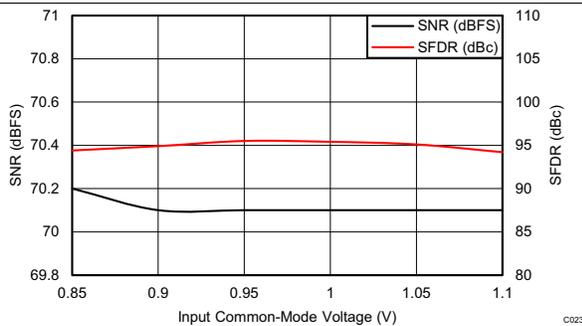


Figure 122. Performance vs Input Common-Mode Voltage (30 MHz)

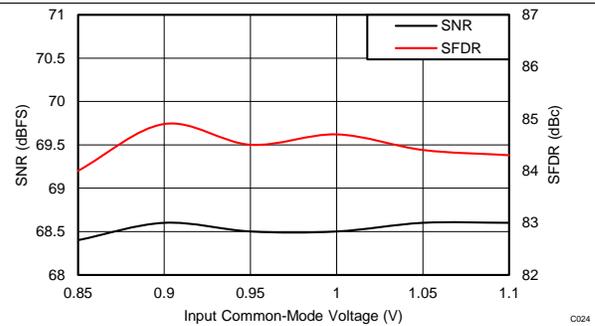
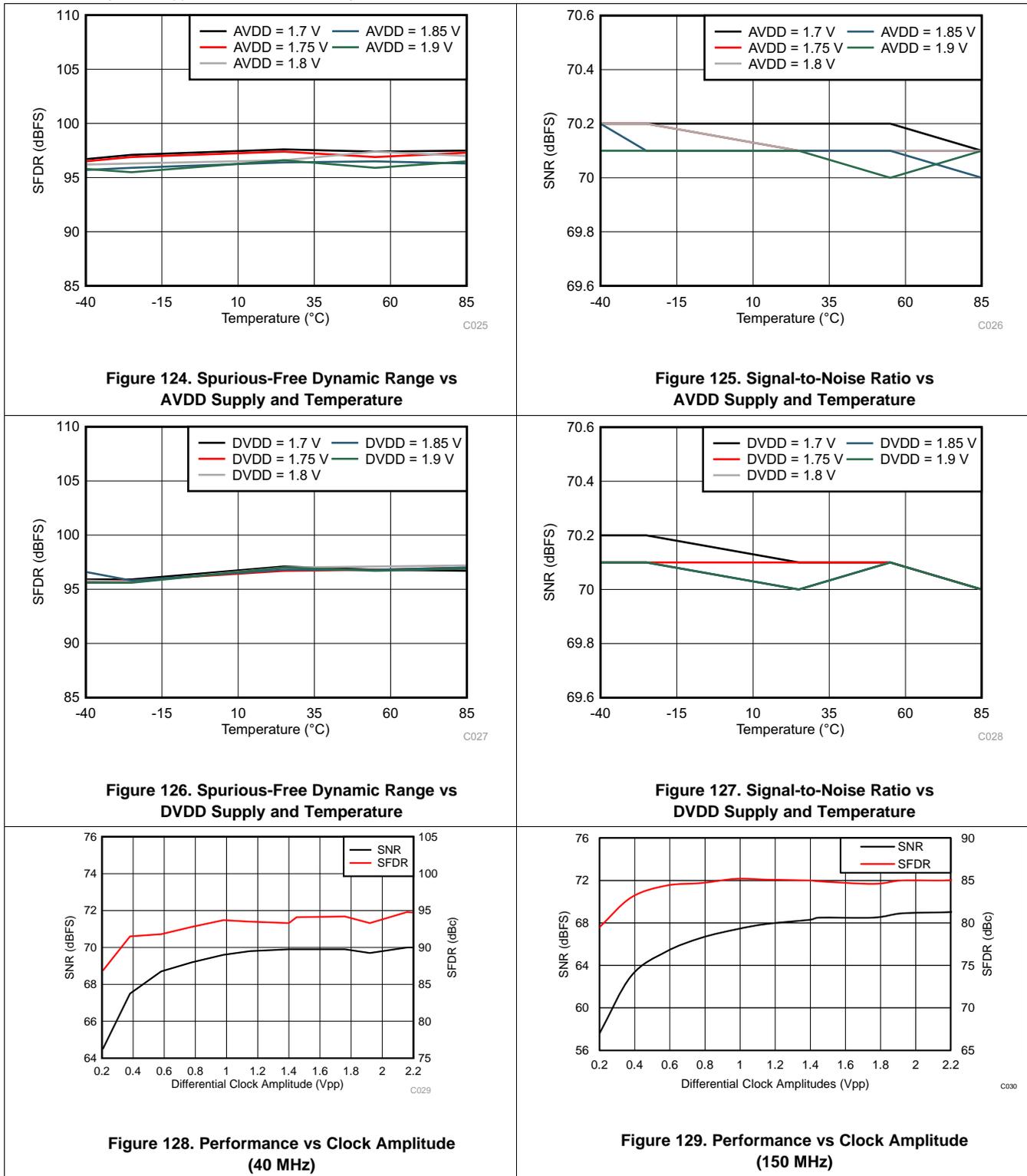


Figure 123. Performance vs Input Common-Mode Voltage (170 MHz)

Typical Characteristics: ADC34J22 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



Typical Characteristics: ADC34J22 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $AV_{DD} = DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.

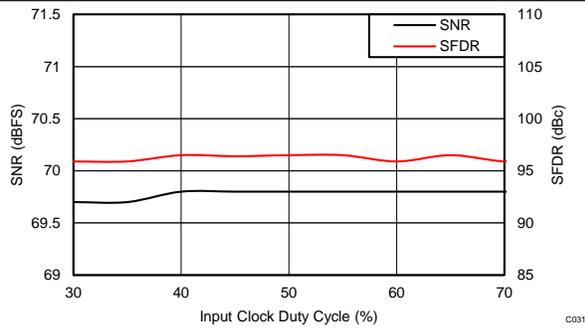


Figure 130. Performance vs Clock Duty Cycle (40 MHz)

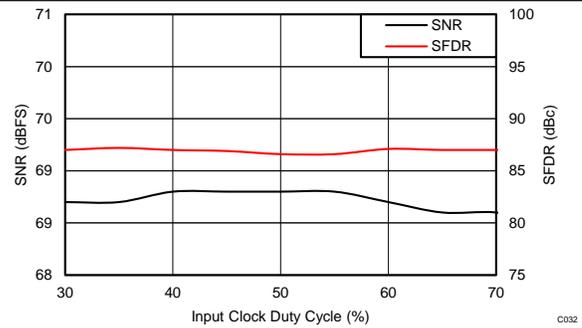


Figure 131. Performance vs Clock Duty Cycle (150 MHz)

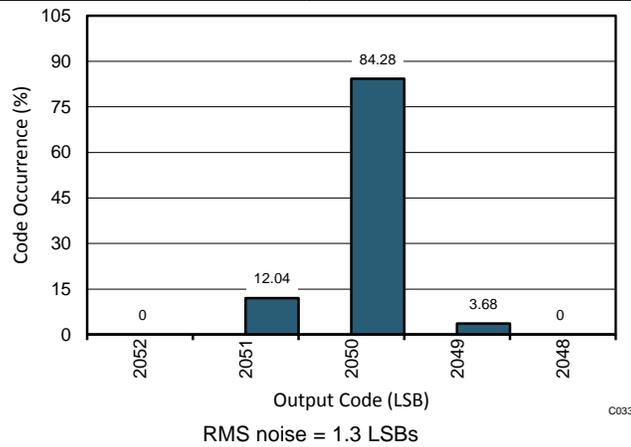
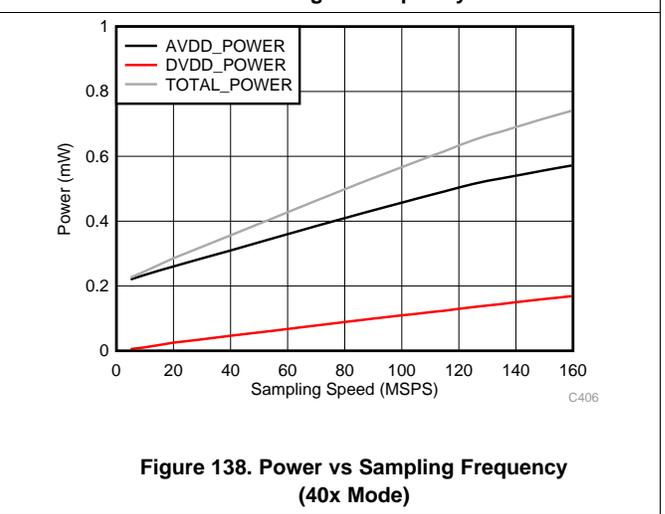
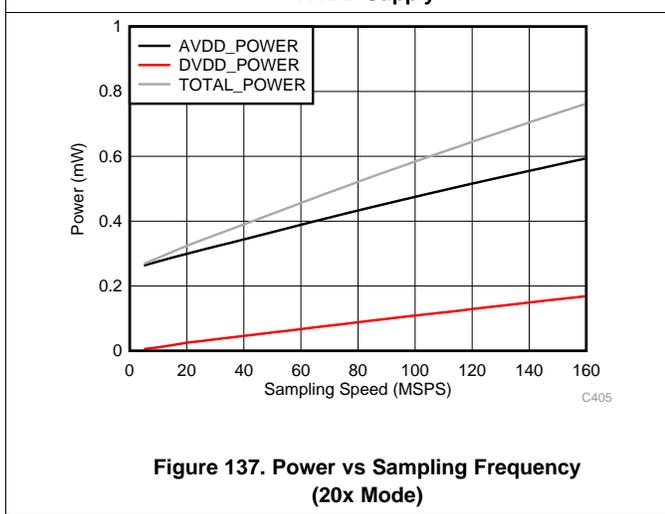
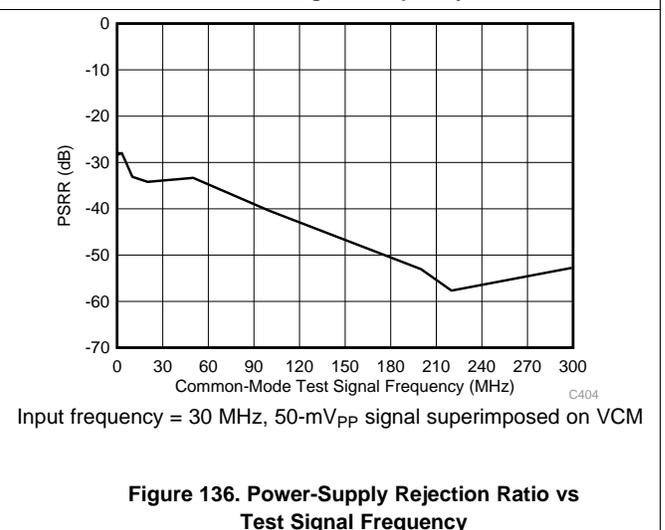
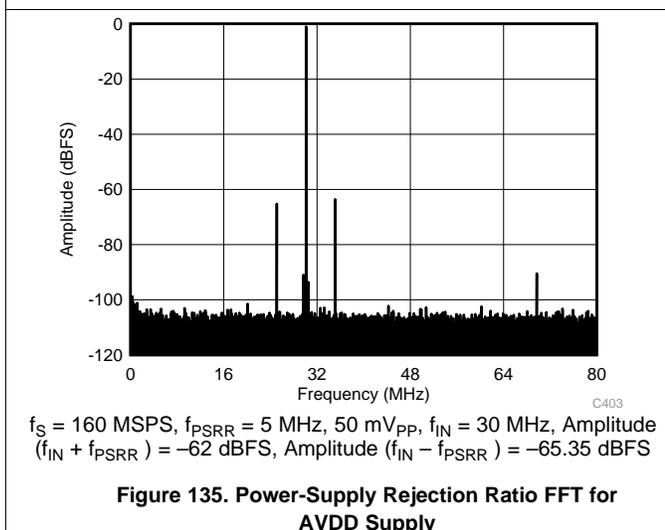
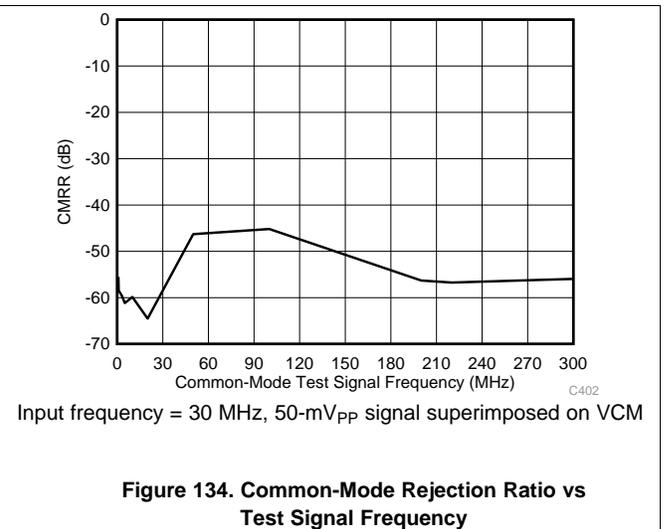
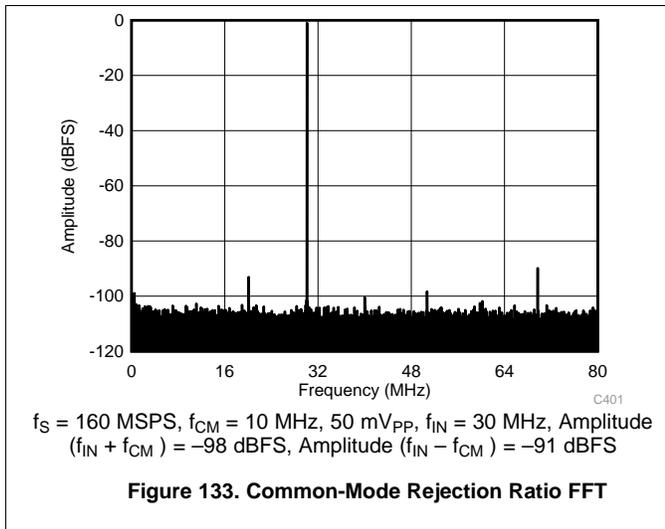


Figure 132. Idle Channel Histogram

7.19 Typical Characteristics: Common Plots

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 160 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.



7.20 Typical Characteristics: Contour Plots

Typical values are at $T_A = 25^\circ\text{C}$, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.

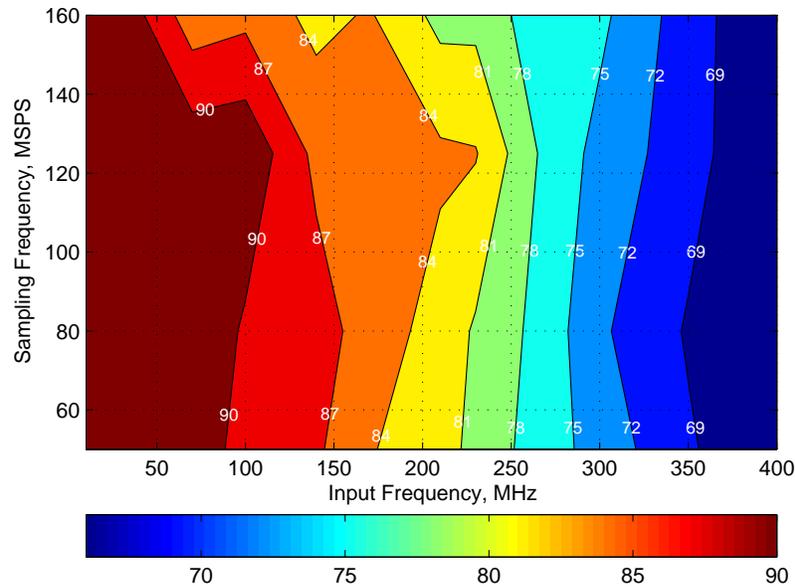


Figure 139. Spurious-Free Dynamic Range (SFDR) for 0-dB Gain

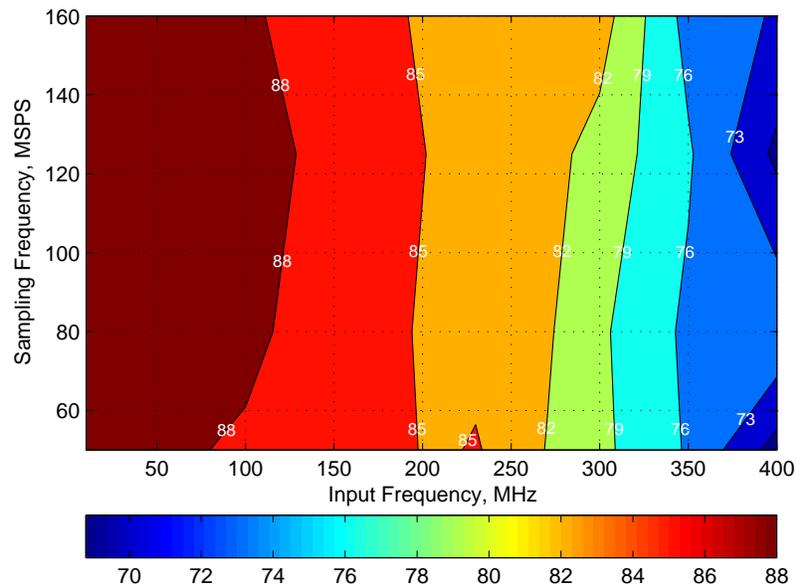


Figure 140. Spurious-Free Dynamic Range (SFDR) for 6-dB Gain

Typical Characteristics: Contour Plots (continued)

Typical values are at $T_A = 25^\circ\text{C}$, 50% clock duty cycle, $AVDD = DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, and 32k-point FFT, unless otherwise noted.

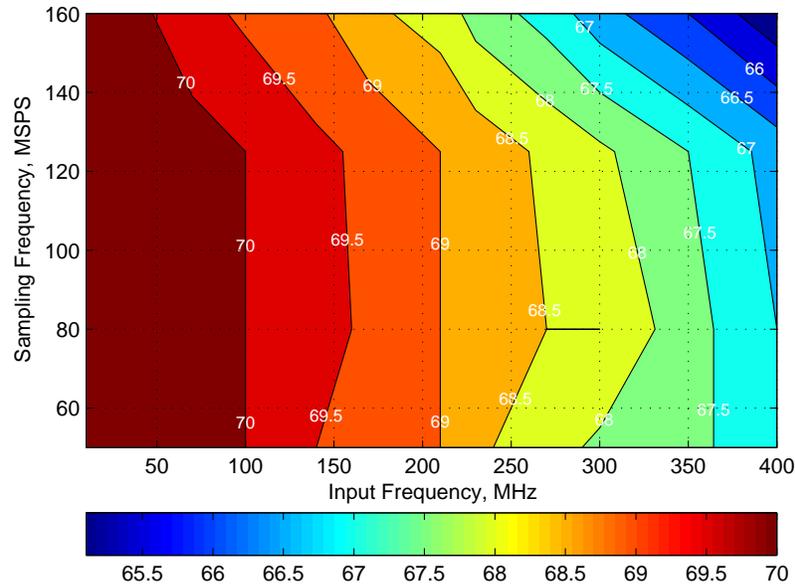


Figure 141. Signal-to-Noise Ratio (SNR) for 0-dB Gain

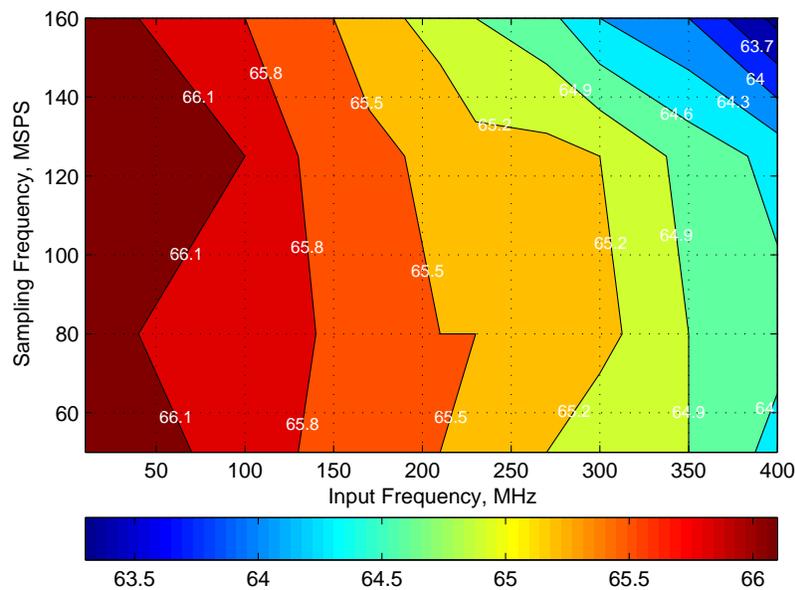
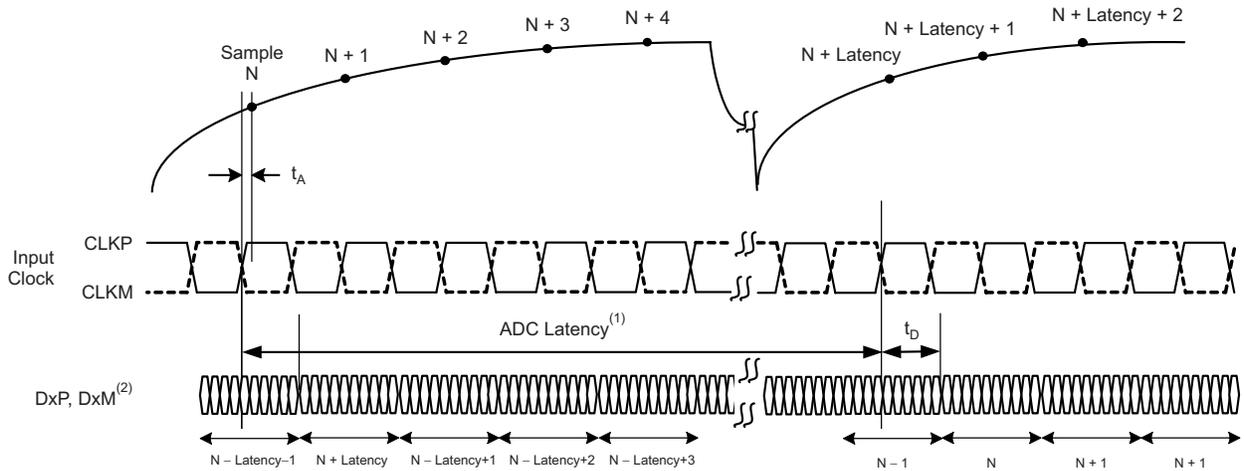


Figure 142. Signal-to-Noise Ratio (SNR) for 6-dB Gain

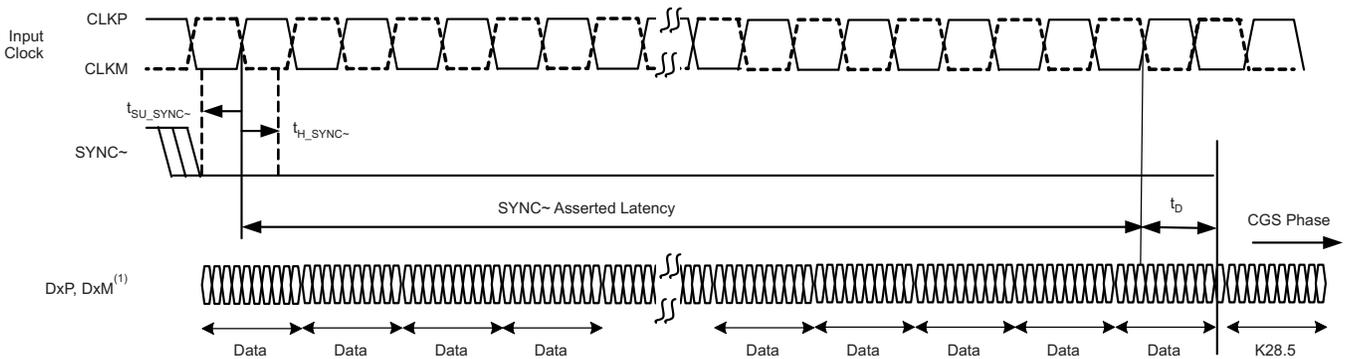
8 Parameter Measurement Information

8.1 Timing Diagrams



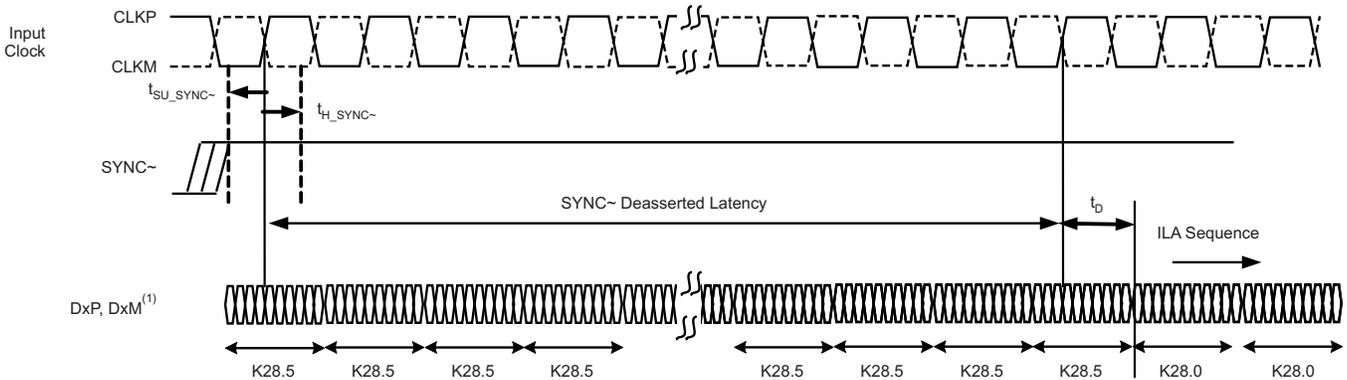
- (1) Overall latency = ADC latency + t_D .
- (2) $x = A$ for channel A and B for channel B.

Figure 143. ADC Latency



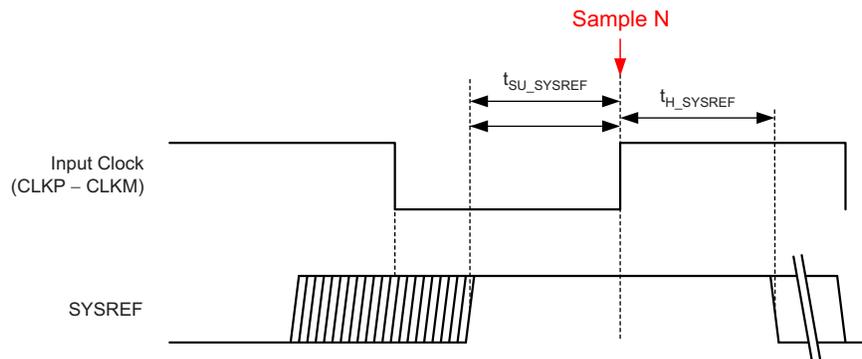
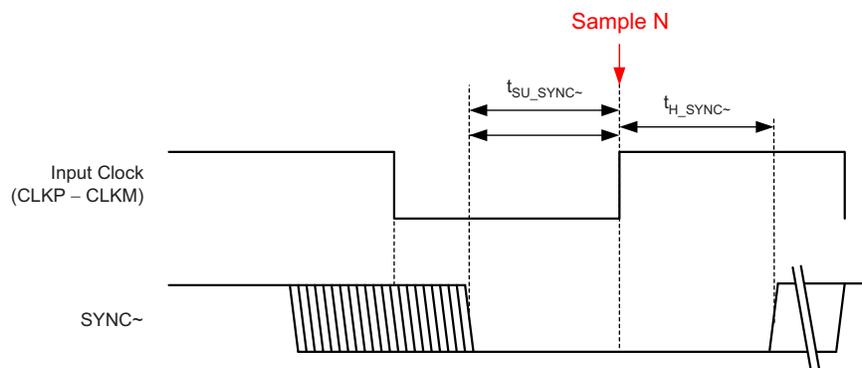
- (1) $x = A$ for channel A, B for channel B, C for channel C, and D for channel D.

Figure 144. SYNC~ Latency in CGS Phase (Two-Lane Mode)



- (1) $x = A$ for channel A, B for channel B, C for channel C, and D for channel D.

Figure 145. SYNC~ Latency in ILAS Phase (Two-Lane Mode)

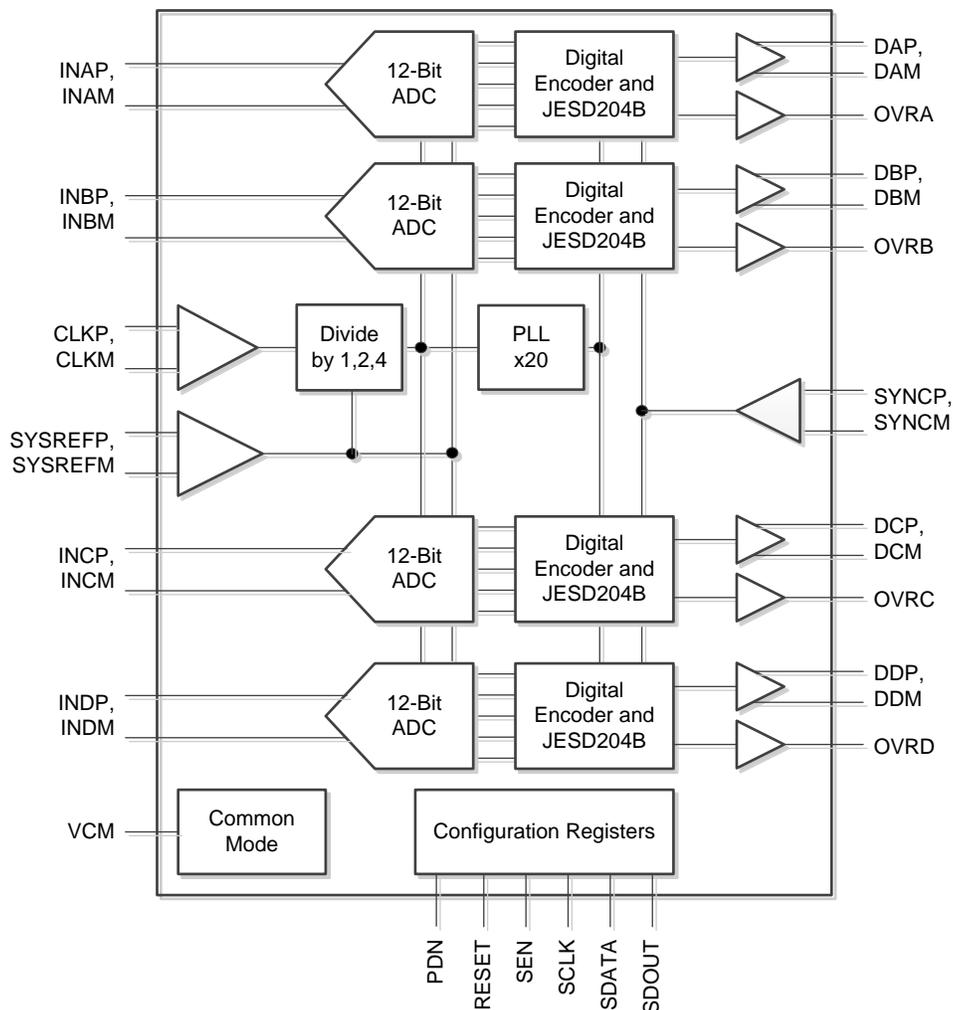
Timing Diagrams (continued)

Figure 146. SYSREF Timing (Subclass 1)

Figure 147. SYNC~ Timing (Subclass 2)

9 Detailed Description

9.1 Overview

The ADC34J2x are a high-linearity, ultra-low power, dual-channel, 12-bit, 50-MSPS to 160-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. A clock input divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The ADC34J2x family supports JESD204B interface in order to reduce the number of interface lines, thus allowing for high system integration density. The JESD204B interface is a serial interface, where the data of each ADC are serialized and output over only one differential pair. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock by 20 to derive the bit clock, which is used to serialize the 12-bit data from each channel. The ADC34J2x devices support subclass 1 with interface data rates up to 3.2 Gbps.

9.2 Functional Block Diagram



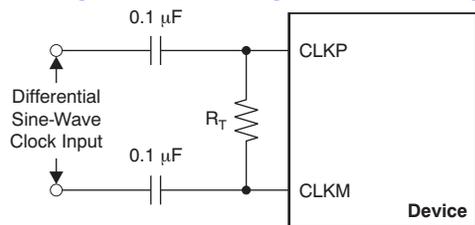
9.3 Feature Description

9.3.1 Analog Inputs

The ADC34J2x analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between $(V_{CM} + 0.5\text{ V})$ and $(V_{CM} - 0.5\text{ V})$, resulting in a $2\text{-}V_{PP}$ (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 450 MHz (50- Ω source driving 50- Ω termination between INP and INM).

9.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 1.4 V using internal 5-k Ω resistors. The self-bias clock inputs of the ADC34J2x can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 148, Figure 149, and Figure 150. See Figure 151 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

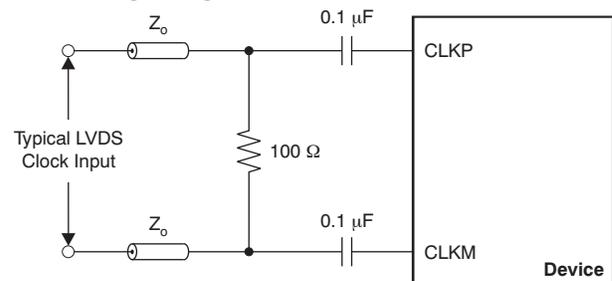


Figure 148. Differential Sine-Wave Clock Driving Circuit

Figure 149. LVDS Clock Driving Circuit

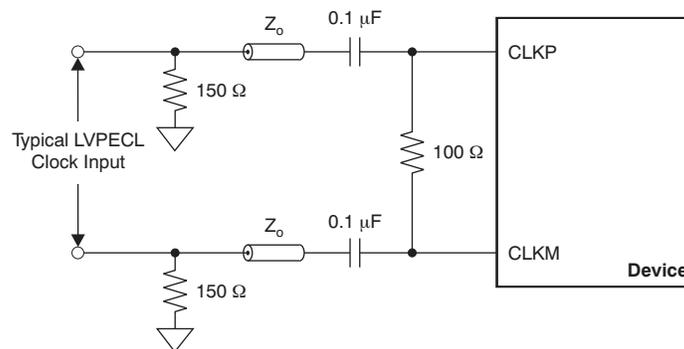
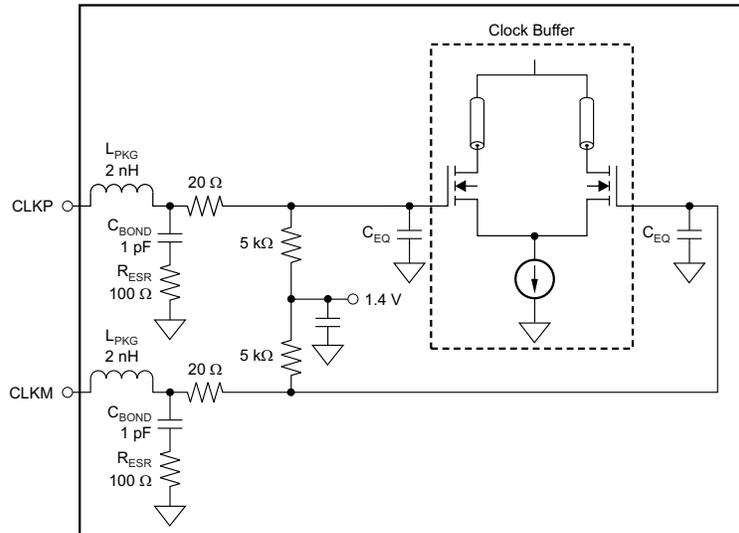


Figure 150. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 151. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1- μ F capacitor, as shown in Figure 152. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

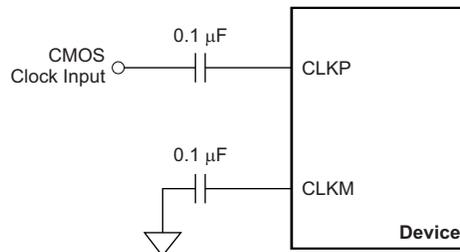


Figure 152. Single-Ended Clock Driving Circuit

9.3.2.1 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter noise, as shown in Equation 1. Quantization noise is typically not noticeable in pipeline converters and is 74 dBFS for a 12-bit ADC. Thermal noise limits SNR at low input frequencies while the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation resulting from sample clock jitter can be calculated with Equation 2:

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter}) \quad (2)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (200 fs for the device) which is set by the noise of the clock input buffer and the external clock. T_{Jitter} can be calculated with Equation 3:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock_Input})^2 + (T_{Aperture_ADC})^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter. The devices have a thermal noise of 73.5 dBFS and internal aperture jitter of 200 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in [Figure 153](#).

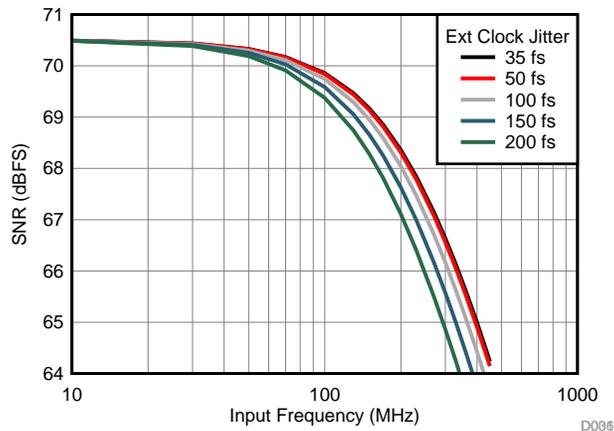


Figure 153. SNR vs Frequency vs Jitter

9.3.2.2 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider can be bypassed (divide-by-1) for operation with a 160-MHz clock while the divide-by-2 option supports a maximum input clock of 320 MHz and the divide-by-4 option supports a maximum input clock frequency of 640 MHz.

9.3.3 Power-Down Control

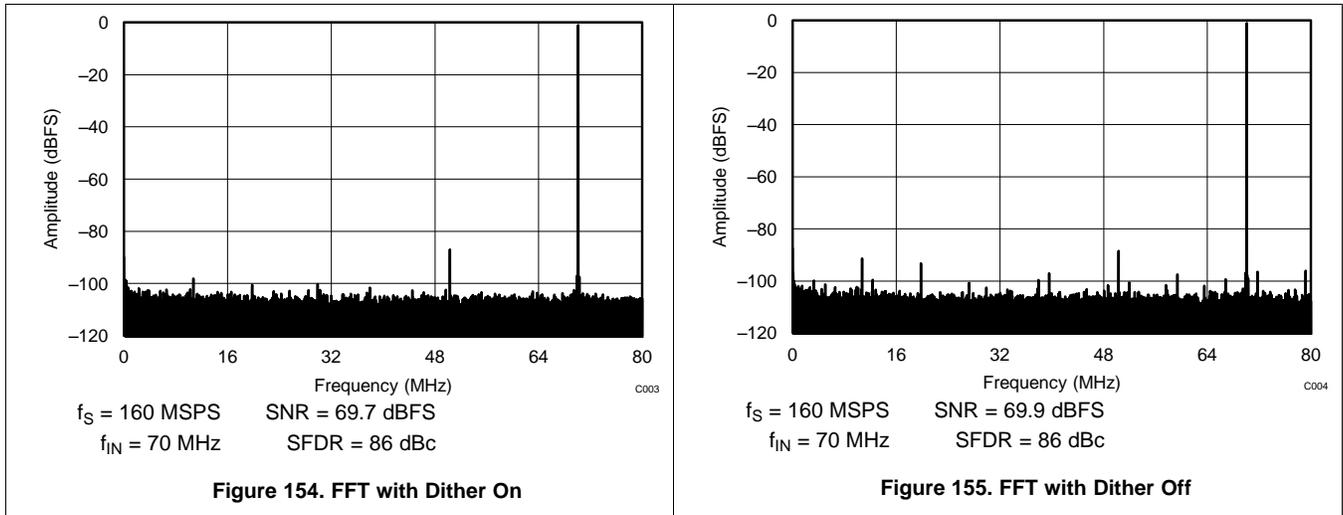
The power-down functions of the ADC34J2x can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see [Figure 181](#), register 15h). The PDN pin can also be configured via SPI to a global power-down or standby functionality.

Table 3. Power-Down Modes

FUNCTION	POWER CONSUMPTION (mW)	WAKE-UP TIME (μ s)
Global power-down	5	85
Standby	185	35

9.3.4 Internal Dither Algorithm

The ADC34J2x uses an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. Figure 154 and Figure 155 show the effect of using dither algorithms.



9.3.5 JESD204B Interface

The ADC34J2x support device subclass 0, 1, and 2 with a maximum output data rate of 3.2 Gbps for each serial transmitter, as shown in Figure 156. The data of each ADC are serialized by 20x using an internal PLL and then transmitted out on one differential pair each. An external SYSREF (subclass 1) or SYNC (subclass 2) signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This process allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty.

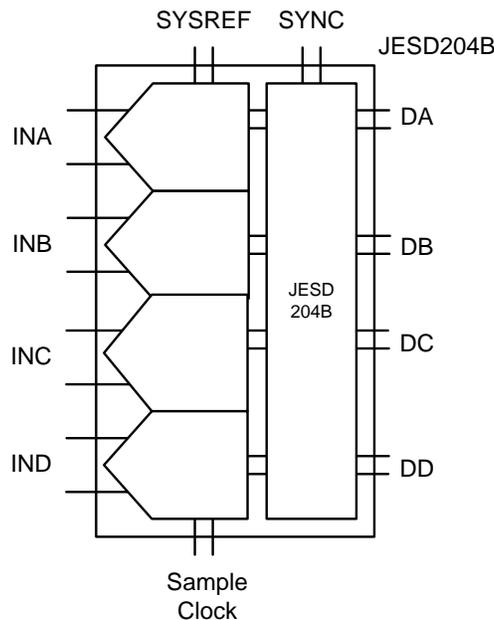


Figure 156. JESD204B Interface

The JESD204B transmitter block consists of the transport layer, the data scrambler, and the link layer, as shown in Figure 157. The transport layer maps the ADC output data into the selected JESD204B frame data format and determines if the ADC output data or test patterns are transmitted. The link layer performs the 8b or 10b data encoding and the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

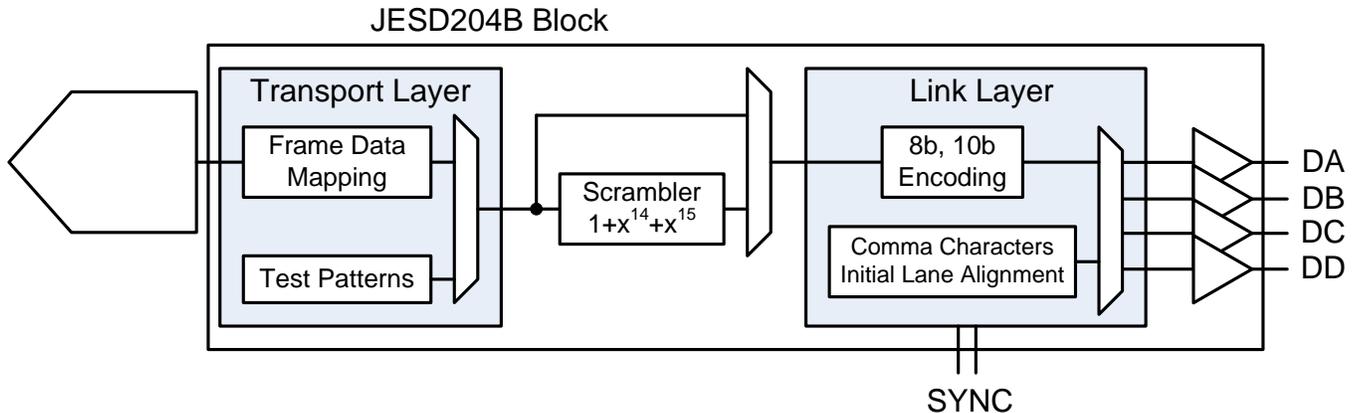


Figure 157. JESD204B Block

9.3.5.1 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started by the receiving device by asserting the SYNC signal. When a logic high is detected on the SYNC input pins, the ADC34J2x starts transmitting comma (K28.5) characters to establish code group synchronization. When synchronization is complete, the receiving device de-asserts the SYNC signal and the ADC34J2x starts the initial lane alignment sequence with the next local multiframe clock boundary. The ADC34J2x transmits four multiframes, each containing K frames (K is SPI programmable). Each multiframe contains the frame start and end symbols; the second multiframe also contains the JESD204 link configuration data.

9.3.5.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADC34J2x supports a clock output, an encoded, and a PRBS ($2^{15} - 1$) pattern. These patterns can be enabled via SPI register writes and are located in address 2Ah (bits 7:6).

9.3.5.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per link,
- M is the number of converters per device,
- F is the number of octets per frame clock period, and
- S is the number of samples per frame.

Table 4 lists the available JESD204B format and valid range for the ADC34J2x. The ranges are limited by the SERDES line rate and the maximum ADC sample frequency.

Table 4. LMFS Values and Interface Rate

L	M	F	S	MINIMUM ADC SAMPLING RATE (MSPS)	MAXIMUM f_{SERDES} (Mbps)	MAXIMUM ADC SAMPLING RATE (MSPS)	MAXIMUM f_{SERDES} (GSPS)	MODE
4	4	2	1	15	300	160	3.2	20x (default)
2	4	4	1	10	400	80	3.2	40x

The detailed frame assembly for quad-channel mode is shown in Figure 158. The frame assembly configuration can be changed from 20x (default) to 40x by setting the registers listed in Table 5.

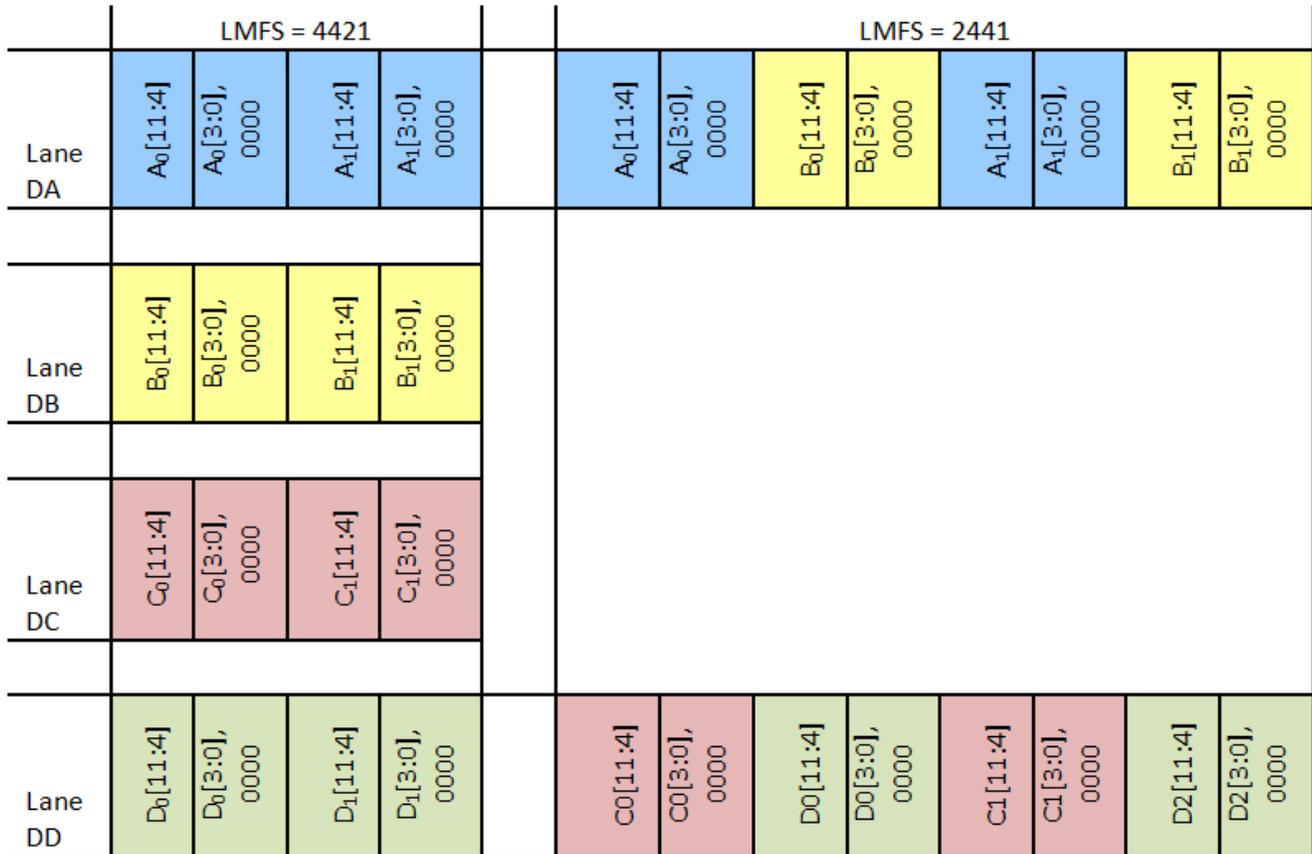


Figure 158. JESD Frame Assembly

Table 5. Configuring 40x Mode

ADDRESS	DATA
2Bh	01h
30h	11h

9.3.5.4 Digital Outputs

The ADC34J2x JESD204B transmitter uses differential CML output drivers. The CML output current is programmable from 5 mA to 20 mA using SPI register settings. The output driver expects to drive a differential 100-Ω load impedance and the termination resistors should be placed as close to the receiver inputs as possible to avoid unwanted reflections and signal distortion. Because the JESD204B employs 8b, 10b encoding, the output data stream is dc-balanced and ac-coupling can be used to avoid the need to match up common-mode voltages between the transmitter and receivers. The termination resistors should be connected to the termination voltage as shown in Figure 159.

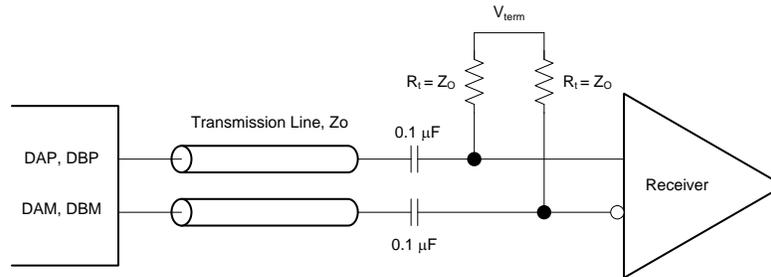


Figure 159. CML Output Connections

Figure 160 shows the data eye measurements of the device JESD204B transmitter against the JESD204B transmitter mask at 3.125 Gbps (156.25 MSPS, 20x mode), respectively.

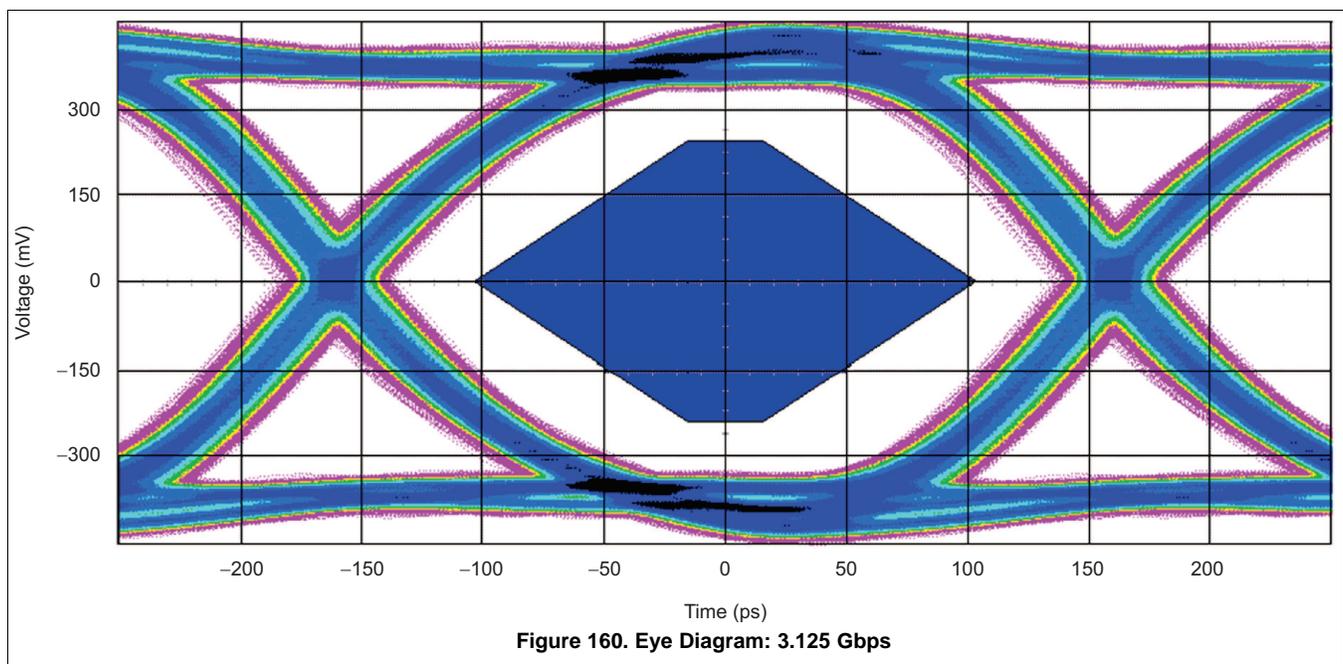


Figure 160. Eye Diagram: 3.125 Gbps

9.4 Device Functional Modes

9.4.1 Digital Gain

The input full-scale amplitude can be selected between $1 V_{PP}$ to $2 V_{PP}$ (default is $2 V_{PP}$) by choosing the appropriate digital gain setting via an SPI register write. Digital gain provides an option to trade-off SNR for SFDR performance. A larger input full-scale increases SNR performance ($2 V_{PP}$ is recommended for maximum SNR) while reduced input swing typically results in better SFDR performance. [Table 6](#) lists the available digital gain settings.

Table 6. Digital Gain vs Full-Scale Amplitude

DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})
0	2.0
0.5	1.89
1	1.78
1.5	1.68
2	1.59
2.5	1.50
3	1.42
3.5	1.34
4	1.26
4.5	1.19
5	1.12
5.5	1.06
6	1.00

9.4.2 Overrange Indication

The ADC34J2x provides two different overrange indications. The normal OVR (default) is triggered if the final 14-bit data output exceeds the maximum code value. The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after just nine clock cycles, thus enabling a quicker reaction to an overrange event. By default, the normal overrange indication is output on the OVRx pins (where x is A, B, C, or D). The fast OVR indication can be presented on the overrange pins instead by using the SPI register map.

9.5 Programming

The ADS34Jxx can be configured using a serial programming interface, as described in this section.

9.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

Programming (continued)

9.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to their default values through a **hardware reset** by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in [Figure 161](#). If required, the serial interface registers can be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

[Figure 161](#) and [Table 7](#) show the timing requirements for the serial register write operation.

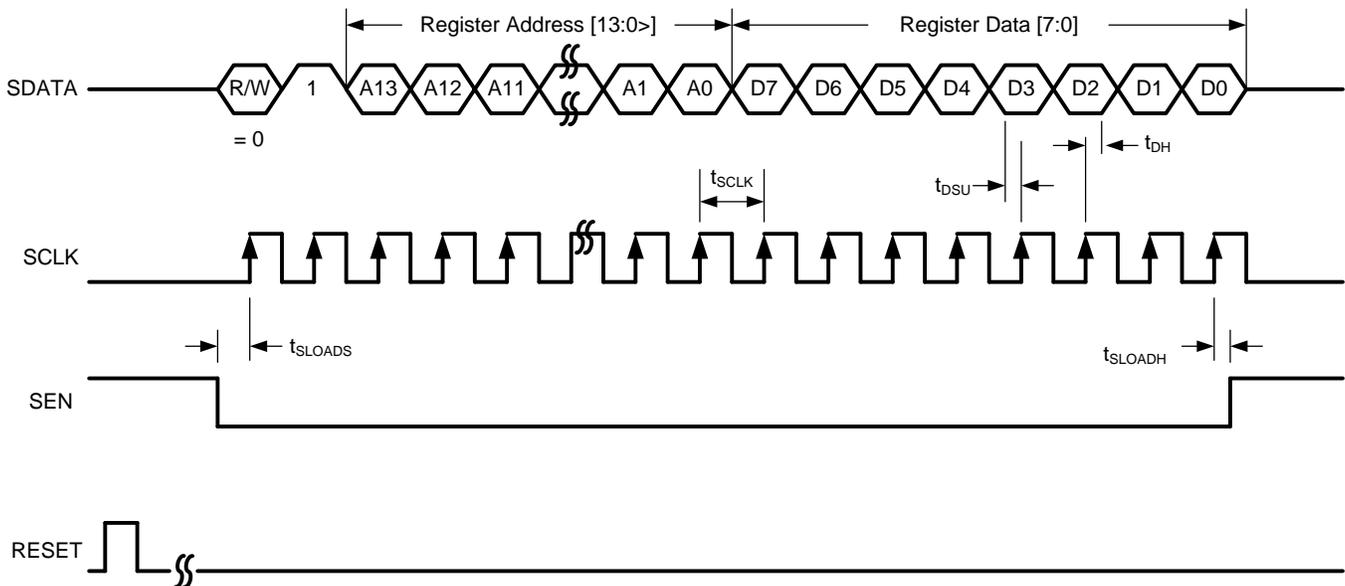


Figure 161. Serial Register Write Timing Diagram

Table 7. Serial Interface Timing⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to $1 / t_{SCLK}$)	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at 25°C, full temperature range is from $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = 85^{\circ}\text{C}$, and $AVDD = DVDD = 1.8\text{ V}$, unless otherwise noted.

9.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. Given below is the procedure to read contents of serial registers:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 162 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 163.

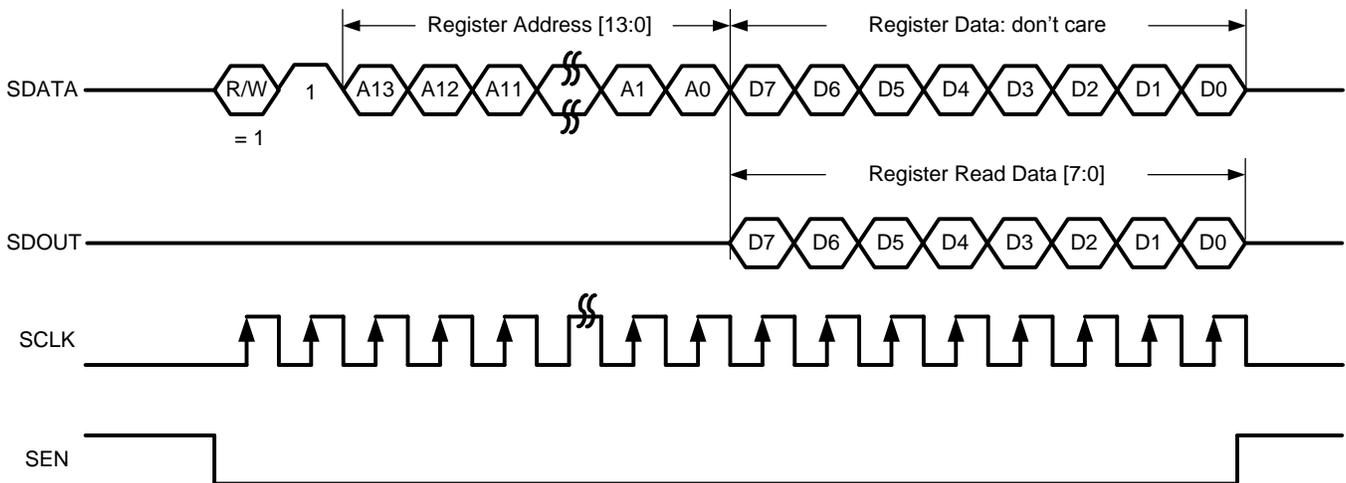


Figure 162. Serial Register Read Timing Diagram

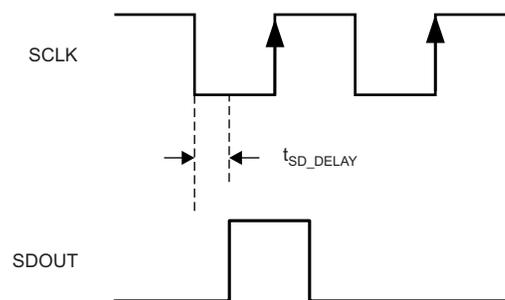


Figure 163. SDOUT Timing Diagram

9.5.2 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in [Figure 164](#) and [Table 8](#).

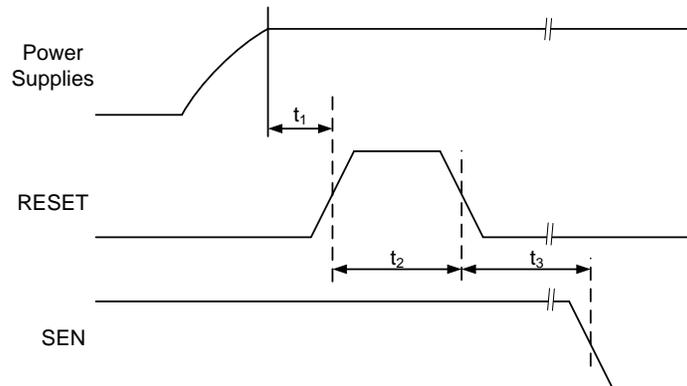


Figure 164. Initialization of Serial Registers after Power-Up

Table 8. Power-Up Timing

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up to active high RESET pulse		1	ms
t_2	Reset pulse width	Active high RESET pulse width		1000	ns
t_3	Register write delay	Delay from RESET disable to SEN active		100	ns

If required, the serial interface registers can be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.3 Start-Up Sequence

After power-up, the sequence described in [Table 9](#) can be used to set up the ADC34J2x for basic operation.

Table 9. Start-Up Settings

STEP	DESCRIPTION	REGISTER ADDRESS AND DATA
1	Bring up all supply voltages. There is no required power supply sequence for AVDD and DVDD	—
2	Pulse hardware reset (low to high to low) on pin 24	—
3	Optional configure LMFS of JESD204B interface to LMFS = 2441 (default is LMFS = 4421)	Address 2Bh, data 01h Address 30h, data 11h
4	Pulse SYNC~ from high to low to transmit data from k28.5 sync mode	—

9.6 Register Map

Table 10. Serial Register Map

REGISTER ADDRESS	REGISTER DATA							
A[13:0] (Hex)	7	6	5	4	3	2	1	0
01	DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	
02	0	0	0	0	0	0	CHA GAIN EN	0
03	0	0	0	0	0	0	CHB GAIN EN	0
04	0	0	0	0	0	0	CHC GAIN EN	0
05	0	0	0	0	0	0	CHD GAIN EN	0
06	0	0	0	SPECIAL MODE1 CHA			TEST PATTERN EN	RESET
07	0	0	0	SPECIAL MODE1 CHB			EN FOVR	0
08	0	0	0	SPECIAL MODE1 CHC			0	0
09	0	0	0	SPECIAL MODE1 CHD			ALIGN TEST PATTERN	DATA FORMAT
0A	CHA TEST PATTERN				CHB TEST PATTERN			
0B	CHC TEST PATTERN				CHD TEST PATTERN			
0C	CHA DIGITAL GAIN				CHB DIGITAL GAIN			
0D	CHC DIGITAL GAIN				CHD DIGITAL GAIN			
0E	CUSTOM PATTERN[11:4]							
0F	CUSTOM PATTERN [3:0]				0	0	0	0
13	LOW SPEED MODE	0	0	0	0	0	0	0
15	CHA PDN	CHB PDN	CHC PDN	CHD PDN	STANDBY	GLOBAL PDN	0	PDN PIN DISABLE
27	CLK DIV		0	0	0	0	0	0
2A	SERDES TEST PATTERN		IDLE SYNC	TRP LAYER TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TXMIT LINKDATA DIS
2B	0	0	0	0	0	0	CTRL K	CTRL F
2F	SCR (SCR EN)	0	0	0	0	0	0	0
30	OCTETS PER FRAME							
31	0	0	0	FRAMES PER MULTI FRAME				
34	SUBCLASSV			0	0	0	0	0
3A	SYNC REQ	OPTION SYNC REG	0	0	OUTPUT CURRENT SEL			
3B	LINK LAYER TESTMODE SEL[2:0]			LINK LAYER RPAT	0	PULSE DET MODES		

Register Map (continued)
Table 10. Serial Register Map (continued)

REGISTER ADDRESS	REGISTER DATA								
	A[13:0] (Hex)	7	6	5	4	3	2	1	0
3C	FORCE LMFC COUNT	LMFC COUNT INIT						LMFC COUNT INIT	
122	0	0	0	0	0	0	SPECIAL MODE2 CHA [1:0]		
134	0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0	
222	0	0	0	0	0	0	SPECIAL MODE2 CHD [1:0]		
234	0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0	
422	0	0	0	0	0	0	SPECIAL MODE2 CHB [1:0]		
434	0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0	
522	0	0	0	0	0	0	SPECIAL MODE2 CHC [1:0]		
534	0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0	

9.6.1 Serial Register Description

Figure 165. Register 01h

7	6	5	4	3	2	1	0
DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	

Table 11. Register 01h Description

Name	Description
Bits 7:6	DIS DITH CHA
	00 = Default 11 = Dither is disabled, high SNR mode is selected for channel A. In this mode, SNR typically improves by 0.3 dB at 70 MHz. Ensure that register 134 (bits 5 and 3) are also set to 11.
Bits 5:4	DIS DITH CHB
	00 = Default 11 = Dither is disabled, high SNR mode is selected for channel B. In this mode, SNR typically improves by 0.3 dB at 70 MHz. Ensure that register 434 (bits 5 and 3) are also set to 11.
Bits 3:2	DIS DITH CHC
	00 = Default 11 = Dither is disabled, high SNR mode is selected for channel C. In this mode, SNR typically improves by 0.3 dB at 70 MHz. Ensure that register 534 (bits 5 and 3) are also set to 11.
Bits 1:0	DIS DITH CHD
	00 = Default 11 = Dither is disabled, high SNR mode is selected for channel D. In this mode, SNR typically improves by 0.3 dB at 70 MHz. Ensure that register 234 (bits 5 and 3) are also set to 11.

Figure 166. Register 02h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHA GAIN EN	0

Table 12. Register 02h Description

Name	Description
Bits 7:2	Must write 0
Bit 1	CHA GAIN EN
	Enable digital gain control for channel A. 0 = Default 1 = Digital gain for channel A can be programmed with the CHA DIGITAL GAIN bits.
Bit 0	Must write 0

Figure 167. Register 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHB GAIN EN	0

Table 13. Register 03h Description

Name	Description
Bits 7:2	Must be 0
Bit 1	CHB GAIN EN:
	Enable digital gain control for channel B. 0 = Default 1 = Digital gain for channel B can be programmed with the CHB DIGITAL GAIN bits.
Bit 0	Must write 0

Figure 168. Register 04h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHC GAIN EN	0

Table 14. Register 04h Description

Name	Description
Bits 7:2	Must write 0
Bit 1	CHC GAIN EN
	Enable digital gain control for channel C. 0 = Default 1 = Digital gain for channel C can be programmed with the CHC DIGITAL GAIN bits.
Bit 0	Must write 0

Figure 169. Register 05h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CHD GAIN EN	0

Table 15. Register 05h Description

Name	Description
Bits 7:2	Must write 0
Bit 1	CHD GAIN EN:
	Enable digital gain control for channel D 0 = Default 1 = Digital gain for channel D can be programmed with the CHD DIGITAL GAIN bits.
Bit 0	Must write 0

Figure 170. Register 06h

7	6	5	4	3	2	1	0
0	0	0	SPECIAL MODE1 CHA			TEST PATTERN EN	RESET

Table 16. Register 06h Description

Name	Description
Bits 7:5	Must write 0
Bits 4:2	SPECIAL MODE1 CHA
	010 = For frequencies < 120 MHz 111 = For frequencies > 120 MHz
Bit 1	TEST PATTERN EN
	This bit enables test pattern selection for the digital outputs. 0 = Normal operation 1 = Test pattern output enabled
Bit 0	RESET: Software reset applied
	This bit resets all internal registers to the default values and self-clears to 0.

Figure 171. Register 07h

7	6	5	4	3	2	1	0
0	0	0	SPECIAL MODE1 CHB			EN FOVR	0

Table 17. Register 07h Description

Name	Description
Bits 7:5	Must write 0
Bits 4:2	SPECIAL MODE1 CHB
	010 = For frequencies < 120 MHz 111 = For frequencies > 120 MHz
Bit 1	EN FOVR
	0 = Normal OVR on OVRx pins 1 = Enable fast OVR on OVRx pins
Bit 0	Must write 0

Figure 172. Register 08h

7	6	5	4	3	2	1	0
0	0	0	SPECIAL MODE1 CHC			0	0

Table 18. Register 08h Description

Name	Description
Bits 7:5	Must write 0
Bits 4:2	SPECIAL MODE1 CHC
	010 = For frequencies < 120 MHz 111 = For frequencies > 120 MHz
Bits 1:0	Must write 0

Figure 173. Register 09h

7	6	5	4	3	2	1	0
0	0	0	SPECIAL MODE1 CHD			ALIGN TEST PATTERN	DATA FORMAT

Table 19. Register 09h Description

Name	Description
Bits 7:5	Must write 0
Bits 4:2	SPECIAL MODE1 CHD
	010 = For frequencies < 120 MHz 111 = For frequencies > 120 MHz
Bit 1	ALIGN TEST PATTERN
	This bit aligns test patterns across the outputs of four channels. 0 = Test patterns of four channels are free running. 1 = Test patterns of four channels are aligned.
Bit 0	DATA FORMAT: Digital output data format
	0 = Twos complement 1 = Offset binary

Figure 174. Register 0Ah

7	6	5	4	3	2	1	0
CHA TEST PATTERN				CHB TEST PATTERN			

Table 20. Register 0Ah Description

Name	Description
Bits 7:4	CHA TEST PATTERN
	These bits control the test pattern for channel A after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095. 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 0110 = Deskew pattern: data are AAAh. 1000 = PRBS pattern: data are a sequence of pseudo random numbers. 1001 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, 599. Others = Do not use
Bits 3:0	CHB TEST PATTERN
	These bits control the test pattern for channel B after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095. 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 0110 = Deskew pattern: data are AAAh. 1000 = PRBS pattern: data are a sequence of pseudo random numbers. 1001 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, 599. Others = Do not use

Figure 175. Register 0Bh

7	6	5	4	3	2	1	0
CHC TEST PATTERN				CHD TEST PATTERN			

Table 21. Register 0Bh Description

Name	Description
Bits 7:4	CHC TEST PATTERN
	<p>These bits control the test pattern for channel C after the TEST PATTERN EN bit is set.</p> <p>0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095. 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 0110 = Deskew pattern: data are AAAh. 1000 = PRBS pattern: data are a sequence of pseudo random numbers. 1001 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, 599. Others = Do not use</p>
Bits 3:0	CHD TEST PATTERN
	<p>These bits control the test pattern for channel D after the TEST PATTERN EN bit is set.</p> <p>0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095. 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 0110 = Deskew pattern: data are AAAh. 1000 = PRBS pattern: data are a sequence of pseudo random numbers. 1001 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, 599. Others = Do not use</p>

Figure 176. Register 0Ch

7	6	5	4	3	2	1	0
CHA TEST PATTERN				CHB TEST PATTERN			

Table 22. Register 0Ch Description

Name	Description
Bits 7:4	CHA TEST PATTERN
	In address 0Ch, these bits control the test pattern for channel A after the CHA GAIN EN bit is set. See Table 23 for register settings.
Bits 3:0	CHB TEST PATTERN
	In address 0Ch, these bits control the test pattern for channel B after the CHB GAIN EN bit is set. See Table 23 for register settings.

Table 23. Channel Digital Gain

REGISTER VALUE	DIGITAL GAIN (dB)	MAXIMUM INPUT VOLTAGE (V _{PP})
0000	0	2.0
0001	0.5	1.89
0010	1	1.78
0011	1.5	1.68
0100	2	1.59
0101	2.5	1.50
0110	3	1.42
0111	3.5	1.34
1000	4	1.26
1001	4.5	1.19
1010	5	1.12
1011	5.5	1.06
1100	6	1.00

Figure 177. Register 0Dh

7	6	5	4	3	2	1	0
CHC TEST PATTERN				CHD TEST PATTERN			

Table 24. Register 0Dh Description

Name	Description
Bits 7:4	CHC TEST PATTERN
	In address 0Dh, these bits control the test pattern for channel C after the CHC GAIN EN bit is set. See Table 23 for register settings.
Bits 3:0	CHD TEST PATTERN
	In address 0Dh, these bits control the test pattern for channel D after the CHD GAIN EN bit is set. See Table 23 for register settings.

Figure 178. Register 0Eh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[11:4]							

Table 25. Register 0Eh Description

Name	Description
Bits 7:0	CUSTOM PATTERN[11:4]
	These bits set the 14-bit custom pattern (11:4) for all channels.

Figure 179. Register 0Fh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[3:0]				0	0	0	0

Table 26. Register 0Fh Description

Name	Description
Bits 7:2	CUSTOM PATTERN[3:0]
	These bits set the 14-bit custom pattern (3:0) for all channels.
Bits 3:0	Must write 0

Figure 180. Register 13h

7	6	5	4	3	2	1	0
LOW SPEED MODE	0	0	0	0	0	0	0

Table 27. Register 13h Description

Name	Description
Bit 7	LOW SPEED MODE
	Use this bit for sampling frequencies < 25 MSPS. 0 = Normal operation 1 = Low-speed mode enabled
Bits 6:0	Must write 0

Figure 181. Register 15h

7	6	5	4	3	2	1	0
CHA PDN	CHB PDN	CHC PDN	CHD PDN	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN

Table 28. Register 15h Description

Name	Description
Bit 7	CHA PDN: Power-down channel A
	0 = Normal operation 1 = Power-down channel A
Bit 6	CHB PDN: Power-down channel B
	0 = Normal operation 1 = Power-down channel B
Bit 5	CHC PDN: Power-down channel C
	0 = Normal operation 1 = Power-down channel C
Bit 4	CHD PDN: Power-down channel D
	0 = Normal operation 1 = Power-down channel D
Bit 3	STANDBY
	This bit places the ADCs of all four channels into standby. 0 = Normal operation 1 = Standby
Bit 2	GLOBAL PDN
	Places device in global power down. 0 = Normal operation 1 = Global power-down
Bit 1	Must write 0
Bit 0	CONFIG PDN PIN
	This bit configures the PDN pin as either global power-down or standby pin. 0 = Logic high voltage on the PDN pin sends places the into global power-down. 1 = Logic high voltage on the PDN pin places the device into standby.

Figure 182. Register 27h

7	6	5	4	3	2	1	0
CLK DIV		0	0	0	0	0	0

Table 29. Register 27h Description

Name	Description
Bits 7:6	CLK DIV: Internal clock divider for the input sampling clock
	00 = Clock divider bypassed 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4
Bits 5:0	Must write 0

Figure 183. Register 2Ah

7	6	5	4	3	2	1	0
SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK CONFIG DATA DIS

Table 30. Register 2Ah Description

Name	Description
Bits 7:6	SERDES TEST PATTERN: These bits set the test patterns in the transport layer of the JESD204B interface. 00 = Normal operation 01 = Outputs clock pattern (output is 10101010) 10 = Encoded pattern (output is 1111111100000000) 11 = Output is $2^{15} - 1$
Bit 5	IDLE SYNC This bit generates the long transport layer test pattern mode according to 5.1.6.3 clause of JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
Bit 4	TESTMODE EN This bit sets the output pattern when SYNC is high. 0 = Sync code is k28.5 (0xBCBC) 1 = Sync code is 0xBC50
Bit 3	FLIP ADC DATA This bit sets the output pattern when SYNC is high. 0 = Normal operation 1 = Output data order is reversed: MSB – LSB
Bit 2	LANE ALIGN This bit inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
Bit 1	FRAME ALIGN This bit inserts a frame alignment character (K28.7) for the receiver to align to the frame boundary per section 5.3.3.4 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
Bit 0	TX LINK CONFIG DATA DIS This bit disables the initial link alignment (ILA) sequence when SYNC is de-asserted. 0 = Normal operation 1 = ILA disabled

Figure 184. Register 2Bh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTRL K	CTRL F

Table 31. Register 2Bh Description

Name	Description
Bits 7:2	Must write 0
Bit 1	CTRL K: Enable bit for number of frames per multiframe 0 = Default is 9 frames (20x mode) per multiframe 1 = Frames per multiframe can be set in register 31h
Bit 0	CTRL F: Enable bit for number of octets per frame 0 = 20x mode using one lane per ADC (default is F = 2) 1 = Octets per frame can be specified in register 30h

Figure 185. Register 2Fh

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0

Table 32. Register 2Fh Description

Name	Description
Bit 7	SCRAMBLE EN
	This bit scrambles the enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled
Bits 6:0	Must write 0

Figure 186. Register 30h

7	6	5	4	3	2	1	0
OCTETS PER FRAME							

Table 33. Register 30h Description

Name	Description
Bits 7:0	OCTETS PER FRAME
	These bits set the number of octets per frame (F). 01 = 20x serialization: two octets per frame 11 = 40x serialization: four octets per frame

Figure 187. Register 31h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTI FRAME				

Table 34. Register 31h Description

Name	Description
Bits 7:5	Must write 0
Bits 4:0	FRAMES PER MULT IFRAME
	These bits set the number of frames per multiframe. After reset, the default settings for frames per multiframe are: 20x mode: K = 8 (for each mode, K should not be set to a lower value).

Figure 188. Register 34h

7	6	5	4	3	2	1	0
SUBCLASS			0	0	0	0	0

Table 35. Register 34h Description

Name	Description
Bits 7:5	SUBCLASS
	These bits set the JESD204B subclass. 000 = Subclass 0 (backward compatibility with JESD204A) 001 = Subclass 1 (deterministic latency using SYSREF signal) 010 = Subclass 2 (deterministic latency using SYNC detection)
Bits 4:0	Must write 0

Figure 189. Register 3Ah

7	6	5	4	3	2	1	0
SYNC REQ	SYNC REQ EN	0	0	OUTPUT CURRENT SEL			

Table 36. Register 3Ah Description

Name	Description
Bit 7	SYNC REQ
	This bit generates a synchronization request only when the SYNC REQ EN register bit is set. 0 = Normal operation 1 = Generates sync request
Bit 6	SYNC REQ EN
	0 = Sync request is made with the SYNCP~, SYNCM~ pins 1 = Sync request is made with the SYNC REQ register bit
Bits 5:4	Must write 0
Bits 3:0	OUTPUT CURRENT SEL: JESD output buffer current selection
	Program current (mA)
	100 = 32
	000 = 16
	101 = 28
	001 = 12
	110 = 24
	010 = 8
	111 = 20
	011 = 4

Figure 190. Register 3Bh

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		

Table 37. Register 3Bh Description

Name	Description
Bits 7:5	LINK LAYER TESTMODE
	These bits generate a pattern according to clause 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high frequency jitter pattern) 010 = K28.5 (mixed frequency jitter pattern) 011 = Repeat initial lane alignment (generates K28.5 character and repeat lane alignment sequences continuously) 100 = 12 octet RPAT jitter pattern
Bit 4	LINK LAYER RPAT
	This bit changes the running disparity in the modified RPAT pattern test mode (only when link layer test mode = 100). 0 = normal operation 1 = changes disparity
Bit 3	Must write 0
Bits 2:0	PULSE DET MODES
	These bits select different detection modes for SYSREF (subclass 1) and SYNC (subclass2).

Table 38. PULSE DET MODES Register Settings

D2	D1	D0	FUNCTIONALITY
0	Don't care	0	Allow all pulses to reset input clock dividers
1	Don't care	0	Do not allow reset of analog clock dividers
Don't care	0 to 1 transition	1	Allow one pulse immediately after the 0 to 1 transition to reset the divider

Figure 191. Register 3Ch

7	6	5	4	3	2	1	0
FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	

Table 39. Register 3Ch Description

Name	Description
Bit 7	FORCE LMFC COUNT: Force LMFC count
	0 = Normal operation 1 = Enables using different starting values for the LMFC counter
Bits 6:2	LMFC COUNT INIT
	If SYSREF is transmitted to the digital block, the LMFC count resets to 0 and K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the Rx can be synchronized early because the Rx receives the LANE ALIGNMENT SEQUENCE early. The FORCE LMFC COUNT register bit must be enabled.
Bits 1:0	RELEASE ILANE SEQ
	These bits delay the lane alignment sequence generation by 0, 1, 2, or 3 multiframe after the code group synchronization. 00 = 0 01 = 1 10 = 2 11 = 3

Figure 192. Register 122h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPECIAL MODE2 CHA [1:0]	

Table 40. Register 122h Description

Name	Description
Bits 7:2	Must write 0
Bit 1:0	SPECIAL MODE2 CHA [1:0]
	Always write '11' for better HD2 performance.

Figure 193. Register 134h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0

Table 41. Register 134h Description

Name	Description
Bits 7:6	Must write 0
Bit 5	DIS DITH CHA
	00 = Default 11 = Dither is disabled and high SNR mode is selected for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz. Ensure that register 01h (bits 7:6) are also set to 11.
Bit 4	Must write 0
Bit 3	DIS DITH CHA
	00 = Default 11 = Dither is disabled and high SNR mode is selected for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz. Ensure that register 01h (bits 7:6) are also set to 11.
Bits 2:0	Must write 0

Figure 194. Register 222h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPECIAL MODE 2 CHD [1:0]	

Table 42. Register 222h Description

Name	Description
Bits 7:2	Must write 0
Bit 1:0	SPECIAL MODE 2 CHD [1:0]
	Always write '11' for better HD2 performance.

Figure 195. Register 234h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0

Table 43. Register 234h Description

Name	Description
Bits 7:6	Must write 0
Bit 5	DIS DITH CHD
	00 = Default 11 = Dither is disabled and high SNR mode is selected for channel D. In this mode, SNR typically improves by 0.5 dB at 70 MHz. Ensure that register 01h (bits 1:0) are also set to 11.
Bit 4	Must write 0
Bit 3	DIS DITH CHD
	00 = Default 11 = Dither is disabled and high SNR mode is selected for channel D. In this mode, SNR typically improves by 0.5 dB at 70 MHz. Ensure that register 01h (bits 1:0) are also set to 11.
Bits 2:0	Must write 0

Figure 196. Register 422h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPECIAL MODE 2 CHB [1:0]	

Table 44. Register 422h Description

Name	Description
Bits 7:2	Must write 0
Bit 1:0	SPECIAL MODE 2 CHB [1:0]
	Always write '11' for better HD2 performance.

Figure 197. Register 434h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0

Table 45. Register 434h Description

Name	Description
Bits 7:6	Must write 0
Bit 5	DIS DITH CHB
	00 = Default 11 = Dither is disabled and high SNR mode is selected for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz. Ensure that register 01h (bits 5:4) are also set to 11.
Bit 4	Must write 0
Bit 3	DIS DITH CHB
	00 = Default 11 = Dither is disabled and high SNR mode is selected for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz. Ensure that register 01h (bits 5:4) are also set to 11.
Bits 2:0	Must write 0

Figure 198. Register 522h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SPECIAL MODE 2 CHC [1:0]	

Table 46. Register 522h Description

Name	Description
Bits 7:2	Must write 0
Bit 1:0	SPECIAL MODE 2 CHC [1:0]
	Always write '11' for better HD2 performance.

Figure 199. Register 534h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0

Table 47. Register 534h Description

Name	Description
Bits 7:6	Must write 0
Bit 5	DIS DITH CHC
	00 = Default 11 = Dither is disabled and high SNR mode is selected for channel C. In this mode, SNR typically improves by 0.5 dB at 70 MHz. Ensure that register 01h (bits 3:2) are also set to 11.
Bit 4	Must write 0
Bit 3	DIS DITH CHC
	00 = Default 11 = Dither is disabled and high SNR mode is selected for channel C. In this mode, SNR typically improves by 0.5 dB at 70 MHz. Ensure that register 01h (bits 3:2) are also set to 11.
Bits 2:0	Must write 0

10 Application and Implementation

10.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. While designing the dc driving circuits, the ADC input impedance must be considered. Figure 200 and Figure 201 show the impedance ($Z_{in} = R_{in} \parallel C_{in}$) across the ADC input pins.

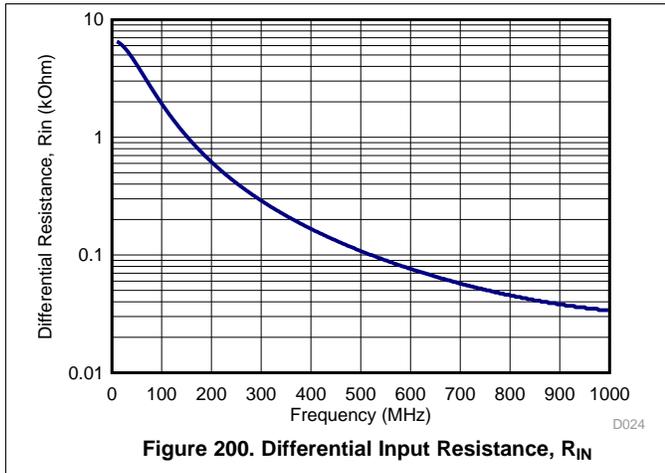


Figure 200. Differential Input Resistance, R_{IN}

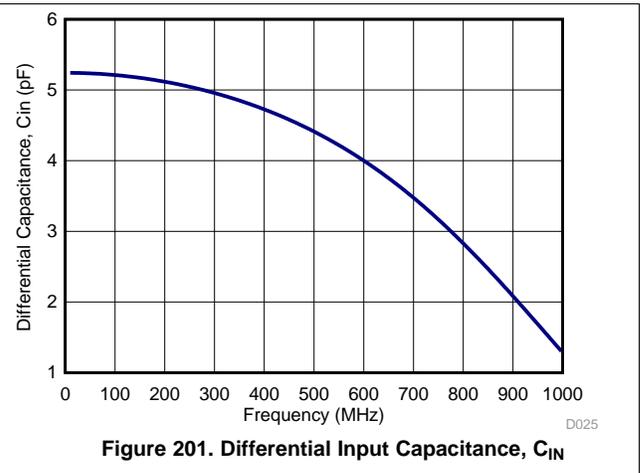


Figure 201. Differential Input Capacitance, C_{IN}

10.2 Typical Applications

10.2.1 Driving Circuit Design: Low Input Frequencies

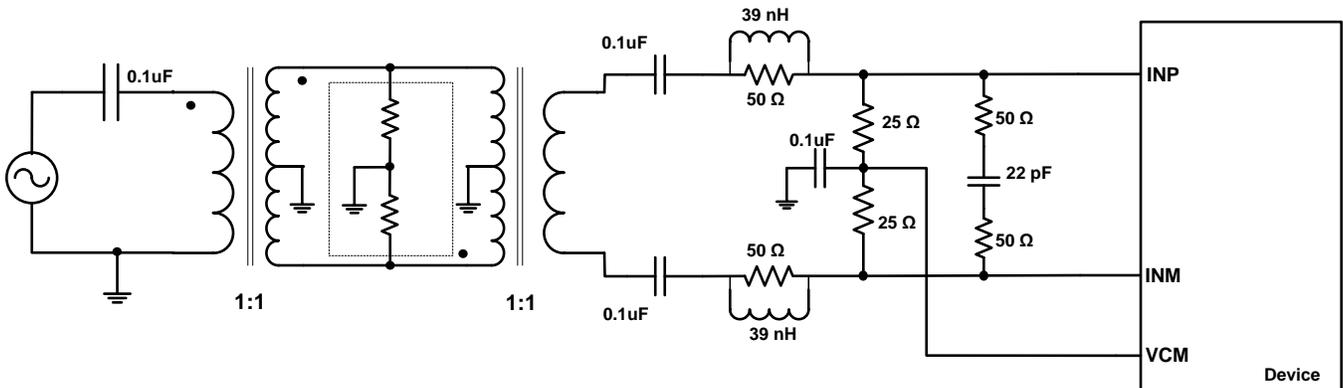


Figure 202. Driving Circuit for Low Input Frequencies

10.2.1.1 Design Requirements

For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitics. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

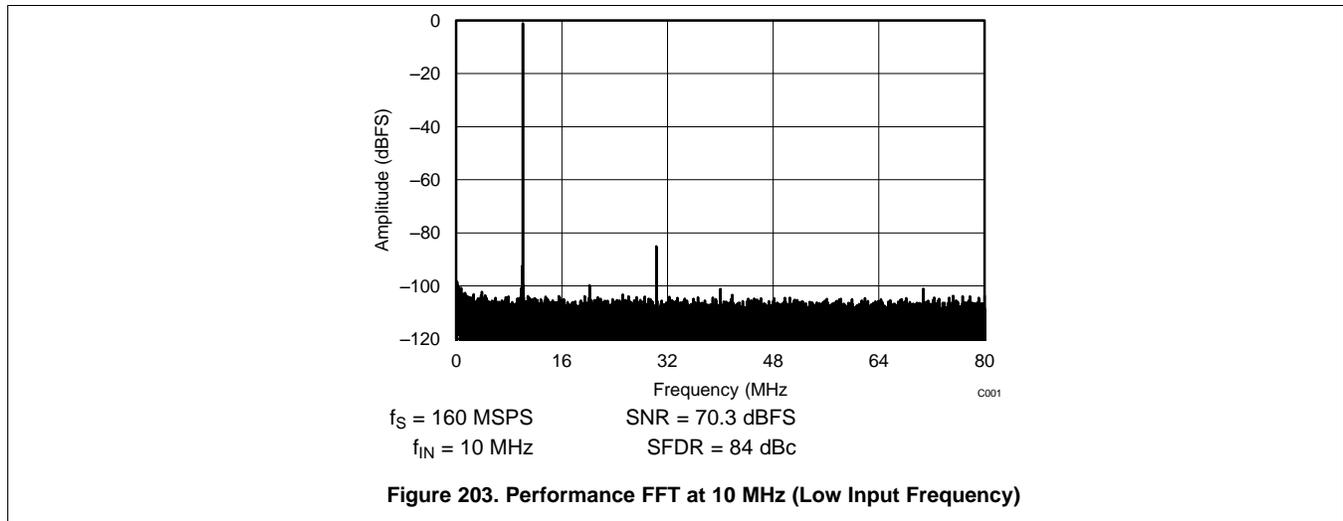
10.2.1.2 Detailed Design Procedure

A typical application using two back-to-back coupled transformers is illustrated in Figure 202. The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used. With the series inductor (39 nH), this combination helps absorb the sampling glitches.

Typical Applications (continued)

10.2.1.3 Application Curve

Figure 203 shows the performance obtained by using the circuit shown in Figure 202.



Typical Applications (continued)

10.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz

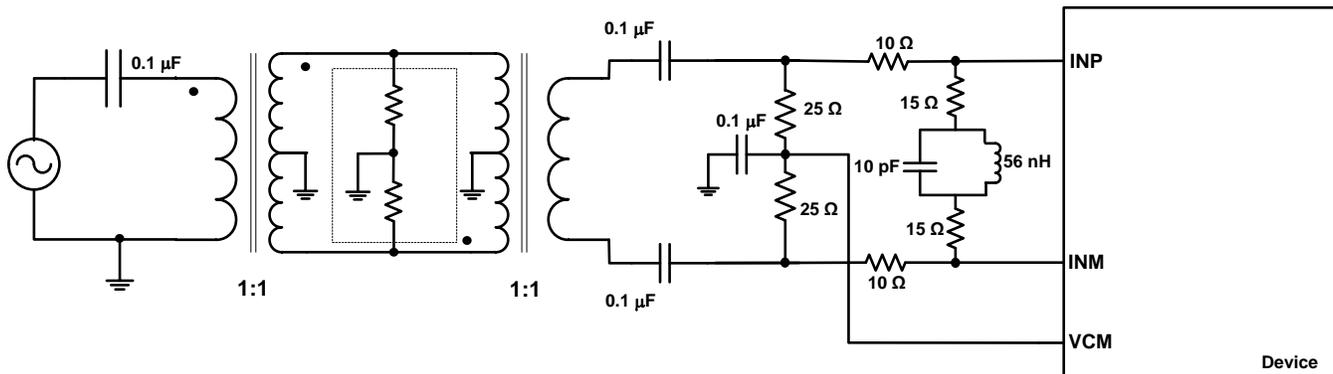


Figure 204. Driving Circuit for Mid-Range Input Frequencies ($100 \text{ MHz} < f_{IN} < 230 \text{ MHz}$)

10.2.2.1 Design Requirements

See the [Design Requirements](#) section for further details.

10.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in [Figure 204](#).

10.2.2.3 Application Curve

[Figure 205](#) shows the performance obtained by using the circuit shown in [Figure 204](#).

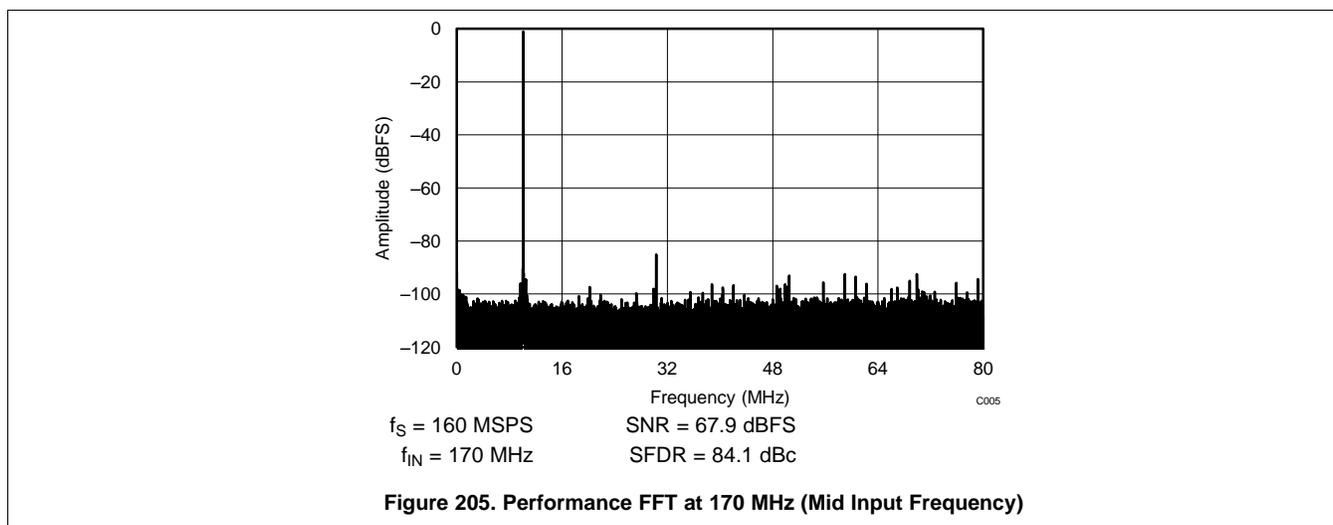


Figure 205. Performance FFT at 170 MHz (Mid Input Frequency)

Typical Applications (continued)

10.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

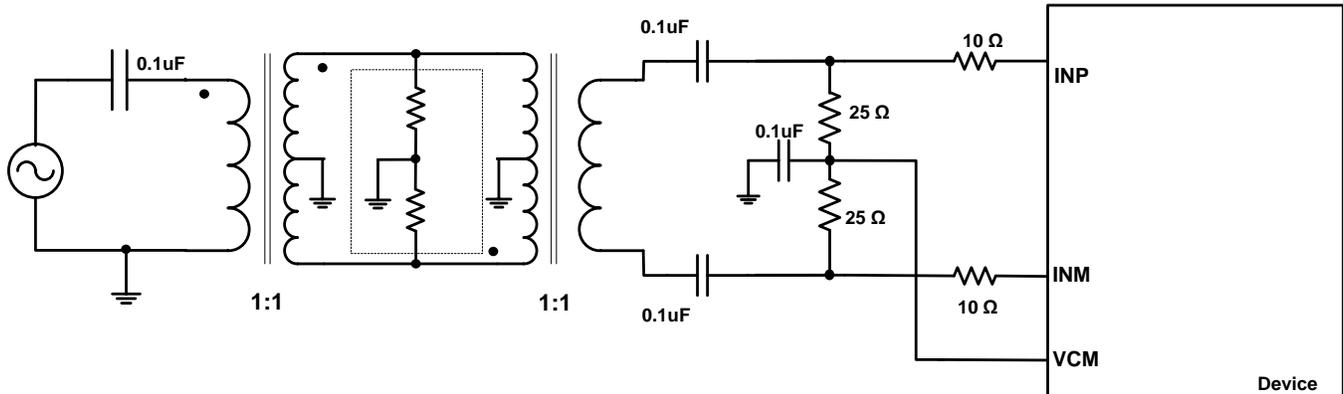


Figure 206. Driving Circuit for High Input Frequencies ($f_{IN} > 230$ MHz)

10.2.3.1 Design Requirements

See the [Design Requirements](#) section for further details.

10.2.3.2 Detailed Design Procedure

For high input frequencies (> 230 MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of 10Ω can be used as shown in [Figure 206](#).

10.2.3.3 Application Curve

[Figure 207](#) shows the performance obtained by using the circuit shown in [Figure 206](#).

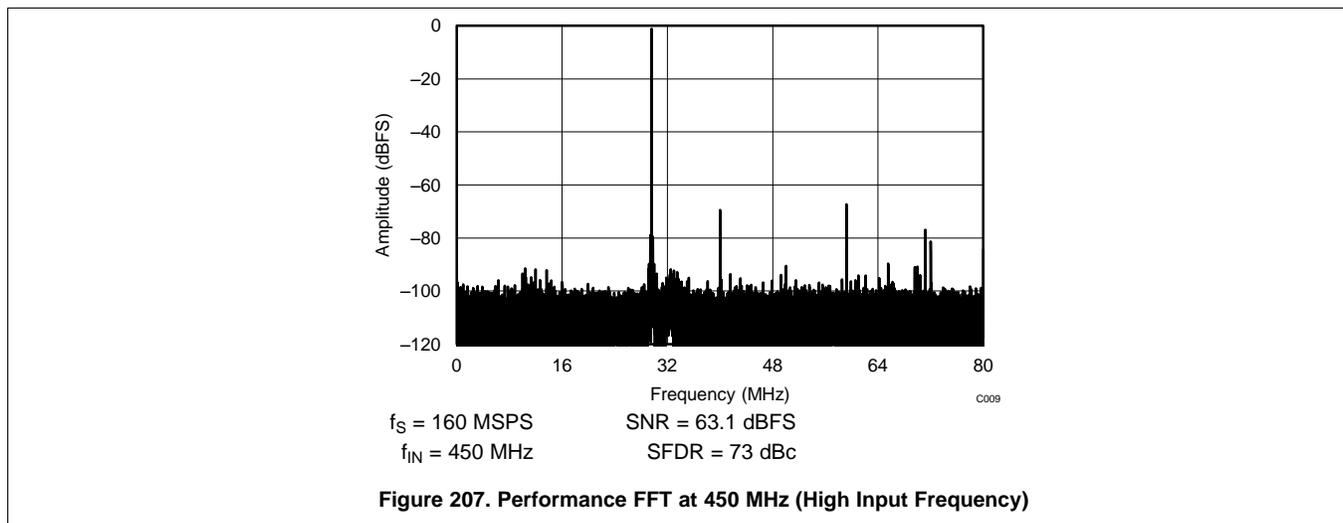


Figure 207. Performance FFT at 450 MHz (High Input Frequency)

11 Power-Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

12 Layout

12.1 Layout Guidelines

The ADC34J2x EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in [Figure 208](#). Some important points to remember while laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs should exit the pin out in opposite directions, as shown in the reference layout of [Figure 208](#) as much as possible.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of [Figure 208](#) as much as possible.
3. Digital outputs should be kept away from the analog inputs. When these digital outputs exit the pin out, the digital output traces should not be kept parallel to the analog input traces because this configuration may result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] should be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), a 0.1- μ F decoupling capacitor should be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10- μ F, 1- μ F, and 0.1- μ F capacitors can be kept close to the supply source.

12.2 Layout Example

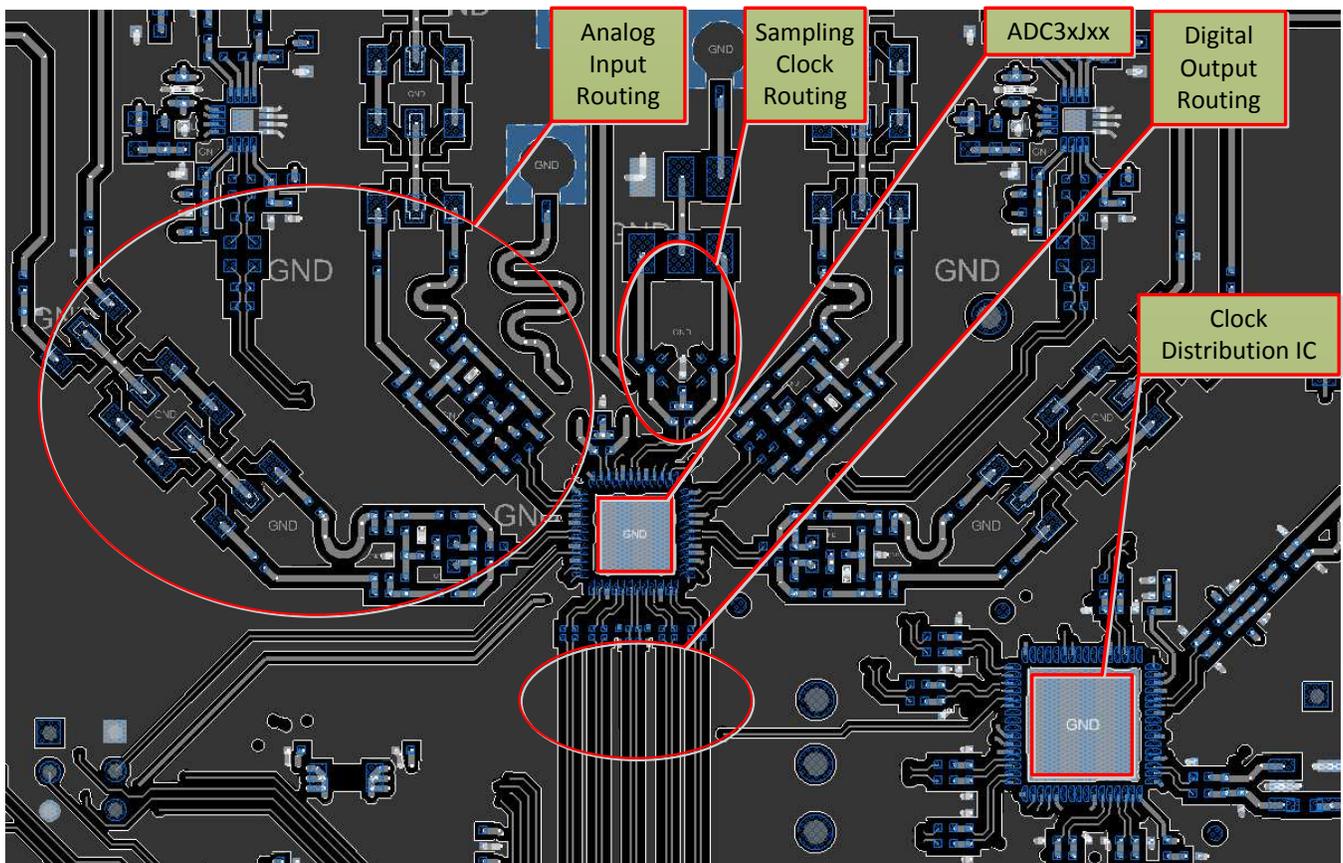


Figure 208. Typical Layout of the ADC34J2x Board

13 Device and Documentation Support

13.1 Related Links

[Table 48](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 48. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADC34J22	Click here				
ADC34J23	Click here				
ADC34J24	Click here				
ADC34J25	Click here				

13.2 Trademarks

PowerPAD is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC34J22IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34J22	Samples
ADC34J22IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34J22	Samples
ADC34J23IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34J23	Samples
ADC34J23IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34J23	Samples
ADC34J24IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34J24	Samples
ADC34J24IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34J24	Samples
ADC34J25IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34J25	Samples
ADC34J25IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ34J25	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

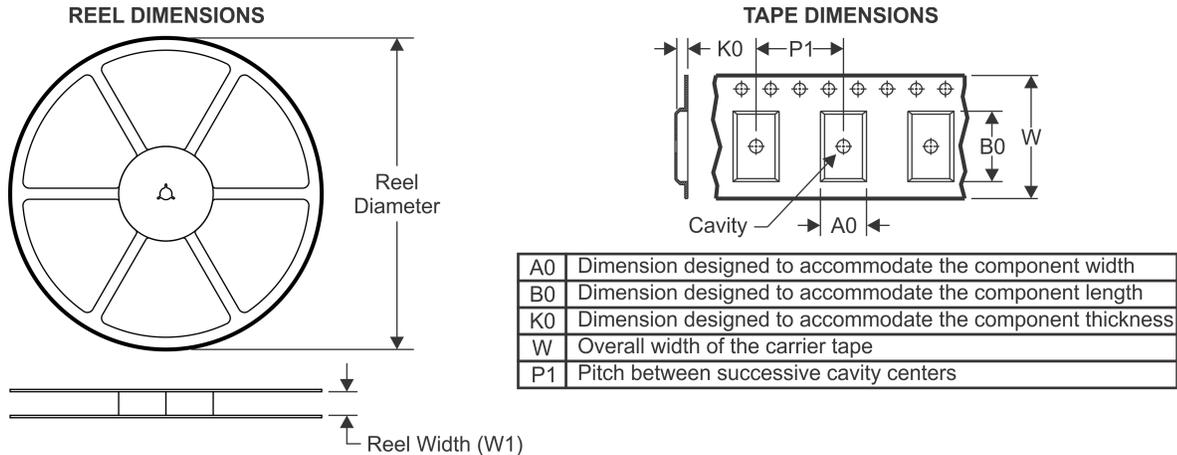
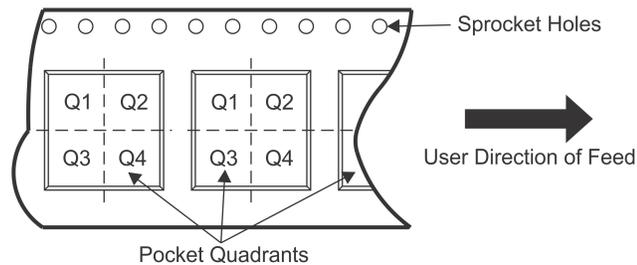
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

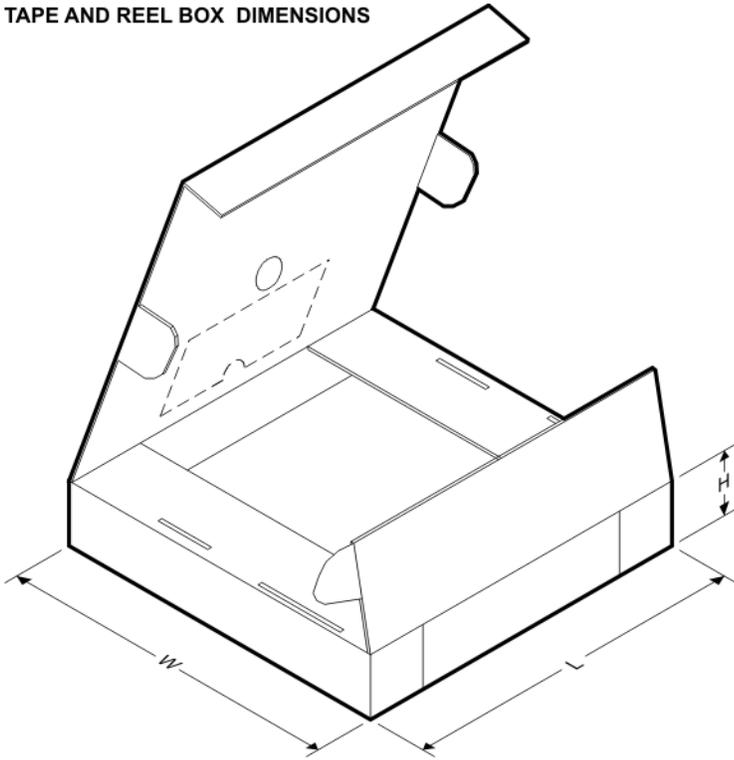
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC34J22IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC34J22IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC34J23IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC34J23IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC34J24IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC34J24IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC34J25IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADC34J25IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC34J22IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADC34J22IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADC34J23IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADC34J23IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADC34J24IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADC34J24IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADC34J25IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0
ADC34J25IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

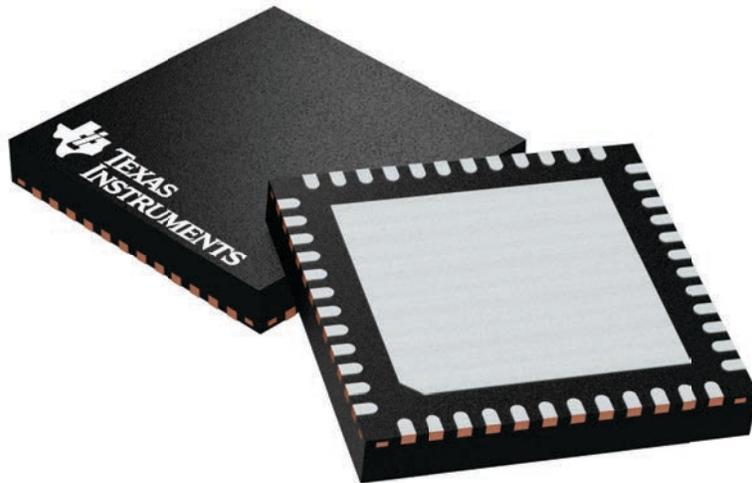
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

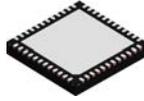
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

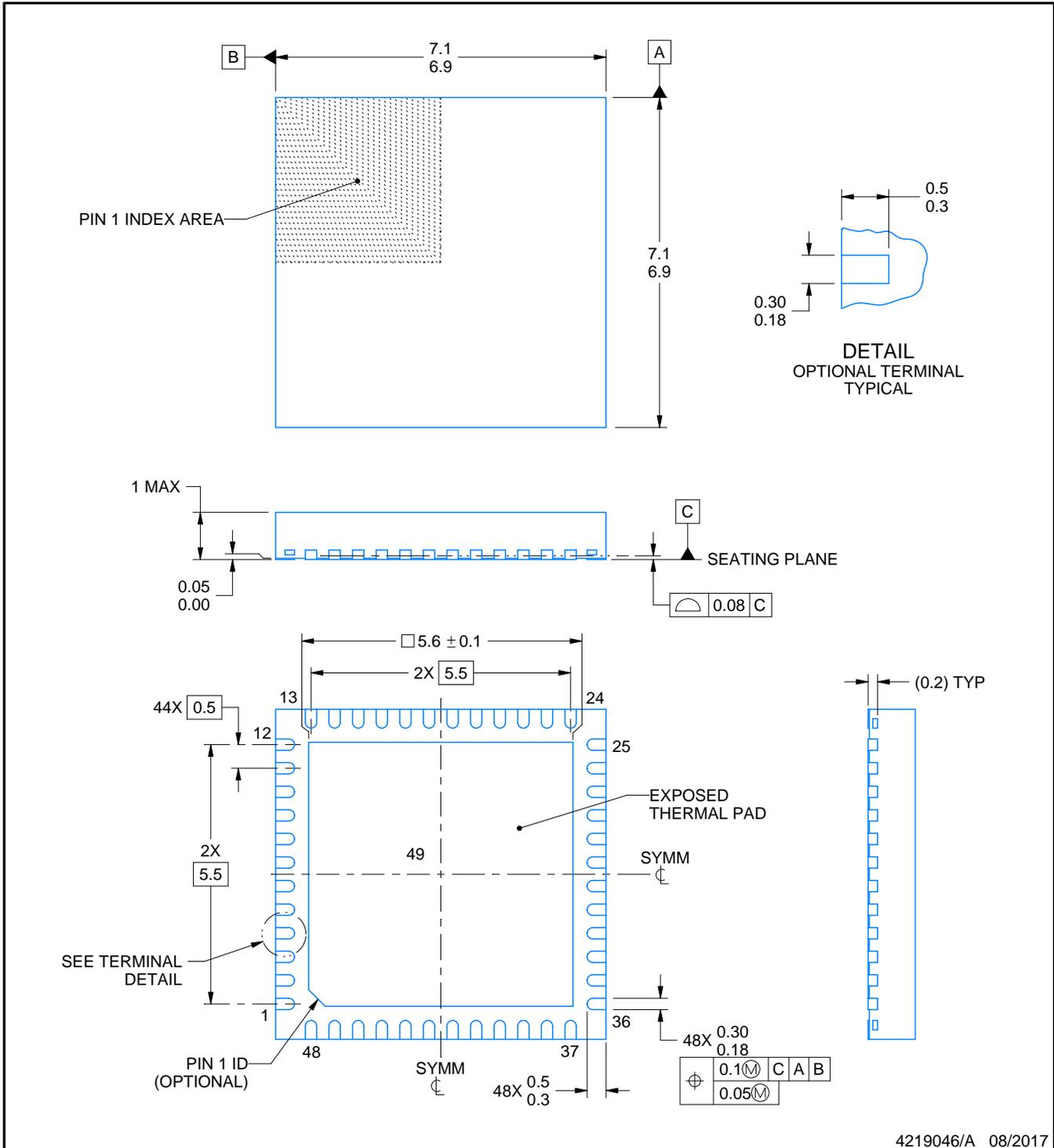
RGZ0048D



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219046/A 08/2017

NOTES:

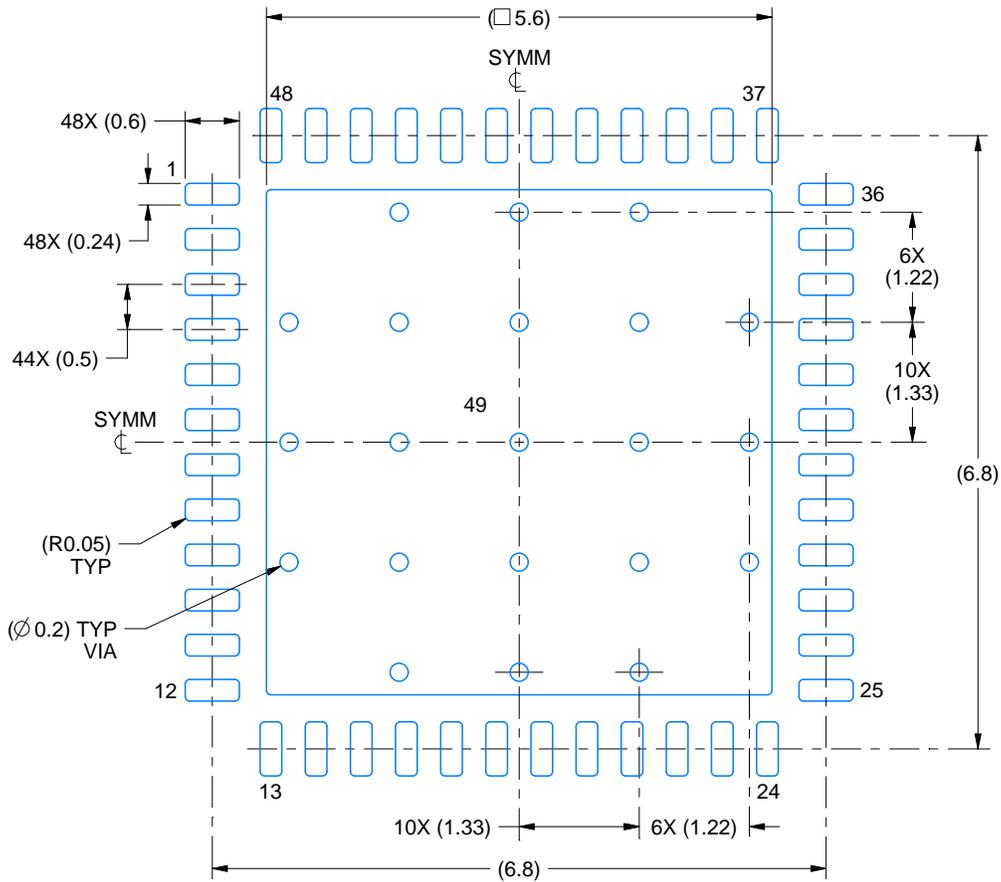
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

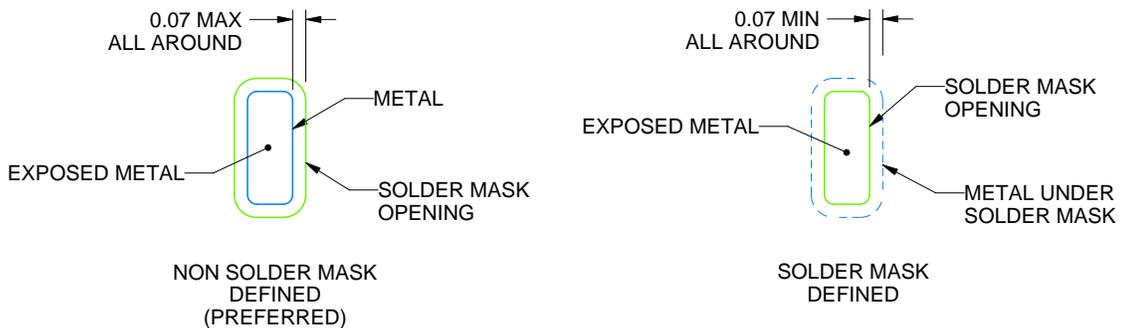
RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4219046/A 08/2017

NOTES: (continued)

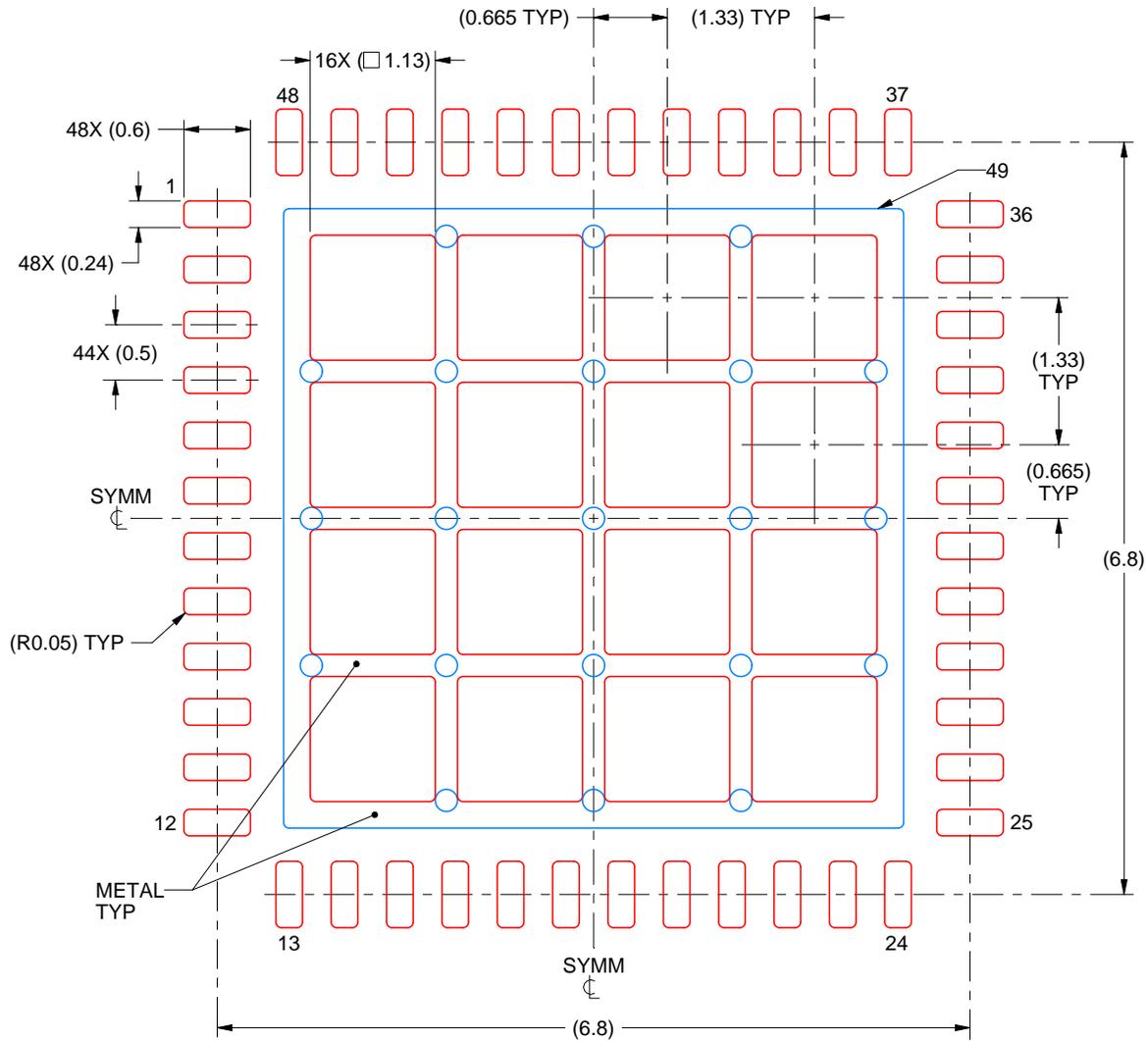
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
 66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:15X

4219046/A 08/2017

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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