ADVANCE INFORMATION

VCT 49xyI, VCT 48xyI

Video-Controller-Text-IF-Audio IC Family

Edition 12.12.2003
6251-573-1AI

MICRONAS

Contents

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

Contents, continued

ADVANCE INFORMATION

VCT 49xyl, VCT 48xyl

Volume 1:
General Description

Edition 12.12.2003
6251-573-1-1AI

MICRONAS

Contents

Contents, continued

General Description

Release Note: This data sheet describes functions and characteristics of the VCT 49xyI, VCT 48xyI-C4.

1. Introduction

The VCT 49xyI, VCT 48xyI is an IC family of high-quality single-chip TV processors. Modular design and deep-submicron technology allow the economic integration of features in all classes of single-scan TV sets. The VCT 49xyI, VCT 48xyI family is based on functional blocks contained and approved in existing products like DRX 396xA, MSP 34x5G, VSP 94x7B, DDP 3315C, and SDA 55xx.

Each member of the family contains the entire IF, audio, video, display, and deflection processing for 4:3 and 16:9 50/60-Hz mono and stereo TV sets. The integrated microcontroller is supported by a powerful OSD generator with integrated Teletext & CC acquisition including on-chip page memory.

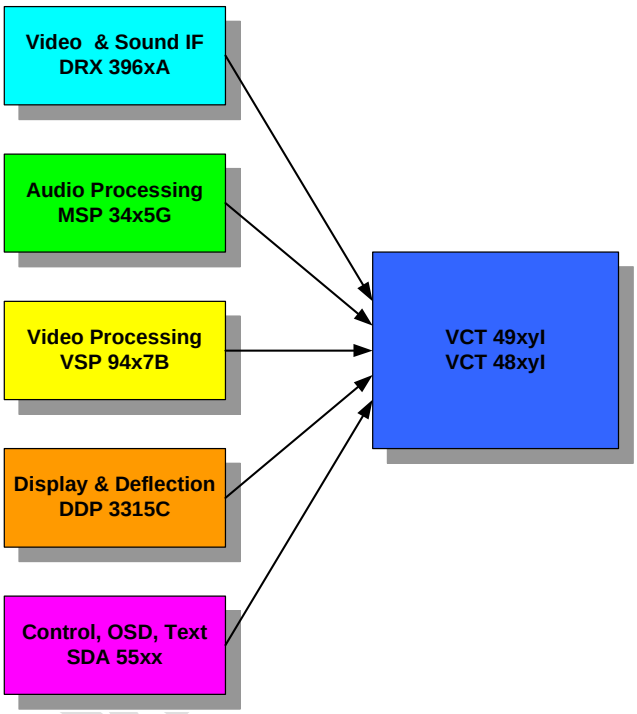


Fig. 1–1: Single-chip VCT 49xyI, VCT 48xyI

1.1. Features

The VCT 49xyI, VCT 48xyI family offers a rich feature set, covering the whole range of state-of-the-art 50/60 Hz TV applications.

- PSSDIP88-1/-2 package
- PMQFP144-2 package
- Submicron CMOS technology
- Low-power standby mode
- Single 20.25 MHz reference crystal
- 8-bit 8051 instruction set compatible CPU
- Up to 256 kB on-chip program ROM
- WST, PDC, VPS, and WSS acquisition
- Closed Caption and V-chip acquisition
- Up to 10 pages on-chip teletext memory
- Multi-standard QSS IF processing with single SAW
- FM Radio and RDS with standard TV tuner
- TV-sound demodulation:
  - all A2 standards
  - all NICAM standards
  - BTSC/SAP with MNR (DBX optional)
  - EIA-J
- Baseband sound processing for loudspeaker channel:
  - volume and balance
  - bass/treble or equalizer
  - loudness and spatial effect (e.g. pseudo stereo)
  - Micronas AROUND (virtual Dolby optional)
  - Micronas BASS and Subwoofer output
  - further optional and licence requiring sound enhancements as BBE, SRS Wow and Micronas VOICE
- CVBS, S-VHS, YC_rC_b and RGB inputs
- 4H adaptive comb filter (PAL/NTSC)
- multi-standard color decoder (PAL/NTSC/SECAM)
- Nonlinear horizontal scaling “panorama vision”
- Luma and chroma transient improvement (LTI, CTI)
- Non-linear color space enhancement (NCE)
- Dynamic black level expander (BLE)
- Scan velocity modulation output
- Soft start/stop of H-drive
- Vertical angle and bow correction
- Average and peak beam current limiter
- Nonlinear and dynamic EHT compensation
- Black switch off procedure (BSO)

Table 1–1: VCT 49xyI, VCT 48xyI Family

Typical TV Application:	Eco CRT								Basic CRT												Basic 16/9 CRT												LCD								Emu
Features in VCT49xy Versions:	4x21	4x22	4923	4924	4931	4932	4933	4934	4x41	4x42	4943	4944	4x46	4947	4948	4951	4952	4953	4954	4956	4957	4958	4962	4963	4964	4966	4967	4968	4972	4973	4974	4976	4977	4978	4982	4983	4986	4987	4992	4993	4996	4997	49xy
Global analog stereo decoder A2, EIA-J, BTSC (dbx), FM Radio + auto. stand. detect., STATUS-reg., auto. sound sel., fm-hdev		y	y			y	y			y	y		y	y			y	y		y	y		y	y		y	y		y	y		y	y		y	y	y	y	y	y	y	y
Radio Data System (RDS/RBDS)		y	y	y		y	y	y		y	y	y	y	y	y		y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
NICAM stereo decoder			y				y				y			y				y			y			y			y			y			y				y		y		y		y
Eco stereo feature pack bass, treble, loudness, balance, spatial effects, beeper		y	y	y		y	y	y		y	y	y	y	y	y		y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
Basic stereo feature pack Micronas BASS, subwoofer, Micronas AROUND virtual, equalizer		opt	opt	opt		opt	opt	opt		y	y	y	y	y	y		y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
Virtual Dolby Surround® (VDS)													y	y	y					y	y	y				y	y	y				y	y	y			y	y			y	y	y
Micronas VOICE		opt	opt	opt		opt	opt	opt		opt	opt	opt	opt	opt	opt		opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt
SRS® (3D-Audio)		opt	opt	opt		opt	opt	opt		opt	opt	opt	opt	opt	opt		opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt
SRS® TruBass		opt	opt	opt		opt	opt	opt		opt	opt	opt	opt	opt	opt		opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt
SRS® WOW (SRS&TruBass&Focus)		opt	opt	opt		opt	opt	opt		opt	opt	opt	opt	opt	opt		opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt
BBE™ (High Definition Sound)		opt	opt	opt		opt	opt	opt		opt	opt	opt	opt	opt	opt		opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt	opt
4H adaptive comb filter									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
Panorama scaler																							y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
2nd RGB/YCrCb input									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
Softmix 2nd RGB via fastblank																							y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
CTI, LTI, histogram									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
Dynamic EHT compensation									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
Scan velocity modulation (SVM)									y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
Dynamic focus control																							y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y	y
ITU-656 Input or Output																																			y	y	y	y	y	y	y	y	y
Teletext, VPS, PDC, WSS					y	y	y	y								y	y	y	y	y	y	y							y	y	y	y	y	y					y	y	y	y	y
On-chip program memory	JE	JE	JE	JE	JE	JE	JE	JE	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG	IFG
Packages	PY PZ	PY PZ	PY PZ	PY PZ	PY PZ	PY PZ	PY PZ	PY PZ	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	PY PZ XM	XM	XM	XM	XM	XM	XM	XM	XM	XM
Memory/Package Definition:	ROM: J = 128 kB; I = 256 kB; Flash: E = 128 kB; F = 256 kB; G = 512 kB; PY = PSSDIP88-1; PZ = PSSDIP88-2 (mirrored); XM = PMQFP144-2;																																										
Common Features:																																										
IF Processing:	global alignment-free quasi split sound video and sound IF with single SAW, SIF-out (alternatively to AIN1_R)																																									
Audio Processing:	global mono audio, mono FM radio, standard selection, automatic volume control, volume, 1 speaker out PSSDIP88: 2/3 line in, 2/1 line out (switchable); PMQFP144: 3 line in, 2 line out , 4xy1 versions in PSSDIP88: 3 line in, 1 line out																																									
Color Decoder:	11 CVBS/YC/RGB/YCrCb inputs, 3 CVBS outputs, 1H NTSC comb filter, blackline detector 49xy: global color decoder; 48xy: NTSC only color decoder																																										
Video Processing:	contrast, saturation, tint, peaking, brightness, gamma, black and blue stretch, programmable RGB matrix																																									
Display Processing:	analog RGB inputs, cutoff and white balance control, beamcurrent limiter																																									
Deflection:	H, V and E/W deflection, H and V EHT compensation, soft start/stop, black switch off, angle and bow, protection circuit																																									
Controller:	CC, V-Chip, ROM, RAM, OSD, DAC, ADC, RTC, timer, watchdog, interrupt controller, UART, I2C bus, Flash version, patch modul																																									
Miscellaneous:	one crystal, few external components, alignment-free																																									

1.2. Chip Architecture

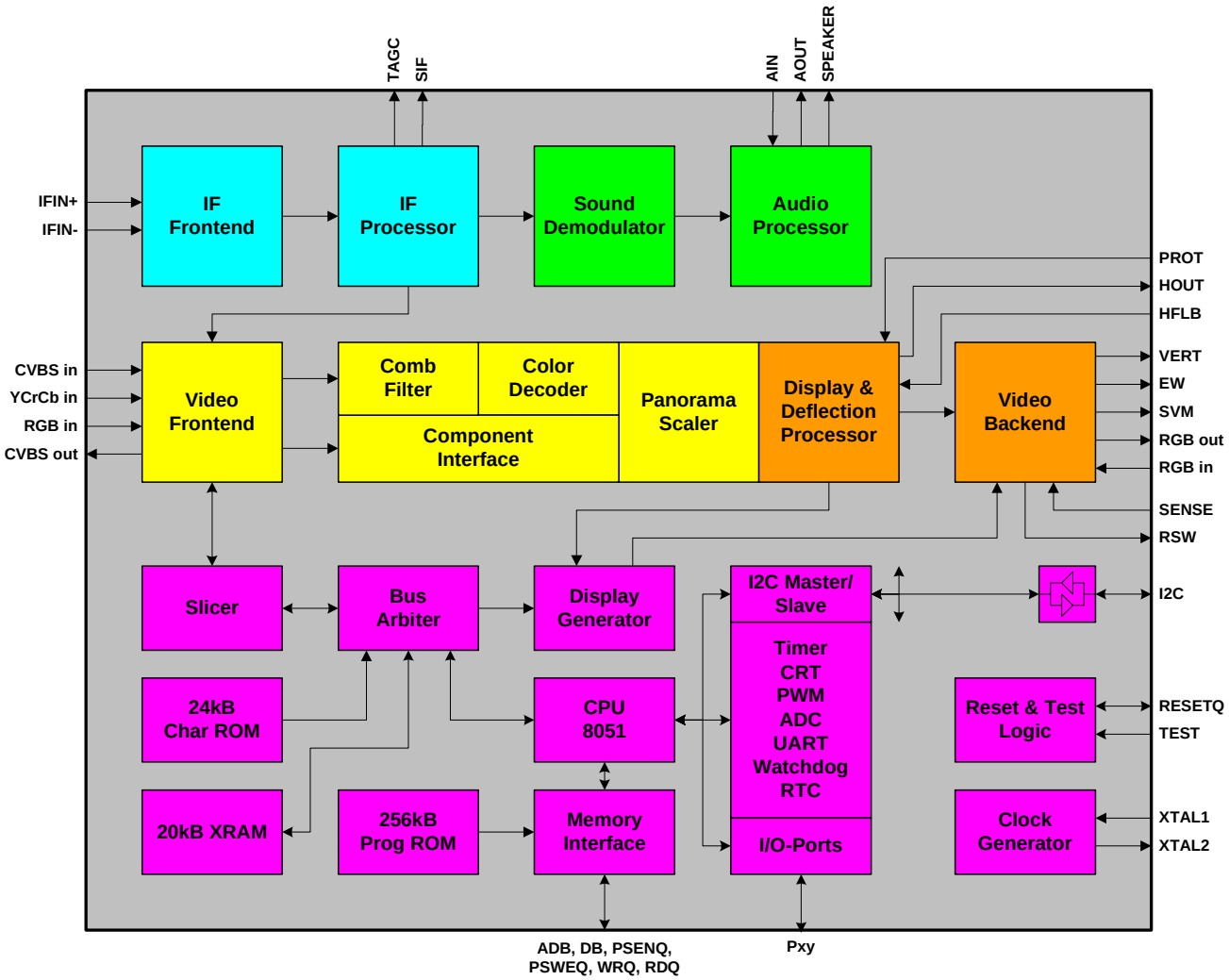


Fig. 1–2: Block diagram of the VCT 49xyl, VCT 48xyl

1.3. System Application

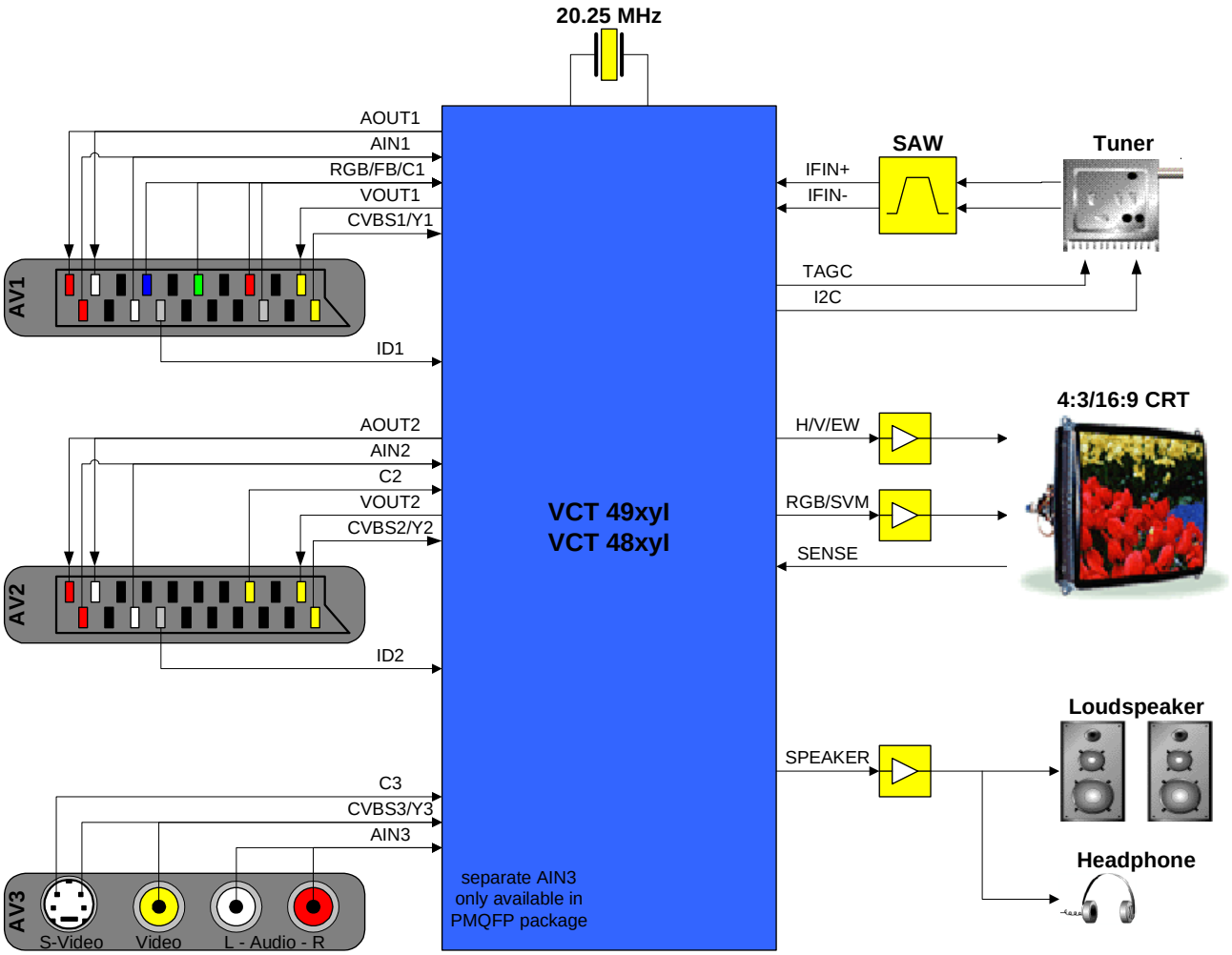


Fig. 1–3: Stereo TV set with VCT 49xyl, VCT 48xyl

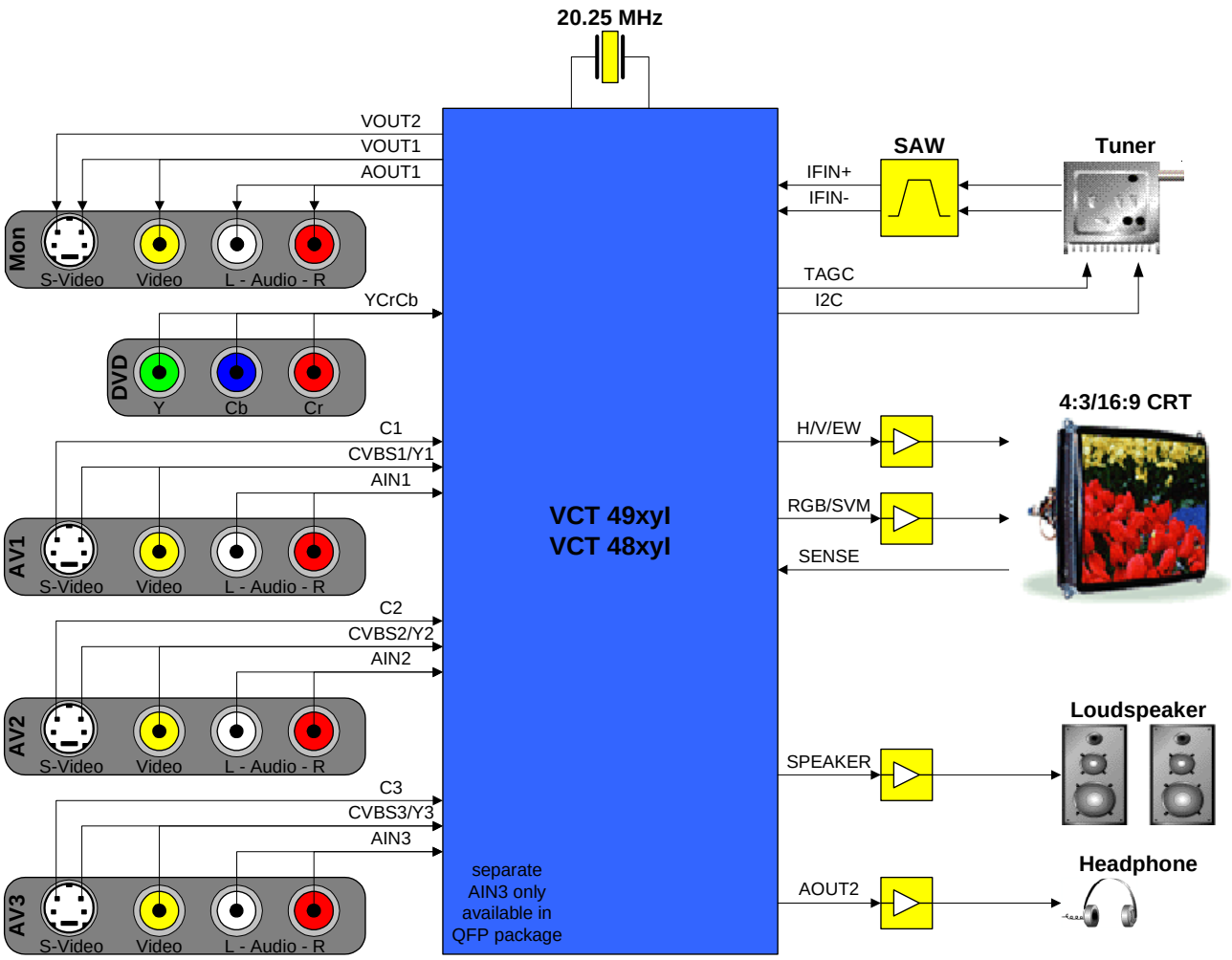


Fig. 1–4: Stereo TV set with VCT 49xyl, VCT 48xyl

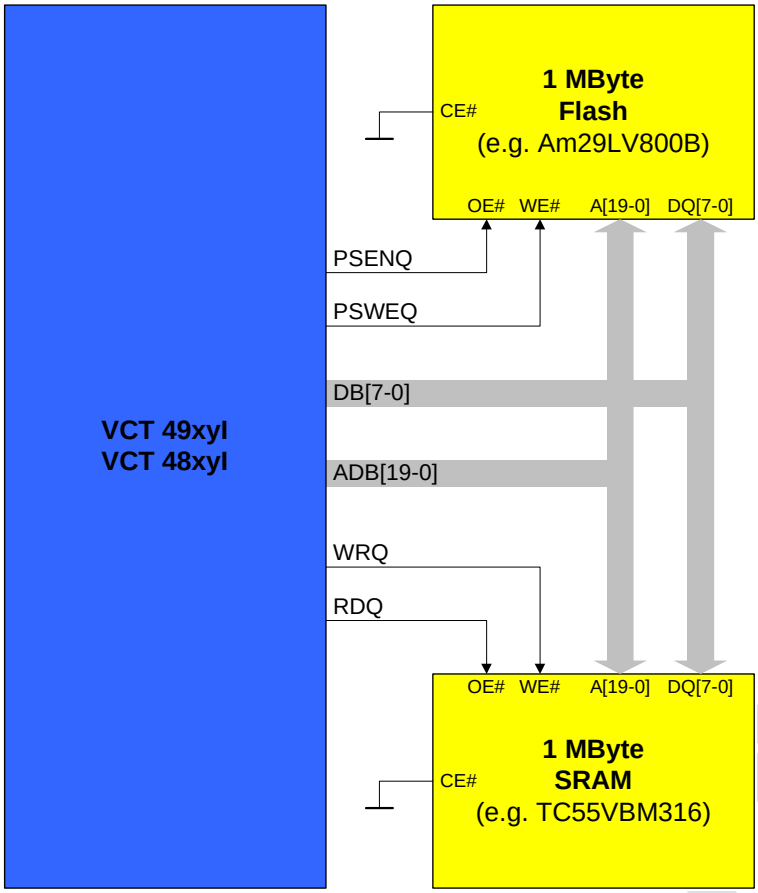


Fig. 1–5: VCT 49xyl, VCT 48xyl application with external program and teletext memory

2. Functional Description

The functional description of the VCT 49xyI, VCT 48xyI is split up into several volumes:

2.1. VCTI

Volume 1: General Description (this document)

2.2. DRX

Volume 2: DRX - Analog TV IF- Demodulator

2.3. MSP

Volume 3: Multistandard Sound Processor

2.4. VSP

Volume 4: Video Processor

2.5. DDP

Volume 5: Display and Deflection Processor

2.6. TVT

Volume 6: Controller, OSD and Text Processing

3. Control Interface

Table 3–1: I2C Slave Device Addresses

Block	8-bit Device Address	
	Write	**Read**
DRX	h'8E	h'8F
MSP	h'8C	h'8D
VSP	h'B0	h'B1
DDP	h'BC	h'BD
TVT	h'D0	h'D1
	programmable via SFR	

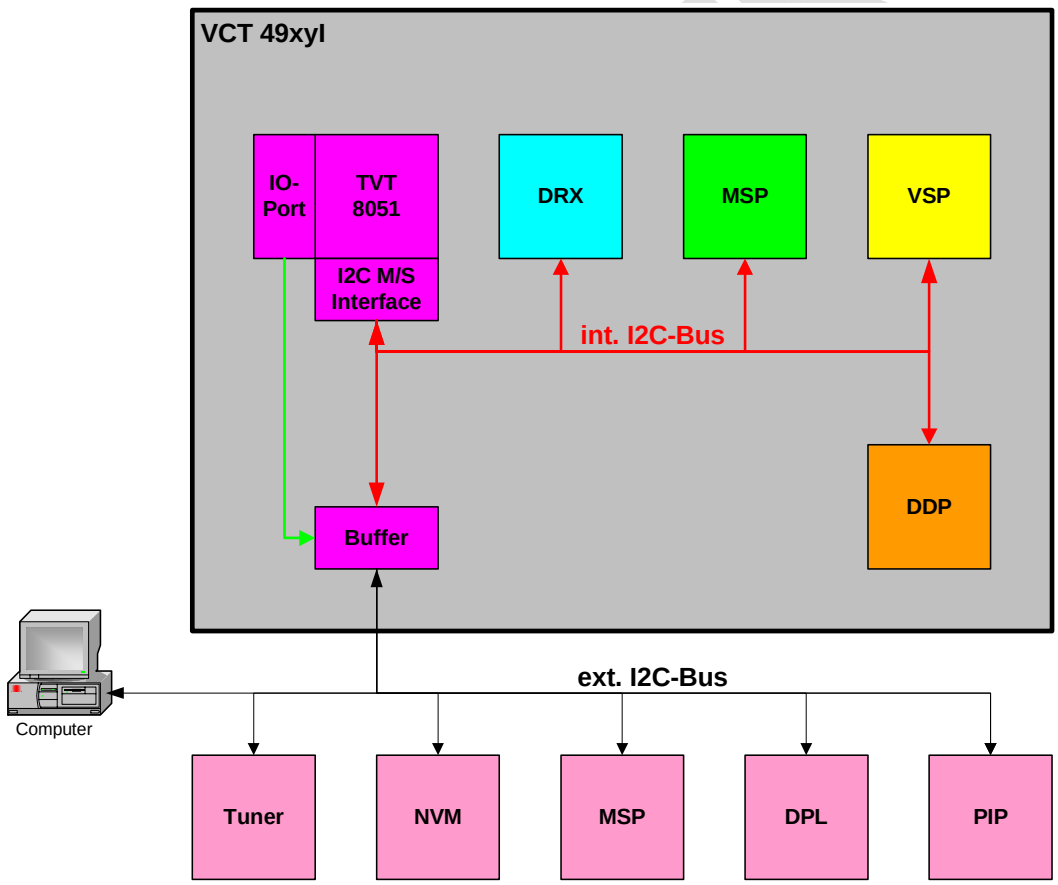
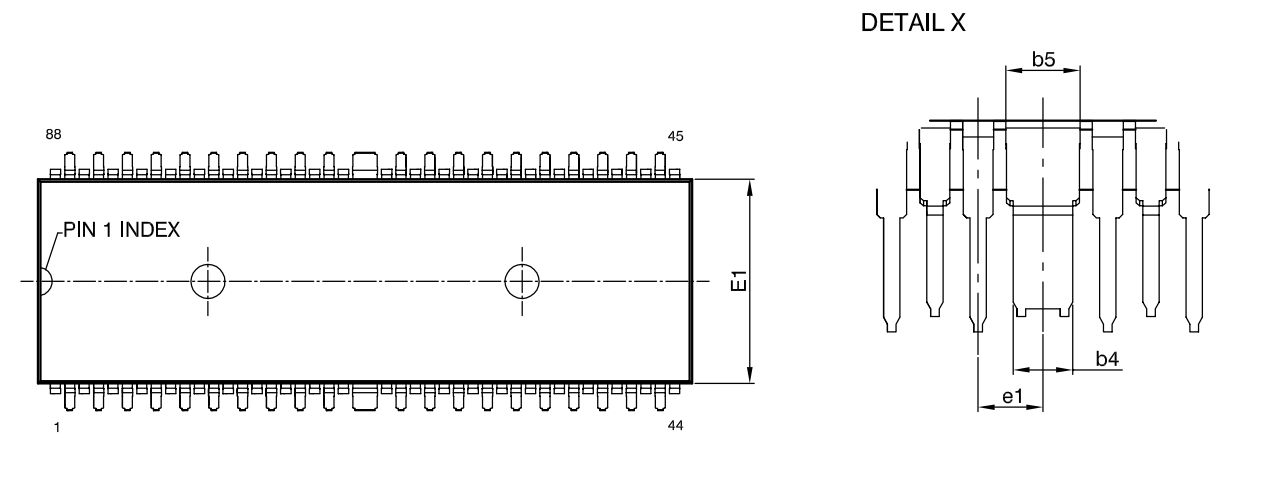
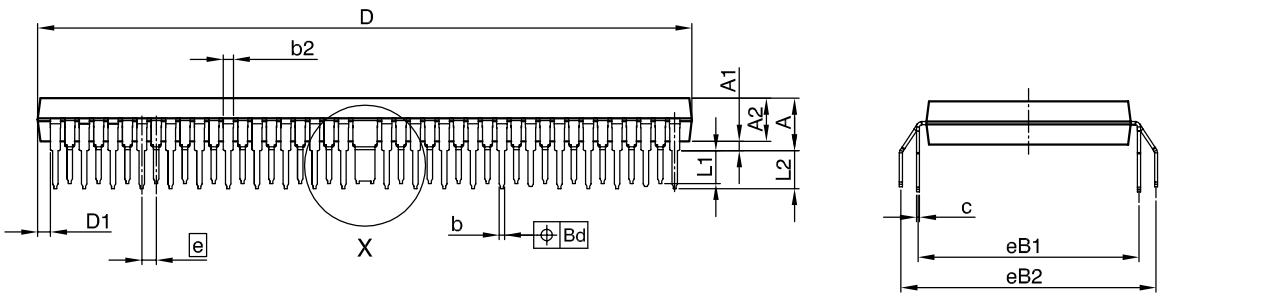


Fig. 3–1: I^2C Environment

4. Specifications

4.1. Outline Dimensions





UNIT	eB2	L1 min	L2 min
mm	22.8 22.2	2.8	3.2

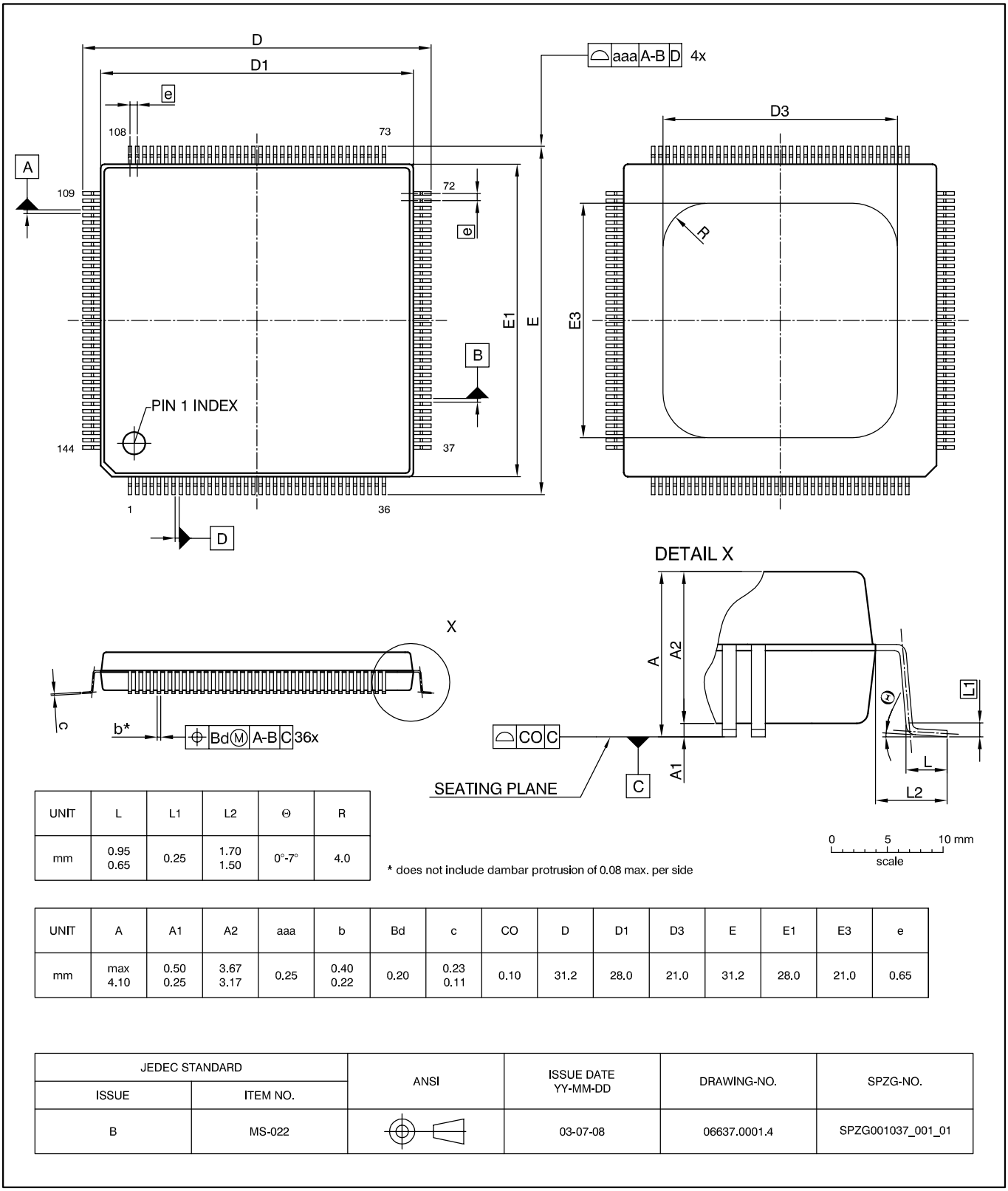
PY Package: Pin 1 Index molded
PZ Package: Pin 1 Index lasered

0 10 20 mm
scale

UNIT	A max	A1 min	A2 max	b	b2	b4	b5	Bd	c	D	D1	E1	e	e1	eB1
mm	4.9	0.5	3.9	0.6 0.4	0.95 0.80	1.85 1.65	2.3 2.1	0.25	0.35 0.20	57.8 57.6	1.21 1.01	18.1 17.9	1.27	1.91	19.8 19.2

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
A	MS-021		03-06-16	06633.0001.4	SPZG001033_001_01

Fig. 4–1:
PSSDIP88-1: Plastic **S**taggered **S**hrink **D**ual **I**n-line **P**ackage, **88** leads, 750 mil
Ordering code: PY or PZ
Weight approximately 9.46 g



UNIT	L	L1	L2	Θ	R
mm	0.95 0.65	0.25	1.70 1.50	0°-7°	4.0

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	D3	E	E1	E3	e
mm	max 4.10	0.50 0.25	3.67 3.17	0.25	0.40 0.22	0.20	0.23 0.11	0.10	31.2	28.0	21.0	31.2	28.0	21.0	0.65

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-07-08	06637.0001.4	SPZG001037_001_01

Fig. 4–2:
PMQFP144-2: Plastic **M**etric **Q**uad **F**lat **P**ackage, **144** leads, $28 \times 28 \times 3.4$ mm^3, 21×21 mm^2 heat slug
Ordering code: XM
Weight approximately 10.1 g

4.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
IN = Input Pin
OUT = Output Pin
SUPPLY = Supply Pin

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
1	88	128	GND	SUPPLY	OBL	Ground Platform
2	87	129	VSUP5.0BE	SUPPLY	OBL	Supply Voltage Analog Video Back-end, 5.0 V
3	86	130	TEST / SUBW	IN OUT	GND	Test Input, reserved for Test Subwoofer Output
4	85	131	VERT+	OUT	GND	Differential Vertical Sawtooth Output
5	84	132	VERT-	OUT	GND	Differential Vertical Sawtooth Output
6	83	133	EW	OUT	GND	Vertical Parabola Output
7	82	134	RSW2	OUT	LV	Range Switch 2 Output
8	81	135	RSW1	OUT	LV	Range Switch 1 Output
9	80	136	SENSE	IN	GND	Sense ADC Input
10	79	137	GNDM	IN	GND	Reference Ground for Sense ADC
11	78	138	FBIN	IN	GND	Fast Blank Input, Back-end
12	77	139	RIN	IN	GND	Analog Red Input, Back-end
13	76	140	GIN	IN	GND	Analog Green Input, Back-end
14	75	141	BIN	IN	GND	Analog Blue Input, Back-end
15	74	142	SVMOUT	OUT	VSUP5.0BE	Scan Velocity Modulation Output
16	73	143	ROUT	OUT	VSUP5.0BE	Analog Red Output
17	72	144	GOUT	OUT	VSUP5.0BE	Analog Green Output
18	71	1	BOUT	OUT	VSUP5.0BE	Analog Blue Output
19	70	2	VRD		OBL	Reference Voltage for RGB DACs
20	69	3	XREF		OBL	Reference Current for RGB DACs
21	68	4	VSUP3.3BE	SUPPLY	OBL	Supply Voltage Analog Video Back-end, 3.3 V
22	67	5	GND	SUPPLY	OBL	Ground Platform
23	66	6	GND	SUPPLY	OBL	Ground Platform
24	65	7	VSUP3.3IO	SUPPLY	OBL	Supply Voltage I/O Ports, 3.3 V
25	64	8	VSUP3.3DAC	SUPPLY	OBL	Supply Voltage Video DACs, 3.3 V
26	63	9	GNDDAC	SUPPLY	OBL	Ground Video DACs
27	62	10	SAFETY	IN	GND	Safety Input

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
28	61	11	HFLB	IN	HOUT	Horizontal Flyback Input
29	60	12	HOUT	OUT	LV	Horizontal Drive Output
30	59	13	VPROT	IN	GND	Vertical Protection Input
–	–	37	PWMV	OUT	LV	PWM Vertical Output
–	–	38	DFVBL	OUT	LV	Dynamic Focus Vertical Blanking Output
31	58	39	SDA	IN/OUT	OBL	I^2C Bus Data Input/Output
32	57	40	SCL	IN/OUT	OBL	I^2C Bus Clock Input/Output
33	56	41	P21	IN/OUT	LV	Port 2, Bit 1 Input/Output
34	55	42	P20	IN/OUT	LV	Port 2, Bit 0 Input/Output
35	54	43	P17	IN/OUT	LV	Port 1, Bit 7 Input/Output
36	53	44	P16	IN/OUT	LV	Port 1, Bit 6 Input/Output
37	52	45	P15	IN/OUT	LV	Port 1, Bit 5 Input/Output
38	51	46	P14	IN/OUT	LV	Port 1, Bit 4 Input/Output
39	50	47	P13	IN/OUT	LV	Port 1, Bit 3 Input/Output
40	49	48	P12	IN/OUT	LV	Port 1, Bit 2 Input/Output
41	48	49	P11	IN/OUT	LV	Port 1, Bit 1 Input/Output
42	47	50	P10	IN/OUT	LV	Port 1, Bit 0 Input/Output
43	46	53	VSUP3.3FE	SUPPLY	OBL	Supply Voltage Analog Video Front-end, 3.3 V
44	45	54	GND	SUPPLY	OBL	Ground Platform
45	44	55	GND	SUPPLY	OBL	Ground Platform
46	43	56	VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Front-end, 1.8 V
47	42	57	VOUT3	OUT	LV	Analog Video 3 Output
48	41	58	VOUT2	OUT	LV	Analog Video 2 Output
49	40	59	VOUT1	OUT	LV	Analog Video 1 Output
50	39	60	VIN1	IN	GND	Analog Video 1 Input
51	38	61	VIN2	IN	GND	Analog Video 2 Input
52	37	62	VIN3	IN	GND	Analog Video 3 Input
53	36	63	VIN4	IN	GND	Analog Video 4 Input
54	35	64	VIN5	IN	GND	Analog Video 5 Input
55	34	65	VIN6	IN	GND	Analog Video 6 Input
56	33	66	VIN7	IN	GND	Analog Video 7 Input
57	32	67	VIN8	IN	GND	Analog Video 8 Input
58	31	68	VIN9	IN	GND	Analog Video 9 Input

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
59	30	69	VIN10	IN	GND	Analog Video 10 Input
60	29	70	VIN11	IN	GND	Analog Video 11 Input
61	28	98	P23	IN/OUT	LV	Port 2, Bit 3 Input/Output
62	27	99	P22	IN/OUT	LV	Port 2, Bit 2 Input/Output
63	26	100	XTAL2	OUT	OBL	Analog Crystal Output
64	25	101	XTAL1	IN	OBL	Analog Crystal Input
65	24	102	VSUP1.8DIG	SUPPLY	OBL	Supply Voltage Digital Core, 1.8 V
66	23	103	GND	SUPPLY	OBL	Ground Platform
67	22	104	GND	SUPPLY	OBL	Ground Platform
68	21	105	VSUP3.3DIG	SUPPLY	OBL	Supply Voltage Digital Core, 3.3 V
69	20	106	VSUP5.0IF	SUPPLY	OBL	Supply Voltage IF ADC, 5.0 V
70	19	107	VSUP5.0FE	SUPPLY	OBL	Supply Voltage Analog IF Front-end, 5.0 V
71	18	108	RESETQ	IN/OUT	OBL	$\overline{\text{Reset}}$ Input/Output
72	17	109	IFIN+	IN	$VREF_{IF}$	Differential IF Input
73	16	110	IFIN-	IN	$VREF_{IF}$	Differential IF Input
74	15	111	VREFIF		OBL	Reference Voltage, IF ADC
75	14	112	TAGC	OUT	LV	Tuner AGC Output
76	13	113	AIN1R / SIF	IN/OUT	GND	Analog Audio 1 Input, Right Analog 2nd Sound IF Output
77	12	114	AIN1L	IN	GND	Analog Audio 1 Input, Left
78	11	115	AIN2R	IN	GND	Analog Audio 2 Input, Right
79	10	116	AIN2L	IN	GND	Analog Audio 2 Input, Left
–	–	117	AIN3R	IN	GND	Analog Audio 3 Input, Right
–	–	118	AIN3L	IN	GND	Analog Audio 3 Input, Left
–	–	119	AOUT2R	OUT	LV	Analog Audio 2 Output, Right
–	–	120	AOUT2L	OUT	LV	Analog Audio 2 Output, Left
80	9	–	AIN3R / AOUT2R	IN / OUT	LV	Analog Audio 3 Input, Right Analog Audio 2 Output, Right
81	8	–	AIN3L / AOUT2L	IN / OUT	LV	Analog Audio 3 Input, Left Analog Audio 2 Output, Left
82	7	121	AOUT1R	OUT	LV	Analog Audio 1 Output, Right
83	6	122	AOUT1L	OUT	LV	Analog Audio 1 Output, Left
84	5	123	SPEAKERR	OUT	LV	Analog Loudspeaker Output, Right
85	4	124	SPEAKERL	OUT	LV	Analog Loudspeaker Output, Left

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
86	3	125	VREFAU		OBL	Reference Voltage, Audio
87	2	126	VSUP8.0AU	SUPPLY	OBL	Supply Voltage Analog Audio, 8.0 V
88	1	127	GND	SUPPLY	OBL	Ground Platform
–	–	71	P37 / 656IO7	IN/OUT	LV	Port 3, Bit 7 Input/Output Digital 656 Bus 7 Input/Output
–	–	72	P36 / 656IO6	IN/OUT	LV	Port 3, Bit 6 Input/Output Digital 656 Bus 6 Input/Output
–	–	73	P35 / 656IO5	IN/OUT	LV	Port 3, Bit 5 Input/Output Digital 656 Bus 5 Input/Output
–	–	74	P34 / 656IO4	IN/OUT	LV	Port 3, Bit 4 Input/Output Digital 656 Bus 4 Input/Output
–	–	75	P33 / 656IO3	IN/OUT	LV	Port 3, Bit 3 Input/Output Digital 656 Bus 3 Input/Output
–	–	76	GNDEIO	SUPPLY	OBL	Ground Extended I/O Ports
–	–	77	VSUP3.3EIO	SUPPLY	OBL	Supply Voltage Extended I/O Ports, 3.3 V
–	–	78	P32 / 656IO2	IN/OUT	LV	Port 3, Bit 2 Input/Output Digital 656 Bus 2 Input/Output
–	–	79	P31 / 656IO1	IN/OUT	LV	Port 3, Bit 1 Input/Output Digital 656 Bus 1 Input/Output
–	–	80	P30 / 656IO0	IN/OUT	LV	Port 3, Bit 0 Input/Output Digital 656 Bus 0 Input/Output
–	–	81	P26 / 656VIO	IN/OUT	LV	Port 2, Bit 6 Input/Output Digital 656 Vsync Input/Output
–	–	82	P25 / 656HIO	IN/OUT	LV	Port 2, Bit 5 Input/Output Digital 656 Hsync Input/Output
–	–	83	P24 / 656CLKIO	IN/OUT	LV	Port 2, Bit 4 Input/Output Digital 656 Clock Input/Output
–	–	31	ADB19	OUT	LV	Address Bus 19 Output
–	–	21	ADB18	OUT	LV	Address Bus 18 Output
–	–	19	ADB17	OUT	LV	Address Bus 17 Output
–	–	22	ADB16	OUT	LV	Address Bus 16 Output
–	–	23	ADB15	OUT	LV	Address Bus 15 Output
–	–	18	ADB14	OUT	LV	Address Bus 14 Output
–	–	17	ADB13	OUT	LV	Address Bus 13 Output
–	–	26	ADB12	OUT	LV	Address Bus 12 Output
–	–	14	ADB11	OUT	LV	Address Bus 11 Output
–	–	96	ADB10	OUT	LV	Address Bus 10 Output

Pin No. PSSDIP88-1	Pin No. PSSDIP88-2	Pin No. PMQFP144-2	Pin Name	Type	Connection (If not used)	Short Description
–	–	15	ADB9	OUT	LV	Address Bus 9 Output
–	–	16	ADB8	OUT	LV	Address Bus 8 Output
–	–	27	ADB7	OUT	LV	Address Bus 7 Output
–	–	28	ADB6	OUT	LV	Address Bus 6 Output
–	–	29	ADB5	OUT	LV	Address Bus 5 Output
–	–	30	ADB4	OUT	LV	Address Bus 4 Output
–	–	84	ADB3	OUT	LV	Address Bus 3 Output
–	–	85	ADB2	OUT	LV	Address Bus 2 Output
–	–	86	ADB1	OUT	LV	Address Bus 1 Output
–	–	87	ADB0	OUT	LV	Address Bus 0 Output
–	–	88	DB0	IN/OUT	LV	Data Bus 0 Input/Output
–	–	89	DB1	IN/OUT	LV	Data Bus 1 Input/Output
–	–	90	DB2	IN/OUT	LV	Data Bus 2 Input/Output
–	–	91	DB3	IN/OUT	LV	Data Bus 3 Input/Output
–	–	92	DB4	IN/OUT	LV	Data Bus 4 Input/Output
–	–	93	DB5	IN/OUT	LV	Data Bus 5 Input/Output
–	–	94	DB6	IN/OUT	LV	Data Bus 6 Input/Output
–	–	95	DB7	IN/OUT	LV	Data Bus 7 Input/Output
–	–	32	RDQ	OUT	LV	$\overline{\text{Data Read Enable}}$ Output
–	–	33	WRQ	OUT	LV	$\overline{\text{Data Write Enable}}$ Output
–	–	34	OCF	OUT	LV	Opcode Fetch Output
–	–	35	ALE	OUT	LV	Address Latch Enable Output
–	–	36	RSTQ	OUT	LV	$\overline{\text{Internal CPU Reset}}$ Output
–	–	97	PSENQ	OUT	LV	$\overline{\text{Program Store Enable}}$ Output
–	–	20	PSWEQ	OUT	LV	$\overline{\text{Program Store Write Enable}}$ Output
–	–	51	XROMQ	IN	OBL	$\overline{\text{External ROM Enable}}$ Input
–	–	52	EXTIFQ	IN	LV	$\overline{\text{Enable External Interface}}$ Input
–	–	24	STOPQ	IN	LV	$\overline{\text{Stop CPU}}$ Input
–	–	25	ENEQ	IN	LV	$\overline{\text{Enable Emulation}}$ Input

4.3. Pin Descriptions

4.3.1. Supply Pins

VSUP1.8DIG – Supply Voltage 1.8 V
This pin is main and standby supply for the digital core logic of controller, video, display and deflection processing.

VSUP1.8FE – Supply Voltage 1.8 V
This pin is main and standby supply for the analog video front-end.

VSUP3.3FE – Supply Voltage 3.3 V
This pin is main and standby supply for the analog video front-end.

VSUP3.3IO – Supply Voltage 3.3 V
This pin is main and standby supply for the digital I/O-ports.

VSUP3.3DIG – Supply Voltage 3.3 V
This pin is main supply for the digital core logic of IF and audio processing and digital video back-end.

VSUP3.3BE – Supply Voltage 3.3 V
This pin is main supply for the analog video back-end.

VSUP5.0FE – Supply Voltage 5.0 V
This pin is main supply for the analog IF front-end.

VSUP5.0IF – Supply Voltage 5.0 V
This pin is main supply for the IF ADC.

VSUP5.0BE – Supply Voltage 5.0 V
This pin is main supply for the analog video back-end.

VSUP8.0AU – Supply Voltage 8.0 V
This pin is main supply for the analog audio processing.

GND – Ground Platform
This pin is main ground for all above supplies.

VSUP3.3DAC – Supply Voltage 3.3 V
This pin is main supply for the video DACs.

GNDDAC – Ground for 3.3 V Video DAC Supply

VSUP3.3EIO – Supply Voltage 3.3 V
This pin is main and standby supply for the extended digital I/O-ports available in QFP package only. It is internally connected to **VSUP3.3IO.**

GNDEIO – Ground for 3.3 V Extended I/O Supply
It is internally connected to GND.

Application Note:
All **GND** pins must be connected to a low-resistive ground plane underneath the IC. All supply pins must be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from **VSUPxx** to **GND** have to be placed as closely as possible to these pins. It is recommended to use more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended.

4.3.2. IF Pins

VREFIF – Reference Voltage for analog IF (Fig. 4–8)
This pin must be connected to **GND** via a circuitry according to the application circuit. Low inductance caps are necessary.

IFIN+, IFIN- – Balanced IF Input (Fig. 4–6)
These pins must be connected to the SAW filter output. The SAW filter has to be placed as close as possible. The layout of the IF input should be symmetrical with respect to **GND**.

SIF – 2nd Sound IF Output (Fig. 4–9)
Output level is set via I^2C-Bus. An appropriate sound processor (e.g. MSP) can be connected to this pin. This pin is also configurable as audio input (see Fig. 4–10).

TAGC – Tuner AGC Output (Fig. 4–7)
This pin controls the delayed tuner AGC. As it is a noise-shaped-I-DAC output, it has to be connected according to the application circuit.

4.3.3. Audio Pins

VREFAU – Reference Voltage for Analog Audio (Fig. 4–14)
This pin serves as the internal ground connection for the analog audio circuitry. It must be connected to the **GND** pin with a 3.3 µF and a 100 nF capacitor in parallel. This pins shows a DC level of typically 3.77 V.

AIN1 R/L – Audio 1 Inputs (Fig. 4–10)
The analog input signals for audio 1 are fed to these pins. Analog input connection must be AC coupled. The **AIN1 R** pin is also configurable as sound IF output (see Fig. 4–9).

AIN2 R/L – Audio 2 Inputs (Fig. 4–10)
The analog input signals for audio 2 are fed to these pins. Analog input connection must be AC coupled.

AIN3 R/L – Audio 3 Inputs (Fig. 4–10)
The analog input signals for audio 3 are fed to these pins. Analog input connection must be AC coupled.

AOUT1 R/L – Audio 1 Outputs (Fig. 4–11)
Output of the analog audio 1 signal. Connections to these pins are intended to be AC coupled.

AOUT2 R/L – Audio 2 Outputs (Fig. 4–11)
Output of the analog audio 2 signal. Connections to these pins are intended to be AC coupled.

SPEAKER R/L – Loudspeaker Outputs (Fig. 4–13)
Output of the loudspeaker signal. A 1 nF capacitor to **GND** must be connected to these pins. Connections to these pins are intended to be AC-coupled.

SUBW – Subwoofer Outputs (Fig. 4–13)
Output of the subwoofer signal. A 1 nF capacitor and a 10 kΩ resistor to **GND** must be connected to this pin. Connections to this pin are intended to be AC-coupled.

4.3.4. Video Pins

VIN 1–11 – Analog Video Input (Fig. 4–15)
These are the analog video inputs. A CVBS, S-VHS, YCrCb or RGB/FB signal is converted using the luma, chroma and component AD converters. The input signals must be AC-coupled by 100nF. In case of an analog fast blank signal carrying alpha blending information the input signal must be DC-coupled.

VOUT 1-3 – Analog Video Output (Fig. 4–16)
The analog video inputs that are selected by the video source select matrix are output at these pins.

RIN, GIN, BIN – Analog RGB Input (Fig. 4–17)
These pins are used to insert an external analog RGB signal, e.g. from a SCART connector which can be switched to the analog RGB outputs with the fast blank signal. Separate brightness and contrast settings for the external analog signals are provided.

FBIN – Fast Blank Input (Fig. 4–18)
This pin is used to switch the RGB outputs to the external analog RGB inputs. The active level (low or high) can be selected by software.

ROUT, GOUT, BOUT – Analog RGB Output (Fig. 4–19)
These pins are the analog Red/Green/Blue outputs of the back-end. The outputs are current sinks.

SVMOUT – Scan Velocity Modulation Output (Fig. 4–19)
This output delivers the analog SVM signal. The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50% of the maximum output current.

VRD – DAC Reference Decoupling (Fig. 4–20)
Via this pin the RGB-DAC reference voltage is decoupled by an external capacitor. The DAC output currents depend on this voltage, therefore a pulldown transistor can be used to shut off all beam currents. A decoupling capacitor of 4.7 µF in parallel to 100 nF (low inductance) is required.

XREF – DAC Current Reference (Fig. 4–20)
External reference resistor for DAC output currents, typical 1 kΩ to adjust the output current of the D/A converters. (see recommended operating conditions). This resistor has to be connected to ground as closely as possible to the pin.

4.3.5. CRT Pins

HOUT – Horizontal Drive Output (Fig. 4–21)
This open source output supplies the drive pulse for the horizontal output stage. An external pulldown resistor has to be used. The polarity and gating with the flyback pulse are selectable by software.

HFLB – Horizontal Flyback Input (Fig. 4–22)
Via this pin the horizontal flyback pulse is supplied to the VCT 49xyl, VCT 48xyl.

VPROT – Vertical Protection Input (Fig. 4–22)
The vertical protection circuitry prevents the picture tube from burn-in in the event of a malfunction of the vertical deflection stage. If the peak-to-peak value of the sawtooth signal from the vertical deflection stage is too small, the RGB output signals are blanked.

SAFETY – Safety Input (Fig. 4–22)
This input has two thresholds. A signal between the lower and upper threshold means normal function. A signal below the lower threshold or above the upper threshold is detected as malfunction and the RGB signals will be blanked.

VERT+, VERT– – Vertical Sawtooth Output (Fig. 4–23)
These pins supply the symmetrical drive signal for the vertical output stage. The drive signal is generated with 15-bit precision. The analog voltage is generated by a 4 bit current-DAC with an external resistor of 6.8 kΩ and uses digital noise shaping.

EW – East-West Parabola Output (Fig. 4–24)
This pin supplies the parabola signal for the East-West correction. The drive signal is generated with 15 bit precision. The analog voltage is generated by a 4 bit current-DAC with an external resistor of 6.8 kΩ and uses digital noise shaping.

PWMV – PWM Vertical Output (Fig. 4–21)
This pin provides an adjustable vertical parabola with 7 bit resolution and approx. 79.4 kHz PWM frequency.

DFVBL – Dynamic Focus Vertical Blanking (Fig. 4–21)
This pin supplies the blank pulse for dynamic focus during vertical blanking period or a free programmable horizontal pulse for horizontal dynamic focus generation. Alternatively it can be programmed as FIELD output, delivering even/odd field information.

SENSE – Measurement ADC Input (Fig. 4–27)
This is the input of the analog to digital converter for

the picture and tube measurement. Three measurement ranges are selectable with RSW1 and RSW2.

GNDM – Measurement ADC Reference Input
This is the reference ground for the measurement A/D converter. Connect this pin to GND.

RSW1 – Range Switch1 for Measuring ADC (Fig. 4–25)
These pin is an open drain pull-down output. During cutoff and white drive measurement the switch is off. During the rest of time it is on. The RSW1 pin can be used as second measurement ADC input for picture beam current measurement.

RSW2 – Range Switch2 for Measuring ADC (Fig. 4–26)
These pin is an open drain pull-down output. During cutoff measurement the switch is off. During white drive measurement the switch is on. Also during the rest of time it is on. It is used to set the range for white drive current measurement.

4.3.6. Controller Pins

XTAL1 – Crystal Input and **XTAL2** Crystal Output (Fig. 4–28)
These pins connect a 20.25 MHz crystal to the internal oscillator. An external clock can be fed into XTAL2.

RESETQ – Reset Input/Output (Fig. 4–29)
A low level on this pin resets the VCT 49xyI, VCT 48xyI. The internal CPU can pull down this pin to reset external devices connected to this pin.

TEST – Test Input (Fig. 4–30)
This pin enables factory test modes. For normal operation, it must be connected to ground. Alternatively this pins serves as subwoofwer output.

SCL – I^2C Bus Clock (Fig. 4–31)
This pin delivers the I^2C bus clock line. The signal can be pulled down by external slave ICs to slow down data transfer.

SDA – I^2C Bus Data (Fig. 4–31)
This pin delivers the I^2C bus data line.

P10–**P13, P20**–**P23** – I/O Port (Fig. 4–32)
These pins provide CPU controlled I/O ports.

P14–**P17** – I/O Port (Fig. 4–33)
These pins provide CPU controlled I/O ports. Additionally they can be used as analog inputs for the controller ADC.

P24–**P26, P30**–**P37** – I/O Port (Fig. 4–34)
These pins provide CPU controlled I/O ports.

ADB0–**ADB19** – Address Bus Output (Fig. 4–35)
These 20 lines provide the CPU address bus output to access external memory.

DB0–**DB7** – Data Bus Input/Output (Fig. 4–36)
These 8 lines provide the bidirectional CPU data bus to access external memory.

WRQ – $\overline{\text{Data Write Enable}}$ Output (Fig. 4–35)
This pin controls the direction of data exchange between the CPU and the external data memory device (SRAM).

RDQ – $\overline{\text{Data Read Enable}}$ Output (Fig. 4–35)
This pin is used to enable the output driver of the external data memory device (SRAM) for read access.

PSENQ – $\overline{\text{Program Store Enable}}$ Output (Fig. 4–35)
This pin is used to enable the output driver of the external program memory device (ROM/FLASH) for read access.

PSWEQ – $\overline{\text{Program Store Write Enable}}$ Output (Fig. 4–35)
This pin is used to write into the external program flash memory device.

XROMQ – $\overline{\text{External ROM Enable}}$ Input (Fig. 4–37)
This pin must be pulled low to access the external program memory. **XROMQ** has an internal pull-up resistor.

EXTIFQ – $\overline{\text{Enable External Memory Interface}}$ Input (Fig. 4–37)
This pin must be pulled low to enable the external memory interface. **EXTIFQ** has an internal pull-up resistor.

STOPQ – $\overline{\text{Stop}}$ CPU Input (Fig. 4–37)
Applying a low level during the input phase freezes the real-time relevant internal peripherals such as timers and interrupt controller. **STOPQ** has an internal pull-up resistor.

ENEQ – $\overline{\text{Enable Emulation}}$ Input (Fig. 4–37)
Only if this pin is set to low level, STOPQ and OCF are operational. **ENEQ** has an internal pull-up resistor.

ALE – Address Latch Enable Output (Fig. 4–35)
This signal indicates changes on the address bus.

OCF – Opcode Fetch Output (Fig. 4–35)
A high level driven by the CPU during output phase indicates the beginning of a new instruction.

RSTQ – $\overline{\text{Internal CPU Reset}}$ Input/Output (Fig. 4–38)
This pin is used for emulation purpose only. A low level on this pin resets the CPU. It also indicates an internal reset of the CPU. **RSTQ** has an internal pull-up resistor.

4.4. Pin Configuration

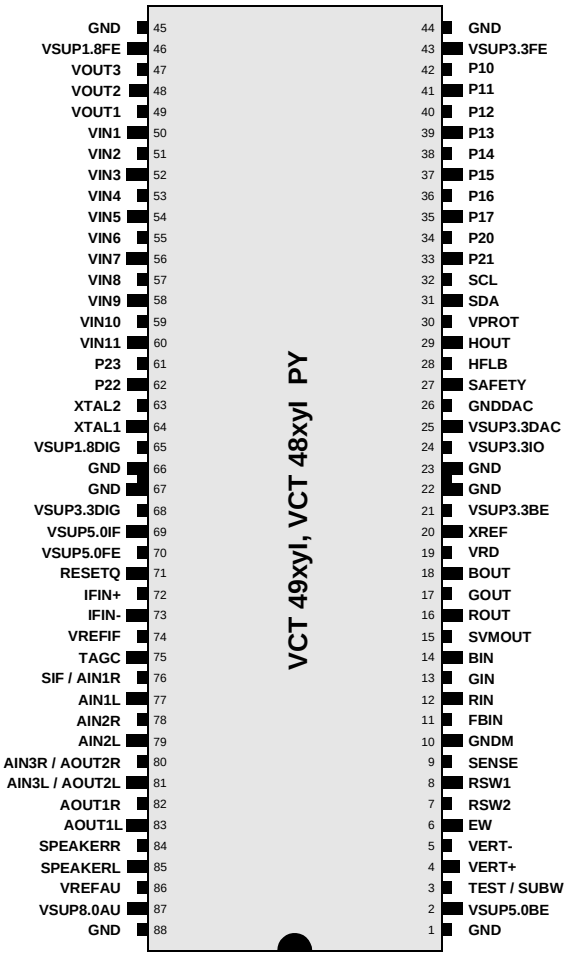


Fig. 4–3: PSSDIP88-1 package

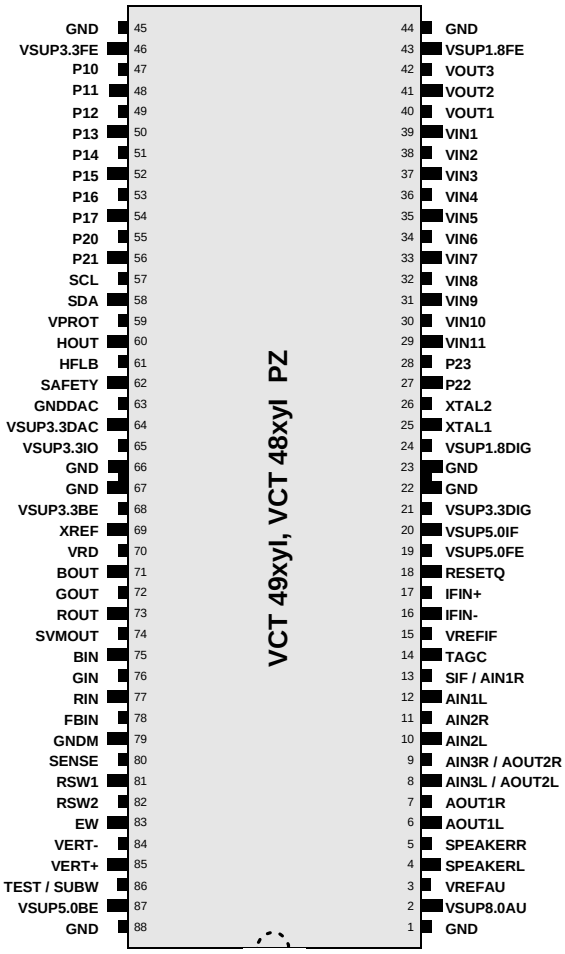


Fig. 4–4: PSSDIP88-2 package (pinning mirrored)

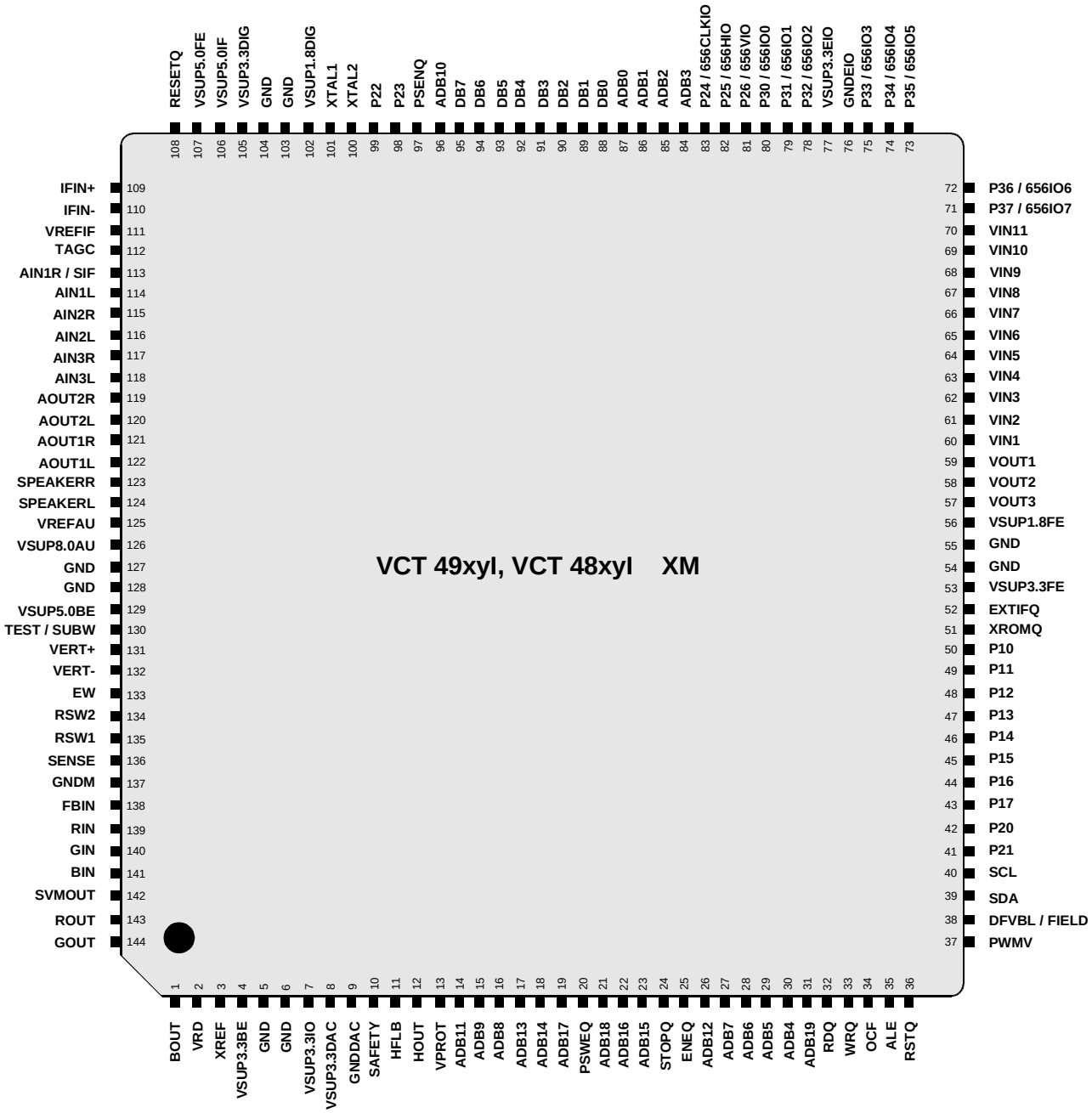


Fig. 4–5: PMQFP144-2 package

4.5. Pin Circuits

4.5.1. IF Pins

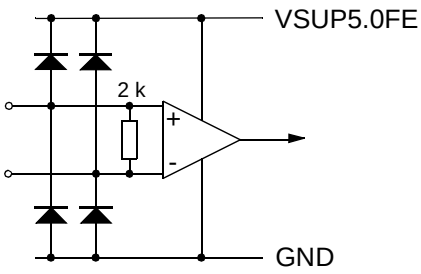


Fig. 4–6: Input Pins: **IFIN+, IFIN-**

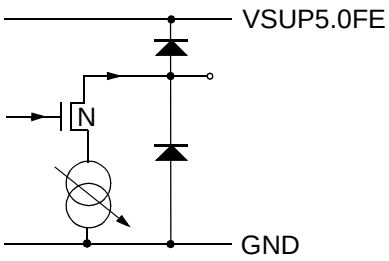


Fig. 4–7: Output Pin: **TAGC**

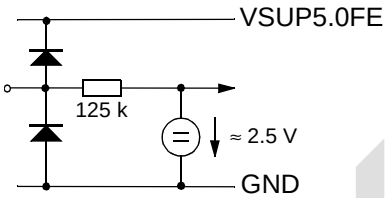


Fig. 4–8: Supply Pin: **VREFIF**

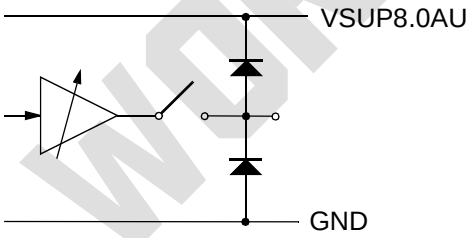


Fig. 4–9: Output Pin: **SIF**

4.5.2. Audio Pins

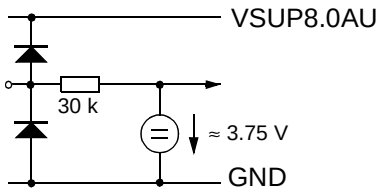


Fig. 4–10: Input Pins: **AIN1-3 R/L**

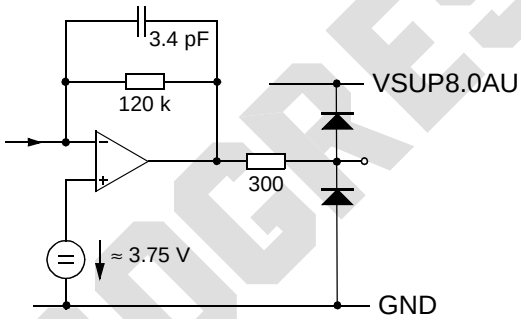


Fig. 4–11: Output Pins: **AOUT1 R/L**

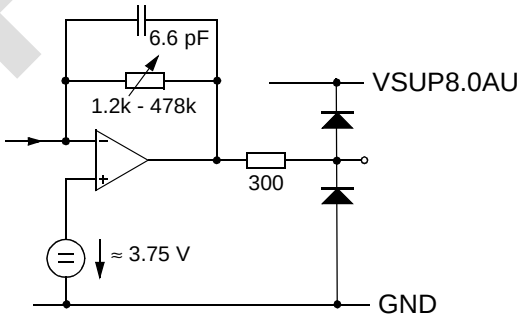


Fig. 4–12: Output Pins: **AOUT2 R/L**

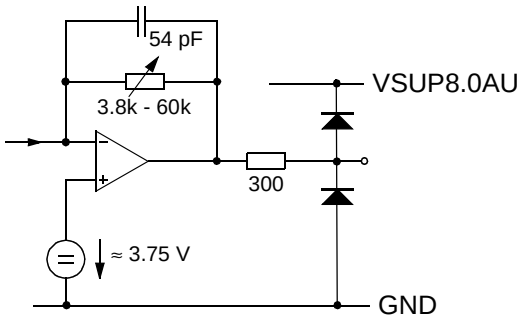


Fig. 4–13: Output Pins: **SPEAKER R/L, SUBW**

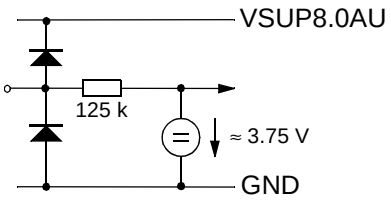


Fig. 4–14: Supply Pin: **VREFAU**

4.5.3. Video Pins

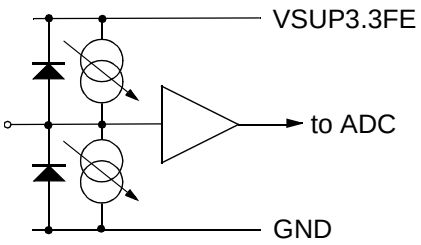


Fig. 4–15: Input Pins: **VIN 1-11**

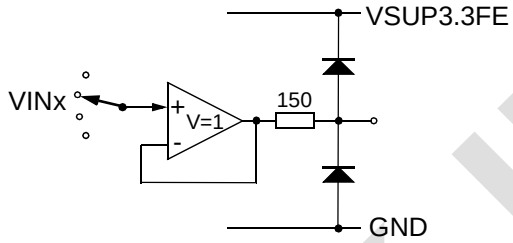


Fig. 4–16: Output Pins: **VOUT 1-3**

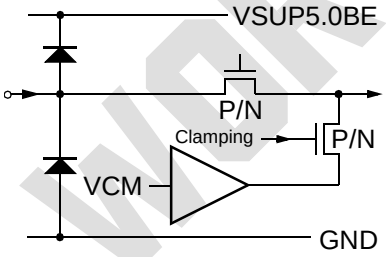


Fig. 4–17: Input Pins: **RIN, GIN, BIN**

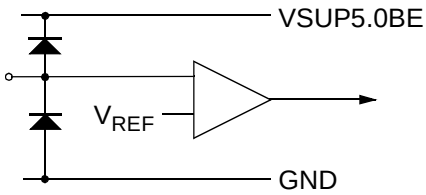


Fig. 4–18: Input Pin: **FBIN**

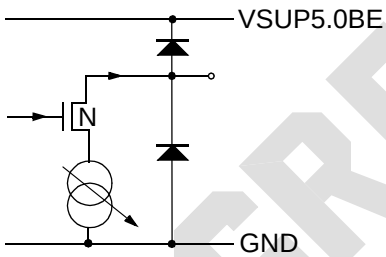


Fig. 4–19: Output Pins: **ROUT, GOUT, BOUT, SVMOUT**

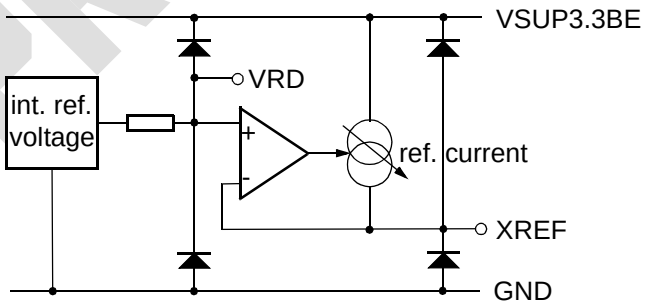


Fig. 4–20: Supply Pins: **XREF, VRD**

4.5.4. CRT Pins

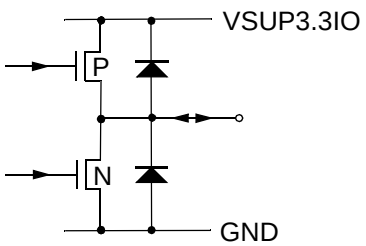


Fig. 4–21: Output Pins: **HOUT, FIELD, DFVBL, PWMV**

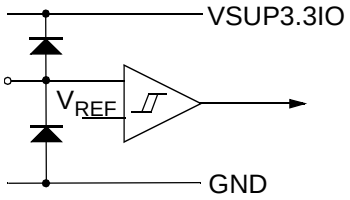


Fig. 4–22: Input Pins: **SAFETY, VPROT, HFLB**

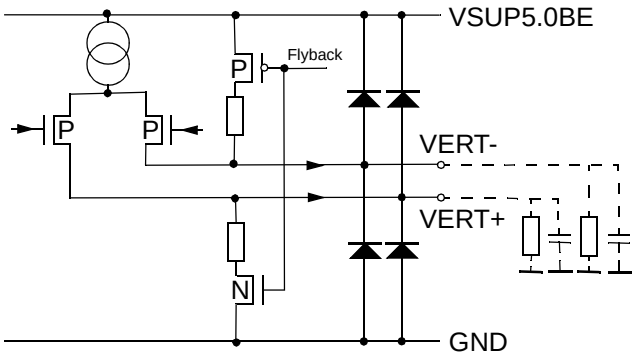


Fig. 4–23: Output Pins: **VERT+, VERT-**

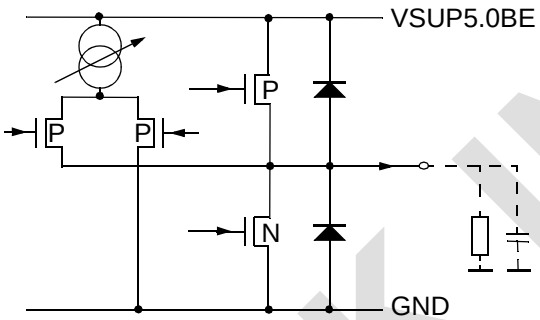


Fig. 4–24: Output Pin: **EW**

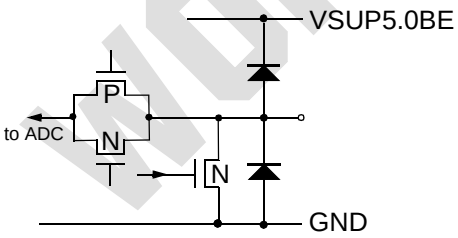


Fig. 4–25: Input/Output Pin: **RSW1**

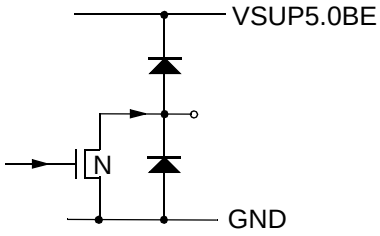


Fig. 4–26: Output Pin: **RSW2**

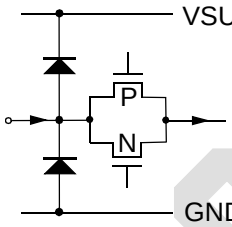


Fig. 4–27: Input Pin: **SENSE**

4.5.5. Controller Pins

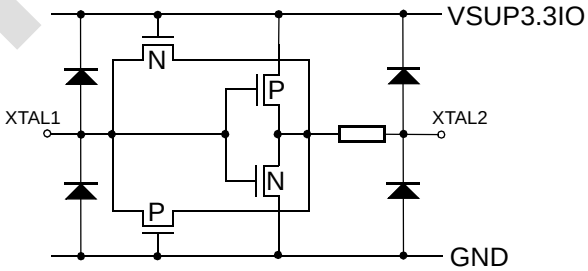


Fig. 4–28: Input/Output Pins: **XTAL1, XTAL2**

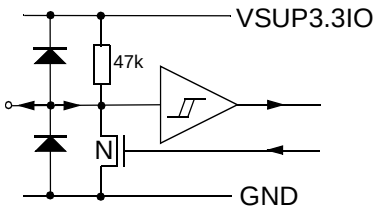


Fig. 4–29: Input/Output Pin: **RESETQ**

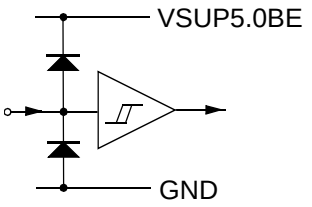


Fig. 4–30: Input Pin: **TEST**

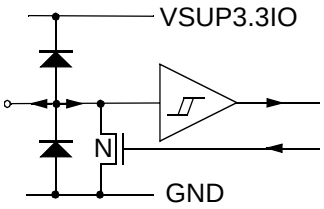


Fig. 4–31: Input/Output Pins: **SDA, SCL**

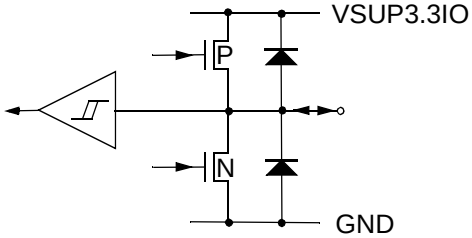


Fig. 4–32: Input/Output Pins: **P10-P13, P20-P23**

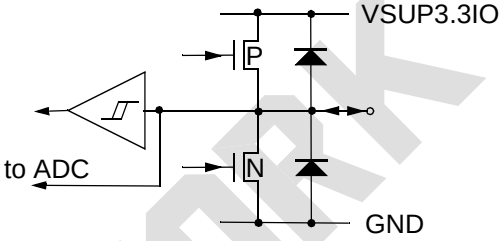


Fig. 4–33: Input/Output Pins: **P14-P17**

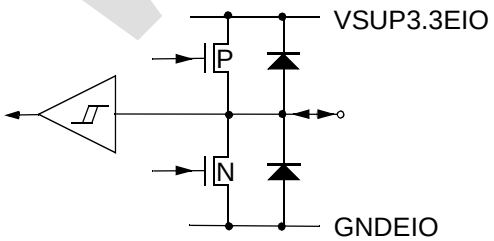


Fig. 4–34: Input/Output Pins: **P24-P26, P30-P37**

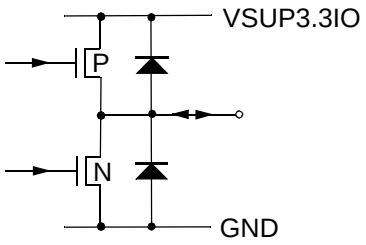


Fig. 4–35: Output Pins: **ADB0-ADB19, WRQ, RDQ, PSENQ, PSWEQ, ALE, OCF**

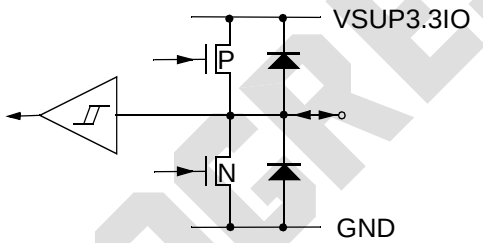


Fig. 4–36: Input/Output Pins: **DB0-DB7**

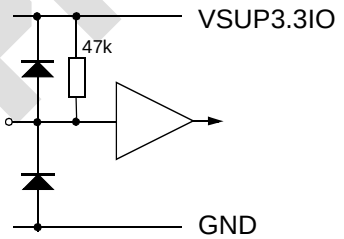


Fig. 4–37: Input Pins: **XROMQ, EXTIFQ, STOPQ, ENEQ**

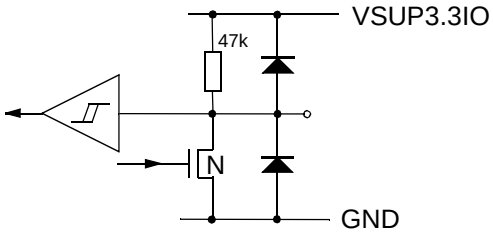


Fig. 4–38: Input/Output Pin: **RSTQ**

4.6. Electrical Characteristics

Abbreviations:

tbd = to be defined
vacant = not applicable
positive current values mean current flowing into the chip

4.6.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

All voltages listed are referenced to ground (list voltages = 0 V) except where noted. ???

All GND pins must be connected to a low-resistive ground plane close to the IC.

Table 4–1: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
T_A [1]	Ambient Operating Temperature PSSDIP88-1/-2 PMQFP144-2		 0 0	 65 [2] 65 [2]	 °C °C
T_C	Case Operating Temperature PSSDIP88-1/-2 PMQFP144-2		tbd	tbd	°C
T_S	Storage Temperature		–40	125	°C
P_{MAX}	Maximum Power Dissipation PSSDIP88-1/-2 PMQFP144-2		 – –	 2600 2600	 mW mW
$V_{SUP8.0}$	Supply Voltage 8.0 V	VSUP8.0AU	–0.3	9.0	V
$V_{SUP5.0}$	Supply Voltage 5.0 V	VSUP5.0x	–0.3	6.0	V
$V_{SUP3.3}$	Supply Voltage 3.3 V	VSUP3.3x	–0.3	3.6	V
$V_{SUP1.8}$	Supply Voltage 1.8 V	VSUP1.8x	–0.3	2.0	V
ΔV_{SUP}	Voltage differences within supply domains	???	-0.5	0.5	V

1) Measured on Micronas typical 2-layer (1s1p) board based on JESD - 51.2 Standard with maximum power consumption allowed for this package

2) A power-optimized board layout is recommended. The Case Operating Temperature mentioned in the “Absolute Maximum Ratings” must not be exceeded at worst case conditions of the application.

Table 4–1: Absolute Maximum Ratings, continued

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
V_I	Input Voltage		–0.3	$VSUP_x$+0.3[1)]	V
I_I	Input Current				mA
V_O	Output Voltage		–0.3	$VSUP_x$+0.3[1)]	V
I_O	Output Current				mA

[1)] Refer to Pin Circuits section 4.5. on page 24

4.6.2. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions/Characteristics” is not implied and may result in unpredictable behavior, reduce reliability and lifetime of the device.

All voltages listed are referenced to ground (list voltages = 0 V) except where noted. ???

All GND pins must be connected to a low-resistive ground plane close to the IC.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. For power up/down sequences, see the instructions in volume 6.

4.6.2.1. General Recommended Operating Conditions

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
T_A	Ambient Operating Temperature PSSDIP88-1/-2 PMQFP144-2		 0 0	 – –	 65[1)] 65[1)]	 °C °C
T_C	Case Operating Temperature PSSDIP88-1/-2 PMQFP144-2		tbd		tbd	°C
P_{MAX}	Maximum Power Dissipation PSSDIP88-1/-2 PMQFP144-2				 2600[2)] 2600[2)]	 mW mW
f_{XTAL}	Clock Frequency	XTAL1/2	–	20.25	–	MHz
$V_{SUP8.0}$	Supply Voltage 8.0 V (Range = 8 V)	VSUP8.0AU	7.6	8.0	8.7	V
	Supply Voltage 8.0 V (Range = 5 V)		4.75	5.0	5.25	V
$V_{SUP5.0}$	Supply Voltage 5.0 V	VSUP5.0x	4.75	5.0	5.25	V
$V_{SUP3.3}$	Supply Voltage 3.3 V	VSUP3.3x	3.15	3.3	3.45	V
$V_{SUP1.8}$	Supply Voltage 1.8 V	VSUP1.8x	1.71	1.8	1.89	V
ΔV_{SUP}	Voltage differences within supply domains	???	-0.5	0	0.5	V
VIL	Input Voltage Low					V
VIH	Input Voltage High					V
RV	Reset Voltage					V

1) A power-optimized board layout is recommended. The Case Operating Temperatures mentioned in the “Recommended Operating Conditions” must not be exceeded at worst case conditions of the application.

2) P_{MAX} variation: user-determined by application circuit for I/Os

4.6.3. Recommended Tuner Characteristics

Symbol	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
a_{tuner}	Minimum Gain Control Range	40	–	–	dB
S_{tuner}	AGC Control Voltage Sensitivity	–	–	50	dB/V

4.6.3.1. Recommended Crystal Characteristics

Symbol	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
T_A	Operating Ambient Temperature	0	–	65	°C
f_P	Parallel Resonance Frequency with Load Capacitance **C_L = 13 pF**	20.248	20.250	20.252	MHz
$\Delta f_P/f_P$	Accuracy of Adjustment	–	–	±40	ppm
$\Delta f_P/f_P$	Frequency Temperature Drift	–	–	±30	ppm
R_R	Series Resistance	–	–	25	W
C_0	Shunt Capacitance	3	–	7	pF
Load Capacitance Recommendation					
C_{Lext}	External Load Capacitance [1] from Pins to Ground (pin names: Xtal1 Xtal2)	–	3.3	–	pF

[1] Remarks on defining the External Load Capacitance:
External capacitors at each crystal pin to ground are required. They are necessary to tune the effective load capacitance of the PCBs to the required load capacitance C_L of the crystal. The higher the capacitors, the lower the clock frequency results. The nominal free running frequency should match f_p MHz. Due to different layouts of customer PCBs the matching capacitor size should be determined in the application. The suggested value is a figure based on experience with various PCB layouts.

4.6.3.2. Analog Input and Output Recommendations

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
IF						
f_{in}	Input Frequency	IFIN+, IFIN-	–	38.9	60	MHz
V_{tot}	Maximum Input Voltage TOP = 0 TOP = 15		 – –	 200 20	 – –	 mVpp mVpp
Audio						
C_{VREF}	VREF Filter Capacitor	VREFAU	–20%	3.3	+20%	µF
	Ceramic Capacitor in Parallel		–20%	100	+20%	nF
C_{Ain}	DC-Decoupling Capacitor for Audio Inputs	AINns[1)]	–20%	470	+20%	nF
V_{Ain}	Audio Input Level		–	–	2.0	V_{RMS}
R_{Aout}	Audio Load Resistance	AOUTns[1)] SPEAKERs[1)] SUBW	10	–	–	kΩ
C_{Aout}	Audio Load Capacitance		–	–	6.0	nF
Video						
V_{VIN}	Video Input Level	VIN1–11	0.5	1.0	1.5	V
C_{VIN}	Input Coupling Capacitor Video Inputs		–	100	–	nF
RGB						
R_{xref}	RGB–DAC Current defining Resistor	XREF	0.95	1	1.5	K
C_{RGBIN}	RGB Input Coupling Capacitor	RIN GIN BIN	–	15	–	nF
Deflection						
R_{load}	Deflection Load Resistance	EW, VERT+, VERT-	-	6.8	-	kΩ
C_{load}	Deflection Load Capacitance		-	68	-	nF

1) “n” means “1”, “2” or “3”, “s” means “L” or “R”

4.6.4. Characteristics

If not otherwise designated under test conditions, all characteristics are specified for recommended operating conditions (see Section 4.6.2. on page 1-30).

4.6.4.1. Package Characteristics

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
R_{thjc}	Junction-to-Case Thermal Resistance: PSSDIP88-1/-2 PMQFP144-2		 – –	 5 tbd	 – –	 K/W K/W	
R_{thja}	Junction-to-Ambient Thermal Resistance: PSSDIP88-1/-2 PMQFP144-2		 – –	 21 tbd	 – –	 K/W K/W	

4.6.4.2. Standby Power Consumption

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
P_{STDBY}	Standby Power Dissipation	VSUP1.8DIG VSUP1.8FE VSUP3.3FE VSUP3.3IO VSUP3.3EIO	–	65	tbd	mW	VSUP8.0AU = VSUP5.0IF = VSUP5.0FE = VSUP5.0BE = VSUP3.3DAC = VSUP3.3BE = VSUP3.3DIG = GND, all ports in input mode, CLK_SRC=1, PLLOFF=1, all clock domains off, all ADCs, VOUTs and DACs in standby mode
$I_{STDBY1.8DIG}$	Standby Current Consumption	VSUP1.8DIG	–	16	tbd	mA	
$I_{STDBY1.8FE}$	Standby Current Consumption	VSUP1.8FE	–	0	tbd	mA	
$I_{STDBY3.3FE}$	Standby Current Consumption	VSUP3.3FE	–	0	tbd	mA	
$I_{STDBY3.3IO}$	Standby Current Consumption	VSUP3.3IO VSUP3.3EIO	–	11	tbd	mA	on-chip flash

4.6.4.3. Normal Power Consumption

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
P_{TOT}	Total Power Dissipation	VSUPxx	–	2200	tbd	mW	recommended operating conditions, all ports in input mode
$I_{VSUP1.8DIG}$	Current Consumption	VSUP1.8DIG	–	175	tbd	mA	
$I_{VSUP1.8FE}$	Current Consumption	VSUP1.8FE	–	225	tbd	mA	
$I_{VSUP3.3FE}$	Current Consumption	VSUP3.3FE	–	48	tbd	mA	
$I_{VSUP3.3IO}$ $I_{VSUP3.3EIO}$	Current Consumption	VSUP3.3IO VSUP3.3EIO	–	11	tbd	mA	
$I_{VSUP3.3DAC}$	Current Consumption	VSUP3.3DAC	–	26	tbd	mA	
$I_{VSUP3.3BE}$	Current Consumption	VSUP3.3BE	–	25	tbd	mA	
$I_{VSUP3.3DIG}$	Current Consumption	VSUP3.3DIG	–	95	tbd	mA	
$I_{VSUP5.0FE}$	Current Consumption	VSUP5.0FE	–	65	tbd	mA	
$I_{VSUP5.0IF}$	Current Consumption	VSUP5.0IF	–	65	tbd	mA	
$I_{VSUP5.0BE}$	Current Consumption	VSUP5.0BE	–	18	tbd	mA	
$I_{VSUP8.0AU}$	Current Consumption	VSUP8.0AU	–	12	tbd	mA	

4.6.4.4. Leakage Current

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
I_L	Input and Output Leakage Current	All I/O Pins	–	–	1	µA	

4.6.4.5. Test Input

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{IL}	Input Low Voltage	TEST	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	

4.6.4.6. Reset Input/Output

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{IL}	Input Low Voltage	RESETQ	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4	V	I_I = 2 mA

4.6.4.7. I²C Bus Interface

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{IL}	Input Low Voltage	SDA, SCL	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4 0.6	V V	I_I = 3 mA I_I = 6 mA
C_I	Input Capacitance		–	–	5	pF	
t_F	Signal Fall Time		–	–	300	ns	C_L = 400 pF
t_R	Signal Rise Time		–	–	300	ns	C_L = 400 pF
f_{SCL}	Clock Frequency	SCL	0	–	400	kHz	
t_{LOW}	Low Period of SCL		1.3	–	–	µs	
t_{HIGH}	High Period of SCL		0.6	–	–	µs	
$t_{SU\ Data}$	Data Set Up Time to SCL high	SDA	100	–	–	ns	
$t_{HD\ Data}$	DATA Hold Time to SCL low		0	–	0.9	µs	

4.6.4.8. IF Input

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
SAW Input							
Z_{in}	Differential Input Impedance R C	IFIN+ IFIN–	 1.6 1	 2 –	 2.4 4	 kΩ pF	
V_{wanted}	Maximum wanted Signal Input Voltage TOP = 0 TOP = 15		 – – – –	 200 97 20 77	 – – – –	 mV_{pp} dBuV mV_{pp} dBuV	FS
S_{IF}	Sensitivity (S/N unweighted = 26 dB)		–	1	–	mV	fin = 38.9 MHz, TOP gain = 10 dB
Low Noise Preamplifier (with Tuner Take Over Point Setting)							
TOP_{min}	Minimum Gain		–	0	–	dB	
TOP_{max}	Maximum Gain		–	20	–	dB	
TOP_{step}	Stepsize of Gain		–	1.33	–	dB	
Analog Front-end							
G_{tol}	Total Gain Tolerance		–	–	±1	dB	matched inputs
Carrier Recovery							
D_{AFC}	Frequency Tolerance = AFC Accuracy		–	–	50	kHz	
f_{lock}	Lock in range = frequency true demodulation range		0.8 1.0	– –	– –	MHz MHz	direction: adjacent channel direction: own channel

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
VIF AGC							
f_{VAGC}	Control Bandwidth		–	–	–		
BW_n	Negative Modulation		–	200	–	Hz	
BW_p	Positive Modulation		–	1	–	Hz	
BW_{pinc}	Positive Modulation Increasing Signal (white picture)		–	200	–	Hz	
BW_{bp}	Positive Modulation Back Porch Control		–	200	–	Hz	
Video Output of IF Demodulator/ IF Stage to Video Front-end/Matrix							
V_{sync}	Sync Level (minimum DAC value)	VIN0	1.0	1.2	1.4	V	
V_{vidmax}	Maximum Level (maximum DAC value)		1.8	2.1	2.4	V	
V_{vidpp}	Full-Scale Voltage		0.8	0.9	1.0	V_{pp}	
$f_{-1dBvid}$	Cutoff Frequency		6	–	–	MHz	
SNR_{vidw}	Weighted Video S/N		56	58	–	dB	Weighted video S/N (CCIR567, 10 kHz...5 MHz) 50% white picture
SNR_{vidu}	Unweighted Video S/N		48	51	–	dB	Unweighted video S/N (10 kHz...5 MHz) 50% white picture
$a_{1.07}$	Intermodulation ratio		65	–	–	dB	blue picture, P_{SC1} = –13 dB, no sound shelf $\alpha_{1.07} = P_{CC} - P_{1.07}$ +3 dB

4.6.4.9. Sound IF Output

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{sifpp}	Full-Scale Voltage	SIF	– – – –	1.5 1.1 0.8 0.6	– – – –	V_{pp}	@ SIF_REF=0 @ SIF_REF=1 @ SIF_REF=2 @ SIF_REF=3
$f_{-1dBsif}$	Cutoff Frequency $f_{-1\ dB}$		6	–	–	MHz	C_{Load} < 30 pF, R_{Load_AC} > 1 kΩ
R_{outsif}	Output Resistance		–	–	50	Ω	f < 6 MHz
SNR_{fm_b}	Weighted Sound S/N SC1/SC2		52/52	–	–	dB	black picture, CCIR 468, quasi peak, 0 dB = 27 kHz
SNR_{fm_w}	Weighted Sound S/N SC1/SC2		52/52	–	–	dB	white picture, CCIR 468, quasi peak, 0 dB = 27 kHz
SNR_{fm_fubk}	Weighted Sound S/N SC1/SC2		48/46	–	–	dB	FuBK picture, CCIR 468, quasi peak, 0 dB = 27 kHz
SNR_{fm_250}	Weighted Sound S/N SC1/SC2		52/45	–	–	dB	250 kHz picture, CCIR 468, quasi peak, 0 dB = 27 kHz

4.6.4.10. Tuner AGC Output

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{sup_tun}	Maximum Output Voltage	TAGC	–	–	5	V	
V_{sup_min}	Minimum Voltage for Monotony		0.3	–	–	V	
I_{TAGC}	Maximum Output Sink Current		680	800	920	µA	90% FS

4.6.4.11. Analog Audio Inputs and Outputs

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Reference Voltage							
V_{VREF}	VREFAU Open Circuit Voltage (VSUP8.0AU = 8 V)	VREFAU	–	3.77	–	V	R_{load} ≥10 MΩ
	VREFAU Open Circuit Voltage (VSUP8.0AU = 5 V)		–	2.51	–	V	
R_{outAGN}	VREFAU Output Resistance (VSUP8.0AU = 8 V)		70	125	180	kΩ	3 V ≤ V_{VREF} ≤ 4 V
	VREFAU Output Resistance (VSUP8.0AU = 5 V)		47	83	120	kΩ	
PSRR	Power Supply Rejection		–	80	–	dB	1 kHz Noise on VSUP8.0AU
Analog Audio Input							
R_{AIN}	Audio Input Resistance from T_A = 0 to 70 °C	AINns[1)]	19	30	44	kΩ	f_{signal} = 1 kHz, I = 0.05 mA
V_{AINCL}	Analog Input Clipping Level for Analog-to-Digital-Conversion (VSUP8.0AU = 8 V)		2.00	–	2.25	V_{RMS}	f_{signal} = 1 kHz
	Analog Input Clipping Level for Analog-to-Digital-Conversion (VSUP8.0AU = 5 V)		1.13	–	1.51	V_{RMS}	
Analog Audio Output							
R_{AOut}	Audio Output Resistance	AOUTns[1)]	200 200	330 –	460 500	Ω Ω	f_{signal} = 1 kHz, I = 0.1 mA T_j = 27 °C T_A = 0 to 70 °C
dV_{AoutDC}	Deviation of DC-Level at Audio Output from VREFAU Voltage		–70	–	+70	mV	
V_{Aout}	Signal Level at Audio Output (VSUP8.0AU = 8 V)		1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz Volume 0 dB Full Scale input
	Signal Level at Audio Output (VSUP8.0AU = 5 V)		1.17	1.27	1.37	V_{RMS}	

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
$A_{AintoAout}$	Gain from Analog Audio Input to Audio Output	AINns[1] → AOUTns[1]	–1.0	–	+0.5	dB	f_{signal} = 1 kHz
$f_{rAintoAout}$	Frequency Response from Analog Input to Audio Output		–0.5	–	+0.5	dB	with resp. to 1 kHz Bandwidth: 0 to 20000 Hz
PSRR	Power Supply Rejection		–	70	–	dB	1 kHz Noise on VSUP8.0AU
Speaker Output							
$R_{Speaker}$	Speaker Output Resistance	SPEAKERs[1]	200 200	330 –	460 500	Ω Ω	f_{signal} = 1 kHz, I = 0.1 mA T_j = 27 °C T_A = 0 to 70 °C
$dV_{SpeakerDC}$	Deviation of DC-Level at Speaker Output from VREFAU Voltage		–70	–	+70	mV	
$V_{Speaker}$	Signal Level at Speaker Output (VSUP8.0AU = 8 V)		1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz Volume 0 dB Full-scale input
	Signal Level at Speaker Output (VSUP8.0AU = 5 V)		1.17	1.27	1.37	V_{RMS}	
[1] "n" means "1", "2", or "3"; "s" means "L" or "R"							
Subwoofer Output							
R_{Subw}	Subwoofer Output Resistance	SUBW	200 200	330 –	460 500	Ω Ω	f_{signal} = 100 Hz, I = 0.1 mA T_j = 27 °C T_A = 0 to 70 °C
dV_{SubwDC}	Deviation of DC-Level at Sub-woofer Output from VREFAU Voltage		–70	–	+70	mV	
V_{Subw}	Signal Level at Subwoofer Output (VSUP8.0AU = 8 V)		1.8	1.9	2.0	V_{RMS}	f_{signal} = 100 Hz Volume 0 dB Full-scale input
	Signal Level at Subwoofer Output (VSUP8.0AU = 5 V)		1.17	1.27	1.37	V_{RMS}	

4.6.4.11.1. Analog Audio Performance

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Specifications for VSUP8.0AU = 8 V							
SNR	Signal-to-Noise Ratio						
	from Analog Audio Input to Audio Output	AINns[1] → AOUTns[1]	93	96	–	dB	Input Level = –20 dB, f_{sig} = 1 kHz, unweighted 20 Hz...20 kHz
	from Analog Audio Input to Speaker Output for Analog Volume at 0 dB for Analog Volume at –30 dB	SPEAKERs[1]	 tbd tbd	 tbd tbd		 dB dB	Input Level = –20 dB, f_{sig} = 1 kHz, unweighted 20 Hz...16 kHz
THD	Total Harmonic Distortion						
	from Analog Audio Input to Audio Output	AINns[1] → AOUTns[1]	–	0.01	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, unweighted 20 Hz...20 kHz
Specifications for VSUP8.0AU = 5 V							
SNR	Signal-to-Noise Ratio						
	from Analog Audio Input to Audio Output	AINns[1] → AOUTns[1]	90	93	–	dB	Input Level = –20 dB, f_{sig} = 1 kHz, unweighted 20 Hz...20 kHz
	from Analog Audio Input to Speaker Output for Analog Volume at 0 dB for Analog Volume at –30 dB	SPEAKERs[1]	 tbd tbd	 tbd tbd		 dB dB	Input Level = –20 dB, f_{sig} = 1 kHz, unweighted 20 Hz...16 kHz
THD	Total Harmonic Distortion						
	from Analog Audio Input to Audio Output	AINns[1] → AOUTns[1]	–	–	0.1	%	Input Level = –3 dBr, f_{sig} = 1 kHz, unweighted 20 Hz...20 kHz
CROSSTALK Specifications for VSUP8.0AU = 8 V and 5 V							
XTALK	Crosstalk Attenuation						Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ
	between left and right channel within Audio Input/Output pair (L→R, R→L) AINns[1] → AOUTns[1]		 80	 –	 –	 dB	unweighted 20 Hz...20 kHz
	between Audio Input/Output pairs D = disturbing program O = observed program D: AINns[1] → AOUTns[1] O: AINns[1] → AOUTns[1]		 100	 –	 –	 dB	unweighted 20 Hz...20 kHz same signal source on left and right disturbing channel, effect on each observed output channel

[1] "n" means "1"or "2" or "3"; "s" means "L" or "R"

4.6.4.11.2. Sound Standard Dependent Characteristics

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
NICAM Characteristics (MSP Standard Code = 8)							DRX-Input: norm conditions
$dV_{NICAMOUT}$	Tolerance of Output Voltage of NICAM Baseband Signal	SPEAKERs[1] AOUTns[1]	–1.5	–	+1.5	dB	2.12 kHz, Modulator input level = 0 dBref
S/N_{NICAM}	S/N of NICAM Baseband Signal		72	–	–	dB	
THD_{NICAM}	Total Harmonic Distortion + Noise of NICAM Baseband Signal		–	–	0.1	%	2.12 kHz, Modulator input level = 0 dBref
BER_{NICAM}	NICAM: Bit Error Rate		–	–	1	10^{-7}	norm conditions
fR_{NICAM}	NICAM Frequency Response, 20...15000 Hz		–1.0	–	+1.0	dB	Modulator input level = –12 dB dBref; RMS
$XTALK_{NICAM}$	NICAM Crosstalk Attenuation (Dual)		80	–	–	dB	
SEP_{NICAM}	NICAM Channel Separation (Stereo)		80	–	–	dB	
FM Characteristics (MSP Standard Code = 3)							DRX-Input: norm conditions
dV_{FMOUT}	Tolerance of Output Voltage of FM Demodulated Signal	SPEAKERs[1] AOUTns[1]	–1.5	–	+1.5	dB	1 FM-carrier, 50 µs, 1 kHz, 40 kHz deviation; RMS
S/N_{FM}	S/N of FM Demodulated Signal		tbd	–	–	dB	
THD_{FM}	Total Harmonic Distortion + Noise of FM Demodulated Signal		–	–	0.1	%	
fR_{FM}	FM Frequency Responses, 20...15000 Hz		–1.0	–	+1.0	dB	1 FM-carrier 5.5 MHz, 50 µs, Modulator input level = –14.6 dBref; RMS
$XTALK_{FM}$	FM Crosstalk Attenuation (Dual)		80	–	–	dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; Bandpass 1 kHz
SEP_{FM}	FM Channel Separation (Stereo)		50	–	–	dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS
AM Characteristics (MSP Standard Code = 9)							DRX-Input: norm conditions
$S/N_{AM(1)}$	S/N of AM Demodulated Signal Measurement Condition: RMS/Flat	SPEAKERs[1] AOUTns[1]	tbd	–	–	dB	
$S/N_{AM(2)}$	S/N of AM Demodulated Signal Measurement Condition: QP/CCIR		tbd	–	–	dB	
THD_{AM}	Total Harmonic Distortion + Noise of AM Demodulated Signal		–	–	0.6	%	
fR_{AM}	AM Frequency Response 50...12000 Hz		–2.5	–	+1.0	dB	

[1] "n" means "1"or "2" or "3"; "s" means "L" or "R"

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
BTSC Characteristics (MSP Standard Code = 20_{hex}, 21_{hex})							DRX-Input: norm conditions
S/N_{BTSC}	S/N of BTSC Stereo Signal S/N of BTSC-SAP Signal	SPEAKERs[1] AOUTns[1]	tbd tbd	– –	– –	dB dB	1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz
THD_{BTSC}	THD+N of BTSC Stereo Signal THD+N of BTSC SAP Signal		– –	– –	0.1 0.5	% %	1 kHz L or R or SAP, 100% 75 µs EIM[2], DBX NR or MNR, RMS unweighted 0 to 15 kHz
fR_{DBX}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz Frequency Response of BTSC-SAP, 50 Hz...9 kHz		–1.0 –1.0	– –	1.0 1.0	dB dB	L or R or SAP, 1%...66% EIM[2], DBX NR
fR_{MNR}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz		–2.0	–	2.0	dB	L or R 5%...66% EIM[2], MNR
	Frequency Response of BTSC-SAP, 50 Hz...9 kHz		–2.0	–	2.0	dB	SAP, white noise, 10% Modulation, MNR
$XTALK_{BTSC}$	Stereo → SAP SAP → Stereo		76 80	– –	– –	dB dB	1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz
SEP_{DBX}	Stereo Separation DBX NR 50 Hz...10 kHz 50 Hz...12 kHz		 tbd tbd	 – –	 – –	 dB dB	L or R 1%...66% EIM[2], DBX NR
SEP_{MNR}	Stereo Separation MNR		tbd	–	–	dB	L = 300 Hz, R = 3.1 kHz 14% Modulation, MNR
FM_{pil}	Pilot deviation threshold Stereo off → on Stereo on → off	SIF	 3.2 1.2	 – –	 3.5 1.5	 kHz kHz	4.5 MHz carrier modulated with f_h = 15.734 kHz SIF level = 100 mV_{pp} indication: STATUS Bit[6]
f_{Pilot}	Pilot Frequency Range		15.563	–	15.843	kHz	standard BTSC stereo signal, sound carrier only

1) "n" means "1"or "2" or "3"; "s" means "L" or "R"
2) EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
BTSC Characteristics (MSP Standard Code = 20_{hex}, 21_{hex}) with a minimum IF input signal level of 70 mVpp (measured without any video/chroma signal components)							DRX-Input: norm conditions
S/N_{BTSC}	S/N of BTSC Stereo Signal S/N of BTSC-SAP Signal	SPEAKERs[1] AOUTns[1]	tbd tbd	– –	– –	dB dB	1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz
THD_{BTSC}	THD+N of BTSC Stereo Signal THD+N of BTSC SAP Signal		– –	– –	0.15 0.8	% %	1 kHz L or R or SAP, 100% 75 µs EIM[2], DBX NR or MNR, RMS unweighted 0 to 15 kHz
fR_{DBX}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz Frequency Response of BTSC-SAP, 50 Hz...9 kHz		–1.0 –1.0	– –	1.0 1.0	dB dB	L or R or SAP, 1%...66% EIM[2], DBX NR
fR_{MNR}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz		–2.0	–	2.0	dB	L or R 5%...66% EIM[2], MNR
	Frequency Response of BTSC-SAP, 50 Hz...9 kHz		–2.0	–	2.0	dB	SAP, white noise, 10% Modulation, MNR
$XTALK_{BTSC}$	Stereo → SAP SAP → Stereo		75 75	– –	– –	dB dB	1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz
SEP_{DBX}	Stereo Separation DBX NR 50 Hz...10 kHz 50 Hz...12 kHz		 tbd tbd	 – –	 – –	 dB dB	L or R 1%...66% EIM[2], DBX NR
SEP_{MNR}	Stereo Separation MNR		tbd	–	–	dB	L = 300 Hz, R = 3.1 kHz 14% Modulation, MNR

[1] "n" means "1"or "2" or "3"; "s" means "L" or "R"
[2] EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
EIA-J Characteristics (MSP Standard Code = 30_{hex})							DRX-Input: norm conditions
S/N_{EIAJ}	S/N of EIA-J Stereo Signal S/N of EIA-J Sub-Channel	SPEAKERs[1)] AOUTns[1)]	tbd tbd	– –	– –	dB dB	1 kHz L or R, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz
THD_{EIAJ}	THD+N of EIA-J Stereo Signal THD+N of EIA-J Sub-Channel		– –	– –	0.2 0.3	% %	
fR_{EIAJ}	Frequency Response of EIA-J Stereo, 50 Hz...12 kHz Frequency Response of EIA-J Sub-Channel, 50 Hz...12 kHz		–1.0 –1.0	– –	1.0 1.0	dB dB	100% modulation, 75 µs deemphasis
$XTALK_{EIAJ}$	Main → SUB Sub → MAIN		66 80	– –	– –	dB dB	1 kHz L or R, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz
SEP_{EIAJ}	Stereo Separation 50 Hz...5 kHz 50 Hz...10 kHz		 tbd tbd	 – –	 – –	 dB dB	EIA-J Stereo Signal, L or R 100% modulation
FM-Radio Characteristics (MSP Standard Code = 40_{hex})							DRX-Input: norm conditions
S/N_{UKW}	S/N of FM-Radio Stereo Signal	SPEAKERs[1)] AOUTns[1)]	tbd	–	–	dB	1 kHz L or R, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz
THD_{UKW}	THD+N of FM-Radio Stereo Signal		–	–	0.1	%	
fR_{UKW}	Frequency Response of FM-Radio Stereo 50 Hz...15 kHz		–1.0	–	+1.0	dB	L or R, 1%...100% modulation, 75 µs deemphasis
SEP_{UKW}	Stereo Separation 50 Hz...15 kHz		tbd	–	–	dB	
f_{Pilot}	Pilot Frequency Range	SIF	18.844	–	19.125	kHz	standard FM radio stereo signal

[1)] “n” means “1”or “2” or “3”; “s” means “L” or “R”

4.6.4.12. Analog Video Inputs

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
R_{VIN}	Input Resistance	VIN1–11	1	–	–	MΩ	Code Clamp – DAC = 0
C_{VIN}	Input Capacitance		–	5	–	pF	
V_{VIN}	Full-Scale Input Voltage		1.3	1.5	1.7	V_{PP}	min. AGC Gain
V_{VIN}	Full-Scale Input Voltage		0.4	0.5	0.6	V_{PP}	max. AGC Gain
AGC	AGC Step Width		–	3/64	–	Gain	6-Bit Resolution = 64 Steps
DNL_{AGC}	AGC Differential Non-Linearity		–	–	±0.5	LSB	f_{sig}=1MHz, – 2 dBr of max. AGC – Gain
V_{VINCL}	Input Clamping Level, CVBS		–	0.44	–	V	Binary Level = 64 LSB min. AGC Gain
Q_{CL}	Clamping DAC Resolution		–15	–	15	steps	6 Bit – I–DAC, bipolar V_{VIN} = 1.5 V
DNL_{ICL}	Clamping DAC Differential Non-Linearity		–	–	±0.5	LSB	
$I_{CL–LSB}$	Input Clamping Current per Step		–	20	–	mA	6 Bit – I–DAC, bipolar V_{VIN} = 1.5 V, @ high current clamping
BW	Bandwidth		5.5	–	9	MHz	–2 dBr input signal level, 5-bit setting
BW_{tol}	Tolerance Bandwidth		–	±23	–	%	@ one setting value
XTALK	Crosstalk, any Two Video Inputs		–	–53	–	dB	1 MHz, –2 dBr signal level
THD	Total Harmonic Distortion		–	–54	–	dB	1 MHz, 5 harmonics, –2 dBr signal level
SINAD	Signal-to-Noise and Distortion Ratio		–	47	–	dB	1 MHz, all outputs, –2 dBr signal level
INL	Integral Non-Linearity		–	–	±1	LSB	Code Density, DC-ramp @ 20 MHz sampling
DNL	Differential Non-Linearity		–	–	±0.5	LSB	
DGE	Differential Gain Error		–	–	±3	%	–12 dBr, 4.4 MHz signal on DC-ramp
DPHE	Differential Phase Error		–	–	1.5	deg	

4.6.4.13. Analog Video Outputs

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{OUT}	Output Voltage	VOUT1-3	–	1.0	–	V_{PP}	V_{VIN} = 1 V_{PP}
V_{OUTDC}	DC-Level		–	1	–	V	clamped to back porch, min. AGC for ADC path
BW	V_{OUT} Bandwidth		7	–	–	MHz	Input: −2 dBr of main ADC range, $C_L \leq 10$ pF
THD	V_{OUT} Total Harmonic Distortion		–	–50	–46	dB	Input: −2 dBr of main ADC range, $C_L \leq 10$ pF 1 MHz, 5 Harmonics
C_L	Load Capacitance		–	–	10	pF	
I_L	Output Current		–	–	±0.1	mA	

4.6.4.14. Horizontal Flyback Input

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{IL}	Input Threshold	HFLB	–1%	$V_{SUP3.3IO}$ * 0.67	+1%	V	
V_{IMAX}	Maximum Input Voltage		–	–	$V_{SUP3.3IO}$ + 0.3	V	clamping current 10 mA
V_{IHST}	Input Hysteresis		0.1	0.2	–	V	
PSRR	Power Supply Rejection Ratio		–	28	–	dB	@ 20.25 MHz, not tested, according to design

4.6.4.15. Horizontal Drive Output

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{OL}	Output Low Voltage	HOUT strong	–	–	0.1 0.7 1.5	V	I_{OL} = 5 mA I_{OL} = 30 mA I_{OL} = 50 mA
V_{OH}	Output High Voltage		$V_{SUP3.3IO}$ – 0.1 – 0.7 – 1.5	–	–	V	I_{OH} = 5 mA I_{OH} = 30 mA I_{OH} = 50 mA
t_{OT}	Output Transition Time		– –	8 20	10 35	ns ns	C_{LOAD} = 50 pF C_{LOAD} = 500 pF
I_{OH}	Output Current		–	–	50	mA	
V_{OL}	Output Low Voltage	HOUT weak	–	–	0.4 1.5	V	I_{OL} = 2mA I_{OL} = 10 mA
V_{OH}	Output High Voltage		$V_{SUP3.3IO}$ – 0.4 – 1.5	–	–	V	I_{OH} = 2 mA I_{OH} = 10 mA
t_{OT}	Output Transition Time		– –	5 15	8 20	ns ns	C_{LOAD} = 10 pF C_{LOAD} = 50 pF
I_{OH}	Output Current		–	–	10	mA	

4.6.4.16. Dynamic Focus Output

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{OL}	Output Low Voltage	DFVBL PWMV	–	–	0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage		$V_{SUP3.3IO}$ – 0.4	–	$V_{SUP3.3IO}$	V	$-I_{OL}$ = 2 mA
t_{OT}	Output Transition Time		–	10	20	ns	C_{LOAD} = 50 pF
I_{OL}	Output Current		–10	–	10	mA	

4.6.4.17. Protection Inputs

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{IA}	Input Threshold A	SAFETY VPROT	–1%	$V_{SUP3.3IO}$ * 0.85	+1%	V	
V_{IB}	Input Threshold B		–1%	$V_{SUP3.3IO}$ * 0.45	+1%	V	
V_{IMAX}	Maximum Input Voltage		–	–	$V_{SUP3.3IO}$ + 0.3	V	clamping current 10 mA
V_{IHST}	Input Hysteresis A and B		0.1	0.2	–	V	
PSRR	Power Supply Rejection Ratio		–	28	–	dB	@ 20.25 MHz, not tested, according to design

4.6.4.18. Vertical and East/West D/A Converter Output

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
	Resolution	EW VERT+ VERT-	–	15	–	bit	
V_{OMIN}	Minimum Output Voltage		–	0	–	V	R_{load} = 6.8 kΩ R_{xref} = 1 K
V_{OMAX}	Maximum Output Voltage		2.82	3	3.2	V	R_{load} = 6.8 kΩ R_{xref} = 1 K
I_{DACN}	Full-Scale DAC Output Current		415	440	465	µA	R_{xref} = 1 K
PSRR	Power Supply Rejection Ratio		–	20	–	dB	

4.6.4.19. East/West PWM Output

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{OL}	Output Low Voltage	EW	–	–	0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage		$V_{SUP5.0BE}$ – 0.4	–	$V_{SUP5.0BE}$	V	$-I_{OL}$ = 2 mA
t_{OT}	Output Transition Time		–	4	–	ns	CLOAD = 10 pF Rlp = 4.7 kΩ Clp = 100 nF

4.6.4.20. Sense A/D Converter Input

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{I511}	Input Voltage for Code 511	SENSE RSW1	–	2.6	–	V	
C_0	Digital Output for Zero Input		–	–	16	LSB	
R_I	Input Impedance		1	–	–	MΩ	
Range Switch Outputs							
R_{ON}	Output On Resistance	RSW1 RSW2	–	12	25	W	I_{OL} = 10 mA
I_{Max}	Maximum Current		–	–	15	mA	
I_{LEAK}	Leakage Current		–	–	600	nA	RSW High Impedance
C_{IN}	Input Capacitance		–	–	5	pF	

4.6.4.21. Analog RGB and FB Inputs

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
RGB Input Characteristics							
V_{RGBIN}	Absolute Maximum External RGB Inputs Voltage Range	RIN GIN BIN	–0.3	–	1.4	V	at pin
V_{RGBIN}	Nominal RGB Input Voltage Peak-to-Peak		0.5	0.7	1.0	V_{PP}	SCART Spec: 0.7 V ±3 dB
V_{RGBIN}	RGB Inputs Voltage for Maximum Output Current		–	0.5	–	V	Contrast setting: 2047
			–	0.7	–	V	Contrast setting: 1714
			–	1	–	V	Contrast setting: 1200
C_{RGBIN}	External RGB Input Coupling Capacitor		–	15	–	nF	
t_{CLP}	Clamp Pulse Width		–	3.2	–	µs	
C_{IN}	Input Capacitance		–	–	13	pF	
I_{IL}	Input Leakage Current		–0.5	–	0.5	µA	Clamping OFF, V_{IN} = –0.3...3 V
V_{CLIP}	RGB Input Voltage for Clipping Current		–	1.4	–	V	
V_{CLAMP}	Clamp Level at Input		–	0.2	–	V	Clamping ON
I_{ICMAX}	Mxximum Clamp Current during t_{CLP}		–1.5	–	1.5	mA	Clamping ON
V_{INOFF}	Offset Level at Input		–10	–	10	mV	Extrapolated from V_{IN} = 100 and 200 mV
Fast Blank Input Characteristics							
V_{FBLOFF}	Fast Blanking Low Level	FBIN	–	–	0.5	V	
V_{FBLON}	Fast Blanking High Level		0.9	–	–	V	
$V_{FBLTRIG}$	Fast Blanking Trigger Level		–	0.7	–	V	
t_{PID}	Delay Fast Blanking to RGB_{OUT} from midst of FBIN–transition to 90% of RGB_{OUT}- transition		–	8	15	ns	Internal RGB = 3.75 mA Full Scale Int. Brightness = 0 External Brightness = 1.5 mA (Full Scale) RGBin = 0 V_{FBLOFF} = 0.4 V V_{FBLON} = 1.0 V Rise and fall time = 2 ns
	Difference of Internal Delay to External RGBin Delay		–5	–	+5	ns	
	Switch-Over-Glitch		–	0.5	–	pAs	Switch from 3.75 mA (int) to 1.5 mA (ext)

4.6.4.22. D/A Converter Reference

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{DACREF}	DAC-Ref. Voltage	VRD	1.19	1.25	1.31	V	
V_{DACR}	DAC-Ref. Output Resistance		18	25	32	kΩ	
V_{XREF}	DAC-Ref. Voltage Bias Current Generation	XREF	1.14	1.21	1.28	V	R_{xref} = 1 K

4.6.4.23. Scan Velocity Modulation Output

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
	Resolution	SVMOUT	–	8	–	bit	
I_{OUT}	Full-Scale Output Current		1.55	1.875	2.25	mA	
I_{OUT}	Differential Nonlinearity		–	–	0.5	LSB	
I_{OUT}	Integral Nonlinearity		–	–	1	LSB	
I_{OUT}	Glitch Pulse Charge		–	0.5	–	pAs	Ramp, output line is terminated on both ends with 50 Ω
I_{OUT}	Rise and Fall Time		–	3	–	ns	10% to 90%, 90% to 10%

4.6.4.24. Analog RGB Outputs, D/A Converters

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Internal RGB Signal D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	10	–	bit	
I_{OUT}	Full-Scale Output Current		3.6	3.75	3.9	mA	R_{ref} = 1 K
I_{OUT}	Differential Nonlinearity		–	–	1	LSB	
I_{OUT}	Integral Nonlinearity		–	–	2	LSB	
I_{OUT}	Glitch Pulse Charge		–	0.5	–	pAs	Ramp signal, 25 Ω output termination
I_{OUT}	Rise and Fall Time		–	3	–	ns	10% to 90%, 90% to 10%
I_{OUT}	Intermodulation		–	–	–50	dB	2/2.5MHz full scale
I_{OUT}	Signal to Noise		+50	–	–	dB	Signal: 1MHz full scale Bandwidth: 10MHz
I_{OUT}	Matching R-G, R-B, G-B		–2	–	2	%	
	R/B/G Crosstalk one channel talks two channels talk		–	–	–46	dB	Passive channel: I_{OUT} = 1.88 mA Crosstalk-Signal: 1.25 MHz, 3 mA_{PP}
	RGB Input Crosstalk from external RGB one channel talks two channels talk three channels talk		 – – –	 – – –	 –50 –50 –50	 dB dB dB	
Internal RGB Brightness D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	9	–	bit	
I_{BR}	Full-Scale Output Current, relative		39.2	40	40.8	%	Ref to max. digital RGB
I_{BR}	Full-Scale Output Current, absolute		–	1.5	–	mA	
I_{BR}	Differential Nonlinearity		–	–	1	LSB	
I_{BR}	Integral Nonlinearity		–	–	2	LSB	
I_{BR}	Match R-G, R-B, G-B		–2	–	2	%	
I_{BR}	Match to digital RGB R-R, G-G, B-B		–2	–	2	%	

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
External RGB Voltage/Current Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	11	–	bit	
I_{EXOUT}	Full-Scale Output Current, relative		96	100	104	%	Ref. to max. Digital RGB V_{IN} = 0.7 V_{PP}, contrast = 1714
	Full-Scale Output Current, absolute		–	3.75	–	mA	Same as Digital RGB
CR	Contrast Adjust Range		–	0:2047	–		
	Gain Match R-G, R-B, G-B		–3	–	3	%	Measured at RGB Outputs V_{IN} = 0.7 V, contrast = 1714
	Gain Match to RGB-DACs R-R, G-G, B-B		–3	–	3	%	Measured at RGB Outputs V_{IN} = 0.7 V, contrast = 1714
	R/B/G Input Crosstalk one channel talks two channels talk		–	–	–46	dB	Passive channel: V_{IN} = 0.7V, contrast = 1714 Crosstalk signal: 1.25 MHz, 3 mA_{PP}
	RGB Input Crosstalk from Internal RGB one channel talks two channels talk tree channels talk		–	–	–50	dB	
	RGB Input Noise and Distortion		–	–	–50	dB	V_{IN} = 0.7 V_{PP} at 1 MHz contrast = 1714 Bandwidth: 10 MHz
	RGB Input Bandwidth –3 dB		–	15	–	MHz	V_{IN} = 0.7 V_{PP}, contrast = 1714
	RGB Input THD		– –	–50 –40	– –	dB dB	Input signal 1 MHz Input signal 6 MHz V_{IN} = 0.7 V_{PP} contrast = 1714
	Differential Nonlinearity of Contrast Adjust		–	–	1	LSB_{10}	V_{IN} = 0.7 V
	Integral Nonlinearity of Contrast Adjust		–	–	7	LSB_{10}	V_{IN} = 0.7 V
Analog RGB Output Pins							
V_{RGBO}	R,G,B Output Voltage	ROUT GOUT BOUT	–1.0	–	0.3	V	Referred to $V_{SUP5.0BE}$
R_{LRGB}	R,G,B Output Load Resistance		–	–	100	Ω	Ref. to $V_{SUP5.0BE}$
I_{MAX}	Maximum Output Current		–	8.25	–	mA	
External RGB Brightness D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	9	–	bit	
I_{EXBR}	Full-Scale Output Current, relative		39.2	40	40.8	%	Ref to max. digital RGB
	Full-Scale Output Current absolute		–	1.5	–	mA	
	Differential Nonlinearity		–	–	1	LSB	
	Integral Nonlinearity		–	–	2	LSB	
	Matching R-G, R-B, G-B		–2	–	2	%	
	Matching to digital RGB R-R, G-G, B-B		–2	–	2	%	

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
RGB Output Cutoff D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	9	–	bit	
I_{CUT}	Full-Scale Output Current, relative		58.8	60	61.2	%	Ref to max. digital RGB
	Full-Scale Output Current absolute		–	2.25	–	mA	
	Differential Nonlinearity		–	–	1	LSB	
	Integral Nonlinearity		–	–	2	LSB	
	Matching to digital RGB R-R, G-G, B-B		–2	–	2	%	
RGB Output Ultrablack D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	1	–	bit	
I_{UB}	Full-Scale Output Current, relative		19.6	20	20.4	%	Ref to max. digital RGB
	Full-Scale Output Current, absolute		–	0.75	–	mA	
	Match to digital RGB R–R, G–G, B–B		–2	–	2	%	

4.6.4.25. CADC Input Port

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
VREF	CADC Comparator Reference Voltage	Px.y	–	$V_{SUP3.3IO}$	–	V	
LSB	LSB Value		–	$V_{SUP3.3IO}$ /256	–	V	
R	Conversion Range		GND	–	$V_{SUP3.3IO}$	V	
A	Conversion Result		–	INT (V_{P1x}/ LSB)	–	hex	GND < V_{P1x} < VSUP3.3IO
			00	–	–	hex	$V_{P1x} \leq$ GND
			–	–	FF	hex	$V_{P1x} \geq$ VSUP3.3IO
tc	Conversion Time		–	10	–	µs	
ts	Sample Time		–	2	–	µs	
TUE	Total Unadjusted Error		–6	–	6	LSB	
DNL	Differential Non-Linearity		–3	–	3	LSB	
Ci	Input Capacitance during Sampling Period		–	15	–	pF	
Ri	Serial Input Resistance during Sampling Period		–	5	–	kΩ	

4.6.4.26. I/O Ports

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{OL}	Output Low Voltage	P1x P2x P3x	–	–	0.4 1.5	V	I_{OL} = 2 mA I_{OL} = 10 mA
V_{OH}	Output High Voltage		$V_{SUP3.3IO}$ –0.4 $V_{SUP3.3IO}$ –1.5	–	–	V	I_{OH} = –2 mA $I_{O\,H}$= –10 mA
V_{IL}	Input Low Voltage		–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
Ii	Input Leakage Current		–1.0	–	1.0	µA	0 < Vi < VSUP3.3IO

4.6.4.27. Memory Interface

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
V_{OL}	Output Low Voltage	ADB[19-0] DB[7:0] WRQ RDQ PSENQ PSWEQ ALE OCF RSTQ	–	–	0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage		$V_{SUP3.3IO}$ –0.4	–	–	V	I_{OH} = –2 mA
V_{IL}	Input Low Voltage	DB[7:0] STOPQ ENEQ XROMQ EXTIFQ RSTQ	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
Ii	Input Leakage Current		–1.0	–	1.0	µA	0 < Vi < VSUP3.3IO

4.6.4.28. Memory Interface Timing

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
t_{CYCD}	Data Read/Write Cycle Time		–	296	–	ns	C_L = 50 pF
t_{CYCP}	Program Read Cycle Time		–	148	–	ns	
t_{ALS}	Address Latch Setup Time	ALE	15	25	–	ns	
t_{ALH}	Address Latch Hold Time		15	25	–	ns	
t_{AWS}	Address Data Write Setup Time	ADB[19–0]	89	99	–	ns	
t_{ARS}	Address Data Read Setup Time		89	99	–	ns	
t_{APS}	Address Program Read Setup Time		39	49	–	ns	
t_{AADR}	Address Access Data Read Time		–	150	193	ns	see ext. SRAM spec
t_{AAPR}	Address Access Program Read Time		–	90	94	ns	see ext. FLASH spec
t_{DWS}	Data Write Setup Time	DB[7:0]	128	148	–	ns	C_L = 50 pF
t_{DWH}	Data Write Hold Time		5	25	45	ns	
t_{OEDR}	Output Enable Data Read Time		–	90	94	ns	see ext. SRAM spec
t_{DRS}	Data Read Setup Time		54	–	–	ns	C_L = 50 pF
t_{DRH}	Data Read Hold Time		0	0	25	ns	
t_{OEPR}	Output Enable Program Read Time		0	45	45	ns	see ext. FLASH spec
t_{PRS}	Program Read Setup Time		29	–	–	ns	C_L = 50 pF
t_{PRH}	Program Read Hold Time		0	0	25	ns	
t_{WW}	Write Enable Pulse Width	WRQ PSWEQ	138	148	–	ns	
t_{RW}	Read Enable Pulse Width	RDQ	138	148	–	ns	
t_{PW}	Program Read Enable Pulse Width	PSENQ	64	74	–	ns	

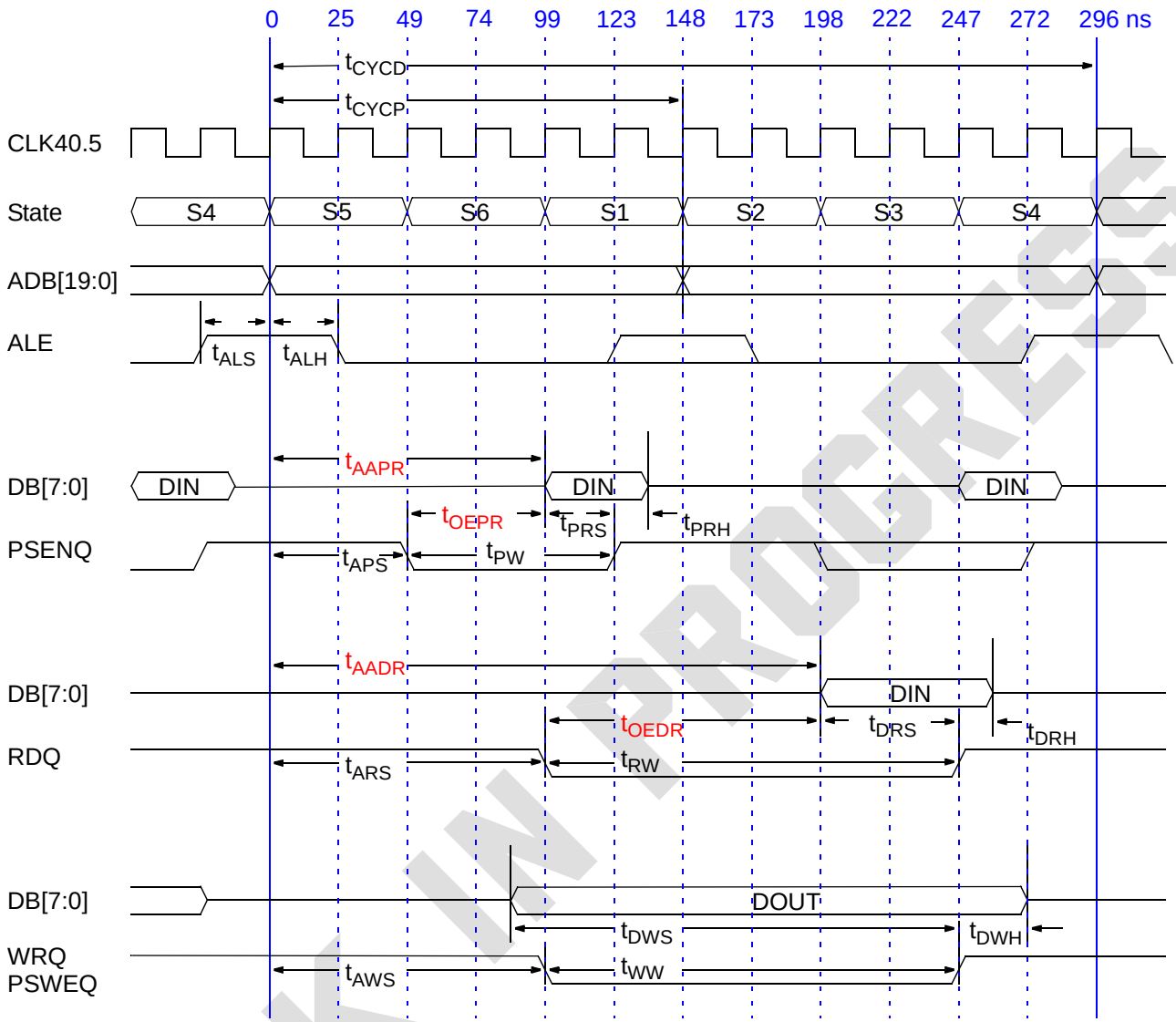


Fig. 4–39: Memory Interface Timing

5. Application

The following circuit diagrams show the design of the COSIMA-2 (Cost Optimized Singlescan Multistandard Application) reference TV set using VCT 49xyl, VCT 48xyl.

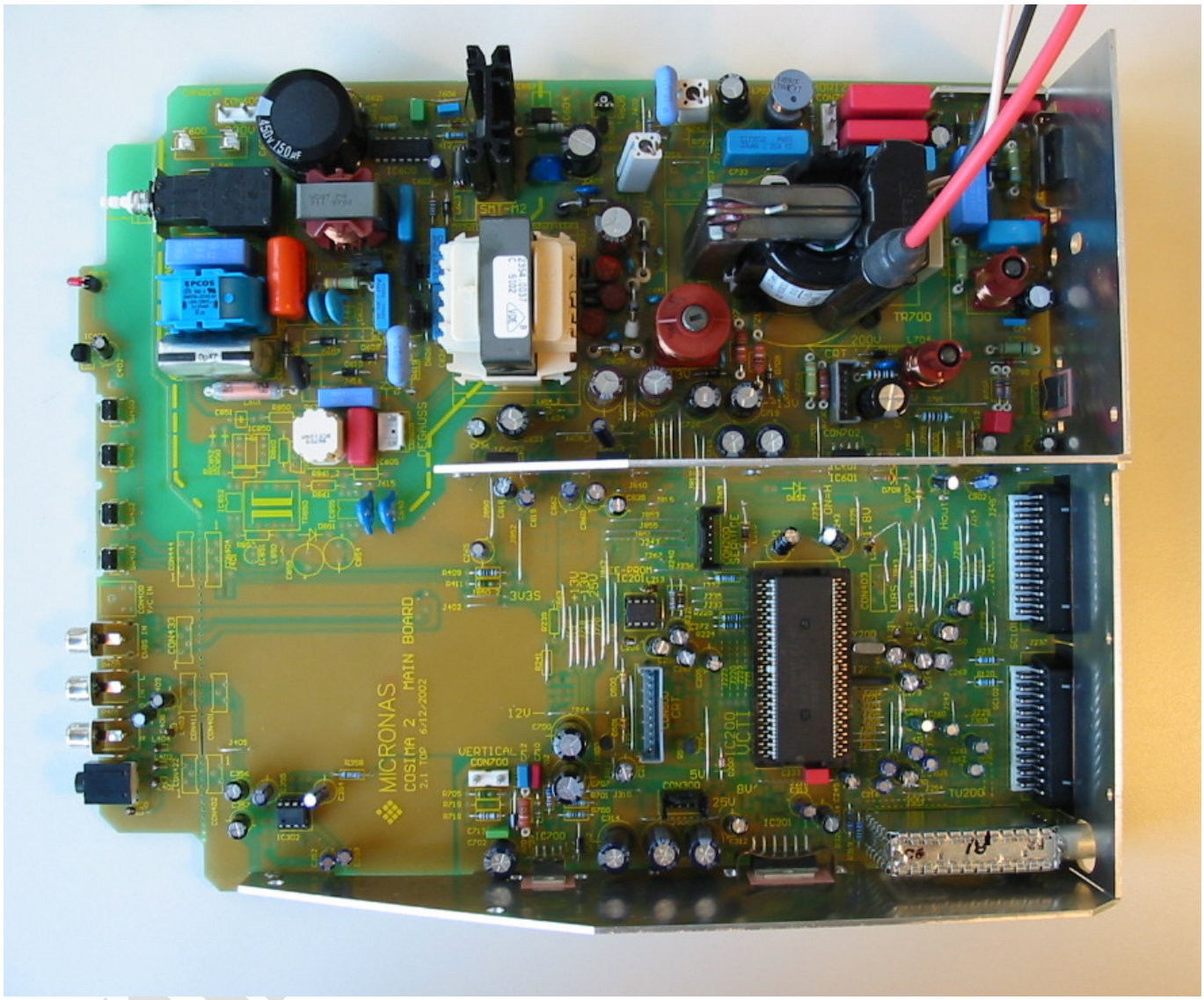


Fig. 5–1: COSIMA-2 TV chassis

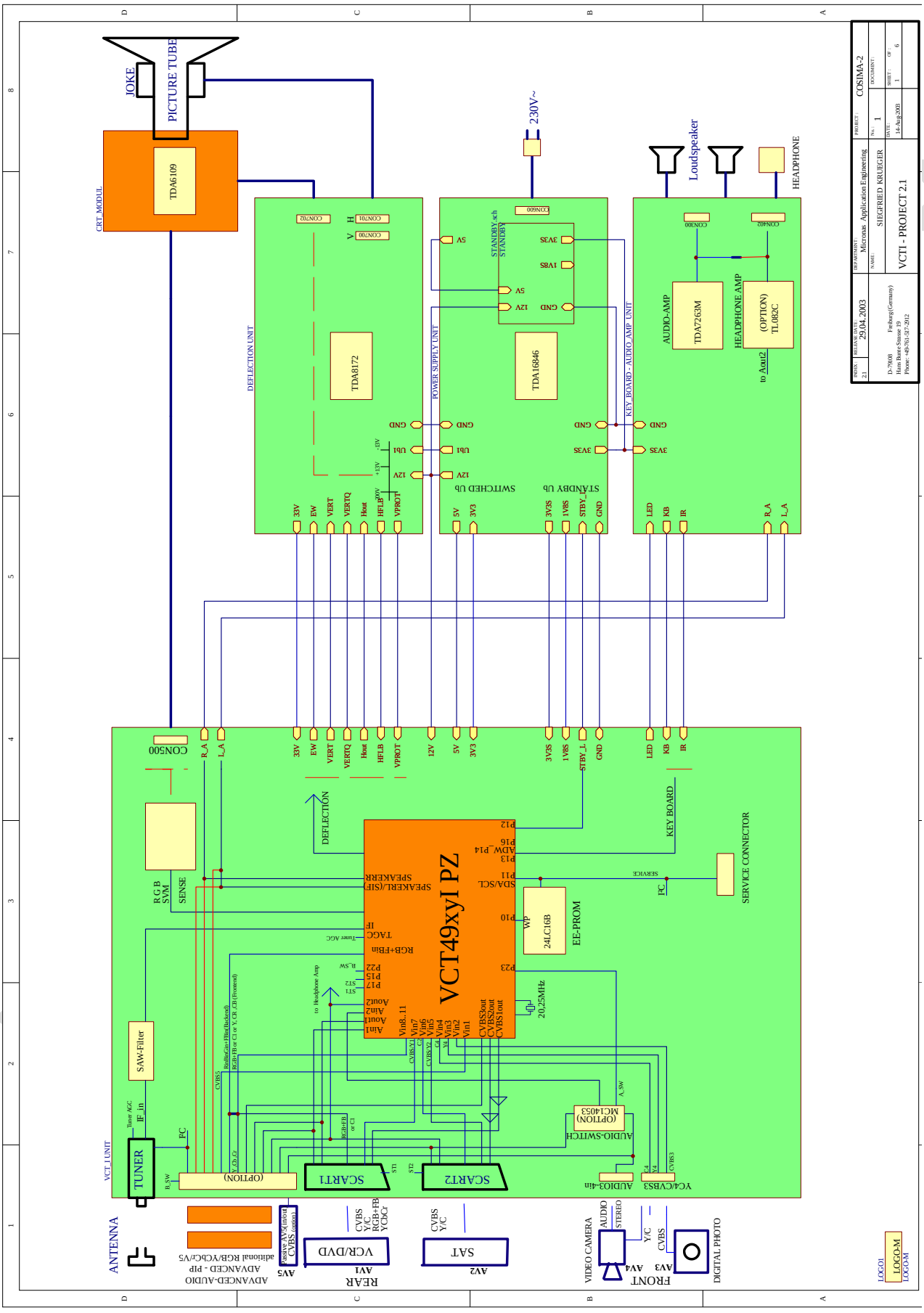


Fig. 5–2: 21" Reference TV with VCT 49xyl, VCT 48xyl

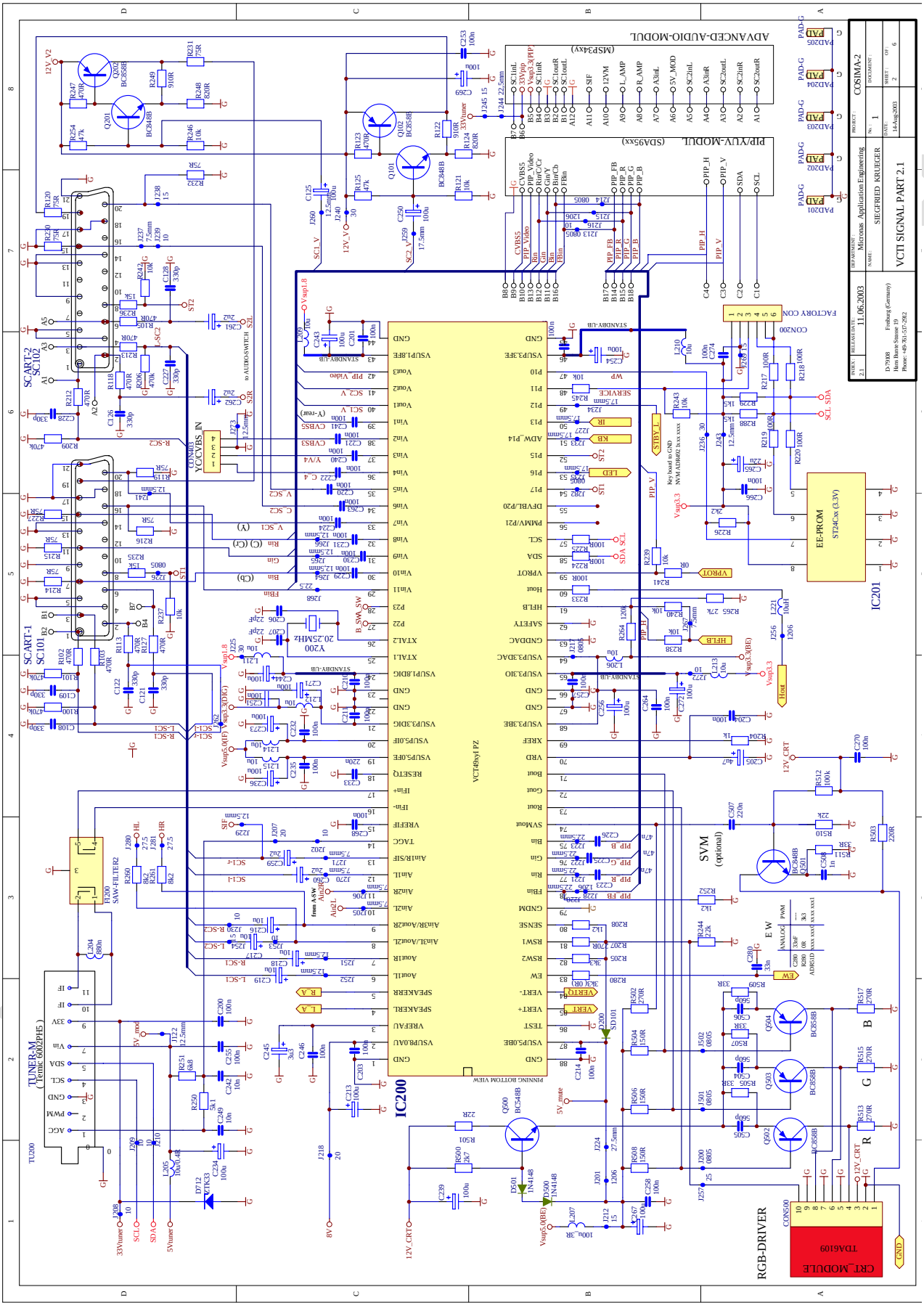


Fig. 5–3: 21” Reference TV with VCT 49xyl, VCT 48xyl

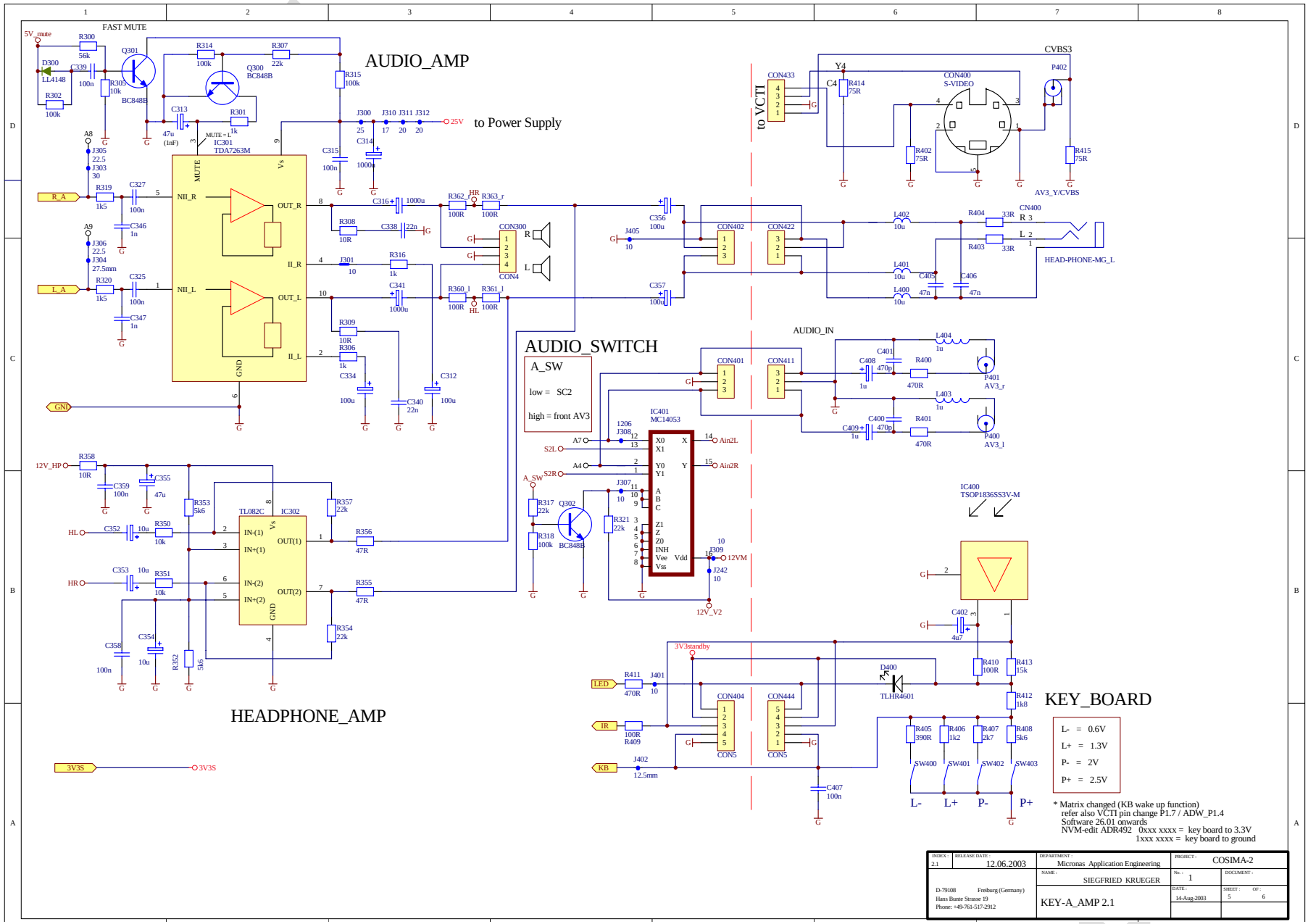


Fig. 5–4: 21” Reference TV with VCT 49xyl, VCT 48xyl

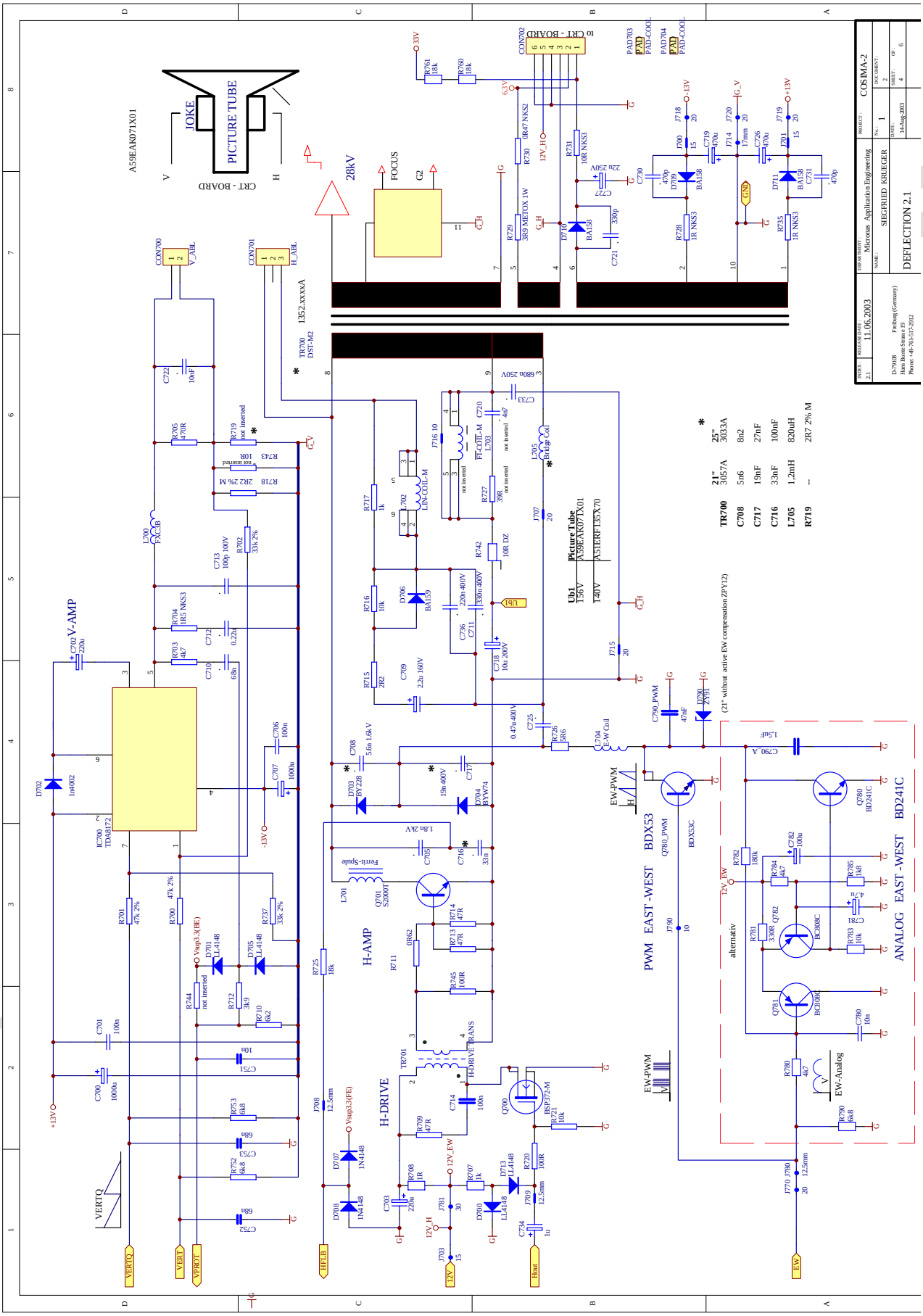


Fig. 5–5: 21" Reference TV with VCT 49xyl, VCT 48xyl

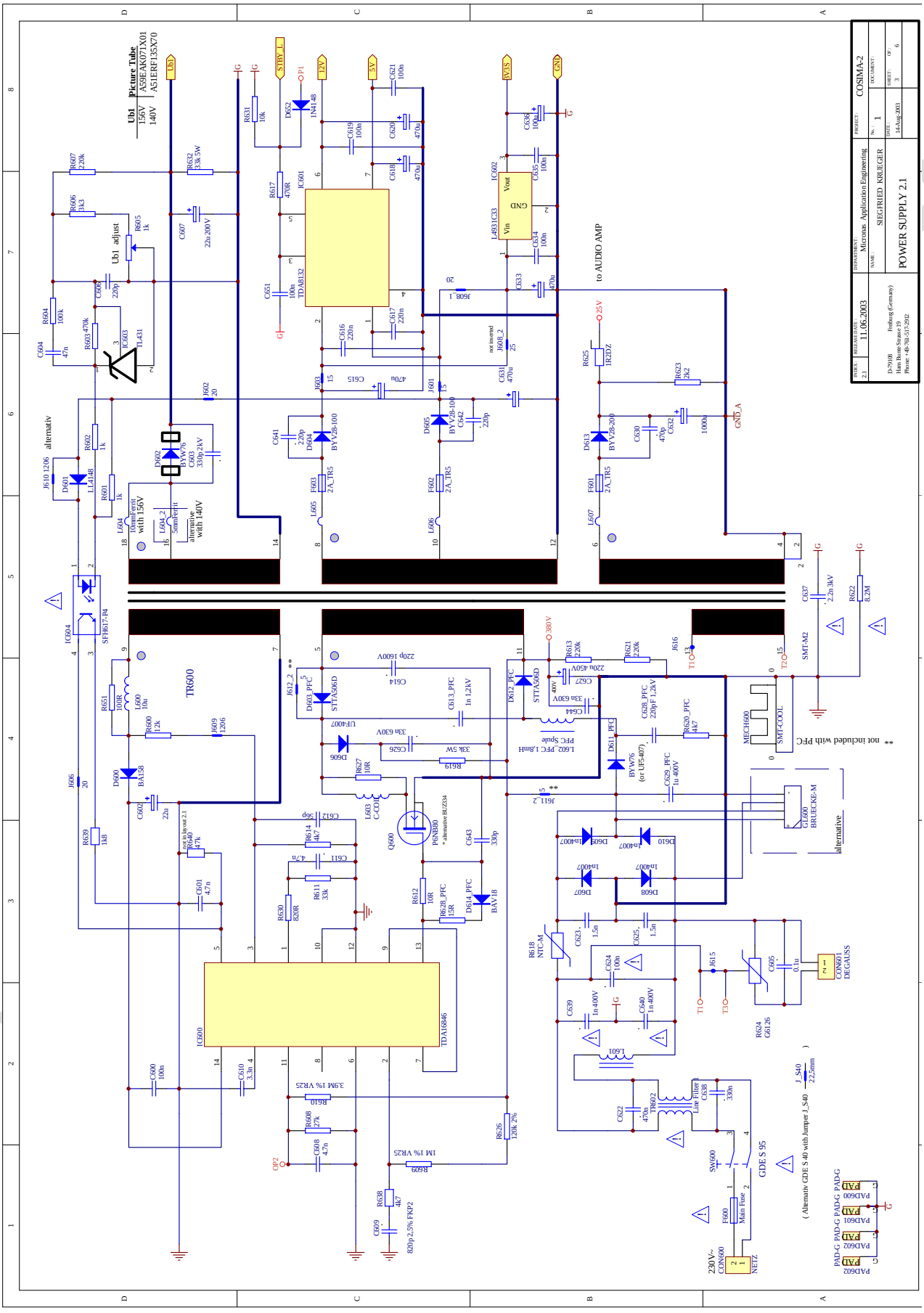


Fig. 5–6: 21" Reference TV with VCT 49xyl, VCT 48xyl

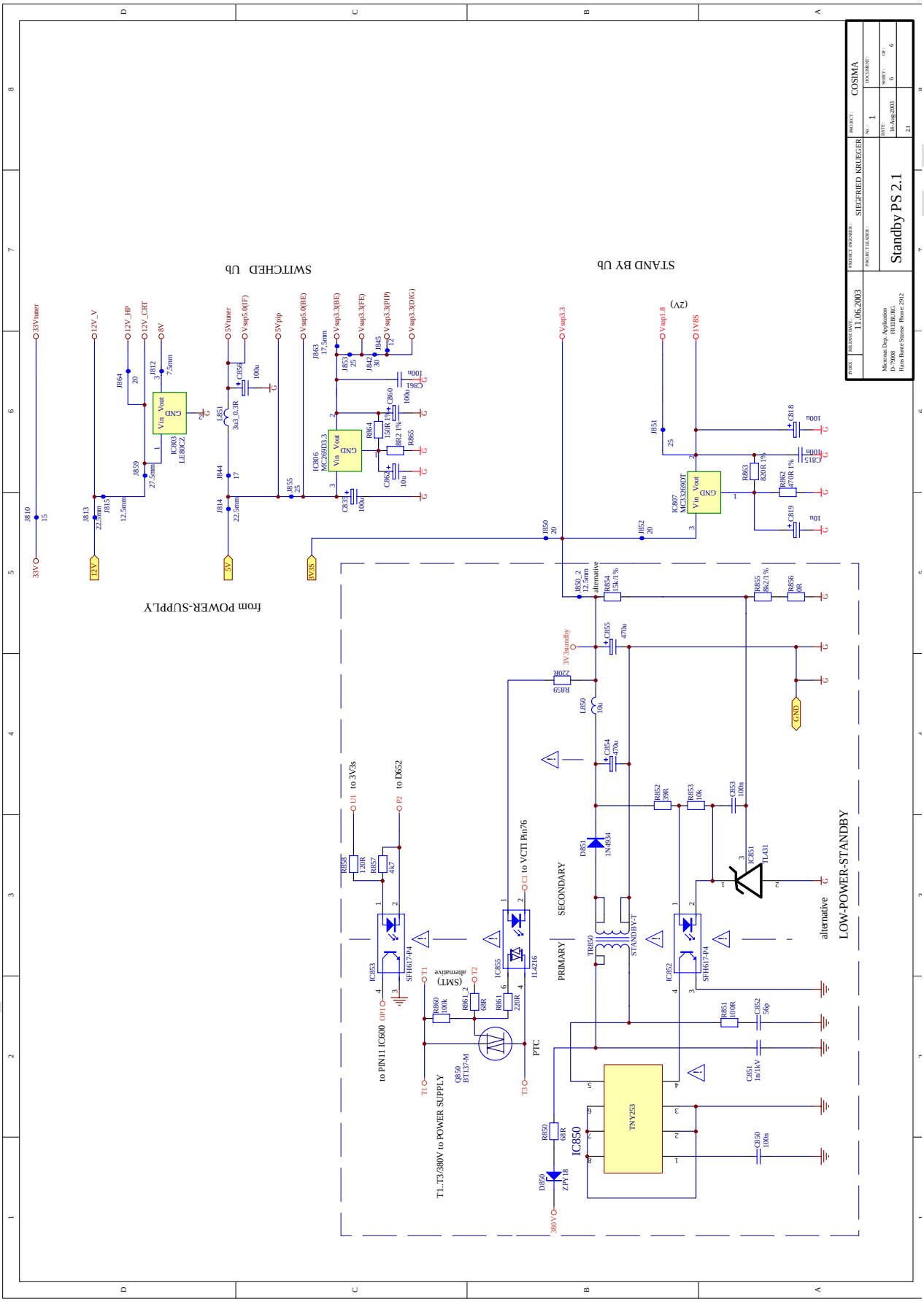


Fig. 5–7: 21" Reference TV with VCT 49xyl, VCT 48xyl

6. Data Sheet History

1. Advance Information: “VCT 49xyl, VCT 48xyl General Description”, 12.12.2003, 6251-573-1-1AI. First release of the advance information.

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ADVANCE INFORMATION

VCT 49xyI, VCT 48xyI

Volume 2:
DRX - Analog TV IF-Demodulator

Edition Dec. 12, 2003
6251-573-2-1AI

MICRONAS

Contents

Volume 2: DRX - Analog TV IF- Demodulator

1. Introduction

Volume 2 describes the DRX - Analog TV IF- Demodulator of VCT 49xyI, VCT 48xyI.

1.1. Chip Architecture

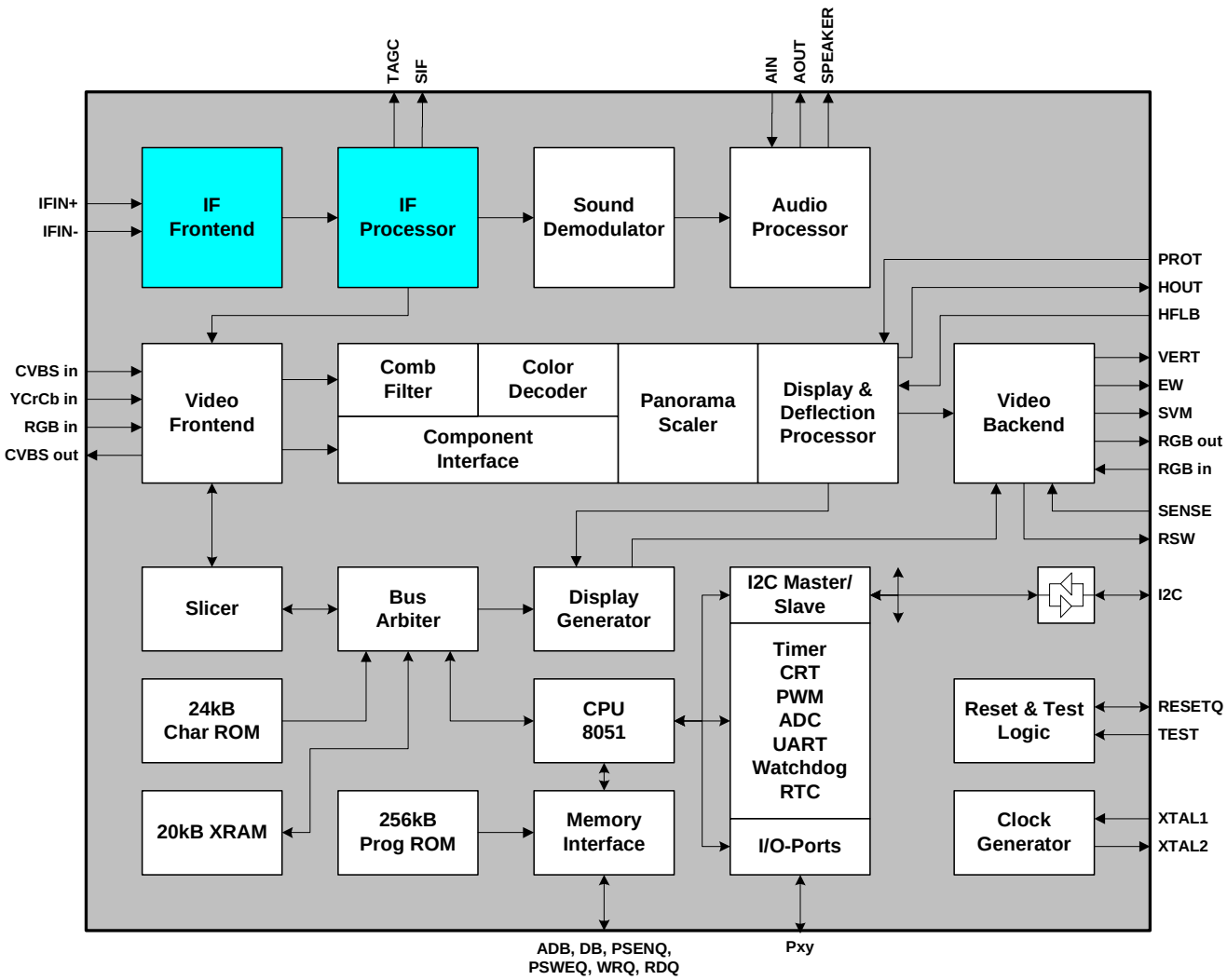


Fig. 1–1: Block diagram of the VCT 49xyI, VCT 48xyI highlighting the DRX Parts

1.2. Features

- Multistandard QSS IF processing with a single SAW
- Highly reduced amount of external components (no tank circuit, no potentiometers, no SAW switching)
- Programmable IF frequency (38.9 MHz, 45.75 MHz, 32.9 MHz, 58.75 MHz, 36.125 MHz etc.)
- Digital IF processing for the following standards: B/G, D/K, I, L/L', and M/N
- Standard specific digital post filtering
- Standard specific digital video/audio splitting
- Standard specific digital picture carrier recovery:
  - alignment-free
  - quartz-stable and accurate
  - stable frequency lock at 100% modulation and overmodulation up to 150%
  - quartz-accurate AFC information
- Programmable standard specific digital group delay equalization
- Automatically frequency-adjusted Nyquist slope, therefore optimal picture and sound performance

over complete lock in frequency range

- Standard-specific digital AGC and delayed tuner AGC with programmable tuner Take Over Point
- Fast AGC due to linear structure
- Adaptive back porch control, therefore fast positive modulation AGC
- No sound traps needed at video output
- Second SIF output with standard dependent pre-filtering and amplitude controlled output level
- Optimal sound SNR due to carrier recovery without quadrature distortions
- FM radio capability without external components and with standard TV tuner
- I^2C bus interface

1.3. Overview

The DRX - Analog TV IF- Demodulator performs the entire multistandard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, and generation of the second sound IF (SIF) requiring only one SAW filter.

The alignment-free DRX does not need special external components. All control functions and status registers are accessible via I^2C bus interface. Therefore, it simplifies the design of high-quality, highly standardized IF stages.

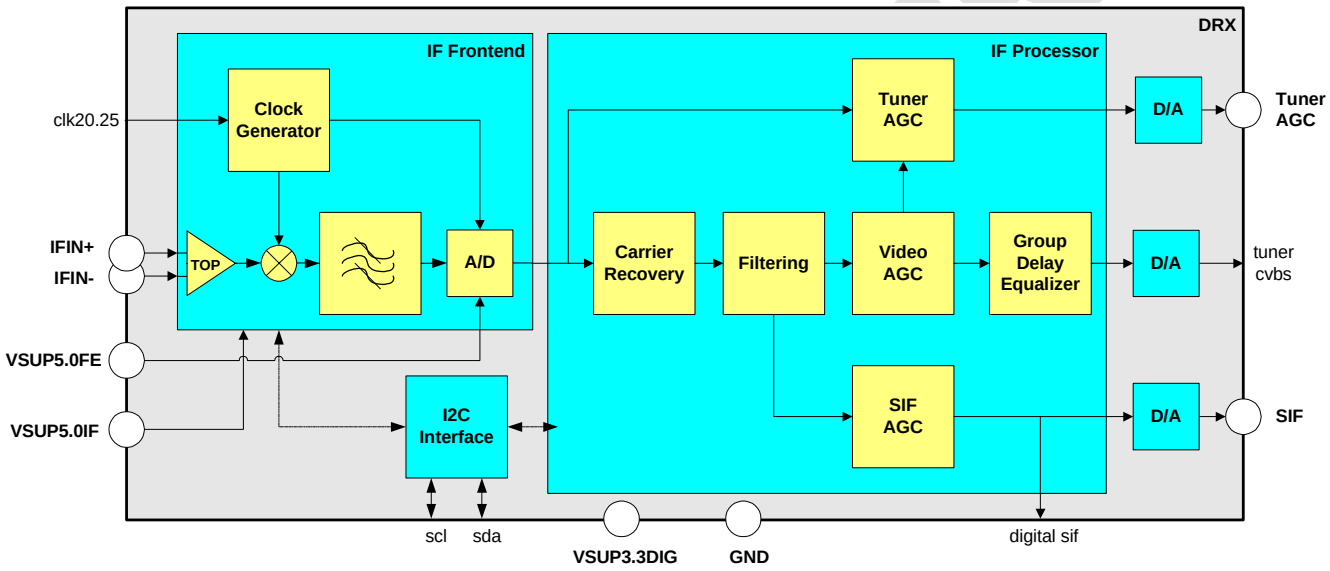


Fig. 1–2: Block diagram of the DRX

1.4. Analog TV Application

The DRX is able to replace a conventional IF IC including several SAWs. Nevertheless, quasi split sound processing is performed with standard specific internal filtering and group delay equalizing.

The input signal of the DRX is the TV IF with its carrier at:

- 38.9 MHz (B/G, D/K, I, L, and M/N in multistandard applications)
- 32.9 MHz (L')
- 45.75 MHz (M/N in US applications)
- 58.75 MHz (M/N in Japan applications)
- other frequencies are also programmable
- 36.125 MHz (DVB-C or DVB-T in further versions)

These signals are available from conventional tuners.

1.4.1. SAW Filter

For pre-filtering, **one** 8-MHz channel SAW filter must be used, e.g. the Epcos X6897D (recommended), X6874D or the X6966M. Nevertheless, the entire multistandard processing is performed. The prefilter limits the signal bandwidth to 8 MHz and suppresses major parts of the adjacent channels.

1.4.2. Processing Overview

After the desired standard information is transferred into the DRX, the following standard specific procedures are performed:

- Analog down mixing to 2nd IF

- Adjacent channel suppression
- Analog-to-digital-conversion
- Carrier locking including AFC information generation
- Nyquist slope adjustment
- Video/sound splitting
- Video AGC, including delayed tuner AGC
- Group delay equalization
- Video and sound frequency shaping
- Video demodulation
- Second SIF generation and AGC

Similar to conventional analog frontends, the tuner gain is controlled by the DRX. New AGC algorithms have been implemented for superior level tracking for both positive and negative video modulation.

The demodulated CVBS signal and the second sound IF (SIF) are externally available as analog output signals.

1.4.3. Initialization for Analog TV

The standard to be processed has to be set via I^2C bus.

Additional controlling is only needed if the default values for the remaining write registers are not applicable.

1.4.4. Multistandard Configuration for B/G, L, I, D/K and M/N

In multistandard applications for B/G, L, I, D/K, and M/N, the picture carrier frequency at the tuner output should be 38.9 MHz. The sound carrier frequencies are below in a distance corresponding to the transmission standard. Thus, all wanted channel components are within the passband of the SAW and forwarded to the DRX.

The demodulated and filtered video signal will be available at the CVBS output and the down-converted sound carriers will be available in digital form for the internal MSP-processing and in analog form at the SIF output pin.

1.4.5. Multistandard Configuration for L'

In the L-standard, the band-1 channels (40 MHz to 65 MHz) have a different frequency configuration. Their sound carriers are below the according picture carrier. This sub-standard is called L'. In that case, the picture carrier frequency at the tuner output should be 32.9 MHz. Using conventional tuners, the sound carrier frequencies in L' at the tuner output are above the picture carrier. All desired channel components are thus within the passband of the SAW.

1.5. FM Radio

In FM radio applications, the tuner has to convert the wanted FM Radio signal down to 32.4 MHz. Therefore, the lower slope of the SAW frequency response rejects adjacent carriers on one side of that channel. The DRX further converts the wanted FM Radio signal down to 7.7 MHz. The frequency has been chosen according to the standard selection of the Micronas Multistandard Sound Processor.
After additional digital FM radio specific filtering, the signal is fed to the 2nd SIF output.

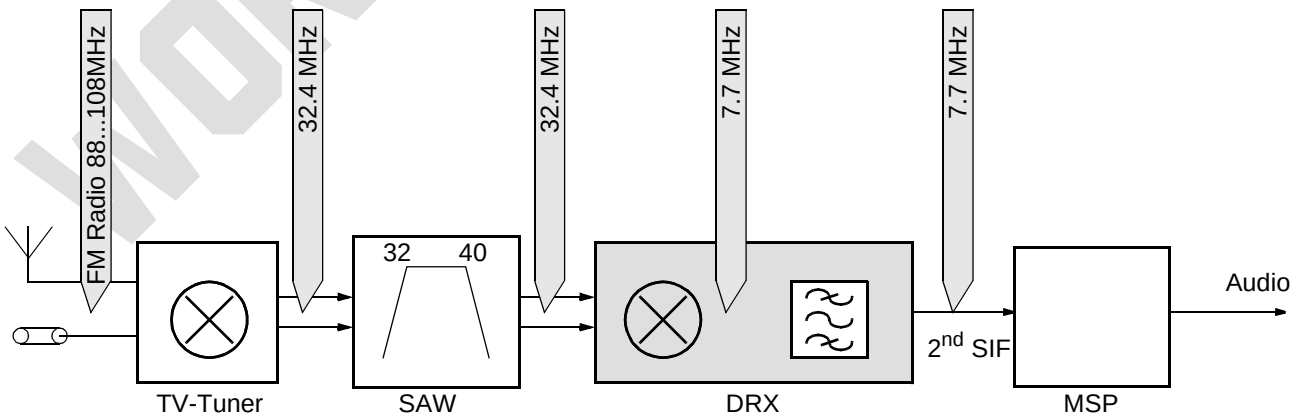


Fig. 1–1: FM Radio processing with VCTI

1.6. Using DRX with an IF frequency other than 38.9 MHz

Internally, the DRX mixes the wanted picture carrier down to a frequency that corresponds to the typical channel raster of the selected standard, e.g. 7 MHz for B, 8 MHz for G, D/K, I, L and L', and 6 MHz for M/N. This is performed using a PLL (later called LO-PLL) that is set to a frequency corresponding to the IF frequency minus the above-mentioned channel raster. Only for L', the situation is different, since the default IF is 32.9 MHz and the mixing frequency must be 8 MHz higher than the picture carrier frequency. The reason for this is the mirrored RF spectrum of L'.

Table 1–1: Default settings of LO_PLL in MHz

TV standard	Channel width	Default LO-PLL
B	7	31.9
G, D/K, I, L	8	30.9
L' (IF=32.9)	8	40.9
M/N	6	32.9

Generally, the DRX can handle any IF input frequency that lies in the range of 30 to 60 MHz. This is achieved by setting the frequency of the LO-PLL so that the resulting mixing frequency again corresponds to the standard specific channel raster. The default IF frequency after reset and after every STANDARD_SEL register change, however, is 38.9 MHz.

1.6.1. I²C settings

The frequency of the LO-PLL can be adjusted via the I²C register 0x1022 (IF_FREQ). The entered value corresponds to the desired frequency divided by 100.24 kHz. For instance, to set the LO_PLL to 39.8 MHz, the value 397 must be entered.

This setting must be made **after every** STANDARD_SEL setting, since changing the TV standard resets IF_FREQ to the default value.

Table 1–2: IF_FREQ register values

TV Std.	Setting for 38.0 MHz	Setting for 45.75 MHz	Setting for 58.75 MHz
B G	310 (0x136) 300 (0x12C)	not recommended	
D/K, I, L, L'	not recommended		

Table 1–2: IF_FREQ register values

TV Std.	Setting for 38.0 MHz	Setting for 45.75 MHz	Setting for 58.75 MHz
M/N	320 (0x140)	397 (0x18D)	526 (0x20E)
SAW type*	X6894	X6964	X6989

*: example SAW types

The values labeled "not recommended" are due to restrictions of available SAW filters.

Example 1: Set M/N standard with 45.75 MHz IF

```
<0x82 0x10 0x00 0x20 0x00 0x02> 'std.M/N
<0x82 0x10 0x10 0x22 0x01 0x8D> 'IF_FREQ
```

Example 2: Set B standard with 38.0 MHz IF

```
<0x82 0x10 0x00 0x20 0x01 0x03> 'std.B
<0x82 0x10 0x10 0x22 0x01 0x36> 'IF_FREQ
```

Example 3: Set L standard with 38.9 MHz IF

```
<0x82 0x10 0x00 0x20 0x00 0x09> 'std.L
```
(no IF_FREQ setting necessary)

1.6.2. SAW filter considerations

A bandpass SAW filter that matches the chosen IF frequency must be used. Care must be taken that for all standards to be processed, both picture and sound carrier lie within the passband range of the SAW.

Using the X6966M SAW filter at 38.0 MHz, with standards that have a 6.5 MHz sound carrier, causes problems since the sound carrier then lies at 31.5 MHz. This is in the transition area between passband and stopband. In these cases, only NICAM reception at 5.85 MHz works without problems. For I standard, however, the situation is reversed: 6.0 MHz are just inside the passband but NICAM at 6.55 MHz are not. For 38.0 MHz applications filters like EPCOS X6894D are recommended.

It is not recommended to use 45.75 MHz or 58.75 MHz with any other standard than M/N, for on one hand, the available bandpass SAW filters like X6964 or X6989 have only 6 MHz passband range, on the other hand, these IF frequencies are commonly used only with M/N standards anyway.

2. Functional Description

2.1. Input Amplifier with TOP Setting

The first block of the DRX is a low-noise preamplifier. It has a setable gain between 0 and 20 dB for setting the Tuner take Over Point voltage (TOP). This adjustment is responsible for optimal tuner operation.

Note: The TOP is the tuner input voltage at which the IF circuit (e.g. the DRX) begins to reduce the tuner gain. Thus, above this voltage the tuner output voltage remains nearly constant.

Of course, the gain of the tuner is only allowed to be reduced if the S/N is sufficiently high. A level of 60...70 dBµV at the antenna input is a typical value.

On the other hand, the output voltage of the tuner has to be limited to prevent the tuner from generating intermodulation. 105...110 dBµV is a common range for the maximum tuner output level. Hence, with a tuner gain of 35...45 dB the input voltage requirement (60...70 dB µV) is achieved automatically.

As the DRX is able to measure the tuner output voltage very accurately, the desired maximum tuner output voltage can be set with **TOP_SET_BS[3:0]**.

The values in Table 2–1 refer to the wanted channel. A headroom for adjacent channels which may have higher levels, must be taken into account.

No production alignment is needed and the setting is not affected by temperature or aging.

Table 2–1: TOP setting (for 21 dB SAW insertion loss)

TOP	Tuner Output Voltage [dBµV]
0	115
1	113.7
2	112.3
3	111
4	109.7
5	108.3
6	107
7	105.7
8	104.3
9	103
10	101.7
11	100.3
12	99
13	97.7
14	96.3
15	95

2.2. Down Mixer Synthesizer

To reduce the level of the adjacent picture carrier PC_{adj} the input signal is mixed with that frequency. Thus, the PC_{adj} is down-converted to DC were it can easily be filtered out by a highpass. Additionally, the signal frequencies are down-converted to a frequency range where the ADC has better SINAD performance.

To generate the down-mixing frequency, a synthesizer is implemented on chip. It has to generate the PC_{adj} of the according standard. In general the PC_{adj} lies below the desired IF signal, but in L' standard this frequency is higher. Thus, mirroring the spectrum in L' standard is also performed by this processing step.
At the internal second IF, the wanted picture carrier PC_{wanted} always has the same frequency as the channel bandwidth of the actual standard.

2.3. ADC

A 10-bit Analog-to-Digital Converter (ADC) transfers the analog signal into the digital domain at a sampling rate of 40.5 MHz. To fulfill the high linearity requirements, a self-adjustment procedure has been implemented. It is activated automatically 150 ms after Power-On Reset (POR) and lasts 1 ms. Additionally it can be activated at any time, for example during channel change. While the self-adjustment is active, the output signals are not valid.

2.4. Carrier Recovery

A digital PLL performs the tracking of the picture carrier and therefore synchronous demodulation.

The lock in range refers to the desired IF frequency which is chosen according to the programmed TV standard (e.g. 32.9 MHz at L' or 38.9 MHz at all other standards).

The PLL incorporates its own AFC function and provides the frequency offset from the desired IF frequency for external use (AFC_DEV). A special digital validation algorithm allows long frequency lock at 100% modulation. Additionally, the PLL aligns the digitally calculated Nyquist slope to the picture carrier frequency.

The proportional, integral and differential gain of the loop (CR_P, CR_I, CR_F) can be set via I²C; but the default values are optimized and should remain unchanged. To optimize the PLL performance at signals from transmitters with high modulator imbalance it can be switched off during low carrier periods (CR_AMP_TH). The threshold up to which overmodulation is accepted can be set, too (CR_OVM_TH). For more details, please refer to the register definition.

Due to its digital implementation, the carrier recovery is absolutely offset-free, alignment-free, drift-free, and quartz-accurate.

2.5. Channel Filtering and Audio/Video Splitting

According to the selected standard, channel filtering (suppression of not wanted signals) is performed internally by digital filters. These filters additionally separate the video and sound components of the desired channel and transfer them to the according output. The processing is competitive to conventional QSS systems.

2.6. Video and Tuner AGC

The video AGC controls the CVBS amplitude to a given value (VID_AMP). This value may be set via I²C bus.

In positive modulation mode, an adaptive back porch control (BPC) is activated. If the detected BP reference is higher than 38% of the CVBS amplitude, or lower than 17%, it is set to the according limit.

If the video AGC gain is too low, the tuner AGC increases its output current. Thus, the tuner reduces its gain.

The current gain value of both AGCs can be read out (VID_GAIN, TAGC_I) as information about the input signal strength.

The current loop gains (AGC_KI, TAGC_KI) of the video and tuner AGC influence the velocity of the AGCs and can be read via I²C. They are changed by the internal controlling. Thus, writing these values is not allowed. But, two control registers are available (TAGC_REDUCE, VAGC_REDUCE) to lower the loop gains in principle.

In case of ADC range overflow due to very strong adjacent channels, the tuner gain is reduced, too (TAGC_HR).

2.7. Group Delay Equalizing

The group delay is set to compensate the pre-distortion of the transmitter. Additionally, the standard settings can be changed by means of four coefficients to optimize the complete signal path (EQU_0, EQU_1, EQU_2, EQU_3).

2.8. Peaking

To shape the frequency response, a peaking filter is implemented. The following figure indicates the possible frequency responses:

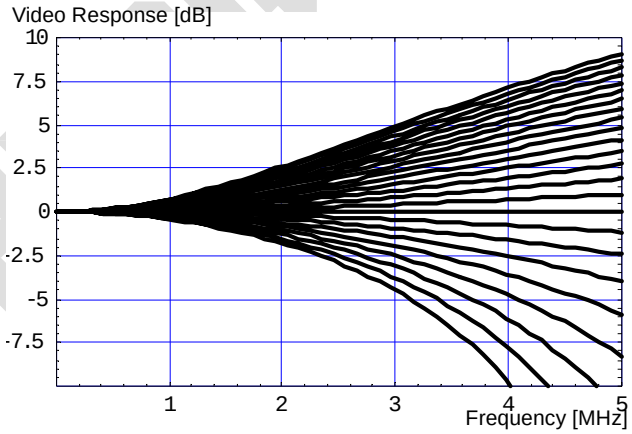


Fig. 2–1: Peaking filter frequency response

The peaking value is setable via I²C (VID_PEAK).

2.9. Video Output

A standard video DAC is used to generate the analog video (CVBS) output signal. Due to the internal filtering no sound traps are needed.

The DAC is clocked with an internally generated 40.5-MHz signal.

2.10.SIF AGC

The SIF AGC controls the level of the sound carrier output. Four different reference amplitude values are available (SIF_REF). The current gain (SIF_GAIN) can be read out and set via I²C.

According to the standard, the time constant is switched to FM/NICAM (fast AGC) or AM (slow AGC).

2.11.SIF Output

A standard video DAC is used to generate the analog SIF output signal. Due to the internal filtering no video traps are needed.

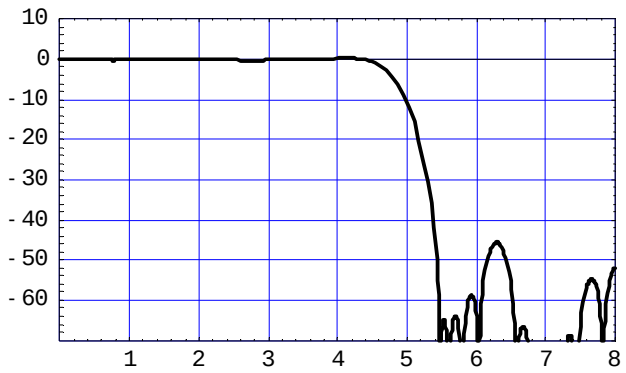
The DAC is clocked with an internally generated 40.5 MHz signal. No aliasing will occur if the SIF signal is sampled by a Micronas audio processor MSP 34xy or MSP 44xy.

2.12.Standard Specific Filter Curves

The external SAW only preforms a coarse attenuation of major parts of adjacent channels. The main filtering is done by means of the DSP. The following figures indicate the overall filter curves of the DRX including the SAW.

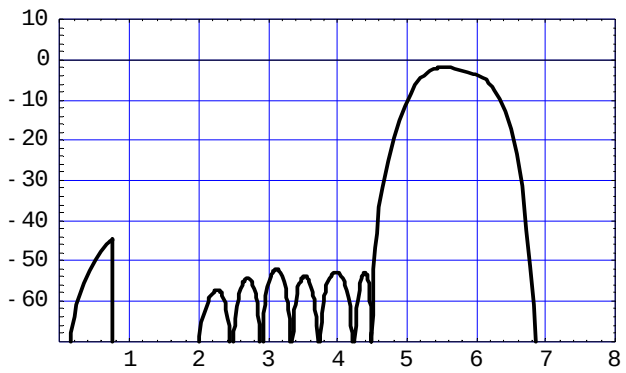
2.12.1.Standard B

Video Response [dB]



Frequency [MHz]

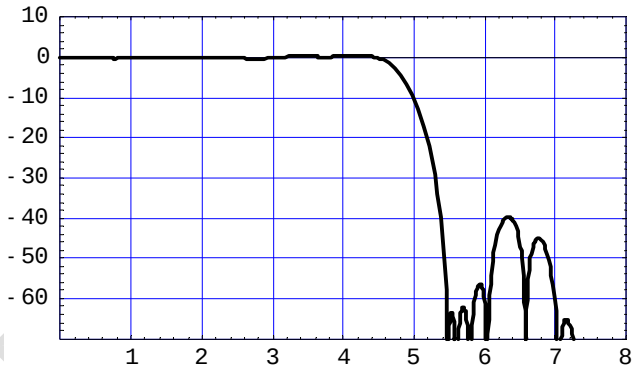
SIF Response [dB]



Frequency [MHz]

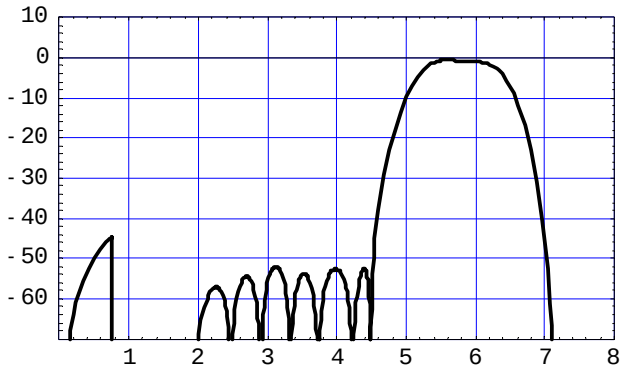
2.12.2.Standard G

Video Response [dB]



Frequency [MHz]

SIF Response [dB]



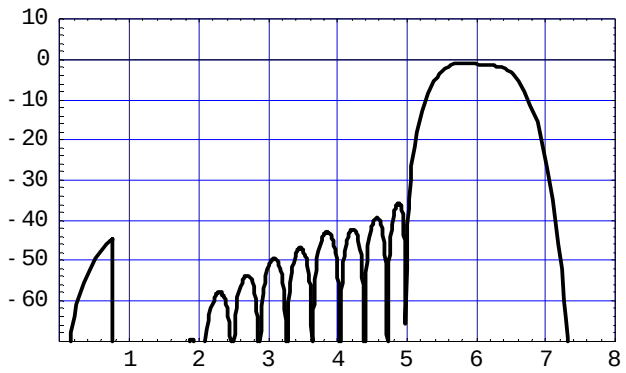
Frequency [MHz]

2.12.3.Standard D/K, I, L/L'

Video Response [dB]

Frequency [MHz]

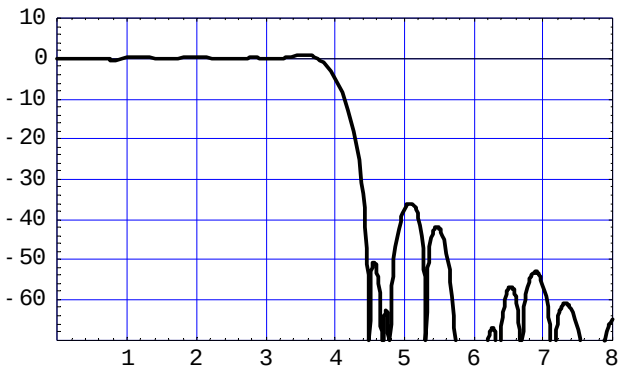
SIF Response [dB]



Frequency [MHz]

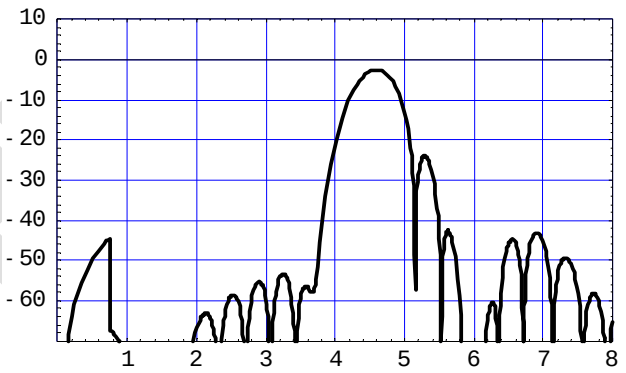
2.12.4.Standard M/N

Video Response [dB]



Frequency [MHz]

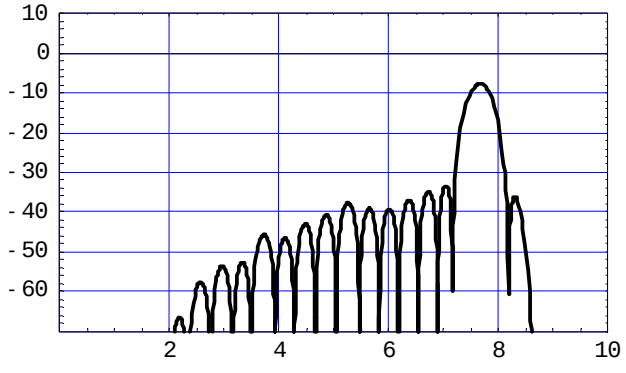
SIF Response [dB]



Frequency [MHz]

2.12.5.Standard FM

SIF Response [dB]



Frequency [MHz]

3. Control Interface

3.1. I2C Bus Interface

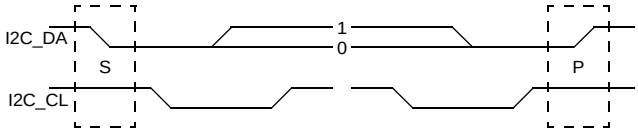


Fig. 3–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

3.1.1. Device and Subaddresses

The DRX is controlled via the I^2C bus slave interface. The DRX is selected by transmitting its device address. A device address pair is defined as a write address and a read address.

Table 3–1: I^2C Bus Device Address

Mode	Write	Read
DRX device address	$8E_{hex}$	$8F_{hex}$

Writing is done by sending the device write address, followed by the subaddress byte, two address bytes, and two data bytes. Reading is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data.

Due to the internal architecture of the DRX, the DRX cannot react immediately to an I^2C request. The typical response time is about 0.3 ms. If the DRX cannot accept another complete byte of data until it has performed some other function (for example, servicing an internal interrupt), it will hold the clock line low to force the transmitter into a wait state. The maximum wait period during normal operation mode is less than 1 ms.

Table 3–2: I^2C Bus Subaddresses

Name	Sub-address	Mode	Function	Reference
CONTROL	00	Read/Write-short	Write: Software reset of DRX and MSP-Part Read: Hardware error status of MSP	Table 3–4 on page 2-16
WR_DRX	10	Write-long	write address	
RD_DRX	11	Write-long	read address	

3.1.2. Protocol Description

Write-Long protocol

S	$8E_{hex}$	Wait	ACK	sub-addr 10h	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read-Long protocol

S	$8E_{hex}$	Wait	ACK	sub-addr 11h	ACK	addr-byte high	ACK	addr-byte low	ACK	S	$8F_{hex}$	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Write-Short to Control

S	$8E_{hex}$	Wait	ACK	00	ACK	data-byte high	ACK	data-byte low	ACK	P

Read-Short from Control Register

S	$8E_{hex}$	Wait	ACK	00_{hex}	ACK	S	$8F_{hex}$	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Note: S = I^2C bus Start Condition from master
P = I^2C bus Stop Condition from master
ACK = Acknowledge-bit: LOW on SDA from slave (= DRX, light gray) or master (= controller dark gray)
NAK = Not Acknowledge-bit: HIGH on SDA from master (dark gray) to indicate ‘End of Read’ or from DRX indicating internal error state
Wait = I^2C clock line is held low, while the DRX is processing the I^2C command. This waiting time is max. 1 ms

3.1.3. Proposals for General DRX I^2C Telegrams

3.1.3.1. Symbols

daw	write device address ($8E_{hex}$)
dar	read device address ($8F_{hex}$)
<	Start Condition
>	Stop Condition
aa	Address Byte
dd	Data Byte

3.1.3.2. Write Telegrams

<daw 00 d0 00>	write to CONTROL register
<daw 10 aa aa dd dd>	write data into DRX

3.1.3.3. Read Telegrams

<daw 11 aa aa <dar dd dd>	read data from DRX

3.2.I2C Register Block Index

Name	Page
Advanced Read-Out	18
Advanced Settings	16
Configuration	16
Control	18
Read-Out	18

3.3.I2C Register Index

Name	Addr	Page
AFC_DEV[7:0]	h11-100B	18
AFC_LOCK	h11-100B	18
AFC_LOCK_QUAL[10:0]	h11-100C	18
BP_EN	h10-1023	17
CLIP_REF_BS[8:0]	h10-1016	17
COMP_STATE[1:0]	h10-10B0	18
CR_AMP_TH_BS[7:0]	h10-1017	17
CR_D[2:0]	h10-1014	17
CR_I[2:0]	h10-1014	17
CR_OVM_TH_BS[7:0]	h10-1015	17
CR_P[2:0]	h10-1014	17
DPHI_2IF_BS[11:0]	h10-1021	17
DRX_TIME_OUT	h00	18
EQU_C0[8:0]	h10-1070	18
EQU_C1[8:0]	h10-1071	18
EQU_C2[8:0]	h10-1072	18
EQU_C3[8:0]	h10-1073	18
EQU_UPD	h10-1070	18
IF_FREQ_BS[9:0]	h10-1022	17
KI_CHANGE_TH[11:0]	h10-10AF	18
MOD_POL	h10-1023	18
MSP_TIME_OUT	h00	18
SIF_GAIN_BS[10:0]	h11-100A	18
SIF_REF[1:0]	h10-1001	16
SIF_STD[1:0]	h10-1023	17
SOFT_RESET	h00	18
STANDARD_BS[11:0]	h10-0020	16
SYNC_SLICE_BS[9:0]	h11-1003	18
T_COC_BS[11:0]	h10-1097	18
TAGC_HR_BS[10:0]	h10-1008	17
TAGC_I_BS[10:0]	h11-1006	18
TAGC_KI[2:0]	h11-1007	18
TAGC_REDUC[1:0]	h10-1007	16
TOP_SET_BS[3:0]	h10-1012	16
VAGC_KI[2:0]	h11-1007	18
VAGC_REDUC[1:0]	h10-1007	17
VAGC_VEL	h10-1023	17
VID_AMP[1:0]	h10-1001	16
VID_AMP_HEAD_BS[11:0]	h11-100D	17
VID_AMP_HIRES_BS[9:0]	h10-1002	16
VID_GAIN_BS[10:0]	h11-1005	18
VID_PEAK[4:0]	h10-1001	16

3.4.I2C Register Subaddress Index

Table 3–3: I2C Subaddress Index

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h10-0020					STANDARD_BS[11:0]												h0103
h10-1001								VID_AMP[1:0]		SIF_REF[1:0]		VID_PEAK[4:0]					h0123
h10-1002							VID_AMP_HIRES_BS[9:0]										h0000
h11-1003							SYNC_SLICE_BS[9:0]										
h11-1005						VID_GAIN_BS[10:0]											
h11-1006						TAGC_I_BS[10:0]											
h11-1007											TAGC_KI[2:0]			VAGC_KI[2:0]			
h10-1007					TAGC_REDUC[1:0]		VAGC_REDUC[1:0]										h0000
h10-1008						TAGC_HR_BS[10:0]											h0096
h11-100A						SIF_GAIN_BS[10:0]											
h11-100B								AFC_DEV[7:0]								AFC_LOCK	
h11-100C						AFC_LOCK_QUAL[10:0]											
h11-100D					VID_AMP_HEAD_BS[11:0]												h0380
h10-1012													TOP_SET_BS[3:0]				h0008
h10-1014								CR_I[2:0]			CR_D[2:0]			CR_P[2:0]			h009B
h10-1015									CR_OVM_TH_BS[7:0]								h00A0
h10-1016								CLIP_REF_BS[8:0]									h01C0
h10-1017									CR_AMP_TH_BS[7:0]								h0010
h10-1021					DPHI_2IF_BS[11:0]												h0B10
h10-1022							IF_FREQ_BS[9:0]										h013D
h10-1023									SIF_STD[1:0]		BP_EN	VAGC_VEL	MOD_POL				h0040
h10-1070							EQU_C0[8:0]									EQU_UPD	h000E
h10-1071								EQU_C1[8:0]									h0197
h10-1072								EQU_C2[8:0]									h00C5
h10-1073								EQU_C3[8:0]									h012E
h10-1097					T_COC_BS[11:0]												h00FA
h10-10AF					KI_CHANGE_TH[11:0]												h001E
h10-10B0															COMP_STATE[1:0]		h0003
h00		DRX_TIME_OUT	MSP_TIME_OUT														
h00	SOFT_RESET																h0000

3.5.I2C Register Description

Note: For compatibility reasons every undefined bit in a writeable register should be set to '0'. Undefined bits in a readable register should be treated as "don't care"!

Table 3–4: I2C Register Description

Name	Sub	Addr	Dir	Reset	Range	Function
Configuration						
STANDARD_BS[11:0]	h10	h0020[11:0]	W	259	2, 3, 4, 9, hA, h40, h103, h109	**Standard Selection** Defines TV- or FM-Radio standard: h000: reserved h001: reserved h002: M/N h103: B (default) h003: G h004: D/K h009: L h109: L' h00A: I h040: FM-Radio
VID_AMP[1:0]	h10	h1001[8:7]	W	2	0,1,2,3	**Reference value for video amplitude (white to sync)** (the maximum level may exceed this value due to color content) 0: 2.0V 1: 1.5V 2: 1.0V (default) 3: 0.7V
SIF_REF[1:0]	h10	h1001[6:5]	W	1	0,1,2,3	**Reference value for analog SIF maximum amplitude** 0: 1000 mVpp 1: 700 mVpp (default) 2: 500 mVpp 3: 350 mVpp
VID_PEAK[4:0]	h10	h1001[4:0]	W	3	-8..15	**Frequency response of video peaking filter at 5 MHz** -8: -11.0 dB -7: -9.0 dB ... ... -2: -2.1 dB -1: -1.0 dB 0: 0.0 dB 1: 0.8 dB 2: 1.5 dB 3: 2.1 dB (default) ... ... 14: 8.1 dB 15: 8.3 dB
TOP_SET_BS[3:0]	h10	h1012[3:0]	W	8	0..15	**Tuner Take Over Point (TOP)** Defines the gain of the internal preamplifier to set the TOP 0: 0 dB 1: 1.33 dB 2: 2.67 dB ... 8: 10.33 dB (default) ... 14: 18.67 dB 15: 20 dB
Advanced Settings						
VID_AMP_HIRES_BS[9:0]	h10	h1002[9:0]	W	0	0..1023	**High resolution video reference amplitude** LSB = 1/1024 of output voltage This value is set according to the selected standard: B/G,M/N h2BC D/K h2D0 I h314 L/L' h28A
TAGC_REDUC[1:0]	h10	h1007[11:10]	W	0	0..3	**Tuner AGC loop gain reduction**

Table 3–4: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
VAGC_REDUC[1:0]	h10	h1007[9:8]	W	0	0..3	**Video AGC loop gain Reduction**
TAGC_HR_BS[10:0]	h10	h1008[10:0]	W	150	0..1023	**Reference value for the tuner AGC** Defines the ADC Headroom (equals wanted VID_GAIN) Minimum value: B/G,D/K, L/Lí, M/N : h96 I : hAA
VID_AMP_HEAD_BS[11:0]	h11	h100D[11:0]	W	896	-2048..2047	**Video Amplitude Headroom** Controls the DC level of the CVBS output signal
CR_I[2:0]	h10	h1014[8:6]	W	2	0..7	**Carrier Recovery Control Integral Coefficient**
CR_D[2:0]	h10	h1014[5:3]	W	3	0..7	**Carrier Recovery Control Differential Coefficient**
CR_P[2:0]	h10	h1014[2:0]	W	3	0..7	**Carrier Recovery Control Proportional Coefficient** The carrier recovery performs like a PLL and includes a **PID**-control (**P**roportional **I**ntegral **D**ifferential) block. Each part has a gain coefficient. Together they define the loop characteristics (resonance frequency, damping factor).
CR_OVM_TH_BS[7:0]	h10	h1015[7:0]	W	160	0..255	**Carrier Recovery Overmodulation Thresholds** Overmodulation causes a phase shift of 180 degrees. The overmodulation threshold defines the amplitude up to which such phase shifts are tolerated.
CLIP_REF_BS[8:0]	h10	h1016[8:0]	W	448	0..511	**Reference value for clipping detection**
CR_AMP_TH_BS[7:0]	h10	h1017[7:0]	W	16	0..255	**Carrier Recovery Amplitude Threshold** Bad modulators generate a orthogonal signal vector. Therefore, the phase of the picture carrier at small carrier amplitudes becomes unreliable. The amplitude threshold defines the carrier level below which the PLL does not consider the phase information.
DPHI_2IF_BS[11:0]	h10	h1021[11:0]	W	2832	0..4095	**Manual 2nd IF setting f =(DPHI_2IF/16384)*40.5 MHz** B hB3B G hCA D/K hCA4 I hCA4 L hCA4 Lí hCA4 M/N h97B FM hFFF
IF_FREQ_BS[9:0]	h10	h1022[9:0]	W	317	0..1023	**Manual IF frequency setting** Sets the frequency of the analog synthesizer if the default IF frequency does not fit. Calculation formula: IF_FREQ = (IF ± channel width)/Fref with Fref = 100.247 kHz, "+" for L' and "-" for all remaining standards Default IF_FREQ-values as applied by the Standard Selection: IF_FREQ: Standard 13Dh: B 134h: G 134h: D/K 134h: I 134h: L 198h: L' 148h: M/N 12Bh: FM-Radio An Application Note covering this item is also available.
SIF_STD[1:0]	h10	h1023[7:6]	W	1	0..3	**SIF AGC velocity** AGC off 0 FM,NICAM 1 AM 2 not allowed 3
BP_EN	h10	h1023[5]	W	0	0,1	**Video AGC Back Porch control enable** disable 0 enable 1 (valid only at VAGC_VEL = 1)
VAGC_VEL	h10	h1023[4]	W	0	0,1	**Video AGC velocity** fast 0 slow 1

Table 3–4: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
MOD_POL	h10	h1023[3]	W	0	0,1	**Video modulation polarity** negative 0 positive 1
EQU_C0[8:0]	h10	h1070[9:1]	W	7	-256..255	**Equalizer Coefficient 0**
EQU_UPD	h10	h1070[0]	W	0	0,1	**Update bit for Equalizer Coefficients** 0: do not update coefficients 1: update coefficients
EQU_C1[8:0]	h10	h1071[8:0]	W	407	-256..255	**Equalizer Coefficient 1**
EQU_C2[8:0]	h10	h1072[8:0]	W	197	-256..255	**Equalizer Coefficient 2**
EQU_C3[8:0]	h10	h1073[8:0]	W	302	-256..255	**Equalizer Coefficient 3**
T_COC_BS[11:0]	h10	h1097[11:0]	W	250	-1..2047	**Tuner cut off current** The tuner AGC normally has a small sensitivity above 3V. Thus, the control can be accelerated at low currents. The tuner cut off current indicates the current below which the tuner AGC has a increased loop gain. Unit: 1LSB = 0,4uA
KI_CHANGE_TH[11:0]	h10	h10AF[11:0]	W	30	0..4095	**AGC KI Change Threshold** Video gain variation above/below that value will increase/decrease the AGC Kis
COMP_STATE[1:0]	h10	h10B0[1:0]	W	3	0..3	**State of ADC Compensation** 0: bypass 1: softstart 2: not allowed 3: active
Advanced Read-Out						
SYNC_SLICE_BS[9:0]	h11	h1003[9:0]	R		0..1023	**Sync Slice Value**
Read-Out						
VID_GAIN_BS[10:0]	h11	h1005[10:0]	R		0..2047	**Gain of video AGC** 0.05 dB/LSB h96: 0dB
TAGC_I_BS[10:0]	h11	h1006[10:0]	R		0..2047	**Current of tuner AGC** 0.4 uA/LSB
TAGC_KI[2:0]	h11	h1007[5:3]	R		0..7	**Tuner AGC loop gain**
VAGC_KI[2:0]	h11	h1007[2:0]	R		0..7	**Video AGC loop gain**
SIF_GAIN_BS[10:0]	h11	h100A[10:0]	R		0..2047	**Gain of SIF AGC** 0.05 dB/LSB C8h: 0dB
AFC_DEV[7:0]	h11	h100B[8:1]	R		-128..127	**AFC Frequency deviation** 10 kHz/LSB
AFC_LOCK	h11	h100B[0]	R		0,1	**AFC Lock bit** 0: Carrier Recovery unlocked 1: Carrier Recovery locked
AFC_LOCK_QUAL[10:0]	h11	h100C[10:0]	R		0..2047	**AFC Lock Quality** < 080h: strong signal 080h...700h: weak signal > 700h: no signal
Control						
DRX_TIME_OUT	h00[14]		R		0,1	**DRX I2C Time Out** 0: no error occurred 1: response time >1.3 ms
MSP_TIME_OUT	h00[13]		R		0,1	**MSP I2C Time Out** 0: no error occurred 1: response time >1.3 ms
SOFT_RESET	h00[15]		W	0	0,1	**Software Reset** a) Write: Soft-(I2C)-Reset for DRX and MSP-Part 0: no reset 1: reset b) Read: Reset status of DRX and MSP-parts after last reading of CONTROL 0: no reset occurred 1: reset occurred

4. Data Sheet History

1. Advance Information: “VCT 49xyl, VCT 48xyl DRX - Analog TV IF- Demodulator”, Dec. 12, 2003, 6251-573-2-1AI. First release of the advance information.

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MICRONAS

Contents

Contents, continued

1. Introduction

Volume 3 describes the Multistandard Sound Processor (MSP) of VCT 49xyl, VCT 48xyl.

1.1. Chip Architecture

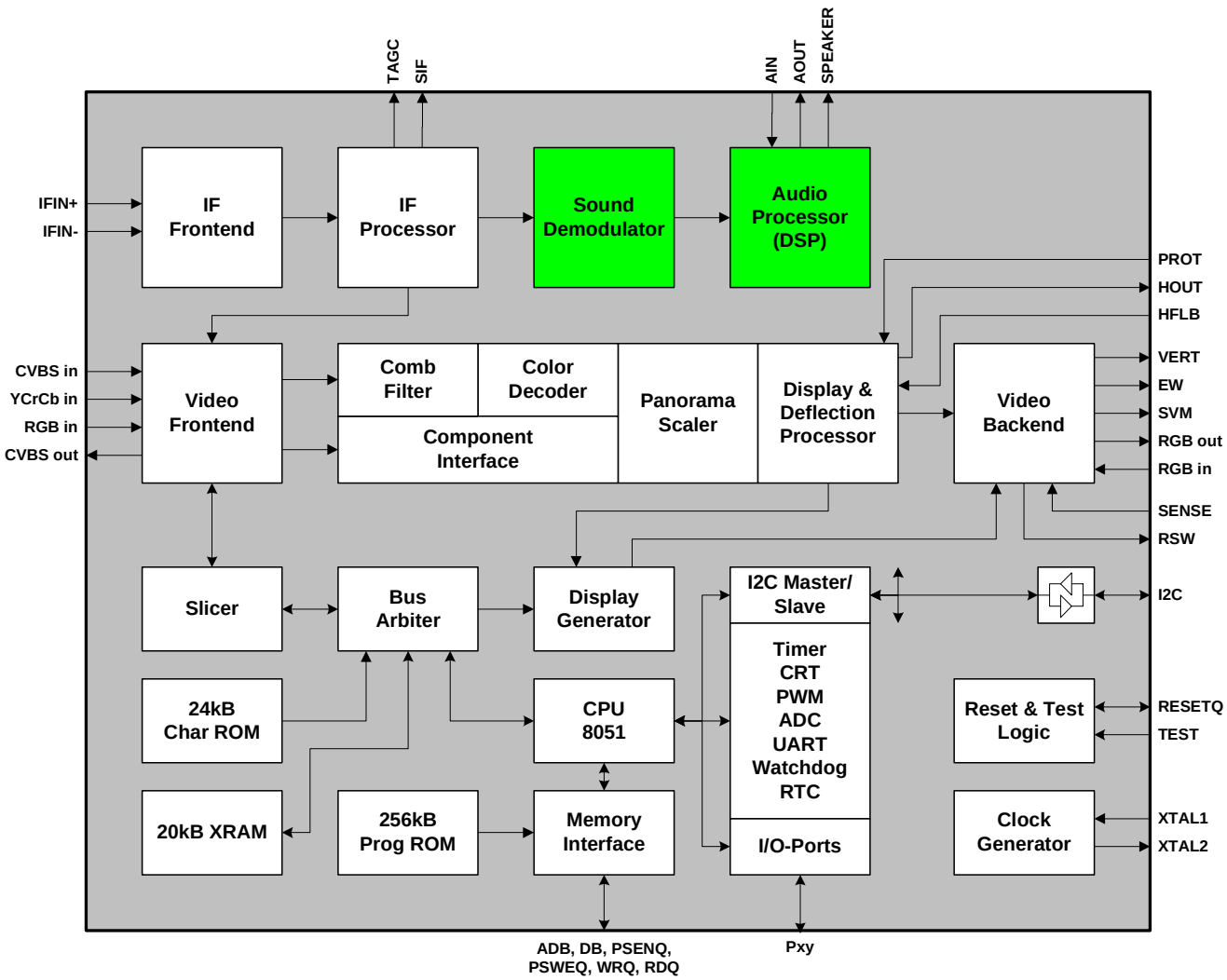


Fig. 1–1: Block diagram of the VCT 49xyl, VCT 48xyl highlighting the MSP-Parts

1.2. MSP Features

– Sound demodulator and stereo decoder:
  - worldwide FM/AM-mono demodulation
  - FM carrier based demodulation (A2, EIA-J)
  - FM stereo radio and RDS demodulation
  - NICAM demodulation/decoding
  - BTSC/SAP with DBX
  - optimum stereo separation without adjustments
  - Automatic Standard Detection (ASD): automatic standard detection for all stereo standards
  - Automatic Sound Select (ASS): mono/stereo/ bilingual switching without controller interaction

– Audio processing for loudspeaker channels:
  - volume
  - Automatic Volume Correction (AVC)
  - bass/treble or equalizer
  - loudness
  - balance
  - spatial effect (e.g. pseudo stereo)
  - Micronas AROUND
  - Micronas BASS (MB)
  - configurable Subwoofer output

– Optional features for loudspeaker channels:
  - Virtual Dolby Surround (VDS)
  - SRS WOW
  - BBE High Definition Sound
  - Micronas VOICE (MV)

– PMQFP144-2 package:
  - 6 analog audio inputs
  - 4 analog audio outputs

– PSSDIP88-1 package:
  - 4 analog audio inputs
  - 2 analog audio outputs
  - 2 configurable analog audio inputs/outputs

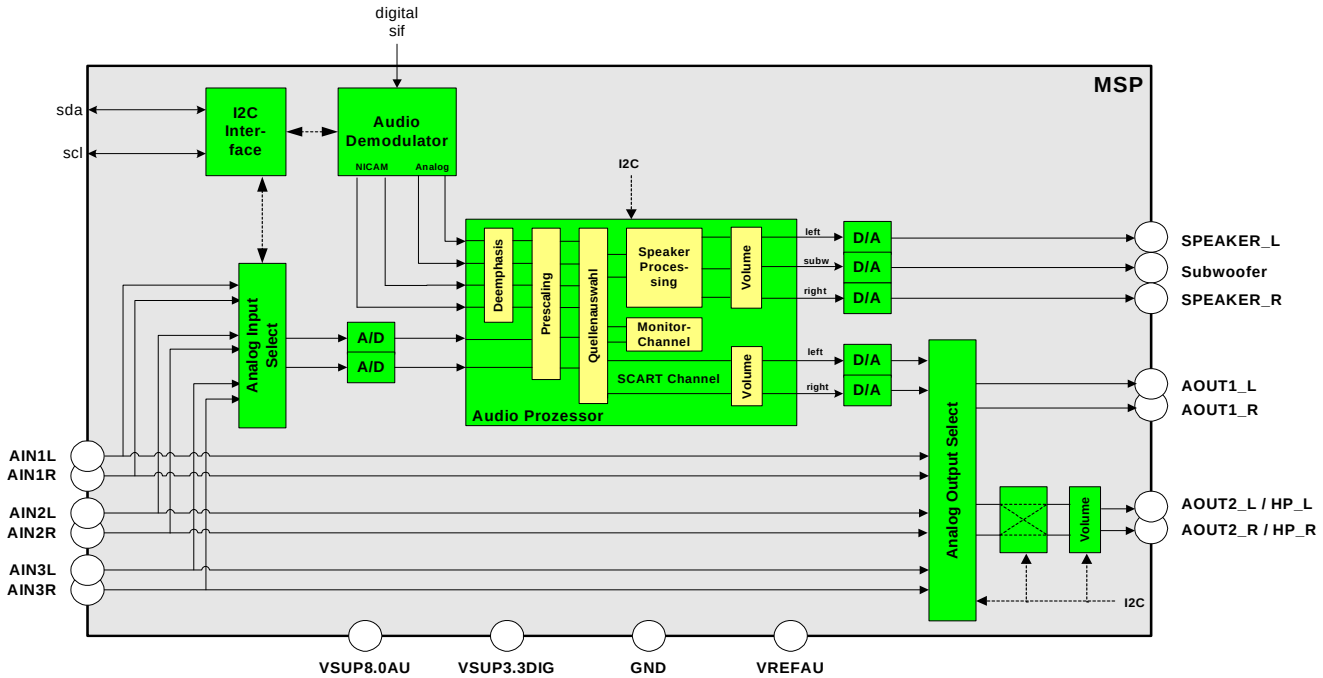


Fig. 1–2: MSP Sound Processing

1.3. Application Fields

Table 1–1 provides an overview of sound standards processed by the MSP.

Table 1–1: Stereo Sound Standards covered by the VCTI Family (details see Appendix A)

TV-System	Position of Sound Carrier /MHz	Sound Modulation	Color System	Broadcast e.g. in:
B/G	5.5/5.7421875	Dual FM-Carrier (“A2”)	PAL	Germany
	5.5/5.85	NICAM-FM	PAL	Scandinavia, Spain
L	6.5/5.85	NICAM-AM	SECAM-L	France
I	6.0/6.552	NICAM-FM	PAL	UK, Hong Kong
D/K	6.5/6.2578125	Dual FM-Carrier (D/K1)	SECAM-East	Slovak. Rep.
	6.5/6.7421875	Dual FM-Carrier (D/K2)	PAL	currently no broad-cast
	6.5/5.7421875	Dual FM-Carrier (D/K3)	SECAM-East	Poland
	6.5/5.85	NICAM-FM	PAL	Hungary
M/N	4.5/4.724212	Dual FM-Carrier	NTSC	Korea
	4.5	FM-FM (EIA-J)	NTSC	Japan
	4.5	BTSC-Stereo + SAP	NTSC, PAL	USA, Argentina, Brasil
FM-Radio + RDS		FM-Stereo Radio		USA, Europe

2. Functional Description

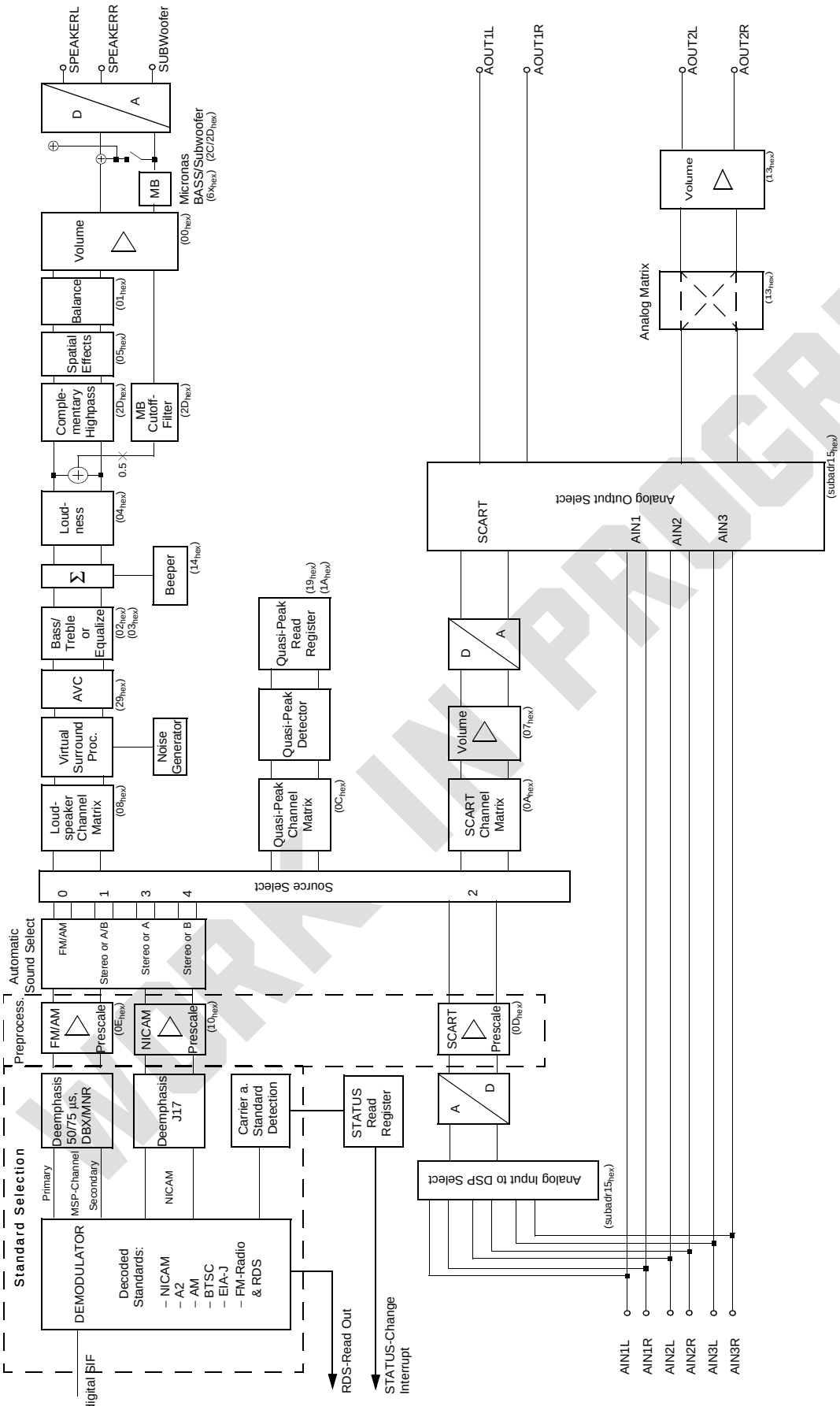


Fig. 2–1: Signal flow block diagram of the MSP section (input and output names correspond to pin names)

2.1. Architecture of the MSP

Fig. 2–1 on page 3-7 shows a simplified block diagram of a typical MSP. Other members of the VCT family do not have the complete set of features.

2.2. Demodulator

2.2.1. Overview on Sound Standards

The MSP receives the digital Sound IF signal from the DRX part.

The MSP is able to demodulate all TV sound standards worldwide including the digital NICAM system. Depending on the **VCTI** version, the following demodulation modes can be performed. TV stereo sound standards that are unavailable for a specific **VCTI** version are processed in analog mono sound of the standard. In that case, stereo or bilingual processing will not be possible.

A2-Systems: Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

NICAM-Systems: Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog (FM or AM) carrier.

High deviation FM-Mono: The primary MSP-Sound channel can be switched into the High Deviation Mode, providing robust demodulation of the FM1 carrier with a maximum deviation of more than 420 kHz.

BTSC-Stereo: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L-R)-carrier and detection of the SAP subcarrier. Noise reduction by DBX processing.

BTSC-Mono + SAP: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP-subcarrier. Noise reduction by DBX processing.

Japan Stereo (EIA-J): Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L-R)-carrier.

FM-Stereo-Radio plus RDS: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L-R)-carrier. Demodulation and channel-decoding of the RDS-signal, resulting in the RDS data stream, readable array-wise via I^2C registers.

RDS-Data are provided array-wise, each array containing 18 words of 12 bit RDS-data. A new array is indicated in the STATUS-register and optionally by an interrupt (see MODUS-register). Additionally for each new RDS-array the RDS_Array_Ct is incremented to enable the synchronisation of reading RDS-Data.

Note: There is a Micronas MINT-Software module available to decode and evaluate the RDS-datastream delivered by the MSP-part of the VCTI.

2.2.2. Demodulator Features

Note: For all analog demodulation systems the **primary MSP-Channel** contains the signal of the mono FM/AM carrier or the L+R signal of stereo systems. The **secondary MSP-Channel** contains the signal of the 2nd FM carrier, the L-R signal of the MPX carrier, or the SAP signal.

2.2.2.1. Standard Selection

TV-Sound Standards are selected by means of the Standard Selection Register. Either standard-specific codes are available or alternatively the general Automatic Standard Detection feature is selectable. All standard relevant parameters are defined by the standard selection.

Automatic Standard Detection: If the TV sound standard is unknown, the MSP can automatically detect the main (primary) carrier of analog standards and the NICAM carrier of digital standards. Then it switches to that standard, and responds the actual MSP standard code. Automatic Standard Detection is to be understood as a single procedure.

Since some TV-sound-standards have the same main carrier frequencies (i.e. all M- or analog D/K-standards), the feature Automatic Sound Select (see Section 2.2.2.3.) is able to complete the standard detection, searching for identification signals in the background and finally switching to the detected stereo-standard. In case of M/N-standards the standard to be checked first can be determined . Note that Automatic Sound Select is a continuous feature.

AM and FM carriers with identical SIF-frequencies cannot be distinguished by the Automatic Standard Detection. Therefore, it is possible to predefine whether a detected 6.5 MHz analog carrier is assigned to L or D/K standard .

2.2.2.2. Carrier Detection/Mute

To prevent noise effects or FM identification problems in the absence of an FM/AM carrier, the MSP offers a carrier detection feature, which can be separately switched on/off and configured for the primary and secondary MSP-Channel. If no FM carrier is detected at one or both of the two demodulator channels, the corresponding demodulator output is muted. This is indicated in the STATUS register. On/off-switching and configuration is independent from the Standard Selection and the feature Automatic Sound Select.

2.2.2.3. Automatic Sound Select (ASS)

In the Automatic Sound Select mode, the following source channels of demodulated sound are defined (see Fig. 2–1 on page 3-7):

– **“FM/AM” channel:** Analog mono sound, stereo if available.

– **“Stereo or A/B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).

– **“Stereo or A” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).

– **“Stereo or B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Selection of these source channels is done by means of the Source Select registers. Table 2–2 shows the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

Additionally the demodulator supports the identification check by switching between mono-compatible standards (standards that have the same FM-Mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, D/K3-FM and D/K-NICAM. and for the M/N standards Korea, BTSC and EIA-J. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

If automatic standard switching is not desired, it can be disabled.

In case of high bit-error rates, the MSP automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2–1 summarizes all actions that take place when Automatic Sound Select is switched on.

Table 2–1: Performed actions of the Automatic Sound Selection

Selected TV Sound Standard	Performed Actions
all analog sound standards	Evaluation of the identification or pilot signal and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2.
B/G-NICAM, L-NICAM, I-NICAM, D/K-NICAM	Evaluation of NICAM-C-bits and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2.
	In case of bad or no NICAM reception, the MSP switches automatically to FM/AM mono and switches back to NICAM if possible. A hysteresis prevents periodical switching.
B/G-FM, B/G-NICAM or D/K1-FM, D/K2-FM, D/K3-FM, and D/K-NICAM or M/N-Korea, M/N-BTSC and M/N-EIA-J	If not disabled: Automatic searching for stereo/bilingual-identification in case of mono transmission. Automatic and non-audible changes between Dual-FM and FM-NICAM standards while listening to the basic FM-mono sound carrier. Example: If starting with B/G-FM-Stereo, there will be a periodical alternation to B/G-NICAM in the absence of FM-Stereo/Bilingual or NICAM-identification. Once an identification is detected, the MSP keeps the corresponding standard.
M/N-BTSC-SAP	In the absence of SAP, the MSP switches to BTSC-stereo if available. If SAP is detected, the MSP switches automatically to SAP (see Table 2–2).

Table 2–2: Sound modes for the demodulator source channels with Automatic Sound Select

			Source Channels in Automatic Sound Select Mode			
Broadcasted Sound Standard	**Selected MSP Standard Code**[3]	**Broadcasted Sound Mode**	**FM/AM** (source select: 0)	**Stereo or A/B** (source select: 1)	**Stereo or A** (source select: 3)	**Stereo or B** (source select: 4)
M/N-Korea B/G-Dual FM D/K-Dual FM M/N-EIA-J	02 03, 08[1] 04, 05, 07, $0B_{hex}$[1], 30_{hex}	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo
		BILINGUAL: Languages A and B	Right = B	Left = A Right = B	A	B
B/G-NICAM L-NICAM I-NICAM D/K-NICAM	08, 03[2] 09 $0A_{hex}$ $0B_{hex}$, 04[2], 05[2] $0C_{hex}$	NICAM not available or error rate too high	analog Mono	analog Mono	analog Mono	analog Mono
		MONO	analog Mono	NICAM Mono	NICAM Mono	NICAM Mono
		STEREO	analog Mono	NICAM Stereo	NICAM Stereo	NICAM Stereo
		BILINGUAL: Languages A and B	analog Mono	Left = NICAM A Right = NICAM B	NICAM A	NICAM B
M/N BTSC	20_{hex} and 20_{hex}-SAP [4]	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo
	20_{hex}	MONO + SAP	Mono	Mono	Mono	Mono
		STEREO + SAP	Stereo	Stereo	Stereo	Stereo
	20_{hex}-SAP [4]	MONO + SAP	Left = Mono Right = SAP	Left = Mono Right = SAP	Mono	SAP
		STEREO + SAP	Left = Mono Right = SAP	Left = Mono Right = SAP	Mono	SAP
FM Radio	40_{hex}	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo

[1] The Automatic Sound Select process will automatically switch to the mono compatible analog standard.
[2] The Automatic Sound Select process will automatically switch to the mono compatible digital standard.
[3] For the MSP Standard Codes see .(see Section 3.6. “I2C Bit Slice Description” on page 23)
[4] 20_{hex}-SAP: Standard Code = 20_{hex} and Mod_BTSC = 1

2.2.2.3.1. Configuration of Automatic Sound Select

Although all parameters of ASS are defined carefully, it might be necessary to adjust some parameters to adapt the behavior to individual requirements. Therefore it is possible to configure the thresholds for stereo/bilingual-, NICAM- and carrier detection manually. Any modification is valid until a further modification or a reset.

2.2.2.4. STATUS Change Interrupt to Controller

By means of an interrupt-line to the VCTI-Controller section the MSP can send an interrupt request signal, indicating any changes in the read register STATUS. This makes polling unnecessary; I^2C-bus interactions are reduced to a minimum. By default this option is disabled.

2.3. Audio Baseband Processing (DSP)

2.3.1. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The level adjustment has to be done by means of the FM/AM and NICAM prescale registers.

2.3.2. Preprocessing for Analog Inputs

After selection of one analog input for A/D-conversion this input signal can be adjusted in level by means of the SCART prescale register.

2.3.3. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels and/or one of the analog inputs) to the loudspeaker or the analog output channels. All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix must stay fixed to stereo (transparent) for demodulated signals.

2.3.4. Features for Loudspeaker Outputs

Depending on the VCTI-version, the following baseband features are available for the loudspeaker output channel: Volume and automatic volume correction (AVC), balance, bass/treble or equalizer and loudness. A square wave beeper can be added to the loudspeaker channel. Optionally additional key coded features can be purchased.

2.3.4.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The AVC solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register.

For input signals ranging from –24 dBr to 0 dBr, the AVC maintains a fixed output level of –18 dBr. Fig. 2–2 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

– Input/output 0 dBr = 2.0 V_{rms}

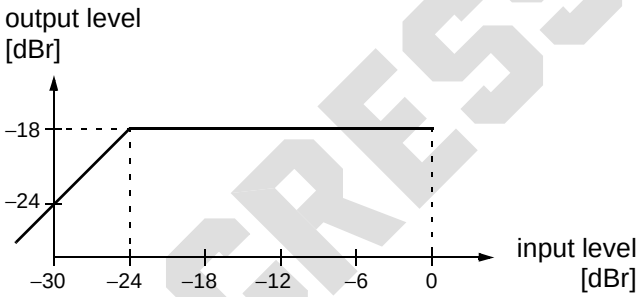


Fig. 2–2: Simplified AVC characteristics

2.3.4.2. Subwoofer Output

The subwoofer signal is created by combining the left and right channels directly behind the loudness block using the formula (L+R)/2. Due to the division by 2, the D/A converter will not be overloaded, even with full scale input signals. The subwoofer signal is filtered by a third-order low-pass with programmable corner frequency followed by a level adjustment. At the loudspeaker channels, a complementary high-pass filter can be switched on. Subwoofer and loudspeaker output use the same volume (Loudspeaker Volume Register). Use "SUBW_Enable" to activate the Subwoofer.

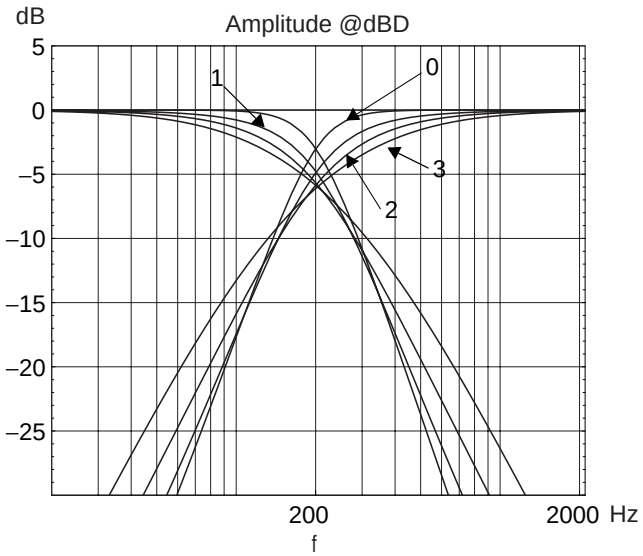


Fig. 2–3: Frequency response of subwoofer filter
0: sharp; 1: medium; 2: soft; 3: very soft edge

2.3.4.3. Micronas BASS (MB)

The **M**icronas **B**ASS system extends the frequency range of loudspeakers or headphones.

After the adaption of MB to the loudspeakers and the cabinet, further customizing of MB allows individual fine tuning of the sound.

Micronas BASS is placed in the subwoofer path. For applications without a subwoofer, the enhanced bass signal can be added back onto the Left/Right channels (see Fig. 2–1 on page 3-7). MB combines two effects: Dynamic Amplification and Adding Harmonics.

2.3.4.3.1. Dynamic Amplification

Low frequency signals can be boosted while the output signal amplitude is measured. If the amplitude comes close to a definable limit, the gain is reduced automatically in dynamic Volume mode. Therefore, the system adapts to the signal amplitude which is really present at the output of the MSP device. Clipping effects are avoided.

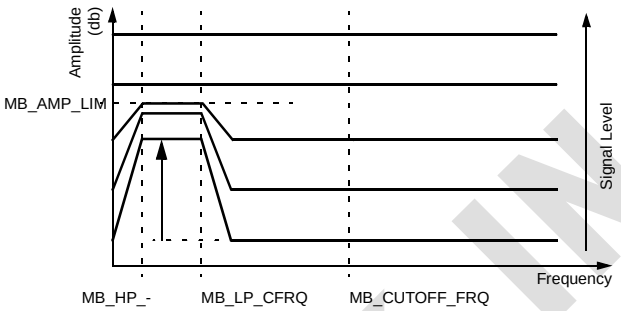


Fig. 2–4: Dynamic Amplification

2.3.4.3.2. Adding Harmonics

Micronas BASS exploits the psychoacoustic phenomenon of the ‘missing fundamental’. Adding harmonics of the frequency components below the MB_HP corner-frequency gives the impression of actually hearing the low frequency fundamental. In other words: The listener has the impression that a loudspeaker system seems to reproduce frequencies although physically not possible.

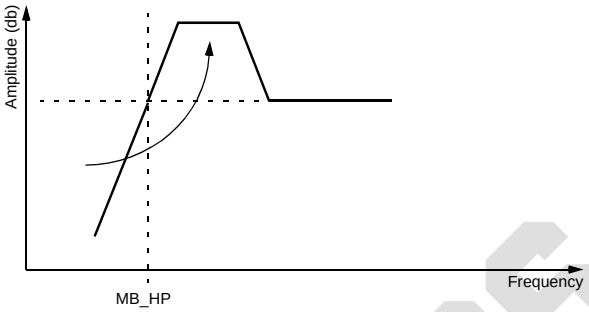


Fig. 2–5: Adding Harmonics

2.3.4.3.3. Micronas BASS Parameters

Several parameters allow tuning the characteristics of Micronas BASS according to the TV loudspeaker, the cabinet, and personal preferences. For more detailed information on how to set up Micronas BASS, please refer to the corresponding application note on the Micronas homepage.

2.3.4.4. SRS WOW

License Notice: SRS, SRS WOW and the SRS Logo are trademarks of SRS Labs, Inc. A license from SRS Labs, Inc. is required before a SRS-version of the VCT can be purchased.

SRS Labs’ WOW technology enlarges the sound image field and improves the bass performance of television speakers. Manufacturers can save costs by licensing WOW while utilizing smaller speakers and still provide a higher quality audio experience.

WOW consists of three sections:

– Clarity Improvement,
– 3D-Audio (SRS, Sound Retrieval System), and
– Bass Enhancement (TruBass).

Key features of WOW include:

– Wider and taller sound image field
– Larger sweet spot
– Deep, rich bass tones
– Quality improvements to audio listening experience
– Improved clarity of speech

All VCTs are shipped without SRS except otherwise ordered. When an SRS-version of VCT is ordered, it carries a special marking on the chip for identification. The SRS WOW functionality must be enabled by writ-

ing a "license key" into the MSP section of the VCT. For information on how to obtain this license key from Micronas, please contact your Micronas sales representative.

2.3.4.5. BBE High Definition Sound

License Notice: BBE is a registered trademark of BBE Sound Inc., the BBE Logo is a trademark of BBE Sound Inc. A license from BBE Sound Inc. is required before a BBE-version of the VCT can be purchased.

BBE High Definition Sound or, also called, Sonic Maximizer technology improves the clarity of music when played back via loudspeakers. A more “life like” feeling is created by BBE. The BBE-approved Micronas implementation works in the digital domain and thus needs no external components and does not suffer from tolerances and aging effects.

All VCTs are shipped without BBE except otherwise ordered. When a BBE-version of VCT is ordered, it carries a special marking on the chip for identification. The BBE Sonic Maximizer functionality must be enabled by writing a "license key" into the MSP section of the VCT. For information on how to obtain this license key from Micronas, please contact your Micronas sales representative.

2.3.4.6. Micronas VOICE (MV)

Micronas **V**OICE was developed to add the following improvements to speech signals:

– Increase speech signal over background noise to increase intelligibility in noisy environments

– Move voice to the foreground, closer to the listener, while other sounds are moved to the back

– Improve voices, that are hard to understand, leave clear voices largely undisturbed

Micronas VOICE dynamically enhances those portions of speech that are important for the intelligibility while at the same time decreasing portions of the signal that disturb the intelligibility. The average amplitude of the signal is not changed.

According to speech theory, there are two main effects that affect the intelligibility of speech. Micronas VOICE combines both effects to achieve a maximum enhancement of intelligibility.

– Forward and backward masking: For intelligibility, consonants are more important than vowels, but the amplitude of consonants is much lower than that of vowels. The consonants are masked by the vowels. Therefore the amplitude of consonants is increased and the amplitude of vowels decreased.

– Phonemes and formants: Most important for the intelligibility are the second to fourth formants of speech. These formants are detected and increased, while other parts of the signal are decreased.

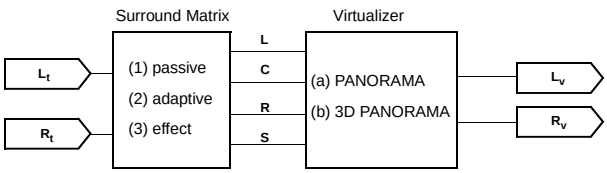
All VCTI are shipped without Micronas VOICE except otherwise ordered. When a Micronas VOICE - version of VCTI is ordered, it carries a special marking on the chip for identification. The Micronas VOICE functionality must be enabled by writing a "license key" into VCTI. For information on how to obtain this license key from Micronas, please contact your Micronas sales representative.

2.3.4.7. Virtual Surround Sound

License Notice: "Dolby", “Virtual Dolby Surround” and the double-D symbol are trademarks of Dolby Laboratories. Supply of this implementation of Dolby Technology does not convey a license nor imply a right under any patent, or any other industrial or intellectual property right of Dolby Laboratories, to use this implementation in any finished end-user or ready-to-use final product. Companies planning to use this implementation in products must obtain a license from Dolby Laboratories Licensing Corporation before designing such products.

Some VCTs versions are shipped with Virtual Surround Sound technologies.

Surround capable VCT-versions always allow the Micronas AROUND system, but only at a subset of versions the Virtual Dolby Surround system is implemented additionaly. Fig. 2–6 shows the possible Virtual Surround Sound systems, which are to be configured by the Surround Matrix and Virtualizer register.



Possible Virtual Surround Sound systems:
(1) & (b) = Micronas AROUND Virtual
(2) & (b) = Virtual Dolby Surround (VDS)
(3) & (b) = Micronas AROUND Virtual for monophonic input

Fig. 2–6: Possible Virtual Surround Sound systems

2.3.5. Headphone Outputs

The analog output pair AOUT2 can alternatively be used as headphone output, providing volume and matrix control.

2.3.6. Quasi-Peak Detector Channel

The quasi-peak readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

attack time: 1.3 ms
decay time: 37 ms

2.4. Analog Section

2.4.1. Analog Configuration Setup

In case of SDIP88 package one pin pair is shared for either analog input 3 (AIN3) or analog output 2 (AOUT2). To avoid misconfiguration the required configuration has to be defined after reset and should not be changed unless reset.

To reduce plops while switching the device on or off, a specific start-up and power-down sequence concerning the analog configuration is recommended.

2.4.2. Analog Input/Output Selection

The “Analog Input to DSP Select” and “Analog Output Select” blocks include full matrix switching facilities. In case of PMQFP package to design a TV set with three pairs of analog inputs and two pairs of analog outputs, no external switching hardware is reqired.

3. Control Interface

3.1. I²C Bus Register and Interface Description

The MSP is controlled by the VCT controller section via the I²C bus slave interface.

The MSP is selected by transmitting the MSP device address. A device address pair is defined as a write address and a read address (see Table 3–1).

Two register types require different protocolls to access them. There are registers, which are addressed merely by the subaddress (“short”), others require an additional address (below the subaddress, “long”). Each of the following protocolls is framed by a start and stop condition.

Write-Long is done by sending the write device address, followed by the subaddress byte, two address bytes, and two data bytes.

Write-Short is done by sending the write device address, followed by the subaddress byte and two data bytes.

Read-Long is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data.

Read-Short is done by sending the write device address, followed by the subaddress byte. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data.

Write and read registers are 16 bit wide (except the FBL-Status register), whereby the MSB is denoted bit[15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, with the most significant byte transferred first). All write registers, except the demodulator write registers are readable.

Unused parts of the 16-bit write registers must be zero.

Refer to Section 3.1.5. for the detailed I²C bus protocol and to Section 3.1.7. on page 3-18 for generalized I²C telegrams. See a list of available subaddresses in Table 3–2 on page 3-17. Details concerning start and stop bits are shown in Fig. 3–1.

Table 3–1: I²C Bus Device Address

Mode	Write	Read
MSP-device address	$8C_{hex}$	$8D_{hex}$

3.1.1. Reset of MSP and DRX via I²C (Soft-Reset)

Besides the possibility of hardware reset, the MSP can also be reset by means of the RESET bit in the CONTROL register (see Section 3.1.6. on page 3-17) by the controller via I²C bus. This register is shared with the DRX-section, using the DRX-device addresses for read and write. Note, that the Soft-Reset affects always the MSP and the DRX.

3.1.2. I²C Bus Response Time

Due to the architecture of the MSP, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the MSP cannot accept another byte of data (e.g. while servicing an internal interrupt), it holds the clock line I2C_CL low to force the transmitter into a wait state. The I²C Bus Master must read back the clock line to detect when the MSP is ready to receive the next I²C transmission. The positions within a transmission where this may happen are indicated by ’Wait’ in Section 3.1.5. The maximum wait period of the MSP during normal operation mode is less than 1 ms.

3.1.3. Internal Hardware Error Handling

In case of any hardware problems (e.g. interruption of the power supply of the MSP), the MSP’s wait period is extended to 1.6 ms. After this time period has elapsed, the MSP releases data and clock lines.

Indication and solving the error status:

To indicate the error status, the remaining acknowledge bits of the actual I²C-protocol will be left high. Additionally, bit[13] of CONTROL is set to one. The MSP can then be reset via the I²C bus by transmitting the RESET condition to CONTROL (see Table 3–4 and Table 3–3 on page 3-17).

Indication of reset:

Any reset, even caused by an unstable reset line etc., is indicated in bit[15] of CONTROL (see Table 3–4 on page 3-17).

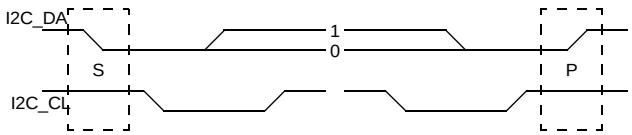


Fig. 3–1: I²C bus protocol (MSB first; data must be stable while clock is high)

3.1.4. FBL-Status

Due to architecture reasons the DDP-read register **FBL-STATUS** has to be accessed using the MSP device addresses. Note that this is an 8-bit register. For more information, see Section 2.2.2. of Volume 5.

3.1.5. Protocol Description

Write-Long to DSP or Demodulator

S	$8C_{hex}$	Wait	ACK	sub-addr 10h or 12h	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read-Long from DSP or Demodulator

S	$8C_{hex}$	Wait	ACK	sub-addr 11h or 13h	ACK	addr-byte high	ACK	addr-byte low	ACK	S	$8D_{hex}$	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Write-Short to APC and ACB

S	$8C_{hex}$	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Read-Short from FBL_Status-Register

S	$8C_{hex}$	Wait	ACK	80_{hex}	ACK	S	$8D_{hex}$	Wait	ACK	data-byte	NAK	P

Write-Short to Control

S	$8E_{hex}$	Wait	ACK	00	ACK	data-byte high	ACK	data-byte low	ACK	P

Read-Short from Control Register

S	$8E_{hex}$	Wait	ACK	00_{hex}	ACK	S	$8F_{hex}$	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= MSP, light gray) or master (= controller, dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate ‘End of Read’ or from MSP indicating internal error state
Wait = I^2C-Clock line is held low, while the MSP is processing the I^2C command. This waiting time is max. 1 ms

Table 3–2: I²C Bus Subaddresses for MSP-Section

Name	Sub-address	Mode	Function	Reference
CONTROL Note: DRX-Device-Addr.	00	Read/Write-short	Write: Software reset of DRX and MSP-Part Read: Hardware error status of MSP	(see Section 3.1.6. on page 3-17)
WR_DEM	10	Write-long	write address for demodulator registers	(see Table 3–6 on page -23)
RD_DEM	11	Write-long	read address for demodulator registers	
WR_DSP	12	Write-long	write address for Baseband Processing registers	
RD_DSP	13	Write-long	read address for Baseband Processing registers	
APC-Bits	14hex	Write-short	Analog Power-Up and Configuration Register	
ACB-Bits	15hex	Write-short	Analog Input/Output Selection	
FBL_STATUS	80hex	Read-short	Fast Blank Register (8 Bit)	

3.1.6. Description of CONTROL Register

Table 3–3: CONTROL as a Write Register; use the **DRX-device** Address

Name	Sub-Address	Bit[15] (MSB)	Bits[14:0]
CONTROL	00_{hex}	1 : RESET for DRX and MSP-Part 0 : normal	0
Note: Reset is active for appr. 50 µs			

Table 3–4: CONTROL as a Read Register; use the **DRX-device** Address

Name	Sub-Address	Bit[15] (MSB)	Bit[14]	Bit[13]	Bit[12:0]
CONTROL	00_{hex}	RESET status of DRX and MSP-parts after last reading of CONTROL: 0 : no reset occured 1 : reset occured	DRX: I²C Time Out 0 : no error occured 1 : response time >1.6 ms occured	MSP: I²C Time Out 0 : no error occured 1 : response time >1.6 ms occured	not of interest
Reading of CONTROL will reset the bits[15,14,13] of CONTROL. After Power-on, bit[15] of CONTROL will be set; it must be read once to be reset.					

3.1.7. Generalized I²C Telegrams

3.1.7.1. Symbols

daw	write device address ($8C_{hex}$, DRX: $8E_{hex}$)
dar	read device address ($8D_{hex}$, DRX: $8F_{hex}$)
<	Start Condition
>	Stop Condition
aa	Address Byte
dd	Data Byte

3.1.7.2. Write Telegrams

`<daw 00 d0 00>`	write to CONTROL register
`<daw 10 aa aa dd dd>`	write data into demodulator
`<daw 12 aa aa dd dd>`	write data into DSP

3.1.7.3. Read Telegrams

`<daw 00 <dar dd dd>`	read data from CONTROL register
`<daw 11 aa aa <dar dd dd>`	read data from demodulator
`<daw 13 aa aa <dar dd dd>`	read data from DSP

3.1.7.4. Examples

`<8E 00 80 00>`	RESET MSP and DRX statically
`<8C 10 00 30 00 01>`	activate ASS
`<8C 10 00 20 00 03>`	Set demodulator to stand. 03_{hex}
`<8C 11 02 00 <8D dd dd>`	Read STATUS
`<8C 12 00 08 01 20>`	Set loudspeaker channel source to Stereo or A/B and Matrix to STEREO

More examples of typical application protocols are listed in Section 3.7. “Application and Programming Tips” on page 3-37).

3.2. Start-Up Sequence: Power-Up and I²C-Controlling

After POWER-ON or RESET, the MSP is in an inactive state. All registers are in the Reset position, the analog outputs are muted. The controller has to initialize all registers for which a non-default setting is necessary (see Section 3.7. “Application and Programming Tips” on page 3-37).

3.3. I²C Register Block Index

3.4. I²C Bit Slices Index

3.5. I²C Register Subaddress Index

Table 3–5: I2C Subaddress Index

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h00																	h0000
h10-001D																	h000C
h10-0030	Mod_BTSC	Mod_4_5MHz[1:0]		Mod_6_5MHz	Mod_FMRadio	Mod_CM_B	Mod_CM_A	Mod_HDEV_A						Mod_Dis_Std_Chg	Mod_StatInterr	Mod_ASS	h0000
h10-0020					STD_Sel[11:0]												h0000
h11-007E	STD_Result[15:0]																
h11-0200							Stat_Bad_NICAM	Stat_Bil_or_SAP	Stat_Indep_Mono	Stat_Stereo	Stat_NICAM			Stat_Carr_B	Stat_Carr_A	Stat_New_RDS_D	
h10-0021					NICAM_Thld[11:0]												h02BC
h10-0022					A2_Thld[11:0]												h0190
h10-0023					BTSC_Thld[11:0]												h000C
h10-0024					CM_A_Thld[11:0]												h002A
h10-0025					CM_B_Thld[11:0]												h002A
h11-020F					RDS_Array_Ct[11:0]												
h11-0210					RDS_Data[11:0]												
h12-000E	FM_AM_Presc[7:0]																h0000
h12-0010	NICAM_Presc[7:0]																h0000
h12-0016																	h0000
h12-000D	SCART_Presc[7:0]																h0000
h12-0000	Vol_Main[7:0]								Vol_Main_Resol[2:0]						Vol_Clip_Mode[1:0]		h0000
h12-0001	Bal_Main[7:0]														Bal_Mode_Main[1:0]		h0000
h12-0002	Bass_Main[7:0]																h0000
h12-0003	Treble_Main[7:0]																h0000
h12-0004	Loud_Main[7:0]													Loud_Main_Mode[2:0]			h0000
h12-0008	Src_Sel_Main[7:0]								Matr_Sel_Main[7:0]								h0000
h12-000A	Src_Sel_SC_Out[7:0]								Matr_Sel_SC_Out[7:0]								h0000
h12-000B																	h0000
h12-000C	Src_Sel_QP[7:0]								Matr_Sel_QP[7:0]								h0000
h12-0005	Eff_Strgth_Main[7:0]										Eff_Mode_Main[1:0]		Eff_HP_G_Main[3:0]				h0000
h12-0007	Vol_SC_Proc_Ch[7:0]								Vol_SC_Resol[2:0]								h0000

Table 3–5: I2C Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h12-0013	Vol_AOUT2[7:0]														Matrix_AOUT2[1:0]		h0000
h12-0014	Vol_Beeper[7:0]								Frequ_Beeper[7:0]								h0000
h12-0020	Tone_Mode_Main[7:0]																h0000
h12-0021	EQ_Band1_Main[7:0]																h0000
h12-0022	EQ_Band2_Main[7:0]																h0000
h12-0023	EQ_Band3_Main[7:0]																h0000
h12-0024	EQ_Band4_Main[7:0]																h0000
h12-0025	EQ_Band5_Main[7:0]																h0000
h12-0029	AVC_SW_Main[3:0]				AVC_DEC_Main[3:0]												h0000
h12-0048								VSS_SW_Main[0]									h0000
h12-0049	VSS_Spat_Str[7:0]																h0000
h12-004A	VSS_3D_Str[7:0]																h0000
h12-004B	VSS_Matr_Mode[7:0]								VSS_Virt_Mode[7:0]								h0000
h12-004D	VSS_Noise_SW[7:0]								VSS_Noise_Sel[7:0]								h0000
h12-002C	SUBW_LEV[7:0]																h0000
h12-002D	SUBW_CFRQ[7:0]																h0000
h12-002D									SUBW_CHAR[7:4]								h0000
h12-002D													SUBW_HP[3:0]				h0000
h12-0067	MVOICE_Str[7:0]																h0000
h12-0068	MB_EFF_Str[7:0]																h0000
h12-0069	MB_AMP_LIM[7:0]																h0000
h12-006A	MB_HARM_CT[7:0]																h0000
h12-006B	MB_LP_CFRQ[7:0]																h0000
h12-006C	MB_HP_CFRQ[7:0]																h0000
h13-0019	Q_Peak_Left[15:0]																
h13-001A	Q_Peak_Right[15:0]																
h14	AOUT2_Enable	Ana_Amp_On_Off						SUBW_Enable							SIF_Out_Enable	Ana_Ref_On_Off	h0000
h15								Ana_DSP_In_Sel[2:0]			AOUT1_SEL[2:0]			AOUT2_SEL[2:0]			h0000
h11-0220	MSP_HW_Rev[15:0]																
h11-0221	MSP_FW_Rev[15:0]																
h10-009B					DCO_B_HI[11:0]												h0000
h10-0093					DCO_B_LO[11:0]												h0000

Table 3–5: I2C Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h10-00AB					DCO_A_HI[11:0]												h0000
h10-00A3					DCO_A_LO[11:0]												h0000
h11-0023									ADD_BIT[2:0]								
h11-0038									ADD_BIT[10:3]								
h11-003E																CIB2	
h11-003E															CIB1		
h11-0057					Error_Rate[11:0]												
h12-000F	FM_Deemph[7:0]																h0000
h12-006F									FM_Matrix[7:0]								h0000
h13-0018	FM_Ident[7:0]																
h13-001B	FM_DC_LEV_A[15:0]																
h13-001C	FM_DC_LEV_B[15:0]																
h12-0017																	h0000
h80									Static_Fast_Blank	Dynam_Fast_Blank							
h12-4444																	h0000

3.6. I²C Bit Slice Description

Note:
For compatibility reasons, every undefined bit in a writeable register should be set to '0'. Undefined bits in a readable register should be treated as "don't care"! **Addresses not given in this table must not be accessed.**

Although not mentioned explicitly, all registers addressed by the write-subaddress h12 are readable by means of the read-subaddress h13.

Table 3–6: I2C Register Description

Name	Sub	Addr	Dir	Reset	Range	Function
MODUS						
Mod_BTSC	h10	h0030[15]	W	0	0,1	**Standard 20h is focused on:** 0 BTSC-Stereo 1 BTSC-Mono and SAP Valid after the next application of the Standard Selection Register.
Mod_4_5MHz[1:0]	h10	h0030[14:13]	W	0	0,1,2,3	**Detected 4.5 MHz carrier is interpreted as:** 0 standard M-Korea 1 standard M-BTSC (USA) 2 standard M-EIA-J (Japan) 3 chroma carrier (M-standards are ignored) Valid after the next start of Automatic Standard Detection.
Mod_6_5MHz	h10	h0030[12]	W	0	0,1	**Detected 6.5 MHz carrier is interpreted as:** 0 standard L (SECAM) 1 standard D/K Valid after the next start of Automatic Standard Detection
Mod_FMRadio	h10	h0030[11]	W	0	0,1	**FM-Radio-Mode uses:** 0 75 µs Deemphasis (US) 1 50 µs Deemphasis (EU) Valid after the next application of the Standard Selection Register.
Mod_CM_B	h10	h0030[10]	W	0	0,1	**Behavior of Secondary MSP-channel**, if no 2ndary carrier is detected: 0 mute 1 noise
Mod_CM_A	h10	h0030[9]	W	0	0,1	**Behavior of Primary MSP-channel** , if no primary carrier is detected: 0 mute 1 noise
Mod_HDEV_A	h10	h0030[8]	W	0	0,1	**Modus of Primary MSP-channel (FM1):** 0 normal FM-Mode 1 High Deviation FM-Mode Valid after the next application of the Standard Selection Register.
Mod_Dis_Std_Chg	h10	h0030[2]	W	0	0,1	**ASS: Automatic standard change to search for Stereo** 0 enabled 1 disabled
Mod_StatInterr	h10	h0030[1]	W	0	0,1	**STATUS change indication** by means of the INTERRUPT-line: 0 disable interrupt 1 enable interrupt
Mod_ASS	h10	h0030[0]	W	0	0,1	**Automatic Sound Select (ASS):** 0 off 1 on (highly recommended) If changed from "1" to "0", it is recommended to apply the STANDARD SELECTION Register.

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
Demodulator						
STD_Sel[11:0]	h10	h0020[11:0]	W	0	1,2,3,4,5,7,8,9,hA,hb,h20,h30,h40	**Standard Selection** Defines TV-Sound or FM-Radio Standard: 00 01h Start Automatic Standard Detection 00 02h NTSC-M-Dual Carrier FM 00 03h B/G-Dual Carrier FM (A2) 00 04h D/K1-Dual Carrier FM 00 05h D/K2-Dual Carrier FM 00 07h D/K3-Dual Carrier FM 00 08h B/G-NICAM-FM 00 09h L-NICAM-AM 00 0Ah I-NICAM-FM 00 0Bh D/K-NICAM-FM 00 20h NTSC-BTSC Stereo/SAP (see MOD_BTSC) 00 30h NTSC-EIA-J 00 40h FM-Stereo Radio/RDS Note: Due to the internal automatic processes it is not allowed to refresh the Standard Select register periodically.
STD_Result[15:0]	h11	h007E[15:0]	R		0,2,3,4,5,8,9,hA,hb,h20,h21,h30,h40,h07ff	**RESULT of Automatic Standard Detection, if ASS = on.** Please regard special MODUS-Bits. 00 00h no sound standard detected 00 02h NTSC-M-Dual Carrier FM (s. Mod_4_5MHz) 00 03h B/G-Dual Carrier FM (A2) 00 04h D/K1-Dual Carrier FM 00 05h D/K2-Dual Carrier FM 00 07h D/K3-Dual Carrier FM 00 08h B/G-NICAM-FM 00 09h L-NICAM-AM (s. Mod_6_5MHz) 00 0Ah I-NICAM-FM 00 0Bh D/K-NICAM-FM (s. Mod_6_5MHz) 00 20h BTSC Stereo (s. Mod_BTSC & Mod_4_5MHz) 00 21h BTSC Mono and SAP (s. Mod_BTSC) 00 30h NTSC-EIA-J (s. Mod_4_5MHz) 00 40h FM-Stereo Radio/RDS US/EU (s. Mod_FMRadio) >07 FFh Automatic Standard Detection still active
STATUS-Read-Out						
Stat_Bad_NICAM	h11	h0200[9]	R		0,1	**Reception condition of digital sound (NICAM):** 0 NICAM reception o.k. 1 NICAM reception bad due to either: a. high error rate b. unimplemented sound code c. data transmission only
Stat_Bil_or_SAP	h11	h0200[8]	R		0,1	**Bilingual mode or SAP indication:** 0 no bilingual (SAP) detected 1 bilingual (SAP) detected
Stat_Indep_Mono	h11	h0200[7]	R		0,1	**Dependency of FM- to NICAM program (only for NICAM):** 0 dependent FM-mono program 1 independent FM-mono program
Stat_Stereo	h11	h0200[6]	R		0,1	**Stereo sound mode indication:** 0 no stereo detected 1 stereo detected
Stat_NICAM	h11	h0200[5]	R		0,1	**Digital sound (NICAM) indication:** 0 no NICAM detected 1 NICAM detected
Stat_Carr_B	h11	h0200[2]	R		0,1	**Secondary carrier (FM2 or SAP):** 0 detected 1 not detected
Stat_Carr_A	h11	h0200[1]	R		0,1	**Primary (mono or MPX) carrier:** 0 detected 1 not detected
Stat_New_RDS_D	h11	h0200[0]	R		0,1	**New RDS-data indicator:** 0 no RDS data 1 New RDS Data available

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
Automatic Sound Select-Configuration						
NICAM_Thld[11:0]	h10	h0021[11:0]	W	700	0..h7FF	**NICAM Threshold for individual ASS configuration:** If the error rate exceeds the NICAM Threshold STATUS will indicate BAD or no NICAM and the MSP will switch from NICAM to FM/AM. A hysteris avoids NICAM-FM toggling. 0000h force FM/AM-mono ... 02BCh default setting after reset (=700dez) ... 07FFh maximum Value; always switched to NICAM Recommended range : 0032h...07D0h = 50dez...2000dez The default ERROR_RATE value of 700dez corresponds to a BER (Bit-Error-Rate) of approximately 8.61*10-3 /s.
A2_Thld[11:0]	h10	h0022[11:0]	W	400	0..h7FF	**A2-Threshold for individual ASS configuration:** If the Identification Level exceeds the A2-Threshold STATUS switches from Mono to Stereo or Bilingual indication. In case of ASS=on the MSP switches to the corresponding sound mode. A hysteris avoids sound-mode toggling. 07FFh force Mono Identification ... 0190h default setting after reset ... 00A0h minimum threshold for stable detection Recommended range : 00A0h...03C0h
BTSC_Thld[11:0]	h10	h0023[11:0]	W	12	0..h7FF	**BTSC/FM-Radio-Threshold for individual ASS configuration:** If the Pilot Level exceeds the threshold value, STATUS switches from Mono to Stereo indication. In case of ASS=on the system switches to the stereo sound mode. A hysteris avoids sound-mode toggling. 07FFh force Mono Identification ... 000Ch default setting after reset ... 0006h minimum threshold for stable detection Recommended range : 0006h...000Fh
CM_A_Thld[11:0]	h10	h0024[11:0]	W	42	0..h7FF	**Primary Carrier Detection Threshold:** If carrier value exceeds the threshold STATUS indicates "no carrier detected". If the feature is not disabled, the corresponding sound channel is muted. 0000h force to ignore carrier and mute channel ... 002Ah default setting after reset ... 07FFh maximum value: Force to detect carrier and do not mute channel Recommended range : 0014h...0050h
CM_B_Thld[11:0]	h10	h0025[11:0]	W	42	0..h7FF	**Secondary Carrier Detection Threshold:** If carrier value exceeds the threshold STATUS indicates "no carrier detected". If the feature is not disabled, the corresponding sound channel is muted. 0000h force to ignore carrier and mute channel ... 002Ah default setting after reset ... 07FFh maximum value: Force to detect carrier and do not mute channel Recommended range : 0014h...0050h

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
RDS-Data						
RDS_Array_Ct[11:0]	h11	h020F[11:0]	R		hFFF,0..h7FF	**RDS-Array-Counter**, incremented once each time a new RDS-Data Array is available. Note that a new RDS-Array is indicated by STATUS[0]. The Array rate is appr. 181,9 ms. Possible values and meaning of the RDS-Array-Counter: hFFF RDS_Data are not valid 0...h7FF RDS_Data are valid
RDS_Data[11:0]	h11	h0210[11:0]	R		0..hFFF	**RDS-Data Readout Register:** After indication of a new RDS-Data Array by STATUS[0], this register has to be read out 18 times to get 18*12 bits of RDS-information. Bit[11] of the first read-out denotes the oldest bit, bit[0] of the last readout the newest bit of the actual RDS-Array.
Source Prescaling						
FM_AM_Presc[7:0]	h12	h000E[15:8]	RW	0	0..h7F	**Prescaling gain for the demodulated FM or AM source.** For all FM modes, the combinations of prescale value and FM deviation listed below lead to internal full scale with 1 kHz testsignal and 50µs emphasis. 7Fh 28 kHz FM deviation 48h 50 kHz FM deviation 30h 75 kHz FM deviation 24h 100 kHz FM deviation 18h 150 kHz FM deviation 13h 180 kHz FM deviation 09h 380 kHz FM deviation (limit) For AM mode (MSP Standard Code = 9) the register is recommended to be set to 24h. Due to the DRX-AGC the AM-output level remains stable and independent of the actual SIF-level.
NICAM_Presc[7:0]	h12	h0010[15:8]	RW	0	0..h7F	**Prescaling gain for the digital NICAM source:** Examples: 00h off 10h 0 dB gain 2Dh +9 dB gain (recommendation) 7Fh +18 dB gain (maximum gain)
SCART_Presc[7:0]	h12	h000D[15:8]	RW	0	0..h7F	**Prescaling gain for the analog SCART source:** Examples: 00h off 19h 0 dB gain (2 VRMS input leads to digital full scale) 7Fh +14 dB gain (400 mVRMS input leads to digital full scale) Note: Due to the Dolby requirements, 19h is the maximum value allowed to prohibit clipping of a 2 VRMS input signal.
Speaker Channel: Volume						
Vol_Main[7:0]	h12	h0000[15:8]	RW	0	-1..127	**Volume Loudspeaker Channel:** Table with 1 dB step size 7Fh +12 dB (maximum volume) 7Eh +11 dB ... 74h +1 dB 73h 0 dB 72h -1 dB ... 02h -113 dB 01h -114 dB 00h Mute (reset condition) FFh Fast Mute (complete execution takes appr. 75 ms) With large scale input signals, positive volume settings may lead to signal clipping. The loudspeaker volume function is divided into a digital and an analog section. With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. To turn volume on again, the volume step that has been used before Fast Mute was activated must be transmitted.

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
Vol_Main_Resol[2:0]	h12	h0000[7:5]	RW	0	0..7	**Volume Loudspeaker Channel: Higher resolution table** 0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table
Vol_Clip_Mode[1:0]	h12	h0000[1:0]	RW	0	0,1,2,3	**Volume Loudspeaker Channel: Clipping modes** 0 reduce volume 1 reduce tone control 2 compromise 3 dynamic **Reduce volume:** To prevent severe clipping effects with bass, treble, or equalizer boosts, the internal volume is automatically limited to a level where, in combination with either bass, treble, or equalizer setting, the amplification does not exceed 12 dB. **Reduce tone control:** The bass or treble value is reduced if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced, where amplification together with volume exceeds 12 dB. **Compromise:** The bass or treble value and volume are reduced half and half if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced half and half, where amplification together with volume exceeds 12 dB. **Dynamic:** Volume is reduced automatically if the signal amplitudes would exceed -2 dBFS within the IC. For operation of Micronas BASS, dynamic mode must be switched on.
Speaker Channel: Basic Features						
Bal_Main[7:0]	h12	h0001[15:8]	RW	0	-128..127	**Balance Loudspeaker Channel:** 1. Linear Mode 7Fh Left muted, Right 100% 7Eh Left 0.8%, Right 100% ... 01h Left 99.2%, Right 100% 00h Left 100%, Right 100% FFh Left 100%, Right 99.2% ... 82h Left 100%, Right 0.8% 81h Left 100%, Right muted 2. Logarithmic Mode 7Fh Left -127 dB, Right 0 dB 7Eh Left -126 dB, Right 0 dB ... 01h Left -1 dB, Right 0 dB 00h Left 0 dB, Right 0 dB FFh Left 0 dB, Right -1 dB ... 81h Left 0 dB, Right -127 dB 80h Left 0 dB, Right -128 dB Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected.
Bal_Mode_Main[1:0]	h12	h0001[1:0]	RW	0	0,1	**Balance Mode Loudspeaker Channel:** 0 linear 1 logarithmic

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
Bass_Main[7:0]	h12	h0002[15:8]	RW	0	-96..127	**Bass Loudspeaker Channel:** Extended range 7Fh +20 dB 78h +18 dB 70h +16 dB 68h +14 dB normal range 60h +12 dB 58h +11 dB ... 08h +1 dB 00h 0 dB F8h -1 dB ... A8h -11 dB A0h -12 dB Higher resolution is possible: an LSB step in the normal range results in a gain step of about 1/8 dB, in the extended range about 1/4 dB. With positive bass settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.
Treble_Main[7:0]	h12	h0003[15:8]	RW	0	-96..120	**Treble Loudspeaker Channel:** 78h +15 dB 70h +14 dB ... 08h +1 dB 00h 0 dB F8h -1 dB ... A8h -11 dB A0h -12 dB Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB. With positive treble settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain.
Loud_Main[7:0]	h12	h0004[15:8]	RW	0	0..h44	**Loudness Loudspeaker Channel: Loudness Gain** 44h +17 dB 40h +16 dB ... 04h +1 dB 03h +0.75 dB 02h +0.5 dB 01h +0.25 dB 00h 0 dB Higher resolution of Loudness Gain is possible: An LSB step results in a gain step of about 1/4 dB. Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain.
Loud_Main_Mode[2:0]	h12	h0004[2:0]	RW	0	0,4	**Loudness Loudspeaker Channel: Modes** 0 normal (constant volume at 1 kHz) 4 Super Bass (constant volume at 2 kHz) The corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
Src_Sel_Main[7:0]	h12	h0008[15:8]	RW	0	0, 1, 2, 3, 4	**Source for Loudspeaker Output Channel:** 0 FM/AM (demodulated FM or AM mono signal) 1 Stereo or A/B (NICAM, if Automatic Sound Select = off) 2 SCART input 3 Stereo or A (only defined for Automatic Sound Select) 4 Stereo or B (only defined for Automatic Sound Select)
Matr_Sel_Main[7:0]	h12	h0008[7:0]	RW	0	0,h10,h20 ,h30	**Matrix Mode for Loudspeaker Output Channel:** 00h Sound A Mono (or Left Mono) 10h Sound B Mono (or Right Mono) 20h Stereo (transparent mode) 30h Mono (sum of left and right inputs divided by 2) In Automatic Sound Select mode for the demodulator sources the matrix should be set to ìStereoî (transparent).
Eff_Strgth_Main[7:0]	h12	h0005[15:8]	RW	0	-128..127	**Spatial Effects Loudspeaker Channel: Effect Strength** 7Fh Enlargement 100% 3Fh Enlargement 50% ... 01h Enlargement 1.5% 00h Effect off FFh reduction 1.5% ... C0h reduction 50% 80h reduction 100% A negative value reduces the stereo image. A strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large screen TV sets, a more moderate spatial effect is recommended. **Spatial effects should not be used together with 3D-PANORAMA or PANORAMA.**
Eff_Mode_Main[1:0]	h12	h0005[5:4]	RW	0	0, 2	**Spatial Effect Mode:** 0 Mode A: Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). 2 Mode B: Stereo Basewidth Enlargement (SBE) only. In mode A the spatial effect depends on the source mode. If the incoming signal is mono, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. In mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.
Eff_HP_G_Main[3:0]	h12	h0005[3:0]	RW	0	0,2,4,6,8	**Spatial Effect High-Pass Gain:** 0 max. high-pass gain 2 2/3 high-pass gain 4 1/3 high-pass gain 6 min. high-pass gain 8 automatic All spatial effects affect amplitude and phase response. With the High-Pass Gain, the frequency response can be customized. A value of 0 yields a flat response for center signals (L = R), but a high-pass function for L or R only signals. A value of 6 has a flat response for L or R only signals, but a low-pass function for center signals. By using 8, the frequency response is automatically adapted to the sound material by choosing an optimal high-pass gain.
Vol_Beeper[7:0]	h12	h0014[15:8]	RW	0	0..h7F	**Beeper Volume:** 00h off 7Fh maximum volume
Frequ_Beeper[7:0]	h12	h0014[7:0]	RW	0	1..hFF	**Beeper Frequency:** 01h 16 Hz (lowest) 40h 1 kHz FFh 4 kHz
AVC_SW_Main[3:0]	h12	h0029[15:12]	RW	0	0, 8	**Automatic Volume Correction (AVC) Loudspeaker Channel: On/Off Switch** 0 AVC off (and reset internal variables) 8 AVC on

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
AVC_DEC_Main[3:0]	h12	h0029[11:8]	RW	0	8,4,2,1	**Automatic Volume Correction (AVC) Loudspeaker Channel: Decay Time** 8 8 sec decay time 4 4 sec decay time 2 2 sec decay time 1 20 ms decay time (should be used for approx. 100 ms after channel change)
SCART-Processing Channel						
Src_Sel_SC_Out[7:0]	h12	h000A[15:8]	RW	0	0, 1, 2, 3, 4	**Source for SCART- Output Channel:** 0 FM/AM (demodulated FM or AM mono signal) 1 Stereo or A/B (NICAM, if Automatic Sound Select = off) 2 SCART input 3 Stereo or A (only defined for Automatic Sound Select) 4 Stereo or B (only defined for Automatic Sound Select)
Matr_Sel_SC_Out[7:0]	h12	h000A[7:0]	RW	0	0,h10,h20,h30	**Matrix Mode for SCART- Output Channel:** 00h Sound A Mono (or Left Mono) 10h Sound B Mono (or Right Mono) 20h Stereo (transparent mode) 30h Mono (sum of left and right inputs divided by 2) In Automatic Sound Select mode for the demodulator sources the matrix should be set to ìStereoî (transparent).
Vol_SC_Proc_Ch[7:0]	h12	h0007[15:8]	RW	0	0..h7F	**Volume SCART Processing Channel: Table with 1 dB step size** 7Fh +12 dB (maximum volume) 7Eh +11 dB ... 74h +1 dB 73h 0 dB 72h -1 dB ... 02h -113 dB 01h -114 dB 00h Mute (reset condition)
Vol_SC_Resol[2:0]	h12	h0007[7:5]	RW	0	0..7	**Volume SCART Processing Channel: Higher resolution table** 0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table
Quasi Peak Channel						
Src_Sel_QP[7:0]	h12	h000C[15:8]	RW	0	0, 1, 2, 3, 4	**Source for Quasi-Peak Detector:** 0 FM/AM (demodulated FM or AM mono signal) 2 SCART input 1 Stereo or A/B (NICAM, if Automatic Sound Select = off) 3 Stereo or A (only defined for Automatic Sound Select) 4 Stereo or B (only defined for Automatic Sound Select)
Matr_Sel_QP[7:0]	h12	h000C[7:0]	RW	0	0,h10,h20,h30	**Matrix Mode for Quasi-Peak Detector:** 00h Sound A Mono (or Left Mono) 10h Sound B Mono (or Right Mono) 20h Stereo (transparent mode) 30h Mono (sum of left and right inputs divided by 2) In Automatic Sound Select mode for the demodulator sources the matrix should be set to ìStereoî (transparent).
Q_Peak_Left[15:0]	h13	h0019[15:0]	R		0..h7FFF	**Quasi-Peak Detector Readout Left:** 0h... 7FFFh values are 16 bit twoís complement (only positive)
Q_Peak_Right[15:0]	h13	h001A[15:0]	R		0..h7FFF	**Quasi-Peak Detector Readout Right:** 0h... 7FFFh values are 16 bit twoís complement (only positive)

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
AOUT2: Volume and Matrix						
Vol_AOUT2[7:0]	h12	h0013[15:8]	RW	0	0..h7F	**Volume Analog Output2 Channel: Table with 1 dB step size** 7Fh +12 dB (maximum volume) 7Eh +11 dB ... 74h +1 dB 73h 0 dB (RESET Position) 72h -1 dB ... 4Ch -39dB 4Bh -40dB (minimum volume) 00h Mute
Matrix_AOUT2[1:0]	h12	h0013[1:0]	RW	0	0,1, 2	**Matrix Analog Output2 Channel:** 0 Stereo or A/B (RESET position) 1 Channel A Mono 2 Channel B Mono If Output2 is used as Headphone Output, the Matrix must be switched to A-Mono (Language A) or B-Mono (Language B) in case of bilingual transmission.
Speaker Channel: Equalizer						
Tone_Mode_Main[7:0]	h12	h0020[15:8]	RW	0	0,hFF	**Tone Control Mode Loudspeaker Channel:** 00h Bass and treble is active FFh Equalizer is active Defines whether Bass/Treble or Equalizer is activated for the loudspeaker channel. Bass and Equalizer cannot work simultaneously. If Equalizer is used, Bass, and Treble coefficients must be set to zero and vice versa.
EQ_Band1_Main[7:0]	h12	h0021[15:8]	RW	0	-96..96	**Equalizer Loudspeaker Channel Band 1 (below 120 Hz):** 60h +12 dB 58h +11 dB ... 08h +1 dB 00h 0 dB F8h -1 dB ... A8h -11 dB A0h -12 dB Higher resolution is possible: An LSB step results in a gain step of about 1/8 dB. With positive equalizer settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain.
EQ_Band2_Main[7:0]	h12	h0022[15:8]	RW	0	-96..96	**Equalizer Loudspeaker Channel Band 2 (center: 500 Hz):** To be configured as described for "Band 1".
EQ_Band3_Main[7:0]	h12	h0023[15:8]	RW	0	-96..96	**Equalizer Loudspeaker Channel Band 3 (center: 1.5 kHz):** To be configured as described for "Band 1".
EQ_Band4_Main[7:0]	h12	h0024[15:8]	RW	0	-96..96	**Equalizer Loudspeaker Channel Band 4 (center: 5 kHz):** To be configured as described for "Band 1".
EQ_Band5_Main[7:0]	h12	h0025[15:8]	RW	0	-96..96	**Equalizer Loudspeaker Channel Band 5 (above 10 kHz):** To be configured as described for "Band 1".
Speaker Channel: Virtual Surround						
VSS_SW_Main[0]	h12	h0048[8]	RW	0	0,1	**Virtual Surround Sound on Loudspeaker Channel: On/Off Switch** 0 virtual surround sound = off 1 virtual surround sound = on **Spatial Effects Loudspeaker Channel (register 0005h) must be switched off if Virtual Surround is in use.**

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
VSS_Spat_Str[7:0]	h12	h0049[15:8]	RW	0	0..h7F	**Virtual Surround: Spatial Effect Strength** 7Fh Enlargement 100% 3Fh Enlargement 50% ... 01h Enlargement 0.78% 00h Effect off Increases the perceived basewidth of the reproduced left and right front channels. Recommended value: 50% = 3Fh. In contrast to the Spatial Effects Loudspeaker Channel, the Surround Spatial Effects is optimized for virtual surround.
VSS_3D_Str[7:0]	h12	h004A[15:8]	RW	0	0..h7F	**Virtual Surround: 3D Effect Strength** 7Fh Effect 100% 3Fh Effect 50% ... 01h Effect 0.78% 00h Effect off Strength of the surround effect. Recommended value: 66% = 54h.
VSS_Matr_Mode[7:0]	h12	h004B[15:8]	RW	0	h00,h10,h20	**Virtual Surround: Matrix Mode** 00h adaptive (compliant to Virtual Dolby Surround) 10h passive (for Micronas AROUND Virtual) 20h effect (for monophonic signals)
VSS_Virt_Mode[7:0]	h12	h004B[7:0]	RW	0	h50,h60	**Virtual Surround: Virtualizer Mode** 50h PANORAMA 60h 3D-PANORAMA (virtualizer approved by Dolby Laboratories)
VSS_Noise_SW[7:0]	h12	h004D[15:8]	RW	0	0,h80	**Virtual Surround Noise Generator: On/Off Switch** 00h Noise generator off 80h Noise generator on
VSS_Noise_Sel[7:0]	h12	h004D[7:0]	RW	0	hA0,hB0,hC0,hD0	**Virtual Surround Noise Generator: Channel Selector** A0h Noise on left channel B0h Noise on center channel C0h Noise on right channel D0h Noise on surround channel
Speaker Channel: Subwoofer						
SUBW_LEV[7:0]	h12	h002C[15:8]	RW	0	-128..12	**Subwoofer Level Adjustment with 1 dB step size** 0Ch +12 dB (maximum) 0Bh +11 dB ... 01h +1 dB 00h 0 dB (RESET Position) FFh -1 dB ... E3h -29dB E2h -30dB ... 80h Mute Note: If Micronas BASS is added onto speaker channels L/R, this register should be set to 00hex
SUBW_CFRQ[7:0]	h12	h002D[15:8]	RW	0	0, 5..40	**Subwoofer Corner Frequency:** 0 Subwoofer is switched off 5...40dez corner frequency in 10-Hz steps from 50 to 400 Hz Note: If Micronas BASS is active, SUBW_CFREQ must be set to a value higher than the MB Lowpass Corner Frequency (MB_LP_CFRQ). Choosing the corner frequency of the subwoofer closer to MB_LP_CFRQ results in a narrower MB frequency range. Recommended value: 1.5ÞMB_LP_CFRQ

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
SUBW_CHAR[7:4]	h12	h002D[7:4]	RW	0	0,1,2,3	**Subwoofer Characteristics:** 0h sharp edge Subwoofer characteristics (RESET Position) 1h medium edge Subwoofer characteristics 2h soft edge Subwoofer characteristics 3h very soft edge Subwoofer characteristics An adjustable subwoofer filter characterisitic with four different filter sets can be selected. Due to the complementary filter design, the output of high- and lowpass filter add up to 0db at the crossover region for all filter sets.
SUBW_HP[3:0]	h12	h002D[3:0]	RW	0	0,1,2	**Subwoofer: Complementary Highpass Filter for L/R-Speaker channels and Micronas BASS on/off switch** 0h speaker channels L/R unfiltered (RESET Position) 1h complementary high-pass is processed for L/R 2h Micronas BASS is added onto speaker channels L/R
Speaker Channel: Micronas VOICE						
MVOICE_Str[7:0]	h12	h0067[15:8]	RW	0	0..h60	**Micronas VOICE (Speech Enhancement) Strength:** 60h +12 dB 58h +11 dB ... 08h +1 dB 00h 0 dB Micronas VOICE cannot be used together with Micronas BASS. To operate MV, MB must be switched off (Reg. 68h=0). Note that the Volume Clipping Mode must be set to ìdynamicî.
Speaker Channel: Micronas BASS						
MB_EFF_Str[7:0]	h12	h0068[15:8]	RW	0	0..h7F	**Micronas BASS Effect Strength:** 00h Micronas BASS OFF (default) 7Fh maximum Micronas BASS The Micronas BASS effect strength can be adjusted in 1 dB steps. A value of 44h will yield a medium Micronas BASS effect.
MB_AMP_LIM[7:0]	h12	h0069[15:8]	RW	0	hE0..0	**Micronas BASS Amplitude Limit:** 00h 0 dBFS (default limitation) FFh -1 dBFS ... E0h -32 dBFS The Micronas BASS Amplitude Limit defines the maximum allowed amplitude at the output of the Micronas BASS relative to 0 dbFS. If the amplitude exceeds MB_AMP_LIM, the gain of the Micronas BASS is automatically reduced. Note that the Volume Clipping Mode must be set to ìdynamicî.
MB_HARM_CT[7:0]	h12	h006A[15:8]	RW	0	0..h7F	**Micronas BASS Harmonic Content:** 00h no harmonics are added (default) 64h 50% fundamentals + 50% harmonics 7Fh 100% harmonics Micronas BASS creates harmonics of the frequencies below the MB highpass frequency (MB_HP). The variable MB_HARM_CT describes the ratio of the harmonics towards the original signal.
MB_LP_CFRQ[7:0]	h12	h006B[15:8]	RW	0	5..h1E	**Micronas BASS Low Pass Corner Frequency:** 5...30dez corner frequency in 10-Hz steps from 50 to 300 Hz The Micronas BASS lowpass corner frequency (range 50...300 Hz) defines the upper corner frequency of the MB bandpass filter. Recommended values are the same as for the MB highpass corner frequency (MB_HP).
MB_HP_CFRQ[7:0]	h12	h006C[15:8]	RW	0	2..h1E	**Micronas BASS High Pass Corner Frequency:** 2...30dez corner frequency in 10-Hz steps from 20 to 300 Hz The Micronas BASS highpass corner frequency defines the lower corner frequency of the MB bandpass filter. The highpass filter avoids loading the loudspeakers with low frequency components that are below the speakersí cut off frequency. Recommended values for subwoofer systems are around 5 (=50 Hz), for regular TV sets around 10 (=100 Hz).

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
Analog Power-Up Configuration						
AOUT2_Enable	h14[15]		RW	0	0,1	**AOUT2 Configuration** 0 AOUT2 is disabled, AIN3 is selected (RESET position) 1 AOUT2 is selected, for SDIP88 package AIN3 is disabled Note: It is not possible to reconfigure this bit during normal operation. See also section "Programming Tips".
Ana_Amp_On_Off	h14[14]		RW	0	0,1	**Analog output amplifier Switch:** 0 off (RESET position) 1 on See also section "Programming Tips".
SUBW_Enable	h14[8]		RW	0	0,1	**Subwoofer Enable:** 0 off (RESET position) 1 on Note: Available for VCTI D1 or higher
SIF_Out_Enable	h14[1]		RW	0	0,1	**Analog SIF-Out Switch:** 0 off (RESET position) 1 on Note: Available for VCTI D1 or higher
Ana_Ref_On_Off	h14[0]		RW	0	0,1	**Analog Reference Switch:** 0 off (RESET position) 1 on See also section "Programming Tips".
Analog I/O Selection						
Ana_DSP_In_Sel[2:0]	h15[8:6]		RW	0	0,1,2,7	**Source Select for DSP-Input:** 1. If AIN3 is selected and for PQFP Packages: 0 AIN1 (RESET position) 1 AIN2 2 AIN3 7 mute DSP input 2. If AOUT2 is selected: 0 AIN1 (RESET position) 1 AIN2 2 must not be used 7 mute DSP input
AOUT1_SEL[2:0]	h15[5:3]		RW	0	0, 1, 2, 3, 7	**Source Select for AOUT1-Output:** 1. If AIN3 is selected and for PQFP Packages: 0 AIN2 (RESET position) 1 SCART DA 2 AIN1 3 AIN3 7 mute AOUT1 2. If AOUT2 is selected: 0 AIN2 (RESET position) 1 SCART DA 2 AIN1 3 must not be used 7 mute AOUT1

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
AOUT2_SEL[2:0]	h15[2:0]		RW	0	0, 1, 2, 3, 7	**Source Select for AOUT2-Output:** 1. For PQFP Packages: 0 SCART DA (RESET position) 1 AIN1 2 AIN2 3 AIN3 7 mute AOUT2 2. If AIN3 is selected: AOUT2 not existing 7 mute AOUT2 3. If AOUT2 is selected: 0 SCART DA (RESET position) 1 AIN1 2 AIN2 3 not defined; do not use 7 mute AOUT2
Hard- and Software Revision						
MSP_HW_Rev[15:0]	h11	h0220[15:0]	R		0..hFF	**MSP Hardware_Revision Code**
MSP_FW_Rev[15:0]	h11	h0221[15:0]	R		0..hFF	**MSP Firmware_Revision Code**
Demodulator: Manual Tuning						
DCO_B_HI[11:0]	h10	h009B[11:0]	W	0	0..hFFF	**Frequency Adjustment for Secondary Channel: High Part**
DCO_B_LO[11:0]	h10	h0093[11:0]	W	0	0..hFFF	**Frequency Adjustment for Secondary Channel: Low Part**
DCO_A_HI[11:0]	h10	h00AB[11:0]	W	0	0..hFFF	**Frequency Adjustment for Primary Channel: High Part**
DCO_A_LO[11:0]	h10	h00A3[11:0]	W	0	0..hFFF	**Frequency Adjustment for Primary Channel: Low Part**
Additional NICAM-Information						
ADD_BIT[2:0]	h11	h0023[7:5]	R		0..7	NICAM: Additional Data Bits[2:0]
ADD_BIT[10:3]	h11	h0038[7:0]	R		0..hFF	NICAM: Additional Data Bits[10:3]
CIB2	h11	h003E[0]	R		0,1	NICAM: CIB2 Bit
CIB1	h11	h003E[1]	R		0,1	NICAM: CIB1 Bit
Error_Rate[11:0]	h11	h0057[11:0]	R		0..h7FF	**NICAM: Error Rate:** Average error rate of the NICAM reception in a time interval of 182 ms, which should be close to 0. The initial and maximum value of ERROR_RATE is 2047. Since the value is achieved by filtering, a certain transition time (approx. 0.5 sec) is unavoidable. Acceptable audio may have error rates up to a value of 700 int. Individual evaluation of this value by the controller and an appropriate threshold may define the fallback mode from NICAM to FM/AM-mono in case of poor NICAM reception. The bit error rate per second (BER) can be calculated by means of the following formula: BER/s = ERROR_RATE * 12.3*10exp-6
Additional DSP Registers						
FM_Deemph[7:0]	h12	h000F[15:8]	RMW		0,1,h3F	**FM-Deemphasis:** 00h 50 µs (reset) 01h 75 µs 3Fh off **Note:** This register is initialized during STANDARD SELECTION and is automatically updated when ASS=on.

Table 3–6: I2C Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
FM_Matrix[7:0]	h12	h006F[7:0]	RMW		0,1,2,3,4	**FM Matrix Mode** Dematrix function for the demodulated FM signal: 00h no matrix (used for bilingual and unmatrixed stereo sound) 01h German stereo (Standard B/G) 02h Korean stereo (also used for BTSC, EIA-J and FM Radio) 03h sound A mono (left and right channel contain the mono sound of the FM/AM mono carrier) 04h sound B mono **Note:** In case of ASS=on, the FM Matrix Mode is set automatically. In order not to disturb the automatic process, it is not recommended to overwrite this parameter manually. In case of ASS=off, the FM Matrix Mode must be set as shown in the Appendix.
FM_Ident[7:0]	h13	h0018[15:8]	R		h80..h7F	**FM Identification Value for A2 and EIA-J systems:** Value near zero: Mono-Transmission Positive Value: Stereo-Transmission Negative Value: Bilingual Transmission **Note:** It is not necessary to read out and evaluate the A2 identification level. All evaluation is performed in the MSP and indicated in the STATUS register.
FM_DC_LEV_A[15:0]	h13	h001B[15:0]	R		h8000..h7FFF	**DC level of the incoming FM signal of the Primary Sound Channel** This value can be used for frequency fine tuning. A too low demodulation frequency (DCO) results in a positive DC-level and vice versa. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant t, defining the transition time of the DC Level Register, is approximately 28 ms.
FM_DC_LEV_B[15:0]	h13	h001C[15:0]	R		h8000..h7FFF	**DC level of the incoming FM signal of the Secondary Sound Channel** This value can be used for frequency fine tuning. A too low demodulation frequency (DCO) results in a positive DC-level and vice versa. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant t, defining the transition time of the DC Level Register, is approximately 28 ms.
FBL						
Static_Fast_Blank	h80[7]		R		0,1	**Static Fastblank Status** 0 no fastblank active 1 fastblank active
Dynam_Fast_Blank	h80[6]		R		0,1	**Dynamic Fastblank Status** 0 no fastblank edge detected 1 fastblank edge detected

3.7. Application and Programming Tips

This section describes the preferred method for initializing and switch off the MSP. The initialization is grouped into four sections:

- **3.7.1. Analog Power Configuration Setup**
- **3.7.2. Define Analog Input to DSP and AOUT1/2**
- **3.7.3. Demodulator Setup**
- **3.7.4. Loudspeaker and SCART Channel Setup**

See **Fig. 2–1 on page 3-7** for a complete signal flow.

It is recommended to start the initialization with an I^2C controlled reset of the IC (“soft-reset).

3.7.1. Analog Power Configuration Setup

Start-Up: To avoid misconfiguration of the AIN3/AOUT2-Pin for PSSDIP88-1 package and to reduce plops on AOUT1, AOUT2 and loudspeaker outputs, the following start-up sequence is to be recommended:

1. Power-Up of VSUP8.0AU
2. Set “Enable_AOUT2” as required, “Ana_Amp_On_Off” & “Ana_Ref_On_Off” to “1”
3. Wait at least 0.1 to 2 s (tbd)
4. Demute by means of Volume-Registers (Loudspeaker a. SCART)

Power-Down: To avoid power-down-plops on AOUT1, AOUT2 and loudspeaker outputs, the following power-down sequence is recommended:

1. Mute by means of Volume-Registers (Loudspeaker a. SCART)
2. Set “Ana_Ref_On_Off” to “0”, but keep “Ana_Amp_On_Off” to “1”
3. Wait at least 200 ms (tbd)
4. Set “Ana_Amp_On_Off” to “0”
5. Power-down of VSUP8.0AU

Note: If the above power-down procedure cannot be obeyed, the mute function of current power amplifier circuits has to be included into the shut-down process of the TV-set. An external voltage trace circuit (see Fig. 5–4 on page 1-59) observes the 5V supply VSUP5.0BE. If the supply voltages falls below the threshold (appr. 4 V), the circuit activates the mute input of the audio amplifier IC.

Note that this process only works properly on condition that the VCTI’s VSUP8.0AU must be hold up for at least 30 ms longer than the 3.3 V and the 5 V power supply to be traced.

3.7.2. Define Analog Input to DSP and AOUT1/2

1. Select analog input for the SCART processing path by means of the register Ana_DSP_In_Sel.
2. Set preferred prescale for SCART_IN processing path (SCART_Presc)
3. Select the sources for AOUT1 and AOUT2 using AOUT1/2_SEL.

3.7.3. Demodulator Setup

For a complete setup of the TV or Radio sound processing from DRX-SIF-input to the source selection, the following steps must be performed:

1. Set MODUS register to the preferred mode (Automatic Sound Select ASS = on is highly recommended).
2. Set preferred prescale (FM/AM and NICAM) values.
3. Write STANDARD SELECT register, applying either Automatic Standard Detection or specifying a concrete standard.

3.7.4. Loudspeaker and SCART Channel Setup

1. Select the source channel and matrix for each output channel (for ASS=on the matrix must be “stereo”)
2. Set audio baseband processing parameters
3. Select volume for each output channel.

3.7.5. Examples for Minimum Initialization Codes

Initialization of the MSP after Power-On according to these listings reproduces sound of the selected standard on the loudspeaker output. All numbers are hexadecimal. The examples have the following structure:

1. Perform an I^2C controlled reset of the IC (optional).
2. Perform Analog Power Configuration Setup (APC Setup)
3. Write MODUS register (ASS=on).
4. Set Source Selection for loudspeaker channel (with matrix set to STEREO).
5. Set Prescale Values for FM/AM and/or NICAM.
6. Write STANDARD SELECT register.
7. Set Volume loudspeaker channel: Automatic Standard Detection recommended

3.7.5.1. TV-Standard B/G (A2 or NICAM)

```
<8E 00 80 00>          // Soft reset (optional)
<8C 14 40 01>          // Analog Power-up configuration
<8C 10 00 30 00 03>    // Mod_StatInterr=1
                          Mod_ASS=1
<8C 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<8C 12 00 0E 24 00>    // FM/AM-Prescale = 24hex,
<8C 12 00 10 2D 00>    // NICAM-Prescale = 2Dhex
<8C 10 00 20 00 08>    // Standard Selection: Preferred Standard
<8C 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

3.7.5.2. TV-Standard M/N (BTSC,EIA-J, A2-Korea)

```
<8E 00 80 00>          // Soft reset (optional)
<8C 14 40 01>          // Analog Power-up configuration
<8C 10 00 30 00 03>    // Mod_BTSC=0
                          Mod_StatInterr=1
                          Mod_ASS=1
<8C 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<8C 12 00 0E 24 00>    // FM/AM-Prescale = 24hex,
<8C 10 00 20 00 20>    // Standard Select: Preferred standard
<8C 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

3.7.5.3. BTSC-SAP with SAP at Loudspeakers

```
<8E 00 80 00>          // Softreset (optional)
<8C 14 40 01>          // Analog Power-up configuration
<8C 10 00 30 80 03>    // Mod_BTSC=1 (BTSC-SAP)
                          Mod_StatInterr=1
                          Mod_ASS=1
<8C 12 00 08 04 20>    // Source Sel. = (St or B) & Ch. Matr. = St
<8C 12 00 0E 24 00>    // FM/AM-Prescale = 24hex,
<8C 10 00 20 00 20>    // Standard Select: BTSC-SAP
<8C 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

3.7.5.4. FM-Stereo Radio

```
<8E 00 80 00>          // Softreset (optional)
<8C 14 40 01>          // Analog Power-up configuration
<8C 10 00 30 00 03>    // Mod_FMRadio=0 or 1 (US/EU)
                          Mod_StatInterr=1
                          Mod_ASS=1
<8C 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<8C 12 00 0E 24 00>    // FM/AM-Prescale = 24hex,
<8C 10 00 20 00 40>    // Standard Select: FM-Radio
<8C 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

3.7.5.5. Automatic Standard Detection for D/K, applying STATUS-Change Interrupt

```
<8E 00 80 00>          // Softreset (optional)
<8C 14 40 01>          // Analog Power-up configuration
<8C 10 00 30 07 03>    // Mod_4_5MHz=3
                          Mod_6_5MHz=1
                          Mod_StatInterr=1
                          Mod_ASS=1
<8C 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<8C 12 00 0E 24 00>    // FM/AM-Prescale = 24hex,
<8C 12 00 10 2D 00>    // NICAM-Prescale = 2Dhex
<8C 10 00 20 00 01>    // Standard Select: Autom. Standard Det.
<8C 11 00 7E <8D dd dd>// Read STANDARD RESULT
// Wait until STANDARD RESULT contains a value ≤ 07FF
// IF STANDARD RESULT contains 0000
                       // error handling: set former standard or
                          derive standard from video information
// ELSE
<8C 12 00 00 73 00>    // Loudspeaker Volume 0 dB

Interrupt Handler:
<8C 11 02 00 <8D dd dd>// Read STATUS
// Adjust TV-display with given STATUS information
// Return from Interrupt
```

3.8. Manual Demodulator Programming Facilities

3.8.1. Source Channel Assigment if Automatic Sound Select is not applied

Fig. 3–2 shows the source channel assignment of demodulated signals in case of manual mode (ASS = off). Specific information can be found in Table 3–7 “Demodulator Source Channels in Manual Mode”.

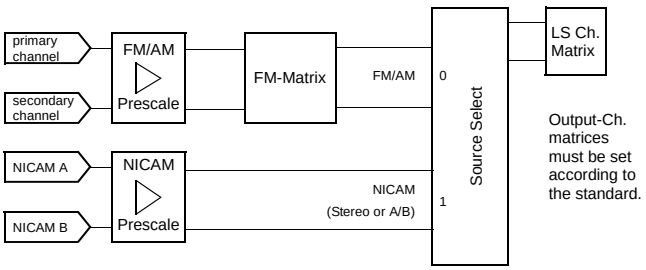


Fig. 3–2: Source channel assignment of demodulated

3.8.2. Manual Tuning

The DCO registers are useful to adapt the MSP to a non-documented sound standard. In that case it is recommended to start by means of the STANDARD SELECT register with the “nearest” implemented standard and then to adapt the frequency tuning by means of the DCO registers. To avoid any overwriting of this setting the Automatic Standard Change feature of the Automatic Sound Select feature has to be disabled. The formula for the calculation of the registers for any chosen IF Frequency is as follows:

$$INCR_{dec} = int(f/fs \cdot 2^{24})$$

with: int = integer function
f = IF frequency in MHz
f_S = sampling frequency (20.25 MHz)

Conversion of INCR into hex-format and dividing up into 12-bit high and low parts lead to the required register values (DCO_B_HI and_LO for the secondary MSP Channel, DCO_A_HI and LO for the primary MSP Channel.

Table 3–7: Manual Sound Select Mode for Terrestric Sound Standards

				Source Channels of Sound Select Block	
Broadcasted Sound Standard	**Selected MSP Standard Code**	**Broadcasted Sound Mode**	**FM Matrix**	**FM/AM** (use 0 for channel select)	**Stereo or A/B** (use 1 for channel select)
B/G-FM D/K-FM M-Korea M-Japan	03 04, 05 02 30h	MONO	Sound A Mono	Mono	Mono
		STEREO	German Stereo Korean Stereo	Stereo	Stereo
		BILINGUAL, Languages A and B	No Matrix	Left = A Right = B	Left = A Right = B
B/G-NICAM L-NICAM I-NICAM D/K-NICAM	08 09 0A 0B 0C	NICAM not available or NICAM error rate too high	Sound A Mono[1)]	analog Mono	analog Mono
		MONO	Sound A Mono[1)]	analog Mono	NICAM Mono
		STEREO	Sound A Mono[1)]	analog Mono	NICAM Stereo
		BILINGUAL, Languages A and B	Sound A Mono[1)]	analog Mono	Left = NICAM A Right = NICAM B
BTSC	20h (stereo)	MONO	Sound A Mono	Mono	Mono
		STEREO	Korean Stereo	Stereo	Stereo
		MONO + SAP	Sound A Mono	Mono	Mono
		STEREO + SAP	Korean Stereo	Stereo	Stereo
	20h (SAP)	MONO	Sound A Mono	Mono	Mono
		STEREO			
		MONO + SAP	No Matrix	Left = Mono Right = SAP	Left = Mono Right = SAP
		STEREO + SAP			
FM-Radio	40h	MONO	Sound A Mono	Mono	Mono
		STEREO	Korean Stereo	Stereo	Stereo

[1)] Automatic refresh to Sound A Mono, do not write any other value to the register FM Matrix!

4. Appendix: Overview of (TV) Sound Standards

4.1. NICAM 728

Table 4–1: Summary of NICAM 728 sound modulation parameters

Specification	I	B/G	L		D/K	
Carrier frequency of digital sound	6.552 MHz	5.85 MHz	5.85 MHz		5.85 MHz	
Transmission rate	728 kbit/s					
Type of modulation	Differentially encoded quadrature phase shift keying (DQPSK)					
Spectrum shaping Roll-off factor	by means of Roll-off filters					
	1.0	0.4	0.4		0.4	
Carrier frequency of analog sound component	6.0 MHz FM mono	5.5 MHz FM mono	6.5 MHz AM mono		6.5 MHz FM mono	
			terrestrial	cable		
Power ratio between vision carrier and analog sound carrier	10 dB	13 dB	10 dB	16 dB	13 dB	
Power ratio between analog and modulated digital sound carrier	10 dB	7 dB	17 dB	11 dB	China/ Hungary	Poland
					12 dB	7 dB

Table 4–2: Summary of NICAM 728 sound coding characteristics

Characteristics	Values
Audio sampling frequency	32 kHz
Number of channels	2
Initial resolution	14 bit/sample
Companding characteristics	near instantaneous, with compression to 10 bits/sample in 32-samples (1 ms) blocks
Coding for compressed samples	2’s complement
Preemphasis	CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz)
Audio overload level	+12 dBm measured at the unity gain frequency of the preemphasis network (2 kHz)

4.2. A2 Systems

Table 4–3: Key parameters for A2 Systems of Standards B/G, D/K, and M

Characteristics	**Sound Carrier FM1**			**Sound Carrier FM2**		
TV-Sound Standard	**B/G**	**D/K**	**M**	**B/G**	**D/K**	**M**
Carrier frequency in MHz	5.5	6.5	4.5	5.7421875	6.2578125 6.7421875 5.7421875	4.724212
Vision/sound power difference	13 dB			20 dB		
Sound bandwidth	40 Hz to 15 kHz					
Preemphasis	50 µs		75 µs	50 µs		75 µs
Frequency deviation (nom/max)	±27/±50 kHz		±17/±25 kHz	±27/±50 kHz		±15/±25 kHz
Transmission Modes						
Mono transmission	mono			mono		
Stereo transmission	(L+R)/2		(L+R)/2	R		(L–R)/2
Dual sound transmission	language A			language B		
Identification of Transmission Mode						
Pilot carrier frequency				54.6875 kHz		55.0699 kHz
Max. deviation portion				±2.5 kHz		
Type of modulation / modulation depth				AM / 50%		
Modulation frequency				mono: unmodulated stereo: 117.5 Hz dual: 274.1 Hz		 149.9 Hz 276.0 Hz

4.3. M/N-BTSC-Sound System

Table 4–4: Key parameters for BTSC-Sound Systems

	Aural Carrier	BTSC-MPX-Components				
		(L+R)	Pilot	(L–R)	SAP	Prof. Ch.
Carrier frequency (M: f_{hNTSC} = 15.734 kHz) (N: f_{hPAL} = 15.625 kHz)	4.5 MHz	Baseband	f_h	2 f_h	5 f_h	6.5 f_h
Sound bandwidth in kHz		0.05 - 15		0.05 - 15	0.05 - 12	0.05 - 3.4
Preemphasis		75 µs		DBX	DBX	150 µs
Max. deviation to Aural Carrier	73 kHz (total)	25 kHz[1)]	5 kHz	50 kHz[1)]	15 kHz	3 kHz
Max. Freq. Deviation of Subcarrier Modulation Type				AM	10 kHz FM	3 kHz FM
[1)] Sum does not exceed 50 kHz due to interleaving effects						

4.4. M-Japanese FM Stereo System (EIA-J)

Table 4–5: Key parameters for Japanese FM-Stereo Sound System EIA-J

	Aural Carrier FM	EIA-J-MPX-Components		
		(L+R)	(L–R)	Identification
Carrier frequency (f_h = 15.734 kHz)	4.5 MHz	Baseband	2 f_h	3.5 f_h
Sound bandwidth		0.05 - 15 kHz	0.05 - 15 kHz	–
Preemphasis		75 µs	75 µs	none
Max. deviation portion to Aural Carrier	47 kHz	25 kHz	20 kHz	2 kHz
Max. Freq. Deviation of Subcarrier Modulation Type			10 kHz FM	60% AM
Transmitter-sided delay		20 µs	0 µs	0 µs
Mono transmission		L+R	–	unmodulated
Stereo transmission		L+R	L–R	982.5 Hz
Bilingual transmission		Language A	Language B	922.5 Hz

4.5. FM-Stereo Radio and RDS

Table 4–6: Key parameters for FM-Stereo Radio Systems and RDS

	Aural Carrier	FM-Radio-MPX-Components			
		(L+R)	Pilot	(L–R)	RDS/ARI
Carrier frequency (f_p = 19 kHz)	DRX-dependent	Baseband	f_p ± 2 Hz	2 f_p	3 f_h ± 6Hz
Sound bandwidth in kHz		0.05 - 15		0.05 - 15	
Preemphasis: – USA – Europe		 75 µs 50 µs		 75 µs 50 µs	
Max. deviation to Aural Carrier	75 kHz (100%)	90%[1)]	10%	90%[1)]	5% RDS: ± 1.2kHz ARI: ± 3.5 kHz
[1)] Sum does not exceed 90% due to interleaving effects.					

Table 4–7: Summary of RDS modulation parameters (channel coding)

Specification	
Transmission rate	1.1875 kbit/s ± 0.125 bit/s
Type of modulation	Differentially encoded Biphase Coding
Spectrum shaping Roll-off factor	by means of Roll-off filter 1.0

4.6. Differences between the MSP part of VCTI and MSP 34/44xyG Stand-Alone Products

Table 4–8: Differences between the MSP part of VCTI and MSP 34/44xyG stand-alone products

Block	Feature	MSP 34/44xyG	MSP Part of VCTI	Comment
General	I^2C-Device Address Wr/Rd	$80/81_{hex}$; $84/85_{hex}$; $88/89_{hex}$ depending on ADR_SEL-Pin	$8C/8D_{hex}$	
	Device-Addr. of CONTROL	= MSP 34/44xyG Device Address	$8E/8F_{hex}$ (= Device-Addr. of DRX-Part)	
	Software-Reset via I^2C-Bus	Write CONTROL[15]=1 Write CONTROL[15]=0	Write CONTROL[15]=1 wait appr. 50 µs	
Demodulator	Programming-Modes	- Standard Select Register - manually	Standard Select Register only	
	Automatic Standard Change as part of Automatic Sound Select (ASS) in case of Mono	- for B/G and D/K-Standards - always active if ASS = on	- for B/G, D/K, and NTSC-Standards - to be disabled by MODU[2]	
	Result of Automatic Standard Detection	Regarding only Main-Carrier referring to MODUS[14:12]	indicating final Standard, if ASS and Autom. Stand. Change = on	
	Carrier-Mute: - Enable/Disable by - Dependent on Standard Sel. - Carrier Detect Threhold(s)	AD_CV[9] for both MSP-Chs. Standard Sel. enables Carr. Det. - CM_Threshold for both carriers	MODUS[9]: primary MSP-Ch. MODUS[10]: secondary MSP-Ch. independent of Standard Sel. CM_A_Thld: primary MSP-Ch. CM_B_Thld: secondary MSP-Ch.	VCTI: Automatic Carrier-Mute can be disabled while using Automatic Sound Select
	BTSC_Pilot Threshold	not available	Register “BTSC_Thld”	
	A2_Threshold - force Mono Identification	$07F0_{hex}$	$07FF_{hex}$	
	NICAM-Threshold	Register “AUTO_FM”	Register “NICAM_Thld”	Same I^2C-Address
	Setting for BTSC-SAP	Standard Select = 21_{hex}	MODUS[15] = 1; then - Standard Select = 20_{hex} or - Automatic Standard Detection	
	Select of FM-Radio US/EU	- Standard Select = 40_{hex} (US) - set EU-version by changing Deemphasis manually	- MODUS[11] = 0 : US (75 µs) = 1 : EU (50 µs) - Standard Select = 40_{hex}	VCTI: US/EU-Version can be predefined for Automatic Standard Detection
	Level of AM-demod. signal		+6 dB referring to MSP 34/44xyG	
	FM-Deviation-Modes: - max. Deviation - Activation of HDEV-Mode: - Level-difference between normal and HDEV(2) mode	normal: ±180 kHz. HDEV2: ±350 kHz HDEV3: > ±500 kHz by Standard Select Register –6 dB	normal: > ±200 kHz HDEV: > ±400 kHz by using MODUS[8] for each Code of Standard Select Register 0 dB	VCTI: max. Deviation also depends on Mode of DRX-Part
Baseband Process.	NICAM-Prescaling	00_{hex}...$7F_{hex}$: off ...+12 dB	00_{hex}.....$7F_{hex}$: off .....+ **18** dB	VCTI: 6 dB more gain possible for NICAM
Speaker Output	Output resistance	typ. 3.3 kOhm	typ. 330 Ohm	
	max. Output-Level (VSUP8.0 = 8 V)	1.4 Vrms	2 Vrms	
	DC-Level	Volume = 0 dB: appr. 2 V Volume = –30 dB: appr. 0.06 V	constant: appr. 3.7 V	
	Power-up/down conditions to avoid plops	reduce Volume to –30 dB at power down	apply Analog-Power-Up Configuration Register	

5. Data Sheet History

1. Advance Information: “VCT 49xyl, VCT 48xyl Multistandard Sound Processor”, Dec. 04, 2003, 6251-573-3-1AI. First release of the advance information.

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Contents

Contents, continued

1. Introduction

Volume 4 describes the Video Processor (VSP) of the VCT 49xyl, VCT 48xyl.

1.1. Chip Architecture

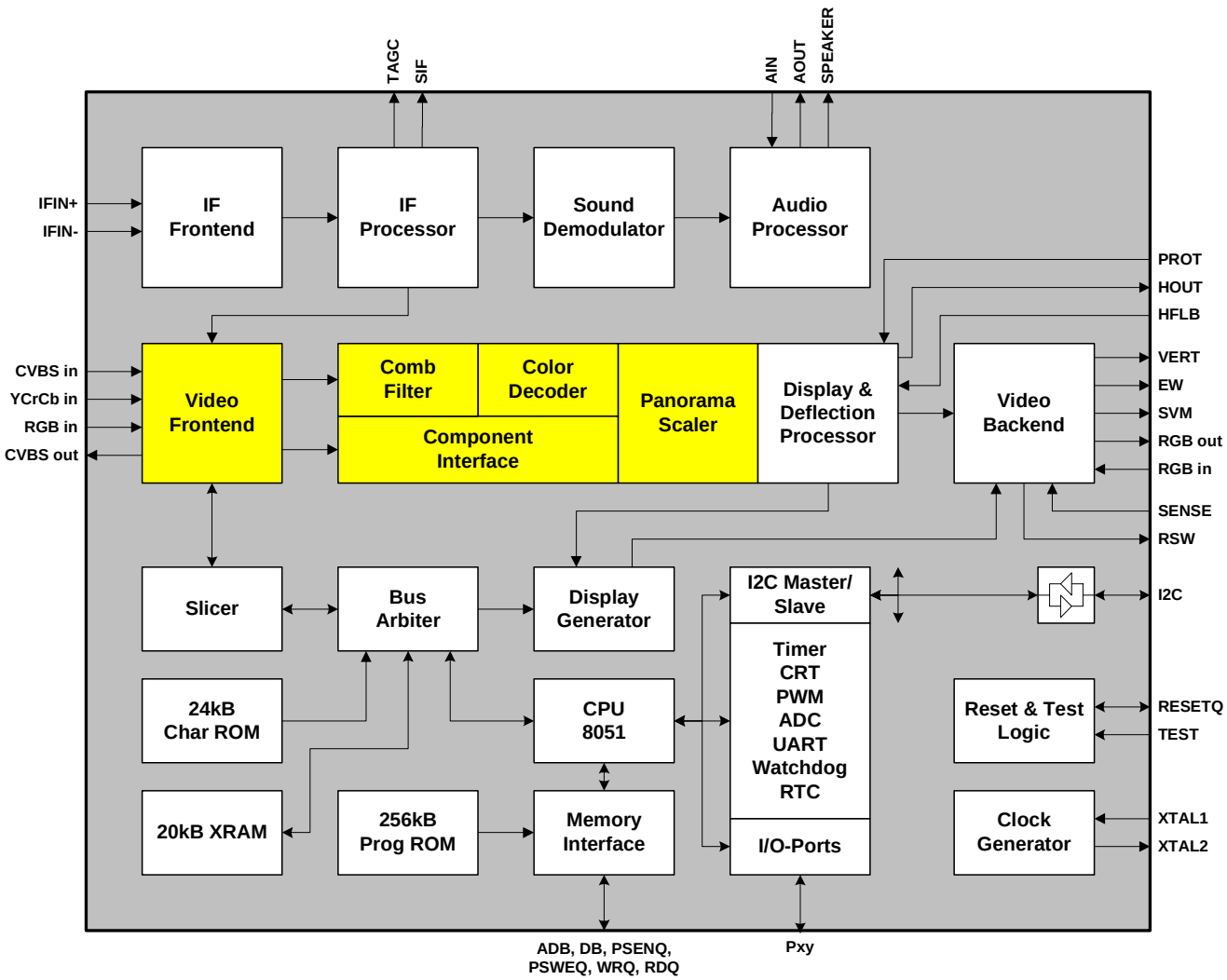


Fig. 1–1: Block diagram of the VCT 49xyl, VCT 48xyl

1.2. Video Features

– 11 analog video inputs (CVBS/Y/C/RGB/YCrCb)

– 3 analog video outputs

– integrated Y+C adder

– integrated high-quality A/D converters and associated clamp and AGC circuits

– high-performance 4H comb filter (PAL/NTSC) with vertical peaking

– multistandard color decoder PAL/NTSC/SECAM including all substandards

– macrovision-compliant multistandard sync processing

– RGB/YC, C_b component processing and associated contrast, color saturation and tint circuits

– high-quality soft mixer controlled by fast blank (alpha blending)

– fast blank monitor via I^2C

– linear horizontal scaling (0.25 to 4)

– nonlinear horizontal scaling “panorama vision”

– split screen (OSD and video side by side)

– letter box detector (auto-wide)

– SNR measurement

2. Functional Description

2.1. Source Select

2.1.1. Analog Source Select

The VSP provides 11 analog video inputs. The DRX delivers an additional CVBS signal. Internally, three additional CVBS signals are generated.

The analog source select connects these 15 analog input sources to 6 ADCs and to 3 analog outputs (see Fig. 2–1). It also delivers the clamping signals to the selected inputs.

VINSEL1-6 route the input signals to ADC1-6. ***VOUTSEL1-3*** route the input signals to the analog video outputs VOUT1-3.

While all inputs can be used to process Y/C signals, only VIN3&4, VIN5&6 or VIN7&8 support Y/C to CVBS conversion.

The clamped input signals are lowpass-filtered, amplified and converted to digital signals.

Video recording in standby (copy-mode) is supported by ***STANDBYADC1-6*** switching off the ADCs and keeping the source-selector and the output buffers operational. The output buffers can be disabled independently by ***STANDBYBUF1-3***.

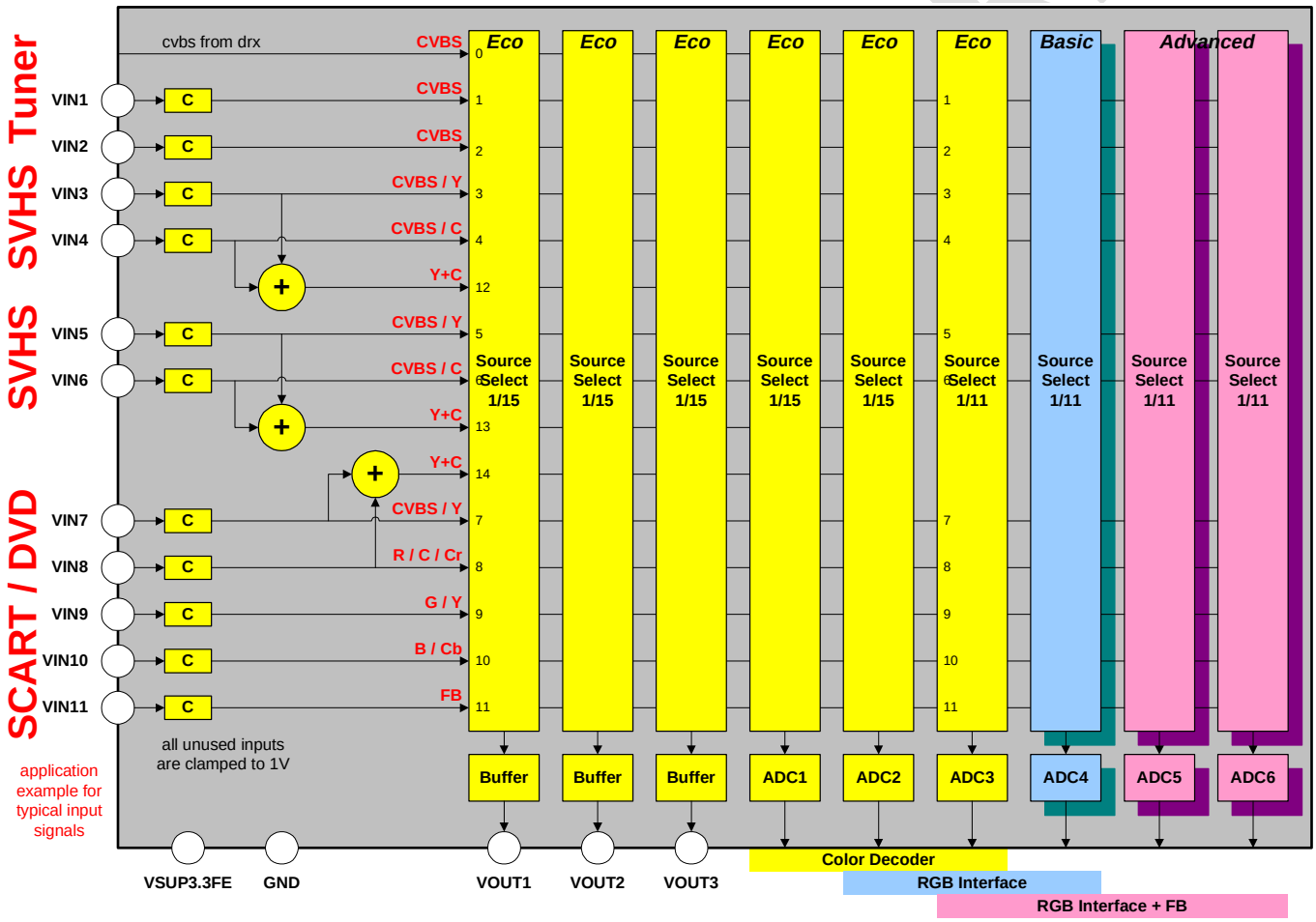


Fig. 2–1: Input Selection

2.1.2. Digital Source Select

In normal operation, color decoder and teletext slicer share the same CVBS signal. Nevertheless, as two ADCs are available, it is possible to use different sources for color decoder and slicer. Therefore, an additional switching matrix is implemented to select the appropriate source for each module. A second switching matrix connects clamping and agc signals from color decoder and slicer with the corresponding ADC (see Fig. 2–3). The inputs for color decoder and teletext slicer (***CVBS2LF***, ***DCVBSVBI***) are connected to the A/D converter via switching matrices and a comb filter. Depending on ***COMBUSECD*** and ***COMBUSEVBI***, ADC1, ADC2 or the comb filter are selected as signal source. Color decoder and sync signals used in the comb-filter are selected in the comb filter interface (see Fig. 2–2).

Table 2–1: Color Decoder Input Select

COMBUSECD	YCBYR	CVBS2LF	DCVBS2CD
0	0	cvbs1	chroma
	1		adcr
1	0	cvbs2	cvbs2
	1		adcr
2	X	ycomb	ccomb
3	0	adcgf	adcgf
	1		adcr

Table 2–2: Teletext Slicer Input Select

COMBUSEVBI	DCVBSVBI
0	cvbs1
1	cvbs2l
2	ycomb
3	adcgf

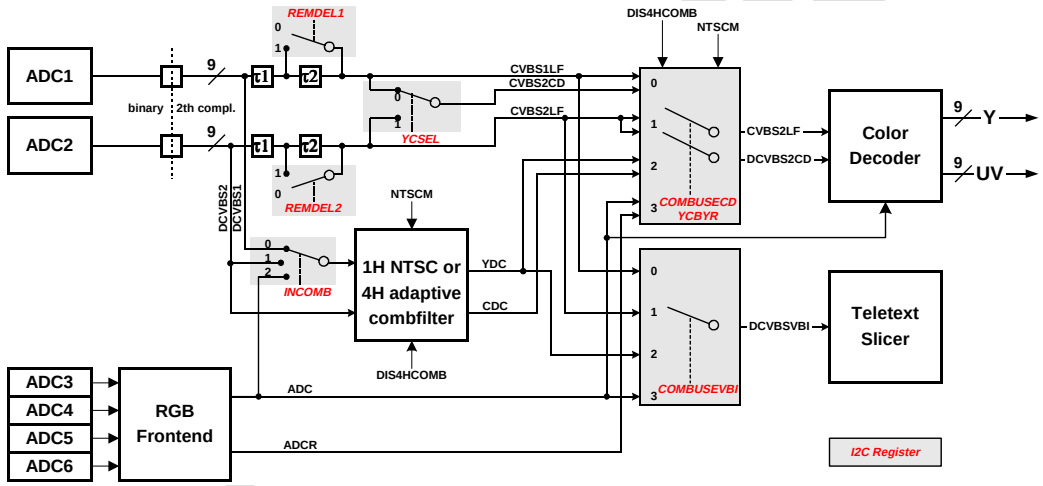


Fig. 2–2: CVBS Frontend

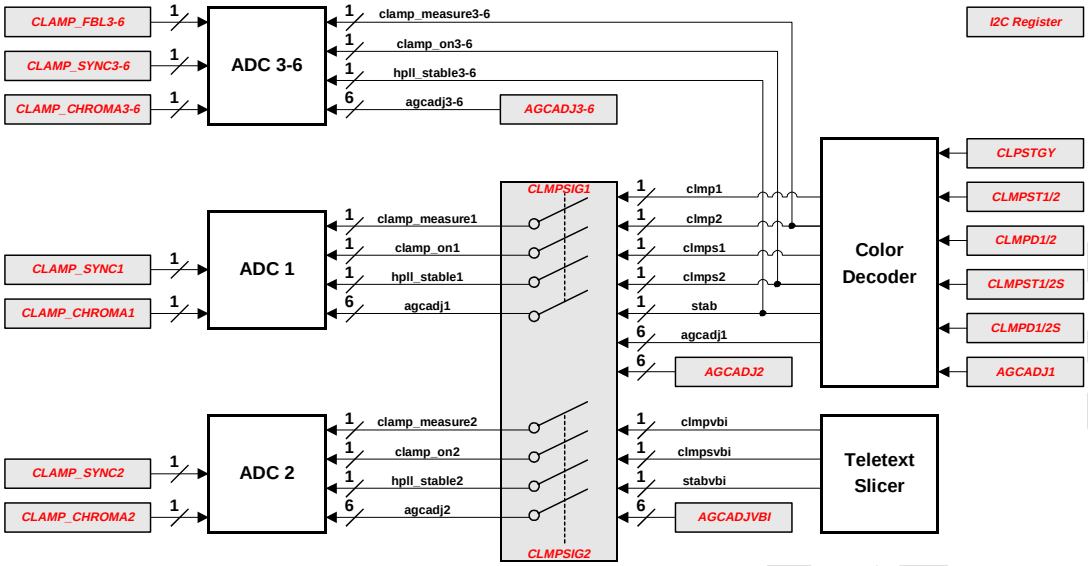


Fig. 2–3: Clamping Mux

2.1.3. Signal Magnitudes and Gain Control

To adjust to different CVBS input voltages a digitally working automatic gain control with 64 linear steps is implemented for input voltages ranging from 0.5 V_{pp} to 1.5 V_{pp}. The AGC behavior depends on ***AGCMD***.

Table 2–3: AGC operation mode

AGCMD	AGC Operation Mode
00	AGC uses the height of the sync pulse as a reference and additionally reduces amplification when ADC overflows.
01	AGC uses the height of the sync pulse as a reference.
10	AGC uses ADC overflows only. The gain is set to maximum and is reduced whenever an “overflow” occurs.
11	AGC is disabled and the gain is manually adjusted by **AGCADJ1-2.**

The signal is lowpassed so that chrominance and noise do not disturb the AGC.

The AGC overflow detector is adjustable via ***PWTHD***. A manual reset by ***AGCRES*** or a channel change will force the AGC to restart. ***AGCFRZE*** stops the AGC measurement.

2.1.4. Clamping

The clamp timing for the analog inputs is internally generated by the H-PLL. The clamping algorithm works with independent *measurement* and *clamping* pulses. The measurement pulse is used to detect the clamping error. The clamping pulse is used to enable current sources for reducing the detected clamping errors.

There are 2 independent sets of clamping signals available.

Start and length of the measurement signals 1 and 2 can be adjusted via ***CLMPD1[3:0]***, ***CLMPD2[3:0],*** ***CLMPST1[5:0]*** and ***CLMPST2[5:0]***. Start and length of the clamping signals 1 and 2 can be adjusted via ***CLMPD1S[3:0]***, ***CLMPD2S[3:0],*** ***CLMPST1S[5:0]*** and ***CLMPST2S[5:0]***.

Clamping can be suppressed during vertical blanking by ***CLMPLOW[3:0]*** and ***CLMPHIGH[7:0]*** to ignore copy protection information.

Table 2–4: Clamping Adjustment

Signal	Description
CLMPST1/2	measurement start 1/2
CLMPD1/2	measurement duration 1/2
CLMPST1/2S	clamping start 1/2
CLMPD1/2S	clamping duration 1/2

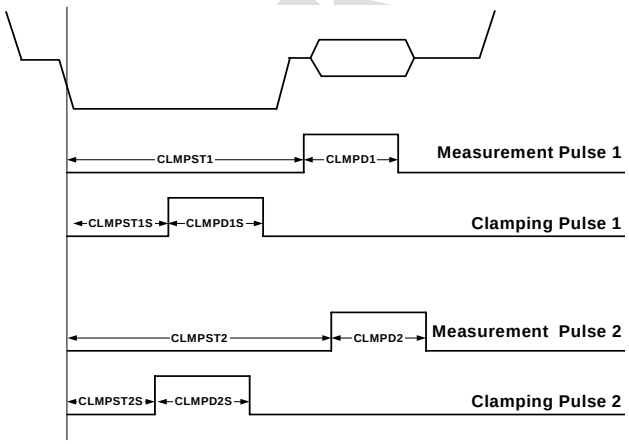


Fig. 2–4: Clamping signals

2.2. CVBS Frontend

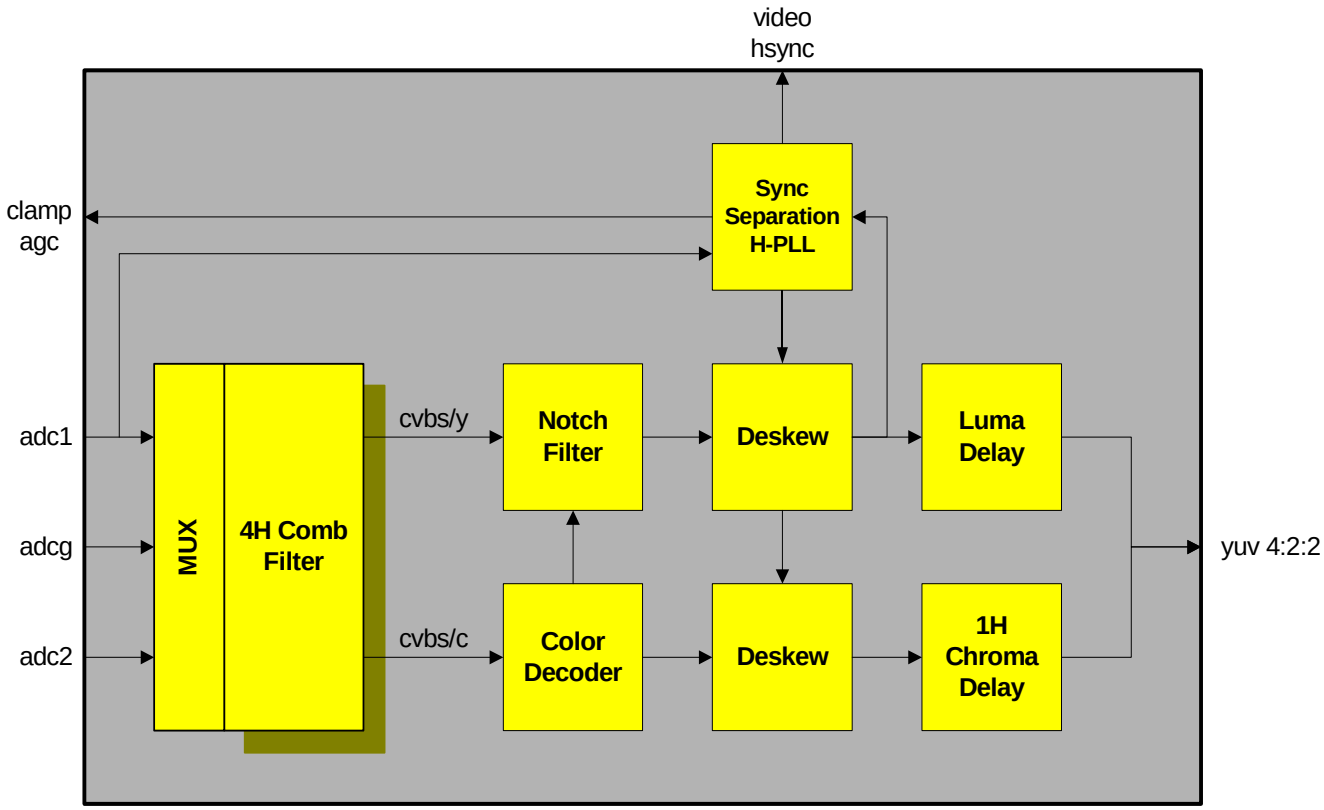


Fig. 2–5: Comb filter and color decoder

The CVBS frontend consists mainly of four parts, the 4H comb filter, the notch filter, the color decoder and a synchronization circuit. The 4H comb filter separates luminance and chrominance information from the CVBS input signal, while the notch filter removes the color carrier in no comb mode. The color decoder decodes the input CVBS signal to Cr and Cb. The sync processing circuit separates the H/V sync out of the input signal. Additionally a skew correction filter and a baseband delay line are used. In PAL and SECAM mode the baseband delay line is used for Cr and Cb. In NTSC mode it acts as comb filter for chroma.

A switching matrix in front of the color decoder interfaces to the 4H comb filter or to the ADC modules. The output signals of the color decoder are fed to the Softmix.

2.2.1. Comb Filter

The 4H adaptive comb filter is used for high quality luminance/chrominance separation for PAL or NTSC composite video signals. The comb filter improves the luminance resolution (bandwidth) and reduces interferences like cross-luminance and cross-color. The adaptive algorithm eliminates most of the mentioned errors without introducing new artifacts or noise.

The comb-filter input can be selected by ***INCOMB.*** First or second CVBS ADC or green ADC can be used. The filter uses four line delays to process the information of three video lines. To have a fixed phase relationship of the color subcarrier in the three channels, the digital data is fractionally locked to the color subcarrier. This allows the processing of all color standards and substandards using a single crystal frequency.

The comb filter uses the middle line as reference, therefore, the comb filter delay is two lines. If the comb filter is switched off, (***DISCOMB***), the delay lines are used to pass the luma/chroma signals from the A/D converters to the luma/chroma outputs (***YCTCOMB***). Thus, the processing delay always consists of two lines.

In order to obtain the most optimal picture quality, the user has the possibility to influence the behavior of the adaption algorithm going from moderate combing to strong combing. Therefore, the following three parameters can be adjusted:

HDG (horizontal difference gain)

VDG (vertical difference gain)

DDR (diagonal dot reducer)

HDG typically defines the comb strength on horizontal edges. It determines the amount of the remaining cross-luminance and the sharpness on edges respectively. As HDG increases, the comb strength, e.g., cross-luminance reduction and sharpness, increases.

VDG typically determines the comb filter behavior on vertical edges. As ***VDG*** increases, the comb strength, e.g., the amount of hanging dots, decreases.

After selecting the comb filter performance in horizontal and vertical direction, the diagonal picture performance may further be optimized by adjusting ***DDR***. As ***DDR*** increases, the dot crawl on diagonal colored edges is reduced.

2.2.2. Color Decoder

The digital multistandard chroma decoder decodes NTSC and PAL signals with a subcarrier frequency of 3.58 MHz and 4.43 MHz (PAL B/G/H/I/M/N/60, NTSC M/44) as well as SECAM signals with automatic standard detection. Alternatively, a standard can be forced. The demodulation is done with a regenerated color carrier.

For use of non-standard crystals or factory adjustment, the frequency of the free-running regenerated subcarrier can be adjusted between ±270 ppm via ***SCADJ***. For this purpose the crystal deviation (***SCDEV***) can be read out via I²C after chroma PLL locking (indicated by ***SCOUTEN***) and can be stored in µC ROM for ***SCADJ***. For test purposes, ***CPLLOF*** allows a loop opening of the chroma PLL. The delay between Y and C is well aligned and can also be adjusted in steps of 50ns (***YCDEL***).

A delay-line is implemented for PAL and SECAM signals. It acts as a simple chrominance comb filter for NTSC to reduce cross-color and can be disabled by ***COMB.***

2.2.3. IF-Compensation

With off-air or mistuned reception, any attenuation at higher frequencies or asymmetry around the color subcarrier is compensated. Five different settings (***IFCOMP***) of the IF compensation are possible:

– Flat (no compensation)
– 6 dB/octave
– 12 dB/octave
– 4.4 MHz prefiltering (with or without prefiltering)

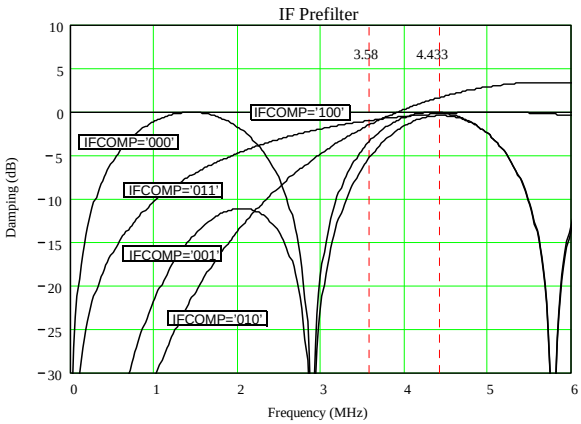


Fig. 2–6: IF prefilter

2.2.4. Chrominance Filter

The demodulation is followed by a lowpass filter for the color difference signals for PAL/NTSC. SECAM requires a modified lowpass function with bell filter characteristic. For SECAM mode, the de-emphasis filter can be adjusted by ***DEEMPFIR*** and ***DEEMPIIR***. A wide band chroma filter can be selected. This filter is intended for high bandwidth chroma signals, e.g., S-VHS signal or when comb filter is enabled. The chroma bandwidth can be adjusted by ***CHRF*** (see Fig. 2–7).

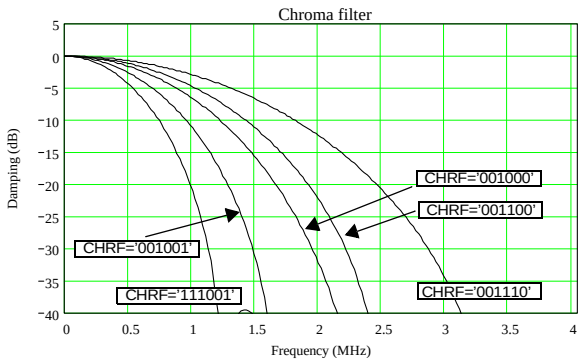


Fig. 2–7: Chroma filter characteristics

2.2.5. Automatic Standard Recognition (ASR)

The ASR supports the following standards:

– 50 Hz: PAL B/N, SECAM
– 60 Hz: NTSC M/44, PAL M/60

The automatic detection can be disabled and single standards can be forced.

This standard detection process can be set to slow or fast behavior **(*LOCKSP*).** In slow behavior, 25 fields are used to detect the standard, whereas 15 fields are used in fast behavior. If unsuccessful within this time period the system tries to detect another standard.

For SECAM detection, a choice between different recognition levels is possible (***SCMIDL, SCMREL***) and the evaluated burst position is selectable (***BGPOS***).

Color standard (***STDET***), line standard (***LNSTDRD***) and color killer status (***CKSTAT***) can be read out.

Table 2–5: Allowed combinations for 60 Hz standards

Standard	CSTAND			
(60 Hz)	D6	D5	D4	D3
None	0	0	0	0
PAL60	0	0	0	1
PAL M	0	0	1	0
NTSC M	0	1	0	0
NTSC44	1	0	0	0
Automatic PAL M/NTSC M	0	1	1	0
Automatic NTSC M/NTSC44/PAL60	1	1	0	0(!)

Table 2–6: Allowed combinations for 50 Hz standards

Standard	CSTAND		
(50 Hz)	D2	D1	D0
None	0	0	0
PAL N	0	0	1
PAL B	0	1	0
SECAM	1	0	0
Automatic PAL B/SECAM	1	1	0

2.2.6. Color Saturation Control

In the PAL/NTSC system the burst is the reference for the color signal. An Automatic Chroma Control (ACC) produces a stable output for input chroma variations from (approximately) –30 dB to +6 dB compared to nominal burst value. The ACC reference value is programmable for NTSC and PAL independently (***NTSCREF***, ***PALREF***) to ensure correct color saturation.

With ***ACCFIX***, the ACC is disabled and a constant value (dependent on ***NTSCREF*** and ***PALREF***) is used. ***ACCFRZ*** stops the ACC measurement. The maximum amplification of the ACC is limited by ***ACCLIM.*** This results in a smooth attenuation of color intensity for weak color carrier (see Fig. 2–8).

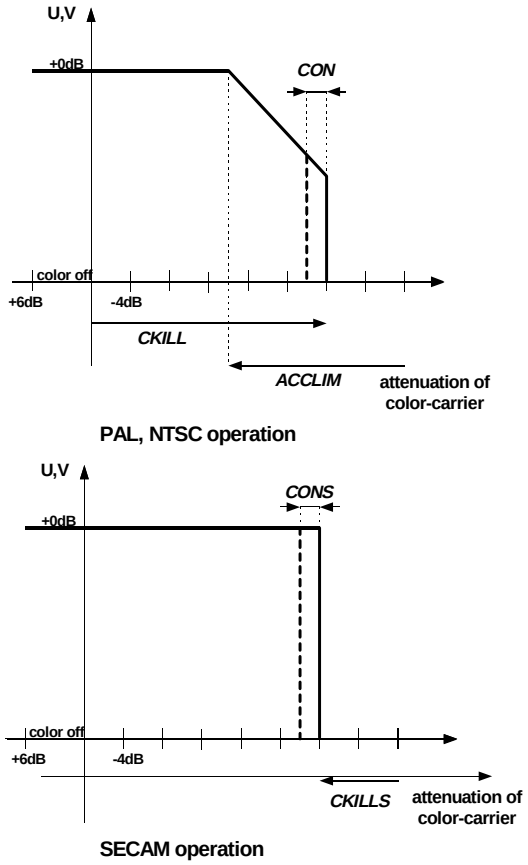


Fig. 2–8: Color killer adjustment

For NTSC only, the color impression (tint) can be adjusted by the hue control between –88° and 90° in steps of 0.7° (***HUE***).

2.2.7. Color Killer

If the chrominance signal is below an adjustable threshold (***CKILL*** (PAL; NTSC) or ***CKILLS*** (SECAM)) the color is switched off. To prevent on/off switching, a hysteresis is given by ***CON*** or ***CONS*** which is the value of switching on the color. ***COLON*** switches on the color under any circumstance.

2.2.8. Luminance Processing

A luminance notch filter is implemented to reject the chroma information from luminance. The notch frequency depends on the color standard (PAL/NTSC/SECAM). The filter characteristic is adjustable by ***NTCHSEL*** (see Fig. 2–9 to Fig. 2–12).

NOTCHOFF automatically disables or enables the notch filter depending on color standard. ***TNOTCHOFF*** always disables the notch filter.

A simple lowpass-filter is enabled by ***LPPOST*** to reduce high-frequency noise component from the CVBS signal.

Table 2–7: Notch-filter

NOTCHOFF	TNOTCHOFF	Notch-filter
0	0	Always enabled
0	1	Always disabled
1	0	Depending on color standard
1	1	Always disabled

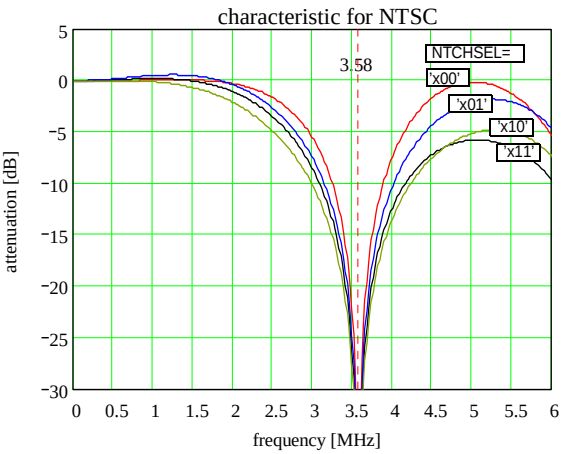


Fig. 2–9: Filter characteristics for NTSC, PAL M and PAL N

.

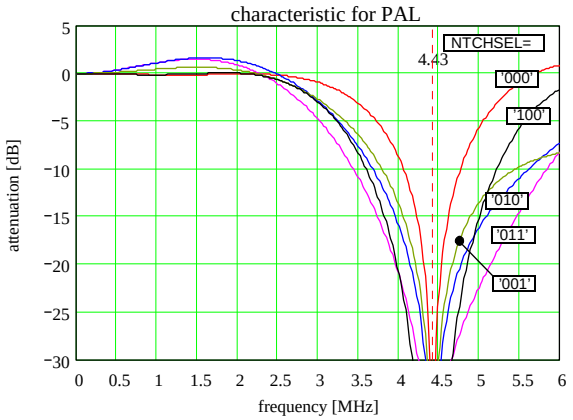


Fig. 2–10: Filter characteristics for PAL B/G, NTSC44, PAL60

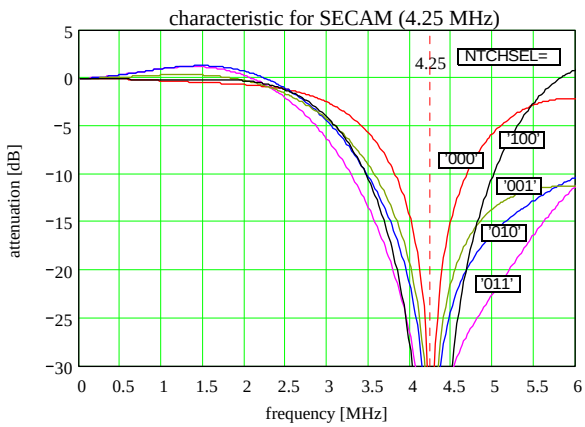


Fig. 2–11: Filter characteristics for SECAM (*SECNTCH*='01', 4.25 MHz)

For applications for which a black offset is not desired, controlling may be done using ***LMOFST*** (see Fig. 2–12). The positive or negative offset is added to the Y signal.

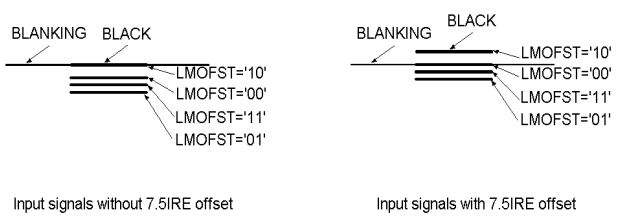


Fig. 2–12: Adjustment of “Black” to “Blanking value”

2.2.9. Synchronization

After elimination of the high frequency components of the CVBS signal by a low pass filter, horizontal and vertical sync pulses are separated. Horizontal sync pulses are generated by a digital phase locked loop. The time constant can be adjusted between fast and slow behavior in four steps (***PLLTC***) to accommodate different input sources (e.g. VCR). The time-constant can be changed during normal operation without visible picture degradation. A fine tuning of the PLL time constant can be done by ***NSRED***.

Additionally weak input signals from a satellite dish ('fish') become more stable when ***SATNR*** is enabled. Vertical sync pulses are separated by integration of equalizing pulses. A vertical flywheel mode improves vertical sync separation for weak signals (***VFLYWHL, VFLYWHLMD***).

Additionally, v-syncs may be gated by ***VTHRL*** and ***VTHRH*** to reject invalid v-syncs (independently adjustable for 50 and 60 Hz sources). When no input signal is connected the device switches to a free-running mode. The device can be configured to switch-on background color when no or only a weak signal is applied (***NOSIGB***). 50 Hz or 60 Hz operation for sync separation may be forced separately or selected to work automatically (***FLNSTRD***).

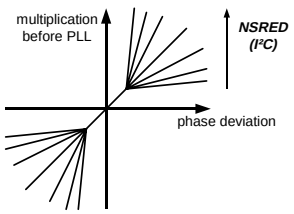


Fig. 2–13: NSRED characteristics

2.3. RGB Frontend

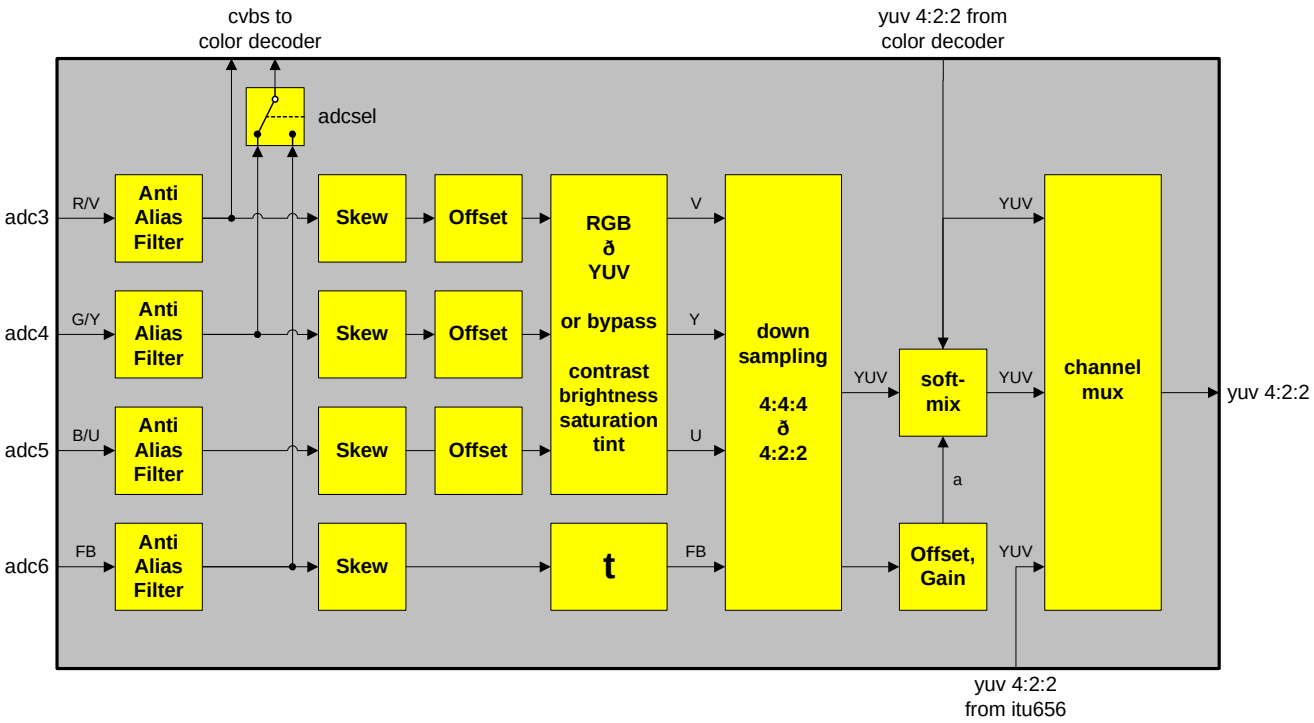


Fig. 2–14: Component Interface

The VSP provides an analog component interface, either for RGB or YCrCb/YPrPb. For input source selection see Section 2.1.1. on page 4-6. The component processing is synchronized either by the main CVBS or by the component input signal.

The clamped and digitized signals are filtered, converted to the common YCrCb color space and downsampled to 4:2:2.

In soft mix mode, the 4:2:2 component signal is overlaid onto the main video signal. This mode requires a component signal synchronous to the main CVBS/YC signal.

2.3.1. Signal Magnitudes and Gain Control

Each ADC can be gain adjusted by ***AGCADJR***, ***AGCADJG***, ***AGCADJB***, ***AGCADJF***

2.3.2. Clamping

The analog clamping value of all component inputs can be adjusted independently by ***CLAMP_SYNC, CLAMP_RGB*** and ***CLAMP_CHROMA***. Depending on the input signal format (YUV, RGB, sync signal or not) these bits must be set accordingly. On the digital side, a correction of the analog clamping value must be performed to reconstruct the black level. This is achieved by ***RBOFST*** and ***GOFST***. When using the dynamic softmix-mode with fast-blank, clamping of fast-blank input must be disabled by ***CLAMP_FBL***.

2.3.3. Digital Prefiltering

To reduce the bandwidth of very steep input signals, such as characters, a digital prefilter can be enabled. Two different characteristics are available via ***AASEL***. The filtering is performed in all four channels and can be disabled by ***AABYP***. For signal conversion to 4:2:2, an additional chrominance lowpass can be enabled by ***CHRSF***.

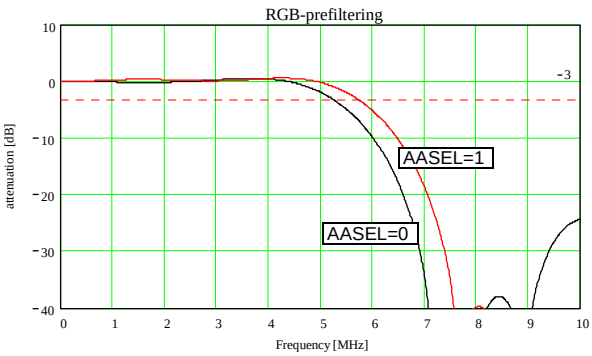


Fig. 2–15: Digital Prefiltering of RGB input

Table 2–8: Configurations of input signals

Mode	Clamp Reference	GOFST	RBOFST	CLAMP_FBL
YUV, sync on Y	160/256/256	128	256	don't care
YUV, sync on H,V	32/256/256	0	256	0 (clamping enabled)
RGB, sync on G	160/32/32	128	0	don't care
RGB, sync on RGB	160/160/160	128	128	don't care
RGB, sync on H,V	32/32/32	0	0	0 (clamping enabled)
RGB with fast-blank, synchronous to CVBS	32/32/32	0	0	1 (clamping disabled)
YUV with fast-blank, synchronous to CVBS	32/256/256	0	256	1 (clamping disabled)

2.3.4. RGB/YPbPr to YCrCb Matrix

RGB or YPbPr signals are converted to the YCrCb format by a matrix operation (***YUVMAT***). In case of YCrCb input the matrix is bypassed (***YUVSEL***).

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} R \\ G \\ B \end{bmatrix} \cdot \begin{bmatrix} 0{,}299 & 0{,}587 & 0{,}114 \\ -0{,}169 & -0{,}331 & 0{,}500 \\ 0{,}5 & -0{,}419 & -0{,}081 \end{bmatrix}$$

Fig. 2–16: RGB to YCrCb matrix (CCIR)

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} Pr \\ Y \\ Pb \end{bmatrix} \cdot \begin{bmatrix} 0{,}191 & 1 & 0{,}075 \\ -0{,}108 & 0 & 0{,}991 \\ 0{,}991 & 0 & -0{,}054 \end{bmatrix}$$

Fig. 2–17: YPbPr to YCrCb matrix (BTA)

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} Pr \\ Y \\ Pb \end{bmatrix} \cdot \begin{bmatrix} 0{,}196 & 1 & 0{,}102 \\ -0{,}111 & 0 & 0{,}991 \\ 0{,}988 & 0 & -0{,}073 \end{bmatrix}$$

Fig. 2–18: YPbPr to YCrCb matrix (CCIR)

2.3.5. Component YCrCb Control

The following picture adjustment parameters on the component signal are supported:

– 0 ≤ contrast ≤63/32 (***CONADJ)***
– –128 ≤ brightness ≤ 127 (***BRTADJ)***
– 0 ≤ saturation C_r ≤ 63/32 (***VSATADJ***)
– 0 ≤ saturation C_b ≤ 63/32 (***USATADJ***)
– -45° ≤ tint ≤ +45° (***TINT***)

The delay of luminance and fast-blank is adjustable by ***YFDEL***, while the chrominance delay is adjustable by ***UVDEL***.The fast-blank delay is fine-tuned by ***FBLDEL***.

2.3.6. Soft Mix

The softmixer circuit consists of a Fast Blank (FB) processing block supplying a mixing factor k (0... 128) to a high-quality signal mixer achieving the output function:

$$YUVmix = \frac{YUV_{main} \cdot (128 - k) + YUV_{inserted} \cdot k}{128}$$

k=”0” means that only the main signal is fed through to the output. k=”128” means that only the inserted signal becomes visible. The mixing is done once for the luminance and once for the chrominance in the subsampled domain (4:2:2). The softmixer supports four modes that are selected by ***MIXOP*** and ***SMOP.***

Table 2–9: RGB operation modes

MIXOP	SMOP	Softmix-mode
00	0	Dynamic Soft-Mix
00	1	Static Soft-Mix
01	x	Only RGB/YUV path visible
10	x	Only CVBS path visible
11	x	(Reserved)

2.3.6.1. Static Switch Mode

In its simplest and most common application the softmixer is used as a static switch between YUVmain and YUVinsert. This is for instance, the adequate way to handle a DVD component signal. By using ***MIXOP***, k is internally set to 0 or 128 respectively.

2.3.6.2. Static Mixer Mode

The signal YUVmain and the component signal YUVinsert may also be statically mixed. In this environment, k is manually controlled via ***FBLOFFST*** and ***MIXGAIN***.

$$k = MIXGAIN \cdot (31 - FBLOFFST) + 32$$

All necessary limitation and rounding operations are built-in to fit the range: 0 ≤ k ≤ 128.

Considering ***MIXGAIN***=3, k is obtained by:

$$k = 158 - 3 \cdot FBLOFFST$$

k limited to 0 and 128

The mixing is only controlled by ***FBLOFFST***.

In the static mixer mode as well as in the previously mentioned static switch mode, the softmixer operates independently of the analog fast blank input.

2.3.6.3. Dynamic Mixer Mode

In the dynamic mixer mode, the mixer is controlled by the Fast Blank signal. The VSPB provides a linear mixing coefficient.

$$k = \frac{MIXGAIN(FB - FBLOFFST \cdot 2)}{2} + 64$$

The dynamic mode is used for mixing which is dependent on FB input. FB is the preprocessed digitized fast-blank input in the range from 0...127. FBL manipulation is done both for luminance and chrominance FBL signal.

Fast blank is delay adjustable by ***FBLDEL*** in the range of –2...4 clock cycles.

2.3.7. Fast Blank Activity and Overflow Detection

It is important to know whether the FBL input is used or not. Therefore a detection circuit gives information via the I²C bus to the microcontroller. The circuit uses the digitized FBL as input. If it is greater than a threshold for one or five clock cycles (***FBLCONF***), the I²C bit ***FBLACTIVE*** is set. This bit is reset when it is read by the microcontroller.

For a detailed SCART signal ident analysis by the microcontroller, the fast blank monitor provides additional status information (see Fig. 2–19):

– ***FBSTAT***: FB status at register read

– ***FBRISE***: set by FB rising edge, reset by register read

– ***FBFALL***: set by FB falling edge, reset by register read

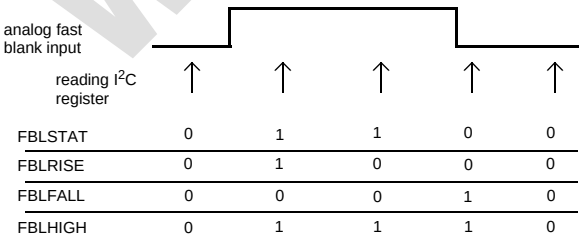


Fig. 2–19: Fast Blank Monitor

PFBL, ***PG***, ***PR***, ***PB*** indicate an overflow of the corresponding ADC (upper limit: ADC=511) exceeding 5 clock cycles duration. These signals are also set by overflow and reset by I²C read only.

2.4. Picture Measurement and Horizontal Scaler

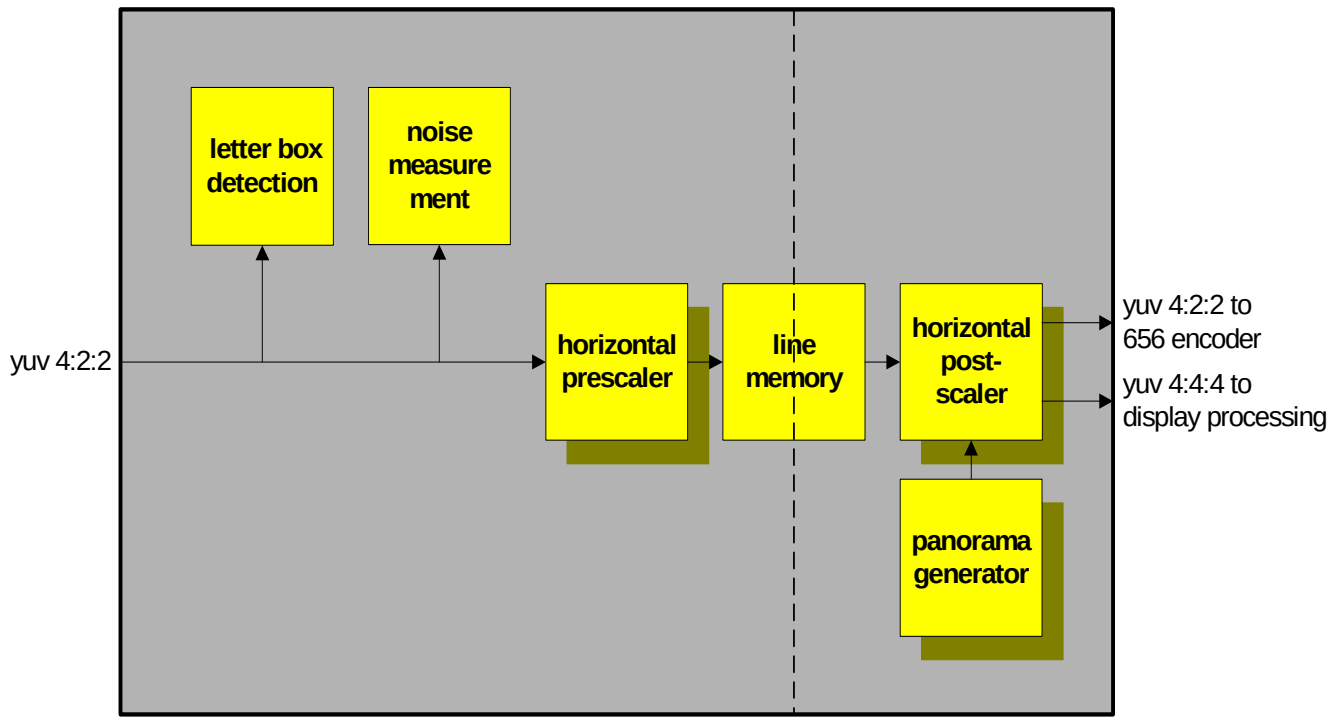


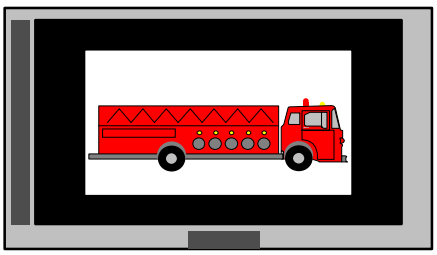
Fig. 2–20: Picture Measurement and Horizontal Scaler

2.4.1. Noise Measurement

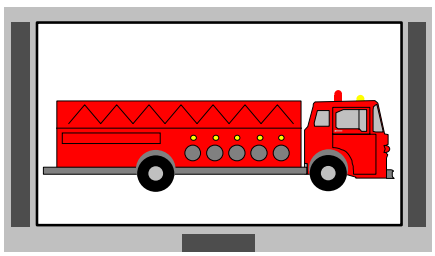
The noise measurement detects noise in the vertical blanking interval. The line used for noise measurement is selected by ***NMLINE***. The measurement position inside selected line can be adjusted (***NMPOS***) as well as the sensitivity (***NMSENSE***). The noise level can be used to change some parameters adaptively. For example, the sharpness can be reduced by much noise or the synchronization can be set to slower time-constant.

2.4.2. Letter Box Detection

A drawback of wide screen 16:9 TV sets are the black bars on the left and the right side on the screen when displaying a 4:3 source on a 16:9 screen with correct aspect ratio. In the case of letter box source material, even black bars across the top and bottom exist. With the help of an expansion algorithm, it is possible to expand the letter box picture vertically and horizontally so that the letter box picture will fill the complete screen without loosing information (see Fig. 2–21). To do so, the information on the active part of the letter box picture is necessary. Active part means the information about the first active line and the last active line of the letter box picture.



4:3 Letter Box Picture



Expanded Letter Box Picture

Fig. 2–21: Handling of Letter Box pictures on 16:9 tubes

The WSS (Wide Screen Signal) signal contains information on the picture format (4:3 or 14:9 or 16:9), but not all existing formats are covered and not all signals

contain WSS. Therefore, a separate algorithm is necessary which delivers the necessary information. Fig. 2–22 shows the concept of the letter box detection. One part of the algorithm is dedicated hardware and located in the VSP, another part is software and located in the RAM of the TV microcontroller. The part located in VSP is called measurement part. The measurement part delivers 5 signals to the controller part. Based on the delivered information the controller part calculates an expansion and a vertical pan factor and sends these values back to the VSP for manipulation of the video signal.

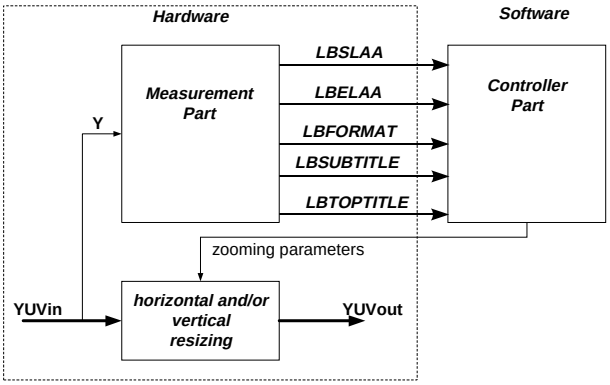


Fig. 2–22: HW/SW Partitioning of Letter Box Detection

The input picture is separated in one upper and one lower part (see Fig. 2–23). The measurement windows are defined by the parameters ***LBVWSTUP***, ***LBVWENDUP*** (upper vertical measurement window), ***LBVWSTLO***, ***LBVWENDLO*** (lower measurement window) and ***LBHWST***, ***LBHWEND*** (horizontal measurement window).

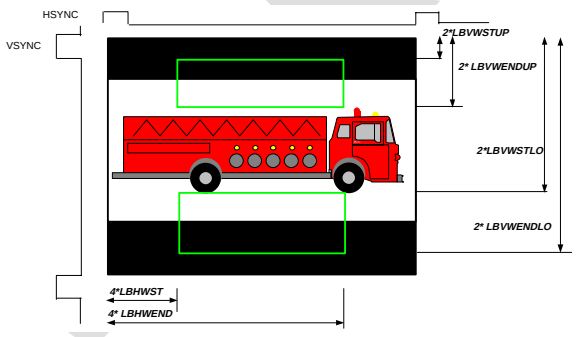


Fig. 2–23: Measurement windows

2.4.3. Horizontal Prescaler

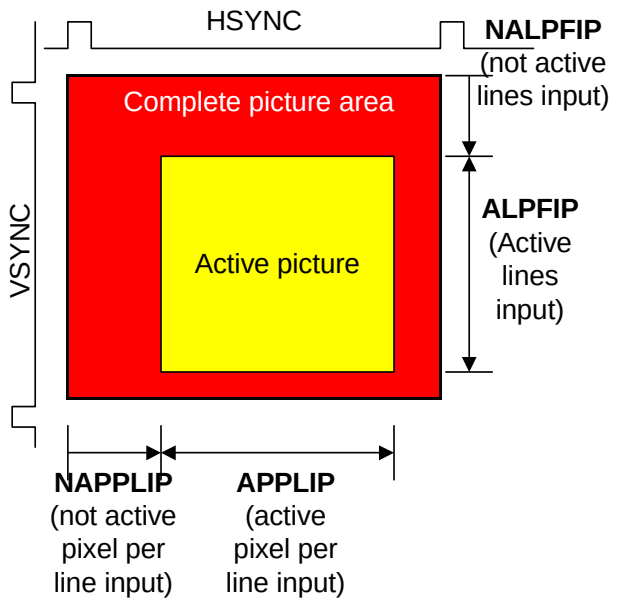


Fig. 2–24: Image format before memory

The horizontal prescaler reduces the number of input pixels by subsampling between 1 and 64. To prevent the introduction of alias distortion low pass filters are used for luminance and chrominance processing controlled by ***HAAPRESC***. In case of automatic mode the filter characteristic is adopted to the prescaler settings ***HSCPRESC*** and ***HDCPRESC***, while in case of ITU656 input, the lowpass filter must be disabled.

The horizontal prescaler is controlled by ***HSCPRESC*** (fine steps from 1 to 2) and ***HDCPRESC*** (integer decimation factors 1, 2, 3, ...). For digital 656 input, the scaler must be bypassed (***HSCPRESC***=0 and ***HDCPRESC***=0).

The start of the horizontal prescaler is defined by the ***NAPPLIP*** (Not Active Pixel Per Line Input) register, the amount of pixels is defined by the ***APPL*** (Active Pixel Per Line) register (see Fig. 2–24).

2.4.4. Horizontal Postscaler

The horizontal postscaler provides a linear or a non-linear expansion of the picture.

The linear expansion mode is required, for example, to display the center part of a 16:9 picture on a 4:3 tube. Its setting range is 1...4 in steps of 2 pixel (***HSCPOSC***) and the horizontal scaling factor is calculated by

$$HSCALE = \frac{4095}{HSPOSC}$$

2.4.5. Panorama Mode

For an improved impression of an expanded 4:3 picture displayed on a 16:9 tube, the picture can be geometrically distorted in horizontal direction. This panorama mode keeps a 4:3 ratio for the center part of the picture, while it stretches the left and right side of the picture to fill the entire 16:9 screen. It is enabled by ***HPANON***.

Also the inverse effect - called lens - can be produced to display a 16:9 picture on a 4:3 tube. Here the center part of the picture keeps its (expanded) 4:3 ratio, while the left and right side of the picture are compressed.

To realize this expansion, the picture is divided into 5 segments. Each segment is adjustable by its horizontal width and its expansion factor (see Fig. 2–25).

HSEG1...***HSEG4*** define the end position of the first four segments, while the size of the 5th segment is defined by (***PPLOP - HSEG4***). The setting accuracy of HSEGx is two pixels.

HINC0...***HINC4*** define the increment of each segment, indicating the amount of decimation/expansion. One LSB is equivalent to an offset of 0.125 to ***HSCPRESC*** per double pixel. Thus, HINCx alters ***HSCPRESC*** in the range from –32...31.875 per double pixel.

Table 2–10: Examples of Panorama Mode

Function	Normal	Extreme	Lens
HSCPRESC	1536_d	1536	1536_d
APPL	405_d	405	405_d
HSCPOSC	2378_d	1530_d	3828_d
HSEG1	108_d	108_d	108_d
HSEG2	216_d	216_d	216_d
HSEG3	324_d	324_d	324_d
HSEG4	432_d	432_d	432_d
HINC0	29_d	63_d	-31_d
HINC1	14_d	32_d	-16_d
HINC2	000_d	000_d	000_d
HINC3	-14_d	-32_d	16_d
HINC4	-29_d	-63_d	31_d

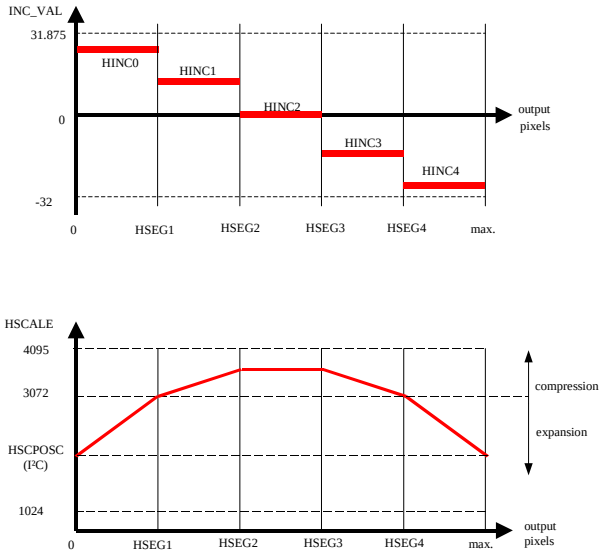
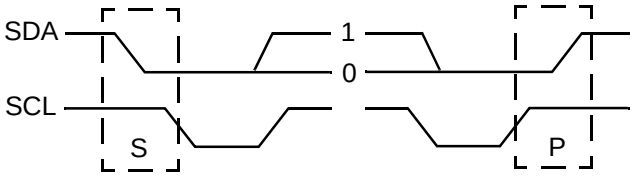


Fig. 2–25: Visualization of panorama segments

3. Control Interface

3.1. I²C Bus Interface

Communication between the VSP and the TVT (or external controller) takes place via I²C bus. The I²C bus interface of the VSP acts both as a slave receiver and as a slave transmitter. I²C clock synchronization is used to slow down the I²C bus, if required. The interface supports the normal 100 kHz transmission as well as the high-speed 400 kHz transmission.



S = I²C-Bus Start Condition
P = I²C-Bus Stop Condition

Fig. 3–1: I²C Bus protocol (MSB first, data must be stable while clock is high)

The VSP is selected by transmitting the VSP device address. A device address pair is defined as a write address and a read address.

Table 3–2: I²C Bus device address

Mode	Write	Read
VSP device address	$B0_{hex}$	$B1_{hex}$

3.2. I²C Bus Format

The VSP has 16-bit I²C registers only. The individual registers are addressed by an 8-bit subaddress following the device address.

The two bytes per register are referred to as high-byte and low-byte. The high-byte is transmitted first. The low-byte must not be transmitted if only the high-byte is of interest. All write registers are auto-increment registers, meaning that the subaddress is incremented internally after every 2 byte data transmission. However, the auto-increment function can be disabled by the control bit ***AUTOINC***. If the auto-increment function is switched off, any number of 2 byte data transmissions will be written into the same subaddress. Read-only registers with polling functions have no autoincrement function..

Table 3–3: Index of I²C abbreviations

S	Start
A	Acknowledge
NA	No Acknowledge
DAW	Device Address Write
DAR	Device Address Read
SUB	Subaddress
DH	Data High Byte
DL	Data Low Byte
P	Stop

Table 3–4: Example of write sequences

S	DAW	A	SUB	A	DH	A	P				
S	DAW	A	SUB	A	DH	A	DL	A	P		
S	DAW	A	SUB	A	DH	A	DL	A	DH	...	A	P

Table 3–5: Example of read sequences

S	DAW	A	SUB	A	S	DAR	A	DH	NA	P				
S	DAW	A	SUB	A	S	DAR	A	DH	A	DL	NA	P		
S	DAW	A	SUB	A	S	DAR	A	DH	A	DL	A	DH	...	NA	P

3.3. I²C Register Types

The following register types are defined in the detailed I²C register description (see Table 3–9 on page -33) :

Table 3–6: I²C register types

Register Types	Dir
readable write register	RW
write only register	W
read only register	R
reset after read register	R

3.4. I²C Register Domains

The I²C registers are located in different functional domains (see Table 3–7). Every domain has an independent update mechanism controlled by a set of update registers (see **I2C** on page -55).

Table 3–7: I²C register domains

Functional Block	Domain	Sub-Domain	Sync
color decoder ADC frontend comb filter	CD	CD ADC COMB	VS_CD VS_ADC VS_COMB
RGB processing	RGB	RGB	VS_RGB
ITU656 input	ITUI	ITUI	VS_ITU
scaler input	IP	IP	VS_IP
scaler output	OP	OP	VS_OP

Wether a vertical update has occured inside a domain can be checked by software by reading the status registers **VS_CD_STAT**, **VS_RGB_STAT**, **VS_ITUI_STAT**, **VS_IP_STAT** and **VS_OP_STAT**. These bits are set with the internal vertical sync and automatically reset after read.

3.5. Update of I²C Write Registers

I²C write registers change the behaviour of internal hardware. It is often required to synchronize these changes so that they cause no visible artifacts on the screen.

The register is updated either immediately or by an internal vertical sync signal. Alternatively, the register update can also be disabled. This is controlled by the I²C register bits **VS_CD**, **VS_RGB**, **VS_ITUI**, **VS_IP** and **VS_OP** for vertical update and **IM_CD**, **IM_RGB**, **IM_ITUI**, **IM_IP** and **IM_OP** for immediate update.

Registers without sync information in the I²C register description (see Table 3–9 on page -33) have immediate take-over.

3.6. .Update of I²C Read Registers

I²C read registers reflect the status of internal hardware. The take-over from hardware into the I²C register can be immediate or synchronized with an internal vertical sync signal. This is indicated by the sync information in the I²C register description (see Table 3–9 on page -33). Registers without sync information have immediate take-over.

Some I²C read registers have a special update mechanism to allow detection of fast and single events. These registers behave like a RS flip-flop and are therefore called “RS type” registers. Whenever the corresponding signal has a high level, it sets the register to “1”. After being read via I²C bus, the register will automatically be reset to “0”. These registers have an extra note in in the I²C register description (see Table 3–9 on page -33).

For example, the register **FBLACTIVE** belongs to the “RS type” read registers. It indicates activity on the fastblank input pin. Reading **FBLACTIVE** = “1” means that there was at least one short fastblank pulse since the last reading of this register.

3.7.I²C Register Block Index

3.8.I²C Register Index

3.9.I²C Register Subaddress Index

Table 3–8: I2C Subaddress Index

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h00	SYNCFTHD[1:0]		VTHRH60[6:0]							VTHRL60[6:0]							h073C
h01	CONS[2:0]					LPPOST	ACCFIX	ACCFRZ				DIS-CHCH	CLMPD1[3:0]				h400B
h02	CON[2:0]					SECNTCH[1:0]					COMBUSECD[1:0]		CLMPD2[3:0]				h462B
h03	PWTHD[1:0]				LMOFST[1:0]			YCSEL	NOSIGB		CLMPST1[5:0]						h580E
h04	VFLYWHLMD[1:0]		CHRF[5:0]						PLLTC[1:0]		CLMPST2[5:0]						h1C0E
h05	COMB	CSTAND[6:0]							CKILL[7:0]								h6640
h06	CKILLS[7:0]																h40E4
h07			THR-SEL		YCDEL[3:0]				DISALL-RES	SATNR	NSRED[2:0]						h0010
h08	HUE[7:0]																h0020
h09	NTSCREF[7:0]								PALIDL1	VTHRL50[6:0]							hA5C1
h0A	PALREF[7:0]								PALIDL0	VTHRH50[6:0]							h5F8C
h0B	SLLTHD[1:0]		SCADJ[5:0]						AGCMD[1:0]		VCHR-SEL	VCHRL[4:0]					h0F17
h0C	AGCRES	AGC-FRZE	SKILL[5:0]						VFLY-WHL	CPLL-RES	CLMPST1S[5:0]						h0019
h0D	CLMPHIGH[7:0]								SCMIDL[1:0]		CLMPST2S[5:0]						h3C19
h0E	IFCOMPSTR	SECACCL[2:0]			CLMPLOW[3:0]				ACCLIM[4:0]					IFCOMP[2:0]			h03A4
h0F	SLLTH-DVP		VDE-TIFS						CLMPD2S[3:0]				CLMPD1S[3:0]				h1F77
h10		BELLIIR[2:0]				VDETITC[2:0]				SECDIV					SCMREL[1:0]		hF701
h11	DEEMP-STD	BELLFIR[2:0]				SLLTHDV[2:0]			FLNSTRD[1:0]			ISHFT[1:0]		NOTCH OFF	VLP[1:0]		h3005
h12	PALDEL[1:0]		TNOTC HOFF				PALINC1	PALINC2	PALIDL2	CLRANGE[1:0]		NOTCHSEL[2:0]			TRAP-BLU	TRA-PRED	h4800
h13		CDYUVIN		COMBUSEVBI[1:0]				CDYUVTINT[8:0]									h0000
h14														BGSHIFT	PALDETIDL[1:0]		h0004
h15	FEMAG[4:0]					SDR[1:0]		SDB[1:0]						ITUSYNC	ART-SYNC		h8280
h16	DEEMPFIR[3:0]				DEEMPIIR[2:0]			AMSTD50[1:0]		AMSTD60[1:0]			AGCP-WRES		AGCTHD[1:0]		h5400

Table 3–8: I2C Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h17									CLMPSIG1[1:0]		CLMPSIG2[1:0]			YCBYR	UNSTABMINT	STAB-WINRED	h0810
h18				PWADJCNT[4:0]					MINV[7:0]								
h19	LPFLD[7:0]								NRPIXEL[7:0]								
h1A			STDET[2:0]			SCOUTEN	PALID	CKSTAT	LNST-DRD	INT	SCDEV[5:0]						
h1B	VFLYMD	VLENGTH[6:0]									AGCADJ[5:0]						
h1C	AM50	AM60	PALDET	STAB					BAMPL[7:0]								
h1D	PHERR_AVG[7:0]								PHERR_MAX[7:0]								
h1E											DIS-COMB		VDG[1:0]		HDG[1:0]		h000E
h1F	DDR[1:0]							COR	NOSEL[1:0]		DCR		VPK[3:0]				h40C0
h20	LINELENH50[3:0]				LINELENH60[3:0]				REMDEL2	REMDEL1	INCOMB[1:0]				VCRDE-THD	YCT-COMB	hC300
h21																TVMODE	
h23			MVCS-PARA	MVP-SONLY	MVSTOP[5:0]							MVSTART[4:0]					h0347
h24									MVAGCLENGTH[3:0]				MVPSLENGTH[3:0]				h0099
h25					MVPSDET[3:0]				MVAGCDET[3:0]				MVCSDET[3:0]				h0967
h26										MVPSPULSE	MVAGCPULSE	MVC-STRIPET	MVC-STRIPE	MVAGCPRO-CESS	MVRESULT[1:0]		
h28	TRIM_FILTER1[4:0]						AGCADJ1[5:0]						VINSEL1[3:0]				h4A00
h29	TRIM_FILTER2[4:0]						AGCADJ2[5:0]						VINSEL2[3:0]				h4A0F
h2A							AGCADJVBI[5:0]										h0200
h2B									CLAMP_SHUTOFF1	CLAMP_SYNC1	CLAMP_RGB1	CLAMP_CHROMA1					h0000
h2C									CLAMP_SHUTOFF2	CLAMP_SYNC2	CLAMP_RGB2	CLAMP_CHROMA2					h0000
h2D					VOUTSEL3[3:0]				VOUTSEL2[3:0]				VOUTSEL1[3:0]				h0FF0
h2E												STANDBY_VOUT3	STANDBY_VOUT2	STANDBY_VOUT1	STANDBY_ADC2	STANDBY_ADC1	h0000
h2F																	h0000
h30																	h0000
h31																	

Table 3–8: I2C Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h32																	
h33																	h81AC
h34																	h00E4
h36																	h00E4
h37																	h00E4
h38																	h81AC
h39																	h81AC
h3A																	
h3B																	
h3C	TRIM_FILTER3[4:0]						AGCADJ3[5:0]						VINSEL3[3:0]				h4A0F
h3D	TRIM_FILTER4[4:0]						AGCADJ4[5:0]						VINSEL4[3:0]				h4A0F
h3E	TRIM_FILTER5[4:0]						AGCADJ5[5:0]						VINSEL5[3:0]				h4A0F
h3F	TRIM_FILTER6[4:0]						AGCADJ6[5:0]						VINSEL6[3:0]				h4A0F
h40									CLAMP_SHUTOFF3	CLAMP_SYNC3	CLAMP_RGB3	CLAMP_CHROMA3	CLAMP_FBL3				h0020
h41									CLAMP_SHUTOFF4	CLAMP_SYNC4	CLAMP_RGB4	CLAMP_CHROMA4	CLAMP_FBL4				h0020
h42									CLAMP_SHUTOFF5	CLAMP_SYNC5	CLAMP_RGB5	CLAMP_CHROMA5	CLAMP_FBL5				h0020
h43									CLAMP_SHUTOFF6	CLAMP_SYNC6	CLAMP_RGB6	CLAMP_CHROMA6	CLAMP_FBL6				h0020
h44													STANDBY_ADC6	STANDBY_ADC5	STANDBY_ADC4	STANDBY_ADC3	h000F
h45							YUVMAT[1:0]			TINT[6:0]							h0000
h46	BRTADJ[7:0]								CONADJ[5:0]						CHRSF	AASEL	h0080
h47	FBLDEL[2:0]			GOFST[2:0]			MIXGAIN[6:0]								SELMASTER[1:0]		h4018
h48	YFDEL[6:0]							UVDEL[6:0]								FBLCONF	h0000
h49	USATADJ[5:0]						VSATADJ[5:0]						ADC-SEL	AABYP			h8200
h4A													MIXOP[1:0]				h0000
h4B	FBLOFFST[5:0]							YUVSEL	SMOP				RBOFST[2:0]				h8100
h4C																FBSTAT	

Table 3–8: I2C Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h4D										FBFALL	FBRISE	PFBL	PG	PB	PR	FBLAC-TIVE	
h50										CFOR-MAT	VSIG-NAL	H_POL	V_POL	F_POL	EN_656[1:0]		h0058
h51				ADINS	ADLINE[4:0]					NAPIPPHI[1:0]		F_OFFS[1:0]		VSREF	IMODE[1:0]		h0000
h52	HSPPL[7:0]									VSLPF[6:0]							h0000
h53	APPLIPI[8:0]									NALPFIPI[6:0]							hB414
h54	NAPPLIPI[7:0]								ALPFIPI[7:0]								h4890
h55							DIS_FIL TER	F656DE L	V656DE L	AFPRO C	REDMODE[1:0]		OSDMODE[1:0]		OMODE[1:0]		h00C0
h56	ADATA0[7:0]								ADATA1[7:0]								
h57	ADATA2[7:0]								ADATA3[7:0]								
h58	ADATA4[7:0]								ADATA5[7:0]								
h59	ADATA6[7:0]								ADATA7[7:0]								
h5A																AD_RD Y	
h64	NMLINE[8:0]									NMSENSE[1:0]		NMPOS[1:0]					h0000
h65										NOISEME[6:0]							
h66																NMSTA-TUS	
h6E	LBSUB[1:0]		LBGRA DRST	LBSTA-BILITY	LB43SE NS	LBNG-FEN	LBTHDNBNHA[4:0]					LBHSDEL[4:0]					h8FAA
h6F	LBGRADDET[7:0]								LBVWENDLO[7:0]								h3296
h70	LBHIWHITE[7:0]								LBHWEND[7:0]								h32B4
h71	LBHISTBLA[7:0]									LBHWST[6:0]							h1924
h72		LBVWSTLO[6:0]							LBFS	LBVWENDUP[6:0]							hE049
h73	LBGSDEL[4:0]					LBGFBDEL[4:0]					LBVWSTUP[5:0]						h52D4
h74	LBASDEL[4:0]						LBACTIVITY[4:0]					LBTHDNBNG[4:0]					h00AF
h75																	
h76																	
h77																	
h78																	
h79																	
h7A																	
h7B	LBFOR-MAT	LBSUB-TITLE	LBTOP-TITLE														
h7C	LBSLAA[6:0]							LBELAA[8:0]									

Table 3–8: I2C Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h7D																	
h7E																LBD-STATUS	
h82	YBORDER[3:0]				UBORDER[3:0]				VBORDER[3:0]								h1000
h83	FRC_BGN																h0000
h84					HSCPRESC[11:0]												h0000
h85	HAAPRESC[1:0]			HDCPRESC[3:0]													h0000
h86							APPL[9:0]										h021C
h87							NAPPLIP[9:0]										h005C
h88							ALPF[9:0]										h03FF
h89								NALPFIP[8:0]									h0000
h8A	HPANON	DIS-BORDE-THPOS	CHROMDELH-POS		HSCPOSC[11:0]												h4FFF
h8B								HINC0[8:0]									h0000
h8C								HINC1[8:0]									h0000
h8D								HINC2[8:0]									h0000
h8E								HINC3[8:0]									h0000
h8F								HINC4[8:0]									h0000
h90						HSEG1[10:0]											h0000
h91						HSEG2[10:0]											h0000
h92						HSEG3[10:0]											h0000
h93						HSEG4[10:0]											h0000
hF0			LOMID-FREQ	OSDCLKCTRL[1:0]		OSD-OFF	RGBOFF	CVB-SOFF	CLKFE40OFF	ITUIOFF	ITUOOFF	DIS-POFF	DEFLOFF	LLPLLOFF	FCLKB2LL	PLLOFF	h07FC
hF1														PUP-DAC	PUPIO	PUPDIG	
hF9	DISCPURES[15:0]																h0000
hFA																	h0000
hFB				VCTH_ID_SET[4:0]												AUTO-INC	h0000
hFC				VCTH_ID_RD[4:0]								REV[4:0]					
hFD												VS_OP_STAT	VS_IP_STAT	VS_ITUI_STAT	VS_RGB_STAT	VS_CD_STAT	
hFE												IM_OP	IM_IP	IM_ITUI	IM_RGB	IM_CD	h0000
hFF												VS_OP	VS_IP	VS_ITUI	VS_RGB	VS_CD	h001F

3.10.I²C Register Description

Note: For compatibility reasons every undefined bit in a writeable register should be set to '0'. Undefined bits in a readable register should be treated as "don't care"!

Table 3–9: I2C Register Description

Name	Sub	Dir	Sync	Reset	Range	Function
CD						
SYNCFTHD[1:0]	h00[15:14]	RW	VS_CD	0	0,1, 2, 3	**SYNCF Threshold** 00: 4 lines 01: 3 lines 10: 2 lines 11: 1 line
VTHRH60[6:0]	h00[13:7]	RW	VS_CD	14	0..127	**V-Sync Detection Stop 60 Hz** (262+VTHRH60*4) 0000000: stop in line 262 0001110: stop in line 318 (=262+4*14) 1111111: stop in line 770
VTHRL60[6:0]	h00[6:0]	RW	VS_CD	60	0..127	**V-Sync Detection Start 60 Hz** (VTHRL60*4) 0000000: start in first line 0111100: start in line 240 (=4*60) 1111111: start in line 508
CONS[2:0]	h01[15:13]	RW	VS_CD	2	0..7	**Color On (SECAM)** color on at level=CKILLS+CONS 000: min value 010: default 111: max value
LPPOST	h01[10]	RW	VS_CD	0	0,1	**Additional Luma Filtering** 0: off 1: on
ACCFIX	h01[9]	RW	VS_CD	0	0,1	**Fix ACC to nominal value** 0: ACC is working 1: ACC is set to PALREF/NTSCREF
ACCFRZ	h01[8]	RW	VS_CD	0	0,1	**Freeze ACC** 0: ACC is working 1: ACC is frozen at current value
DISCHCH	h01[4]	RW	VS_CD	0	0,1	**Disable Channel Change Reset** 0: Color Decoder not reset after detection of channel-change 1: Color Decoder reset after detection of channel-change
CLMPD1[3:0]	h01[3:0]	RW	VS_CD	11	0..15	**Clamping Measurement Duration 1** Granularity: 4/20.25MHz 0000: 0 us 0111: 1.38 us 1111: 2.96 us
CON[2:0]	h02[15:13]	RW	VS_CD	2	0..7	**Color On (PAL/NTSC)** color on at level=CKILL+CON 000: min value 010: default 111: max value
SECNTCH[1:0]	h02[10:9]	RW	VS_CD	3	0,1,2,3	**Notch Filter Frequency (SECAM)** 00: 4.406 MHz 01: 4.250 MHz 10: 4.33 MHz 11: 4.406 / 4.205 dependent on transmitted color
COMBUSECD[1:0]	h02[5:4]	RW	VS_CD	2	0,1,2,3	**Comb Filter Usage CD** 00: use first CVBS input 01: use second CVBS input 10: use comb-filter 11: ADCG / ADCF (dependent on ADCSEL)

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
CLMPD2[3:0]	h02[3:0]	RW	VS_CD	11	0..15	**Clamping Measurement Duration 2** Granularity: 4/20.25MHz 0000: 0 us 0111: 1.38 us 1111: 2.96 us
PWTHD[1:0]	h03[15:14]	RW	VS_CD	1	0,1,2,3	**AGC Peak-White Threshold** 00: 448 01: 470 10: 500 11: 511
LMOFST[1:0]	h03[11:10]	RW	VS_CD	2	0,1,2,3	**Luminance Offset** 00: no offset (NTSC) 01: - 7.5 IRE 10: + 7.5 IRE (PAL, SECAM) 11: - 3.7 IRE
YCSEL	h03[8]	RW	VS_CD	0	0,1	**Y/C Select** 0: CVBS processing 1: Y/C processing
NOSIGB	h03[7]	RW	VS_CD	0	0,1	**No Signal Blanking** 0: off 1: colored background when out of sync
CLMPST1[5:0]	h03[5:0]	RW	VS_CD	14	0..63	**Clamping Measurement Start 1** Granularity: 4/20.25MHz 000000: 0 us 011100: 5.53 us 111111: 12.44 us
VFLYWHLMD[1:0]	h04[15:14]	RW	VS_CD	0	0,1,2,3	**Vertical Flywheel Mode** 00: no deviation allowed 01: 3 lines deviation allowed 10: 4 lines deviation allowed 11: 5 lines deviation allowed
CHRF[5:0]	h04[13:8]	RW	VS_CD	28	0..63	**Chroma Bandwidth** 001110: extra wide 001100: wide 001000: broad 001001: nominal 111001: narrow
PLLTC[1:0]	h04[7:6]	RW	VS_CD	0	0,1,2,3	**Time Constant HPLL** 00: very fast 01: fast 10: slow 11: very slow
CLMPST2[5:0]	h04[5:0]	RW	VS_CD	14	0..63	**Clamping Measurement Start 2** Granularity: 4/20.25MHz 000000: 0 us 011100: 5.53 us 111111: 12.44 us
COMB	h05[15]	RW	VS_CD	0	0,1	**PAL Delay Line** 0: on (PAL/SECAM) 1: off (NTSC)
CSTAND[6:0]	h05[14:8]	RW	VS_CD	102	0..127	**Color Standard Assignment** 0000000: no color standard chosen 0000001: PAL N 0000010: PAL B 0000100: SECAM 0001000: PAL 60 0010000: PAL M 0100000: NTSC M 1000000: NTSC 44 For allowed combinations please refer to chapter 'Color Decoder' 1100110: PALB/SECAM/NTSCM/NTSC44/PAL60
CKILL[7:0]	h05[7:0]	RW	VS_CD	64	0..255	**Color Killer Threshold (PAL/NTSC)** killer on if burst amplitude < CKILL
CKILLS[7:0]	h06[15:8]	RW	VS_CD	64	0..255	**Color Killer Threshold (SECAM)** killer on if burst amplitude > CKILLS **Note:** behavior is opposite to CKILL

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
THRSEL	h07[13]	RW	VS_CD	0	0,1	**H Slicing Level Threshold** 0: 50% 1: 37%
YCDEL[3:0]	h07[11:8]	RW	VS_CD	0	-8..7	**Luminance Delay** 1000: -8 samples (shift right) 0000: no delay 0111: 7 samples (shift left)
DISALLRES	h07[7]	RW	VS_CD	0	0,1	**Disable all Chroma Resets** 0: allow resets 1: disable resets may only be used if ONE color standard is selected
SATNR	h07[6]	RW	VS_CD	0	0,1	**Noise Reduction for Satellite Signal** 0: disable 1: enable
NSRED[2:0]	h07[5:3]	RW	VS_CD	2	0..7	**Noise Reduction H-PLL** 000: 1/8 001: 1/4 010: 1/2 011: 1 100: 2 101: 4 110: 8 111: 16
HUE[7:0]	h08[15:8]	RW	VS_CD	0	-128..127	**Hue Control (Tint)** 10000000: -89 degree 00000000: 0 degree 01111111: +88 degree
NTSCREF[7:0]	h09[15:8]	RW	VS_CD	165	0..255	**ACC Reference (NTSC)** 0: low reference value 165: nominal value 255: high reference value
PALIDL1	h09[7]	RW	VS_CD	1	0,1	**PAL / NTSC Identification Level 1** 0: less sensitive (192) 1: more sensitive (64)
VTHRL50[6:0]	h09[6:0]	RW	VS_CD	65	0..127	**V-Sync Detection Start 50 Hz** (VTHRL50*4) 0000000: start in first line 1000001: start in line 260 (=4*65) 1111111: start in line 508
PALREF[7:0]	h0A[15:8]	RW	VS_CD	95	0..255	**ACC Reference (PAL)** 0: low reference value 95: nominal value 255: high reference value
PALIDL0	h0A[7]	RW	VS_CD	1	0,1	**PAL / NTSC Identification Level 0** 0: less sensitive 1: more sensitive
VTHRH50[6:0]	h0A[6:0]	RW	VS_CD	12	0..127	**V-Sync Detection Stop 50 Hz** (312+VTHRH50*4) 0000000: stop in line 312 0001100: stop in line 360 (=312+4*12) 1111111: stop in line 820
SLLTHD[1:0]	h0B[15:14]	RW	VS_CD	0	0,1,2,3	**Slicing Level Threshold H** 00: no offset 01: small negative 10: small positive 11: large positive (adaptive)
SCADJ[5:0]	h0B[13:8]	RW	VS_CD	15	0..63	**Subcarrier Adjustment** 000000: -262 ppm 001111: 0 ppm 111111: 840 ppm
AGCMD[1:0]	h0B[7:6]	RW	VS_CD	0	0,1,2,3	**AGC Method** 00: sync amplitude and peak white 01: sync amplitude only 10: peak white only 11: fixed to value AGCADJ1

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
VCHRSEL	h0B[5]	RW	VS_CD	0	0,1	**Vertical Chroma Blanking Selection** 0: SECAM only 1: always
VCHRL[4:0]	h0B[4:0]	RW	VS_CD	23	0..31	**Vertical Chroma Blanking Line** defines number of VBI lines in which chroma signal is blanked
AGCRES	h0C[15]	RW	VS_CD	0	0,1	**AGC Reset** 0: no reset 1: reset
AGCFRZE	h0C[14]	RW	VS_CD	0	0,1	**AGC Freeze** 0: normal operation 1: freeze AGC at current value
SKILL[5:0]	h0C[13:8]	RW	VS_CD	0	0..63	**Adaptive Notch Threshold** adaptive notch on if burst amplitude > SKILL
VFLYWHL	h0C[7]	RW	VS_CD	0	0,1	**Vertical Flywheel** 0: disable 1: enable
CPLLRES	h0C[6]	RW	VS_CD	0	0,1	**Force Chroma PLL Reset** 0: no reset 1: reset chroma PLL after use, CPLLRES must be set to 0 again
CLMPST1S[5:0]	h0C[5:0]	RW	VS_CD	25	0..63	**Clamping Pulse Start 1** Granularity: 4/20.25MHz 000000: 0 us 011100: 5.53 us 111111: 12.44 us
CLMPHIGH[7:0]	h0D[15:8]	RW	VS_CD	60	0..255	**Vertical End Of Clamping Pulse** 00000000: line 256 00111100: line 376 11111111: line 766
SCMIDL[1:0]	h0D[7:6]	RW	VS_CD	0	0..3	**SECAM Identification Level** 00: 128 01: 64 10: 96 11: 80
CLMPST2S[5:0]	h0D[5:0]	RW	VS_CD	25	0..63	**Clamping Pulse Start 2** Granularity: 4/20.25MHz 000000: 0 us 011100: 5.53 us 111111: 12.44 us
IFCOMPSTR	h0E[15]	RW	VS_CD	0	0,1	**IF Compensation Filter Secam** 0: dependent on IFCOMP 1: force filter 7 (except for IFCOMP=4)
SECACCL[2:0]	h0E[14:12]	RW	VS_CD	0	0..7	**SECAM Acceptance Level** 000: 100 001: 84 010: 64 011: 32 100: 70 101: 76 110: 90 Note: has only effect if SECACC is enabled
CLMPLOW[3:0]	h0E[11:8]	RW	VS_CD	3	0..15	**Vertical Start Of Clamping Pulse** 0000: line 0 0011: line 6 1111: line 30
ACCLIM[4:0]	h0E[7:3]	RW	VS_CD	20	0..31	**ACC Limitation** 00000: limit at high color-carrier 01000: limit at -24 dB 11111: limit at low color-carrier

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
IFCOMP[2:0]	h0E[2:0]	RW	VS_CD	4	0,1,2,3,4, 5,6,7	**IF Compensation Filter** 000: pal prefiltering 001: pal prefiltering + IF 010: prefiltering 011: IF 6dB 100: flat 101: 6dB/octave 110: 12db/octave 111: 10dB/MHz (secam)
SLLTHDVP	h0F[15]	RW	VS_CD	0	0,1	**Vertical Slicing Level Threshold Polarity** 0: positive 1: negative
VDETIFS	h0F[13]	RW	VS_CD	0	0,1	**Vertical Sync Detection Slope** 0: normal 1: slow
CLMPD2S[3:0]	h0F[7:4]	RW	VS_CD	7	0..15	**Clamping Pulse Duration 2** Granularity: 4/20.25MHz 0000: 0 us 0111: 1.38 us 1111: 2.96 us
CLMPD1S[3:0]	h0F[3:0]	RW	VS_CD	7	0..15	**Clamping Pulse Duration 1** Granularity: 4/20.25MHz 0000: 0 us 0111: 1.38 us 1111: 2.96 us
BELLIIR[2:0]	h10[14:12]	RW	VS_CD	7	0..7	**Bell Filter IIR Component** 000: 8 001: 9 010: 10 011: 11 100: 12 101: 13 110: 14 111: 16
VDETITC[2:0]	h10[10:8]	RW	VS_CD	7	0,1,2,3,4, 5,6,7	**Vertical Detection Integration Time Constant** 000: 400 clock cycles 001: 375 clock cycles 010: 350 clock cycles 011: 300 clock cycles 100: 250 clock cycles 101: 225 clock cycles 110: 200 clock cycles 111: automatic
SECDIV	h10[6]	RW	VS_CD	0	0,1	**SECAM Divider** 0: divide by 4 1: divide by 2
SCMREL[1:0]	h10[1:0]	RW	VS_CD	1	0..3	**SECAM RejectionLevel** 00: 320 01: 384 10: 352 11: 1024
DEEMPSTD	h11[15]	RW	VS_CD	0	0,1	**Deemphase Filtering For Standard Detection** 0: weak 1: strong
BELLFIR[2:0]	h11[14:12]	RW	VS_CD	3	0..7	**Bell Filter FIR Component** 000: -116 001: -113 010: -110 011: -108 100: -106 101: -104 110: -102 111: -100

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
SLLTHDV[2:0]	h11[10:8]	RW	VS_CD	0	0..7	**Slicing Level Threshold V** 000: no offset 001: 4 010: 8 011: 12 101: adaptive (limited to +-4) 110: adaptive (limited to +-8) 111: adaptive (limited to +-12)
FLNSTRD[1:0]	h11[7:6]	RW	VS_CD	0	0,1,2,3	**Force Line Standard** 00: automatic 01: force 50 Hz 10: force 60 Hz 11: (reserved)
ISHFT[1:0]	h11[4:3]	RW	VS_CD	0	0,1,2,3	**Integral Gain of H-PLL** 00: *1 01: *16 10: *4 11: *8
NOTCHOFF	h11[2]	RW	VS_CD	1	0,1	**Luminance Notch Filter** 0: notch-filter enabled 1: filter bypassed for PAL/NTSC / filter enabled for SECAM to switch-off filter for SECAM use TNOTCHOFF
VLP[1:0]	h11[1:0]	RW	VS_CD	1	0,1,2,3	**Lowpass for Vertical Sync Separation** 00: none 01: weak 10: medium 11: strong
PALDEL[1:0]	h12[15:14]	RW	VS_CD	1	0..3	**PAL/NTSC Delay vs. SECAM (chrominance)** 00: PAL/NTSC most left 01: 11: PAL/NTSC most right
TNOTCHOFF	h12[13]	RW	VS_CD	0	0,1	**Luminance Notch Filter** 0: notch-filter according to NOTCHOFF 1: notch-filter always disabled
PALINC1	h12[9]	RW	VS_CD	0	0,1	**Pal Detection Increment 1** 0: +3 1: +2
PALINC2	h12[8]	RW	VS_CD	0	0,1	**Pal Detection Increment 2** 0: -1 1: -2 do not use PALINC2=1 in combination with PALINC1=1
PALIDL2	h12[7]	RW	VS_CD	0	0,1	**PAL / NTSC Identification Level 2** 0: less sensitive 1: more sensitive
CLRANGE[1:0]	h12[6:5]	RW	VS_CD	0	0,1,2,3	**Chroma Lock Range** 00: +/- 425 Hz 01: +/- 463 Hz 10: +/- 505 Hz 11: +/- 550 Hz
NOTCHSEL[2:0]	h12[4:2]	RW	VS_CD	0	0,1,2,3,4	**Luminance Notch Selection** 000: sharp notch 001: medium 1 010: medium 2 011: broad notch 100: broad steep notch (PAL, SECAM only)
TRAPBLU	h12[1]	RW	VS_CD	0	0,1	**SECAM Notch Frequency Blue** 0: 4.25 MHz 1: 4.2 MHz
TRAPRED	h12[0]	RW	VS_CD	0	0,1	**SECAM Notch Frequency Red** 0: 4.406 MHz 1 :4.356 MHz
CDYUVIN	h13[14]	RW	VS_CD	0	0,1	**Eco YCrCb Input** 0: CVBS or Y/C input 1: YCrCb input

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
COMBUSEVBI[1:0]	h13[12:11]	RW	VS_CD	0	0,1,2,3	**Comb Filter Usage Slicer** 00: use first CVBS input 01: use second CVBS input 10: use comb-filter 11: ADCG / ADCF (dependent on ADCSEL)
CDYUVTINT[8:0]	h13[8:0]	RW	VS_CD	0	-256..255	**Tint Eco YCrCb Input** stepsize: 0.703× 100000000: -180× 000000000: no phase deviation 011111111: +179×
BGSHIFT	h14[2]	RW	VS_CD	1	0,1	**Clamp Window Adaption** 0: no adaption 1: adapt to linelength Note: must be enabled if internal 4h comb filter is used with non-standard input signals (e.g. VCR)
PALDETIDL[1:0]	h14[1:0]	RW	VS_CD	0	0..3	**PALDET Identification Level** 00: 240 01: 192 10: 128 11: 64
FEMAG[4:0]	h15[15:11]	RW	VS_CD	16	0..31	**Fine Error Magnitude** 00000: 0.5 10000: 1 11111: 1.5
SDR[1:0]	h15[10:9]	RW	VS_CD	1	0..3	**SECAM Dr Adjustment** 00: 191 01: 194 10: 197 11: 200
SDB[1:0]	h15[8:7]	RW	VS_CD	1	0..3	**SECAM Db Adjustment** 00: -55 01: -58 10: -61 11: -64
ITUSYNC	h15[2]	RW	VS_CD	0	0,1	**Digital Sync Pulse from ITU Input Interface** 0: use cvbs sync 1: use itu sync
ARTSYNC	h15[1]	RW	VS_CD	0	0,1	**Artificially Generated Sync** 0: sync from luminance processing 1: sync from synthesizer
DEEMPFIR[3:0]	h16[15:12]	RW	VS_CD	5	0..15	**Deemphase Filter FIR Component** 0000: -16 0101: -21 0111: -23 1111: -31
DEEMPIIR[2:0]	h16[11:9]	RW	VS_CD	2	0..7	**Deemphase Filter IIR Component** 000 :5 001: 6 010: 7 011: 8 100: 9 101: 10 110: (reserved) 111: (reserved)
AMSTD50[1:0]	h16[8:7]	RW	VS_CD	0	0,1,2,3	**Automatic Standard Detection Priority 50** 00: PAL B/G 01: SECAM 10: (reserved) 11: automatic
AMSTD60[1:0]	h16[6:5]	RW	VS_CD	0	0,1,2,3	**Automatic Standard Detection Priority 60** 00: NTSC M 01: PAL60 / NTSC44 10: (reserved) 11: automatic
AGCPWRES	h16[3]	RW	VS_CD	0	0,1	**AGC Peak-White Counter Reset** 0: no reset 1: reset

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
AGCTHD[1:0]	h16[1:0]	RW	VS_CD	0	0,1,2,3	**AGC Hysteresis Threshold** 00: broad 01: 10: 11: narrow
CLMPSIG1[1:0]	h17[7:6]	RW	VS_CD	0	0,1,2	**Clamping Signals ADC1** 00: colordecoder signals 1 01: colordecoder signals 2 10: slicer 11: reserved
CLMPSIG2[1:0]	h17[5:4]	RW	VS_CD	1	0,1,2	**Clamping Signals ADC2** 00: colordecoder signals 1 01: colordecoder signals 2 10: slicer 11: reserved
YCBYR	h17[2]	RW	VS_CD	0	0,1	**YC by Red** 0: normal operation 1: chroma input from ADCR
UNSTABMINT	h17[1]	RW	VS_CD	0	0,1	**Unstable Minimum Threshold** defines minimum threshold for Hsync separation when unstable 0: 16 LSB 1: 32 LSB
STABWINRED	h17[0]	RW	VS_CD	0	0,1	**STAB Window Reduction** 0: 64 clock cycles (normal window) 1: 32 clock cycles (short window)
PWADJCNT[4:0]	h18[12:8]	R	VS_CD		0..31	**Peak-White Reduction Counter** 00000: no reduction 11111: max. reduction
MINV[7:0]	h18[7:0]	R	VS_CD		0..255	**Measured Sync Amplitude**
LPFLD[7:0]	h19[15:8]	R	VS_CD		0..255	**Measured Lines Per Field** lines=2*LPFLD+256 00000000: 256 lines or less ... 00000011: 262 lines ... 00011100: 312 lines ... 11111111: 766 lines or more
NRPIXEL[7:0]	h19[7:0]	R	VS_CD		0..255	**Measured Pixel per Line** pixel=4*NRPIXEL+384 00000000: 384 pixel or less 11111111: 1404 pixel or more
STDET[2:0]	h1A[13:11]	R	VS_CD		0,1,2,3,4,5,6,7	**Detected Color Standard** 000: non standard or standard not detected 001: NTSC M 010: PAL M 011: NTSC44 100: PAL60 101: PAL N 110: SECAM 111: PAL B/G
SCOUTEN	h1A[10]	R	VS_CD		0,1	**SCDEV Valid** 0: not valid 1: valid
PALID	h1A[9]	R	VS_CD		0,1	**PAL Identification** 0: not PAL 1: PAL
CKSTAT	h1A[8]	R	VS_CD		0,1	**Color Killer Status** 0: color off 1: color on
LNSTDRD	h1A[7]	R	VS_CD		0,1	**Line Standard Detection** 0: 60 Hz 1: 50 Hz
INT	h1A[6]	R	VS_CD		0,1	**Interlace Detection** 0: non-interlaced input 1: interlaced input

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
SCDEV[5:0]	h1A[5:0]	R	VS_CD		-32..31	**Deviation Of Clock System or Color Carrier** 100000: maximum neg. deviation 000000: no deviation 011111: maximum pos. deviation
VFLYMD	h1B[15]	R	VS_CD		0,1	**Vertical Flywheel Status** 0: unlocked 1: locked
VLENGTH[6:0]	h1B[14:8]	R	VS_CD		0..127	**Length of Vertical Pulse** 0000000: short 1111111: long
AGCADJ[5:0]	h1B[5:0]	R	VS_CD		0..63	**AGC Value**
AM50	h1C[15]	R	VS_CD		0,1	**Last Detected Standard 50 Hz** 0: PAL or none 1: SECAM
AM60	h1C[14]	R	VS_CD		0,1	**Last Detected Standard 60 Hz** 0: NTSC M or none 1: NTSC44 or PAL60
PALDET	h1C[13]	R	VS_CD		0,1	**PAL Identification (algorithm 2)** 0: not PAL 1: PAL
STAB	h1C[12]	R	VS_CD		0,1	**Status of H-PLL** 0: unlocked 1: locked
BAMPL[7:0]	h1C[7:0]	R	VS_CD		0..255	**Burst Amplitude** (only valid for PAL/NTSC when color='on') 00000000: biggest burst 11111111: smallest burst
PHERR_AVG[7:0]	h1D[15:8]	R	VS_CD		0..255	**Measured Phase Error Average**
PHERR_MAX[7:0]	h1D[7:0]	R	VS_CD		0..255	**Measured Phase Error Maximum**
COMB						
DISCOMB	h1E[5]	RW	VS_COMB	0	0,1	**Disable Comb Filter** 0: enable 1: disable
VDG[1:0]	h1E[3:2]	RW	VS_COMB	3	0..3	**Vertical difference Gain** 00: max. gain 01: medium 2 10: medium 1 11: min. gain
HDG[1:0]	h1E[1:0]	RW	VS_COMB	2	0..3	**Horizontal difference Gain** 00: min. gain 01: medium 1 10: medium 2 11: max. gain
DDR[1:0]	h1F[15:14]	RW	VS_COMB	1	0..3	**Diagonal Dot Reduction** 00: min. reduction 01: medium 1 10: medium 2 11: max. reduction
COR	h1F[8]	RW	VS_COMB	0	0,1	**Vertical Peaking coring** 0: disable 1: enable
NOSEL[1:0]	h1F[7:6]	RW	VS_COMB	3	0,1,2,3	**Notch filter select** 00: flat frequency characteristic 01: min. peaked 10: med. peaked 11: max. peaked
DCR	h1F[5]	RW	VS_COMB	0	0,1	**Vertical Peaking DC rejection filter** 0: disable 1: enable
VPK[3:0]	h1F[3:0]	RW	VS_COMB	0	0..15	**Vertical Peaking Gain** 0000: no vertical peaking 1111: max. vertical peaking
LINELENH50[3:0]	h20[15:12]	RW	VS_COMB	12	0..15	**Pixel per Line 50 Hz** pixel=1284+LINLENH50 12: 1296 pixel per line

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
LINELENH60[3:0]	h20[11:8]	RW	VS_COMB	3	0..15	**Pixel per Line 60 Hz** pixel=1284+LINLENH60 3: 1287 pixel per line
REMDEL2	h20[7]	RW	VS_COMB	0	0,1	**Combfilter Compensation Delay (ADC2)** 0: enable 1: disable
REMDEL1	h20[6]	RW	VS_COMB	0	0,1	**Combfilter Compensation Delay (ADC1)** 0: enable 1: disable
INCOMB[1:0]	h20[5:4]	RW	VS_COMB	0	0,1,2,3	**Combfilter Luma Input Select** 00: ADC 1 01: ADC 2 10: ADCG / ADCF (depends on ADCSEL)
VCRDETHD	h20[1]	RW	VS_COMB	0	0,1	**VCR Detection Threshold** 0: low threshold 1: high threshold
YCTCOMB	h20[0]	RW	VS_COMB	0	0,1	**YC through Comb filter** 0: normal comb operation 1: yc signal fed through comb delays
TVMODE	h21[0]	R	VS_COMB		0,1	**TV mode detection** 0: VCR input 1: TV input
MACROVISION						
MVCSPARA	h23[13]	RW	VS_CD	0	0,1	**Burst Inversion** 0: minimum 1/4 burst inversion required 1: minimum 1/8 burst inversion required
MVPSONLY	h23[12]	RW	VS_CD	0	0,1	**AGC Process Detection** 0: use PS and AGC pulses for AGC process detection 1: use only PS pulses for AGC process detection
MVSTOP[5:0]	h23[11:6]	RW	VS_CD	13	0..63	**End Line of Macrovision Detection** 000000: line 4/267 (525) or line 1/314 (625) 001101: line 17/280 (525) or line 14/327 (625) 111111: line 67/330 (525) or line 64/357 (625)
MVSTART[4:0]	h23[4:0]	RW	VS_CD	7	0..31	**Start Line of Macrovision Detection** 00000: line 4/267 (525) or line 1/314 (625) 00111: line 11/274 (525) or line 8/321 (625) 11111: line 35/298 (525) or line 32/345 (625)
MVAGCLENGTH[3:0]	h24[7:4]	RW	VS_CD	9	0..15	**Minimum Detection Threshold for AGC pulses** 0000: 0 us 1001: 1.8 us 1111: 3 us Note: for progressive signals, set to 5 (1 us)
MVPSLENGTH[3:0]	h24[3:0]	RW	VS_CD	9	0..15	**Minimum Detection Threshold for PS pulses** 0000: 0 us 1001: 0.9 us 1111: 1.5 us Note: for progressive signals, set to 5 (0.5 us)
MVPSDET[3:0]	h25[11:8]	RW	VS_CD	9	0..15	**PS Detection Threshold** 0011: 0 lines 1001: 6 lines 1111: 12 lines
MVAGCDET[3:0]	h25[7:4]	RW	VS_CD	6	0..15	**AGC Detection Threshold** 0000: 0 lines 0110: 6 lines 1111: 15 lines
MVCSDET[3:0]	h25[3:0]	RW	VS_CD	7	0..15	**Colorstripe Detection Threshold** 0000: 0 lines 0111: 7 lines 1111: 15 lines
MVPSPULSE	h26[6]	R	VS_CD		0, 1	**Raw Pseudo-Sync Pulse Detection** 0: pseudo-sync pulse not present 1: pseudo-sync pulse present

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
MVAGCPULSE	h26[5]	R	VS_CD		0, 1	**Raw AGC Pulse Detection** 0: AGC pulse not present 1: AGC pulse present Note: Due to cyclic change of AGC pulse amplitude, this value changes ist value periodically when AGC process is present
MVCSTRIPET	h26[4]	R	VS_CD		0, 1	**Colorstripe Process Type** 0: colorstripe type 2 1: colorstripe type 3 Note: only valid if MVCSTRIPE=1
MVCSTRIPE	h26[3]	R	VS_CD		0,1	**Colorstripe Process Detection** 0: colorstripe process not present 1: colorstripe process present
MVAGCPROCESS	h26[2]	R	VS_CD		0,1	**AGC Process Detection** 0: AGC process not present 1: AGC process present
MVRESULT[1:0]	h26[1:0]	R	VS_CD		0,1, 2, 3	**Macrovision Detection** 00: nothing present 01: AGC process present and colorstripe process not present 10: AGC process present and colorstripe process type 2 present 11: AGC process present and colorstripe process type 3 present
ADC						
TRIM_FILTER1[4:0]	h28[15:11]	RW	VS_ADC	9	0..31	**Bandwidth Antialias Filter ADC1** 00000: narrow 01001: normal 11111: wide
AGCADJ1[5:0]	h28[9:4]	RW	VS_ADC	32	0..63	**Manual AGC Adjust ADC1** 000000: 0.5 V input voltage 100000: 1.0 V input voltage 111111: 1.5 V input voltage
VINSEL1[3:0]	h28[3:0]	RW	VS_ADC	0	0..15	**Video Input Select ADC1** 0000: VIN0 (DRX) 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: VIN3 + VIN4 (Y1+C1) 1101: VIN5 + VIN6 (Y2+C2) 1110: VIN7 + VIN8 (Y3+C3) 1111: off
TRIM_FILTER2[4:0]	h29[15:11]	RW	VS_ADC	9	0..31	**Bandwidth Antialias Filter ADC2** 00000: narrow 01001: normal 11111: wide
AGCADJ2[5:0]	h29[9:4]	RW	VS_ADC	32	0..63	**Manual AGC Adjust ADC2** 000000: 0.5 V input voltage 100000: 1.0 V input voltage 111111: 1.5 V input voltage

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
VINSEL2[3:0]	h29[3:0]	RW	VS_ADC	15	0..15	**Video Input Select ADC2** 0000: VIN0 (DRX) 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: VIN3 + VIN4 (Y1+C1) 1101: VIN5 + VIN6 (Y2+C2) 1110: VIN7 + VIN8 (Y3+C3) 1111: off
AGCADJVBI[5:0]	h2A[9:4]	RW	VS_ADC	32	0..63	**Manual AGC Adjust for VBI Teletext Slicer** 000000: 0.5 V input voltage 100000: 1.0 V input voltage 111111: 1.5 V input voltage
CLAMP_SHUTOFF1	h2B[7]	RW	VS_ADC	0	0,1	**Disable Clamping ADC1** 0: normal operation 1: disable clamping current if another ADC uses same input
CLAMP_SYNC1	h2B[6]	RW	VS_ADC	0	0,1	**Clamping Mode ADC1** 0: back porch 1: sync tip
CLAMP_RGB1	h2B[5]	RW	VS_ADC	0	0,1	**RGB Clamping ADC1** 0: CVBS 1: RGB/YCrCb
CLAMP_CHROMA1	h2B[4]	RW	VS_ADC	0	0,1	**Chroma Clamping ADC1** 0: CVBS/Y/RGB 1: Chroma/CrCb
CLAMP_SHUTOFF2	h2C[7]	RW	VS_ADC	0	0,1	**Disable Clamping ADC2** 0: normal operation 1: disable clamping current if another ADC uses same input
CLAMP_SYNC2	h2C[6]	RW	VS_ADC	0	0,1	**Clamping Mode ADC2** 0: back porch 1: sync tip
CLAMP_RGB2	h2C[5]	RW	VS_ADC	0	0,1	**RGB Clamping ADC2** 0: CVBS 1: RGB/YCrCb
CLAMP_CHROMA2	h2C[4]	RW	VS_ADC	0	0,1	**Chroma Clamping ADC2** 0: CVBS/Y/RGB 1: Chroma/CrCb
VOUTSEL3[3:0]	h2D[11:8]	RW	VS_ADC	15	0..15	**Video Output Select 3** 0000: VIN0 (DRX) 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: VIN3 + VIN4 (Y1+C1) 1101: VIN5 + VIN6 (Y2+C2) 1110: VIN7 + VIN8 (Y3+C3) 1111: off

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
VOUTSEL2[3:0]	h2D[7:4]	RW	VS_ADC	15	0..15	**Video Output Select 2** 0000: VIN0 (DRX) 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: VIN3 + VIN4 (Y1+C1) 1101: VIN5 + VIN6 (Y2+C2) 1110: VIN7 + VIN8 (Y3+C3) 1111: off
VOUTSEL1[3:0]	h2D[3:0]	RW	VS_ADC	0	0..15	**Video Output Select 1** 0000: VIN0 (DRX) 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: VIN3 + VIN4 (Y1+C1) 1101: VIN5 + VIN6 (Y2+C2) 1110: VIN7 + VIN8 (Y3+C3) 1111: off
STANDBY_VOUT3	h2E[4]	RW	VS_ADC	0	0,1	**Standby VOUT3** 0: normal operation 1: standby
STANDBY_VOUT2	h2E[3]	RW	VS_ADC	0	0,1	**Standby VOUT2** 0: normal operation 1: standby
STANDBY_VOUT1	h2E[2]	RW	VS_ADC	0	0,1	**Standby VOUT1** 0: normal operation 1: standby
STANDBY_ADC2	h2E[1]	RW	VS_ADC	0	0,1	**Standby ADC2** 0: normal operation 1: standby
STANDBY_ADC1	h2E[0]	RW	VS_ADC	0	0,1	**Standby ADC1** 0: normal operation 1: standby
ADC_RGB						
TRIM_FILTER3[4:0]	h3C[15:11]	RW	VS_ADC	9	0..31	**Bandwidth Antialias Filter ADC3** 00000: narrow 01001: normal 11111: wide
AGCADJ3[5:0]	h3C[9:4]	RW	VS_ADC	32	0..63	**Manual AGC Adjust ADC3** 000000: 0.5 V input voltage 100000: 1.0 V input voltage 111111: 1.5 V input voltage

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
VINSEL3[3:0]	h3C[3:0]	RW	VS_ADC	15	0..15	**Video Input Select ADC3** 0000: off 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: off 1101: off 1110: off 1111: off
TRIM_FILTER4[4:0]	h3D[15:11]	RW	VS_ADC	9	0..31	**Bandwidth Antialias Filter ADC4** 00000: narrow 01001: normal 11111: wide
AGCADJ4[5:0]	h3D[9:4]	RW	VS_ADC	32	0..63	**Manual AGC Adjust ADC4** 000000: 0.5 V input voltage 100000: 1.0 V input voltage 111111: 1.5 V input voltage
VINSEL4[3:0]	h3D[3:0]	RW	VS_ADC	15	0..15	**Video Input Select ADC4** 0000: off 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: off 1101: off 1110: off 1111: off
TRIM_FILTER5[4:0]	h3E[15:11]	RW	VS_ADC	9	0..31	**Bandwidth Antialias Filter ADC5** 00000: narrow 01001: normal 11111: wide
AGCADJ5[5:0]	h3E[9:4]	RW	VS_ADC	32	0..63	**Manual AGC Adjust ADC5** 000000: 0.5 V input voltage 100000: 1.0 V input voltage 111111: 1.5 V input voltage
VINSEL5[3:0]	h3E[3:0]	RW	VS_ADC	15	0..15	**Video Input Select ADC5** 0000: off 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: off 1101: off 1110: off 1111: off
TRIM_FILTER6[4:0]	h3F[15:11]	RW	VS_ADC	9	0..31	**Bandwidth Antialias Filter ADC6** 00000: narrow 01001: normal 11111: wide

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
AGCADJ6[5:0]	h3F[9:4]	RW	VS_ADC	32	0..63	**Manual AGC Adjust ADC6** 000000: 0.5 V input voltage 100000: 1.0 V input voltage 111111: 1.5 V input voltage
VINSEL6[3:0]	h3F[3:0]	RW	VS_ADC	15	0..15	**Video Input Select ADC6** 0000: off 0001: VIN1 0010: VIN2 0011: VIN3 0100: VIN4 0101: VIN5 0110: VIN6 0111: VIN7 1000: VIN8 1001: VIN9 1010: VIN10 1011: VIN11 1100: off 1101: off 1110: off 1111: off
CLAMP_SHUTOFF3	h40[7]	RW	VS_ADC	0	0,1	**Disable Clamping ADC3** 0: normal operation 1: disable clamping current if another ADC uses same input
CLAMP_SYNC3	h40[6]	RW	VS_ADC	0	0,1	**Clamping Mode ADC3** 0: back porch 1: sync tip
CLAMP_RGB3	h40[5]	RW	VS_ADC	1	0,1	**RGB Clamping ADC3** 0: CVBS 1: RGB/YCrCb
CLAMP_CHROMA3	h40[4]	RW	VS_ADC	0	0,1	**Chroma Clamping ADC3** 0: CVBS/Y/RGB 1: Chroma/CrCb
CLAMP_FBL3	h40[3]	RW	VS_ADC	0	0,1	**Fastblank Clamping ADC3** 0: normal clamping 1: fastblank clamping (dc coupled)
CLAMP_SHUTOFF4	h41[7]	RW	VS_ADC	0	0,1	**Disable Clamping ADC4** 0: normal operation 1: disable clamping current if another ADC uses same input
CLAMP_SYNC4	h41[6]	RW	VS_ADC	0	0,1	**Clamping Mode ADC4** 0: back porch 1: sync tip
CLAMP_RGB4	h41[5]	RW	VS_ADC	1	0,1	**RGB Clamping ADC4** 0: CVBS 1: RGB/YCrCb
CLAMP_CHROMA4	h41[4]	RW	VS_ADC	0	0,1	**Chroma Clamping ADC4** 0: CVBS/Y/RGB 1: Chroma/CrCb
CLAMP_FBL4	h41[3]	RW	VS_ADC	0	0,1	**Fastblank Clamping ADC4** 0: normal clamping 1: fastblank clamping (dc coupled)
CLAMP_SHUTOFF5	h42[7]	RW	VS_ADC	0	0,1	**Disable Clamping ADC5** 0: normal operation 1: disable clamping current if another ADC uses same input
CLAMP_SYNC5	h42[6]	RW	VS_ADC	0	0,1	**Clamping Mode ADC5** 0: back porch 1: sync tip
CLAMP_RGB5	h42[5]	RW	VS_ADC	1	0,1	**RGB Clamping ADC5** 0: CVBS 1: RGB/YCrCb
CLAMP_CHROMA5	h42[4]	RW	VS_ADC	0	0,1	**Chroma Clamping ADC5** 0: CVBS/Y/RGB 1: Chroma/CrCb
CLAMP_FBL5	h42[3]	RW	VS_ADC	0	0,1	**Fastblank Clamping ADC5** 0: normal clamping 1: fastblank clamping (dc coupled)

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
CLAMP_SHUTOFF6	h43[7]	RW	VS_ADC	0	0,1	**Disable Clamping ADC6** 0: normal operation 1: disable clamping current if another ADC uses same input
CLAMP_SYNC6	h43[6]	RW	VS_ADC	0	0,1	**Clamping Mode ADC6** 0: back porch 1: sync tip
CLAMP_RGB6	h43[5]	RW	VS_ADC	1	0,1	**RGB Clamping ADC6** 0: CVBS 1: RGB/YCrCb
CLAMP_CHROMA6	h43[4]	RW	VS_ADC	0	0,1	**Chroma Clamping ADC6** 0: CVBS/Y/RGB 1: Chroma/CrCb
CLAMP_FBL6	h43[3]	RW	VS_ADC	0	0,1	**Fastblank Clamping ADC6** 0: normal clamping 1: fastblank clamping (dc coupled)
STANDBY_ADC6	h44[3]	RW	VS_ADC	1	0,1	**Standby ADC6** 0: normal operation 1: standby
STANDBY_ADC5	h44[2]	RW	VS_ADC	1	0,1	**Standby ADC5** 0: normal operation 1: standby
STANDBY_ADC4	h44[1]	RW	VS_ADC	1	0,1	**Standby ADC4** 0: normal operation 1: standby
STANDBY_ADC3	h44[0]	RW	VS_ADC	1	0,1	**Standby ADC3** 0: normal operation 1: standby
RGB						
YUVMAT[1:0]	h45[9:8]	RW	VS_RGB	0	0,1,2	**YCrCb Matrix** 0: YCrCb bypass 1: YPrPb to YCrCb (CCIR) 2: YPrPb to YCrCb (BTA) 3: reserved
TINT[6:0]	h45[6:0]	RW	VS_RGB	0	-63..63	**Tint** -63: -45 degree 0: 0 degree 63: 45 degree
BRTADJ[7:0]	h46[15:8]	RW	VS_RGB	0	-128..127	**Brightness** 10000000: -128 00000000: 0 01111111: 127
CONADJ[5:0]	h46[7:2]	RW	VS_RGB	32	0..63	**Contrast** 000000: 0 100000: 32/32 111111: 63/32
CHRSF	h46[1]	RW	VS_RGB	0	0,1	**Chroma Subsampling Filter** 0: disable 1: enable
AASEL	h46[0]	RW	VS_RGB	0	0,1	**Antialias Filter Bandwidth** 0: -3dB @ 5.2MHz 1: -3dB @ 5.7MHz
FBLDEL[2:0]	h47[15:13]	RW	VS_RGB	2	0..7	**Fastblank Delay** fastblank vs. RGB/YCrCb 000: -100 ns delay 001: -50 ns delay 010: no delay 011: +50 ns delay 100: +100 ns delay 101: +150 ns delay 11x: +200 ns delay
GOFST[2:0]	h47[12:10]	RW	VS_RGB	0	0,1,2,3	**Offset Adjustment for Green channel** 00: 0 (e.g. G or Y, pedestal offset visible) 01: -32 (e.g. G or Y, no pedestal offset visible) 10: -128 (e.g. G or Y with sync, pedestal offset visible) 11: -160 (e.g. G or Y with sync, no pedestal offset visible)

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
MIXGAIN[6:0]	h47[9:3]	RW	VS_RGB	3	-64..63	**Mixer Gain of fast blank signal** 1000000: -64 0000000: 0 0111111: +63 Note: in dynamic softmix mode, absolute value of MIXGAIN must be > 2
SELMASTER[1:0]	h47[1:0]	RW	VS_RGB	0	0, 1, 2, 3	**Channel Mux** 00: Color Decoder 01: reserved 10: Soft Mixer 11: ITUR-656 input
YFDEL[6:0]	h48[15:9]	RW	VS_RGB	0	0..127	**Y/FBL Delay** 0000000: no delay 1111111: 127/20.25MHz = 6.27 us
UVDEL[6:0]	h48[8:2]	RW	VS_RGB	0	0..127	**CrCb Delay** 0000000: no delay 1111111: 127/20.25MHz = 6.27 us
FBLCONF	h48[0]	RW	VS_RGB	0	0,1	**FBLACTIVE Detection Threshold** 0: FBL >= 1 clock 1: FBL >= 5 clock
USATADJ[5:0]	h49[15:10]	RW	VS_RGB	32	0..63	**Cb Saturation** 000000: 0 100000: 32/32 111111: 63/32
VSATADJ[5:0]	h49[9:4]	RW	VS_RGB	32	0..63	**Cr Saturation** 000000: 0 100000: 32/32 111111: 63/31
ADCSEL	h49[3]	RW	VS_RGB	0	0,1	**Select ADC for sync source** 0: ADC4 1: ADC6
AABYP	h49[2]	RW	VS_RGB	0	0,1	**Bypass Digital Antialiasfilter** 0: normal 1: bypass
MIXOP[1:0]	h4A[3:2]	RW	VS_RGB	0	0, 1, 2, 3	**Mixing Operation** 00: soft mixing RGB & CVBS 01: only RGB 10: only CVBS 11: (reserved)
FBLOFFST[5:0]	h4B[15:10]	RW	VS_RGB	32	0..63	**Offset Adjustment for Fastblank channel**
YUVSEL	h4B[8]	RW	VS_RGB	1	0,1	**RGB Matrix** 0: YCrCb/YPrPb 1: RGB
SMOP	h4B[7]	RW	VS_RGB	0	0, 1	**Softmix Mode** 0: dynamic 1: static
RBOFST[2:0]	h4B[3:1]	RW	VS_RGB	0	0,1,2,3,4, 5,6	**Offset Adjustment for R and B channel** 000: 0 (e.g. RB, pedestal offset visible) 001: -32 (e.g. RB, no pedestal offset visible) 010: -128 (e.g. RB with sync, pedestal offset visible) 011: -160 (e.g. RB with sync, no pedestal offset visible) 100: -255 (CrCb negative pedestal offset) 101: -256 (CrCb) 110: -257 (CrCb positive pedestal offset) 111: (reserved)
FBSTAT	h4C[0]	R	VS_RGB		0,1	**Fastblank Status** 0: fastblank input low 1: fastblank input high
FBFALL	h4D[6]	R	FBLAC-TIVE		0,1	**Fastblank Falling Edge Detection** 0: no activity 1: activity Note: reset after read
FBRISE	h4D[5]	R	FBLAC-TIVE		0,1	**Fastblank Rising Edge Detection** 0: no activity 1: activity Note: reset after read

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
PFBL	h4D[4]	R	FBLAC-TIVE		0,1	**Overflow on Fastblank input** 0: no overflow 1: overflow Note: reset after read
PG	h4D[3]	R	FBLAC-TIVE		0,1	**Overflow on Green input** 0: no overflow 1: overflow Note: reset after read
PB	h4D[2]	R	FBLAC-TIVE		0,1	**Overflow on Blue input** 0: no overflow 1: overflow Note: reset after read
PR	h4D[1]	R	FBLAC-TIVE		0,1	**Overflow on RED input** 0: no overflow 1: overflow Note: reset after read
FBLACTIVE	h4D[0]	R	FBLAC-TIVE		0,1	**Fastblank Activity** 0: no activity 1: activity Note: reset after read
ITU						
CFORMAT	h50[6]	RW	VS_ITU	1	0,1	**Chroma Data Format (ITU656 Input/Output)** 0: unsigned 1: 2s complement
VSIGNAL	h50[5]	RW	VS_ITU	0	0,1	**Vertical Sync Mode (ITU656 Input)** 0: interlaced 1: non interlaced
H_POL	h50[4]	RW	VS_ITU	1	0,1	**HSync Polarity (ITU656 Input/Output)** 0: 656HIO active low 1: 656HIO active high
V_POL	h50[3]	RW	VS_ITU	1	0,1	**VSync Polarity (ITU656 Input/Output)** 0: 656VIO active low 1: 656VIO active high
F_POL	h50[2]	RW	VS_ITU	0	0,1	**Field Flag Polarity (ITU656 Input)** 0: Field A=0, Field B=1 1: Field A=1, Field B=0
EN_656[1:0]	h50[1:0]	RW	VS_ITU	0	0,1,2,3	**Enable ITU656 Interface** 00: input & output disabled 01: input enabled 10: output enabled 11: input & output enabled
ADINS	h51[12]	RW	VS_ITU	0	0,1	**Ancillary Data Insertion (ITU656 Input)** 0: Transmitter preamble is detected in the data stream. If identical as ADLINE data are stored in I2C-Registers. 1: Ancillary data detection in video line ADLINE only, transmitter address ignored. If preamble detected, data are stored in I2C-Registers.
ADLINE[4:0]	h51[11:7]	RW	VS_ITU	0	0..31	**Ancillary Data Line Number (ITU656 Input)** if ADINS=0: transmitter address is: 111(+5 bits of ADLINE), if ADINS=1: ADLINE defines the line, which should contain the ancillary data.
NAPIPPHI[1:0]	h51[6:5]	RW	VS_ITU	0	0..3	**CbYCrY Phase Shift (ITU656 Input)** YC multiplex adjust in units of clocks 00: no phase shift 01: 1 clock 10: 2 clocks 11: 3 clocks
F_OFFS[1:0]	h51[4:3]	RW	VS_ITU	0	0..3	**Active Field Offset (ITU656 Input)** 00: NALPFIPI in field A and B 01: NALPFIPI+1 in field A, NALPFIPI in field B 10: NALPFIPI in field A and B 11: NALPFIPI in field A, NALPFIPI+1 in field B
VSREF	h51[2]	RW	VS_ITU	0	0,1	**VSync Reference (ITU656 Input)** generate vsync related to F- or V-flag 0: use F-flag 1: use V-flag

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
IMODE[1:0]	h51[1:0]	RW	VS_ITU	0	0,1,2,3	**ITU656 Input Format** 00: automatic mode (sync signals embedded in data stream) 01: manual mode (active video programmable, sync signals in data stream) 10: ext-sync mode, (ext. H/V-sync according PAL/NTSC) 11: ext-blank mode, (ext. H/V-blanking according ITU656)
HSPPL[7:0]	h52[15:8]	RW	VS_ITU	0	0..255	**HSync Shift (ITU656 Input)** number of pixel relative to line start hsync shift = HSPPL * 4
VSLPF[6:0]	h52[6:0]	RW	VS_ITU	0	0..127	**VSync Shift (ITU656 Input)** number of lines relative to field start vsync shift = VSLPF * 4
APPLIPI[8:0]	h53[15:7]	RW	VS_ITU	360	0..511	**Active Pixel per Line (ITU656 Input)** active pixels = APPLIPI * 2
NALPFIPI[6:0]	h53[6:0]	RW	VS_ITU	20	0..127	**Not Active Lines per Field (ITU656 Input)**
NAPPLIPI[7:0]	h54[15:8]	RW	VS_ITU	72	0..255	**Not Active Pixel per Line (ITU656 Input)** delay from HSYNC to input data = NAPPLIPI * 2 + NAPIP-PHI
ALPFIPI[7:0]	h54[7:0]	RW	VS_ITU	144	0..255	**Active Lines per Field (ITU656 Input)** active lines = ALPFIPI * 2
DIS_FILTER	h55[9]	RW	VS_ITU	0	0,1	**Disable 4:2:2 Decimation Filter (ITU656 Output)** 0: filter enabled 1: filter disabled
F656DEL	h55[8]	RW	VS_ITU	0	0,1	**F-Flag Delay (ITU656 Output)** defines delay between F-flag and rising edge of V-flag in ITU656 data stream 0: 3 lines delay in field A, 2 lines in field B 1: 2 lines delay in field A and B
V656DEL	h55[7]	RW	VS_ITU	1	0,1	**V-Flag Delay (ITU656 Output)** defines delay of rising edge of V-flag in field A in reference to internal VSYNC (only used when AFPROC=1) 0: no delay 1: 1 line delay
AFPROC	h55[6]	RW	VS_ITU	1	0,1	**Active Field Processing (ITU656 Output)** defines reference point of rising edge of V-flag in ITU656 data stream 0: falling edge of internal AF signal 1: internal VSYNC signal
REDMODE[1:0]	h55[5:4]	RW	VS_ITU	0	0,1,2, 3	**Reduction Mode (ITU656 Output)** 00: 10 bit 01: 8 bit Y & C rounding 10: 8 bit Y dither, C rounding 11: 8 bit Y & C dither
OSDMODE[1:0]	h55[3:2]	RW	VS_ITU	0	0,1,2, 3	**OSD Mixing Mode (ITU656 Output)** 00: mix OSD & video (synchronized) 01: video only 10: OSD only 11: mix OSD & video (not synchronized)
OMODE[1:0]	h55[1:0]	RW	VS_ITU	0	0,1	**ITU656 Output Format** 00: 10bit ITU656 mode with embedded syncs 01: 8bit ITU656 mode with separate H/V-sync signals 1x: reserved
ADATA0[7:0]	h56[15:8]	R	VS_ITU		0..255	**ITU656 Input Data Byte 1**
ADATA1[7:0]	h56[7:0]	R	VS_ITU		0..255	**ITU656 Input Data Byte 0**
ADATA2[7:0]	h57[15:8]	R	VS_ITU		0..255	**ITU656 Input Data Byte 3**
ADATA3[7:0]	h57[7:0]	R	VS_ITU		0..255	**ITU656 Input Data Byte 2**
ADATA4[7:0]	h58[15:8]	R	VS_ITU		0..255	**ITU656 Input Data Byte 5**
ADATA5[7:0]	h58[7:0]	R	VS_ITU		0..255	**ITU656 Input Data Byte 4**
ADATA6[7:0]	h59[15:8]	R	VS_ITU		0..255	**ITU656 Input Data Byte 7**
ADATA7[7:0]	h59[7:0]	R	VS_ITU		0..255	**ITU656 Input Data Byte 6**
AD_RDY	h5A[0]	R	AD_RDY		0,1	**Ancillary Data Ready (ITU656 Input)** 0: no ancillary data available 1: ancillary data available reset automatically when read

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
NM						
NMLINE[8:0]	h64[15:7]	RW	VS_IP	0	0..511	**Noise Measurement Line** 0: line 2 1: line 3 261: line 1 (NTSC) 311: line 1 (PAL) lines 3-260 are not standard dependent
NMSENSE[1:0]	h64[6:5]	RW	VS_IP	0	0,1,2,3	**Noise Measurement Sensitivity** 00: *1 01: *2 10: *4 11: *8
NMPOS[1:0]	h64[4:3]	RW	VS_IP	0	0,1,2,3	**Noise Measurement Position** 00: 6.3 ms 01: 12.6 ms 10: 18.9 ms 11: 23.7 ms
NOISEME[6:0]	h65[6:0]	R	VS_IP		0..127	**Noise Measurement Value** 0000000: no noise 1111110: strong noise 1111111: strong noise or measurement failed
NMSTATUS	h66[0]	R	NMSTATUS		0,1	**Noise Measurement Status** 0: NOISEME has not been updated 1: New value of NOISEME available reset automatically when read
LBD						
LBSUB[1:0]	h6E[15:14]	RW	VS_IP	2	0..3	**Subsampling Mode** 0x: others (factor 1) 10: 20.25 MHz source (factor 1.5) 11: 40.5 MHz source (factor 3)
LBGRADRST	h6E[13]	RW	VS_IP	0	0,1	**Reset of Gradient Method** 0: no reset 1: reset
LBSTABILITY	h6E[12]	RW	VS_IP	0	0,1	**Stability Flag** 0: continuous format update 1: format update only once
LB43SENS	h6E[11]	RW	VS_IP	1	0,1	**Sensitivity to 4:3 Switch** 0: off 1: on
LBNGFEN	h6E[10]	RW	VS_IP	1	0,1	**No Gradient Found** 0: disable 1: enable
LBTHDNBNHA[4:0]	h6E[9:5]	RW	VS_IP	29	0..31	**Threshold for Darkness-Brightness Histogram Activity**
LBHSDEL[4:0]	h6E[4:0]	RW	VS_IP	10	0..31	**Histogram Stability Delay**
LBGRADDET[7:0]	h6F[15:8]	RW	VS_IP	50	0..255	**Threshold for Gradient Detection**
LBVWENDLO[7:0]	h6F[7:0]	RW	VS_IP	150	0..255	**Vertical Measure Window Lower End** granularity = 2 lines
LBHIWHITE[7:0]	h70[15:8]	RW	VS_IP	50	0..255	**Histogram White**
LBHWEND[7:0]	h70[7:0]	RW	VS_IP	180	0..255	**Horizontal Measure Window End** granularity = 4 pixel
LBHISTBLA[7:0]	h71[15:8]	RW	VS_IP	25	0..255	**Histogram Black**
LBHWST[6:0]	h71[6:0]	RW	VS_IP	36	0..127	**Horizontal Measure Window Start** granularity = 4 pixel
LBVWSTLO[6:0]	h72[14:8]	RW	VS_IP	96	0..127	**Vertical Measure Window Lower Start** granularity = 2 lines
LBFS	h72[7]	RW	VS_IP	0	0,1	**Field Subsampling Mode** 0: A+B fields 1: only A field
LBVWENDUP[6:0]	h72[6:0]	RW	VS_IP	73	0..127	**Vertical Measure Window Upper End** granularity = 2 lines
LBGSDEL[4:0]	h73[15:11]	RW	VS_IP	10	0..31	**Gradient Stability Delay**
LBGFBDEL[4:0]	h73[10:6]	RW	VS_IP	11	0..31	**Gradient Fall Back Delay**

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
LBVWSTUP[5:0]	h73[5:0]	RW	VS_IP	20	0..63	**Vertical Measure Window Upper Start** granularity = 2 lines
LBASDEL[4:0]	h74[15:11]	RW	VS_IP	0	0..31	**Activity Stability Delay**
LBACTIVITY[4:0]	h74[9:5]	RW	VS_IP	5	0..31	**Activity**
LBTHDNBNG[4:0]	h74[4:0]	RW	VS_IP	15	0..31	**Threshold for Darkness-Brightness Gradient**
LBFORMAT	h7B[15]	R	VS_IP		0,1	**Format** 0: 4:3 format 1: other format (letter box)
LBSUBTITLE	h7B[14]	R	VS_IP		0,1	**Subtitle Flag** 0: no subtitle 1: subtitle available
LBTOPTITLE	h7B[13]	R	VS_IP		0,1	**Toptitle Flag** 0: no toptitle 1: toptitle available
LBSLAA[6:0]	h7C[15:9]	R	VS_IP		0..127	**Start Line of Active Area** LBSLAA is measured in relation to VSYNC
LBELAA[8:0]	h7C[8:0]	R	VS_IP		0..511	**End Line of Active Area** LBELAA is measured in relation to VSYNC
LBDSTATUS	h7E[0]	R	LBD-STA-TUS		0,1	**Letter Box Detection Status** 0: no value available 1: new value available
PREFRAGEN						
YBORDER[3:0]	h82[15:12]	RW	VS_IP	1	0..15	**Y Value Preframe** luma = YBORDER*16
UBORDER[3:0]	h82[11:8]	RW	VS_IP	0	-8..7	**U Value Preframe** u chroma = UBORDER*16
VBORDER[3:0]	h82[7:4]	RW	VS_IP	0	-8..7	**V Value Preframe** v chroma = VBORDER*16
FRC_BGN	h83[15]	RW	VS_IP	0	0,1	**Background Generator** 0: disable 1: enable
HPRESC						
HSCPRESC[11:0]	h84[11:0]	RW	VS_IP	0	0..4095	**Horizontal Pre-Scaling Factor** subsampling factor by prescaler is 0: 1 (1080 pixel) 1536 1.333 (810 pixel) 2048: 1.5 (720 pixel) 4095: 2 (540 pixel)
HAAPRESC[1:0]	h85[15:14]	RW	VS_IP	0	0,1,2,3	**Horizontal Antialias Filter** 00: filter bypassed 01: weak characteristic 10: strong characteristic 11: automatic characteristic (weak or strong)
HDCPRESC[3:0]	h85[12:9]	RW	VS_IP	0	0,1,2,3,4, 5,6,7,8,9	**Horizontal Pre-Scaler Decimation** 0000: 1 0001: 2 0010: 3 0011: 4 0100: 6 0101: 8 0110: 12 0111: 16 1000: 24 1001: 32
APPL[9:0]	h86[9:0]	RW	VS_IP	540	0..540	**Active Pixel Per Line** number of active pixel stored in line memory, granularity: 2 pixel 0: 0 pixel 360: 720 pixel 540: 1080 pixel
NAPPLIP[9:0]	h87[9:0]	RW	VS_IP	92	0..648	**Not Active Pixel Per Line** start of active video for pre-scaler, granularity: 2 pixel 0: 0 pixel 92: 184 pixel 648: 1296 pixel

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
ALPF[9:0]	h88[9:0]	RW	VS_IP	1023	0..1023	**Active Lines Per Field Input** 0: no active line 288: 288 active lines 1023: 1023 lines
NALPFIP[8:0]	h89[8:0]	RW	VS_IP	0	0..312	**Not Active Lines Per Field Input** 0: start of active video in line 0 22: start of active video in line 22 312: start of active video in line 312
HPOSSC						
HPANON	h8A[15]	RW	VS_OP	0	0,1	**Horizontal Panorama Mode** 0: disable 1: enable
DISBORDETHPOS	h8A[14]	RW	VS_OP	1	0,1	**Disable Border Detection** 0: border detection active 1: border detection not active
CHROMDELHPOS	h8A[13]	RW	VS_OP	0	0,1	**Chrominance Delay** 0: no delay 1: half-pixel delay
HSCPOSC[11:0]	h8A[11:0]	RW	VS_OP	4095	0..4095	**Horizontal Post-Scaling Factor** 1024: upsampling factor is 4 2731: upsampling factor is 3/2 (720 -> 1080 pixels) 4095: upsampling factor is 1
HINC0[8:0]	h8B[8:0]	RW	VS_OP	0	-256..255	**Horizontal Post-Scaler Increment 0** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
HINC1[8:0]	h8C[8:0]	RW	VS_OP	0	-256..255	**Horizontal Post-Scaler Increment 1** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
HINC2[8:0]	h8D[8:0]	RW	VS_OP	0	-256..255	**Horizontal Post-Scaler Increment 2** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
HINC3[8:0]	h8E[8:0]	RW	VS_OP	0	-256..255	**Horizontal Post-Scaler Increment 3** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
HINC4[8:0]	h8F[8:0]	RW	VS_OP	0	-256..255	**Horizontal Post-Scaler Increment 4** 100000000: -32 pixels 000000000: 0 pixels 011111111: 31.875 pixels
HSEG1[10:0]	h90[10:0]	RW	VS_OP	0	0..2047	**Horizontal Segment 1** Granularity: 2 pixel 0: 0 pixel behind picture start 2047: 4094 pixel behind picture start
HSEG2[10:0]	h91[10:0]	RW	VS_OP	0	0..2047	**Horizontal Segment 2** Granularity: 2 pixel 0: 0 pixel behind picture start 2047: 4094 pixel behind picture start
HSEG3[10:0]	h92[10:0]	RW	VS_OP	0	0..2047	**Horizontal Segment 3** Granularity: 2 pixel 0: 0 pixel behind picture start 2047: 4094 pixel behind picture start
HSEG4[10:0]	h93[10:0]	RW	VS_OP	0	0..2047	**Horizontal Segment 4** Granularity: 2 pixel 0: 0 pixel behind picture start 2047: 4094 pixel behind picture start
CLOCK						
LOMIDFREQ	hF0[13]	RW		0	0,1	**Freerun Frequency** 0: 20.25MHz 1: 13.5MHz

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
OSDCLKCTRL[1:0]	hF0[12:11]	RW		0	0,1,2, 3	**OSD Clock Control** 00: programmable pixclk 01: backend clock 10: backend clock /2 11: programmable pixclk
OSDOFF	hF0[10]	RW		1	0,1	**OSD Mode** 0: normal operation 1: standby
RGBOFF	hF0[9]	RW		1	0,1	**RGB Mode** 0: normal operation 1: standby
CVBSOFF	hF0[8]	RW		1	0,1	**CVBS Mode** 0: normal operation 1: standby
CLKFE40OFF	hF0[7]	RW		1	0,1	**ADC Mode** 0: normal operation 1: standby
ITUIOFF	hF0[6]	RW		1	0,1	**ITU Input Mode** 0: normal operation 1: standby
ITUOOFF	hF0[5]	RW		1	0,1	**ITU Output Mode** 0: normal operation 1: standby
DISPOFF	hF0[4]	RW		1	0,1	**Display Mode** 0: normal operation 1: standby
DEFLOFF	hF0[3]	RW		1	0,1	**Deflection Mode** 0: normal operation 1: standby
LLPLLOFF	hF0[2]	RW		1	0,1	**LLPLL Mode** 0: normal operation 1: standby
FCLKB2LL	hF0[1]	RW		0	0,1	**Force Clock Backend to Line-Locked**
PLLOFF	hF0[0]	RW		0	0,1	**648MHz PLL Mode** 0: normal operation 1: standby
SUPERVISION						
PUPDAC	hF1[2]	R	PUP-DIG		0,1	**Voltage Supervision Status VSUP3.3DAC** 0: supply voltage above limit 1: supply voltage below limit
PUPIO	hF1[1]	R	PUP-DIG		0,1	**Voltage Supervision Status VSUP3.3IO** 0: supply voltage above limit 1: supply voltage below limit
PUPDIG	hF1[0]	R	PUP-DIG		0,1	**Voltage Supervision Status VSUP1.8DIG** 0: supply voltage above limit 1: supply voltage below limit
I2C						
DISCPURES[15:0]	hF9[15:0]	RW		0	0, h0512, h1408, h1505, h1606, h3A56, hA534	**Reset Signature** 0512h: CPU reset (without Watchdog) 1408h: VSP & DPS reset 1505h: XDFP reset 1606h: XDFP, VSP, DPS, CPU & Watchdog reset 3A56h: disable XDFP, VSP, DPS, CPU & Watchdog reset A534h: disable voltage supervision reset

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
VCTH_ID_SET[4:0]	hFB[12:8]	RW		0	0,1,2,3,4, 5,6,7,8,9, 10,11	**Set VCTH Identification** override bond options for software development (only possible in EMU version) 0: EMU 1: VCT490y 2: VCT491y 3: VCT492y 4: VCT493y 5: VCT494y 6: VCT495y 7: VCT496y 8: VCT497y 9: VCT498y 10: VCT499y 11-31: reserved for future use
AUTOINC	hFB[0]	RW		0	0,1	**I2C Subaddress Autoincrement** defines subaddress autoincrement for all VPS & DPS register 0: subaddress autoincrement after 2 byte access 1: static subaddress
VCTH_ID_RD[4:0]	hFC[12:8]	R			0,1,2,3,4, 5,6,7,8,9, 10,11	**VCTH Identification** 0: EMU 1: VCT490y 2: VCT491y 3: VCT492y 4: VCT493y 5: VCT494y 6: VCT495y 7: VCT496y 8: VCT497y 9: VCT498y 10: VCT499y 11-31: reserved for future use
REV[4:0]	hFC[4:0]	R			1,2,3,4	**VCTH Revision** h01: 01-0x h02: 02-0x h03: 03-0x h04: tbd
VS_OP_STAT	hFD[4]	R	VS_CD		0,1	**Vertical Update Status Scaler Output** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
VS_IP_STAT	hFD[3]	R	VS_CD		0,1	**Vertical Update Status Scaler Input** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
VS_ITUI_STAT	hFD[2]	R	VS_CD		0,1	**Vertical Update Status ITU656 Input** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
VS_RGB_STAT	hFD[1]	R	VS_CD		0,1	**Vertical Update Status RGB Processing** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
VS_CD_STAT	hFD[0]	R	VS_CD		0,1	**Vertical Update Status Color Decoder** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
IM_OP	hFE[4]	RW		0	0,1	**Immediate Update Scaler Output** 0: no immediate take-over 1: immediate take-over
IM_IP	hFE[3]	RW		0	0,1	**Immediate Update Scaler Input** 0: no immediate take-over 1: immediate take-over
IM_ITUI	hFE[2]	RW		0	0,1	**Immediate Update ITU656 Input** 0: no immediate take-over 1: immediate take-over

Table 3–9: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
IM_RGB	hFE[1]	RW		0	0,1	**Immediate Update RGB Processing** 0: no immediate take-over 1: immediate take-over
IM_CD	hFE[0]	RW		0	0,1	**Immediate Update Color Decoder** 0: no immediate take-over 1: immediate take-over
VS_OP	hFF[4]	RW		1	0,1	**Vertical Update Scaler Output** 0: no vertical take-over 1: vertical take-over
VS_IP	hFF[3]	RW		1	0,1	**Vertical Update Scaler Input** 0: no vertical take-over 1: vertical take-over
VS_ITUI	hFF[2]	RW		1	0,1	**Vertical Update ITU656 Input** 0: no vertical take-over 1: vertical take-over
VS_RGB	hFF[1]	RW		1	0,1	**Vertical Update RGB Processing** 0: no vertical take-over 1: vertical take-over
VS_CD	hFF[0]	RW		1	0,1	**Vertical Update Color Decoder** 0: no vertical take-over 1: vertical take-over

4. Data Sheet History

1. Advance Information: “VCT 49xyl, VCT 48xyl Video Processor”, 12.12.2003, 6251-573-4-1AI. First release of the advance information.

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ADVANCE INFORMATION

VCT 49xyI, VCT 48xyI

Volume 5: Display and Deflection Processor

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Contents

Contents, continued

1. Introduction

Volume 5 describes the Display and Deflection Processor (DDP) of the VCT 49xyl, VCT 48xyl.

1.1. Chip Architecture

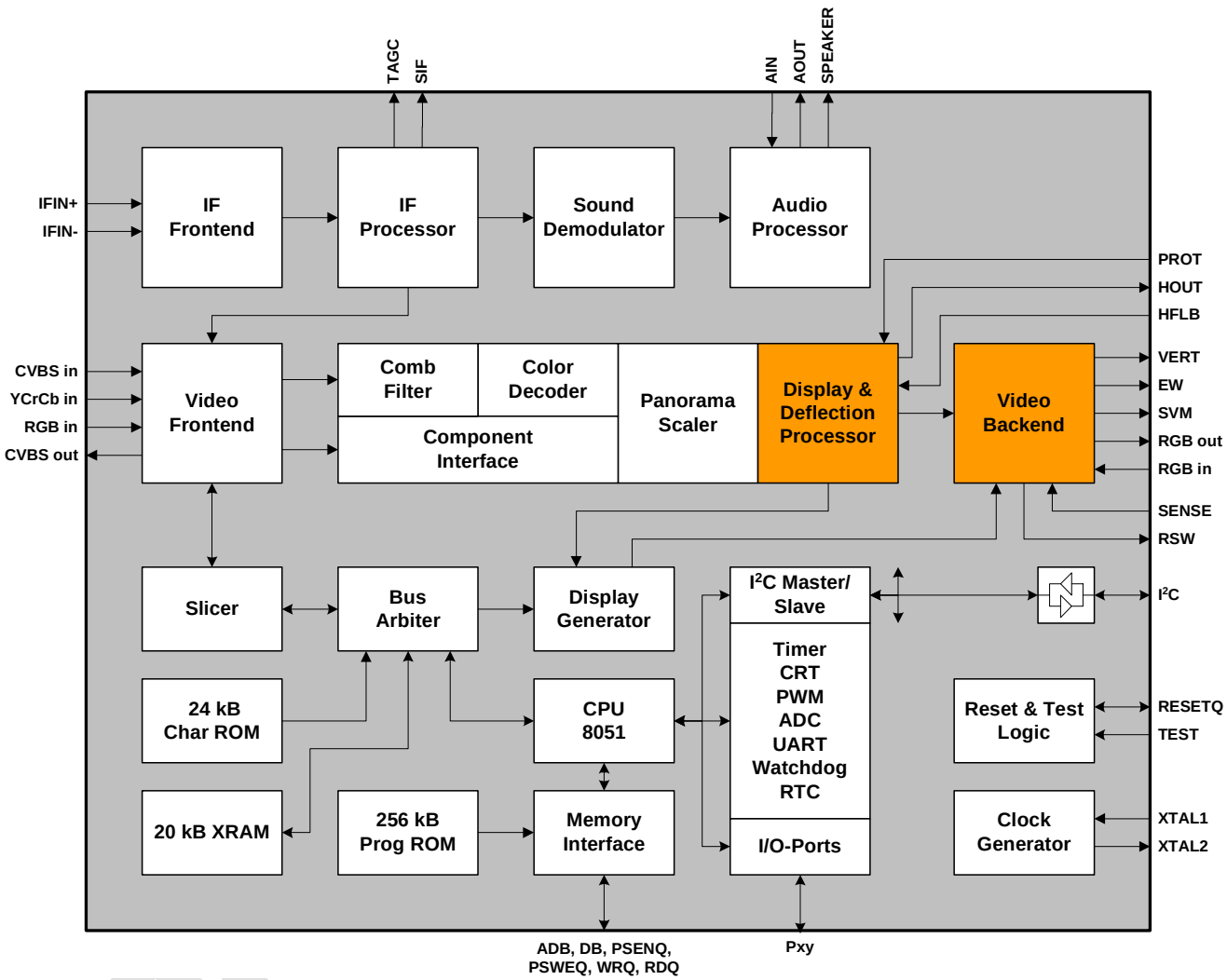


Fig. 1–1: Block diagram of the VCT 49xyl, VCT 48xyl

1.2. Features

The DDP contains the entire digital video component and deflection processing, as well as all analog interfaces to display the picture on a Cathode Ray Tube (see Fig. 1–1).

Display Processing

- dynamic contrast improvement (DCI)
- dynamic black level expander (BLE)
- dynamic black stretch (DBS) with peak black and activity detection and contrast adaption
- luma sharpness enhancement (LSE)
- color transient improvement (CTI)
- brightness, contrast, saturation and tint
- programmable YC_rC_b to RGB matrix
- static black stretch, blue stretch, gamma correction by a programmable Non-linear Colorspace Enhancer (NCE) on RGB

– histogram calculation (8 amplitude steps, taken from 16 regions per line across the whole picture)
– one external analog RGB Fast Blank input
– one internal analog RGB Fast Blank input for OSD insertion with reduced contrast switch (0, 25%, 50%, 75%)
– average beam current limiter (ABL)
– peak beam current limiter (PBL)
– automatic picture tube adjustment (cutoff, white-drive)
– picture frame and test pattern generator
– H and V sync outputs to synchronize an external analog RGB source (e.g. PIP)

Deflection Processing

– vertical sawtooth (amplitude, linearity, S-correction, zoom)
– East/West parabola (trapeze, cushion, upper/lower corner 4th and 6th order)
– scan velocity modulation output
– non-linear EHT compensation for vertical/East-West
– dynamic horizontal EHT (amplitude/phase compensation with T_c ~ 1 line)
– vertical angle and bow correction
– differential vertical outputs
– vertical zoom via deflection adjustment
– horizontal and vertical protection circuit
– black switch-off procedure (BSO)
– soft start/stop of H-drive
– supports horizontal and vertical dynamic focus

Backend Features

– external analog SCART (RGB/FB) input
– internal analog OSD (RGB/FB/COR) input
– fast blank priority and monitoring via I^2C
– analog RGB and SVM current output
– user brightness for main and external RGB signal
– user contrast for analog RGB insertion
– differential vertical sawtooth
– E/W parabola
– separate ADC for beam current measurement

1.3. Overview

The DDP operates with a line-locked 20.25 MHz clock to provide a higher horizontal resolution for feature processing.

For the picture improvement, luma and chroma are processed separately. The luminance contrast ratio can be extended with a dynamic black level expander. In addition the frequency characteristics are improved by a luma sharpness enhancement. The chroma signal is enhanced with a transient improvement (CTI), with proper limitation to avoid wrong colors.

The programmable RGB matrix covers control of color saturation and temperature. A digital white drive control is used to adjust the white balance and for the beam current limitation to prevent the CRT from overload. A non-linear color-space enhancer (NCE) on RGB provides various amplitude characteristics.

High-speed D/A converters are used to convert digital RGB to analog signals. Separate D/A converters control brightness and cutoff. For picture tubes equipped with an appropriate yoke, a scan velocity modulation (SVM) signal is calculated using a differentiated luminance signal.

Two analog sources can be inserted in the main RGB, controlled by separate fast blank (FBL) signals. Contrast and brightness are adjusted separately from main RGB. One internal input is dedicated to RGB for on-screen display (OSD). The second external RGB input is processed with a programmable contrast reduction.

An integrated processor controls the horizontal and vertical deflection, tube measurement loops and beam current limitation. It is also used to calculate an amplitude histogram of the displayed image.

The horizontal deflection is synchronized with two numeric phase-locked loops (PLL) to the incoming sync. One PLL generates the horizontal timing signals, e.g., blanking and key-clamping. The second PLL adjusts the phase of the horizontal drive pulse with a subpixel accuracy less than 1 ns.

Vertical deflection and East/West correction waveforms are calculated as 6th order polynomials. This allows adjustment of an East/West parabola with trapezoidal, pin cushion and an upper/lower corner correction (even for real flat CRTs), as well as a vertical sawtooth with linearity and S-correction. Scaling both waveforms, and limiting to fixed amplitudes, performs a vertical zoom or compression of the displayed image. A field and line frequent control loop compensates EHT distortions depending on picture content.

2. Functional Description

2.1. Display Processing

The display processing part provides a variety of picture improvement features, such as automatic contrast improvement, black level expansion, and luma sharpness enhancement in the luminance part, as well as transient improvement in the chrominance path (see Fig. 2–1). In addition, it supports the adjustment of contrast, brightness, saturation and tint.

A pixel mixer allows the insertion of additional picture layers such as a picture frame, a curtain and a test pattern layer, before the YC_rC_b signals are converted to RGB color space by a programmable matrix.

Furthermore, a non-linear color-space enhancer on RGB allows all kinds of amplitude characteristics for each path, separately.

High-speed D/A converters are used to convert the digital RGB to analog signals.

The display processing part operates on a common clock frequency of 20.25 MHz, line-locked, providing a frequency headroom for the mentioned high-quality picture enhancements.

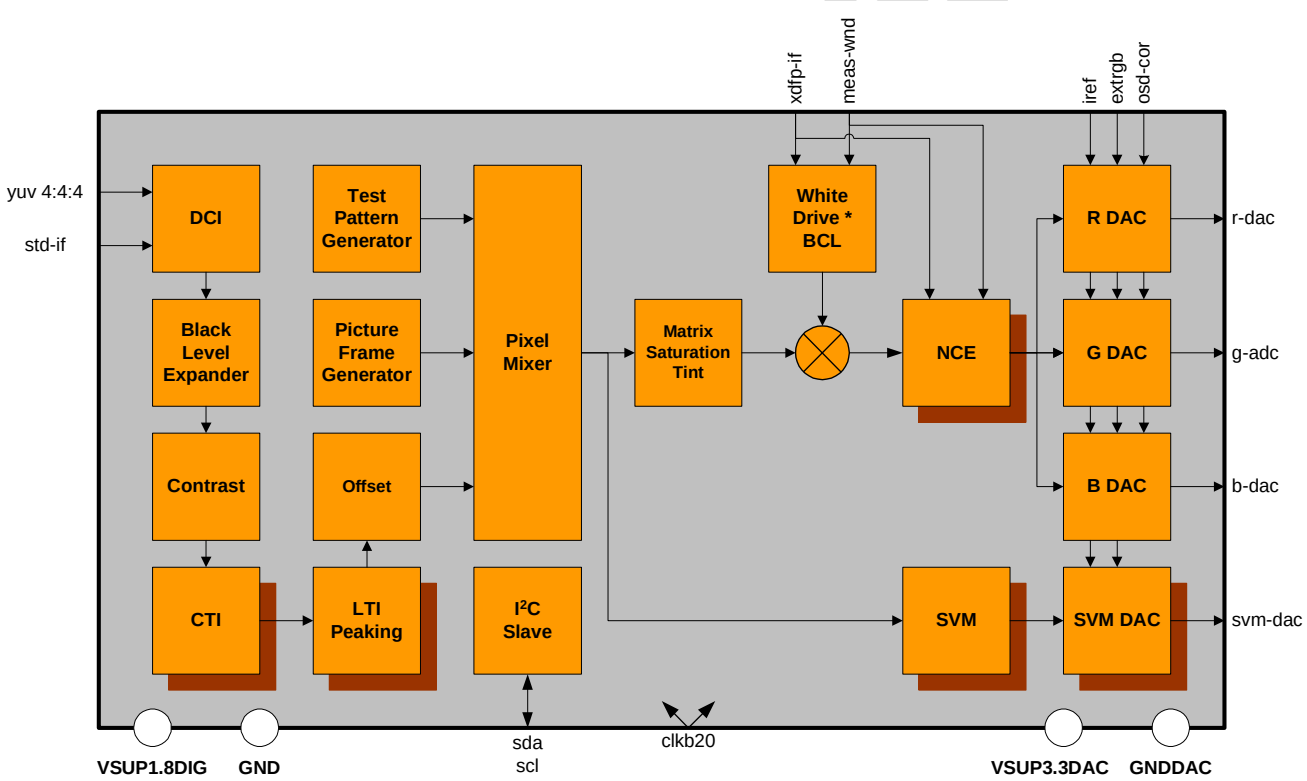


Fig. 2–1: Display Processing Block Diagram

2.1.1. Dynamic Contrast Improvement (DCI)

Although there is a strong demand on picture contrast, every video display has a limited dynamic range. Especially flat display panels, such as LCDs and PDPs (plasma display panels) have a lower dynamic range compared to CRT. The picture contrast cannot be increased by simply increasing the video signal amplitude because exceeding the display-dynamic range causes unwanted effects. An efficient use of display dynamic range depending on the picture contents increases perceived picture contrast and quality.

The basic function of DCI is to analyze the picture framewise and to adjust the parameters of a dual segment transfer function, depending on the analyzed results for the best subjective picture quality. Therefore, each image frame is analyzed for three different characteristics (see Fig. 2–2). The image average brightness (MEAN) of the input picture, which is derived from a histogram of the input picture, a dark and a white sample distribution of the output picture. These parameters control the transfer function. The dual segment transfer function consists of two segments with an adaptive pivot point: a lower segment for dark samples and an upper segment for light samples. The gain of the lower segment is adaptive to the dark sample distribution. A higher gain results from fewer dark samples and a lower gain from a higher number of dark samples. The gain is limited in a certain range. The gain of the upper segment is adaptive to the white sample distribution. Its functionality is the same as for the lower segment.

A special DCI demo mode can be selected to show the left side of the picture unprocessed and the right side processed by the DCI.

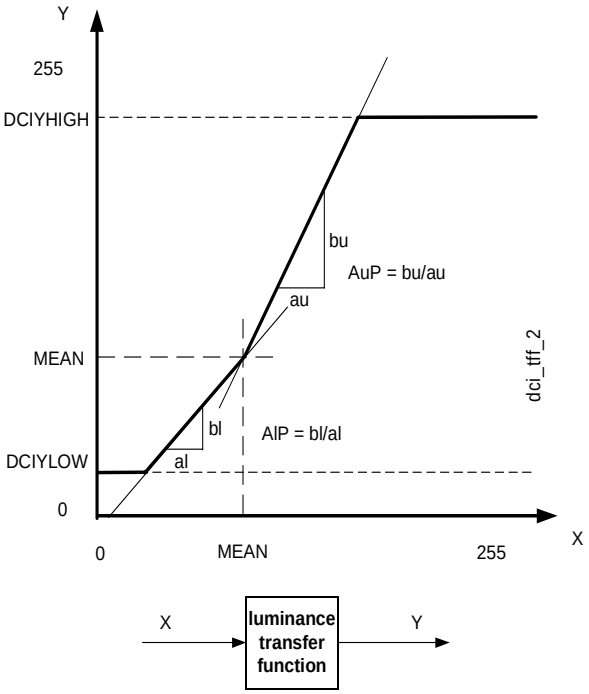


Fig. 2–2: DCI basic function

2.1.2. Black Level Expander/Compressor (BLEC)

The black level expander/compressor modifies the luminance signal with an adjustable non-linear function to enhance the contrast of the picture (see Fig. 2–3). Dark areas are stretched to black, while bright areas remain unchanged. Advantageously, this black level processing is performed dynamically and only if it will be most noticeable to the viewer.

The BLEC supports the following modes (see Fig. 2–4):

– dynamic BLEC mode
  This is the normal operation mode. The expansion depends on a pixel analysis.

– auto contrast mode
  In the auto contrast mode, the TILT point is shifted to its maximum.

– static BLEC mode
  In the static mode, the expansion depends on a programmable value SBLE.

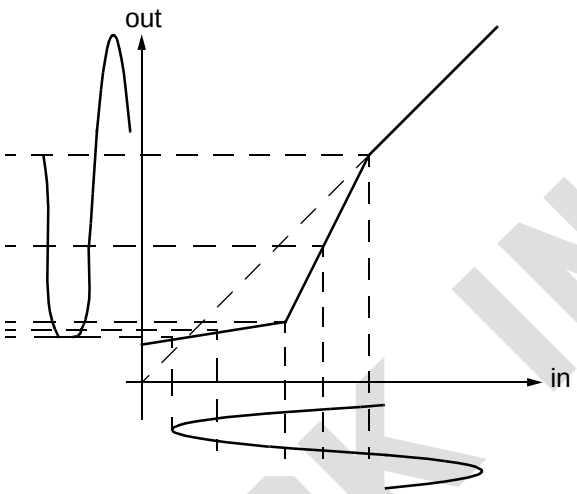
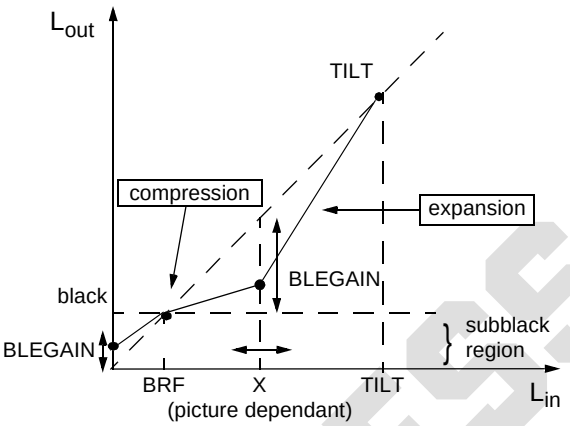
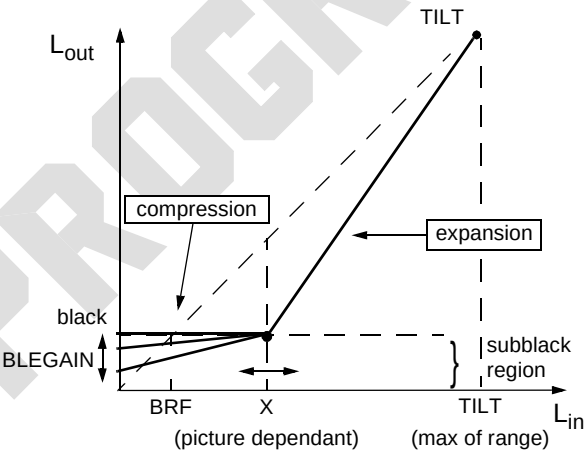


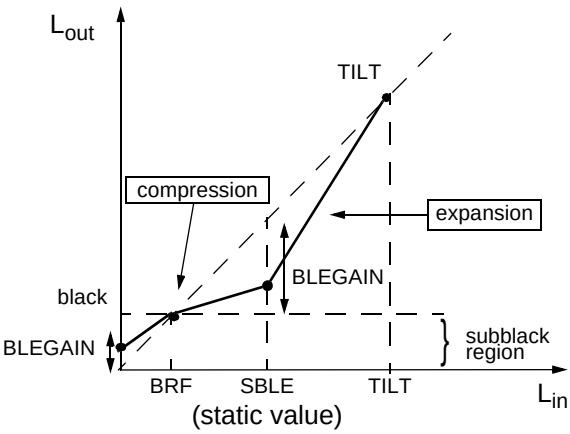
Fig. 2–3: BLEC function



Dynamic BLEC mode



Auto-contrast mode



Static BLEC mode

Fig. 2–4: BLEC modes

2.1.3. Luma Sharpness Enhancer (LSE)

Sharpness is one of the most critical features for optimum picture quality. This important processing is performed in the LSE circuitry of the DDP.

It consists of the dynamic peaking and the luma transient improvement (LTI). The luma input signal is processed in the peaking and LTI block in parallel. Both output signals are combined depending on the selected LSE characteristics.

2.1.3.1. Dynamic Peaking

The dynamic peaking improves the details of a picture using contour emphasis. It adapts to the amplitude and the frequency of the input signal. Small detail amplitudes are sharpened, while large detail amplitudes stay more or less unmodified.

The maximum dynamic range of small high-frequency detail amplitudes is 14 dB. The dynamic range of large detail amplitudes is limited automatically by a non-linear function that does not create any visible alias components (see Fig. 2–5).

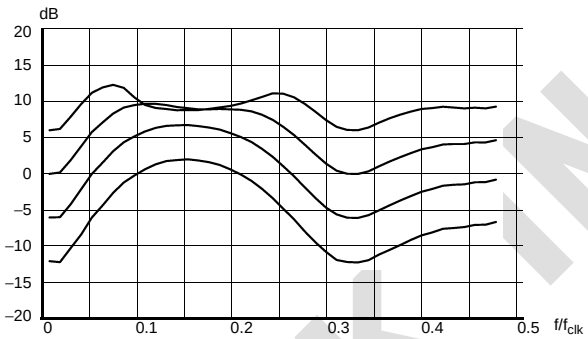


Fig. 2–5: Dynamic peaking frequency response

The peaking features two selectable center frequencies of 2.5 MHz or 3.2 MHz (see Fig. 2–6). An adjustable coring threshold prevents the enhancement of small noise amplitudes.

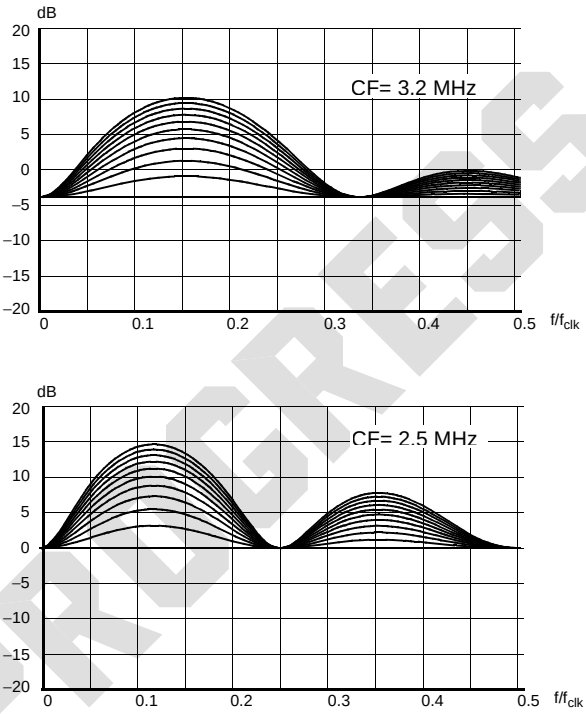


Fig. 2–6: Total frequency response for peaking filter

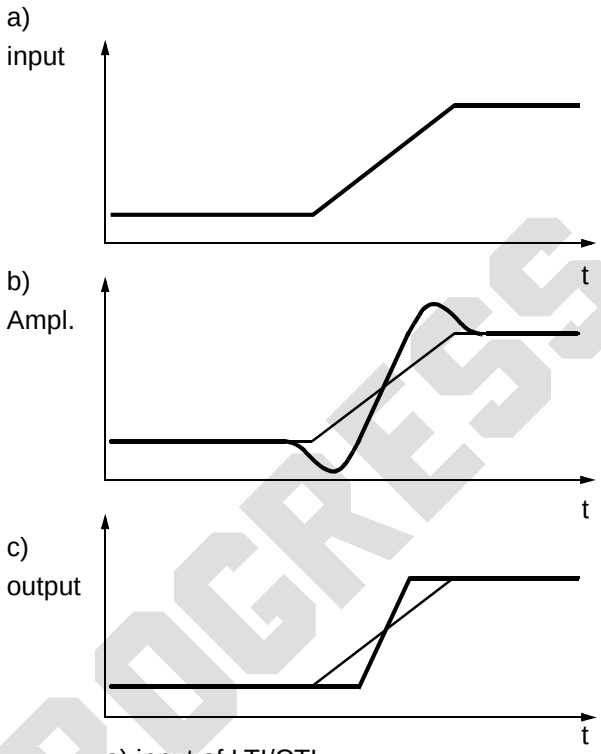
2.1.3.2. Luma Transient Improvement (LTI)

For small detail amplitudes, dynamic peaking is the most appropriate process to improve sharpness. However, for large amplitudes even small over and/or undershoots of the peaking are too annoying.

The luma transient improvement enhances the slope of picture detail without these effects by a non-linear processing. The contour correction signal calculated in this block is limited to the adjacent extreme values to prevent over and undershoots (see Fig. 2–7).

The LTI features an adjustable gain control and an adjustable coring threshold to prevent the enhancement of small noise amplitudes.

The contour correction signals of the dynamic peaking and the LTI block are combined adaptively to achieve best sharpness impression.



a) input of LTI/CTI
b) correction signal
c) sharpened output of LTI/CTI

Fig. 2–7: Luma/chroma transient improvement

2.1.4. Chrominance Transition Improvement (CTI)

The CTI improves the horizontal transitions of the chrominance signals, resulting in a better picture sharpness.

A correction signal is calculated by differentiation of the color difference signals. The differentiation is selectable according to the bandwidth of the input signal, e.g., for decoded CVBS signals or component signals, respectively. The amplitude of the correction signal is adjustable. Small noise amplitudes in the correction signal are suppressed by an adjustable coring circuit. To eliminate “wrong colors”, which are caused by over and undershoots at the chroma transition, the sharpened chroma signals are limited to a proper value automatically (see Fig. 2–7).

2.1.5. Pixel Mixer

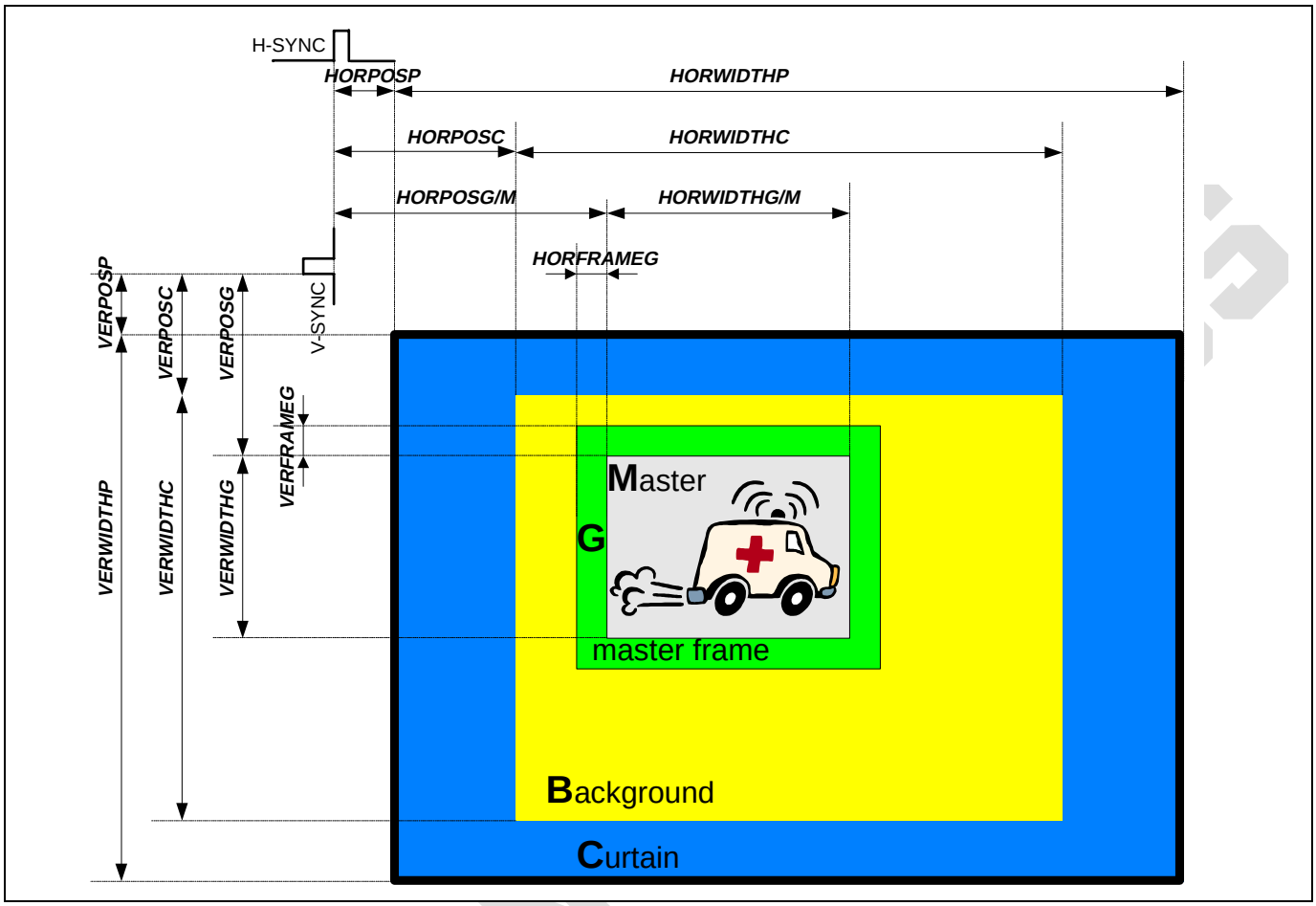


Fig. 2–8: Multi-layer Pixel Mixer output

The pixel mixer combines the following additional layers with the main video (master channel M):

– Picture Frame G

– Curtain C

– Test Pattern and Background P

The position and size of each layer is defined by the corresponding I^2C-register HORPOSx, VERPOSx, HORWIDTHx, VERWIDTHx, HORFRAME and VERFRAME settings (see Fig. 2–8).

Over-/underlay of the different layers depends on the selected priority PRIOx (0 = lowest ... 7 = highest priority). Thus, each layer requires its own priority and it is not possible to use an identical priority for two or more layers.

2.1.5.1. Picture Frame Generator

The picture frame generator provides an adjustable border surrounding the displayed picture, e. g. if the picture does not fill the full screen. Another possibility is the insertion of a horizontal or vertical stripe, e. g. for split-screen applications. Size, position, and active area are programmable, as well as the frame color.

2.1.5.2. Window Generator

The window generator provides a 3-dim window to overlay a curtain on top of the displayed picture. Depending on the window start position and direction (open or close window) the size of the window is increased or decreased in horizontal and /or vertical direction by every field.

Fig. 2–9 shows the horizontal window function. The window can be closed or opened.

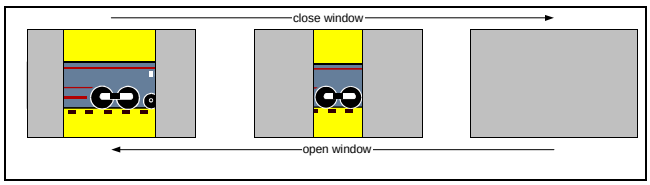


Fig. 2–9: Horizontal windowing

The horizontal window generation depends on the following conditions

– the selected horizontal start position WINDHST (window is open or closed) and

– the selected horizontal direction WINHDR (close or open the window)

– enable horizontal window generator WINDHON

By toggling WINDHDR the window generator changes from “close” to “open” or vice versa. The speed of the horizontal window is programmable. Fig. 2–10 shows the vertical window function.The vertical window generation is similar to the horizontal window generation.

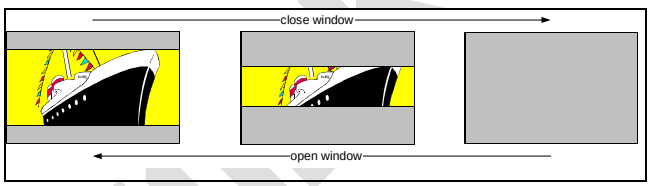


Fig. 2–10: Vertical windowing

Combining the horizontal and vertical window generator supports the generation of a 2-dimensional window (see Fig. 2–11).

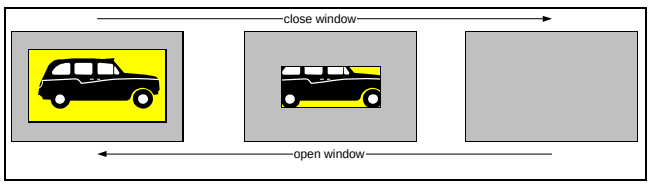


Fig. 2–11: Horizontal and vertical windowing

2.1.5.3. Test Pattern Generator

The test pattern generator provides the following eight video patterns (see Fig. 2–12):

1. colored background (constant luminance and chrominance)
2. geometry (0% and 9.4% overscan grid, as well as center position grid)
3. balance (white drive and cutoff reference)
4. Y ramp (Y ampl. = –7...106%, increased by 2 every clock cycle, $C_r = C_b = 0$)
5. Y ramp soft (Y ampl. = –7...113%, increased by 1 every 2nd clock cycle, $C_r = C_b = 0$)
6. YUV ramp (Y ampl. = –7...113%, increased by 1 every 2nd clock cycle, $C_r = C_b = 0$...100%, increased by 1 every 5th clock cycle)
7. Color bars (ITU100/75/75)
8. Crosshatch

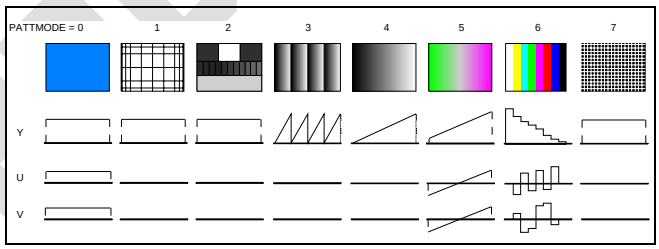


Fig. 2–12: Available test pattern

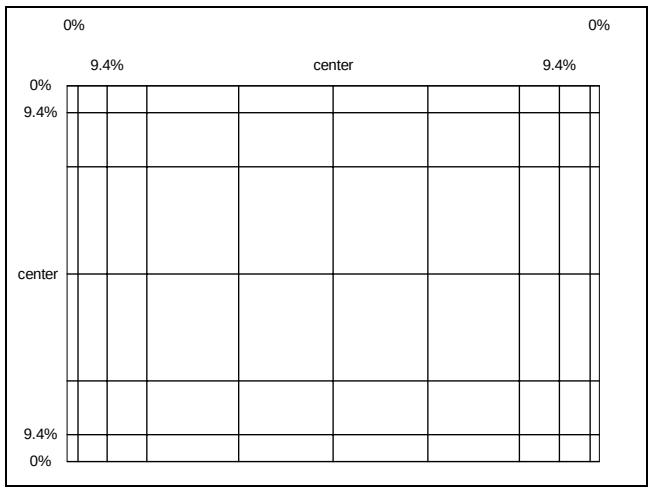


Fig. 2–13: Geometry test pattern

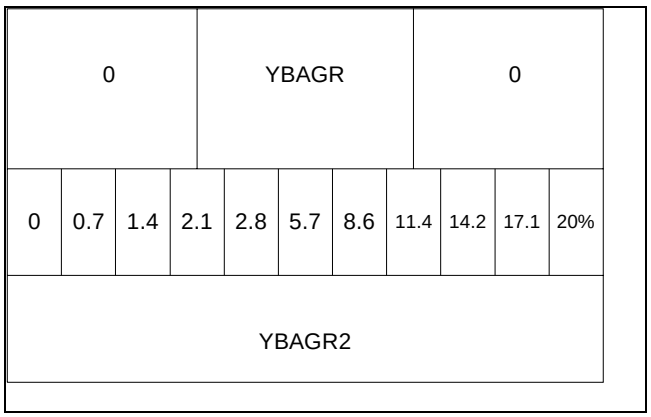


Fig. 2–14: Balance test pattern

The size of the test pattern is 1080 pixel x 288 lines. For a display area greater than 1080 x 288, the surrounding pixels are blanked.

2.1.6. Contrast, Brightness, Saturation and Tint

The luminance signal is multiplied by a contrast value between 0 and 2 subdivided into 64 steps. The matrix coefficients are adapted to the contrast value automatically to preserve the selected ratio between contrast and color saturation.

The digital brightness value shifts the luminance by max. ±100% of its maximal amplitude (contrast gain =1). It is desirable to keep a small positive offset with the signal to prevent peaking undershoots and/or picture content below black from being cut.

The chrominance signal is multiplied by a saturation value between 0 and 4 subdivided into 64 steps. The tint shifts the color space by ±15 degrees.

2.1.7. Programmable Inverse Matrix

Six multipliers in parallel perform the matrix multiplication to transform the C_r and C_b signals to R–Y, B–Y, and G–Y. The initialization values of the matrix corresponds to the standard ITU-R (CCIR) matrix:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.402 \\ 1 & -0.345 & -0.713 \\ 1 & 1.773 & 0 \end{bmatrix} \times \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix}$$

The multipliers are also used to adjust color saturation and picture contrast. The matrix computes:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \frac{CTM}{32} \times \frac{SATM}{32} \times \frac{1}{64} \times \begin{bmatrix} MR1M & MR2M \\ MG1M & MG2M \\ MB1M & MB2M \end{bmatrix} \times \begin{bmatrix} Cb \\ Cr \end{bmatrix} + \left(\frac{CTM}{32} \times Y\right)$$

2.1.8. Non-linear Colorspace Enhancer (NCE)

This block allows all kinds of non-linear corrections such as gamma correction, blue stretch, peak white limitation.

The Non-linear Colorspace Enhancer NCE has following parameters

– Gamma correction with 2 selectable gamma base functions (common for RGB)

– subjective white shaping for R,G and B separately

– Peak White limitation tilt point and gain (common for RGB)

These different functions are cascaded to enable a large palette of non-linear functions.

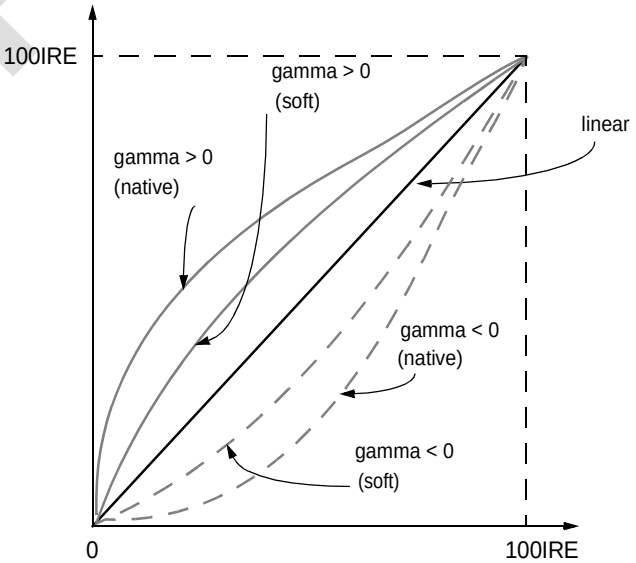


Fig. 2–15: Gamma characteristic

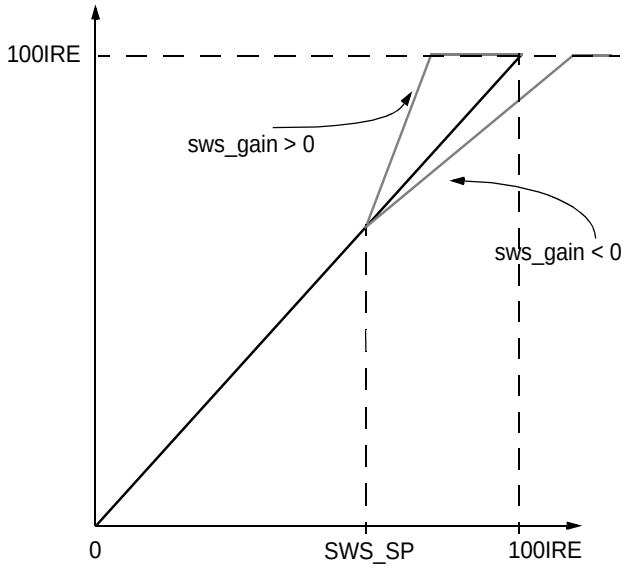


Fig. 2–16: Subjective white shaping characteristics

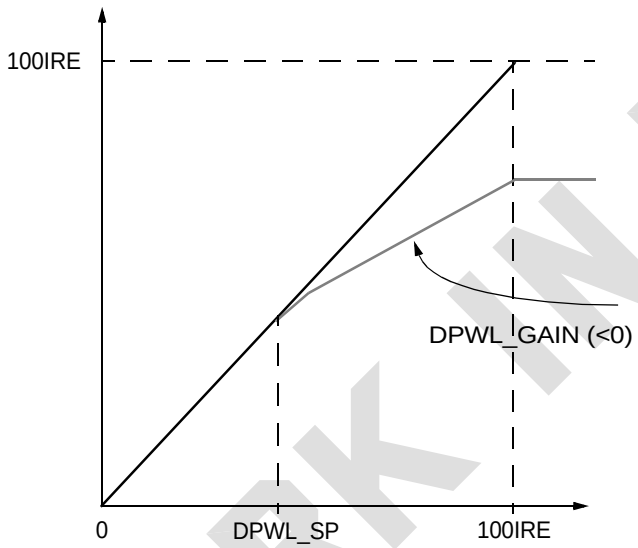


Fig. 2–17: Digital peak white limiter characteristics

2.1.9. Scan Velocity Modulation

Picture tubes equipped with an appropriate yoke can use the Scan Velocity Modulation signal to vary the speed of the electron gun during the entire video scan line dependent upon its content. Transitions from dark to bright will first speed up and then slow down the scan; vice versa for the opposite transition (see Fig. 2–18).

The signal delay is adjustable by ±3.5 clocks in half-clock steps in respect to the analog RGB output signals. This is useful to match the different group delay of analog RGB amplifiers to the one for the SVM yoke current.

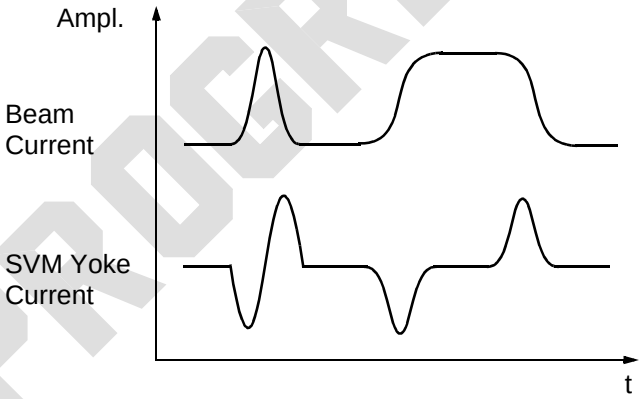


Fig. 2–18: SVM signal waveform

2.2. Analog Component Back-End

The digital RGB signals are converted to analog RGB by three digital to analog converters (DAC).

Each RGB signal has two additional DACs to adjust analog brightness (40% of the full RGB range) and cut-off / black level (60% of the full RGB range). An additional fixed current is applied for the blanking level.

The back-end supports the insertion of two external analog component signals, e.g., OSD or PIP. These signals are clamped, converted by a voltage/current converter (U/I-DAC), and inserted into the main RGB by the fast blank switch.

The analog RGB outputs are current outputs with current-sink characteristics. The maximum current drawn by the output stage is obtained with peak white RGB.

The controlling of the white drive/analog brightness and also the external contrast and brightness adjustments is done via the internal XDFP Processor.

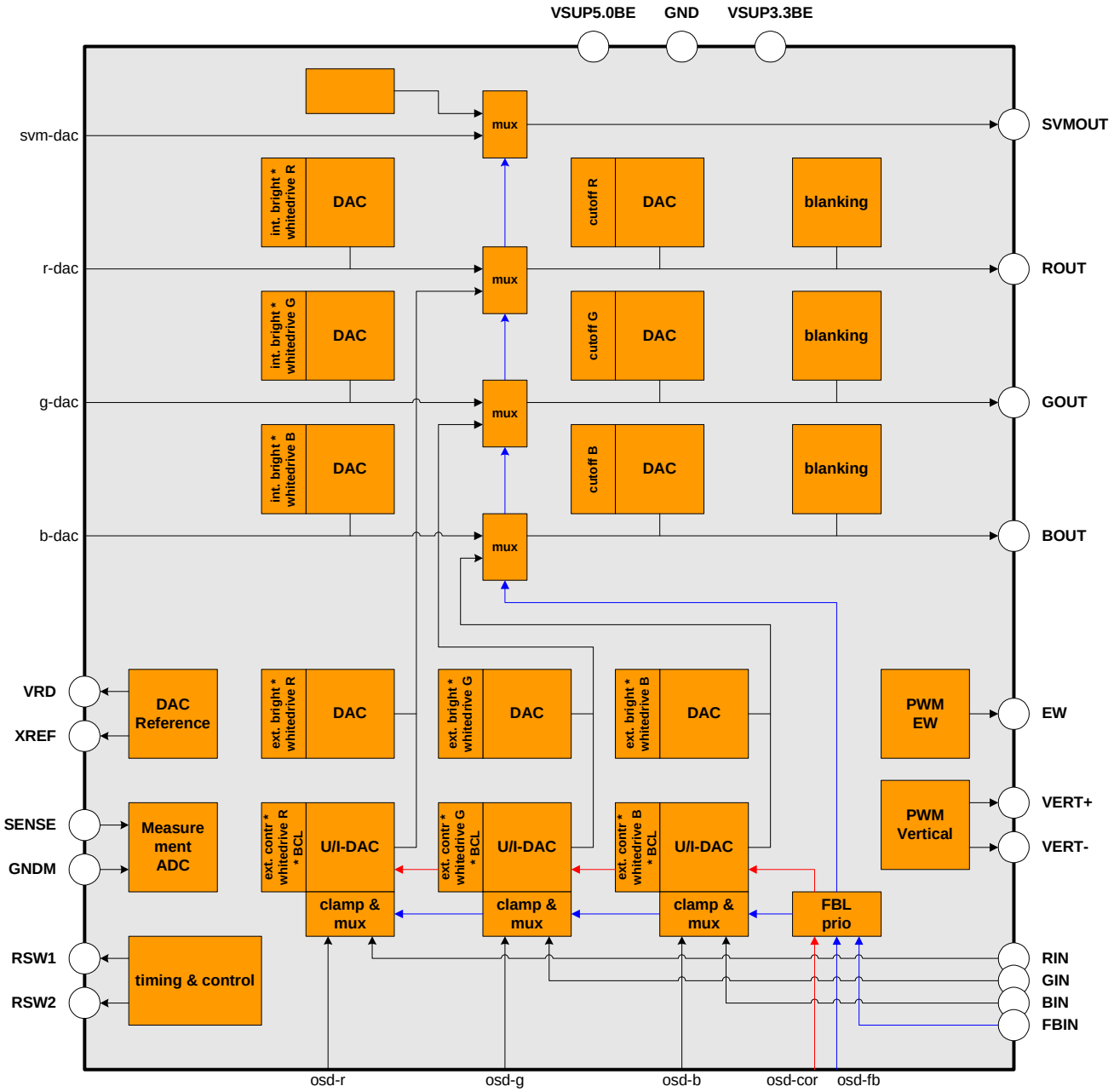


Fig. 2–19: Analog component back-end

2.2.1. Analog RGB Insertion

The DDP supports the insertion of:

– 1 external analog RGB signals (e.g. PIP) and

– 1 internal analog RGB signal (OSD).

Each component signal is clamped and inserted into the main RGB by the fast blank switch. Both component signals are adjustable independently as regards DC level (brightness) and magnitude (contrast).

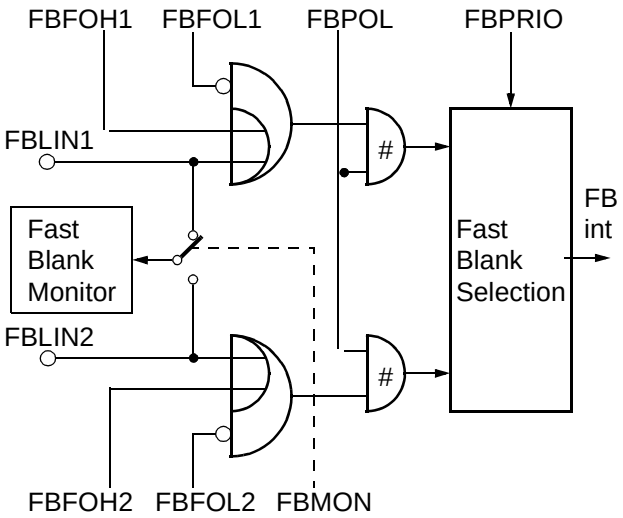


Fig. 2–20: Fast Blank selection logic

Over/underlay of the external component signal and the main RGB signal depends on the fast blank input signals and the corresponding I^2C register (see Fig. 2–20). Both fast blank inputs must be either active low or active high.

All signals for analog component insertion (RIN1/2, GIN1/2, BIN1/2, FBLIN1/2, HCS) must be synchronized to the digital RGB.

2.2.2. Fast Blank Monitor

The presence of external analog RGB sources is detected by means of a fast blank monitor. The status of the selected fast blank input is monitored via an I^2C register. There is a 2-bit information, giving static and dynamic indication of a fast blank signal. The static bit is directly reading the fast blank input line, whereas the dynamic bit is reading the status of a flip-flop triggered by the negative edge of the fast blank signal.

With this monitor logic it is possible to detect if there is an external RGB source active and if it is a full screen insertion or only a box. The monitor logic is connected directly to the FBLIN1 or FBLIN2 pin. Selection is done via I^2C register.

2.2.3. Reduced Contrast Control

Insertion of transparent text pages or OSD onto the video picture is often difficult to read, especially if the video contrast is high. The DDP features a contrast reduction of the video background of 25%, 50% or 75% by means of a contrast reduction signal (COR). This signal is supplied by the display generator of the controller. Inside the reduced contrast area the video picture is displayed with reduced contrast, while the analog component signals are still displayed with full contrast.

2.2.4. CRT Measurement and Control

In order to define accurate color on different CRT displays, the cut-off and white drive settings have to be adjusted depending on the characteristic of CRT phosphor. To guarantee correct colors during the for the lifetime of the display, a build in automatic tube control loop measures and adjusts the black level on every field and white point every third field.

The display processor is equipped with a PDM-ADC for all picture tube measuring purposes. This MADC is connected to the SENSE input pin, the input range is 0 to 2.6 V.

Cutoff and white drive current measurement are carried out during the vertical blanking interval. The current range for cutoff measurement is set by connecting the sense resistor R1 to the SENSE input. Due to the fact of a 1:10 relation between cutoff and white drive current the range select 2 output (RSW2) becomes active for the white drive measurement and connects R3 in parallel to R1, thus determining the correct current range. During the active picture, the MADC is used for the average beam current limiter. Again a different measurement range is selected with active range select 1&2 outputs (RSW1&RSW2) connecting R2 in parallel to R3 and R1. The corresponding timing is shown in Fig. 2–21 and Fig. 2–22.

These measurements are typically done at the summation point of the picture tube cathode currents.

Another method uses two different current measurements:

– The range switch 1 pin (RSW1) can be used as a second sense input, selectable by software. In this case, the cutoff and white drive currents are measured as before at the SENSE input.

– The active picture measurement can be done with the second sense input (RSW1). The signal may come (via a proper interface) from the low end of the EHT coil (CRT anode current). In this case, the resistor R2 in Fig. 2–21 has to be removed.

The picture tube measurement returns results on every field for:

– cutoff R
– cutoff G
– cutoff B
– white drive R or G or B (sequentially)

Thus a cutoff control cycle for RGB requires one field only, while a complete white drive control cycle requires three fields. During cutoff and white drive measurement, the average beam current limiter function (see Section 2.2.5.) is switched off. The amplitude of the cutoff and white drive measurement lines can be programmed separately with IBRM and WDRM (see Fig. 2–22). The start line for the tube measurement (cutoff red) can be programmed via I^2C-bus (TML).

The built-in control loop for cutoff and white drive can operate in three different modes selected by CUT(WDR)_GAIN and CUT(WDR)_DIS.

– The user control mode is selected by setting CUT(WDR)_GAIN = 0. In this mode the registers CUT(WDR)_R/G/B are used as direct control values for cutoff and drive. If the measurement lines are enabled (CUT(WDR)_DIS = 0) the user can read the measured cutoff and white drive values in the CUTOFF(WDRIVE)_R/G/B registers. An external software can now control the settings of the CUT(WDR)_R/G/B registers.
– The automatic mode is selected by setting CUT(WDR)_GAIN > 0 and CUT(WDR)_DIS = 0. In this mode, the registers CUT(WDR)_R/G/B are used as reference for the measured values (CUTOFF(WDRIVE)_R/G/B). The calculated error is used with a small hysteresis (1.5%) to adjust cutoff and drive. The higher the loop gain (CUT(WDR)_GAIN) the smaller the time constant for the adjustment.
– If the automatic mode was once enabled (CUT(WDR)_GAIN > 0), the control loop can be stopped by setting CUT(WDR)_DIS = 1. In this mode the calculated cutoff and drive values will no longer be modified and the measurement lines are suppressed. Changes of the reference values (CUT(WDR)_R/G/B) have no effect.

If one of the calculated red, green, or blue white drive values exceeds its maximal possible value (WDR_R/G/B>511), the white balance becomes maladjusted. An automatic drive saturation avoidance prevents this effect (WDR_SAT = 1). If one drive value exceeds the maximum allowed threshold (MAX_WDR), the amplitude of the white drive measurement line will be increased, and decreased, if one of them goes below the fixed threshold of 475.

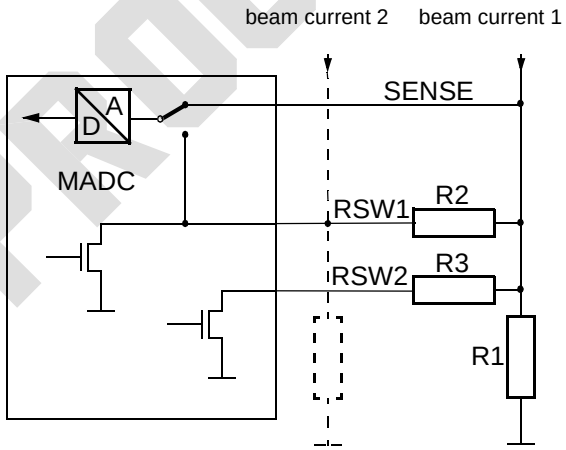


Fig. 2–21: MADC range switch

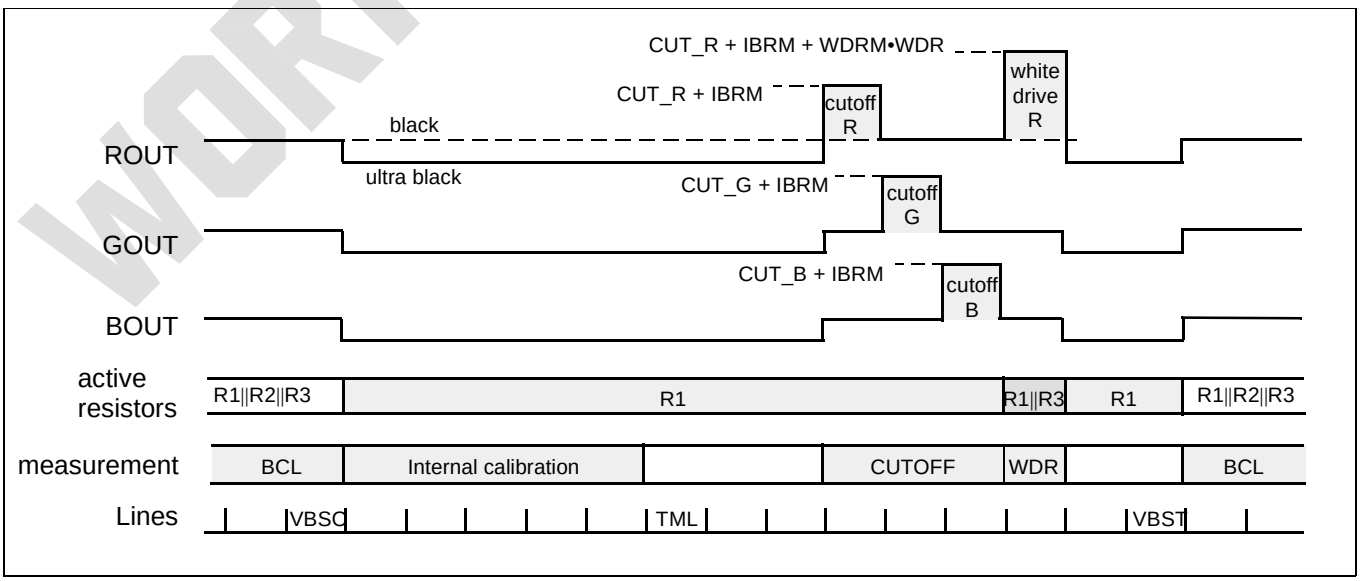


Fig. 2–22: MADC measurement timing

2.2.5. Average Beam Current Limiter

The average beam current limiter (BCL) works on both the digital YC_rC_b input and the inserted analog RGB signals by using either the sense input or the RSW1 input for the beam current measurement. The BCL uses a different filter to average the beam current during the active picture.

The beam current limiter allows the setting of a threshold current, a gain and an additional time constant. If the beam current is above the threshold, the excess current is low-pass filtered with the according gain and time constant. The result is used to attenuate the RGB outputs by adjusting the white drive multipliers for the internal (digital) RGB signals, and the analog contrast multipliers for the analog RGB inputs, respectively. The lower limit of the attenuator is programmable, thus a minimum contrast can always be set. If the minimum contrast is reached, the brightness will be decreased to a programmable minimum as well. Typical characteristics of the BCL for different loop gains are shown in Fig. 2–23; for this example the tube has been assumed to have square law characteristics.

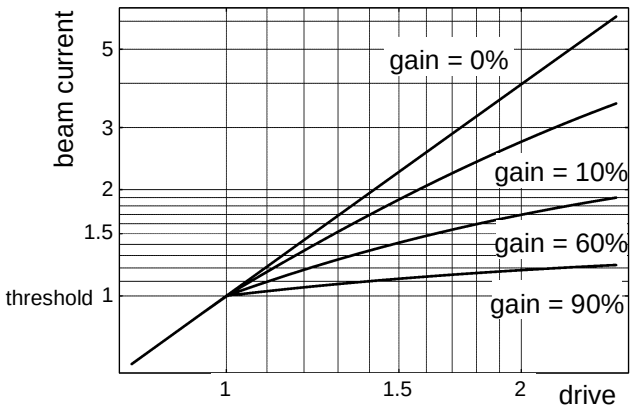


Fig. 2–23: Beam current limiter characteristics: beam current output vs. drive

2.3. Synchronization and Deflection

2.3.1. Line-Locked Clock Generator

The clock generation system derives all clocks from one 20.25 MHz crystal oscillator clock source. Line-locked horizontal sync pulses are generated by a digital phase-locked loop. The time constant can be adjusted between fast and slow behavior (***KPL, KIL***) to accommodate different input sources (e.g.: VCR). Noisy input signals become more stable when noise-reduction is enabled (***HSWIN***).

The PLL control can be frozen up to 15 lines before v-sync (***FION***) for a duration up to 15 lines (***FILE***). This may be used to reduce disturbances by h-phase errors which are produced by VCRs.

2.3.2. Output Data Controller (ODC)

The ODC generates internal horizontal and vertical synchronization signals and defines the position of the active video data.

The ODC supports three different modes:

– locked mode

– free-run mode

– auto free-run mode

In free-run mode, the backend part works stand alone without analyzing the input signal. Thus, input data part and output data part are not related to each other. In free-run mode, the output signals of the ODC are generated depending on I²C-bus settings.

In locked mode the video backend part works with a line locked clock. This means that the video frontend and the video backend depend on each other. The generation of the controlling signals depends on signals from the frontend. This mode is the default mode for standard TV applications.

Table 2–1: HOUT and VOUT generator configurations

Mode	HOUTFR	VOUTFR
“H and-V-locked” mode	0	0
“H-free-running/ V-locked” mode	1	0
“H-locked/ V-free-running” mode	0	1
“H and V-free-running” mode	1	1

When no or very weak signal is connected to the CVBS input, the ODC can be configured to automatically switch into free-running mode. This stabilizes the display which may contain OSD information, e.g. during channel-tune. The configuration can be effected by ***AUTOFRRN***.

During free-run mode the phase offset between the generated h/v sync signals and the input h/v sync signal is undefined. Thus a switch from free-run to locked mode would causes visible artifacts on the screen and inside the deflection circuitry. To prevent these disturbances the generated h/v syncs are synchronized to the input h/v syncs by modifying the horizontal line length (**PPLOFF**) and the number of lines per field (**LPFOPOFF**) until the h/v syncs are switched to locked mode. **NOSYNC** disables the synchronization circuit.

2.3.3. Output Sync Controller (OSC)

The OSC generates a HS and VS signal to support the insertion of external RGB signals (e.g. PIP). The polarity of the sync signals is programmable.

2.3.4. Deflection Processing

The deflection processing generates the signals for the horizontal and vertical drive (see Fig. 2–24) and comprises the following blocks:

– PLL3 adjusts the phase of the horizontal drive pulse and compensates for the delay of the horizontal output stage.

– The Soft-Start guarantees a progressive energy ramp-up of the horizontal power stage

– The vertical sync, sawtooth and East/West circuitry

2.3.5. Soft Start/Stop of Horizontal Drive

In order to increase the energy supply of the horizontal deflection stage smoothly, a soft start decreases the drive frequency from 27 kHz to 15.625 kHz within 85 ms. The high time stays constant at 32 µs. This means the duty factor decreases from 86% to 50% (see Fig. 2–26).

2.3.6. Vertical Synchronization

The number of lines per field can be adjusted by software (LPFD). This number is used to calculate the vertical raster. The deflection processor (DP) synchronizes only to a vertical sync within a programmable detection window (LPFD ± VSYNCWIN). If there is no vsync the DP runs with maximum allowed lines and if the vertical frequency is to high it runs with minimum allowed lines. The smaller the detection window the slower the DP gets synchronized to the incoming vertical sync. In case of an interlaced input signal it is possible to display both fields at the same raster position by setting R_MODE to 1 or 2.

An automatic field length adaptation can be selected (VA_MODE). In this case the vertical raster will be calculated according to the counted number of lines per field instead from LPFD. This is useful for video recorder search mode when the number of lines per field does not comply with the standard, or if a common value of LPFD for PAL and NTSC is desired (e.g.: LPFD = 290; VSYNCWIN = 54).

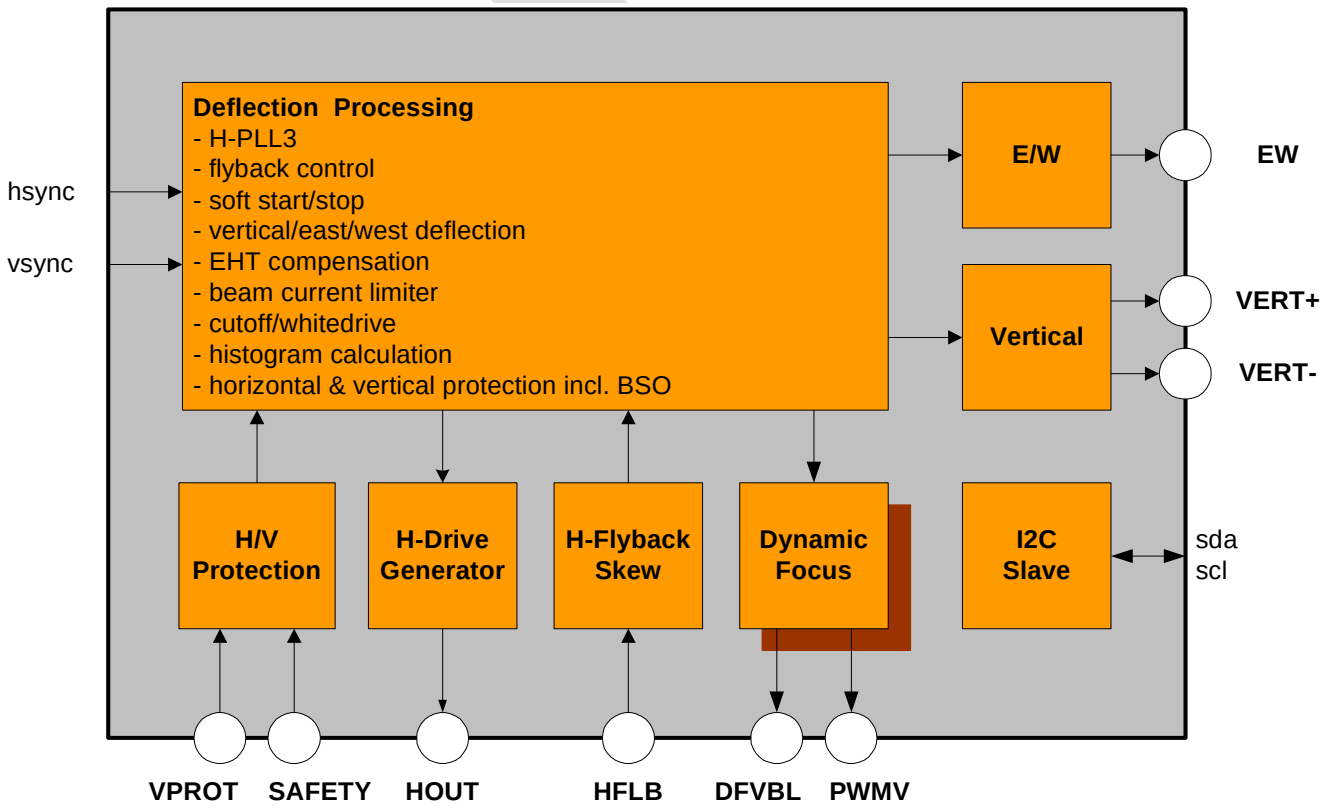


Fig. 2–24: Deflection Processing

2.3.7. Vertical and East/West Deflection

The calculations of the Vertical deflection and East/West correction waveforms are done in the DP. They are described as polynomials in x, where x varies from –0.5•zoom to +0.5•zoom for one field. For zoom>1, the range is limited between –0.5 and +0.5.

The vertical deflection waveform is calculated as follows (without EHT compensation):

$$V = vpos + ampl(x + lin(x^2 - offset) + scor \cdot x(x^2 - offset))$$

- VPOS defines the vertical raster position
- AMPL is the vertical raster amplitude (zoom ≥ 1)
- LIN is the linearity coefficient
- SCOR is the coefficient for S-correction
- OFFSET is an internal parameter

The vertical sawtooth signal will be generated from a differential current D/A converter and can drive a DC coupled power stage. In order to get a faster vertical retrace timing, the output current of the vertical D/A-converter can be increased during the retrace for a programmable number of lines (FLYBL). The range between the end of the flyback and the beginning of the raster is also programmable (HOLDL).

The East/West deflection waveform, generated from a single ended D/A converter, is given with the equation:

$$E/W = width + trapez \cdot x + cush \cdot x^2 + corner \cdot x^4$$

- WIDTH is a DC value for the picture width
- TRAPEZ is the trapezoidal correction
- CUSH is the pincushion correction
- CORNU is the upper corner correction
- CORNL is the lower corner correction

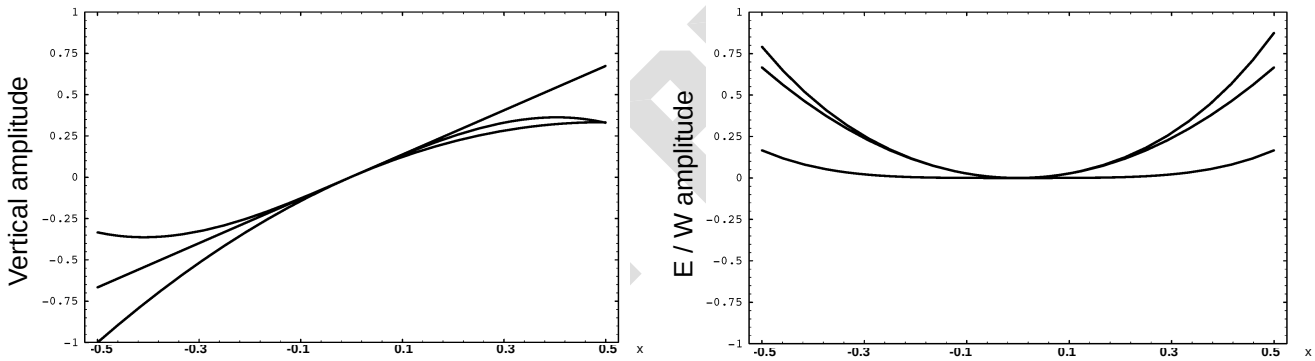


Fig. 2–25: Vertical and East/West deflection waveforms

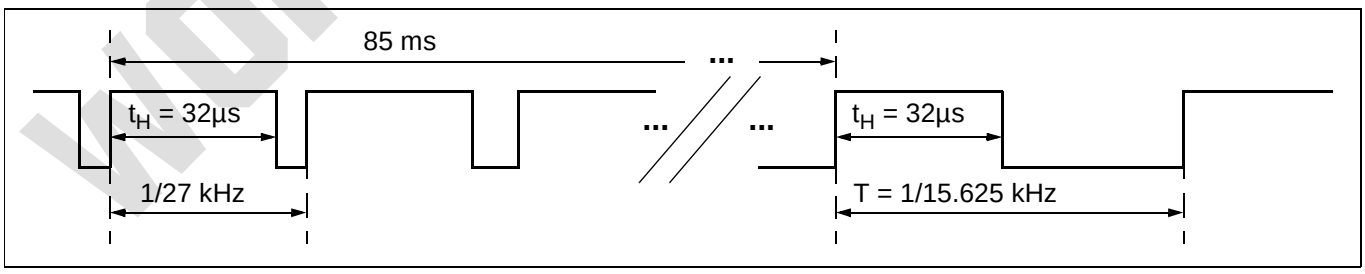


Fig. 2–26: Soft-start operation

2.3.8. Vertical Zoom

With vertical zoom it is possible to display different aspect ratios of the source signal on tubes with 4:3 or 16:9 aspect ratio by adapting the corresponding raster.

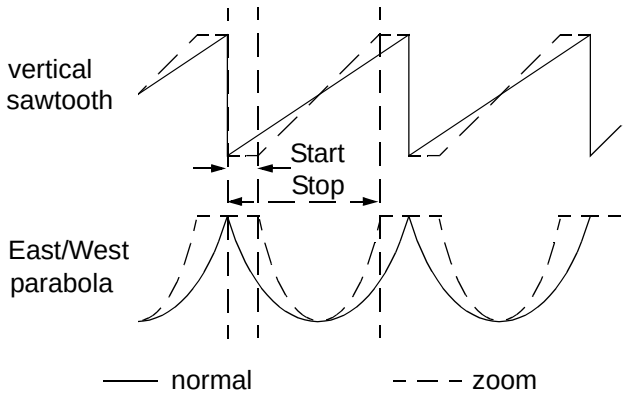


Fig. 2–27: Vertical zoom

2.3.9. EHT Compensation

The vertical deflection waveform can be scaled according the average beam current. This is used to compensate the effects of electric high tension changes due to beam current variations. EHT compensation for East/West deflection is done with an offset corresponding to the average beam current. The time constant of this process is free programmable with a resolution of 18 bit. Both corrections can be enabled separately. The maximum scaling coefficient for vertical deflection is 1±x and the maximum offset for East/West is y, where x, y are adjustable from 0 to 0.25. The horizontal phase at the output HOUT can be influenced according to the average beam current in a range of ±1.5 µs.

2.3.10. Protection Circuitry

Picture tube and drive stage protection is provided through the following measurements:

– Vertical protection input: this pin watches the vertical sawtooth signal. In every field the sawtooth must descend below the lower threshold A and ascend above the upper threshold B. In this case the protection flag is set (sawtooth o.k.). If an error occurs the protection flag is cleared.
After a programmable number of fields with cleared flag the RGB drive signals are blanked. The blanking is cancelled if the flag is set a programmable number of lines (see Fig. 2–28)

– Drive shutoff during flyback: this feature can be selected by software (EFLB)

– Safety input pin: this pin has two thresholds. The lower threshold A watches for a positive edge in every line, and the upper threshold B must not be overshoot, otherwise the RGB signals are blanked and a soft stop can be performed (HPROT_SS). Both thresholds have a small hysteresis.

2.3.11. General Purpose D/A Converter

There are two D/A converters using pulse width modulation. The resolution is 8 bit and the clock frequency is 20.25 MHz. The outputs are of the push-pull type. For a ripple-free output voltage a first order lowpass filter with a corner frequency < 120 Hz should be applied.

The D/A converters are adjusted via the I^2C bus. They can be used to generate two DC voltages, for example for horizontal raster position, raster tilt or just as switching outputs, when the values 0 and 255 are selected.

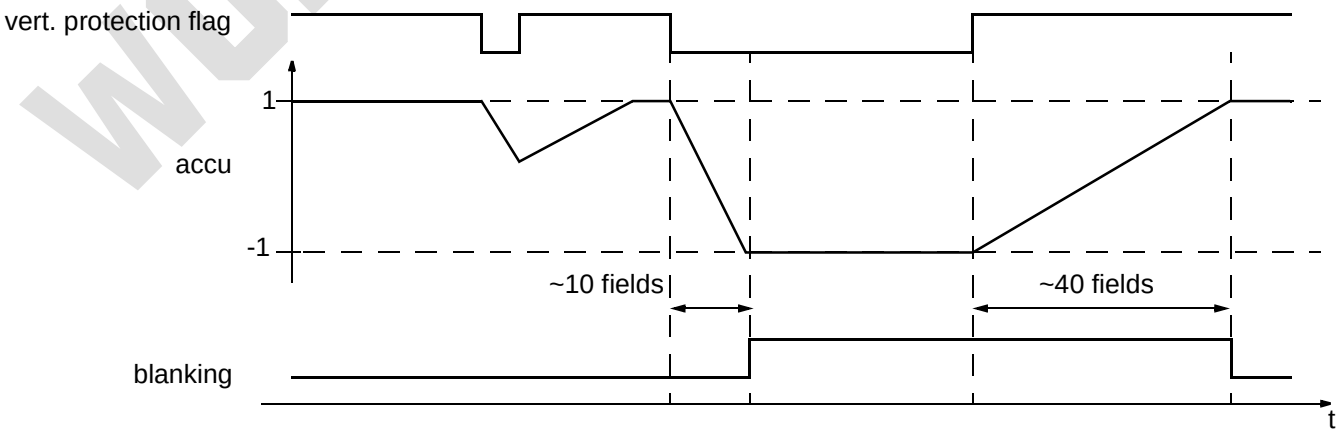


Fig. 2–28: Vertical protection timing

3. Control Interface

3.1. I²C Bus Interface

Communication between the DDP and the TVT (or external controller) is done via I²C bus. The I²C bus interface of the DDP acts as a slave receiver and as a slave transmitter. I²C clock synchronization is used to slow down the I²C bus if required. The interface supports the normal 100 kHz transmission as well as the high-speed 400 kHz transmission.

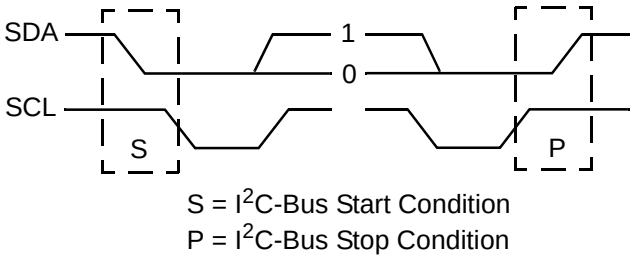


Fig. 3–1: I²C-Bus protocol (MSB first, data must be stable while clock is high)

The DDP is selected by transmitting the DDP device address. A device address pair is defined as a write address and a read address.

Table 3–1: I²C Bus Device Address

Mode	Write	Read
DDP device address	BC_{hex}	BD_{hex}

3.2. I²C Bus Format

Basically there are two classes of I²C registers in the DDP. The first class are directly addressable **I²C Register**. They are embedded in the hardware. These registers are 16 bits wide and support read/write operation.

The second class are **XDFP-Register**, which are part of the on-chip risc processor named “XDFP”. These registers are 16 bits wide and support read/write operation. Communication with these registers requires I²C telegrams with a 16 bit register subaddress and 16 bit register data.

The I²C bus interface uses one level of subaddress. First the device address selects the DDP, then a subaddress selects one of the internal registers. They have 16-bit data size. All 16-bit registers are accessed by reading/writing two 8-bit data words. Writing is done by sending the device address first followed by the subaddress byte and two data bytes. For reading, the read address has to be transmitted first by sending the device write address followed by the subaddress a second start condition with the device read address and reading two bytes of data. Fig. 3–2 shows the I²C register protocol for read and write operations. The read operation requires an extra start condition and repetition of the device address with read bit set.

All modes run with a subaddress auto increment, i.e. if more than 2 bytes of data are transmitted the subaddress is internally incremented every 2 bytes. However, the auto-increment function can be disabled by the control bit ***AUTOINC*** in the VSP. If the auto-increment function is switched off, any number of 2 byte data transmissions will be written into the same subaddress. Read-only registers with polling functions have no auto-increment function.

Write to I²C control register :

S	BC_{hex}	Ack	subaddr.	Ack	highbyte data	Ack	lowbyte data	Ack	P

Read from I²C control register :

S	BC_{hex}	Ack	subaddr.	Ack	S	BD_{hex}	Ack	highbyte data	AM	lowbyte data	Nak	P

Ack = 0 (acknowledge bit from slave)
AM = 0 (acknowledge bit from master)
Nak = 1 (not acknowledge bit from master)

slave active

Fig. 3–2: I²C register protocol

3.3. I²C Register Types

The following register types are defined in the detailed I²C register description (see Table 3–6 on page 5-29):

Table 3–2: I²C register types

Register Types	Dir
readable write register	RW
write only register	W
read only register	R
reset after read register	R

3.4. I²C Register Domains

The I²C registers are located in different functional domains (see Table 3–3). Every domain has an independent update mechanism controlled by a set of update registers (see **I2C** on page 5-38).

Table 3–3: I²C register domains

Functional Block	Domain	Sync
Display processing	DP	VS_DP
Deflection processing	DEFL	VS_DEFL
Output data control	ODC	VS_ODC

Wether a vertical update has occurred inside a domain can be checked by software by reading the status registers **VS_DP_STAT**, **VS_DEFL_STAT** and **VS_ODC_STAT**. These bits are set with the internal vertical sync and automatically reset after read.

3.5. Update of I²C Write Registers

I²C write registers change the behavior of internal hardware. It is often required to synchronize these changes so that they cause no visible artifacts on the screen.

The take-over from the I²C-bus telegram into the register can be either disabled or immediate or synchronized with an internal vertical sync signal. This is controlled by the I²C register bits **VS_DP**, **VS_DEFL** and **VS_ODC** for vertical update and **IM_DP**, **IM_DEFL** and **IM_ODC** for immediate update.

Registers without sync information in the I²C register description (see Table 3–6 on page 5-29) have immediate take-over.

3.6. Update of I²C Read Registers

I²C read registers reflect the status of internal hardware. The take-over from hardware into the I²C register can be immediate or synchronized with an internal vertical sync signal. This is indicated by the sync information in the I²C register description (see Table 3–6 on page 5-29). Registers without sync information have immediate take-over.

Some I²C read registers have a special update mechanism to allow detection of fast and single events. These registers behave like a RS flip-flop and are therefore called “RS type” registers. Whenever the corresponding signal has a high level, it sets the register to “1”. After being read via I²C bus, the register will automatically be reset to “0”. These registers have an extra note in the I²C register description (see Table 3–6 on page 5-29).

3.7. XDFP Control and Status Registers

Access to XDFP registers is achieved by subaddressing (see **XDFP** on page 5-37). The XDFP subaddress registers are part of the DDP deflection domain and use immediate take-over.

Writing to the XDFP registers is done by sending the device write address first, followed by the subaddress “XDFP RAM Write Address” and two address bytes **XDFPWRA[15:0]** for the desired XDFP-register. The two data bytes are send in a second telegram starting with the device write address, followed by the subaddress “XDFP RAM Write Data” and two data bytes **XDFPWRD[15:0]**. For reading, the XDFP-register address has to be transmitted first by sending the device write address, followed by the subaddress “XDFP RAM Read Address” and two address bytes **XDFPRDA[15:0]** for the desired XDFP-register. Reading of the addressed data is done by sending a second telegram with the device read address and the subaddress “XDFP RAM Read Data” and then reading two data bytes **XDFPRDD[15:0]**. Fig. 3–3 shows the I2C protocol for read and write operations.

Table 3–4: XDFP read/write address

XDFP RAM Write Address	$F0_{hex}$
XDFP RAM Read Address	$F1_{hex}$
XDFP RAM Write Data	$F2_{hex}$
XDFP RAM Read Data	$F3_{hex}$
XDFP Status	$F4_{hex}$

Due to the internal architecture, the DDP cannot react immediately to an I^2C requests, which interacts with XDFP registers. The maximum response timing is approximately 20 ms. If the addressed register is not ready for further transmissions on the I^2C bus, the clock line SCL is pulled low. This puts the current transmission into a wait state. After a certain period of time the clock line will be released and the interrupted transmission is carried on. To avoid I^2C bus blocking the software can check the **XDFPBUSY** bit before sending new telegrams to the XDFP.

A hardware reset initializes all control registers to 0. The embedded XDFP firmware loads a selected set of registers with the default values.

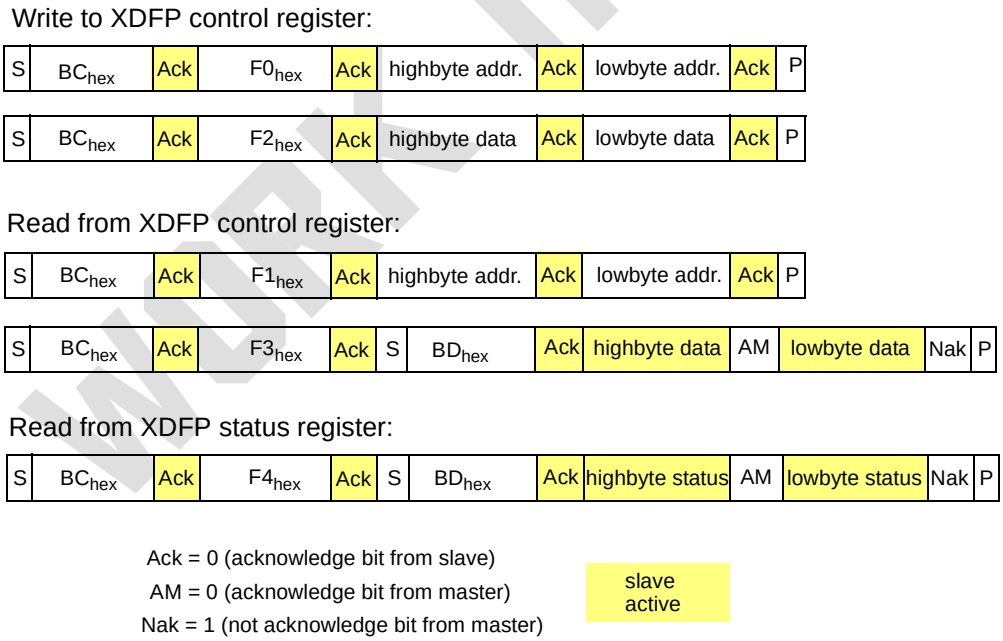


Fig. 3–3: XDFP register protocol

3.8. I²C Register Block Index

3.9. I²C Register Index

3.10. I²C Register Subaddress Index

Table 3–5: I2C Subaddress Index

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h00																	h8000
h01																	h0000
h02																	h0510
h03	KOIWID[1:0]		KOIH[1:0]		LIMEN	HRES		FMOD	HSWIN[3:0]					LNL	DISRES	LIMHI	h6030
h04	LIMII[7:0]								LIMIP[7:0]								hFFFF
h05	FION[3:0]				FILE[3:0]							KIL[4:0]					h0004
h06		KPNL[4:0]					KPL[4:0]					KINL[4:0]					h14A4
h07					FKOI	FKOIHYS		SLLWIN[1:0]				FRZLIMLR	LIMLR[3:0]				h0001
h08																	h0000
h09																STABLL	
h16								LPFOP[8:0]									h009C
h17																	h0510
h18								NAPPLOP[8:0]									h0000
h1A						HORPOS[10:0]											h00BE
h1B						HORWIDTH[10:0]											h0438
h1C							VERPOS[9:0]										h0001
h1D						VERWIDTH[10:0]											h0139
h1E							HOUTDEL[9:0]										h0116
h1F	VAUTOFRRN	HAUTOFRRN				VOUTFR	HOUTFR										h0000
h20						FHPUL-LIN	SHPUL-LIN	PPLOFF[4:0]					LPFOPOFF[3:0]				h138F
h28											CSYEN[1:0]			HOUT-POL	VOUT-POL		h0000
h29																	h0000
h2A																	h0000
h2B																	h0000
h2C																	h0000
h32																	h0001
h33	YHIGH[7:0]									DEMO-MODE	ON	YLOW[4:0]					hFF10
h34	WHITE_TH[7:0]											BLACK_TH[4:0]					hF010

Table 3–5: I2C Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h35	WHITE_LEVEL_L[7:0]								BLACK_LEVEL_L[7:0]								h0101
h36	WHITE_LEVEL_U[7:0]								BLACK_LEVEL_U[7:0]								h0808
h37	AUP_UL[7:0]								ALP_UL[7:0]								hC0C0
h38																	h0225
h39																	h0000
h3A														YDELMATCH[2:0]			h0000
h3C	BLE-FORCE	SBLE[2:0]			TILT[3:0]				BLEGAIN[1:0]			FRAME	DEMO	BRF[2:0]			hB743
h3D	BLEMODE[1:0]																h881C
h3E					VCROP[3:0]				HCROP[3:0]								h7228
h40								SCE-TOG	BSTGAIN[1:0]		GSTGAIN[1:0]		STCGAIN[1:0]		STCANG[1:0]		h0001
h41	BSTYS[3:0]				GSTYE[3:0]				GSTYS[3:0]				STCYS[3:0]				h3F1A
h42									BSTYG[1:0]		GSTYR[1:0]		GSTYG[1:0]		STCYG[1:0]		h0095
h43																	h5654
h44																	h0000
h46								LTIGAIN2	LTIEN	LTICOR[2:0]			LTIGAIN[3:0]				h009F
h47										LMIXGAIN[1:0]		LMIXOFS[4:0]					h4066
h48	PKPOS[3:0]				PKNEG[3:0]							PKCOR[4:0]					h4406
h49														PKCF[1:0]			h0008
h4A							CTIBW	CTILP	CTIGAIN[3:0]				CTICOR[3:0]				h02A1
h50	WINDVSP[1:0]		WIND-VST	WIND-VDR	WIND-VON	HORPOSP[10:0]											h00C8
h51	WINDHSP[1:0]		WINDHST	WINDHDR	WIND-HON	HORWIDTHP[10:0]											h0438
h52							VERPOSP[9:0]										h0001
h53							VERWIDTHP[9:0]										h0139
h54					VCUR[3:0]				UCUR[3:0]				YCUR[3:0]				h0001
h55	YBAGR2[3:0]				VBAGR[3:0]				UBAGR[3:0]				YBAGR[3:0]				h2001
h56					VFRAMEM[3:0]				UFRAMEM[3:0]				YFRAMEM[3:0]				h0001
h57																	h0001
h58						HORPOSG[10:0]											h00C8
h59						HORWIDTHG[10:0]											h0000
h5A	HORFRAMEG[4:0]						VERPOSG[9:0]										h0001
h5B	VERFRAMEG[4:0]						VERWIDTHG[9:0]										h0000
h5C																	h00C8

Table 3–5: I2C Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
h5D																	h0000
h5E																	h0001
h5F																	h0000
h60	PATT-DIS-CHROMA	PATTIN-VERSE						PATTMODE[2:0]						FRA-MEDIMM			h1811
h61		PRIOF[2:0]			PRIOS[2:0]			PRIOG[2:0]			PRIOM[2:0]			PRIOC[2:0]			h3977
h62														PRIOP[2:0]			h0002
h64							MR1M[9:0]										h0000
h65							MR2M[9:0]										h0056
h66							MG1M[9:0]										h03EA
h67							MG2M[9:0]										h03D4
h68							MB1M[9:0]										h0071
h69							MB2M[9:0]										h0000
h6A																	h0000
h6B			TINT[5:0]								SAT[5:0]						h0020
h6C		CONTR[5:0]						BRIGH[8:0]									h4000
h78				SVCORR[3:0]				SVGAIN[5:0]						SVDIFF[2:0]			h0101
h79							SVDEL[3:0]				SVLIM[5:0]						h023F
h82																STAND-BYDAC	h0000
hD2	SAFET-YMODE	OSDSYNCMODE	FIELDEN	HOUT-STR					HPROTLIM[7:0]								h06C0
hF0	XDFPWRA[15:0]																h0000
hF1	XDFPRDA[15:0]																h0000
hF2	XDFPWRD[15:0]																h0000
hF3	XDFPRDD[15:0]																
hF4														XDF-PRD-BUSY	XDFP-WRBUSY	XDFP-BUSY	
hF5																	h0000
hFD													VS_DEFL_STAT	VS_ITUO_STAT	VS_ODC_STAT	VS_DP_STAT	
hFE													IM_DEFL	IM_ITUO	IM_ODC	IM_DP	h0000
hFF													VS_DEFL	VS_ITUO	VS_ODC	VS_DP	h000F

3.11. I²C Register Description

Note: For compatibility reasons every undefined bit in a writeable register should be set to “0”. Undefined bits in a readable register should be treated as “don’t care”!

Table 3–6: I2C Register Description

Name	Sub	Dir	Sync	Reset	Range	Function
LLPLL						
KOIWID[1:0]	h03[15:14]	RW		1	0,1,2,3	**Coincidence Detector Window** 00: +/- 32 pixel (+/- 0.79µs for TV application) 01: +/- 64 pixel (+/- 1.58µs for TV application) 10: +/-128 pixel (+/- 3.16µs for TV application) 11: +/-256 pixel (+/- 6.32µs for TV application)
KOIH[1:0]	h03[13:12]	RW		2	0,1,2,3	**Coincidence Detector Hysteresis** 00: 0 lines 01: 8 lines 10: 16 lines 11: 32 lines
LIMEN	h03[11]	RW		0	0,1	**Limitation of LIMIP and LIMII** 0: limip*1, limii*16 1: limip*16, limii*256
HRES	h03[10]	RW		0	0,1	**LLPLL Reset** triggers controlled reset of LLPLL 0: no reset triggered 1: reset triggered Attention: Bit is set by software and reset by hardware.
FMOD	h03[8]	RW		0	0,1	**Freerun Mode** 0: freerunning clocks derived from crystal 1: freerunning clocks derived from HDTO
HSWIN[3:0]	h03[7:4]	RW		3	0..15	**Horizontal Sync Window** Values given in µs are valid for IICINCR=262144 0000: +/-28µs 0001: +/-24µs 0010: +/-20µs 0011: +/-16µs 0100: +/-12µs 0101: +/-8µs 0110: +/-4µs 0111: dynamic windowing 1000: +/-30µs 1001: +/-27µs 1010: +/-26µs 1011: +/-22µs 1100: +/-18µs 1101: +/-14µs 1110: +/-10µs 1111: +/-6µs **dynamic windowing:** The window starts with +/- 32µs and is reduced each time a H-sync appeared inside the window (+/- 28µs; +/- 24µs; +/- 20µs; +/- 16µs; +/- 12µs; +/- 8µs; +/- 4µs;). If there is no H-sync inside the window it is increased by one step. Note: If PPLIP<1076d only "0101" or "0110" are allowed
LNL	h03[2]	RW		0	0,1	**Linear or Non-Linear Mode** dynamic time constant control 0: linear mode 1: non linear mode
DISRES	h03[1]	RW		0	0,1	**Disable Reset of LLPLL Watchdog** 0: reset disable 1: reset enable
LIMHI	h03[0]	RW		0	0,1	**Limit HDTO Increment** 0: 2047 < HINCR < 524288 1: 2047 < HINCR < 393216

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
LIMII[7:0]	h04[15:8]	RW		255	0..255	**Limiter Control for Integral Loop Filter** LIMIT_I = +/- 16*LIMII 0: +/-0 1: +/-16 2: +/-32 ... 254: +/-4064 255: no limitation
LIMIP[7:0]	h04[7:0]	RW		255	0..255	**Limiter Control for Proportional Loop Filter** LIMIT_P= +/- 16*LIMIP 0: +/-0 1: +/-16 2: +/-32 ... 254: +/-4064 255: no limitation
FION[3:0]	h05[15:12]	RW		0	0..15	**Freeze Increment Start** 0: no freeze 15: freeze starts 15 lines before V-sync
FILE[3:0]	h05[11:8]	RW		0	0..15	**Freeze Increment Length** 0: no freeze 15: increment is frozen for 15 lines
KIL[4:0]	h05[4:0]	RW		4	0..31	**Integral Coefficient Locked** coefficient for loop filter if LLPLL is locked (KOI_HYS=1) 00000: 0 00001: 1 00010: 2 00011: 4 00100: 8 00101: 16 00110: 32 00111: 64 01000: 128 01001: 256 01010: 512 01011: 1024 01100: 2048 01101: 4096 01110: 8192 01111: 16384 10000: 0.5 10001: 1.5 10010: 2.5 10011: 3 10100: 3.5 10101: 4.5 10110: 5 10111: 6 11000: 7

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
KPNL[4:0]	h06[14:10]	RW		5	0..31	**Proportional Coefficient Not Locked** coefficient for loop filter if LLPLL is not locked (KOI_HYS=0) 00000: 0 00001: 1 00010: 2 00011: 4 00100: 8 00101: 16 00110: 32 00111: 64 01000: 128 01001: 256 01010: 512 01011: 1024 01100: 2048 01101: 4096 01110: 8192 01111: 16384 10000: 0.5 10001: 1.5 10010: 2.5 10011: 3 10100: 3.5 10101: 4.5 10110: 5 10111: 6 11000: 7
KPL[4:0]	h06[9:5]	RW		5	0..31	**Proportional Coefficient Locked** coefficient for loop filter if LLPLL is locked (KOI_HYS=1) 00000: 0 00001: 1 00010: 2 00011: 4 00100: 8 00101: 16 00110: 32 00111: 64 01000: 128 01001: 256 01010: 512 01011: 1024 01100: 2048 01101: 4096 01110: 8192 01111: 16384 10000: 0.5 10001: 1.5 10010: 2.5 10011: 3 10100: 3.5 10101: 4.5 10110: 5 10111: 6 11000: 7

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
KINL[4:0]	h06[4:0]	RW		4	0..31	**Integral Coefficient Not Locked** coefficient for loop filter if LLPLL is not locked (KOI_HYS=0) 00000: 0 00001: 1 00010: 2 00011: 4 00100: 8 00101: 16 00110: 32 00111: 64 01000: 128 01001: 256 01010: 512 01011: 1024 01100: 2048 01101: 4096 01110: 8192 01111: 16384 10000: 0.5 10001: 1.5 10010: 2.5 10011: 3 10100: 3.5 10101: 4.5 10110: 5 10111: 6 11000: 7
FKOI	h07[11]	RW		0	0,1	**Force Coincidence Bit** 0: coincidence bit dynamically changed 1: coincidence bit forced to 1
FKOIHYS	h07[10]	RW		0	0,1	**Force Coincidence Hysteresis Bit** 0: coincidence hysteresis bit dynamically changed 1: coincidence hysteresis bit forced to 1
SLLWIN[1:0]	h07[8:7]	RW		0	0..3	**STABLL Detection Window** 00: 64 01: 72 10: 48 11: 32
FRZLIMLR	h07[4]	RW		0	0,1	**Freeze LIMLR** 0: use LIMLR 1: freeze LIMLR=4
LIMLR[3:0]	h07[3:0]	RW		1	0..15	**Limit Lock-in Range** 0000: full lock-in range of +/- 5.85% 0001: lock in range limited to +/- 3.8% 0010: lock in range limited to +/- 2.55% 0011: lock in range limited to +/- 1.27% 0100: lock in range limited to +/- 0.63% 0101: lock in range limited to +/- 0.32% 0110: lock in range limited to +/- 0.19% 0111: lock in range limited to +/- 0.13% 1000: lock in range limited to +/- 5% 1001: lock in range limited to +/- 4.5% 1010: lock in range limited to +/- 3.1% 1011: lock in range limited to +/- 2.1% 1100: lock in range limited to +/- 1.5% 1101: lock in range limited to +/- 1% 1110: (reserved) 1111: (reserved)
STABLL	h09[0]	R			0,1	**LLPLL Lock Status** 0: not locked 1: locked
ODC						
LPFOP[8:0]	h16[8:0]	RW	VS_ODC	156	0..511	**Lines Per Field Output** Only used for freerun mode Granularity: 2 lines
NAPPLOP[8:0]	h18[8:0]	RW	VS_ODC	0	0..511	**Not Active Pixel Per Line Output** Granularity: 4pixel
HORPOS[10:0]	h1A[10:0]	RW	VS_ODC	190	32..2047	**Horizontal Picture Position**

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
HORWIDTH[10:0]	h1B[10:0]	RW	VS_ODC	1080	0..2047	**Horizontal Picture Width**
VERPOS[9:0]	h1C[9:0]	RW	VS_ODC	1	0..1023	**Vertical Picture Position**
VERWIDTH[10:0]	h1D[10:0]	RW	VS_ODC	313	0..2047	**Vertical Picture Width**
HOUTDEL[9:0]	h1E[9:0]	RW	VS_ODC	278	0..322	**HSync Output Delay** Granularity: 4 pixel
VAUTOFRRN	h1F[15]	RW	VS_ODC	0	0,1	**Vertical Automatic Freerun Mode** 0: freerun depends on VOUTFR 1: automatic freerun
HAUTOFRRN	h1F[14]	RW	VS_ODC	0	0,1	**Horizontal Automatic Freerun Mode** 0: freerun depends on HOUTFR 1: automatic freerun
VOUTFR	h1F[10]	RW	VS_ODC	0	0,1	**Vertical Freerun** 0: locked mode 1: freerun mode
HOUTFR	h1F[9]	RW	VS_ODC	0	0,1	**Horizontal Freerun** 0: locked mode 1: freerun mode
FHPULLIN	h20[10]	RW	VS_ODC	0	0,1	**Force Horizontal Pull-In** 0: horizontal pull-in depends on STABLL 1: force horizontal pull-in
SHPULLIN	h20[9]	RW	VS_ODC	1	0,1	**Single Horizontal Pull-In** 0: horizontal pull-in during vertical window 1: single horizontal pull-in until locked
PPLOFF[4:0]	h20[8:4]	RW	VS_ODC	24	0..31	**Pixel Per Line Offset** used when switching from horizontal freerun mode to locked mode
LPFOPOFF[3:0]	h20[3:0]	RW	VS_ODC	15	0..15	**Lines Per Field Offset** used when switching from vertical freerun mode to locked mode Granularity: 2 lines
OSC						
CSYEN[1:0]	h28[5:4]	RW	VS_ODC	0	0,1,2,3	**Composite Sync Enable** sync output available via port mux (see PMUX) or safety pin (see SAFETYMODE) 00: horizontal sync output 01: composite sync output 10: vertical sync output 11: inverted composite sync output
HOUTPOL	h28[2]	RW	VS_ODC	0	0,1	**HOUT Polarity** 0: low active 1: high active
VOUTPOL	h28[1]	RW	VS_ODC	0	0,1	**VOUT Polarity** 0: low active 1: high active
VIF						
DCI						
YHIGH[7:0]	h33[15:8]	RW	VS_DP	255	0..255	**Maximum Luminance Output**
DEMOMODE	h33[6]	RW	VS_DP	0	0,1	**Demo Mode** 0: normal mode 1: demo mode
ON	h33[5]	RW	VS_DP	0	0,1	**Dynamic Contrast Improvement** 0: off 1: on
YLOW[4:0]	h33[4:0]	RW	VS_DP	16	0..31	**Minimum Luminance Output**
WHITE_TH[7:0]	h34[15:8]	RW	VS_DP	240	0..255	**White Detection Threshold**
BLACK_TH[4:0]	h34[4:0]	RW	VS_DP	16	0..31	**Black Detection Threshold**
WHITE_LEVEL_L[7:0]	h35[15:8]	RW	VS_DP	1	0..255	**Lower White Level Threshold**
BLACK_LEVEL_L[7:0]	h35[7:0]	RW	VS_DP	1	0..255	**Lower Black Level Threshold**
WHITE_LEVEL_U[7:0]	h36[15:8]	RW	VS_DP	8	0..255	**Upper White Level Threshold**

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
BLACK_LEVEL_U[7:0]	h36[7:0]	RW	VS_DP	8	0..255	**Upper Black Level Threshold**
AUP_UL[7:0]	h37[15:8]	RW	VS_DP	192	0..255	**Limit Amplification Upper Part**
ALP_UL[7:0]	h37[7:0]	RW	VS_DP	192	0..255	**Limit Amplification Lower Part**
LUMAMATCH						
YDELMATCH[2:0]	h3A[2:0]	RW	VS_DP	0	-4..3	**Luma Chroma Delay Match**
BLE						
BLEFORCE	h3C[15]	RW	VS_DP	1	0,1	**Force BLE** disable activity measurement
SBLE[2:0]	h3C[14:12]	RW	VS_DP	3	0..7	**Static BLE Point** SBLE defines the fix minimum value in the static BLE mode. value = (SBLE + 1) * 32
TILT[3:0]	h3C[11:8]	RW	VS_DP	7	0..15	**Tilt Point** Above this point no expansion is performed. value = (TILT + 1) * 32
BLEGAIN[1:0]	h3C[7:6]	RW	VS_DP	1	0..3	**Gain of Expansion** BLEGAIN defines how much the signal at the measured MIN value or programmed SBLE value is stretched to black. It also defines the subblack slope. 00: max. expansion ... 11: min. expansion
FRAME	h3C[4]	RW	VS_DP	0	0,1	**Display Measurement Window** 0: window hidden 1: window visible
DEMO	h3C[3]	RW	VS_DP	0	0,1	**BLE Demo Mode** 0: normal mode 1: demo mode
BRF[2:0]	h3C[2:0]	RW	VS_DP	3	0..7	**Blacklevel Reference** BLE reference level for black level = BRF * 8
BLEMODE[1:0]	h3D[15:14]	RW	VS_DP	2	0..3	**BLE Mode** 0: BLE bypass 1: autocontrast mode 2: dynamic BLE mode 3: static BLE mode
VCROP[3:0]	h3E[11:8]	RW	VS_DP	2	0..15	**Vertical Crop Value** defines number of dropped lines for minimum measurement window value = VCROP * 16
HCROP[3:0]	h3E[7:4]	RW	VS_DP	2	0..15	**Horizontal Crop Value** defines number of dropped pixel for minimum measurement window value = HCROP * 8
SCE						
SCETOG	h40[8]	RW	VS_DP	0	0,1	**Enable SCE Toggle Mode** 0: disable 1: enable
BSTGAIN[1:0]	h40[7:6]	RW	VS_DP	0	0..3	**BST Gain**
GSTGAIN[1:0]	h40[5:4]	RW	VS_DP	0	0..3	**GST Gain**
STCGAIN[1:0]	h40[3:2]	RW	VS_DP	0	0..3	**STC Gain**
STCANG[1:0]	h40[1:0]	RW	VS_DP	1	0..3	**Target Skintone**
BSTYS[3:0]	h41[15:12]	RW	VS_DP	3	0..15	**BST Y Start Border**
GSTYE[3:0]	h41[11:8]	RW	VS_DP	15	0..15	**GST Y End Border**
GSTYS[3:0]	h41[7:4]	RW	VS_DP	1	0..15	**GST Y Start Border**
STCYS[3:0]	h41[3:0]	RW	VS_DP	10	0..15	**STC Y Start Border**
BSTYG[1:0]	h42[7:6]	RW	VS_DP	2	0..3	**BST Y Start Gain**
GSTYR[1:0]	h42[5:4]	RW	VS_DP	1	0..3	**GST Y Stop Gain**
GSTYG[1:0]	h42[3:2]	RW	VS_DP	1	0..3	**GST Y Start Gain**
STCYG[1:0]	h42[1:0]	RW	VS_DP	1	0..3	**STC Y Start Gain**

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
LTI						
LTIGAIN2	h46[8]	RW	VS_DP	0	0,1	**LTI Gain Doubling** 0: normal gain 1: double gain
LTIEN	h46[7]	RW	VS_DP	1	0,1	**LTI Enable** 0: disable 1: enable
LTICOR[2:0]	h46[6:4]	RW	VS_DP	1	0..7	**LTI Coring**
LTIGAIN[3:0]	h46[3:0]	RW	VS_DP	15	0..15	**LTI Gain**
LUMAMIX						
LMIXGAIN[1:0]	h47[6:5]	RW	VS_DP	3	0,1,2,3	**Mixing Coefficient Gain** velocity of adaptive mixing 0: fast ... 3: slow
LMIXOFS[4:0]	h47[4:0]	RW	VS_DP	6	0..31	**Mixing Coefficient Offset** amplitude offset to start adaptive mixing 0: no offset ... 31: max. offset
PEAKING						
PKPOS[3:0]	h48[15:12]	RW	VS_DP	4	0..15	**Positive Peaking Level**
PKNEG[3:0]	h48[11:8]	RW	VS_DP	4	0..15	**Negative Peaking Level**
PKCOR[4:0]	h48[4:0]	RW	VS_DP	6	0..31	**Peaking Coring**
PKCF[1:0]	h49[2:1]	RW	VS_DP	0	0,1,2,3	**Peaking Filter Center Frequency** 0: 3.2MHz 1: 2.5MHz 2: 10MHz 3: 5MHz
CTI						
CTIBW	h4A[9]	RW	VS_DP	1	0,1	**CTI Bandwith** 0: narrow 1: wide
CTILP	h4A[8]	RW	VS_DP	0	0,1	**CTI Lowpass Filter** 0: disable 1: enable
CTIGAIN[3:0]	h4A[7:4]	RW	VS_DP	10	0..15	**CTI Gain**
CTICOR[3:0]	h4A[3:0]	RW	VS_DP	1	0..15	**CTI Coring**
PIXMIX						
WINDVSP[1:0]	h50[15:14]	RW	VS_DP	0	0,1,2,3	**Vertical Windowing Speed** 00: slow 01: medium 10: fast 11: very fast
WINDVST	h50[13]	RW	VS_DP	0	0,1	**Vertical Windowing Start** 0: no windowing 1: start windowing
WINDVDR	h50[12]	RW	VS_DP	0	0,1	**Vertical Windowing Direction** 0: open the vertical window 1: close the vertical window
WINDVON	h50[11]	RW	VS_DP	0	0,1	**Vertical Windowing Enable** 0: off 1: on
HORPOSP[10:0]	h50[10:0]	RW	VS_DP	200	0..2047	**Horizontal Position Background**
WINDHSP[1:0]	h51[15:14]	RW	VS_DP	0	0,1,2,3	**Horizontal Windowing Speed** 00: slow 01: medium 10: fast 11: very fast
WINDHST	h51[13]	RW	VS_DP	0	0,1	**Horizontal Windowing Start** 0: no windowing 1: start windowing

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
WINDHDR	h51[12]	RW	VS_DP	0	0,1	**Horizontal Windowing Direction** 0: open the horizontal window 1: close the horizontal window
WINDHON	h51[11]	RW	VS_DP	0	0,1	**Horizontal Windowing Enable** 0: off 1: on
HORWIDTHP[10:0]	h51[10:0]	RW	VS_DP	1080	0..2047	**Horizontal Width Background**
VERPOSP[9:0]	h52[9:0]	RW	VS_DP	1	0..1023	**Vertical Start Position of Background**
VERWIDTHP[9:0]	h53[9:0]	RW	VS_DP	313	0..1023	**Vertical Width Background**
VCUR[3:0]	h54[11:8]	RW	VS_DP	0	-8..7	**V Value Curtain** v chroma = VCUR*32
UCUR[3:0]	h54[7:4]	RW	VS_DP	0	-8..7	**U Value Curtain** u chroma = UCUR*32
YCUR[3:0]	h54[3:0]	RW	VS_DP	1	0..15	**Y Value Curtain** luma = YCUR*32
YBAGR2[3:0]	h55[15:12]	RW	VS_DP	2	0..15	**Y Value Background 2** luma = YBAGR2*32
VBAGR[3:0]	h55[11:8]	RW	VS_DP	0	-8..7	**V Value Background** v chroma = VBAGR*32
UBAGR[3:0]	h55[7:4]	RW	VS_DP	0	-8..7	**U Value Background** u chroma = UBAGR*32
YBAGR[3:0]	h55[3:0]	RW	VS_DP	1	0..15	**Y Value Background** luma = YBAGR*32
VFRAMEM[3:0]	h56[11:8]	RW	VS_DP	0	-8..7	**V Value Frame** v chroma = VFRAMEM*32
UFRAMEM[3:0]	h56[7:4]	RW	VS_DP	0	-8..7	**U Value Frame** u chroma = UFRAMEM*32
YFRAMEM[3:0]	h56[3:0]	RW	VS_DP	1	0..15	**Y Value Frame** luma = YFRAMEM*32
HORPOSG[10:0]	h58[10:0]	RW	VS_DP	200	0..2047	**Horizontal Position Frame**
HORWIDTHG[10:0]	h59[10:0]	RW	VS_DP	0	0..2047	**Horizontal Width Frame**
HORFRAMEG[4:0]	h5A[15:11]	RW	VS_DP	0	0..31	**Horizontal Size Frame**
VERPOSG[9:0]	h5A[9:0]	RW	VS_DP	1	0..1023	**Vertical Position Frame**
VERFRAMEG[4:0]	h5B[15:11]	RW	VS_DP	0	0..31	**Vertical Size Frame**
VERWIDTHG[9:0]	h5B[9:0]	RW	VS_DP	0	0..1023	**Vertical Width Frame**
PATTDISCHROMA	h60[15]	RW	VS_DP	0	0,1	**Disable Chroma in all Test Pattern** 0: chroma on 1: chroma off
PATTINVERSE	h60[14]	RW	VS_DP	0	0,1	**Invert Luma Test Pattern** 0: normal 1: inverted
PATTMODE[2:0]	h60[8:6]	RW	VS_DP	0	0,1,2,3,4,5,6,7	**Test Pattern Mode** 000: colored background 001: geometry 010: balance 011: Y-ramp fast 100: Y-ramp slow 101: YUV-ramp 110: color bar 111: crosshatch
FRAMEDIMM	h60[2]	RW	VS_DP	0	0,1	**Frame Dimension Master** 0: 2-dim. 1: 3-dim.
PRIOF[2:0]	h61[14:12]	RW	VS_DP	3	0..7	**Priority PIP Frame**
PRIOS[2:0]	h61[11:9]	RW	VS_DP	4	0..7	**Priority PIP**
PRIOG[2:0]	h61[8:6]	RW	VS_DP	5	0..7	**Priority Video Frame**
PRIOM[2:0]	h61[5:3]	RW	VS_DP	6	0..7	**Priority Video**
PRIOC[2:0]	h61[2:0]	RW	VS_DP	7	0..7	**Priority Curtain**
PRIOP[2:0]	h62[2:0]	RW	VS_DP	2	0..7	**Priority Background/Testpattern**

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
MATRIX						
MR1M[9:0]	h64[9:0]	RW	VS_DP	0	-512..511	**Matrix Coefficient Red 1** R-Y = MR1M/64*CB + MR2M/64*CR
MR2M[9:0]	h65[9:0]	RW	VS_DP	86	-512..511	**Matrix Coefficient Red 2** R-Y = MR1M/64*CB + MR2M/64*CR
MG1M[9:0]	h66[9:0]	RW	VS_DP	1002	-512..511	**Matrix Coefficient Green 1** G-Y = MG1M/64*CB + MG2M/64*CR
MG2M[9:0]	h67[9:0]	RW	VS_DP	980	-512..511	**Matrix Coefficient Green 2** G-Y = MG1M/64*CB + MG2M/64*CR
MB1M[9:0]	h68[9:0]	RW	VS_DP	113	-512..511	**Matrix Coefficient Blue 1** B-Y = MB1M/64*CB + MB2M/64*CR
MB2M[9:0]	h69[9:0]	RW	VS_DP	0	-512..511	**Matrix Coefficient Blue 2** B-Y = MB1M/64*CB + MB2M/64*CR
TINT[5:0]	h6B[13:8]	RW	VS_DP	0	..-32..31..	**Tint**
SAT[5:0]	h6B[5:0]	RW	VS_DP	32	0..63	**Saturation**
CONTR[5:0]	h6C[14:9]	RW	VS_DP	32	0..63	**Contrast**
BRIGH[8:0]	h6C[8:0]	RW	VS_DP	0	-256..255	**Luma Offset**
SVM						
SVCORR[3:0]	h78[12:9]	RW	VS_DP	0	0..15	**SVM Coring**
SVGAIN[5:0]	h78[8:3]	RW	VS_DP	32	0..63	**SVM Gain**
SVDIFF[2:0]	h78[2:0]	RW	VS_DP	1	0..4	**SVM Differentiator Window**
SVDEL[3:0]	h79[9:6]	RW	VS_DP	8	0..15	**SVM Delay** delay of SVM signal versus analog RGB outputs in half clock steps
SVLIM[5:0]	h79[5:0]	RW	VS_DP	63	0..63	**SVM Limiter** SVM output signal is limited to +/-(SVLIM+1)*2
DAC						
STANDBYDAC	h82[0]	RW	VS_DP	0	0,1	**Standby Video DACs** 0: normal mode 1: standby mode
DEFL						
SAFETYMODE	hD2[15]	RW	VS_DEFL	0	0,1	**Safety Pin Mode** 0: SAFETY input 1: Sync output (depending on CSYEN)
OSDSYNCMODE	hD2[14]	RW	VS_DEFL	0	0,1	**OSD Sync Mode** 0: internal syncs from ODC 1: external syncs from VPROT&SAFETY
FIELDEN	hD2[13]	RW	VS_DEFL	0	0,1	**Field Enable** 0: DFVBL output 1: Field output
HOUTSTR	hD2[12]	RW	VS_DEFL	0	0,1	**HOUT Driver Strength** 0: strong 1: weak
HPROTLIM[7:0]	hD2[7:0]	RW	VS_DEFL	192	0..255	**HOUT Limiter** limit of low period of HOUT signal in clk20 steps
XDFP						
XDFPWRA[15:0]	hF0[15:0]	RW		0	0..65535	**XDFP RAM Write Address**
XDFPRDA[15:0]	hF1[15:0]	RW		0	0..65535	**XDFP RAM Read Address**
XDFPWRD[15:0]	hF2[15:0]	RW		0	0..65535	**XDFP RAM Write Data**
XDFPRDD[15:0]	hF3[15:0]	R	loa-dReg		0..65535	**XDFP RAM Read Data**
XDFPRDBUSY	hF4[2]	R			0,1	**XDFP Read Busy** 0: not busy 1: busy
XDFPWRBUSY	hF4[1]	R			0,1	**XDFP Write Busy** 0: not busy 1: busy
XDFPBUSY	hF4[0]	R			0,1	**XDFP Busy** 0: not busy 1: busy

Table 3–6: I2C Register Description, continued

Name	Sub	Dir	Sync	Reset	Range	Function
I2C						
VS_DEFL_STAT	hFD[3]	R	VS_DP		0,1	**Vertical Update Status Deflection** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
VS_ITUO_STAT	hFD[2]	R	VS_DP		0,1	**Vertical Update Status ITU656 Output** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
VS_ODC_STAT	hFD[1]	R	VS_DP		0,1	**Vertical Update Status ODC** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
VS_DP_STAT	hFD[0]	R	VS_DP		0,1	**Vertical Update Status Display Processing** 0: no vertical update since last read 1: vertical update since last read automatically reset after read
IM_DEFL	hFE[3]	RW		0	0,1	**Immediate Update Deflection** 0: no immediate take-over 1: immediate take-over
IM_ITUO	hFE[2]	RW		0	0,1	**Immediate Update ITU656 Output** 0: no immediate take-over 1: immediate take-over
IM_ODC	hFE[1]	RW		0	0,1	**Immediate Update ODC** 0: no immediate take-over 1: immediate take-over
IM_DP	hFE[0]	RW		0	0,1	**Immediate Update Display Processing** 0: no immediate take-over 1: immediate take-over
VS_DEFL	hFF[3]	RW		1	0,1	**Vertical Update Deflection** 0: no vertical take-over 1: vertical take-over
VS_ITUO	hFF[2]	RW		1	0,1	**Vertical Update ITU656 Output** 0: no vertical take-over 1: vertical take-over
VS_ODC	hFF[1]	RW		1	0,1	**Vertical Update ODC** 0: no vertical take-over 1: vertical take-over
VS_DP	hFF[0]	RW		1	0,1	**Vertical Update Display Processing** 0: no vertical take-over 1: vertical take-over

3.12. XDFP Register Block Index

3.13. XDFP Register Index

3.14. XDFP Register Subaddress Index

Table 3–7: XDFP-RAM Subaddress Index

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
hF2-0118																	h0010
hF2-01BB	NCE_UPDATE	GAMMA[9:0]															h0000
hF2-01BC							SWS_SP[9:0]										h0000
hF2-01BD	SWS_GR[9:0]																h0000
hF2-01BE	SWS_GG[9:0]																h0000
hF2-01BF	SWS_GB[9:0]																h0000
hF2-01D8	GBF						DPWL_SP[9:0]										h0000
hF2-01D9	DPWL_GAIN[9:0]																h0000
hF2-0027												BSO	HUP	HLIM	HPROT	VPROT	
hF2-013C								TML[8:0]									h000D
hF2-0104							WDRM[9:0]										h0000
hF2-01C0								IBRM[8:0]									h0000
hF2-01C1					MADCLATCH[11:0]												h0000
hF2-01C2			BWSEL			CLAMPV	CLAMP	SMODE	MBLANK	CUT_DIS	WDR_DIS	WDR_FIRST	BLANK_DIS	ULBLK_DIS			h0000
hF2-006B					CUTMEAS_R[8:0]												
hF2-006C					CUTMEAS_G[8:0]												
hF2-006D					CUTMEAS_B[8:0]												
hF2-010E																	h0000
hF2-010F																	h0000
hF2-0110																	h0000
hF2-01C3				CUTREF_R[8:0]													h0000
hF2-01C4				CUTREF_G[8:0]													h0000
hF2-01C5				CUTREF_B[8:0]													h0000
hF2-01C6		CUT_GAIN[8:0]															h0000
hF2-006E					WDRMEAS_R[8:0]												
hF2-006F					WDRMEAS_G[8:0]												
hF2-0070					WDRMEAS_B[8:0]												
hF2-0101																	h03FC
hF2-0102																	h03FC
hF2-0103																	h03FC

Table 3–7: XDFP-RAM Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
hF2-01C7		WDR_GAIN[8:0]															h0000
hF2-01C8				WDRREF_R[8:0]													h0000
hF2-01C9				WDRREF_G[8:0]													h0000
hF2-01CA				WDRREF_B[8:0]													h0000
hF2-01CB																	h0000
hF2-004F		BC[11:0]															
hF2-01CD				PWL_TC[8:0]													h0000
hF2-01CE		PWL_LIM[8:0]															h0000
hF2-01CF				BCL_BRTRED[8:0]													h0000
hF2-01D0		BCL_GAIN[8:0]															h0000
hF2-01D1	BCL_THRES[12:0]																h0000
hF2-01D2								BCL_TC[8:0]									h0000
hF2-01D3								BCL_TCUP[8:0]									h0000
hF2-01D4		BCL_MIN_C[8:0]															h0000
hF2-01D5																	h0000
hF2-01D6		BC_MIN[11:0]															
hF2-01D7		BC_MAX[11:0]															
hF2-01DA				PIC_TC[8:0]													h0000
hF2-01DB																NOOS-DBCL	h0000
hF2-0071		HB1[14:0]															
hF2-0072		HB2[14:0]															
hF2-0073		HB3[14:0]															
hF2-0074		HB4[14:0]															
hF2-0075		HB5[14:0]															
hF2-0076		HB6[14:0]															
hF2-0077		HB7[14:0]															
hF2-0078		HB8[14:0]															
hF2-01E9															HISTO_EN	WDR_SAT	h0000
hF2-0131						HBST[10:0]											h0502
hF2-0132						HBSO[10:0]											h00D0
hF2-013B	VBST[15:0]																h0136
hF2-013A								VBSO[8:0]									h0018
hF2-0133									CLAMPSTART[7:0]								h0000
hF2-0134																	h0000

Table 3–7: XDFP-RAM Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
hF2-0135																	h0001
hF2-0136						DFHB[10:0]											h01F4
hF2-0137						DFHE[10:0]											h0384
hF2-0000																	
hF2-0001																	
hF2-0002																	
hF2-0080																	
hF2-0081																	
hF2-0082																	
hF2-0083																	
hF2-0084																	
hF2-0085																	
hF2-0180									HPROT_SS	HPROT_BL	HOUT_STOP	RAMP_EN	EFLB		VPROT_BL		h0000
hF2-0181											HDRV[5:0]						h0020
hF2-0182	POFS3[15:0]																hFFF4
hF2-0183																	h0474
hF2-0184																	h0592
hF2-0185		PKP3[8:0]															h4000
hF2-0187	ANGLE[9:0]																h0000
hF2-0188	BOW[9:0]																h0000
hF2-013D																	h050F
hF2-0190	VAMPL[9:0]																h0000
hF2-0191		VZOOM[8:0]															h4000
hF2-0192	VPOS[9:0]																h0000
hF2-0193	VLIN[9:0]																h0000
hF2-0194	SCORR[9:0]																h0000
hF2-0195										VSYNWIN[6:0]							h0020
hF2-0196							LPFD[9:0]										h0138
hF2-0197							HOLDL[9:0]										h000A
hF2-0198							FLYBL[9:0]										h0005
hF2-01E2																	h0000
hF2-01E3															R_MODE[1:0]		h0000
hF2-01E4																	h0000
hF2-01E8																VA_MODE	h0000

Table 3–7: XDFP-RAM Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
hF2-01EB																BSO_EN	h0000
hF2-019A	WIDTH[8:0]																h0000
hF2-019B	TCORR[9:0]																h0000
hF2-019C	CUSH[9:0]															EWPWM	h0080
hF2-019D	CRNU[9:0]																h0000
hF2-019E	CRNL[9:0]																h0000
hF2-019F	CRNUS[9:0]																h0000
hF2-01A0	CRNLS[9:0]																h0000
hF2-01A5		EHT_THRES[10:0]															h1800
hF2-01A6		EHT_STC[8:0]															h0000
hF2-01A7	EHTV_SA1[9:0]																h0000
hF2-01A8	EHTV_SA2[9:0]																h0000
hF2-01A9	EHTH_DA1[9:0]																h0000
hF2-01AA	EHTH_DA2[9:0]																h0000
hF2-01AB		EHT_DTC[8:0]															h0000
hF2-01AC		EHTH_DP1[8:0]															h0000
hF2-01AD		EHTH_DP2[8:0]															h0000
hF2-00C1																	h0010
hF2-00C2																	h0010
hF2-00C3																	h0010
hF2-0105																	h0100
hF2-0106																	h0100
hF2-0107																	h0100
hF2-0108																	h0100
hF2-0109																	h0100
hF2-010A																	h0100
hF2-010B																	h03FC
hF2-010C																	h03FC
hF2-010D																	h03FC
hF2-0111																	h0040
hF2-0112																	h0040
hF2-0113																	h0040
hF2-01DB		EXT_CONTR[8:0]															h0000
hF2-01DC	EXT_BRT[9:0]																h0000

Table 3–7: XDFP-RAM Subaddress Index, continued

Sub	Data Bits																Reset
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
hF2-01DD	INT_BRT[9:0]																h0000
hF2-01DE						CORLEV[1:0]				FBMON	FBPOL	FBPRIO	FBFOL2	FBFOH 2	FBFOL1	FBFOH 1	h0000
hF2-00D1									PWM_VHS[7:0]								h0010
hF2-00D2														PWM_CTRL[2:0]			h0000
hF2-0020	VERSION[15:0]																

3.15. XDFP Register Description

Note: For compatibility reasons every undefined bit in a writeable register should be set to “0”. Undefined bits in a readable register should be treated as “don’t care”!

Table 3–8: XDFP-RAM Register Description

Name	Sub	Addr	Dir	Reset	Range	Function
NCE						
NCE_UPDATE	hF2	h01BB[15]	RW	0	0,1	**NCE Update** 0: don't update NCE settings 1: update NCE settings
GAMMA[9:0]	hF2	h01BB[14:5]	RW	0	-512..511	**Gamma Correction Value**
SWS_SP[9:0]	hF2	h01BC[9:0]	RW	0	0..1023	**Subjective White Shaping Start Point**
SWS_GR[9:0]	hF2	h01BD[15:6]	RW	0	-512..511	**Subjective White Shaping Gain for Red**
SWS_GG[9:0]	hF2	h01BE[15:6]	RW	0	-512..511	**Subjective White Shaping Gain for Green**
SWS_GB[9:0]	hF2	h01BF[15:6]	RW	0	-512..511	**Subjective White Shaping Gain for Blue**
GBF	hF2	h01D8[15]	RW	0	0,1	**Gamma Base Function** 0: native 1: soft
DPWL_SP[9:0]	hF2	h01D8[9:0]	RW	0	0..1023	**Digital Peak White Limiter Start Point**
DPWL_GAIN[9:0]	hF2	h01D9[15:6]	RW	0	-512..0	**Digital Peak White Limiter Gain**
Protection						
BSO	hF2	h0027[4]	R		0,1	**BSO Status** 0: not active 1: active
HUP	hF2	h0027[3]	R		0,1	**HOUT Status** 0: stopped 1: started
HLIM	hF2	h0027[2]	R		0,1	**HOUT stopped on HPROTLIM**
HPROT	hF2	h0027[1]	R		0,1	**Horizontal Protection** 0: okay 1: failed
VPROT	hF2	h0027[0]	R		0,1	**Vertical Protection** 0: okay 1: failed
Measurement						
TML[8:0]	hF2	h013C[8:0]	RW	13	0..511	**Start Line for Tube Measurement**
WDRM[9:0]	hF2	h0104[9:0]	RW	0	0..1023	**RGB Level for White Drive Current Measurement**
IBRM[8:0]	hF2	h01C0[8:0]	RW	0	0..511	**Internal Brightness for Measurement**
MADCLATCH[11:0]	hF2	h01C1[11:0]	RW	0	0..4095	**Latch Measurement Value relative to HBST**
BWSEL	hF2	h01C2[13]	RW	0	0,1	**Select Measurement Bandwidth** 0: 78kHz 1: 39kHz
CLAMPV	hF2	h01C2[10]	RW	0	0,1	**RGB Clamping during Vertical Blanking**
CLAMP	hF2	h01C2[9]	RW	0	0,1	**RGB Clamping**
SMODE	hF2	h01C2[8]	RW	0	0,1	**Sense Mode** 0: use SENSE pin for BCL measurement 1: use RSW1 pin for BCL measurement
MBLANK	hF2	h01C2[7]	RW	0	0,1	**Horizontal Blanking During Measurement Disable** 0: enable 1: disable, stop loop
CUT_DIS	hF2	h01C2[6]	RW	0	0,1	**Cutoff Measurement** 0: enable 1: disable, stop loop
WDR_DIS	hF2	h01C2[5]	RW	0	0,1	**White Drive Measurement** 0: enable 1: disable, stop loop

Table 3–8: XDFP-RAM Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
WDR_FIRST	hF2	h01C2[4]	RW	0	0,1	**White Drive Measurement Timing** 0: after cutoff 1: before cutoff
BLANK_DIS	hF2	h01C2[3]	RW	0	0,1	**Video Mute** 0: video mute (RGB outputs blanked) 1: normal mode
ULBLK_DIS	hF2	h01C2[2]	RW	0	0,1	**Ultra Black during Blanking** 0: ultrablack 1: black
Cutoff						
CUTMEAS_R[8:0]	hF2	h006B[11:3]	R		0..511	**Measured Cutoff Value for Red**
CUTMEAS_G[8:0]	hF2	h006C[11:3]	R		0..511	**Measured Cutoff Value for Green**
CUTMEAS_B[8:0]	hF2	h006D[11:3]	R		0..511	**Measured Cutoff Value for Blue**
CUTREF_R[8:0]	hF2	h01C3[12:4]	RW	0	0..511	**Reference for Cutoff Red**
CUTREF_G[8:0]	hF2	h01C4[12:4]	RW	0	0..511	**Reference for Cutoff Green**
CUTREF_B[8:0]	hF2	h01C5[12:4]	RW	0	0..511	**Reference for Cutoff Blue**
CUT_GAIN[8:0]	hF2	h01C6[14:6]	RW	0	0..511	**Gain for Cutoff Control Loop** 0: the reference values are directly taken as cutoff values 1..511: gain for cutoff control loop
White Drive						
WDRMEAS_R[8:0]	hF2	h006E[11:3]	R		0..511	**Measured White Drive Value for Red**
WDRMEAS_G[8:0]	hF2	h006F[11:3]	R		0..511	**Measured White Drive Value for Green**
WDRMEAS_B[8:0]	hF2	h0070[11:3]	R		0..511	**Measured White Drive Value for Blue**
WDR_GAIN[8:0]	hF2	h01C7[14:6]	RW	0	0..511	**Gain for White Drive Control Loop** 0: the reference values are directly taken as white drive values 1..511: gain for white drive control loop
WDRREF_R[8:0]	hF2	h01C8[12:4]	RW	0	0..511	**Reference for White Drive Red**
WDRREF_G[8:0]	hF2	h01C9[12:4]	RW	0	0..511	**Reference for White Drive Green**
WDRREF_B[8:0]	hF2	h01CA[12:4]	RW	0	0..511	**Reference for White Drive Blue**
BCL						
BC[11:0]	hF2	h004F[14:3]	R		0..4095	**Measured Picture Beam Current** Latched every line except during VBI
PWL_TC[8:0]	hF2	h01CD[12:4]	RW	0	0..511	**Peak White Limiter Time Constant**
PWL_LIM[8:0]	hF2	h01CE[14:6]	RW	0	0..511	**Peak White Limiter Maximum**
BCL_BRTRED[8:0]	hF2	h01CF[12:4]	RW	0	0..511	**BCL Brightness Reduction on Average Picture Level**
BCL_GAIN[8:0]	hF2	h01D0[14:6]	RW	0	0..511	**BCL Loop Gain**
BCL_THRES[12:0]	hF2	h01D1[15:3]	RW	0	-4096..4095	**BCL Threshold Current** 0..4095: measured through sense input (with SMODE=0) -4096..0 measured through RSW1 input (with SMODE=1)
BCL_TC[8:0]	hF2	h01D2[8:0]	RW	0	0..511	**BCL Time Constant** 0: BCL off 1..511: 800ms ... 0.025ms
BCL_TCUP[8:0]	hF2	h01D3[8:0]	RW	0	0..511	**BCL Second Time Constant for Increasing Contrast.** 0: take BCL_TC instead 1..511: 800ms ... 0.025ms
BCL_MIN_C[8:0]	hF2	h01D4[14:6]	RW	0	0..511	**BCL Minimum Contrast** The Beam Current Limiter will stop reducing the contrast at BCL_MIN_C level and will continue by reducing brightness.
BC_MIN[11:0]	hF2	h01D6[14:3]	R		0..4095	**Measured Minimum Beam Current** Updated every field.
BC_MAX[11:0]	hF2	h01D7[14:3]	R		0..4095	**Measured Maximum Beam Current** Updated every field.
PIC_TC[8:0]	hF2	h01DA[12:4]	RW	0	0..511	**Time Constant for Average Picture Level**
NOOSDBCL	hF2	h01DB[0]	RW	0	0,1	**BCL Function for Analog RGB** 0: beam current limiter also reduces OSD/external RGB 1: beam current limiter does not affect OSD/external RGB
Histogram						
HB1[14:0]	hF2	h0071[14:0]	R		0..32767	**Histogram Basket for Values 0-63**

Table 3–8: XDFP-RAM Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
HB2[14:0]	hF2	h0072[14:0]	R		0..32767	**Histogram Basket for Values 64-127**
HB3[14:0]	hF2	h0073[14:0]	R		0..32767	**Histogram Basket for Values 128-191**
HB4[14:0]	hF2	h0074[14:0]	R		0..32767	**Histogram Basket for Values 192-255**
HB5[14:0]	hF2	h0075[14:0]	R		0..32767	**Histogram Basket for Values 256-319**
HB6[14:0]	hF2	h0076[14:0]	R		0..32767	**Histogram Basket for Values 320-383**
HB7[14:0]	hF2	h0077[14:0]	R		0..32767	**Histogram Basket for Values 384-447**
HB8[14:0]	hF2	h0078[14:0]	R		0..32767	**Histogram Basket for Values 448-511**
HISTO_EN	hF2	h01E9[1]	RW	0	0,1	**Histogram Calculation** 0: disable 1: enable
WDR_SAT	hF2	h01E9[0]	RW	0	0,1	**Automatic Drive Saturation Avoidance** 0: disable 1: enable
H/V Timing						
HBST[10:0]	hF2	h0131[10:0]	RW	1282	0..1295	**Horizontal Blanking Start** Granularity: pixel (50ns=1/20.25MHz)
HBSO[10:0]	hF2	h0132[10:0]	RW	208	0..1295	**Horizontal Blanking Stop** Granularity: pixel (50ns=1/20.25MHz)
VBST[15:0]	hF2	h013B[15:0]	RW	310	-127..343	**Vertical Blanking Start Line**
VBSO[8:0]	hF2	h013A[8:0]	RW	24	4..343	**Vertical Blanking Stop Line**
CLAMPSTART[7:0]	hF2	h0133[7:0]	RW	0	0..255	**Horizontal Clamping Start**
DFHB[10:0]	hF2	h0136[10:0]	RW	500	0..1295	**Dynamic Focus Horizontal Begin**
DFHE[10:0]	hF2	h0137[10:0]	RW	900	0..1295	**Dynamic Focus Horizontal End**
Horizontal Deflection						
HPROT_SS	hF2	h0180[7]	RW	0	0,1	**Soft Stop on Horizontal Safety Protection** 0: no action 1: soft stop if HPROT active
HPROT_BL	hF2	h0180[6]	RW	0	0,1	**Blank on Horizontal Safety Protection** 0: no action 1: blank RGB outputs if HPROT active
HOUT_STOP	hF2	h0180[5]	RW	0	0,1	**Stop H-Drive** 0: no action 1: stop hdrive this bit is automatically reset after ramp up
RAMP_EN	hF2	h0180[4]	RW	0	0,1	**Start H-Drive Ramp up** 0: no action 1: start ramp up this bit is automatically reset after write
EFLB	hF2	h0180[3]	RW	0	0,1	**H-Drive High During Flyback** 0: HOUT independent of HFLB 1: HOUT is high as long as HFLB active
VPROT_BL	hF2	h0180[1]	RW	0	0,1	**Blank on Vertical Protection** 0: no action 1: blank RGB outputs if VPROT active
HDRV[5:0]	hF2	h0181[5:0]	RW	32	0..63	**Horizontal Drive Pulse Duration** High time 0..100%
POFS3[15:0]	hF2	h0182[15:0]	RW	65524	-648..647	**PLL3 Phase Offset** Adjustable phase of horizontal flyback
PKP3[8:0]	hF2	h0185[14:6]	RW	256	0..511	**PLL3 Proportional Gain**
ANGLE[9:0]	hF2	h0187[15:6]	RW	0	-512..511	**Angle Compensation**
BOW[9:0]	hF2	h0188[15:6]	RW	0	-512..511	**Bow Compensation**
Vertical Deflection						
VAMPL[9:0]	hF2	h0190[15:6]	RW	0	-512..511	**Vertical Amplitude Correction** -25%..+25%
VZOOM[8:0]	hF2	h0191[14:6]	RW	256	0..511	**Vertical Zoom** 0: 0% 256: 100% 511: 200%

Table 3–8: XDFP-RAM Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
VPOS[9:0]	hF2	h0192[15:6]	RW	0	-512..511	**Vertical Picture Position** -25%..+25% DC offset of sawtooth, independent of EHT compensation
VLIN[9:0]	hF2	h0193[15:6]	RW	0	-512..511	**Vertical Linearity** -25%..+25%
SCORR[9:0]	hF2	h0194[15:6]	RW	0	-512..511	**S-Correction** -20%..+20%
VSYNWIN[6:0]	hF2	h0195[6:0]	RW	32	0..127	**Window for Vertical Sync Capture** The system can synchronize to a signal which lines per field are in the range LPFD+/-VSYNWIN.
LPFD[9:0]	hF2	h0196[9:0]	RW	312	0..1023	**Nominal Number of Lines per Field** 262: 60Hz 312: 50Hz
HOLDL[9:0]	hF2	h0197[9:0]	RW	10	0..127	**Number of Hold Lines** After the vertical retrace the sawtooth signal is kept at the start point during this period (usefull when using zoom).
FLYBL[9:0]	hF2	h0198[9:0]	RW	5	0..127	**Number of Flyback Lines** The flyback booster is active during this period to allow faster vertical retrace.
R_MODE[1:0]	hF2	h01E3[1:0]	RW	0	0,1,2	**Raster Mode** 0: interlaced input - progressive raster 1: interlaced input - interlaced raster AB 2: interlaced input - interlaced raster BA 3: not used
VA_MODE	hF2	h01E8[0]	RW	0	0,1	**Automatic Lines per Field Adaption** 0: disable 1: enable. The sawtooth signal (VERT) is adapted to the lines per field of the video signal. Thus the full picture can be displayed on the display raster.
BSO_EN	hF2	h01EB[0]	RW	0	0,1	**Black Switch Off on Horizontal Safety Protection** 0: no action 1: black switch off if HPROT active
East-West Parabola						
WIDTH[8:0]	hF2	h019A[15:7]	RW	0	-256..255	**Picture Width** 0..100%
TCORR[9:0]	hF2	h019B[15:6]	RW	0	-512..511	**Trapezoidal Correction** -50%..+50%
CUSH[9:0]	hF2	h019C[15:6]	RW	2	-512..511	**Cushion Correction** -25%..+25%
EWPWM	hF2	h019C[0]	RW	0	0,1	**EW Output Mode** 0: analog 1: pwm
CRNU[9:0]	hF2	h019D[15:6]	RW	0	-512..511	**Upper Corner Correction** -6%..+6%
CRNL[9:0]	hF2	h019E[15:6]	RW	0	-512..511	**Lower Corner Correction** -6%..+6%
CRNUS[9:0]	hF2	h019F[15:6]	RW	0	-512..511	**Upper Corner Correction 6th Order Term** -6%..+6%
CRNLS[9:0]	hF2	h01A0[15:6]	RW	0	-512..511	**Lower Corner Correction 6th Order Term** -6%..+6%
EHT Compensation						
EHT_THRES[10:0]	hF2	h01A5[14:4]	RW	384	0..2047	**EHT Compensation Threshold** Threshold for second gains of static horizontal and vertical EHT compensation
EHT_STC[8:0]	hF2	h01A6[14:6]	RW	0	0..511	**EHT Static Time Constant** for horizontal and vertical amplitude compensation 0: EHT compensation off 1: 800ms ... 511: 0.025ms
EHTV_SA1[9:0]	hF2	h01A7[15:6]	RW	0	-512..511	**1st Gain for Static Vertical Amplitude Compensation** +/-100%, for beam current<EHT_THRES

Table 3–8: XDFP-RAM Register Description, continued

Name	Sub	Addr	Dir	Reset	Range	Function
EHTV_SA2[9:0]	hF2	h01A8[15:6]	RW	0	-512..511	**2nd Gain for Static Vertical Amplitude Compensation** +/-100%, for beam current>EHT_THRES
EHTH_DA1[9:0]	hF2	h01A9[15:6]	RW	0	-512..511	**1st Gain for Dynamic Horizontal Amplitude Compensation** +/-100%, for beam current<EHT_THRES
EHTH_DA2[9:0]	hF2	h01AA[15:6]	RW	0	-512..511	**2nd Gain for Dynamic Horizontal Amplitude Compensation** +/-100%, for beam current>EHT_THRES
EHT_DTC[8:0]	hF2	h01AB[14:6]	RW	0	0..511	**EHT Dynamic Time Constant**
EHTH_DP1[8:0]	hF2	h01AC[14:6]	RW	0	0..511	**1st Gain for Dynamic Horizontal Phase Compensation** +/-100%, for beam current<EHT_THRES
EHTH_DP2[8:0]	hF2	h01AD[14:6]	RW	0	0..511	**2nd Gain for Dynamic Horizontal Phase Compensation** +/-100%, for beam current>EHT_THRES
Analog RGB						
EXT_CONTR[8:0]	hF2	h01DB[14:6]	RW	0	0..511	**External Contrast** Analog contrast for OSD and external RGB
EXT_BRT[9:0]	hF2	h01DC[15:6]	RW	0	-256..255	**External Brightness** Analog Brightness for OSD and external RGB. The range allows for both increase and reduction of brightness.
INT_BRT[9:0]	hF2	h01DD[15:6]	RW	0	-256..255	**Internal Brightness** Analog Brightness for main picture (from DACs). The range allows for both increase and reduction of brightness.
CORLEV[1:0]	hF2	h01DE[10:9]	RW	0	0,1,2,3	**Contrast Reduction Level.** For OSD insertion with reduced video contrast as background. Reduction of the RGB signals (except OSD) by: 0: 0% (no reduction) 1: 25% 2: 50% (half contrast) 3: 75%
FBMON	hF2	h01DE[6]	RW	0	0,1	**Fast Blank Monitor Input** 0: from external FB pin 1: from OSD
FBPOL	hF2	h01DE[5]	RW	0	0,1	**Fast Blank Polarity** 0: high active 1: low active
FBPRIO	hF2	h01DE[4]	RW	0	0,1	**Fast Blank Priority** 0: external RGB on top of OSD 1: OSD on top of external RGB
FBFOL2	hF2	h01DE[3]	RW	0	0, 1	**Force OSD Fast Blank Low** 0: FB from OSD 1: force to low
FBFOH2	hF2	h01DE[2]	RW	0	0, 1	**Force OSD Fast Blank High** 0: FB from OSD 1: force to high
FBFOL1	hF2	h01DE[1]	RW	0	0, 1	**Force External Fast Blank Low** 0: fast blank from pin 1: force to low
FBFOH1	hF2	h01DE[0]	RW	0	0, 1	**Force External Fast Blank High** 0: fast blank from pin 1: force to high
PWM						
PWM_VHS[7:0]	hF2	h00D1[7:0]	RW	16	0..255	**PWM Value**
PWM_CTRL[2:0]	hF2	h00D2[2:0]	RW	0	0..7	**PWM Control**
XDFP						
VERSION[15:0]	hF2	h0020[15:0]	R		0..65535	**Version Number** bit15..12: major hardware version bit11..8: minor hardware version bit7..4: major firmware version bit3..0: minor firmware version

4. Data Sheet History

1. Advance Information: “VCT 49xyl, VCT 48xyl Display and Deflection Processor”, 12.12.2003, 6251-573-5-1AI. First release of the advance information.

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Contents

Contents, continued

Contents, continued

Contents, continued

Contents, continued

1. Introduction

Volume 6 describes the Controller, OSD and Text Processing (TVT) of VCT 49xyl, VCT 48xyl.

1.1. Chip Architecture

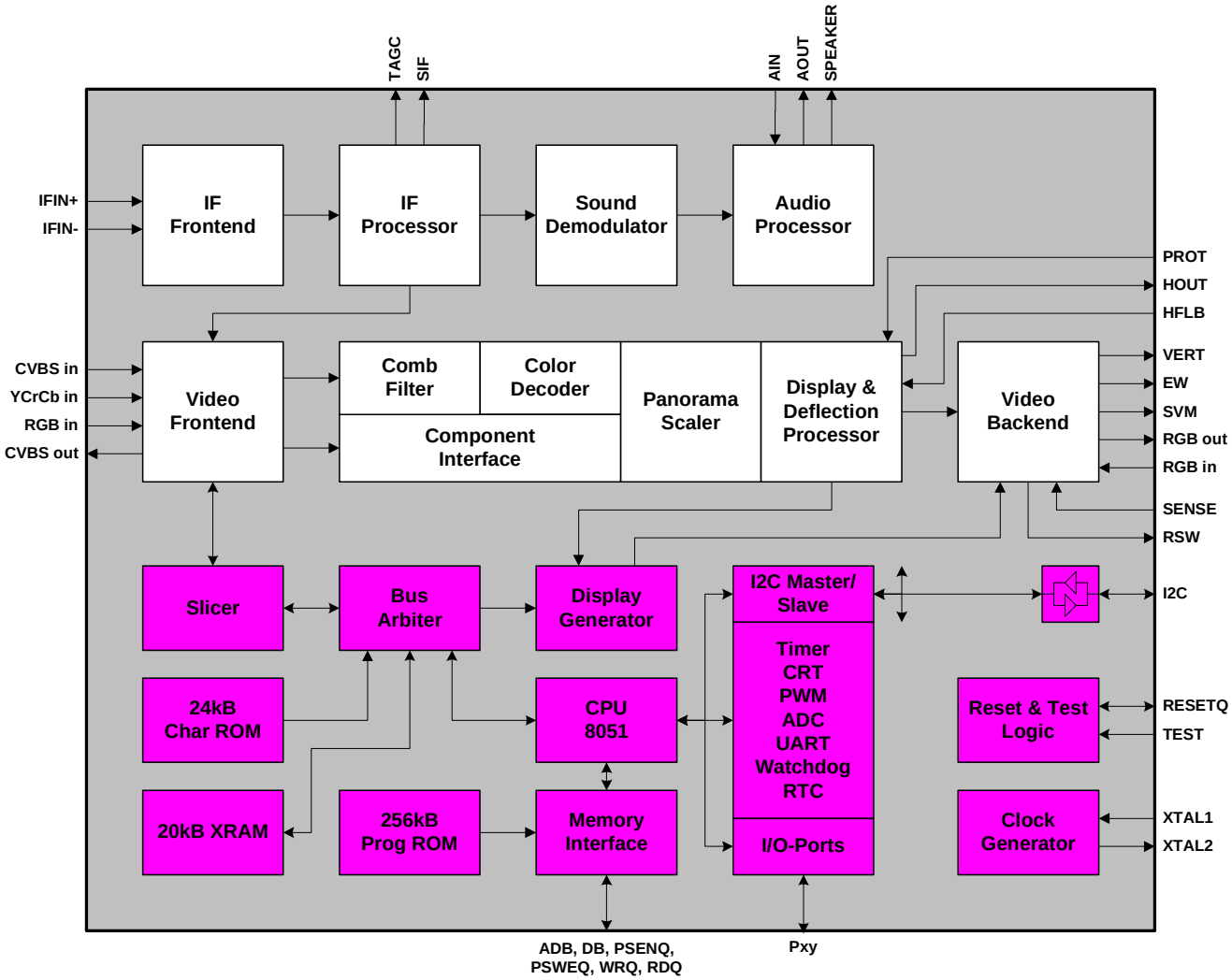


Fig. 1–1: Block diagram of the VCT 49xyl, VCT 48xyl

1.2. Features

Controller Features

- Single external 20.25 MHz crystal, all necessary clocks are generated internally
- Normal mode: 40.5 MHz CPU clock, Power Save mode: 10.125 MHz
- 8-bit 8051 instruction set compatible CPU
- Up to 256 KB on-chip program ROM
- 256 byte on-chip program RAM
- 128 byte on-chip extended stack RAM
- 20 kilobyte on-chip extended data RAM (XRAM)
- Memory banking up to 1 MB
- Non-multiplexed 8-bit data and 20-bit address bus
- Eight 16-bit data pointer registers (DPTR)
- 4-level, 24-input interrupt controller
- Patch module for 16 ROM locations
- Two 16-bit reloadable timers
- Capture-compare timer for infrared decoding
- Watchdog timer
- UART
- Real time clock (RTC)
- PWM units (2 channels 14-bit, 6 channels 8-bit)
- 8-bit ADC (4 channels)
- I^2C bus master/slave interface
- Up to 24 programmable I/O ports
- Flash version for PMQFP144 and PSSDIP88 packages (SST39LF020 or compatible)
- ROM-less version with 1 MB address space for external program and data memory

OSD Features

- 20 KB on-chip OSD RAM
- 24 KB on-chip character ROM
  - supports all East and West European languages
  - national language support (Latin, Cyrillic, Greek, Arabic, Farsi, Hebrew)
  - Mosaic graphic character Set
- WST level 1.5 compliant
- Parallel display attributes
- Single/double width/height characters
- Shadow, underline, italics, flash attributes
- Contrast reduction
- 12 bit programmable color look-up table (64 entries)
- One out of eight colors for foreground and background of 1-bit DRCS and ROM characters
- 16 colors/character in DRCS mode
- Up to 1024 dynamically redefinable characters (DRCS)
- 1024 displayable characters on screen
- Combined character mode
- Horizontal screen resolution: 33…64 columns
- Vertical screen resolution: 25 rows
- Horizontal character resolution: 12 pixel
- Vertical character resolution: 9…16 pixel
- Programmable pixel clock 10…32MHz
- Variable Flash rate
- Vertical soft scroll
- Programmable cursor
- 3×4 bits RGB DACs on-chip

Teletext Features

- Multi-standard digital data slicer
- Full field and VBI data acquisition
- simultaneous WST, PDC, VPS, and WSS acquisition
- Closed Caption and V-chip acquisition
- Up to 11 programmable video inputs
- Acquisition is independent from display part
- Data caption only limited by available memory
- Programmable VBI buffer
- Signal quality detection
- Noise measurement and controlled noise compensation
- Attenuation measurement and compensation
- Group delay measurement and compensation
- Exact decoding of echo disturbed signals
- Up to 10 page on-chip teletext memory
- Up to 1000 page external teletext memory

1.3. Overview

The TVT is a Teletext decoder for decoding World System Teletext data, as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide-Screen Signalling (WSS) data used for PALplus transmissions (line 23). The device also supports Closed Caption acquisition and decoding.

The TVT provides an integrated general-purpose, fully 8051-compatible microcontroller with television-specific hardware features. The microcontroller has been enhanced to provide powerful features such as memory banking, data pointer, additional interrupts, etc.

The on-chip display unit for displaying Level 1.5 Teletext data can also be used for customer-defined on-screen displays.

The TVT has an internal XRAM of 20 KB and an internal ROM of up to 256 KB. ROMless versions can address up to 1 MB of external RAM and ROM.

The 8-bit microcontroller runs at 296 ns cycle time. The controller with dedicated hardware does most of the internal TTX acquisition processing, transfers data to/from external memory interface, and receives/transmits data via I^2C-bus interface.

In combination with dedicated hardware, the slicer stores TTX data in a VBI buffer of 1 KB. The microcontroller firmware performs all the acquisition tasks (hamming and parity checks, page search, and evaluation of header control bits) once per field. Additionally, the firmware can provide high-end Teletext features like Packet-26 handling, FLOF/TOP and list-pages. The interface-to-user software is optimized for minimal overhead.

TVT is realized in deep submicron technology with 1.8 V supply voltage and 3.3 V I/O (TTL compatible).

1.4. Block Diagram

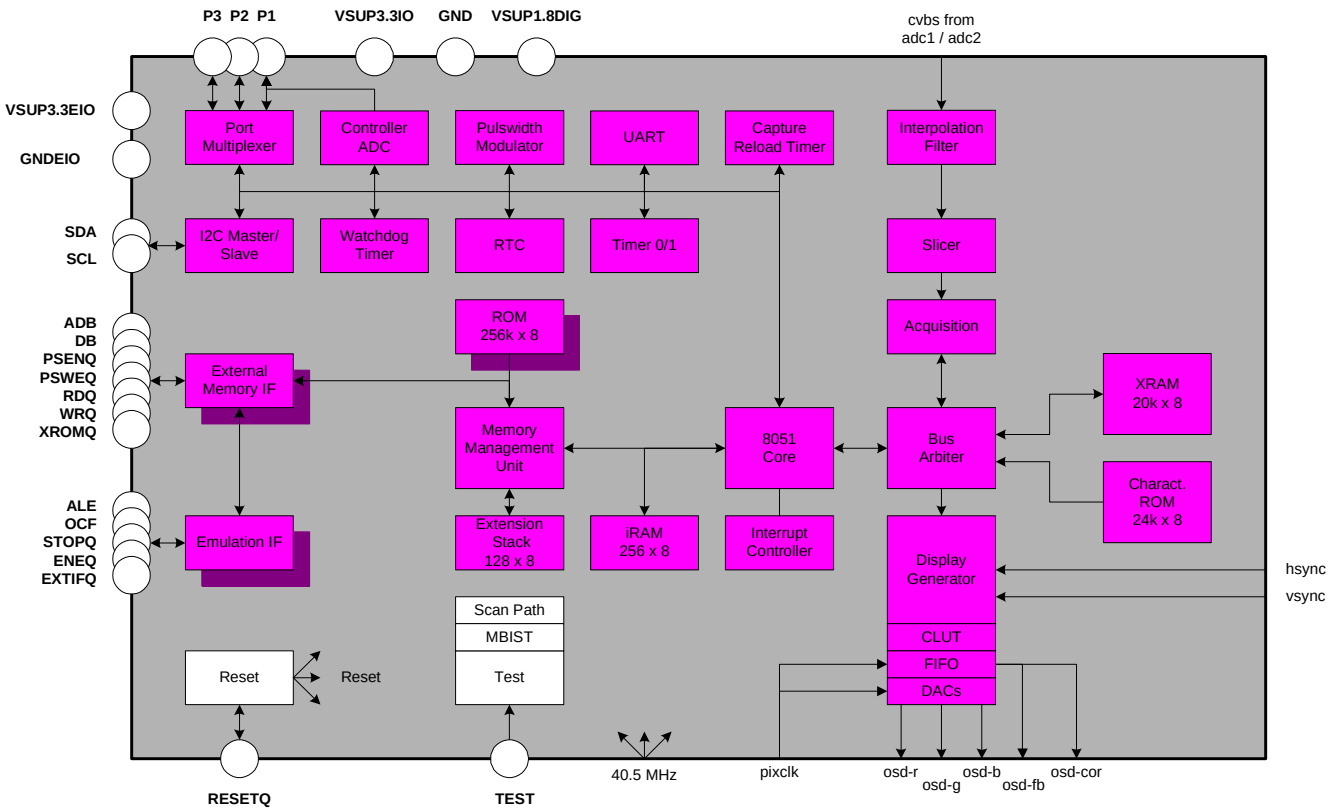


Fig. 1–1: TVT block diagram

2. Functional Description

2.1. Clock System

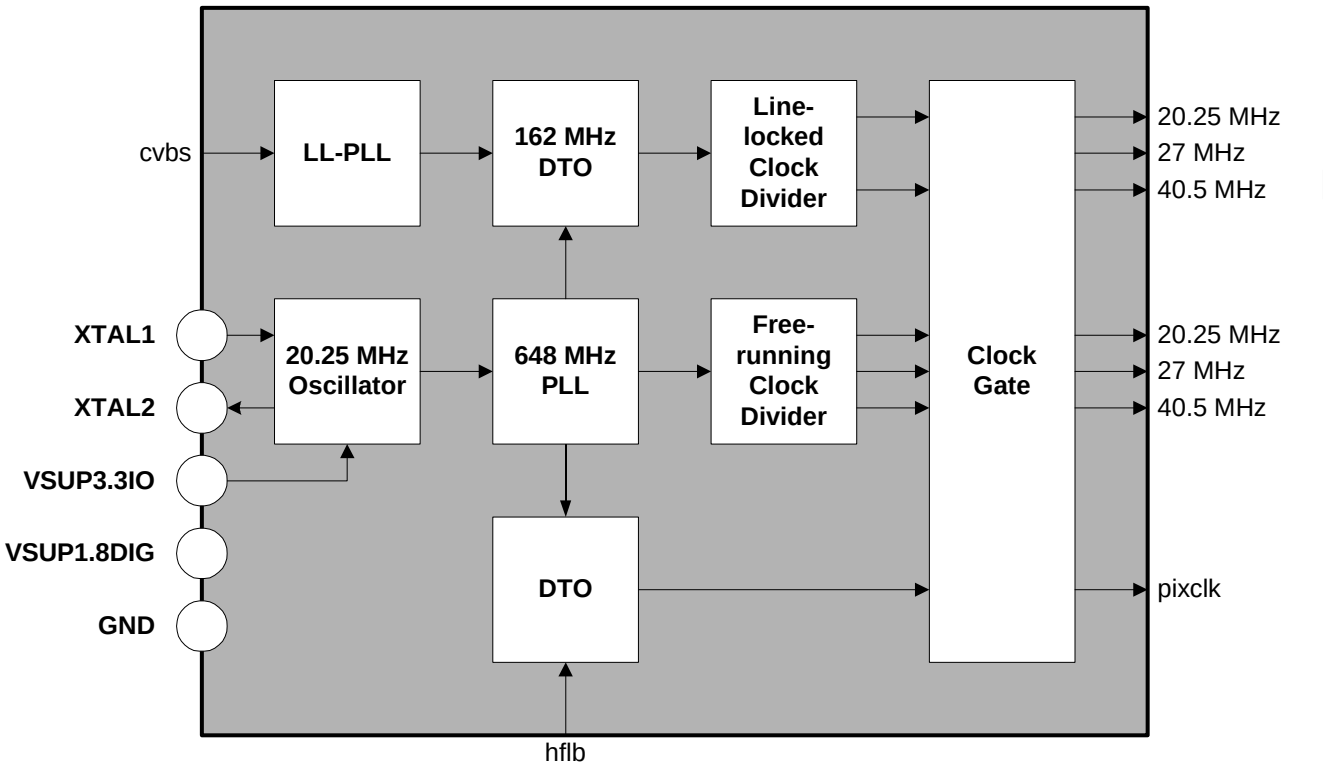


Fig. 2–1: Clock generator

2.1.1. General Function

The on-chip clock generator provides the TVT with its basic clock signals that controls all activities of the hardware. Its oscillator runs with an external crystal and appropriate oscillator circuitry.

The on-chip phase locked loop (PLL) which is internally running at 648 MHz is fed by the oscillator or can be bypassed to reduce the power consumption. If it is not required to wake up immediately the PLL can also be switched off. From the output frequency of the PLL two clock systems are derived:

2.1.2. System Clock

The 40.5 MHz system clock (f_{CPU}) provides the processor, all processor related peripherals, the sync timing logic, the A/D converters, the slicer, the DG and the CLUTs.

It will be possible to use 10.125 MHz (1/4 of 40.5 MHz) for the system clock domain (slow down mode). Moreover the user is able to send the PLL into a power save mode (SFR-bit PLLS = 1).

Before the PLL is switched to power save mode (PLLS = 1), the software has to switch the clock source from 648 MHz PLL-clock to the 20.25 MHz oscillator-clock (SFR bit CLK_src = 1). In this mode the Slicer, Acquisition, DAC and Display Generator are switched off.

To switch back, the software has to end the PLL power save mode (SFR-bit PLLS = 0), reset the PLL for 10 µs (3 machine cycles, SFR bit PLL_res = ‘1’, then ‘0’ again), then wait 150 µs (38 machine cycles) and switch back to the PLL clock (SFR-bit CLK_src = 0).

If Power Down Mode is activated, PLL and Oscillator are send to sleep (SFR bit PDS = 1; refer to Section 2.4.).

Furthermore, there are additional possibilities to disable the clocks for the peripherals. Please refer to Section 2.4.

2.1.3. Pixel Clock

The second clock system is the pixel clock (f_{PIX}), which is programmable in a range from 5 … 38 MHz. It serves the output part of the display FIFO and the D/A converters. The pixel clock is derived from the high frequent output of the PLL and line by line phase shifted to the positive edge of the horizontal sync signal (normal polarity). Because the final display clock is derived from a DTO (digital time oscillator) it has no equidistant clock periods although the average frequency is exact. The pixel clock can also be inserted by an external source which has a fixed and stable phase to an external horizontal sync. This pixel clock generation system has several advantages:

– The frequency of the pixel clock can be programmed independently from the horizontal line period.
– Because the input of the PLL is already a signal with a relative high frequency, the resulting pixel frequency has an extremely low jitter.
– The resulting pixel clock follows the edge of the H-sync impulse without any delay and has always the same quality than the sync timing of the deflection controller.

2.1.4. Register Description

see Section 3.4. on page 6-101

2.2. Microcontroller

2.2.1. Architecture

Every CPU machine cycle consists of 12 internal CPU clock period.

The CPU manipulates operands in two memory spaces: the program memory space, and the data memory space. The program memory address space is provided to accommodate relocatable code.

The data memory address space is divided into the 256-byte internal data RAM, XRAM (extended data memory, accessible with MOVX instructions) and the 128-byte Special Function Register (SFR) address spaces. Four register banks (each bank has eight registers), 128 addressable bits, and the stack reside in the internal data RAM. The stack depth is limited only by the available internal data RAM. Its location is determined by the 8-bit stack pointer. All registers except the program counter and the four 8-register banks reside in the special function register address space. These memory mapped registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, pulse width modulator, capture control unit, watchdog timer, UART, display, acquisition control etc. Many locations in the SFR address space are addressable as bits.

Note: Reading from unused locations within data memory will yield undefined data.

Conditional branches are performed relative to the 16 bit program counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. Sixteen-bit jumps and calls permit branching to any location in the memory address space.

The processor has five methods for addressing source operands: register, direct, register-indirect, immediate, and base register plus index register-indirect addressing.

The first three methods can be used for addressing destination operands. Most instructions have a ‘destination, source’ field that specifies the data type, addressing methods and operands involved. For operations other than moves, the destination operand is also a source operand.

Registers in the four 8-register banks can be accessed through register, direct, or register-indirect addressing; the lower 128 bytes of internal data RAM through direct or register-indirect addressing, the upper 128 bytes of internal data RAM through register-indirect addressing; and the special function registers through direct addressing. Look-up tables resident in program memory can be accessed through base register plus index register-indirect addressing.

2.2.2. CPU-Hardware

2.2.2.1. Instruction Decoder

Each program instruction is decoded by the instruction decoder. This unit generates the internal signals that control the functions of each unit within the CPU section. These signals control the sources and destination of data, as well as the function of the Arithmetic/Logic Unit (ALU).

2.2.2.2. Program Control Section

The program control section controls the sequence in which the instructions stored in program memory are executed. The conditional branch logic enables conditions internal and external to the processor to cause a change in the sequence of program execution. The 16-bit program counter holds the address of the instruction to be executed. It is manipulated with the control transfer instructions listed in Section 2.2.6.

2.2.2.3. Internal Data RAM

The internal data RAM provides a 256-byte scratch pad memory, which includes four register banks and 128 direct addressable software flags. Each register bank contains registers R0 … R7. The addressable flags are located in the 16-byte locations starting at byte address 20_H and ending with byte location $2F_H$ of the RAM address space.

In addition to this standard internal data RAM the processor contains an extended internal RAM. It can be considered as a part of an external data memory. It is referenced by MOVX instructions (MOVX A, @DPTR), the memory organization is explained in Section 2.6.

2.2.2.4. Arithmetic/Logic Unit (ALU)

The arithmetic section of the processor performs many data manipulation functions and includes the Arithmetic/Logic Unit (ALU) and the A-, B- and PSW registers. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations of add, subtract, multiply, divide, increment, decrement, BCD-decimal-add adjust and compare, and the logic operations of and, or, exclusive-or, complement and rotate (right, left, or nibble swap).

The A-register is the accumulator, the B-register is dedicated during multiply and divide and serves as both a source and a destination. During all other operations the B-register is simply another location of the special function register space and may be used for any purpose.

2.2.2.5. Boolean Processor

The Boolean processor is an integral part of the processor architecture. It is an independent bit processor with its own instruction set, its own accumulator (the carry flag) and its own bit-addressable RAM and I/O. The bit manipulation instructions allow the direct addressing of 128 bits within the internal data RAM and several bits within the special function registers. The special function registers which have addresses exactly divisible by eight contain directly addressable bits.

The Boolean processor can perform, on any addressable bit, the bit operations of ‘set’, ‘clear’, ‘complement’, ‘jump-if-set’, ‘jump-if-not-set’, ‘jump-if-set then-clear’ and ‘move to/from carry’. Between any addressable bit (or its complement) and the carry flag it can perform the bit operation of logical AND or logical OR with the result returned to the carry flag.

2.2.2.6. Program Status Word Register (PSW)

The PSW flags record processor status information and control the operation of the processor. The carry (CY), auxiliary carry (AC), two user flags (F0 and F1), register bank select (RS0 and RS1), overflow (OV) and parity (P) flags reside in the program status word register. These flags are bit-memory-mapped within the byte-memory-mapped PSW. The CY, AC, and OV flags generally reflect the status of the latest arithmetic operations. The CY flag is also the Boolean accumulator for bit operations. The P-flag always reflects the parity of the A-register. F0 and F1 are general purpose flags which are pushed onto the stack as part of a PSW save. The two register bank select bits (RS1 and RS0) determine which one of the four register banks is selected as follows:

Table 2–1: Register bank selection

RS1	RS0	Register Bank	Register Location
0	0	0	00_H … 07_H
0	1	1	08_H … $0F_H$
1	0	2	10_H … 17_H
1	1	3	18_H … $1F_H$

2.2.2.7. Stack Pointer (SP)

The 8-bit stack pointer contains the address at which the last byte was pushed onto the stack. This is also the address of the next byte that will be popped. The SP is incremented during a push. SP can be read or written to under software control. The stack may be located anywhere within the internal data RAM address space and may be as large as 256 bytes.

Note: For memory above 64K, memory extension stack is used, refer to Section 2.6.5.

2.2.2.8. Data Pointer Register (DPTR)

The 16-bit Data Pointer Register DPTR is the concatenation of registers DPH (high-order byte) and DPL (low-order byte). The DPTR is used in register-indirect addressing to move program memory constants and to access the extended data memory. DPTR may be manipulated as one 16-bit register or as two independent 8-bit registers DPL and DPH.

Eight data pointer registers are available, the active one is selected by a special function register (DPSEL).

2.2.3. CPU Timing

Timing generation is completely self-contained, except for the frequency reference which can be a crystal or external clock source. The on-board oscillator is a parallel anti-resonant circuit. The XTAL2 pin is the output of a high-gain amplifier, while XTAL1 is its input. A crystal connected between XTAL1 and XTAL2 provides the feedback and phase shift required for oscillation.

In slowdown mode, processor runs at one fourth the normal frequency. This mode is useful when power consumption needs to be reduced. Slow down mode is entered by setting the bit SD in PCON register.

Note: Any Slow-down mode should only be used if teletext reception and the display are disabled. Otherwise processing of the incoming text data might be incomplete and the display structure will be corrupted. For disabling acquisition and display generator refer to Section 2.4..

2.2.4. Addressing Modes

There are five general addressing modes operating on bytes. One of these five addressing modes, however, operates on both bytes and bits:

– Register
– Direct (both bytes and bits)
– Register-indirect
– Immediate
– Base register plus index-register indirect

The following list summarizes, which memory spaces may be accessed by each of the addressing modes:

Register Addressing

R0 … R7
ACC, B, CY (bit), DPTR

Direct Addressing

RAM (low part)
Special Function Registers

Register-indirect Addressing

RAM (@R1, @R0, SP)

Immediate Addressing

Program Memory

Base Register plus Index-Register Indirect Addressing

Program Memory (@DPTR + A, @PC + A)

2.2.4.1. Register Addressing

Register addressing accesses the eight working registers (R0 … R7) of the selected register bank. The PSW register flags RS1 and RS0 determine which register bank is enabled. The least significant three bits of the instruction opcode indicate which register is to be used. ACC, B, DPTR and CY, the Boolean processor accumulator, can also be addressed as registers.

2.2.4.2. Direct Addressing

Direct byte addressing specifies an on-chip RAM location (only low part) or a special function register. Direct addressing is the only method of accessing the special function registers. An additional byte is appended to the instruction opcode to provide the memory location address. The highest-order bit of this byte selects one of two groups of addresses: values between 00_H … $7F_H$ access internal RAM locations, while values between 80_H … $0FF_H$ access one of the special function registers.

2.2.4.3. Register-Indirect Addressing

Register-indirect addressing uses the contents of either R0 or R1 (in the selected register bank) as a pointer to locations in the 256 bytes of internal RAM. Note that the special function registers are not accessible by this method.

Execution of PUSH and POP instructions also use register-indirect addressing. The stack pointer may reside anywhere in internal RAM.

2.2.4.4. Immediate Addressing

Immediate addressing allows constants to be part of the opcode instruction in program memory.

An additional byte is appended to the instruction to hold the source variable. In the assembly language and instruction set, a number sign (#) precedes the value to be used, which may refer to a constant, an expression, or a symbolic name.

2.2.4.5. Base Register plus Index Register-Indirect Addressing

Base register plus index register-indirect addressing allows a byte to be accessed from program memory via an indirect move from the location whose address is the sum of a base register (DPTR or PC) and index register, ACC. This mode facilitates accessing to look-up table resident in program memory.

2.2.5. Ports and I/O-Pins

There are three 8-bit ports P1, P2, and P3 available. Each pin can be individually and independently programmed as input or output and each can be configured dynamically. 4 pins of P1 can be used as analog input.

An instruction that uses a port's bit/byte as a source operand reads a value that is the logical AND of the last value written to the bit/byte and the polarity being applied to the pin/pins by an external device (this assumes that none of the processor's electrical specifications are being violated). An instruction that reads a bit/byte, operates on the content, and writes the result back to the bit/byte, reads the last value written to the bit/byte instead of the logic level at the pin/pins. Pins comprising a single port can be made a mixed collection of inputs and outputs by writing a ‘one’ to each pin that is to be an input. Each time an instruction uses a port as the destination, the operation must write ‘ones’ to those bits that correspond to the input pins. An input to a port pin needs not to be synchronized to the oscillator.

All the port latches have ‘one’ s written to them by the reset function. If a ‘zero’ is subsequently written to a port latch, it can be reconfigured as an input by writing a ‘one’ to it.

The instructions that perform a read of, operation on, and write to a port’s bit/byte are INC, DEC, CPL, JBC, SETB, CLR, MOV P.X, CJNE, DJNZ, ANL, ORL, and XRL. The source read by these operations is the last value that was written to the port, without regard to the levels being applied at the pins. This insures that bits written to a ‘one’ (for use as inputs) are not inadvertently cleared.

Port 0 has an open-drain output. Writing a ‘one’ to the bit latch leaves the output transistor off, so the pin floats.

In that condition it can be used as a high-impedance input. Port 0 is considered ‘true bidirectional’, because when configured as an input it floats.

Ports 1, 3 and 4 have ‘quasi-bidirectional’ output drivers.

In ports P1, P3 and P4 the output drivers provide source current for one system clock period if, and only if, software updates the bit in the output latch from a ‘zero’ to an ‘one’. Sourcing current only on ‘zero to one’ transition prevents a pin, programmed as an input, from sourcing current into the external device that is driving the input pin.

Secondary functions can be selected individually and independently for the pins of Port 1 and 3. Further information on Port 1's secondary functions is given in Section 2.11.. P3 generates the secondary control signals automatically as long as the pin corresponding to the appropriate signal is programmed as an input, i. e. if the corresponding bit latch in the P3 special function register contains a ‘one’.

Read Modify-Write Feature

‘Read-modify-write’ commands are instructions that read a value, possibly change it, and then rewrite it to the latch. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin. The read-modify-write instructions are listed in Table 2–2.

The read-modify-write instructions are directed to the latch rather than the pin in order to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. When a ‘one’ is written to the bit, the transistor is turned on.

If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of ‘one’.

Timer/Counter 0 Mode 3: Two 8-Bit Counters

Table 2–2: Read-Modify-Write Instructions

Mnemonic	Description	Example
ANL	logical AND	ANL P1, A
ORL	logical OR	ORL P2, A
XRL	logical EX – OR	XRL P3, A
JBC	jump if bit = 1 and clear bit	JBC P1.1, LABEL
CPL	complement bit	CPL P3.0
INC	increment	INC P1
DEC	decrement	DEC P1
DJNZ	decrement and jump if not zero	DJNZ P3, LABEL
MOV PX.Y, C[1)]	move carry bit to bit Y of Port X	MOV P1.7, C
CLR PX.Y[1)]	clear bit Y of Port X	CLR P2.6
SET PX.Y[1)]	set bit Y of Port X	SET P3.5

1) Instruction reads the port byte (all 8 bits), modifies the addressed bit, then writes the new byte back to the latch.

2.2.6. Instruction Set

The assembly language uses the same instruction set and the same instruction opcodes as the 8051 microcomputer family.

2.2.6.1. Notes on Data Addressing Modes

Rn – Working register R0 - R7.

direct – 128 internal RAM-locations, any I/O-port, control or status register.

@Ri – Indirect internal RAM-location addressed by register R0 or R1.

#data – 8-bit constant included in instruction.

#data 16 – 16-bit constant included as bytes 2 & 3 of instruction.

bit – 128 software flags, any I/O-pin, control or status bit in special function registers.

Operations working on external data memory (MOVX …) are used to access the extended internal data RAM (XRAM).

2.2.6.2. Notes on Program Addressing Modes

addr 16 – Destination address for LCALL & LJMP may be anywhere within the program memory address space.

addr 11 – Destination address for ACALL & AJMP will be within the same 2 KB of the following instruction.

rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/-128 bytes relative to first byte of the following instruction.

2.2.6.3. Instruction Set Description

Table 2–3: Arithmetic Operations

Mnemonic		Description	Byte
ADD	**A, Rn**	Add register to Accumulator	1
ADD	**A, direct**	Add direct byte to Accumulator	2
ADD	**A, @Ri**	Add indirect RAM to Accumulator	1
ADD	**A, #data**	Add immediate data to Accumulator	2
ADDC	**A, Rn**	Add register to Accumulator with Carry flag	1
ADDC	**A, direct**	Add direct byte to A with Carry flag	2
ADDC	**A, @Ri**	Add indirect RAM to A with Carry flag	1
ADDC	**A, #data**	Add immediate data to A with Carry flag	2
SUBB	**A, Rn**	Subtract register from A with Borrow	1
SUBB	**A, direct**	Subtract direct byte from A with Borrow	2
SUBB	**A, @Ri**	Subtract indirect RAM from A with Borrow	1
SUBB	**A, #data**	Subtract immediate data from A with Borrow	2
INC	**A**	Increment Accumulator	1
INC	**Rn**	Increment register	1
INC	**direct**	Increment direct byte	2
INC	**@Ri**	Increment indirect RAM	1
DEC	**A**	Decrement Accumulator	1
DEC	**Rn**	Decrement register	1
DEC	**direct**	Decrement direct byte	2
DEC	**@Ri**	Decrement indirect RAM	1
INC	**DPTR**	Increment Data Pointer	1
MUL	**AB**	Multiply A & B	1
DIV	**AB**	Divide A & B	1
DA	**A**	Decimal Adjust Accumulator	1

Table 2–4: Logical Operations

Mnemonic		Description	Byte
ANL	**A, Rn**	AND register to Accumulator	1
ANL	**A, direct**	AND direct byte to Accumulator	2
ANL	**A, @Ri**	AND indirect RAM to Accumulator	1
ANL	**A, #data**	AND immediate data to Accumulator	2
ANL	**direct, A**	AND Accumulator to direct byte	2
ANL	**direct, #data**	AND immediate data to direct byte	3
ORL	**A, Rn**	OR register to Accumulator	1
ORL	**A, direct**	OR direct byte to Accumulator	2
ORL	**A, @Ri**	OR indirect RAM to Accumulator	1
ORL	**A, #data**	OR immediate data to Accumulator	2
ORL	**direct, A**	OR Accumulator to direct byte	2
ORL	**direct, #data**	OR immediate data to direct byte	3
XRL	**A, Rn**	Exclusive-OR register to Accumulator	1
XRL	**A, direct**	Exclusive-OR direct byte to Accumulator	2
XRL	**A, @Ri**	Exclusive-OR indirect RAM to Accumulator	1
XRL	**A, #data**	Exclusive-OR immediate data to Accumulator	2
XRL	**direct, A**	Exclusive-OR Accumulator to direct byte	2
XRL	**direct, #data**	Exclusive-OR immediate data to direct	3
CLR	**A**	Clear Accumulator	1
CPL	**A**	Complement Accumulator	1
RL	**A**	Rotate Accumulator left	1
RLC	**A**	Rotate A left through the Carry flag	1
RR	**A**	Rotate Accumulator right	1
RRC	**A**	Rotate A right through Carry flag	1
SWAP	**A**	Swap nibbles within the Accumulator	1

Table 2–5: Data Transfer Operations

Mnemonic		Description	Byte
MOV	**A, Rn**	Move register to Accumulator	1
MOV	**A, direct**	Move direct byte to Accumulator	2
MOV	**A, @Ri**	Move indirect RAM to Accumulator	1
MOV	**A, #data**	Move immediate data to Accumulator	2
MOV	**Rn, A**	Move Accumulator to register	1
MOV	**Rn, direct**	Move direct byte to register	2
MOV	**Rn, #data**	Move immediate data to register	2
MOV	**direct, A**	Move Accumulator to direct byte	2
MOV	**direct, Rn**	Move register to direct byte	2
MOV	**direct, direct**	Move direct byte to direct	3
MOV	**direct, @Ri**	Move indirect RAM to direct byte	2
MOV	**direct, #data**	Move immediate data to direct byte	3
MOV	**@Ri, A**	Move Accumulator to indirect RAM	1
MOV	**@Ri, direct**	Move direct byte to indirect RAM	2
MOV	**@Ri, #data**	Move immediate data to indirect RAM	2
MOV	**DPTR, #data 16**	Load Data Pointer with a 16-bit constant	3
MOVC	**A@A + DPTR**	Move Code byte relative to DPTR to Accumulator	1
MOVC	**A@A + PC**	Move Code byte relative to PC to Accumulator	1
MOVX	**A, @Ri**	Move External RAM (8-bit addr) to Accumulator[1)]	1
MOVX	**A, @DPTR**	Move External RAM (16-bit addr) to Accumulator	1
MOVX	**@Ri, A**	Move A to External RAM (8-bit addr)[1)]	1
MOVX	**@DPTR, A**	Move A to External RAM (16-bit addr)	1
PUSH	**direct**	Push direct byte onto stack	2
POP	**direct**	Pop direct byte from stack	2
XCH	**A, Rn**	Exchange register with Accumulator	1
XCH	**A, direct**	Exchange direct byte with Accumulator	2
XCH	**A, @Ri**	Exchange indirect RAM with Accumulator	1
XCHD	**A, @Ri**	Exchange low-order digital indirect RAM with A[1)]	1

1) **not applicable**

Table 2–6: Boolean Variable Manipulation

Mnemonic		Description	Byte
CLR	**C**	Clear Carry flag	1
CLR	**bit**	Clear direct bit	2
SETB	**C**	Set Carry flag	1
SETB	**bit**	Set direct bit	2
CPL	**C**	Complement Carry flag	1
CPL	**bit**	Complement direct bit	2
ANL	**C, bit**	AND direct bit to Carry flag	2
ANL	**C, /bit**	AND complement of direct bit to Carry	2
ORL	**C, bit**	OR direct bit to Carry flag	2
ORL	**C, /bit**	OR complement of direct bit to Carry	2
MOV	**C, bit**	Move direct bit to Carry flag	2
MOV	**bit, C**	Move Carry flag to direct bit	2

Table 2–7: Program and Machine Control Operations

Mnemonic		Description	Byte
ACALL	**addr 11**	Absolute subroutine call	2
LCALL	**addr 16**	Long subroutine call	3
RET		Return from subroutine	1
RETI		Return from interrupt	1
AJMP	**addr 11**	Absolute jump	2
LJMP	**addr 16**	Long jump	3
SJMP	**rel**	Short jump (relative addr)	2
JMP	**@A + DPTR**	Jump indirect relative to the DPTR	1
JZ	**rel**	Jump if Accumulator is zero	2
JNZ	**rel**	Jump if Accumulator is not zero	2
JC	**rel**	Jump if Carry flag is set	2
JNC	**rel**	Jump if Carry flag is not set	2
JB	**bit, rel**	Jump if direct bit set	3
JNB	**bit, rel**	Jump if direct bit not set	3
JBC	**bit, rel**	Jump if direct bit is set and clear bit	3
CJNE	**A, direct rel**	Compare direct to A and jump if not equal	3
CJNE	**A, #data, rel**	Compare immediate to A and jump if not equal	3
CJNE	**Rn, #data, rel**	Compare immediate to register and jump if not equal	3
CJNE	**@Ri, #data, rel**	Compare immediate to indirect and jump if not equal	3
DJNZ	**Rn, rel**	Decrement register and jump if not zero	2
DJNZ	**direct, rel**	Decrement direct and jump if not zero	3
NOP		No operation	1

2.2.6.4. Instruction Opcodes in Hexadecimal Order

Table 2–8: Instruction Opcodes

Code	Byte	Mnemo	Operands
00	1	NOP	–
01	2	AJMP	code addr
02	3	LJMP	code addr
03	1	RR	A
04	1	INC	A
05	2	INC	data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	bit addr, code addr
11	2	ACALL	code addr
12	3	LCALL	code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	bit addr, code addr
21	2	AJMP	code addr
22	1	RET	–
23	1	RL	A
24	2	ADD	A, #data

Table 2–8: Instruction Opcodes, continued

Code	Byte	Mnemo	Operands
25	2	ADD	A, data addr
26	1	ADD	A, @R0
27	1	ADD	A, @R1
28	1	ADD	A, R0
29	1	ADD	A, R1
2A	1	ADD	A, R2
2B	1	ADD	A, R3
2C	1	ADD	A, R4
2D	1	ADD	A, R5
2E	1	ADD	A, R6
2F	1	ADD	A, R7
30	3	JNB	bit addr, code addr
31	2	ACALL	code addr
32	1	RETI	–
33	1	RLC	A
34	2	ADDC	A, #data
35	2	ADDC	A, data addr
36	1	ADDC	A, @R0
37	1	ADDC	A, @R1
38	1	ADDC	A, R0
39	1	ADDC	A, R1
3A	1	ADDC	A, R2
3B	1	ADDC	A, R3
3C	1	ADDC	A, R4
3D	1	ADDC	A, R5
3E	1	ADDC	A, R6
3F	1	ADDC	A, R7
40	2	JC	code addr
41	2	AJMP	code addr
42	2	ORL	data addr., A
43	3	ORL	data addr, #data
44	2	ORL	A, #data
45	2	ORL	A, data addr
46	1	ORL	A, @R0
47	1	ORL	A, @R1
48	1	ORL	A, R0
49	1	ORL	A, R1

Table 2–8: Instruction Opcodes, continued

Code	Byte	Mnemo	Operands
4A	1	ORL	A, R2
4B	1	ORL	A, R3
4C	1	ORL	A, R4
4D	1	ORL	A, R5
4E	1	ORL	A, R6
4F	1	ORL	A, R7
50	2	JNC	code addr
51	2	ACALL	code addr
52	2	ANL	data addr, A
53	3	ANL	data addr, #data
54	2	ANL	A, #data
55	2	ANL	A, data addr
56	1	ANL	A, @R0
57	1	ANL	A, @R1
58	1	ANL	A, R0
59	1	ANL	A, R1
5A	1	ANL	A, R2
5B	1	ANL	A, R3
5C	1	ANL	A, R4
5D	1	ANL	A, R5
5E	1	ANL	A, R6
5F	1	ANL	A, R7
60	2	JZ	code addr
61	2	AJMP	code addr.
62	2	XRL	data addr, A
63	3	XRL	data addr, #data
64	2	XRL	A, #data
65	2	XRL	A, data addr
66	1	XRL	A, @R0
67	1	XRL	A, @R1
68	1	XRL	A, R0
69	1	XRL	A, R1
6A	1	XRL	A, R2
6B	1	XRL	A, R3
6C	1	XRL	A, R4
6D	1	XRL	A, R5
6E	1	XRL	A, R6
6F	1	XRL	A, R7

Table 2–8: Instruction Opcodes, continued

Code	Byte	Mnemo	Operands
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	ORL	C, bit addr
73	1	JMP	@A + DPTR
74	2	MOV	A, #data
75	3	MOV	data addr, #data
76	2	MOV	@R0, #data
77	2	MOV	@R1, #data
78	2	MOV	R0, #data
79	2	MOV	R1, #data
7A	2	MOV	R2, #data
7B	2	MOV	R3, #data
7C	2	MOV	R4, #data
7D	2	MOV	R5, #data
7E	2	MOV	R6, #data
7F	2	MOV	R7, #data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C, bit addr
83	1	MOVC	A, @A + PC
84	1	DIV	AB
85	3	MOV	data addr, data addr
86	2	MOV	data addr, @R0
87	2	MOV	data addr, @R1
88	2	MOV	data addr, R0
89	2	MOV	data addr, R1
8A	2	MOV	data addr, R2
8B	2	MOV	data addr, R3
8C	2	MOV	data addr, R4
8D	2	MOV	data addr, R5
8E	2	MOV	data addr, R6
8F	2	MOV	data addr, R7
90	3	MOV	DPTR, #data 16
91	2	ACALL	code addr
92	2	MOV	bit addr, C
93	1	MOVC	A, @A + DPTR
94	2	SUBB	A, #data
95	2	SUBB	A, data addr

Table 2–8: Instruction Opcodes, continued

Code	Byte	Mnemo	Operands
96	1	SUBB	A, @R0
97	1	SUBB	A, @R1
98	1	SUBB	A, R0
99	1	SUBB	A, R1
9A	1	SUBB	A, R2
9B	1	SUBB	A, R3
9C	1	SUBB	A, R4
9D	1	SUBB	A, R5
9E	1	SUBB	A, R6
9F	1	SUBB	A, R7
A0	2	ORL	C, /bit addr
A1	2	AJMP	code addr
A2	2	MOV	C, bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5	–	reserved	–
A6	2	MOV	@R0, data addr
A7	2	MOV	@R1, data addr
A8	2	MOV	R0, data addr
A9	2	MOV	R1, data addr
AA	2	MOV	R2, data addr
AB	2	MOV	R3, data addr
AC	2	MOV	R4, data addr
AD	2	MOV	R5, data addr
AE	2	MOV	R6, data addr
AF	2	MOV	R7, data addr
B0	2	ANL	C, /bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A, #data, code addr
B5	3	CJNE	A, data addr, code addr
B6	3	CJNE	@R0, #data, code addr
B7	3	CJNE	@R1, #data, code addr
B8	3	CJNE	R0, #data, code addr
B9	3	CJNE	R1, #data, code addr
BA	3	CJNE	R2, #data, code addr
BB	3	CJNE	R3, #data, code addr

Table 2–8: Instruction Opcodes, continued

Code	Byte	Mnemo	Operands
BC	3	CJNE	R4, #data, code addr
BD	3	CJNE	R5, #data, code addr
BE	3	CJNE	R6, #data, code addr
BF	3	CJNE	R7, #data, code addr
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A, data addr
C6	1	XCH	A, @R0
C7	1	XCH	A, @R1
C8	1	XCH	A, R0
C9	1	XCH	A, R1
CA	1	XCH	A, R2
CB	1	XCH	A, R3
CC	1	XCH	A, R4
CD	1	XCH	A, R5
CE	1	XCH	A, R6
CF	1	XCH	A, R7
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	data addr, code addr
D6	–	–	–
D7	–	–	–
D8	2	DJNZ	R0, code addr
D9	2	DJNZ	R1, code addr
DA	2	DJNZ	R2, code addr
DB	2	DJNZ	R3, code addr
DC	2	DJNZ	R4, code addr
DD	2	DJNZ	R5, code addr
DE	2	DJNZ	R6, code addr
DF	2	DJNZ	R7, code addr
E0	1	MOVX	A, @DPTR
E1	2	AJMP	code addr

Table 2–8: Instruction Opcodes, continued

Code	Byte	Mnemo	Operands
E2	–	–	–
E3	–	–	–
E4	1	CLR	A
E5	2	MOV	A, data addr
E6	1	MOV	A, @R0
E7	1	MOV	A, @R1
E8	1	MOV	A, R0
E9	1	MOV	A, R1
EA	1	MOV	A, R2
EB	1	MOV	A, R3
EC	1	MOV	A, R4
ED	1	MOV	A, R5
EE	1	MOV	A, R6
EF	1	MOV	A, R7
F0	1	MOVX	@DPTR, A
F1	2	ACALL	code addr
F2	–	–	–
F3	–	–	–
F4	1	CPL	A
F5	2	MOV	data addr, A
F6	1	MOV	@R0, A
F7	1	MOV	@R1, A
F8	1	MOV	R0, A
F9	1	MOV	R1, A
FA	1	MOV	R2, A
FB	1	MOV	R3, A
FC	1	MOV	R4, A
FD	1	MOV	R5, A
FE	1	MOV	R6, A
FF	1	MOV	R7, A

2.3. Interrupts

2.3.1. Interrupt System

External events and the real-time on-chip peripherals require CPU service asynchronous to the execution of any particular section of code. To couple the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, four-priority-level, nested interrupt system is provided.

2.3.2. Interrupt Sources

The TVT processor is capable of handling 24 interrupt sources. Two external sources via the INT0 and INT1 pins and two additional external interrupts INTX0 and INTX1 are provided. Peripherals also use interrupts. One from each of the two internal counters, one from the analog-to-digital converter and one from UART. In addition there are four acquisition related interrupts, two display related interrupts and one interrupt indicating change of channel, two interrupts are generated by WDT and PWM overflow in timer mode.

Timer 0 and Timer 1 interrupts are generated by TCON.TF0 and TCON.TF1 following a rollover in their respective registers (except in Mode 3 when TCON.TH0 controls the Timer 1 interrupt).

The external interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are either level or edge triggered depending on bits in TCON and IRCON. Other external interrupts are level sensitive and active high. Any edge triggering will need to be taken care of by individual peripherals.

$\overline{\text{INTX0}}$ and $\overline{\text{INTX1}}$ can be programed to be either negative or positive edge triggered.

The analog digital converter interrupt is generated on completion of the analog digital conversion.

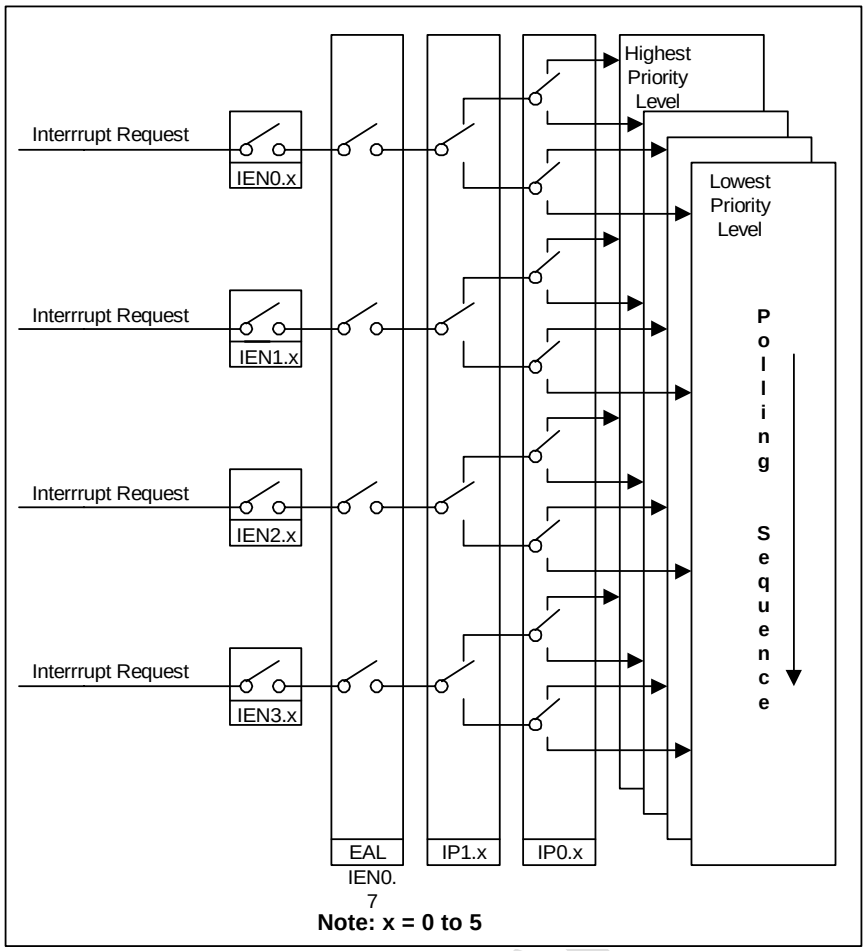


Fig. 2–2: Interrupt handling overview

2.3.3. Enabling Interrupts

Interrupts are enabled through a set of Interrupt Enable registers (IEN0, IEN1, IEN2, IEN3).

Bits 0 to 5 of the Interrupt Enable registers each individually enable/disable a particular interrupt source. Overall control is provided by bit 7 of IEN0 (EAL). When EAL is set to '0', all interrupts are disabled: when EAL is set to '1', interrupts are individually enabled or disabled through the other bits of the Interrupt Enable Registers. EAL may however be overridden by the DISINT signal which provides a global disable signal for the interrupt controller.

2.3.3.1. Interrupt Enable Registers (IEN0, IEN1, IEN2, IEN3)

The processor has 4 Interrupt Enable registers.The details of the registers are as follows. For each bit in these registers, a 1 enables the corresponding interrupt and a 0 disables it.

2.3.4. Interrupt Source Registers

All the interrupts except for timer 0, timer 1, external interrupt 0, external interrupt 1, external extra interrupt 0 and external extra interrupt 1 are generated by the respective blocks and are positive edge triggered. They are sampled in a central interrupt source register, corresponding bit must be cleared by the software after entering the interrupt service routine.

2.3.5. Interrupt Priority

For the purposes of assigning priority, the 24 possible interrupt sources are divided into groups determined by their bit position in the Interrupt Enable Registers and their respective requests are scanned in the order shown below.

Each interrupt group may individually be assigned to one of four priority levels by writing to the IP0 and IP1 Interrupt Priority registers at the corresponding bit position.

An interrupt service routine can only be interrupted by an interrupt of higher priority level. If two interrupts of different priority occur at the same time, the higher level interrupt will be serviced first.

If two interrupts of the same priority level occur simultaneously, the order in which the interrupts are serviced is determined by the scan order shown below ????.

2.3.5.1. Interrupt Priority Registers (IP0 IP1)

The Interrupt Priority registers are structured as follows.

2.3.6. Interrupt Vectors

When an interrupt is serviced, a long call instruction is executed to one of the locations listed in Table 2–9.

2.3.7. Interrupt and Memory Extension

When an interrupt occurs, the Memory Management Unit (MMU) carries out the following sequence of actions:

1. The MEX1 register bits are made available on SDATAO [7:0].
2. The MEXSP register bits are made available on SADD[7:0].
3. The Stack read and write signals are set for a write operation.
4. A write is performed to External memory.
5. The MEXSP Stack Pointer is incremented.
6. The Interrupt Bank bits IB19 - IB16 (MEX2.3 - MEX2.0) are copied to both the NB19 - NB16 and the CB19 - CB16 bits in the MEX1.

Then on return from the interrupt service routine:

1. The MEXSP Stack Pointer is decremented.
2. The MEXSP register bits are made available on SADD [7:0].
3. The Stack read and write signals are set for a read operation.
4. A read is performed on External memory.
5. SDATAI [7:0] is copied to the MEX1 register.

This action allows the user to place interrupt service routines on specific banks.

2.3.8. Interrupt Handling

External interrupt 0, external interrupt 1, timer 0, timer 1 and UART interrupt are handled as following.

Interrupts are sampled at S5P2 in each machine cycle and the sampled interrupts polled during the following machine cycle. If an interrupt is set when it is sampled, it will be serviced provided:

– An interrupt of an equal or higher priority is not currently being serviced
– The polling cycle is not the final cycle of a multi-cycle instruction, and
– The current instruction is neither a RETI nor a write either to one of Interrupt Enable registers or to one of the Interrupt Priority registers.

Note: Active interrupts are only stored for one machine cycle. As a result, if an interrupt was active for one or more polling cycles but not serviced for one of the reasons given above, the interrupt will not be serviced.

For all other interrupts interrupt request is stored as an interrupt flag in CISR0 and CISR1. These request bits must be cleared by software while servicing the interrupt. These interrupts always gets serviced once raised regardless of number of polling cycles required to service them.

The rest of the functionality with regards to sampling from controller and requirements to start the service are same as discussed above.

2.3.9. Interrupt Latency

The response time in a single interrupt system is between 3 and 9 machine cycles.

2.3.10. Interrupt Flag Clear

In case of external interrupt 0 and external interrupt 1, If the external interrupts are edge triggered, the interrupt flag is cleared on vectoring to the service routine but if they are level triggered, the flag is controlled by the external signal. Timer/counter flags are cleared on vectoring to the interrupt service routine. All other interrupt flag, including external extra interrupt 0 and 1 are not cleared by hardware. They must be cleared by software.

2.3.11. Interrupt Return

For the proper operation of the interrupt controller. It is necessary that all interrupt routines end with a RETI instruction.

Table 2–9: Interrupt vectors

Interrupt Source		Vector Address (hex)	Interrupt Enable Flag		Interrupt Request Flag		Group
#	Name		Register	Bit	Register	Bit	
0	External Interrupt 0	0003	IEN0	EX0	TCON	IE0	0
1	Timer 0 Overflow	000B	IEN0	ET0	TCON	TF0	1
2	External Interrupt 1	0013	IEN0	EX1	TCON	IE1	2
3	Timer 1 Overflow	001B	IEN0	ET1	TCON	TF1	3
4	UART	0023	IEN0	EU	SCON	R1 and T1	4
5	CADC	002B	IEN0	EAD	CISR0	ADC	5
6	MSP	0033	IEN1	EMSP	CISR1	MSP	0
7	External X Interrupt 0	003B	IEN1	EXX0	CISR1	IEX0	1
8	Watchdog Timer	0043	IEN1	EWT	CISR0	WTmr	2
9	External X Interrupt 1	004B	IEN1	EXX1	CISR1	IEX1	3
10	Acquisition V-Sync	0053	IEN1	EAV	CISR0	AVS	4
11	Display V-Sync	005B	IEN1	EDV	CISR0	DVS	5
12	RTC	0063	IEN2	ERTC	CISR1	RTC	0
13	reserved	006B	IEN2	bit1	-	-	1
14	not implemented	0073	-	-	-	-	-
15	Voltage Supervision	007B	NMI	NMIEN	-	-	-
16	PWM Timer	0083	IEN2	EPW	CISR0	PWtmr	2
17	Channel Change	008B	IEN2	ECC	CISR1	CC	3
18	Acquisition H-Sync	0093	IEN2	EAH	CISR0	AHS	4
19	Display H-Sync	009B	IEN2	EDH	CISR0	DHS	5
20	reserved	00A3	IEN3	bit0	-	-	0
21	reserved	00AB	IEN3	bit1	-	-	1
22	I2C	00B3	IEN3	EI2C	CISR1	I2C	2
23	Softscroll	00BB	IEN3	ESS	CISR1	SS	3
24	Line 24 Start	00C3	IEN3	E24	CISR0	L24	4
25	CADC Wake up	00CB	IEN3	EADW	CISR1	ADW	5

2.3.12. Interrupt Nesting

The process whereby a higher-level interrupt request interrupts a lower-level interrupt service program is called nesting. In this case the address of the next instruction in the lower-priority service program is pushed onto the stack, the stack pointer is incremented by two and processor control is transferred to the program memory location of the first instruction of the higher-level service program. The last instruction of the higher-priority interrupt service program must be a RETI-instruction. This instruction clears the higher 'priority-level-active' flip-flop. RETI also returns processor control to the next instruction of the lower-level interrupt service program. Since the lower 'priority-level-active' flip-flop has remained set, higher priority interrupts are re-enabled while further lower-priority interrupts remain disabled.

2.3.13. External Interrupts

The external interrupt request inputs ($\overline{\text{NINT0}}$ and $\overline{\text{NINT1}}$) can be programmed for either transition- activated or level-activated operation. Control of the external interrupts is provided in the TCON register.

2.3.14. Extension of Standard 8051 Interrupt Logic

For more flexibility, the TVT provides a new feature in detection EX0 and EX1 in edge-triggered mode. Now, there is the possibility to trigger an interrupt on the falling and / or rising edge at the dedicated INTX0 and INTX1 port pin. In order to use this feature respective IT0 and IT1 bits in the TCON register must be set to activate edge triggering mode. Table 2–10 shows combination for Interrupt 0, however description is true for interrupt 1 also.

Table 2–10: Extension of standard 8051 interrupt logic

IT0	EX0R	EX0F	Interrupt
0	0	0	Disabled
0	0	1	Low level
0	1	0	High level
0	1	1	Disabled
1	0	0	Disabled
1	0	1	Negative edge triggered

Table 2–10: Extension of standard 8051 interrupt logic, continued

IT0	EX0R	EX0F	Interrupt
1	1	0	Positive edge triggered
1	1	1	Positive and negative edge triggered

Note: For Development: In order to implement the edge triggering functionality, IT0 and IT1 are mirrored outside the core.

Note: If both EXxR and EXxF are set both rising and falling edges would generate interrupt. Minimum delay between the interrupts should be ensured by the software. If both the EXxR and EXxF are reset to 0, interrupt is disabled.
External extra interrupts EX1 and EX2 are edge triggered interrupts only.
When int0 or int1 is used together with capture reload timer, it is possible to generate interrupt through CRT. For further details refer to Section 2.10.

Please refer to register bits Intsrc0 and Intsrc1 for further description of external interrupt (0 and 1) source selection.

2.3.15. Interrupt Task Function

The processor records the active priority level(s) by setting internal flip-flop(s). Each interrupt level has its own flip-flop. The flip-flop corresponding to the interrupt level being serviced is reset when the processor executes a RETI-instruction.

The sequence of events for an interrupt is

– A source provokes an interrupt by setting its associated interrupt request bit to let the processor know an interrupt condition has occurred.

– The interrupt request is conditioned by bits in the interrupt enable and interrupt priority registers.

– The processor acknowledges the interrupt by setting one of the four internal 'priority-level active' flip-flops and performing a hardware subroutine call. This call pushes the PC (but not the PSW) onto the stack and, for some sources, clears the interrupt request flag.

– The service program is executed.

– Control is returned to the main program when the RETI-instruction is executed. The RETI- instruction

also clears one of the internal ‘priority-level active’ flip-flops.

The interrupt request flags IE0, IE1, TF0 and TF1 are cleared when the processor transfers control to the first instruction of the interrupt service program.

2.4. Power Saving Modes

The controller provides four modes in which power consumption can be significantly reduced.

– Idle mode: The CPU is gated off from the oscillator. All peripherals except WDT (in watch dog mode) are still provided with the clock and are able to work.
– Power-down mode: Operation of the controller is turned off. This mode is used to save the contents of internal RAM with a very low standby current.
– Power-save mode: In this mode Display Generator, Slicer, CADC, CADC_wakeup, PWM, CRT, WDT, OSD-DAC and PLL can individually be turned off.
– Slow-down mode: In this mode the CPU clock frequency is divided by 4.

All modes are entered by software. Special function register is used to enter one of these modes.

2.4.1. Power-Save Mode Registers

2.4.2. Idle Mode

Entering the idle mode is done by two consecutive instructions immediately following each other. The first instruction has to set bit IDLE (PCON.0) and must not set bit IDLS (PCON.5). The following instruction has to set bit IDLS (PCON.5) and must not set bit IDLE (PCON.0). Bits IDLE and IDLS will automatically be cleared after having been set. This double-instruction sequence is implemented to minimize the chance of unintentionally entering the idle mode. The following instruction sequence may serve as an example:

ORL PCON,#00000001_B ;Set bit IDLE, bit IDLS must not be set.

ORL PCON,#00100000_B ;Set bit IDLS, bit IDLE must not be set.

The instruction that sets bit IDLS is the last instruction executed before going into idle mode.

Concurrent setting of the enable and the start bits does **not** set the device into the respective power saving mode.

The idle mode can be terminated by activation of any enabled interrupt (or a hardware reset). The CPU-operation is resumed, the interrupt will be serviced and the next instruction to be executed after RETI-instruction will be the one following the instruction that set the bit IDLS. The port state and the contents of SFRs are held during idle mode.

Entering idle mode disables Slicer, Display, CADC and OSD-DAC. However note that CADC Wake up unit is still operational. Leaving idle mode brings them to their original power save configuration (See Section 2.4.4.).

2.4.3. Power-Down Mode

Entering the power-down mode is done by two consecutive instructions immediately following each other. The first instruction has to set bit PDE (PCON.1) and must not set bit PDS (PCON.6). The following instruction has to set bit PDS (PCON.6) and must not set bit PDE (PCON.1). Bits PDE and PDS will automatically be cleared after having been set.

This double-instruction sequence is implemented to minimize the chance of unintentionally entering the power-down mode. The following instruction sequence may serve as an example:

ORL PCON,#00000010_B ;Set bit PDE, bit PDS must not be set.

ORL PCON,#01000000_B ;Set bit PDS, bit PDE must not be set.

The instruction that sets bit PDS is the last instruction executed before going into power-down mode.

Concurrent setting of the enable and the start bits does **not** set the device into the respective power saving mode.

If idle mode and power-down mode are invoked simultaneously, the power-down mode takes precedence.

The only exit from power-down mode is a hardware reset. The reset will redefine all SFRs, but will not change the contents of internal RAM.

2.4.4. Power-Save Mode

Bits in the PSave register individually enable and disable different major blocks in the TVT.

Note: Power-save mode is independent of Idle and power-down mode. In case of idle mode, blocks which are in power save mode remains in power-save mode.

Entering the power down mode with power-save mode is possible. However leaving the power down mode (reset) would initialize all the power save register bits.

Note: Power-save mode has a higher priority then idle mode.

2.4.5. Slow-Down Mode

Setting the SD bit in PCON register divides the system frequency by 4. During the normal operation TVT is running with 40.5 MHz and in SD mode TVT runs with 10.125 MHz. In slow-down mode Slicer and Display Generator are disabled regardless of power-save mode or other modes. All the pending request to the bus by these blocks are masked off. Leaving slow-down mode restores the original status of these blocks.

2.5. Reset

2.5.1. Reset Sources

TVT can be reset by two sources.

1. Externally by pulling down the reset pin RESETQ.
2. Internally by Watch dog timer reset.

Note: Both reset signals use the same path however Watchdog reset does not reset the PLL.

2.5.2. Reset Filtering

The RESETQ pin uses a filter with delay element, which suppresses the jitter and spikes in the range of 25 ns to 75 ns.

2.5.3. Reset Duration

With the active edge of the RESETQ an internal signal resets all the flip flops asynchronously. The internal signal is released synchronously to the internal clock when it is stable as described below.

Duration of the external reset depends on the time required for crystal oscillator to stabilize and is dependent on the crystal used.

During the period when the RESETQ pin is held low, the PLL is initialized and it gets locked. The high going reset pulse then initiates a sequence which requires one machine cycle (12 clock cycles) to initialize the processor and all other registers and peripherals.

2.5.4. Registers

Upon reset, all the registers are initialized to the values as defined in Section 3.4. on page 6-101

2.5.5. Functional Blocks

All blocks are initialized to a known state. CPU, acquisition and display will not have any pending bus requests after reset.

2.5.6. RAMs

Reset hardware does not initialize any RAMs.

2.5.7. Analog Blocks

After power-up reset the DAC will output a fix value. CADC and CADC wake up unit does not generate any interrupts till the 12 cycle reset sequence is completed.

2.5.8. Processor

After the reset sequence program counter initializes to 0000_H and starts execution from this location in the ROM. Location 0000_H to 0002_H is reserved for initialization routine.

2.5.9. Ports

With the reset all ports are set to input mode.

2.5.10. Initialization Phase

2.5.10.1. Acquisition

After reset the acquisition will not generate any memory accesses to the RAM, as ACQON bit is initialized to 0. The CPU should then initialize the VBI buffer and set the ACQON bit. The acquisition will also not generate any accesses to the RAM if the synchronization is not achieved.

2.5.10.2. Display

After the reset DAC will output a fix value as defined by EN_DG_OUT, which is reset to 0. COR_BLA is reset to a level indicating COR = 0 and BLank = 1.

Processor should initialize the display memory and set the EN_DG_OUT (OCD_CTRL) bit.

2.6. Memory Organization

The processor has separate Program and Data memory space. Memory spaces can be further classified as:

– Program Memory

– Internal Data Memory 256 Bytes (CPU RAM)

– Internal Extended Data Memory (XRAM)

A 16-bit program counter and a dedicated banking logic provide the processor with 1 MByte addressing capability (for ROM-less versions, up to 20 address lines are available).

The program counter allows the user to execute calls and branches to any location within the program memory space.

Data pointers allows to move data to and from Extended Data RAM.

There are no instructions that permit program execution to move from the program memory space to any of the data memory space.

2.6.1. Program Memory

Program ROM consists of 256 KB on-chip ROM.

Certain locations in program memory are reserved for specific programs. Locations ‘0000’ through ‘0002’ are reserved for the initialization program. Following reset, the CPU always begins execution at location ‘0000’. Locations ‘0003’ through ‘00CB’ are reserved for the interrupt-request service programs (see Section 2.3.6. on page 6-26).

2.6.2. Internal Data RAM

Internal Data RAM is split into CPU RAM and XRAM

2.6.3. CPU RAM

Address Space

The internal CPU RAM (IRAM) occupies address space 00_H to FF_H. This space is further split into two where lower 128 Bytes (00_H-$7F_H$) can be accessed using both direct and indirect register addressing method. Upper half 128 Bytes (80_H-FF_H) can be accessed using register indirect method only. Register direct method for this address space (80_H-FF_H) is reserved for Special function register access.

Registers

Controller registers are also located in IRAM. Four banks of eight registers each occupy locations 0 through 31. Only one of these banks may be enabled at a time through a two-bit field in the PSW.

Bit addressable RAM Area

128-bit locations of the on-chip RAM are accessible through direct addressing.These bits reside in internal data RAM at byte locations 32 through 47.

Stack

The stack can be located anywhere in the internal data RAM address space. The stack depth is limited only by the available internal data RAM, thanks to an 8-bit relocatable stack pointer. The stack is used for storing the program counter during subroutine calls and may also be used for passing parameters. Any byte of internal data RAM or special function registers accessible through direct addressing can be pushed/popped. By default Stack Pointer always has a reset value of 07_H.

2.6.4. Extended Data RAM (XRAM)

An additional on-chip RAM space called ‘XRAM’ extends the internal RAM capacity. Up to 20 Kilobytes of XRAM are accessed by MOVX @DPTR. XRAM is located in the upper area of the 64K address space.

1 KB of the XRAM, called VBI Buffer, is reserved for storing teletext data. 1 KB of address space can be allocated for CPU work space. Three KB of RAM is reserved as Display RAM. The rest of the RAM can be configured between Teletext page memory and DRCS (Dynamically Redefinable Character Set) memory.

Extended Data Memory Address Mapping

XRAM is mapped in the address space of $B000_H$ to $FFFF_H$. 20 KB are implemented on Chip. The address space of the 20K block is decoded starting from $B000_H$. Note that this decoding is done independent of the memory banking. That means that in all 16 banks of 64K, upper 20K address space is reserved for internal Extended data memory. This decoding method has an advantage, while copying data back and forth from on-chip RAM and off-chip RAM, there is no need to switch the memory banks.

2.6.5. Memory Extension

The controller provides four additional address lines A[19:16]. These additional address lines are used to access program and data memory space up to 1 MByte. The extended memory space is split into 16 banks of 64 kByte each. The address lines A[19:16] are therefore called bank address.

The additional address lines A[19:16] are delivered with the same timing as normal address lines A[15:0].

The functionality for memory extension is provided by the Memory Management Unit (MMU) which includes the four SFR registers: **MEX1**, **MEX2**, **MEX3**, and **MEXSP** (see **MEX1** on page 6-103).

These registers can be read and written through MOV instructions like any other SFR registers. Except for CB bits in **MEX1**, which are read only, they can only be written by MMU. During normal operation, the user must not write in the **MEXSP**.

The following instructions depend on memory extension settings:

– LJMP
– MOVC
– MOVX
– LCALL
– ACALL
– RET
– RETI

2.6.5.1. Memory Banking for LJMP Instruction

After reset the bits for current bank **CB[19:16]** and next bank **NB[19:16]** are set to zero. This makes sure that the processor starts at address 00000_H.

When a jump to another bank is required, software changes the bits **NB[19:16]** to the appropriate bank address (before LJMP instruction).

Only when a LJMP instruction is encountered as opcode, the MMU copies **NB[19:16]** into **CB[19:16]**, other JMP instructions have no effect.

Note: The **NB[19:16]** bits are not destroyed.

The **CB[19:16]** bits will appear on address lines A[19:16] during LJMP instructions.

2.6.5.2. Memory Banking for MOVC Instruction

There are two modes for MOVC instructions. The mode is selected by **MM** bit in **MEX2**.

MOVC with Current Bank

When **MM** = ‘0’, MOVC will access the current bank. The **CB[19:16]** bits will appear on address lines A[19:16] during MOVC instructions.

MOVC with Memory Bank

When **MM** = ‘1’, MOVC will access the memory bank. The **MB[19]** and **MB[18:16]** bits will appear on address lines A[19:16] during MOVC instructions.

Note: MEX1 is not destroyed.

2.6.5.3. Memory Banking for MOVX Instruction

There are two modes for MOVX instructions. The mode is selected by **MXM** bit in **MEX3**.

MOVX with Current Bank

When **MXM** = ‘0’, MOVX will access the current bank. The **CB[19:16]** bits will appear on address lines A[19:16] during MOVX instructions.

MOVX with Data Memory Bank

When **MXM** = ‘1’, MOVX will access the data memory bank. The **MX[19]** and **MX[19]** bits will appear on address lines A[19:16] during MOVX instructions.

Note: MEX1 is not destroyed.

2.6.5.4. Memory Banking for Interrupts

After reset the bits for current bank **CB[19:16]** and interrupt bank **IB[19:16]** are set to zero. This makes sure that the interrupt vector is taken from bank 0.

When the interrupt service routine is linked into another bank, the software has to change the bits **IB[19:16]** to the appropriate bank address before enabling interrupt.

When an interrupt is serviced, the **MEX1** register is pushed onto extension stack. **IB[19:16]** is copied into **CB[19:16]** and **NB[19:16]** and the interrupt vector is taken from bank **IB[19:16]**. The return from interrupt (RETI) instruction restores **MEX1** from extension stack and returns to **CB[19:16]**.

Memory Extension Stack

For interrupts and calls the memory extension stack is required. The stack pointer **MEXSP** addresses 128byte on-chip extension stack. No indication for stack full is provided. The programmer is responsible to read **MEXSP** to determine the status of the stack.

2.6.5.5. Application Examples

MOVC

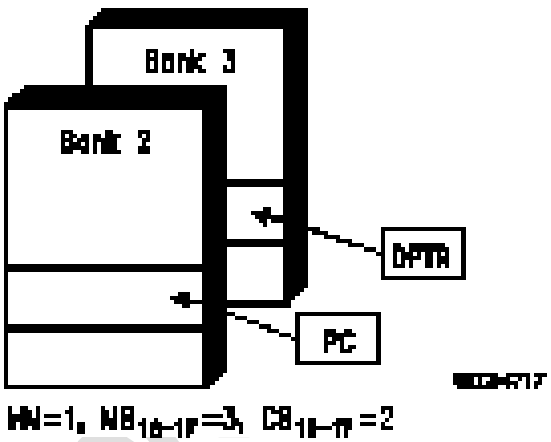


Fig. 2–3: PC and DPTR on different banks

Sample Code

Fig. 2–4 shows an assembler program run, performing the following actions:

1. Start at bank 0 at 00000.
2. Set ISR-page to bank 2.
3. Jump to bank 1 at address 25.
4. Being interrupted to bank 2 ISR.
5. Call a subprogram at bank 2 address 43.
6. After return read data from bank 2.

2.6.5.6. ROM and ROMless Version

The XROM pin determines the on-chip or off-chip ROM access.

If no internal ROM is to be used, then the XROM pin (in ROMless version) should be driven low. The CPU then accesses external ROM only. In ROM version this pin is internally pulled high, indicating no external ROM.

2.7. Patch Modul

2.7.1. Register Description

see **PATCH** on page 6-106

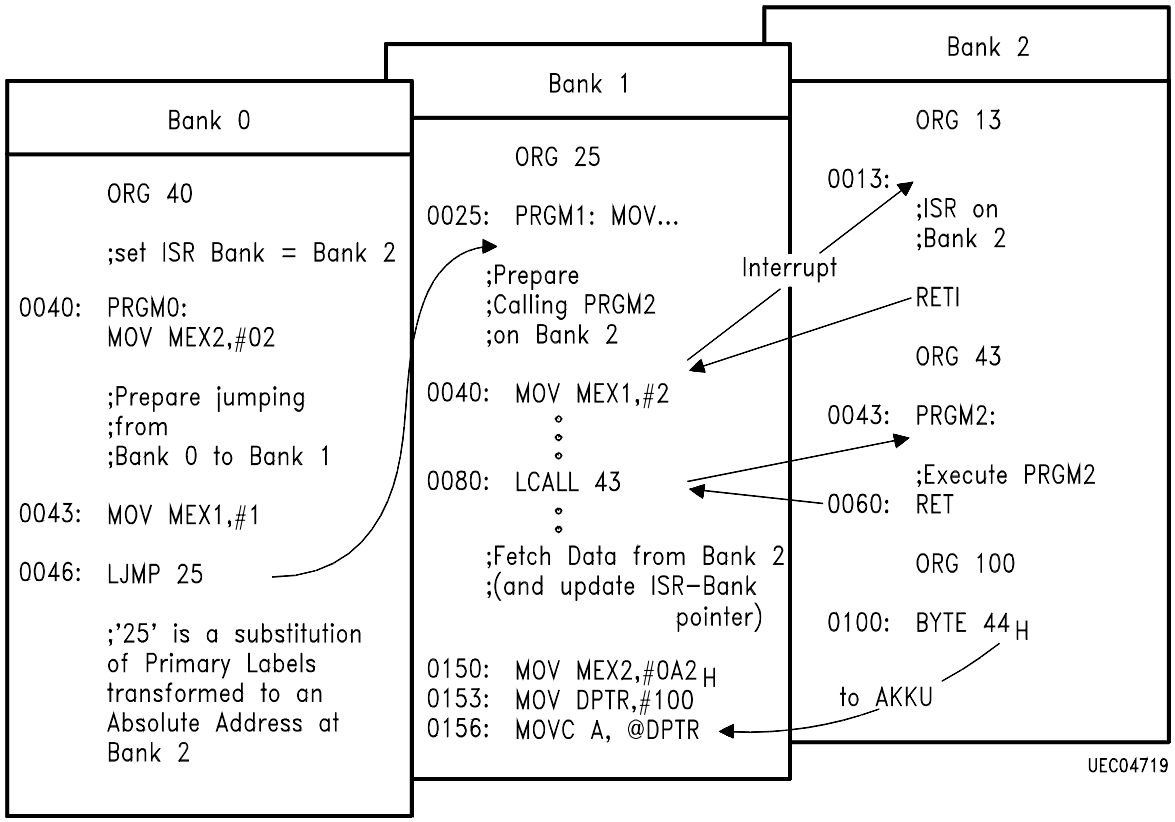


Fig. 2–4: Program Code

2.8. UART

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register (however, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at special function register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The frequencies and baud rates depend on the internal system clock, used by the serial interface.

2.8.1. Modes

The serial port can operate in 4 modes:

Table 2–11: Serial port modes

SM0	SM1	Mode	Description	Baud Rate (CDC = 0)
0	0	0	Shift Reg.	$f_{system/12}$
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	$f_{system/64}$, $f_{system/32}$
1	1	3	9-bit UART	Variable

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

2.8.1.1. Mode 0

Serial data enters and exits through RxD (P3.7). TxD (P3.1) outputs the shift clock.

2.8.1.2. Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On reception, the stop bit goes into RB8 in special function register SCON. The baud rate is variable.

2.8.1.3. Mode 2

11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmission, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On reception, the 9th data bit goes into RB8 in the special function register SCON, while the stop bit is ignored. The baud rate is programmable via SFR-Bit SMOD.

2.8.1.4. Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, mode 3 is the same as mode 2 in all respects except the baud rate. The baud rate in mode 3 is variable.

2.8.2. Multiprocessor Communication

Modes 2 and 3 of the serial interface of the controller have a special provision for multiprocessor communication. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor communications is as follows.

When the master processor wants to transmit a block of data to one of the several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in mode 0, and in mode 1 can be used to check the validity of the stop bit. In a mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

2.9. General Purpose Timers/Counters

Two independent general purpose 16-bit timers/ counters are integrated for use in measuring time intervals, measuring pulse widths, counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter.

In the ‘timer’ function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

A machine cycle consists of 12 oscillator periods.

In the ‘counter’ function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

2.9.1. Timer/Counter 0: Mode Selection

Timer/counter 0 can be configured in one of four operating modes, which are selected by bit-pairs (M1, M0) in TMOD-register (see Section 2.9.4. on page 6-38).

Mode 0

Putting timer/counter 0 into mode 0 makes it look like an 8048 timer, which is an 8-bit counter with a divide-by-32 prescaler. Table 2–12 on page 6-39 shows the mode 0 operation as it applies to timer 0.

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1 s to all 0 s, it sets the timer interrupt flag TF0. The counted input is enabled to the timer when TR0 = 1 and either GATE = 0 or INT0 = 1. (Setting GATE = 1 allows the timer to be controlled by external input INT0, to facilitate pulse width measurements.) TR0 is a control bit in the special function register TCON (see (see Section 2.9.5. on page 6-38)). GATE is contained in register TMOD (see Section 2.9.4. on page 6-38).

The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1

Mode 1 is the same as mode 0, except that the timer/ counter 0 register is being run with all 16 bits.

Mode 2

Mode 2 configures the timer/counter 0 register as an 8-bit counter (TL0) with automatic reload. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

Mode 3

Timer/counter 0 in mode 3 establishes TL0 and TH0 as two separate counters. TL0 uses the timer 0 control bits: C/T, GATE, TR0, INT0 and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from timer 1. Thus, TH0 now controls the ‘timer 1’ interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. With timer 0 in mode 3, the processor can operate as if it has three timers/counters. When timer 0 is in mode 3, timer 1 can be turned on and off by switching it out of and into its own mode 3, or can still be used in any application not requiring an interrupt.

2.9.2. Timer/Counter 1: Mode Selection

Timer/counter 1 can also be configured in one of four modes, which are selected by its own bit pairs (M1, M0) in TMOD-register.

The serial port receives a pulse each time that timer/ counter 1 overflows. This pulse rate is divided to generate the transmission rate of the serial port.

Modes 0 and 1 are the same as for counter 0.

Mode 2

The ‘reload’ mode is reserved to determine the frequency of the serial clock signal (not implemented).

Mode 3

When counter 1's mode is reprogrammed to mode 3 (from mode 0, 1 or 2), it disables the increment counter. This mode is provided as an alternative to using the TR1 bit (in TCON-register) to start and stop timer/counter 1.

2.9.3. Configuring the Timer/Counter Input

The use of the timer/counter is determined by two 8-bit registers, TMOD (timer mode) and TCON (timer control). The input to the counter circuitry is from an external reference (for use as a counter), or from the on-chip oscillator (for use as a timer), depending on whether TMOD's C/T-bit is set or cleared, respectively. When used as a time base, the on-chip oscillator frequency is divided by twelve or six before being used as the counter input. When TMOD's GATE bit is set (1), the external reference input (T1, T0) or the oscillator input is gated to the counter conditional upon a second external input (INT0), (INT1) being high. When the GATE bit is zero (0), the external reference, or oscillator input, is unconditionally enabled. In either case, the normal interrupt function of INT0 and INT1 is not affected by the counter's operation. If enabled, an interrupt will occur when the input at INT0 or INT1 is low. The counters are enabled for incrementing when TCON's TR1 and TR0 bits are set. When the counters overflow, the TF1 and TF0 bits in TCON get set, and interrupt requests are generated.

The counter circuitry counts up to all 1's and then overflows to either 0's or the reload value. Upon overflow, TF1 or TF0 is set. When an instruction changes the timer's mode or alters its control bits, the actual change occurs at the end of the instruction's execution.

2.9.4. Timer/Counter Mode Register

2.9.5. Timer/Counter Control Register

2.10. Capture Reload Timer

Capture control timer is a 16 bit up counter, with special features suited for easier infrared decoding by measuring the time interval between two successive trigger events. Trigger events can be positive, negative or both edges of a digital input signal (INT0 and INT1 on Port Mux). A built in Spike Suppression Unit (SSU) can be used for suppressing pulses with obviously too small or too long time duration at the beginning of an expected telegram, thereby relieving the FW of processing corrupted telegrams. This is especially useful in idle mode.

2.10.1. Input Clock

Input clock is f_{CCT} is same as system clock frequency divided by two. In normal mode system frequency is 40.5 MHz (f_{CCT} = 20.25 MHz) and in slow down mode (SD mode) 10.125 MHz (f_{CCT} = 5.0625 MHz).

PR prescaler bit when set divides the input clock further by 2, PR1 divides further by 8.

Internal to the block change in SD mode is detected and frequency is adjusted accordingly so that maximum time resolution of 15.73 ms or 251.66 ms is achieved depending on Prescaler PR bits.

2.10.2. Reset Values

All the eight 8 bit registers RELL, RELH, CAPL, CAPH, MINCAPL, MINCAPH, CRTCON0 and CRTCON1 are reset to 00_H.

2.10.3. Functional Description

2.10.3.1. Port Pin

Either Port INT0 or INT1 can be selected as capture input via SEL bit. Capture event can be programmed to occur on rising or falling edge or both using the bits RISE and FALL bits.

2.10.3.2. Slow-Down Mode

SD bit when set, reduces the system frequency to 10.125 MHz. However the clk to the counter has a fix frequency (for a particular prescaler value). This is achieved by a divide by 4 chain, which divides the incoming frequency by 4 when SD = 0 and feeds the incoming signal directly to the counter when SD = 1.

2.10.3.3. Run

When counter is started (RUN), 16 bit reload value is automatically loaded in the 16 bit counter.

Note: REL bit is irrelevant in case of RUN function. Setting run bit resets the FIRST and OV bit.

All the control bits PR, PLG, REL, RUN, RISE, FALL, SEL, Start, Int_Src, SD can be changed anytime during the operation, these changes take immediate effect there is no protected mode when counter is running.

2.10.3.4. Overflow

In case no capture event occurs, counter keeps on counting till it overflows from $FFFF_H$ to 0000_H at this transition OV bit is set. After the overflow counter keeps on counting. Overflow does not reload the reload value.

Note: OV bit is set by counter and can be reset by software.

2.10.3.5. Modes

There are three different modes in which counter can be used.

– Normal Capture mode

– Polling mode

– Capture mode with spike suppression at the start of a telegram

Table 2–12: Counter modes

Mode	START	PLG
Normal capture mode	0	0
Capture mode with spike suppression	1	0
Polling mode	X	1

For each mode selection it is recommended to reset the RUN bit (if it is not already at 0), set the appropriate mode bit and then start the counter by setting the RUN bit.

For each of the capture mode the event is captured based on the CRTCON0 (RISE) and CRTCON0 (FALL).

2.10.3.6. Normal Capture Mode

Normal capture mode is started by setting the RUN bit (0 --> 1) and PLG = 0, start = 0. Setting RUN bit will reload the counter with reload value and reset the overflow bit and counter will start to count.

Upon event on the selected port pin, contents of the counter are copied to the capture registers CRT_caph and CRT_capl.

In capture mode if REL bit is set counter is automatically reloaded upon event with the reload value and starts to count. If however REL bit is not set then counter continues to count from the current value.

OV bit is not effected by the capture event.

Note: Min_cap register has no functionality in this mode.

Note: Interrupt would be generated from CRT, however it will only be registered in the int source register if intsrc bits in the CSCR1 are appropriately set. It is not required to use the CRT generated interrupt in this mode. Direct pin interrupt can be used.

2.10.3.7. Polling Mode

Polling mode is started by setting the PLG bit, PLG = 1 (START bit is in don't care for this mode). Setting RUN bit will reload the counter with reload value and reset the overflow bit and start the counting.

In the timer polling mode, capture register mirrors the current timer value,

Note: In this mode any event at selected port pin is ignored. Upon overflow OV bit is set.

Note: Interrupts are not generated as events are not recognized.

2.10.3.8. Capture Mode with Spike Suppression at the Start of a Telegram

This mode is specially been implemented to prevent false interrupt from being generated specially in idle mode while waiting for a new infrared telegram.

This mode is entered by setting the START bit (PLG = 0). Software sets Start bit to indicate it is expecting a new telegram. Setting RUN bit will reload the counter with reload value and reset the overflow bit and start the counting.

2.10.3.9. First Event

On occurrence of capture event, counter value is captured and comparator then sets the First bit. Interrupt is suppressed. OV bit is reset and counter reloads the reload value (regardless of the status of REL bit) and starts counting again.

2.10.3.10. Second Event

On occurrence of second capture event, counter value is captured and interrupt is triggered if the capture value exceeds the value in the Min_Cap register and the OV bit is not set. First bit is reset. Counter will now continue in the normal capture mode. Software may reset the START bit if the capture value is a valid pulse of a telegram.

If the pulse was invalid then software must stop the counter and start again (Run bit first reset and then SET) with start bit set to wait for a new telegram.

If Capture value is less then or equal to MIN_CAP value or OV bit has been set, that is spike has been detected and Interrupt is suppressed. OV bit would be reset counter would be reloaded with reload value (regardless of REL bit).

In this case if either RISE or FALL bit were set then counter will wait for the second event (FIRST = 1), if RISE and FALL both were set then counter will wait for the first event (FIRST = 0).

2.10.3.11. CRT Interrupt

CRT can generate interrupt when SSU is employed.

CRT unit uses the same interrupt line as $\overline{\text{INT1}}$ and INT0. The interrupt line is selected by the SEL bit.

Note: When using CRT to generate interrupt, the direct interrupt source from INT0 or INT1 (which ever is selected) should be switched to CRT (CSCR1(IntSrc0), CSCR1(IntSrc1)). If application uses port pins directly to generate interrupt, then these bits should be reset.

SSU generates interrupt signal as a pulse, which is captured in the int source register TCON (IE1 or IE0). While using this mode TCON (IT0 or IT1) must be set to 1 (edge triggered) and IRCON (EX1R or EX0R) must be set to 1 and IRCON(EX1F or EX0F) must be set to 0.

For further information on interrupts please refer to Section 2.3.

2.10.3.12. Counter Stop

Counter can be stopped any time by resetting the RUN bit. If counter is stopped and started again (reset and set the RUN bit), counter reloads with the RELOAD value and reset the OV bit.

2.10.4. Idle and Power-Down Mode

In idle mode CRT continues to function normally, unless it has been explicitly shut off by PSAVEX (PERI) bit.

In power-down mode CRT is shut off.

2.10.5. Registers

The RELL and RELH are the reload registers (SFR address $B7_H$ and $B9_H$), CAPH and CAPL are corresponding capture registers (SFR address BA_H and BB_H). MIN_CAPL and MIN_CAPH (BC, BB) are Minimum capture registers. CRTCON0 ($E5_H$) and CRTCON1 are the control registers.

Table 2–13: Time Resolution

SD	f_{sys} (MHz)	PR1	PR	f_{ctr} (MHz)	f_{ctr} (MHz)	Time Res. (ns)	Max Pulse Width (ms)
0	33.33	0	0	$f_{sys}/8$	4.17	240	15.73
		0	1	$f_{sys}/16$	2.083	480	31.46
		1	0	$f_{sys}/64$	.5208	1920	125.83
		1	1	$f_{sys}/128$	.2604	3840	251.66
1	8.33	0	0	$f_{sys}/8$	4.17	240	15.73
		0	1	$f_{sys}/16$	2.083	480	31.46
		1	0	$f_{sys}/64$	.5208	1920	125.83
		1	1	$f_{sys}/128$	.2604	3840	251.66

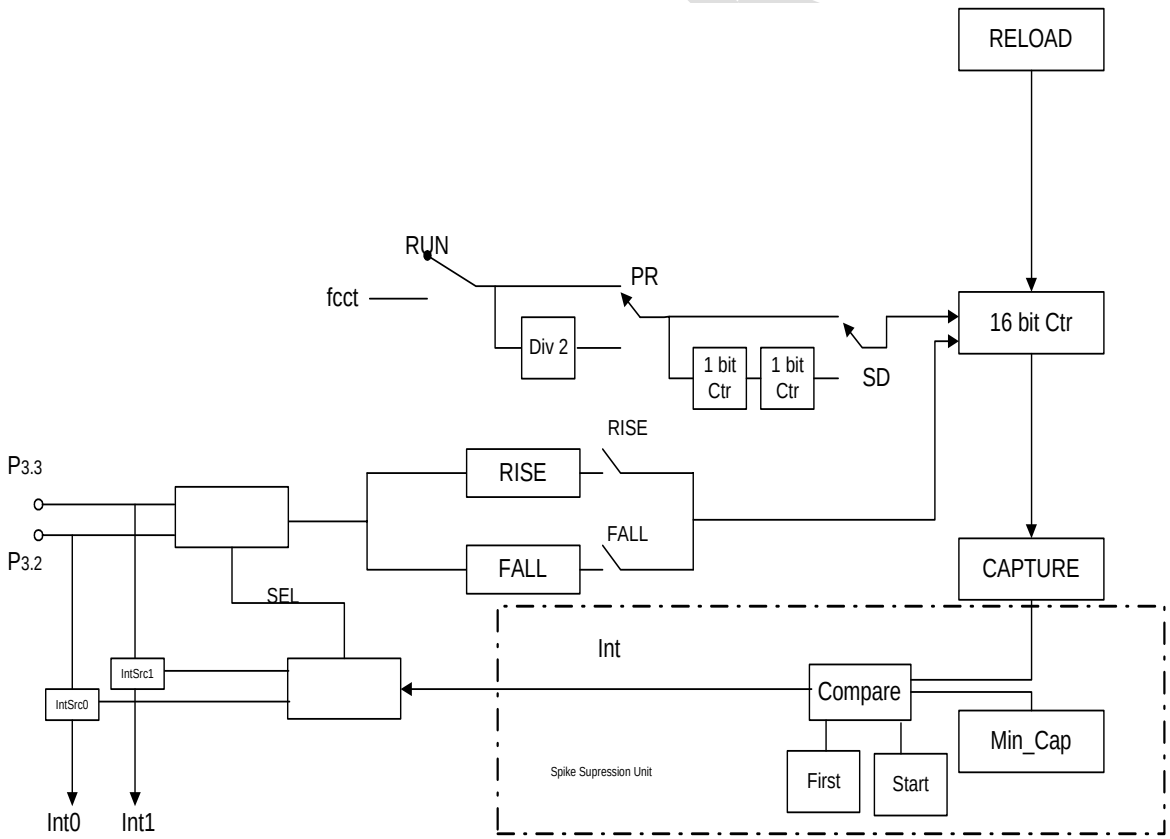


Fig. 2–5: Block Diagram

2.11. Pulse Width Modulation Unit

The Pulse Width Modulation unit consists of 6 quasi 8 bit and 2 quasi 14 bit PWM channels. PWM channels are programmed by special function registers and each individual channel can be enabled and disabled individually.

2.11.1. Reset Values

All the PWM unit registers PWME, PWCOMP8 0-5, PWCOMP14 0-1, PWMCOMPEXT14 0-1, PWML and PWMH are by default reset to 00_H.

2.11.2. Input Clock

Input clock to PWMU FPWM is derived from f_{sys}. f_{sys} is 40.5 MHz in normal mode and in slowdown mode 10.125 MHz. In normal mode f_{sys} is divided by 2 and in slow down mode it is directly fed to the PWMU. Therefore PWM unit is counting at 16.5 MHz in normal mode and 8.25 MHz in slow down mode. If PR bit PCOMPEXT14 0 (bit 0) is set the then the counting frequency is half of that.

In addition PWM_direct bit makes it possible to run PWM counter at system frequency, ignoring PR bit and the built in divide by 2 prescaler.

To reduce electromagnetic radiation, the different PWM-channels are not switched on simultaneously with the same counter value, but delayed each with one clock cycle to the next channel:

Channel 0: 0 clock cycles delayed, Channel 1: 1 clock cycle delayed, …, Channel 5: 5 clock cycles, …, PWM14_0: 6 clock cycles, PWM14_1: 7 clock cycles delayed.

2.11.3. Port Pins

Port 1 is a dual function port. Under normal mode it works as standard Port 1, under alternate function mode it outputs the PWM channels.

P1.0 … P1.5 corresponds to the six 8 bit resolution PWM channels PWM8_0 … PWM8_5. P1.6 and P1.7 corresponds to the two 14 bit resolution PWM channels PWM14_0 and PWM14_1. PWM channels can be individually enabled by corresponding bits in the PWME register provided PWM_Tmr bit is not set (timer mode start bit).

2.11.4. Functional Description

2.11.4.1. 8-Bit PWM

The base frequency of a 8 bit resolution channel is derived from the overflow of a six bit counter.

On every counter overflow, the enabled PWM lines would be set to 1. Except in the case when compare value is set to zero.

In case the comparator bits (7 … 2) are set to 1, the high time of the base cycle is 63 clock cycles. In case all the comparator bits (7 … 0) including the stretching bits are set to 1, the high time of the full cycle (4 base cycles) is 255 clock cycles.

The corresponding PWCOMP8x register determines the duty cycle of the channel. When the counter value is equal to or greater than the compare value then the output channel is set to zero. The duty cycle can be adjusted in steps of FPWM as mentioned in Table 2–14.

In order to achieve the same resolution as 8-bit counter, the high time is stretched periodically by one clock cycle. Stretching cycle is determined based on the two least significant bits in the corresponding PWCOMP8x register.

The relationship for stretching cycle can be seen in Table 2–14 and Fig. 2–6.

Table 2–14: Stretching cycle corresponding to register PWCOMP8X

PWCOMP8X	Cycle Stretched
Bit 1	1, 3
Bit 0	2

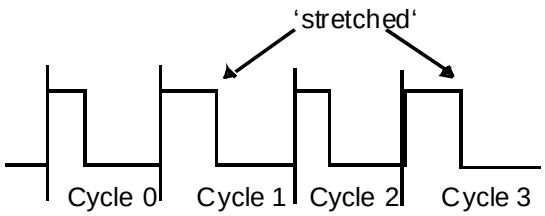


Fig. 2–6: Stretching cycles

2.11.4.2. 14-Bit PWM

The base frequency of a 14 bit resolution channel is derived from the overflow of a eight bit counter.

On every counter overflow, the enabled PWM lines would be set to 1. Except in the case when compare value is set to zero.

The corresponding PWCOMP14x register determines the duty cycle of the channel. When the counter value is equal to or greater than the compare value then the output channel is set to zero. The duty cycle can be adjusted in steps of FPWM as mentioned in Table 2–15.

In order to achieve the same resolution as 14bit counter, the high time is stretched periodically by one clock cycle. Stretching cycle is determined based on the bit 7…1 in the corresponding PWCOMPEXT14x register.L

Table 2–15: Stretching cycle corresponding to register PWCOMPEXT14X

PWCOMPEXT14X	Cycle Stretched
Bit 7	1, 3, 5, 7, …, 59, 61, 63
Bit 6	2, 6, 10, …, 54, 58, 62
Bit 5	4, 12, 20, …, 52, 60
Bit 4	8, 24, 40, 56
Bit 3	16, 48
Bit 2	32

2.11.5. Power Down, Idle, and Power-Save Mode

In idle mode PWMU continues to function normally, unless it has been explicitly shut off by PSAVE(PERI).

Note: In Psave mode all channels are frozen and pins are switch to port output mode making it possible to use the port lines.

In power-down mode PWMU is shut off.

Table 2–16: Cycle Time

PWM Resolution	Slow Down (SD)	PWM_ PR	PWM_ direct	f_{sys} [MHz]	Counting Rate [MHz]	Base Cycle Time [µs]	Full Cycle Time [µs]
8 Bit	**0**	**0**	**0**	**33.33**	**16.66**	**3.84**	**15.37**
	1	0	0	8.33	8.33	7.68	30.73
	0	1	0	33.33	8.33	7.68	30.73
	1	1	0	8.33	4.16	15.37	61.46
	0	X	1	33.33	33.33	1.92	7.68
	1	X	1	8.33	8.33	7.68	30.73
14 Bit	**0**	**0**	**0**	**33.33**	**16.66**	**15.37**	**983.4**
	1	0	0	8.33	8.33	30.7	1967
	0	1	0	33.33	8.33	30.7	1967
	1	1	0	8.33	4.16	61.4	3934
	0	X	1	33.33	33.33	7.68	492
	1	X	1	8.33	8.33	30.7	1967

2.11.6. Timer

PWM unit uses a single 14 bit timer to generate signals for all 8 channels. Timer is mapped into SFR address space and hence is readable by the controller. Timer is enabled (running) if one of the PWM channels is enabled in PWME. If all the channels are disabled counter is stopped. Enabling one of the channels will reset the timer to 0 and start.

Note: This reset is done for the first enabled channel. All other channels enabled later will drive the output from the current value of the counter.

If all the channels are disabled then it can be used as a general purpose timer, by enabling it with PWM_Tmr bit in PWCH.

Setting PWM_Tmr bit switches to timer mode and starts the timer, Timer always starts from a reset value of 0 (OV also reset to 0). Timer can be stopped any time by turning off the PWM_Tmr bit.

When timer overflows it sets an over flow bit OV (bit 6) PWCH and interrupt bit CISR0 (PWtmr) in the central interrupt register. If the corresponding interrupt enable bit is EPW(IEN2) is set the interrupt would be serviced. OV bit and PWtmr bits must be reset by the software.

Note: Before utilizing the timer for PWM channels PWM_Tmr bit must be reset.

Note: On reset CISR0 (PWtmr) bit is initialized to 0, however if counter overflows this bit might be set along with OV bit. However clearing OV bit does not clear the CISR0 (PWtmr) bit. Therefore software must clear this bit before enabling the corresponding interrupt.

2.11.7. Control Registers

All control register for PWM are mapped in the SFR address space. Their address and bit description is given below.

Note: The controller can write any time into these registers. However registers PWM_COMP8_X, PWM_CPMP14_X and PWM_CPMPEXT14_X, including the bits PWM_direct and PWM_PR are double buffered and values from shadow registers are only loaded into the main register in case timer overflows or timer is stopped (PWME = 00_H) of 8 bit counter.

Overflow for 8 bit PWM occurs at the overflow of 6 bit counter and overflow for 14 bit counter occurs at the overflow.

When any of the PWM channels is not used associated compare register can be used as general purpose registers, except PWM_En and PWCOMPEXT14_0 bit 0 and 1.

Note: The described operation is independent of the setting of PWCOMP14_x. The stretch operation is interleaved between PWM-Cycles.

2.12. Watchdog Timer

Watchdog timer is a 16 bit up counter which can be programed to clock by $f_{wdt}/2$ or $f_{wdt}/128$. The current count value of the watchdog timer is contained in the watchdog timer register WDT_High and WDT_Low. which are read-only register. Control and refresh function of the WDT is controlled by WDT_Refresh and WDT_Ctrl.

Additionally, the counter can be used as a general purpose timer in timer mode, and the associated load register can be used either as load register or independent scratch register by the user.

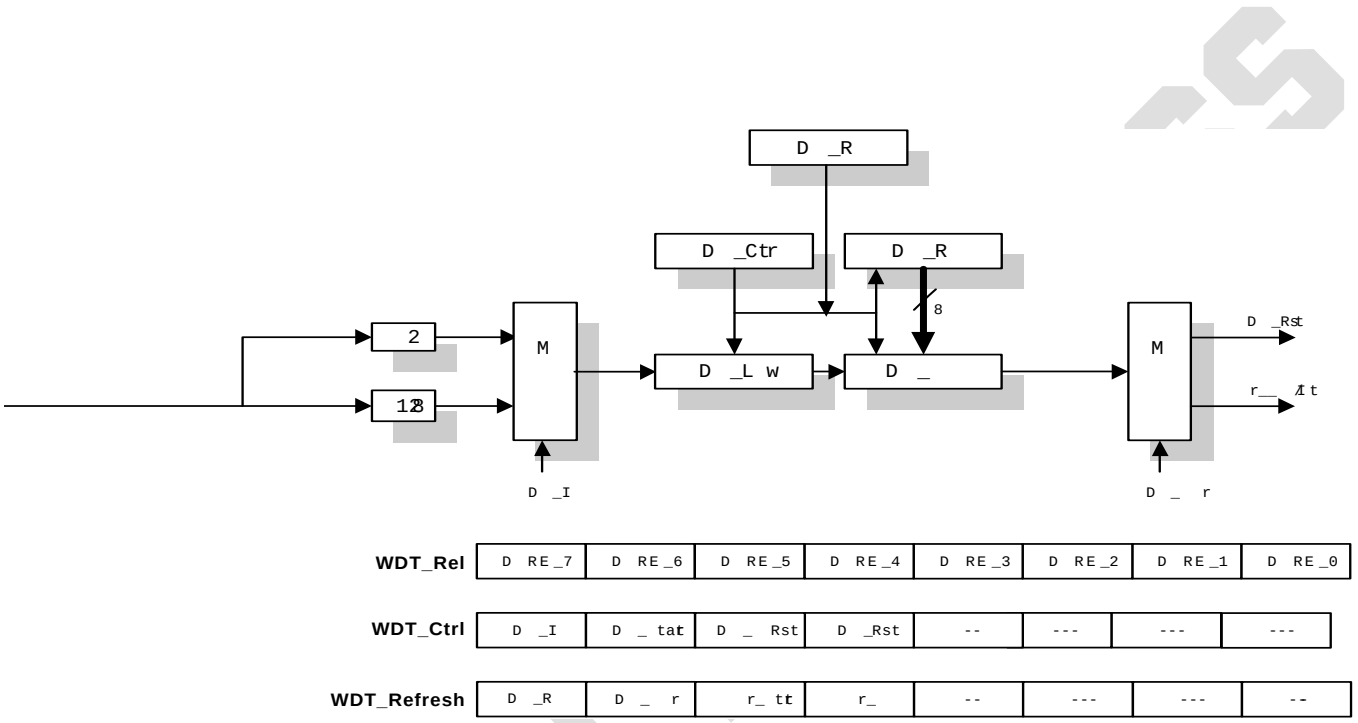


Fig. 2–7: Watchdog timer block diagram

2.12.1. Input Clock

Input clock f_{wdt} is same as CPU clock f_{sys} divided by 12 (i.e. machine cycle) is fed to the WDT either as divide-by-2 or divide-by-128. Divide factor is determined by WDT_In (WDT_ctrl) equal 0 and 1 respectively. WDT_In has the same functionality in both watch dog mode and timer mode.

2.12.2. Starting WDT

WDT can be started if the WDT unit is in the Watch dog mode (WDT_Tmr = 0).

WDT is started by setting the bit WDT_Start in the WDT_Ctrl register. Immediately after the start (1 clock cycle) the reload value from WDT_Rel register is copied to the WDT_High. WDT_Low is always reset to 0 upon start.

Value can be written to WDT_Rel any time during normal controller operation. Value is only loaded to the counter upon start, refresh or watchdog reset (if WDT_nARST is set).

Note: Counter registers are read only and cannot be directly written by the controller.

2.12.3. Refresh

Once WDT is started it cannot be stopped by software.

Note: While WDT is running any change to WDT_tmr bit would be ignored.

A refresh to the WDT is required before the counter overflows. Refreshing WDT requires two instruction sequence whereby first instruction sets WDT_Ref bit and the next instruction sets the WDT_Start bit. (For example if there is NOP between these two instructions, refresh would be ignored). This double instruc-

tion refresh minimize the chances of unintentional reset of the watchdog timer. Once set, WDT_Ref bit is reset by the hardware after three machine cycles.

Refresh causes WDT_low to reset to 00_H and loads the reload value to from WDT_Rel to WDT_High.

2.12.4. WDT Reset

If software fails to refresh the WDT before the counter overflows after $FFFF_H$, an internally generated watchdog reset is entered.

Watchdog timer reset differs only from the normal reset in that during normal reset all the WDT relevant bits in the three registers WDT_Rel, WDT_Refresh, WDT_control are reset to 00_H. Counter gets initialized to 0000_H.

In case of watchdog reset, WDT_Start and WDT_nARST are not reset. Bit WDT_Rst (read only) is set to indicate the source of the reset. In addition the WDT reset does not reset the PLL and clock generator.

If the WDT_nARst bit is set then the values in the WDT_Rel are retained after the WDT reset and counter starts with the same pre-scaler (WDT_in) and reload configuration as before reset. If WDT_nARst is not set then upon watchdog reset, WDT_Rel is reset to 00h and WDT_In to 0.

After the WDT reset counter starts again and must be refreshed by the processor in order to avoid further WDT resets.

Duration of the WDT reset is sufficient to ensure proper reset sequence.

2.12.5. Power-Down Mode

WDT is shut off during power down mode along with the rest of the peripherals.

In idle mode the WDT (in watchdog mode) is frozen, in timer mode it continues it's operation.In power save mode PSAVE (PERI) watchdog continues it's operation any write to this bit is ignored. If in timer mode the timer can be frozen by setting this bit.

2.12.6. Time Period

The period between refreshing the watchdog timer and the next overflow can be determined by the following formula.

PWDT = [2(1 + (WDT_In) × 6) × (216 - (WDT_Rel) × 28)] / [FWDT]

Based on 33.33 MHz system clock minimum time period and maximum time period are as defined in Table 2–17.

Table 2–17: Period between refreshing the watchdog timer and the next overflow

	f_{system}	WDT_In	WDT_Rel	P_{WDT}
Min.	33.33 MHz	0	FF_H	184.3 µs
Max.	33.33 MHz	1	00_H	3.02 s

2.12.7. WDT as General Purpose Timer

WDT counter can be used as a general purpose timer in timer mode and the associated load register can be used either as load register or independent scratch register for the programmer. This is achieved by setting WDT_Tmr bit.

WDT_Tmr bit can only be set before starting the WDT timer. Once watchdog timer is started it is not possible to switch to general purpose timer mode.

If WDT_Tmr bit is set then timer can be started using WTmr_Strt bit.

When timer is started it

– Resets the WTmr_OV overflow flag.

– Loads the preload value from WDT_Rel and starts counting up.

Upon overflow WDT_Rst bit is not set neither is internal watchdog reset initiated. Overflow is indicated by the bit WTmr_Ov (r/w). Overflow also sets the interrupt source bit CISR0 (WTmr). Both of these bits are set by hardware and must be cleared by software. If corresponding watchdog timer interrupt enable IE1 (EWT) bit is set then upon overflow interrupt is initiated.

After overflow timer starts to count from WDT_Rel. It is possible for the processor to stop the timer by resetting the WTmr_strt bit any time.

While timer is running, WDT_Tmr bit cannot be toggled any write to this bit is ignored. To reset the WDT_Tmr bit, either timer is stopped (WTmr_Strt). However, it is possible to stop the timer (WTmr_Strt) and toggle (WDT_Tmr) with the same instruction.

2.13. Real Time Clock (RTC)

2.13.1. Register Description

See **RTC** on page 6-104.

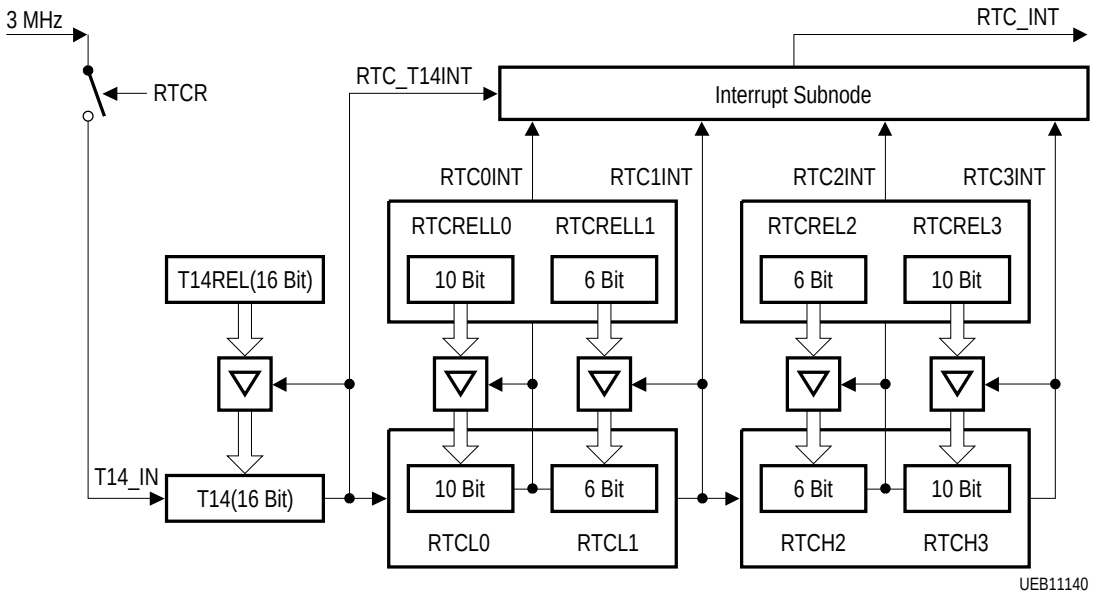


Fig. 2–8: Real Time Clock

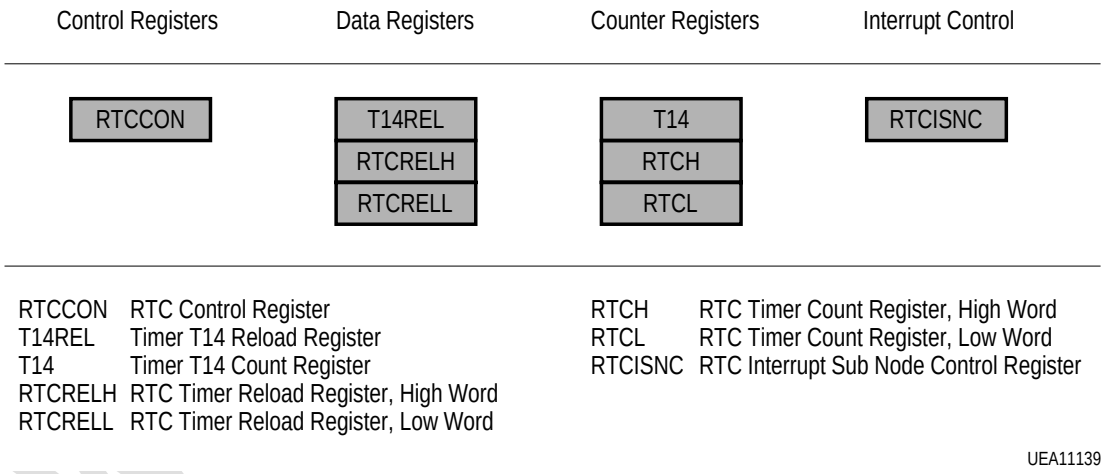


Fig. 2–9: Real Time Clock Register

2.14. Analog Digital Converter (CADC)

TVT includes a four channel 8-bit ADC for control purposes. By means of these four input signals the controller is able to supervise the status of up to four analog signals and take actions if necessary.

This analog signals can be connected to Port 1.4 - Port 1.7 inputs without a special configuration. If the port pins of Port 1 are used as digital input, make sure that the input high level never exceeds VSUP3.3IO.

The input range of the CADC is fixed to the supply voltage range (3.3 V nominal).

The conversion is done continuously on all four channels the results are stored in the SFRs CADC0 … CADC3 and updated automatically every 46 µs. An interrupt can be used to inform the processor about new available results.

2.14.1. Power Down and Wake Up

During idle mode it is required to reduce the power consummation dramatically. In order to do this for the CADC a special wake up unit has been included. During this mode only the signal on input channel 1 is observed. As soon as the input signal has fallen below a predefined level an interrupt is triggered and the system wakes up. Two different levels are available. The first one corresponds to (fullscale−4 LSB) the second one to (fullscale−16 LSB). The actual level can be selected by a control bit (ADWULE).

Nevertheless it is possible to send even this wake up unit into power down (for detailed description refer to Section 2.4.3.).

2.14.2. Register Description

See **CADC** on page 6-112.

2.15. I/O-Ports

2.15.1. Port Mux

2.15.2. Register Description

See **PORT** on page 6-101.

Table 2–18: Port Mux

Port Addr	Port Pin	Input: Port	RXD	TIM0	TIM1	INT0	INT1	INTX0	INTX1	ITUI	CADC	Output: P-P	O-D	TXD	PWM8	PWM14	DFVBL FIELD	PWMV	HSYNC CSYNC	VSYNC	ITUO	I2C: SCL	SDA
0	P10	0	1	2	3	4	5	6	7			9	10	11	12.0	13.0	8					14	
1	P11	0	1	2	3	4	5	6	7			9	10	11	12.1	13.1		8					14
2	P12	0	1	2	3	4	5	6	7			9	10	11	12.2	13.0			8			14	
3	P13	0	1	2	3	4	5	6	7			9	10	11	12.3	13.1				8			14
4	P14	0	1	2	3	4	5	6	7		8.0	9	10	11	12.4	13.0						14	
5	P15	0	1	2	3	4	5	6	7		8.1	9	10	11	12.5	13.1							14
6	P16	0	1	2	3	4	5	6	7		8.2	9	10	11	12.0	13.0						14	
7	P17	0	1	2	3	4	5	6	7		8.3	9	10	11	12.1	13.1							14
8	P20	0	1	2	3	4	5	6	7			9	10	11	12.2	13.0	8					14	
9	P21	0	1	2	3	4	5	6	7			9	10	11	12.3	13.1		8					14
10	P22	0	1	2	3	4	5	6	7			9	10	11	12.4	13.0			8			14	
11	P23	0	1	2	3	4	5	6	7			9	10	11	12.5	13.1				8			14
12	Config1																						
13	Config2																						
14	Config3																						
15	free																						
16	P24	0	1	2	3	4	5	6		7		9	10	11	12.0	13.0					8	14	
17	P25	0	1	2	3	4	5	6		7		9	10	11	12.1	13.1					8		14
18	P26	0	1	2	3	4	5	6		7		9	10	11	12.2	13.0					8	14	
19	P27																						
20	P30	0	1	2	3	4	5	6		7		9	10	11	12.4	13.0					8	14	
21	P31	0	1	2	3	4	5	6		7		9	10	11	12.5	13.1					8		14
22	P32	0	1	2	3	4	5	6		7		9	10	11	12.0	13.0					8	14	
23	P33	0	1	2	3	4	5	6		7		9	10	11	12.1	13.1					8		14
24	P34	0	1	2	3	4	5	6		7		9	10	11	12.2	13.0					8	14	
25	P35	0	1	2	3	4	5	6		7		9	10	11	12.3	13.1					8		14
26	P36	0	1	2	3	4	5	6		7		9	10	11	12.4	13.0					8	14	
27	P37	0	1	2	3	4	5	6		7		9	10	11	12.5	13.1					8		14
28-31	free																						

SFR-Register Addr	Name	Short	Reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
92	Port Mux 1	PMUX1	0	Port Addr 0-11				Port Mode 0-15			
			4	Port Addr 12 = Config1				Ext.	MSP	DPS	VSP
			4	Port Addr 13 = Config2				Ext.	Port	TVT	TVT slave
			0	Port Addr 14 = Config3				Test	not used	DPS	VSP
93	Port Mux 2	PMUX2	0	Port Addr 16-27				Port Mode 0-15			

Port Mode 15 enables read back of port pin configuration

0=enable I2C slave, 1=disable I2C slave (disabling Ext. enables Test slave)

0=enable I2C master, 1=disable I2C master

1=reset I2C slave

Port Mode 15 enables read back of port pin configuration

2.16. Slicer and Acquisition

2.16.1. General Function

TVT provides a full digital data slicer including digital H/V-sync separation and digital sync processing. The acquisition interface is capable to process all known data services transmitted between line 6 to line 23 (TTX, VPS, CC, WSS). Digital signal processing algorithms are applied to compensate various disturbance mechanisms which exist on TV channels. These are

– Noise measurement and compensation.

– Frequency attenuation measurement and compensation.

– Group delay measurement and compensation.

The digital CVBS input signal is taken from the CVBS frontend of VSP (see Section 2.2. on page 4-10). An interpolation filter is used to adapt to the different clock frequency of the slicer.

The sliced data is synchronized to the clock frequency given by the clock-run-in (CRI) of the actual data service and to the framing code (FC) of the data stream. After a successful framing code check the sliced data is written to a programmable VBI buffer. After line 23 is received an interrupt request is delivered to the microcontroller. The microcontroller starts to process the data in the VBI buffer. That means, the data is error checked by software and stored in the memory.

To improve the signal quality the slicer control logic generates horizontal and vertical windows in which the reception of the framing code is allowed. The framing code can be programmed for each line individually, so that in each line a different data service can be received. For TTX, CC and VPS the framing code is hardwired. Additionally a sequence of 8 or 16 bits can be programmed to be compared with the incoming data. In a special mode the framing code can be bypassed, so that all incoming data are stored in the VBI buffer and are further processed by the microcontroller. All follow up acquisition tasks are performed by the microcontroller, so in principle, the data of every data service can be acquired.

2.16.2. Slicer Architecture

The slicer is composed of three main blocks:

– data slicer

– sync separation

– acquisition interface

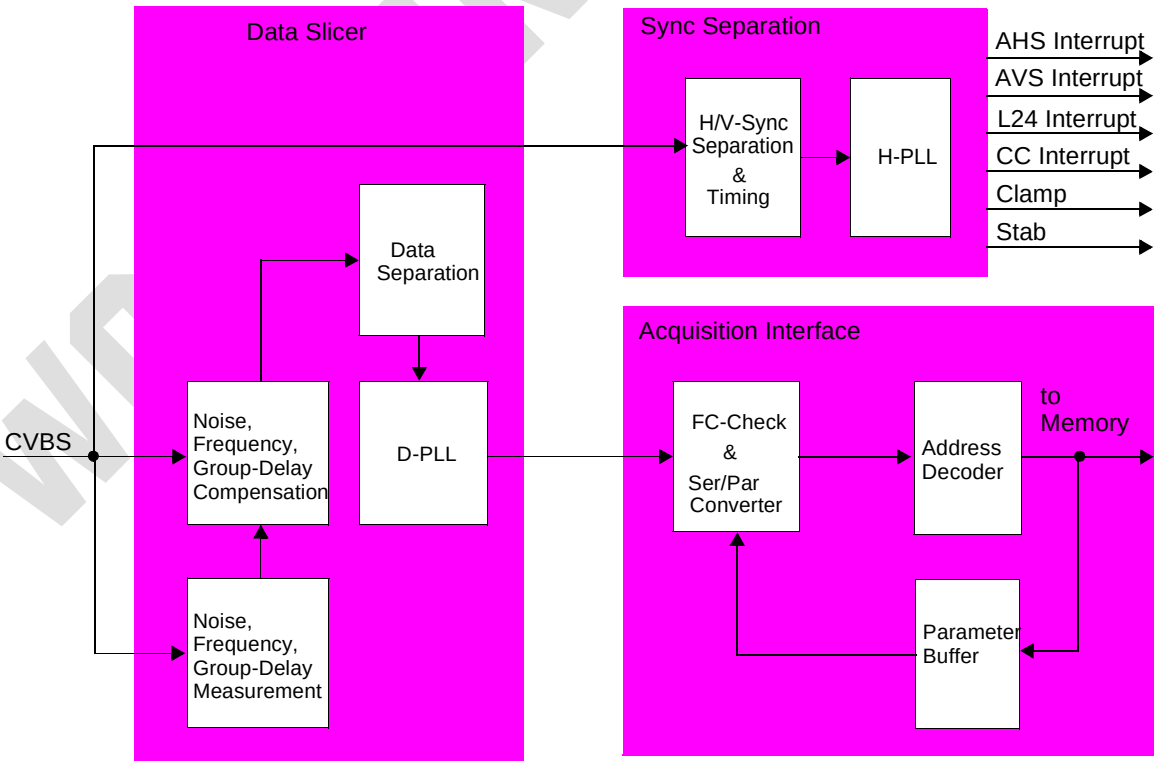


Fig. 2–10: Block Diagram of Digital Slicer and Acquisition Interface

2.16.2.1. Distortion Processing

After A/D conversion the digital CVBS bit stream is applied to a circuitry which corrects for transmission distortion. In order to apply the right algorithm for correcting, a signal measurement is done in parallel. This measurement device can detect the following distortions.

2.16.2.1.1. Noise

The noise measurement unit incorporates two different algorithms. Both algorithm are using the value between two equalizing pulses which corresponds to the black level. As the black level is known to the system a window is placed between two equalizing pulses of line 4. The first algorithm compares successive samples inside a window placed in line 4. The difference between this samples is measured and a flag is set as soon as this difference over several TV lines is greater than a specified value. This algorithm is able to detect higher frequency noise. The second algorithm measures the difference between the black value and the actual sampled value inside this window. As soon as this difference over several TV lines is greater than a specified value a second flag is set. This algorithm is sensitive against low frequency noise as it is known from co-channel distortion. Both flags can be used to optimize the correcting circuit characteristic in order to achieve best reception performance.

2.16.2.1.2. Frequency Attenuation

During signal transmission the CVBS can be attenuated severely. This attenuation normally is frequency depending. That means that the higher the frequency the stronger the attenuation. As the clock-run-in (CRI) for teletext represents the highest possible frequency (3.5 MHz) it can be used to measure the attenuation. As only strong negative attenuation causes problems during data slicing a flag is needed to notify highly negative attenuation. If this flag is set a special peaking filter is switched on in the data-path.

2.16.2.1.3. Group Delay

Quite often the data stream is corrupted because of group delay distortion introduced by the transmission channel. The WST framing code ($E4_H$) is used as a reference for measurement. The delay of the edges inside this code can be used to measure the group delay distortion. The measurement is done every teletext line and filtered over several lines. It can be detected whether the signal has positive, negative or no group delay distortions. Two flags are set accordingly. By means of these two flags an allpass filter contained in the correcting circuit is configured to compensate the positive or negative group delays.

All of the above filters can be individually disabled, forced or set to an automatic mode via control registers.

2.16.2.2. Data Separation

Parallel to the signal analysis and distortion compensation a filter is calculating the slicing level. The slicing level is the mean-value of the CRI. As the teletext is coded using the NRZ format, the slicing level can not be calculated outside the CRI and is therefore frozen after CRI. Using this slicing level the data is separated from the digital CVBS signal. The result is a stream of zeros and ones. In order to find the logical zeros and ones which have been transmitted, the data clock needs to be recovered as well. Therefore a digital data PLL (D-PLL) is synchronized to the data clock during CRI using the transitions in the sliced data stream.

The operating frequency of the D-PLL is programmable using the line parameter DINCR.

$$DINCR = f_{data} * 2^{18} / 40.5MHz$$

Table 2–19: Sampling rate for data services

Service	f_{data} [MHz]	DINCR	
WST	6.9375	44904	AF68h
Antiope	6.203125	40151	9CD7h
NABTS	5.727272	37071	90CFh
VPS/WSS	5.0	32363	7E6Bh
WSS 525	1.789673	11584	2D40h
CCx2	1.006993	6518	1976h
CCx1	0.503496	3259	0CBBh

In TV-mode this D-PLL is frozen after CRI, in VCR-mode it is tuned throughout the line using a slow time constant.

Timing informations for freezing the slicing level, stopping the D-PLL and other actions are generated by the timing circuit. It generates all control signals which depend on the data start or on the horizontal sync.

In order to improve the reception performance the actual measured slicing level for each line is stored in the VBI-buffer. Using this slicing level the controller software is able to average the value over several fields for each data line by means of software filtering. If the averaged value becomes stable this value can be used for slicing instead of the internally calculated slicing level.

2.16.3. H/V-Synchronization

Slicer and acquisition interface need a lot of signals which have to be synchronized to the incoming CVBS (e.g. line number, field or line start). Therefore a sync slicing level is calculated and the sync signal is sliced from the filtered digital CVBS signal. Using digital integration vertical and horizontal sync pulses are separated. The horizontal pulses are fed into a digital H-PLL which has flywheel functionality. The H-PLL includes a counter which is used to generate all the necessary horizontal control signals. The vertical sync is used to synchronize the line counter, which is used to generate the vertical control signals.

The synchronization block includes a watchdog which keeps control of the actual lock condition of the H-PLL. The watchdog can produce a channel change interrupt (CC) if synchronization has been lost.

2.16.4. Acquisition Interface

The acquisition interface manages the data transfer between slicer and memory. First of all a bit synchronization is performed (FC-check). Following this, the data is paralleled and as 8 bit words shifted into memory. In the other direction parameters are loaded from memory to the slicer. This parameter download takes place after the vertical sync and after each horizontal sync. The parameters are used for slicer configuration. The acquisition can be switched from normal mode (line 6 to 23) to full channel mode (all lines of field).

2.16.4.1. Framing Code Check

The FC-check is able to handle a number of different framing codes per field. Two of these framing codes are programmable and could therefore be changed from field to field or adapted to new data services.

There are 8 possible framing codes which are compared to the incoming signal line by line. Only a successful framing code match will enable further reception of the incoming data stream in the actual line. Most of the framing codes are hard-wired for reception of known data services like WST, CC, VPS, WSS.

Note: If VPS should be sliced in field 1 and WST in field 2 the appropriate line parameters for line 16 have to be changed dynamically from field to field.

It is also possible to use a programmable 8-bit framing code without error tolerance and a programmable 16-bit framing code with 16-bit don’t care mask to increase error tolerance. Furthermore it is possible to disable the framing code check completely.

By means of the line parameter FC_SEL it is possible to select which framing code is used for the actual line. If NORM is set to WSS then the hard-wired WSS framing code is used independently of FC_SEL setting.

2.16.4.2. Interrupts

Some events which occur inside the slicer, sync separation or acquisition interface will cause an interrupt (L24, AVS, AHS, CC). They are summarized in register CISR0 and CISR1. The hardware sets the associated interrupt flag which must be reset by software before the next interrupt can be accepted.

2.16.5. Software Interface and Algorithms

2.16.5.1. VBI Buffer and Memory Organization

Slicer and acquisition interface need parameters for configuration and they generate status information for the CPU. These parameters and the received teletext data are stored in a XRAM-segment called VBI buffer (see Fig. 2–11 on page 6-53). They are separated in field and line parameters. The field parameters are loaded after each vertical sync signal and are valid until the next vertical sync. The line parameters are loaded within each line or horizontal sync and are valid until the next line or horizontal sync.

The VBI buffer can be located anywhere in the XRAM on 1 Kilobyte boundaries. The start address of the VBI buffer is configured with the parameter VBIADR in the special function register STRVBI. The start address of the VBI buffer should only be changed if the acquisition is switched off. The acquisition can be started and stopped by the controller using bit ACQON of register STRVBI. The acquisition is stopped as soon as this bit changed to ‘0’. If the bit is changed back to ‘1’ the acquisition starts again with the next V-pulse (only if STAB = 1).

13 bytes are needed for the field parameter. 55 bytes have to be reserved for each sliced data line. If 18 lines of data (in full channel mode 313) have been sent to memory no further acquisition takes place until the next vertical pulse appears and the H-PLL is still locked (VS_OK). To avoid VBI buffer overflow at least 1003 bytes (17228 bytes in full channel mode) have to be allocated in the XRAM.

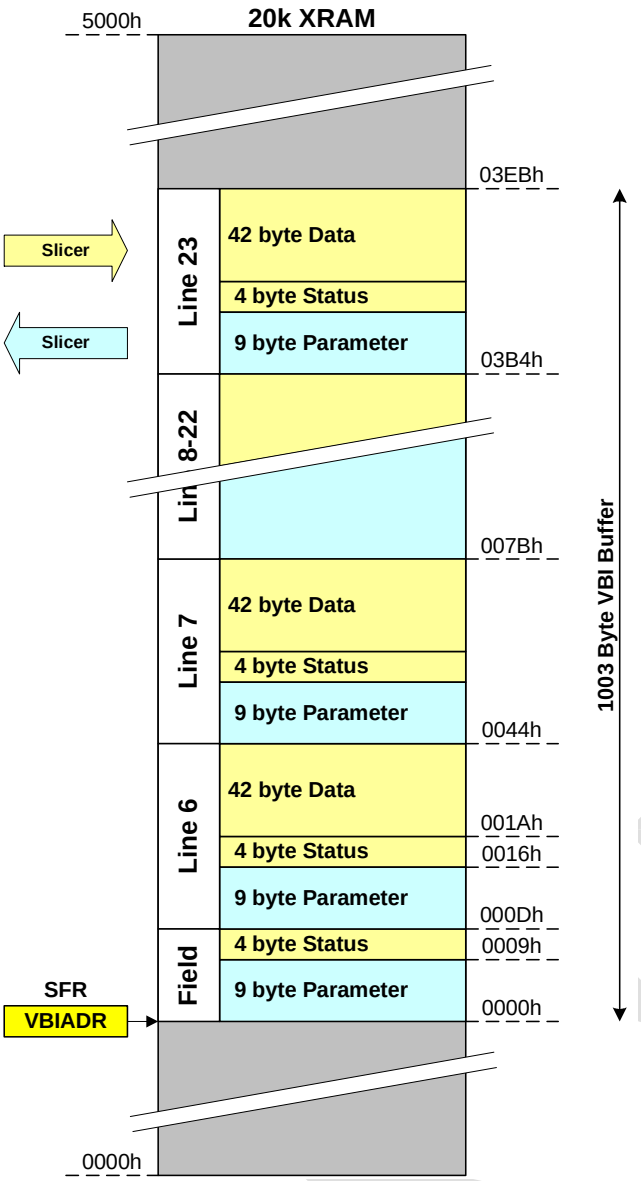


Fig. 2–11: Memory Organization of VBI Buffer

2.16.5.2. Register Description

The acquisition interface has only 1 SFR Register (STRVBI) to setup the VBI buffer address in XRAM and to enable the acquisition. The line and field parameters are stored in the XRAM. They have to be initialized by software before starting the acquisition.

2.16.5.3. Recommended Parameter Settings

Table 2–20: Recommended Field and Line Parameter

Parameter	WST 625/50	NABTS	VPS	WSS 625/50	CC	CCx2	WSS 525/60	VITC 625/50
NORM	0	1	2	3	4	5	6	7
FC_SEL	2	6	3	0	5	7	0	6
FC_PROG8	00h	E4h	00h	00h	00h	00h	00h	00h
FC_PROG16	AAE4h	AAE7h	0000h	0000h	5543h	04edh	FFFFh	0000h
FC_MASK16	0000h	0000h	0000h	0000h	C000h	F000h	FFFFh	0000h
WSS_PREC	00h	00h	00h	0Ah	00h	00h	00h	00h
DINCR	AF68h	90CFh	7E6Bh	7E6Bh	1976h	1976h	2D40h	2DD4h
MLENGTH	0	0	2	1	7	7	7	0
ALENGTH	2	2	2	2	2	2	2	2
CLK_DIV	0	0	0	2	5	5	6	0
TTC_ADJ	0Eh		1Fh	04h	00h	00h	08h	
DATA_STL	0Fh	0Fh	0Fh	0Fh	0Fh	0Fh	0Fh	0Fh
HS_WIN	2	2	2	2	2	2	2	2

AGRD_ON = ANOI_ON = AFRE_ON = ACCU_ON = 1

all other parameter = 0

2.16.6. ACQ Register Block Index

Name	Page
FIELD_PARAMETER	57
FIELD_STATUS	58
LINE_DATA	62
LINE_PARAMETER	59
LINE_STATUS	61

2.16.7. ACQ Register Index

Name	Register	Page
ACCU_ON	ACQLP2	59
AFRE_ON	ACQFP5	57
AGRD_ON	ACQFP5	57
ALENGTH[1:0]	ACQLP4	60
ANOI_ON	ACQFP5	57
BIT_SHUFF	ACQLP2	60
BLACK[0]	ACQFP11	59
BLACK[8:1]	ACQFP10	59
CALC_SLL[0]	ACQLP4	60
CALC_SLL[8:1]	ACQLP3	60
CLK_DIV[2:0]	ACQLP7	60
DATA[7:0]	ACQLD0	62
DATA_STL[0]	ACQLP6	60
DATA_STL[8:1]	ACQLP5	60
DINCR[0]	ACQLP2	60
DINCR[16:9]	ACQLP0	59
DINCR[8:1]	ACQLP1	59
DPHAS_ERR	ACQLP12	62
FC_DET	ACQLP12	62
FC_MASK16[15:8]	ACQFP2	57
FC_MASK16[7:0]	ACQFP3	57
FC_PROG16[15:8]	ACQFP0	57
FC_PROG16[7:0]	ACQFP1	57
FC_PROG8[7:0]	ACQFP4	57
FC_SEL[2:0]	ACQLP8	61
FC_VEC_DET[4:0]	ACQLP12	62
FIELD	ACQFP9	58
FRE_DET	ACQFP9	58
FRE_ON	ACQFP5	57
FREATTL	ACQLP11	62
FULL	ACQFP5	57
GRD_COMP[3:0]	ACQLP7	61
GRD_DET	ACQLP11	61
GRD_ON	ACQFP5	57
GRD_SIGN	ACQLP7	61
HPHAS_ERR	ACQFP11	59
HS_WIN[2:0]	ACQFP6	57
INT_MODE	ACQFP8	58
L525_DET	ACQFP11	59
LEOFLI[11:8]	ACQFP11	59
LEOFLI[7:0]	ACQFP12	59
MEAS_GRD[4:0]	ACQLP11	61
MEAS_SLL[0]	ACQLP11	62
MEAS_SLL[8:1]	ACQLP10	61
MLENGTH[2:0]	ACQLP6	60
MVIS_DET	ACQFP9	59
NOI_HF[3:0]	ACQLP9	61
NOI_HF_DET	ACQFP9	58
NOI_LF[3:0]	ACQLP9	61
NOI_LF_DET	ACQFP9	59
NOI_ON	ACQFP5	57
NOI_THR[3:0]	ACQFP7	58
NORM[2:0]	ACQLP8	61
PLLT_ON	ACQLP2	59
SET_DATA_STL	ACQLP2	59
SET_FIELD_DET	ACQFP8	58
SET_GRD_AVR	ACQFP8	58
SET_HSMODE	ACQFP8	58
SET_SLL	ACQLP2	59
SET_SLLMODE	ACQLP2	59
SET_VS_WIN	ACQFP8	58
STAB	ACQFP9	58
TTC_ADJ[4:0]	ACQLP4	60
VCR	ACQFP5	57
VS_OK	ACQFP9	58
VS_THRE[1:0]	ACQFP7	58
VS_THRM	ACQFP6	57
VS_WIN[1:0]	ACQFP7	58
WSS_PREC[3:0]	ACQFP6	58

2.16.8. ACQ Register Address Index

Table 2–21: ACQ Subaddress Index

Sub	Data Bits								Reset
	7	6	5	4	3	2	1	0	
h0000	FC_PROG16[15:8]								h0000
h0001	FC_PROG16[7:0]								h0000
h0002	FC_MASK16[15:8]								h0000
h0003	FC_MASK16[7:0]								h0000
h0004	FC_PROG8[7:0]								h0000
h0005	AFRE_ON	FRE_ON	AGRD_ON	GRD_ON	VCR	ANOI_ON	NOI_ON	FULL	h0000
h0006	VS_THRM	HS_WIN[2:0]			WSS_PREC[3:0]				h0000
h0007	VS_THRE[1:0]		VS_WIN[1:0]		NOI_THR[3:0]				h0000
h0008	SET_GRD_AVR	INT_MODE	SET_HSMODE	SET_VS_WIN	SET_FIELD_DET				h0000
h0009		FRE_DET	STAB	VS_OK	FIELD	NOI_HF_DET	NOI_LF_DET	MVIS_DET	
h000A	BLACK[8:1]								
h000B	BLACK[0]		HPHAS_ERR	L525_DET	LEOFLI[11:8]				
h000C	LEOFLI[7:0]								
h000D	DINCR[16:9]								h0000
h000E	DINCR[8:1]								h0000
h000F	SET_DATA_STL	SET_SLL	SET_SLLMODE	ACCU_ON	PLLT_ON	BIT_SHUFF		DINCR[0]	h0000
h0010	CALC_SLL[8:1]								h0000
h0011	TTC_ADJ[4:0]					ALENGTH[1:0]		CALC_SLL[0]	h0000
h0012	DATA_STL[8:1]								h0000
h0013		MLENGTH[2:0]						DATA_STL[0]	h0000
h0014	CLK_DIV[2:0]			GRD_SIGN	GRD_COMP[3:0]				h0000
h0015		NORM[2:0]				FC_SEL[2:0]			h0000
h0016	NOI_HF[3:0]				NOI_LF[3:0]				
h0017	MEAS_SLL[8:1]								
h0018	GRD_DET	MEAS_GRD[4:0]					FREATTL	MEAS_SLL[0]	
h0019		FC_VEC_DET[4:0]					DPHAS_ERR	FC_DET	
h001A	DATA[7:0]								

2.16.9. ACQ Register Description

Table 2–22: ACQ Register Description

Name	Addr	Dir	Sync	Reset	Range	Function
FIELD_PARAMETER						
ACQFP0	h0000	RW	VS	h0000		
FC_PROG16[15:8]	h0000[7:0]	RW	VS	0	0..255	
ACQFP1	h0001	RW	VS	h0000		
FC_PROG16[7:0]	h0001[7:0]	RW	VS	0	0..255	**Programmable 16-bit Framing Code** MSB corresponds to first received bit of FC
ACQFP2	h0002	RW	VS	h0000		
FC_MASK16[15:8]	h0002[7:0]	RW	VS	0	0..255	
ACQFP3	h0003	RW	VS	h0000		
FC_MASK16[7:0]	h0003[7:0]	RW	VS	0	0..255	**Mask for Programmable 16-bit Framing Code** MSB corresponds to first received bit of FC 0: this bit is checked 1: this bit is don't care
ACQFP4	h0004	RW	VS	h0000		
FC_PROG8[7:0]	h0004[7:0]	RW	VS	0	0..255	**Programmable 8-bit Framing Code** MSB corresponds to first received bit of FC
ACQFP5	h0005	RW	VS	h0000		
AFRE_ON	h0005[7]	RW	VS	0	0,1	**Automatic Frequency Compensation** 0: compensation controlled by CPU 1: compensation controlled by measurement hardware
FRE_ON	h0005[6]	RW	VS	0	0,1	**Frequency Compensation** 0: frequency compensation depends on AFRE_ON 1: frequency compensation is always on
AGRD_ON	h0005[5]	RW	VS	0	0,1	**Automatic Group Delay Compensation** 0: compensation controlled by CPU 1: compensation controlled by measurement hardware
GRD_ON	h0005[4]	RW	VS	0	0,1	**Group Delay Compensation** 0: group delay compensation depends on AGRD_ON 1: group delay compensation is always on
VCR	h0005[3]	RW	VS	0	0,1	**VCR Mode** 0: D-PLL tuning is stopped after CRI; H-PLL with slow time constant 1: D-PLL is tuned throughout the line; H-PLL with fast time constant; CH_CHANGE is disabled
ANOI_ON	h0005[2]	RW	VS	0	0,1	**Automatic Noise Compensation** 0: compensation controlled by CPU 1: compensation controlled by measurement hardware
NOI_ON	h0005[1]	RW	VS	0	0,1	**Noise Compensation** 0: noise compensation depends on ANOI_ON 1: noise compensation is always on
FULL	h0005[0]	RW	VS	0	0,1	**Full Channel Mode** 0: full channel mode off 1: full channel mode on Note: Donít forget to reserve enough memory for the VBI buffer and to initialize the appropriate line parameters.
ACQFP6	h0006	RW	VS	h0000		
VS_THRM	h0006[7]	RW	VS	0	0,1	**Vsync Threshold Mode** 0: threshold adaptive 1: threshold defined by VS_THRE
HS_WIN[2:0]	h0006[6:4]	RW	VS	0	0..7	**Hsync Window** Defines the width of the window for the acceptance of incoming H-sync pulses 000: +/- 0.92us 001: +/- 1.84us ... 111: +/- 15us

Table 2–22: ACQ Register Description, continued

Name	Addr	Dir	Sync	Reset	Range	Function
WSS_PREC[3:0]	h0006[3:0]	RW	VS	0	0..15	**Precision Control for WSS-FC-Check** This value defines how many error values around edges inside the WSS framing code are accepted. 0: any error acepted 1: 11 errors accepted ... 10: 2 errors accepted 11: 1 error accepted 12: no error accepted
ACQFP7	h0007	RW	VS	h0000		
VS_THRE[1:0]	h0007[7:6]	RW	VS	0	0..3	**Vsync Threshold** Defines the slicing threshold for the incoming V-sync pulses 00: small vsync amplitude ... 11: max vsync amplitude
VS_WIN[1:0]	h0007[5:4]	RW	VS	0	0..3	**Vsync Window** Defines the width of the window for the acceptance of incoming V-sync pulses 00: +/- 4 video lines 01: +/- 5 video lines 10: +/- 6 video lines 11: +/- 7 video lines
NOI_THR[3:0]	h0007[3:0]	RW	VS	0	0..15	**Threshold for Noise Measurement** 0000: weak noise detected ... 1111: strong noise detected
ACQFP8	h0008	RW	VS	h0000		
SET_GRD_AVR	h0008[7]	RW	VS	0	0,1	**Group Delay Measurement Mode** 0: group delay measurement (MEAS_GRD) averaged by hardware 1: raw group delay measurement (MEAS_GRD) for software averaging
INT_MODE	h0008[6]	RW	VS	0	0,1	**Interpolation Mode** 0: FIR interpolation (default) 1: linear interpolation
SET_HSMODE	h0008[5]	RW	VS	0	0,1	**H-PLL Watchdog** 0: enabled 1: disabled
SET_VS_WIN	h0008[4]	RW	VS	0	0,1	**VSYNC Acceptance Window Behavior** 0: vsync accepted only inside VS_WIN 1: vsync always accepted
SET_FIELD_DET	h0008[3]	RW	VS	0	0,1	**Field Detection** 0: free-running with correction circuit if VCR=1 1: normal operation
FIELD_STATUS						
ACQFP9	h0009	R	VS			
FRE_DET	h0009[6]	R	VS		0,1	**Frequency Attenuation Detection** High frequency CVBS components (around 3.5 MHz) are strongly damped (6 to 9 dB) compared to lower frequency CVBS components 0: no frequency depending attenuation has been detected during the last field 1: for at least one text line during the last field frequency depending attenuation has been detected
STAB	h0009[5]	R	VS		0,1	**H-PLL Stable** 0: H-PLL of sync-separation not locked 1: H-PLL of sync-separation locked
VS_OK	h0009[4]	R	VS		0,1	**Vertical Sync Watchdog** 0: vsync not stable 1: vsync stable
FIELD	h0009[3]	R	VS		0,1	**Field Indicator** 0: field 1 1: field 2
NOI_HF_DET	h0009[2]	R	VS		0,1	**High Frequency Noise Detection** 0: high frequency noise below threshold 1: high frequency noise above threshold

Table 2–22: ACQ Register Description, continued

Name	Addr	Dir	Sync	Reset	Range	Function
NOI_LF_DET	h0009[1]	R	VS		0,1	**Low Frequency Noise Detection** 0: low frequency noise below threshold 1: low frequency noise above threshold
MVIS_DET	h0009[0]	R	VS		0,1	**Macrovision Detection** 0: no pseudo sync pulses detected in previous line 1: pseudo sync pulses detected in previous line
ACQFP10	h000A	R	VS			
BLACK[8:1]	h000A[7:0]	R	VS		0..255	**Measured Black Level** The value represents the output of the black level filter (sync separation unit)
ACQFP11	h000B	R	VS			
BLACK[0]	h000B[7]	R	VS		0,1	
HPHAS_ERR	h000B[5]	R	VS		0,1	**H-PLL Phase Error** 0: phase error below threshold 1: phase error above threshold (indicator for vcr-tapes)
L525_DET	h000B[4]	R	VS		0,1	**TV-Norm Detection** 0: 625/50Hz 1: 525/60Hz
LEOFLI[11:8]	h000B[3:0]	R	VS		0..15	**Length of Line** This value is the output of the filter of the H-PLL and represents the actual horizontal period of CVBS in system clock cycles.
ACQFP12	h000C	R	VS			
LEOFLI[7:0]	h000C[7:0]	R	VS		0..255	
LINE_PARAMETER						
ACQLP0	h000D	RW	HS	h0000		
DINCR[16:9]	h000D[7:0]	RW	HS	0	0..255	**D-PLL Increment** Specifies the operating frequency of the D-PLL of the data slicer. DINCR = fdata * 2**18 / 40.5 MHz
ACQLP1	h000E	RW	HS	h0000		
DINCR[8:1]	h000E[7:0]	RW	HS	0	0..255	
ACQLP2	h000F	RW	HS	h0000		
SET_DATA_STL	h000F[7]	RW	HS	0	0,1	**Select Data Start Level** 0: use internal calculated data start level 1: use external data start level from line parameter DATA_STL
SET_SLL	h000F[6]	RW	HS	0	0,1	**Slicing Level Source Selector** The slicer allows the use of an internal calculated slicing level or an external provided slicing level. 0: use internal calculated slicing level 1: use external slicing level from line parameter CALC_SLL
SET_SLLMODE	h000F[5]	RW	HS	0	0,1	**Slicing Level Mode** 0: slicing level from fir lowpass (default) 1: slicing level calculated from data edges (for data services without cri). This setting can be used for low frequency noise compensation (co-channel). Software slicing level filter must be be switched off for compensation.
ACCU_ON	h000F[4]	RW	HS	0	0,1	**Accumulator on** If noise has been detected during automatic mode or if the bit NOI_ON has been set, the internal slicing level calculation can be improved by setting this bit. 0: standard slicing level calculation 1: improved slicing level calculation (improvement depends also on parameter ALENGTH)
PLLT_ON	h000F[3]	RW	HS	0	0,1	**D-PLL tuning on** If noise has been detected during automatic mode or if the bit NOI_ON has been set the D-PLL can be tuned throughout the line by setting this bit. 0: D-PLL is frozen after clock run in 1: D-PLL is tuned throughout the line

Table 2–22: ACQ Register Description, continued

Name	Addr	Dir	Sync	Reset	Range	Function
BIT_SHUFF	h000F[2]	RW	HS	0	0,1	**Bit Shuffle** Bit order of parallel data. WST requires reverse bit order. 0: LSB = left most bit 1: LSB = right most bit
DINCR[0]	h000F[0]	RW	HS	0	0,1	
ACQLP3	h0010	RW	HS	h0000		
CALC_SLL[8:1]	h0010[7:0]	RW	HS	0	0..255	**Calculated Slicing Level** If the bit SET_SLL is set the slicer is using the value of CALC_SLL as slicing level instead of the internal calculated slicing level from the slicing level unit.
ACQLP4	h0011	RW	HS	h0000		
TTC_ADJ[4:0]	h0011[7:3]	RW	HS	0	0..63	**D-PLL Start Phase** depends on the fsample / fdata relationship
ALENGTH[1:0]	h0011[2:1]	RW	HS	0	0..3	**ACCU Length** If noise has been detected or if NOI_ON = 1, the output of the slicing level filter is further averaged by means of an accumulation (arithmetic averaging). ALENGTH specifies the number of slicing level filter output values used for averaging. The accumulation clock depends on CLKDIV. 00: 2 value averaging 01: 4 value averaging 10: 8 value averaging 11: 16 value averaging
CALC_SLL[0]	h0011[0]	RW	HS	0	0,1	
ACQLP5	h0012	RW	HS	h0000		
DATA_STL[8:1]	h0012[7:0]	RW	HS	0	0..255	**Data Start Level** The value is used as threshold for the data-start-comparator of the data slicer. Useful values are between black and maximum of data. This parameter is used only if SET_DATA_STL = 1.
ACQLP6	h0013	RW	HS	h0000		
MLENGTH[2:0]	h0013[6:4]	RW	HS	0	0..7	**Median Filter Length** For noise suppression reasons a median filter has been introduced after the actual data separation because of oversampling successive samples could be averaged. Therefore an odd number of sliced successive samples is taken and if the majority are ë1í a ë1í is sliced otherwise a ë0í. MLENGTH specifies how many samples are taken. 000: 1 sample 001: 3 samples 010: 5 samples 011: 7 samples 100: 9 samples 101: 11 samples 110: 13 samples 111: 15 samples
DATA_STL[0]	h0013[0]	RW	HS	0	0,1	
ACQLP7	h0014	RW	HS	h0000		
CLK_DIV[2:0]	h0014[7:5]	RW	HS	0	0..7	**Clock Divider** The slicing level filter needs to find the DC value of the CVBS during CRI. In order to do this it should suppress at least the CRI frequency. As different services use different data frequencies the CRI frequency will be different as well. Therefore the filter characteristic needs to be shifted. This can be done by using different clocks for the filter. The filter itself shows sufficient suppression for frequencies between 0.061 * SLCLK and 0.13 * SLCLK (SLCLK is the actual filter clock) 000: SLCLK = 1 * fs 001: SLCLK = 1/2 * fs 010: SLCLK = 1/3 * fs 011: SLCLK = 1/4 * fs 100: SLCLK = 1/5 * fs 101: SLCLK = 1/6 * fs 110: SLCLK = 1/7 * fs 111: SLCLK = 1/8 * fs

Table 2–22: ACQ Register Description, continued

Name	Addr	Dir	Sync	Reset	Range	Function
GRD_SIGN	h0014[4]	RW	HS	0	0,1	**Group Delay Compensation Sign** 0: positive group delay compensation 1: negative group delay compensation
GRD_COMP[3:0]	h0014[3:0]	RW	HS	0	0..15	**Group Delay Compensation Magnitude** 0000: small group delay compensation ... 1111: strong group delay compensation
ACQLP8	h0015	RW	HS	h0000		
NORM[2:0]	h0015[6:4]	RW	HS	0	0..7	**Norm Select** Most timing signals are closely related to the actual data service. Therefore 3 bits specify the service received in the actual line. 000: WST 625/50Hz 001: WST 525/60Hz 010: VPS 011: WSS 625/50Hz 100: CC 101: CCx2 110: WSS 525/60Hz 111: VITC
FC_SEL[2:0]	h0015[2:0]	RW	HS	0	0..7	**Framing Code Select** This value selects the framing code used for the actual CVBS line. 000: don't care framing code 001: WST 8-bit 010: WST 16-bit (+parts of cri) 011: VPS 100: CC 8-bit 101: CC 16-bit (+parts of cri) 110: programmable 8-bit framing code 111: programmable 16-bit framing code
LINE_STATUS						
ACQLP9	h0016	R	HS			
NOI_HF[3:0]	h0016[7:4]	R	HS		0..15	**Measured High Frequency Noise** This value is the output of the high frequency noise measurement. 0000: weak high frequency noise ... 1111: strong high frequency noise
NOI_LF[3:0]	h0016[3:0]	R	HS		0..15	**Measured Low Frequency Noise** This value is the output of the low frequency noise measurement (co channel). 0000: weak low frequency noise ... 1111: strong low frequency noise
ACQLP10	h0017	R	HS			
MEAS_SLL[8:1]	h0017[7:0]	R	HS		0..255	**Measured Slicing Level** This value represents the slicing level which has been measured for the current data line. The value can be used to calculate a better slicing level especially for noisy signals by means of software averaging algorithms. The improved slicing level can be set for the following fields by writing to parameter CALC_SLL (SET_SLL=1).
ACQLP11	h0018	R	HS			
GRD_DET	h0018[7]	R	HS		0,1	**Group Delay Detection** 0: no group delay detected 1: group delay detected
MEAS_GRD[4:0]	h0018[6:2]	R	HS		0..31	**Measured Group Delay** x0000: weak group delay ... x1111: strong group delay 0xxxx: positive group delay 1xxxx: negative group delay

Table 2–22: ACQ Register Description, continued

Name	Addr	Dir	Sync	Reset	Range	Function
FREATTL	h0018[1]	R	HS		0,1	**Frequency Depending Attenuation Measurement** High frequency CVBS-components (around 3.5 MHz) are strongly damped (6 to 9 dB) compared to low frequency CVBS-components. 0: no frequency depending attenuation has been detected for the following line 1: strong frequency depending attenuation has been detected for the following line
MEAS_SLL[0]	h0018[0]	R	HS		0,1	
ACQLP12	h0019	R	HS			
FC_VEC_DET[4:0]	h0019[6:2]	R	HS		0..31	**Received Framing Code** Indicator for the actual received framing code xxxx1: WSS xxx1x: PROG-16 or PROG-8 xx1xx: CC-16 or CC-8 x1xxx: VPS 1xxxx: WST-16 or WST-8
DPHAS_ERR	h0019[1]	R	HS		0,1	**Phase Error Watchdog D-PLL** This value is the phase error watchdog output for the current line. The signal shows that the D-PLL found strong phase deviations between D-PLL and sliced data. The signal can be used to detect test lines. 0: no test line 1: probably test line due to strong phase error
FC_DET	h0019[0]	R	HS		0,1	**Framing Code Detection** 0: no framing code has been detected (no new data has been written to memory) 1: the selected framing code has been detected (new data has been written to memory.
LINE_DATA						
ACQLD0	h001A	R	HS			
DATA[7:0]	h001A[7:0]	R	HS		0..255	**Line Data** first byte of 42-byte Line Data Segment

2.17. Display Generator

The display generator is based on the requirements for Level 1.5 Teletext and powerful additional enhanced OSD features.

The display generator reads the contents and attribute settings of the display memory and generates the RGB data for the video back-end signal processing unit.

The display generator uses three 4-bit voltage D/A converters to generate analog RGB output signals with a nominal amplitude of 0.7 V peak-to-peak.

The display can be synchronized to external H/V sync signals (slave mode). The display can be synchronized to 50 Hz as well as to 60 Hz systems. Interlaced display is supported for interlaced sync sources and for non-interlaced ones.

2.17.1. Display Features

- Teletext Level 1.5 feature set
- ROM Character Set to Support all European Languages in Parallel
- Mosaic Graphic Character Set
- Parallel Display Attributes
- Single/Double Width/Height of Characters
- Variable Flash Rate
- Programmable Screen Size (25 Rows × 33 … 64 Columns)
- Flexible Character Matrixes (HxV) 12 × 9 … 16
- Up to 1024 Dynamically Redefinable Characters
- 1/4/16 Colors for DRCS Character
- 1 out of 8 Foreground and Background Colors for 1-bit DRCS and ROM Characters
- Shadowing
- Contrast Reduction
- Pixel by Pixel Shiftable Cursor With up to 4 Different Colors
- Support of Progressive Scan

2.17.2. Display Sync System

The display sync system is completely independent from the acquisition sync system (CVBS timing) and can only work as a sync slave system. Talking about ‘H/V-Syncs’ in this chapter and in Section 2.17. always refers to display related H/V Syncs and never to CVBS related sync timing.

In sync slave mode TVT receives the synchronization information from the video backend which delivers separate horizontal and vertical signals. Due to the not line locked pixel clock generation it can process any possible horizontal and vertical sync frequency.

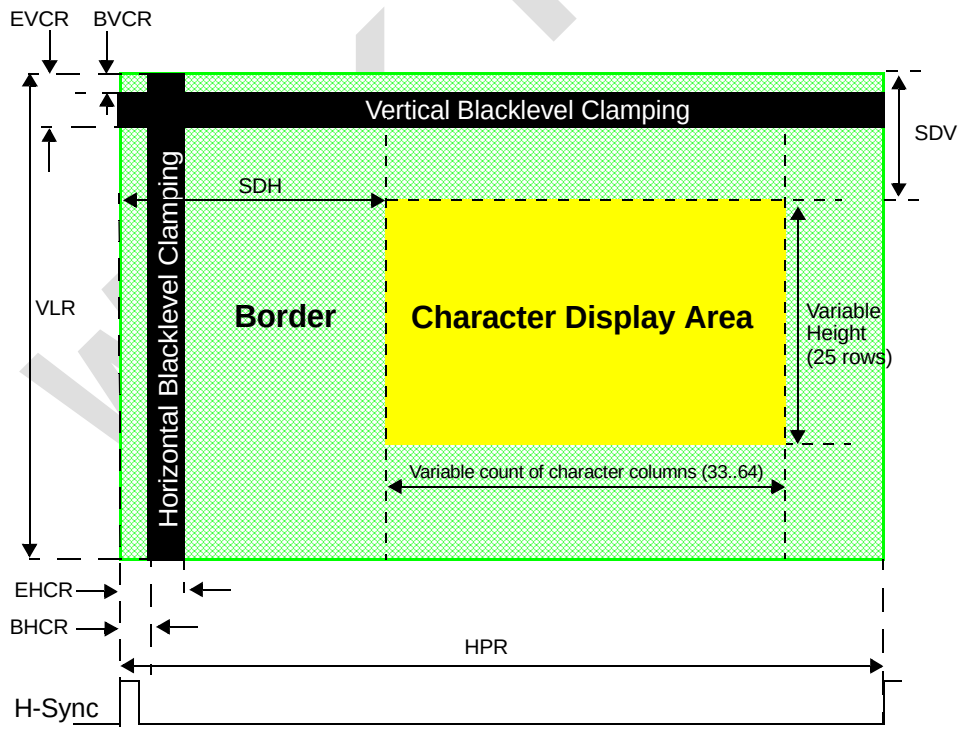


Fig. 2–12: Display timing of the TVT

2.17.2.1. Screen Resolution

The number of displayable pixels on the screen is defined by the pixel frequency (which is independent from horizontal frequency), the line period and number of lines within a field. The screen is divided into three different regions.

2.17.2.1.1. Blacklevel Clamping Area

During horizontal and vertical blacklevel clamping, the black value (RGB = 000) is delivered on output side of TVT. Inside this area the BLANK pin and COR pin are set to the same values which are defined as transparency for subCLUT0 (see Section 2.17.5.8.). This area is programmable in vertical direction (in terms of lines) and in horizontal direction in terms of 40.5 MHz clock cycles.

2.17.2.1.2. Border Area

The size of this area is defined by the sync delay registers (SDH and SDV) and the size of the character display area. The color and transparency of this area is defined by a color look up vector (see Section 2.17.5.4.).

2.17.2.1.3. Character Display Area

Characters and their attributes which are displayed inside this area are programmable according to the specifications of the display generator (see Section 2.17.). The size of that area is defined by attributes inside the gobal display word (see Section 2.17.5.). The start position of that area can be shifted in horizontal and vertical direction by programming the horizontal and vertical sync delay registers (SDH and SDV).

Registers which allow setting up the screen and sync parameters are given in Table 2–23.

User has to take care of setting PCLK and SDH so that SDH/PCLK is greater than 2 µs.

Note: Pixel clock (PCLK) must be appropriately selected to the nearest value in the registers PCLK 0 and PCLK 1.

Table 2–23: Overview of sync register settings

Parameters	Register	Min. Value	Max. Value	Step	Default
Sync Control Register	SCR	see below			
Number of Lines / Field	VLR	1 line	1024 lines	1 line	625 lines
Horizontal Period	HPR	15 µs	122.8 µs	30 ns	64 µs
Pixel Frequency	PCLK	10 MHz	32 MHz	73.25 kHz	12.01 MHz
V-Sync Delay	SDV	4 lines	1024 lines	1 line	32 lines
H-Sync Delay	SDH	32 pixel	2048 pixel	1 pixel	72 pixel
Beginning Of Vertical Clamp Phase	BVCR	1 line	1024 lines	1 line	line 0
End Of Vertical Clamp Phase	EVCR	1 line	1024 lines	1 line	line 4
Beginning Of Horizontal Clamp Phase	BHCR	0 µs	122.8 µs	480 ns	0 µs
End Of Horizontal Clamp Phase	EHCR	0 µs	122.8 µs	480 ns	4.8 µs

Table 2–24 serves as an example, the free programming feature of pixel clock between 10 to 32 MHz makes it possible to adjust and fine-tune the display as per the application requirement.

Table 2–24: Pixel clock and display modes

Character Display Mode	PCLK	$T_{Character\ display\ area}$
40 × 25	12 MHz	40 µs
64 × 25	16 MHz	48 µs
40 × 25	24 MHz	20 µs
64 × 25	32 MHz	24 µs

2.17.2.2. Display Sync Interrupts

The sync unit delivers interrupts (Horizontal and vertical interrupt) to the controller to support the recognition of the frequency of an external sync source. These interrupts are related to the positive edge of the non delayed horizontal and vertical impulses which can be seen at pins HSYNC and VSYNC.

2.17.2.3. Sync Register Description

The clamp phase area has higher priority than the screen background area or the character display area and can be shifted independent from any other register.

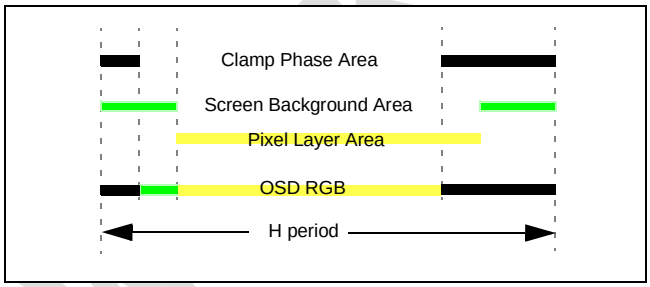


Fig. 2–13: Priority of Clamp Phase, Screen Background and Pixel Layer Area

2.17.2.4. Vertical Field Detection

To realize the odd/even detection of a field next to VSU a second vertical setup time VSU2 is defined by the VSU2 register bits. This horizontal delay is used to recognize the VSYNC to another time than it is recognized at VSU. The field detection is realized by detecting if in between these two latching-points the VSync is rising or stable.

If VSYNC became active for both VSU and VSU2, an odd field is detected. If VSYNC became active only for VSU an even field is detected.

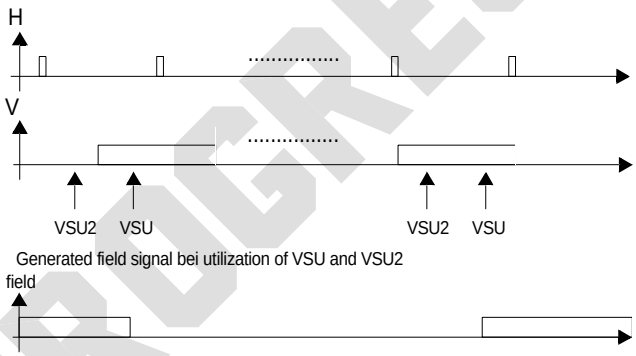


Fig. 2–14: Field detection

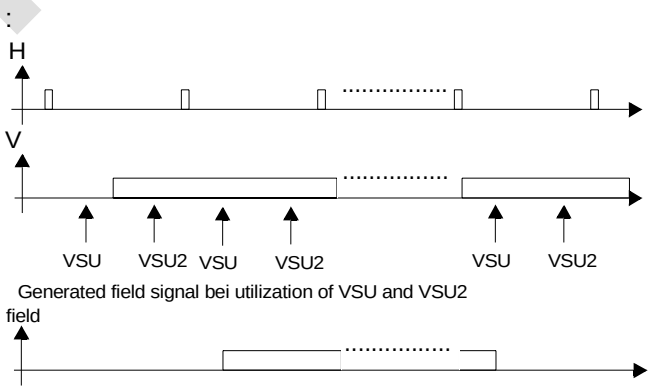


Fig. 2–15: Field detection with inverted VSU and VSU2

2.17.3. Display Memory

The display memory is located inside the internal XRAM. The start address of the display memory is at memory address DISPOINT. This memory address is defined by the user due to a pointer. For each character position three bytes in the display memory are reserved. These three bytes are stored in a serial incremental order for each character and used to define the display attributes of each single character position. The complete amount of allocated display memory depends on the display resolution. In vertical direction the character display area is fixed to 25 rows. In horizontal direction the character display area can be adjusted from 33 up to 64 columns. Table 2–25 is an example for a character display area of 25 rows and 40 columns.

Table 2–25: Display Memory Organization

Row No.	Address	i = 0	…	i = 39
0	DISPOINT + 0_H + i ∗ 3	**Character Display Area**		
1	DISPOINT + 78_H + i ∗ 3			
2	DISPOINT + $F0_H$ + i ∗ 3			
…	…			
23	DISPOINT + $AC8_H$ + i ∗ 3			
24	DISPOINT + $B40_H$ + i ∗ 3			

The following formula helps to calculate a memory address of a character position (X_{CH}, Y_{CH}) depending on the count of characters in horizontal direction (defined in the binary parameters DISALH) and a display start address DISPOINT:

$$CHARADR = DISPOINT + ((Y_{CH} \times (DISALH + 33) + X_{CH}) \times 3)$$

CHARADR = DISPOINT + (Y_{CH} ×(DISALH + 33) + X_{CH}) ×3) hier fehlt eine Klammer!

2.17.4. Character Display Word (CDW)

The character display area content of each character position is defined by a 3-Byte character display word (CDW) in display memory.

2.17.4.1. Access of Characters

The DRCS characters and ROM characters are accessed by a 10-bit character address “CHAR”.

2.17.4.1.1. Address Range from 0_d to 767_d

This address range can either be used to access ROM characters or to access 1-bit DRCS characters.

2.17.4.1.2. Address Range from 768_d to 1023_d

The address range from 768_d to 1023_d is reserved to address the DRCS characters. This range is split into three parts for 1-bit DRCS, 2-bit DRCS and 4-bit DRCS. The boundary between 1-bit DRCS and 2-bit DRCS as well as the boundary between 2-bit DRCS and 4-bit DRCS are defined by two boundary pointers inside the global display word (see Section 2.17.5.).

Table 2–26: Character Display Word (CDW)

Byte	Bit	Name	Function			Cross Reference
			Normal	China	Caption	
0	0	CHAR.0	10-bit Address of ROM or DRCS character		8bit Address of ROM or DRCS character	Section 2.17.4.1.
	1	CHAR.1				
	2	CHAR.2				
	3	CHAR.3				
	4	CHAR.4				
	5	CHAR.5				
	6	CHAR.6				
	7	CHAR.7				
1	0	CHAR.8			Italics	
	1	CHAR.9			Underline	
	2	FLASH	Control of flash modes			Section 2.17.4.2.
	3	UH	Upper half double height			Section 2.17.4.3.
	4	DH	Double height			Section 2.17.4.3.
	5	DW	Double width			Section 2.17.4.4.
	6	BOX	Control for Boxes			Section 2.17.5.7.
	7	CLUT.0	subCLUT select	subCLUT select	subCLUT select	Section 2.17.5.8.
2	0	CLUT.1				
	1	CLUT.2		Char2x2		
	2	FG.0	Foreground color vector			Section 2.17.5.8.1.
	3	FG.1				
	4	FG.2				
	5	BG.0	Background color vector			Section 2.17.5.8.1. Section 2.17.4.2.
	6	BG.1				
	7	BG.2				

2.17.4.2. Flash

Bit FLASH inside character display word (CDW; see also Section 2.17.4.) is used to enable Flash for a character.

Table 2–27: FLASH bit

FLASH	Description
0	steady (flash disabled)
1	flash

The meaning of the flash attribute is different for ROM characters and 1-bit DRCS characters in comparison to the meaning of flash for 2-bit and 4-bit DRCS characters.

For flash rate control refere to the global attribute "FLRATE" in the global display word (see Section 2.17.5.6.).

2.17.4.2.1. Flash for ROM and 1-Bit DRCS Characters

For ROM characters and 1-bit DRCS characters enabled flash causes the foreground pixels to alternate between the foreground and background color vector.

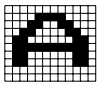
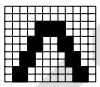
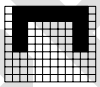
2.17.4.2.2. Flash for 2-Bit and 4-Bit DRCS Characters

For these characters enabled flash causes the DRCS pixels to alternate between the 2-bit/ 4-bit color vector and the background color vector which is defined by the BG attribute inside the character display word (CDW).

2.17.4.3. Character Individual Double Height

Bit UH (Upper half, double height) marks the upper part of a double height character. It is only active, if the DH bit (Double Height) is set to ‘1’. Table 2–28 shows the influence of the DH bit and the UH bit on the character ‘A’.

Table 2–28: Character display depending on DH and UH bit settings

DH	UH	Display
0	X	
1	1	
1	0	

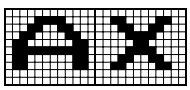
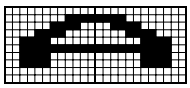
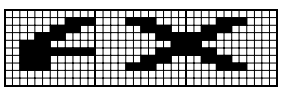
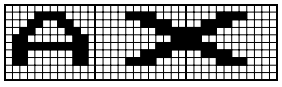
2.17.4.4. Character Individual Double Width

Bit DW (double width) marks the left half of a character with double width. The character to its right will be overwritten by the right half.

If the DW bit of the following character (here the ‘X’) is also set to ‘1’; the right half of the ‘A’ is overwritten by the left half of the ‘X’.

If a character is displayed in double width mode the attribute settings of the left character position are used to display the whole character.

Table 2–29: Character display depending on DW bit settings

DW		Display
Char ’A’	Char ’X’	
0	0	
1	0	
1	1	
0	1	

2.17.5. Global Display Word (GDW)

Next to the parallel attributes stored inside character display word there are global attributes. The settings of the global attributes affect the full screen.

The settings of the global OSD attributes are stored in the global display word (GDW) within 10 Bytes in the XRAM. The location of the GDW is defined by a programmable pointer (see Section 2.17.7.).

Table 2–30: Global Display Word (GDW)

Byte	Bit	Name	Function	Cross Reference
0	0	DISALH.0	Count of display columns in horizontal direction	Section 2.17.5.2.
	1	DISALH.1		
	2	DISALH.2		
	3	DISALH.3		
	4	DISALH.4		
	5	PROGRESS	Used to enable progressive scan mode	Section 2.17.5.11.
	6	CAPTION	Enable Closed Caption mode	
	7	CHINA	Enable combined character mode	
1	0	CURSEN	Enables cursor function	Section 2.17.5.3.
	1	CURHOR.0	Horizontal pixel shift of cursor to character position	
	2	CURHOR.1		
	3	CURHOR.2		
	4	CURHOR.3		
	5	CURVER.0	Vertical pixel shift of cursor to character position	
	6	CURVER.1		
	7	CURVER.2		

Table 2–30: Global Display Word (GDW), continued

Byte	Bit	Name	Function	Cross Reference
2	0	CURVER.3	Vertical pixel shift of cursor to character position	Section 2.17.5.3.
	1	POSHOR.0	Horizontal character position of cursor	
	2	POSHOR.1		
	3	POSHOR.2		
	4	POSHOR.3		
	5	POSHOR.4		
	6	POSHOR.5		
	7	POSVER.0	Vertical character position of cursor	
3	0	POSVER.1		
	1	POSVER.2		
	2	POSVER.3		
	3	POSVER.4		
	4	GLBT_BOX1.0	Used to enable transparency of Box1. CLUT transparency of subCLUT0 can be overruled for destined pixels inside Box1.	Section 2.17.5.7.
	5	GLBT_BOX1.1		
	6	GLBT_BOX1.2		
	7	---	Reserved.	
4	0	BRDCOL.0	Color vector of border	Section 2.17.5.4.
	1	BRDCOL.1		
	2	BRDCOL.2		
	3	BRDCOL.3		
	4	BRDCOL.4		
	5	BRDCOL.5		
	6	BLA_BOX1	Used to define the overruling transparency levels for Box1.	Section 2.17.5.7.
	7	COR_BOX1		
5	0	GDDH.0	Double height of the full screen	Section 2.17.5.5.
	1	GDDH.1		
	2	GDDH.2		
	3	GLBT_BOX0.0	Used to enable transparency of Box0. CLUT transparency of subCLUT0 can be overruled for destined pixels inside Box0.	Section 2.17.5.7.
	4	GLBT_BOX0.1		
	5	GLBT_BOX0.2		
	6	BLA_BOX0	Used to define the overruling transparency levels for Box0.	Section 2.17.5.7.
	7	COR_BOX0		

Table 2–30: Global Display Word (GDW), continued

Byte	Bit	Name	Function	Cross Reference
6	0	CHADRC.0	Defines vertical resolution of DRCS characters.	Section 2.17.5.9.
	1	CHADRC.1		
	2	CHADRC.2		
	3	CHAROM.0	Defines vertical resolution of ROM characters.	
	4	CHAROM.1		
	5	CHAROM.2		
	6	CHAAC	Defines character access mode.	Section 2.17.4.1.
	7	DRCSB0	Used to turn off DRCS boundary	
7	0	DRCSB1.0	Used to define the boundary pointer 1 for DRCS addressing.	Section 2.17.4.1.
	1	DRCSB1.1		
	2	DRCSB1.2		
	3	DRCSB1.3		
	4	DRCSB2.0	Used to define the boundary pointer 2 for DRCS addressing.	Section 2.17.4.1.
	5	DRCSB2.1		
	6	DRCSB2.2		
	7	DRCSB2.3		
8	0	SHEN	Enables shadow.	Section 2.17.5.10.
	1	SHEAWE	Defines if east or west shadow is processed.	
	2	SHCOL.0	Defines the shadow color vector.	
	3	SHCOL.1		
	4	SHCOL.2		
	5	SHCOL.3		
	6	SHCOL.4		
	7	SHCOL.5		
9	0	CURCLUT.0	Used to choose the foreground vector for the cursor (0 … 63).	Section 2.17.5.3.
	1	CURCLUT.1		
	2	CURCLUT.2		
	3	FLRATE.0	Defines the flash rate for flashing characters.	Section 2.17.5.6.
	4	FLRATE.1		
	5	HDWCLUTCOR	Defines the level of COR for the colors of the hardwired CLUT.	Section 2.17.5.8.
	6	HDWCLUTBLANK	Defines the level of BLANK for the colors of the hardwired CLUT.	Section 2.17.5.8.
	7	---	Reserved.	

2.17.5.1. Character Addressing

The DRCS characters and ROM characters are accessed by the 10-bit character address “CHAR” inside the character display word (CDW; (see Section 2.17.4.)).

The selection of ROM or DRCS depends on the following settings in the GDW:

Table 2–31: Character access modes

CHAAC	Description
0	Normal mode: Address range 0_d - 767_d is used to access ROM characters.
1	Enhanced mode: Address range 0_d - 767_d is used to access 1-bit DRCS characters.

Table 2–32: Boundary pointer 1 & 2

DRCSB1 DRCSB2	Description
0	Boundary set to 768_d
1	Boundary set to 784_d
2	Boundary set to 800_d
3	Boundary set to 816_d
…	…
14	Boundary set to 992_d
15	Boundary set to 1008_d

Please note: DRCSB2 must be set to a greater or a equal value than DRCSB1.

Below some examples can be found to show in which way the character addressing depends on the boundary definitions:

Table 2–33: Example1: DRCSB1=5, DRCSB2=10

Character Address		Description
From	To	
768_d	847_d	1-bit DRCS area
848_d	991_d	2-bit DRCS area
928_d	1023_d	4-bit DRCS area

Table 2–34: Example2: DRCSB1=5, DRCSB2=5

Character Address		Description
From	To	
768_d	847_d	1-bit DRCS area
848_d	1023_d	4-bit DRCS area

Table 2–35: Example3: DRCSB1=0, DRCSB2=10

Character Address		Description
From	To	
768_d	927_d	2-bit DRCS area
928_d	1023_d	4-bit DRCS area

2.17.5.2. Character Display Area Resolution

The count of rows of the character display area can be adjusted in a range from 33 to 64 columns in horizontal direction. In vertical direction the character display area is fixed to 25 rows. It depends on the settings for synchronization mode, pixel frequency and character matrix if all these columns are visible on the screen.

The programmable parameter DISALH is the binary representation of an offset value. This offset value plus 33_d gives the count of columns.

Table 2–36: Character display area resolution set by DISALH

DISALH	Description
0	33 columns
1	34 columns
2	35 columns
…	…
15	48 columns
16	49 columns
…	…
30	63 columns
31	64 columns

2.17.5.3. Cursor

The 2-bit color vector matrix of the cursor is stored in the XRAM. A programmable pointer is used, so that the matrix can be stored at any location inside the XRAM (see also Section 2.17.7.3.).

The cursor matrix has the same resolution as the character matrix (see also Section 2.17.5.9.).

If Global Display Double Height (see also Section 2.17.5.5.) is set to double height, the rows which are displayed in double height the cursor is also displayed in double height. For rows which are displayed in normal height, the cursor is also displayed in normal height. If cursor is displayed over two rows and one of these rows is displayed in double height, and the other is displayed in normal height, cursor is also partly displayed in double height and partly in normal height. Cursor-Pixels which are shifted to a non-visible row are also not displayed on the screen.

The cursor can be moved horizontally and vertically, pixel by pixel over the entire character display area.

Table 2–37: Cursor mode setting

CURSEN	Description
0	Cursor mode disabled
1	Cursor mode enabled

The display position of the cursor is determined by a display column value, a display row value and on pixel level by a pixel shift in horizontal and vertical direction.

Cursor can not be shifted more than one character height and one character width on pixel level. Cursor is clipped at border. In full screen double height mode (see also Section 2.17.5.5.) cursor is also displayed in double height.

The pixel shift value is always related to a south-east shift. The pixel shift is determined by the following parameters:

Table 2–38: Character display position (horizontal) setting

CURHOR	Description
0	Horizontal shift of 0
1	Horizontal shift of 1
2	Horizontal shift of 2
3	Horizontal shift of 3
…	…
11	Horizontal shift of 11
>11	not allowed

Table 2–39: Character display position (vertical) setting

CURVER	Description
0	Vertical shift of 0
1	Vertical shift of 1
2	Vertical shift of 2
3	Vertical shift of 3
…	…

Table 2–39: Character display position (vertical) setting, continued

CURVER	Description
14	Vertical shift of 14
15	Vertical shift of 15

The character position of the cursor is determined by the following parameters:

Table 2–40: Cursor position (horizontal) setting

POSHOR	Description
0	Horizontal character column 0
1	Horizontal character column 1
…	…
62	Horizontal character column 62
63	Horizontal character column 63

Table 2–41: Cursor position (vertical) setting

POSVER	Description
0	Vertical character row 0
1	Vertical character row 1
2	Vertical character row 2
3	Vertical character row 3
…	…
30	Vertical character row 30
31	Vertical character row 31

Character position and pixel position have to be changed in parallel. Otherwise it may appear that the character position already has been changed to a new position, but the pixel position is still set to the former value. This may cause a “jumping” cursor.

To avoid this “jumping” cursor there is a EN_LD_GDW (enable load GDW) bit in the SFR bank. If this bit is set to ‘0’ the global display word can be changed without any effect on the screen and in consequence the cursor position can be changed without any effect on the screen. To update the character display area, EN_LD_GDW has to be set to 1 for at least one V period (approximately 50 ms).

The cursor is handled as a layer above the character display area. Pixels of the 2-bit cursor bitplane which are set to ‘00’ are transparent to the OSD/Video layer below. So the cursor can be transparent to the OSD (in case of no transparency of OSD) or to video (in case of transparency of OSD).

Example:

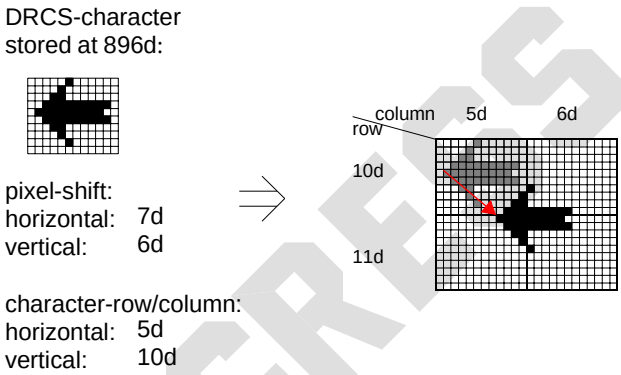


Fig. 2–16: Positioning of HW Cursor

One out of 8 subCLUTs is used to display the cursor. The parameter CURCLUT is used to select the sub-CLUT which is used for color look up of the cursor.

For detailed information of CLUT access see Section 2.17.5.8.

2.17.5.4. Border Color

Next to the character display area in which the characters are displayed there is a area which is surrounding the character display area. The visibility of this border area depends on the width and height of the character display area. The global attribute BRDCOL in the global display word GDW is used to define the color vector of this border (see Section 2.17.5.8.).

2.17.5.5. Full Screen Double Height

If double height is enabled for the full screen each line of the OSD is repeated twice at the RGB output. As a result, characters which are normally displayed in normal height, are now displayed in double height and characters which are normally displayed in double height are now displayed in quadruple height.

Row 0 and 24 are handled in a special way. If double height is selected for the full screen these two rows can be fixed to normal display (each line of these rows is repeated only once).

In double height mode user may want to start the processing of the display at row 12 and not at row 0. To decide this, three bits are used as a global attribute.

Table 2–42: Full screen double height

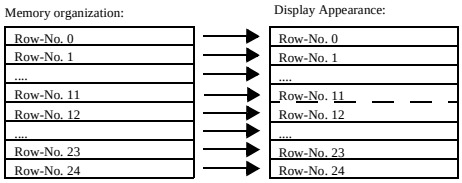
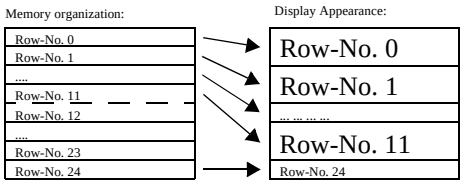
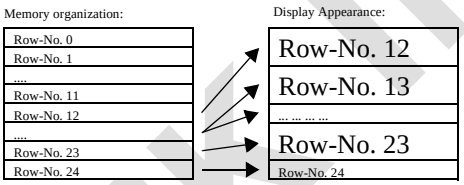
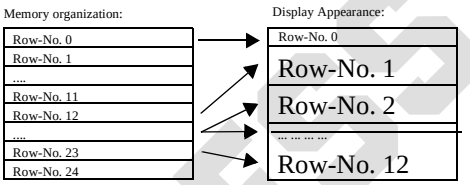
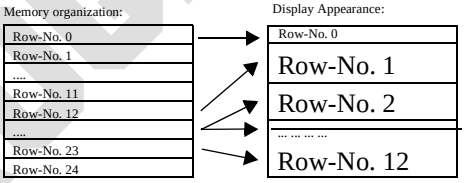
GDDH	Display Area
0	Full Screen Normal Height 
1	Full Screen Double Height Rows 0-11 are displayed in double height. Row 24 is settled on bottom of display in normal height. 
2	Full Screen Double Height Rows 12-23 are displayed in double height. Row 24 is settled on bottom of display in normal height. 

Table 2–42: Full screen double height, continued

GDDH	Display Area
3	Full Screen Double Height Rows 13-24 are displayed in double height. Row 0 is settled on top of display in normal height. 
>3	Full Screen Double Height Rows 1-12 are displayed in double height. Row 0 is settled on top of display in normal height. 

2.17.5.6. Flash Rate Control

This attribute is used to control the flash rate for the full screen. All the characters on the screen for which flash is enabled are flashing with same frequency and in the same phase. The duty cycle is approximately 50%. The flash rate is derived from display V pulse.

Table 2–43: Flash rate control setting

FLRATE	Description
0	Slow flash rate. For 50 Hz systems the flash rate is approximately 0.5 Hz.
1	Medium flash rate. For 50 Hz systems the flash rate is approximately 1.0 Hz.
>1	Fast flash rate. For 50 Hz systems the flash rate is approximately 2.0 Hz.

2.17.5.7. Transparency of Boxes

For characters which are using subCLUT0 the transparency which is defined for the whole CLUT (see Section 2.17.5.8.) can be overruled for foreground or background pixels. There are two different definitions for two box areas to define this overruling. Which of these two box transparencies is used, is selected character individual inside the bit BOX in CDW (see Section 2.17.4.).

Transparency definition for characters for BOX0:

Table 2–44: BOX0 transparency setting

GLBT_BOX0	Description
0 or 4	Box transparency is disabled for BOX0. For all pixels the global defined transparency of subCLUT0 is used.
1	Box transparency is enabled for BOX0 for foreground pixels of ROM characters.
2	Box transparency is enabled for BOX0 for foreground pixels of 1-bit DRCS characters.
3	Box transparency is enabled for BOX0 for foreground pixels of ROM and 1-bit DRCS characters.
5	Box transparency is enabled for BOX0 for background pixels of ROM characters.
6	Box transparency is enabled for BOX0 for background pixels of 1-bit DRCS characters.
7	Box transparency is enabled for BOX0 for background pixels of ROM and 1-bit DRCS characters.

Transparency definition for characters for which BOX is set to 1 and which are using subCLUT0:

Table 2–45: BOX1 transparency setting

GLBT_BOX1	Description
0 or 4	Box transparency is disabled for BOX1.
1	Box transparency is enabled for BOX1 for foreground pixels of ROM characters.
2	Box transparency is enabled for BOX1 for foreground pixels of 1-bit DRCS characters.
3	Box transparency is enabled for BOX1 for foreground pixels of ROM and 1-bit DRCS characters.
5	Box transparency is enabled for BOX1 for background pixels of ROM characters.
6	Box transparency is enabled for BOX1 for background pixels of 1-bit DRCS characters.
7	Box transparency is enabled for BOX1 for background pixels of ROM and 1-bit DRCS characters.

Box0 transparency levels of COR and BLANK are overruled by the global attributes COR_BOX0 and BLA_BOX0.

Box1 transparency levels of COR and BLANK coming from subCLUT0 are overruled by the global attributes COR_BOX1 and BLA_BOX1.

The cursor (see Section 2.17.5.3.) is not affected by the transparency bits.

2.17.5.8. CLUT

The CLUT has a maximum width of 64 entries. The RGB values of the CLUT entries from 0-15 are hard-wired and can not be changed by software.

The contrast reduction and transparency (COR and BLANK) signals for the hardwired CLUT values are set by the global attributes “HDWCLUTCOR“ and “HDW-CLUTBLANK” inside the global display word GDW (see Section 2.17.5.). These attributes also define the polarity of the COR and BLANK signals during black clamp phase (see Section 2.17.2.).

The global settings of COR and BLANK can be over-ruled inside of boxes (see Section 2.17.5.7.).

The RGB values of the CLUT entries from 16 to 63 are programmable. The RGB values of the CLUT are organized in the TVT XRAM in an incremental serial order. CLUT locations inside XRAM which are not used for OSD can be used for any other storage pur-poses.

Each of the 48 programmable CLUT entries holds 2 bytes of data. They define a 3×4-bit RGB value plus the behavior of the COR and BLANK signals. The fol-lowing format is used:

Table 2–46: CLUT Data Format

CLUT Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
+ 0	Green				Blue			
+ 1	reserved		COR	Blank	Red			

The CLUT is divided in 8 subCLUTs with 8 entries for 1-bit DRCS and ROM characters. For 2-bit DRCS characters the CLUT is divided in 8 subCLUTs with 4 entries. For 4-bit DRCS characters the CLUT is divided in 4 subCLUTs with 16 entries.

The subCLUTs can be selected for each character position individually using the “CLUT” attribute inside the character display word CDW (see Section 2.17.4.):

Table 2–47: subCLUT selection

CLUT	ROM and 1-Bit/ 2-Bit DRCS Characters	4-Bit DRCS Characters
0	subCLUT0	subCLUT0
1	subCLUT1	subCLUT1
2	subCLUT2	subCLUT2
3	subCLUT3	subCLUT3
4	subCLUT4	subCLUT0
5	subCLUT5	subCLUT1
6	subCLUT6	subCLUT2
7	subCLUT7	subCLUT3
see Section 2.17.4.: Character Display Word (CDW)		

2.17.5.8.1. CLUT Access for ROM and 1-bit DRCS Characters

Within a ROM or 1-bit DRCS character matrix a 1-bit background/foreground information is available for each pixel. This 1-bit information selects either the foreground “FG” or the background “BG” attribute inside the character display word CDW to address 1 out of 8 subCLUT entries.

2.17.5.8.2. CLUT Access for 2-Bit DRCS Characters

Within a 2-bit DRCS character matrix a 2-bit color information is available for each pixel. This 2-bit infor-mation selects 1 out of 4 subCLUT entries.

2.17.5.8.3. CLUT Access for 4-Bit DRCS Characters

Within a 4-bit DRCS character matrix a 4-bit color information is available for each pixel. This 4-bit infor-mation selects 1 out of 16 subCLUT entries.

Table 2–48: Organization of CLUT

CLUT Address Offset to CLUTPOINT	CLUT Entry	subCLUT No for ROM and 1-Bit DRCS Character		subCLUT No for Cursor		subCLUT No for 2-Bit DRCS Character		subCLUT No for 4-Bit DRCS Character		CLUT Data		
		No.	Entry	No.	Entry	No.	Entry	No.	Entry	R	G	B
not available	0	0	0	not available	0	not available	0	0	0	00_d	00_d	00_d
not available	1		1		1		1		1	15_d	00_d	00_d
not available	2		2		2		2		2	00_d	15_d	00_d
not available	3		3		3		3		3	15_d	15_d	00_d
not available	4		4	not available	0	not available	0		4	00_d	00_d	15_d
not available	5		5		1		1		5	15_d	00_d	15_d
not available	6		6		2		2		6	00_d	15_d	15_d
not available	7		7		3		3		7	15_d	15_d	15_d
not available	8	1	0	not available	0	not available	0	0	8	00_d	00_d	00_d
not available	9		1		1		1		9	07_d	00_d	00_d
not available	10		2		2		2		10	00_d	07_d	00_d
not available	11		3		3		3		11	07_d	07_d	00_d
not available	12		4	not available	0	not available	0		12	00_d	00_d	07_d
not available	13		5		1		1		13	07_d	00_d	07_d
not available	14		6		2		2		14	00_d	07_d	07_d
not available	15		7		3		3		15	07_d	07_d	07_d
00_H	16	2	0	0	0	0	0	1	0	programmable (see Table 2–46)		
02_H	17		1		1		1		1			
04_H	18		2		2		2		2			
06_H	19		3		3		3		3			
08_H	20		4	1	0	1	0		4			
$0A_H$	21		5		1		1		5			
$0C_H$	22		6		2		2		6			
$0E_H$	23		7		3		3		7			
10_H	24	3	0	2	0	2	0		8			
12_H	25		1		1		1		9			
14_H	26		2		2		2		10			
16_H	27		3		3		3		11			
18_H	28		4	3	0	3	0		12			
$1A_H$	29		5		1		1		13			
$1C_H$	30		6		2		2		14			
$1E_H$	31		7		3		3		15			

Table 2–48: Organization of CLUT, continued

CLUT Address Offset to CLUTPOINT	CLUT Entry	subCLUT No for ROM and 1-Bit DRCS Character		subCLUT No for Cursor		subCLUT No for 2-Bit DRCS Character		subCLUT No for 4-Bit DRCS Character		CLUT Data		
		No.	Entry	No.	Entry	No.	Entry	No.	Entry	R	G	B
20_H	32	4	0	4	0	4	0	2	0			
22_H	33		1		1		1		1			
24_H	34		2		2		2		2			
26_H	35		3		3		3		3			
28_H	36		4	5	0	5	0		4			
$2A_H$	37		5		1		1		5			
$2C_H$	38		6		2		2		6			
$2E_H$	39		7		3		3		7			
30_H	40	5	0	6	0	6	0		8			
32_H	41		1		1		1		9			
34_H	42		2		2		2		10			
36_H	43		3		3		3		11			
38_H	44		4	7	0	7	0		12			
$3A_H$	45		5		1		1		13			
$3C_H$	46		6		2		2		14			
$3E_H$	47		7		3		3		15			
40_H	48	6	0	not available	0	not available	0	3	0			
42_H	49		1		1		1		1			
44_H	50		2		2		2		2			
46_H	51		3		3		3		3			
48_H	52		4	not available	0	not available	0		4			
$4A_H$	53		5		1		1		5			
$4C_H$	54		6		2		2		6			
$4E_H$	55		7		3		3		7			
50_H	56	7	0	not available	0	not available	0		8			
52_H	57		1		1		1		9			
54_H	58		2		2		2		10			
56_H	59		3		3		3		11			
58_H	60		4	not available	0	not available	0		12			
$5A_H$	61		5		1		1		13			
$5C_H$	62		6		2		2		14			
$5E_H$	63		7		3		3		15			

2.17.5.9. Character Resolution

The character matrix of DRCS characters can be adjusted in vertical direction from 9 lines up to 16 lines. In horizontal direction the character matrix is fixed to 12 pixels.

The character matrix of the ROM characters can also be adjusted in vertical direction from 9 lines up to 16 lines. In horizontal direction the ROM character matrix is fixed to 12 pixels:

Table 2–49: Character matrix adjustment of DRCS and ROM characters

CHADRC CHAROM	Description
0	9 lines
1	10 lines
2	11 lines
3	12 lines
4	13 lines
5	14 lines
6	15 lines
7	16 lines

The parameter CHAROM is used to characterize the organization of ROM characters. The parameter CHADRC is used to characterize the organization of DRCS characters and the vertical count of lines for a character row on output side. If the count of lines of ROM characters is smaller than the count of DRCS characters the lines of ROM characters are filled up with background colored pixels.

2.17.5.10. Shadowing

If shadowing is enabled the ROM characters and 1-bit DRCS characters of the characters are displayed by west shadow or east shadow. The color vector of the shadow is defined by software. The shadow color vector has a width of 6 bit.

The shadow feature is enabled by the bit SHEN and can be set into 2 modes by the bit SHEAWE.

Table 2–50: Shadow enable

SHEN	Description
0	Shadow disabled.
1	Shadow for ROM characters and 1-bit DRCS characters.

Table 2–51: Shadow options

SHEAWE	Description
0	East shadowing.
1	West shadowing.

CLUT entries from 0-63 can be used as a shadow color vector. The attribute SHCOL in the global display word GDW defines the CLUT entry for the shadow color (see Section 2.17.5.8.).

Example for a “A” displayed in shadow mode:

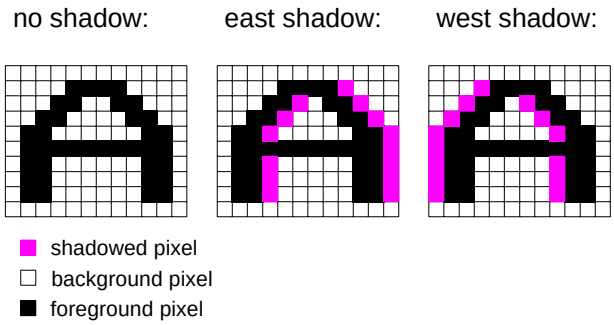


Fig. 2–17: Processing of Shadowing

Within one character matrix shadowing is only processed for the pixels which are belonging to that character matrix. Pixels of one character matrix can not generate a shadow inside a neighbored character matrix.

2.17.5.11. Progressive Scan

This feature is useful for TV-devices in which a frame consists of 1 field with 625 lines instead of 2 fields with 312.5 lines each.

For this TV-fields the RGB-output lines can be repeated twice by enabling the progressive scan feature. This repetition of lines in vertical direction is only processed for lines inside the character display area.

Table 2–52: Progressive scan support

Progress	Description
0	Progressive scan support is disabled.
1	Progressive scan support is enabled.

2.17.6. DRCS Characters

DRCS characters are defined by the user. Up to 16 different colors can be used within one DRCS.

DRCS characters are available in the XRAM. There are three different DRCS color resolution formats available:

– 1-bit per pixel DRCS characters (2 colors)

– 2-bit per pixel DRCS characters (4 colors)

– 4-bit per pixel DRCS characters (16 colors)

In which way this 1-bit, 2-bit or 4-bit color vector information is used to access the CLUT, see Section 2.17.5.8.

2.17.6.1. Memory Organization of DRCS

The following examples are proceeded on the assumption that a height of 11 character lines is selected. The memory organization behaves the same for any other count of lines.

Each character starts at a new byte address. This causes, that for odd heights nibbles may be left free.

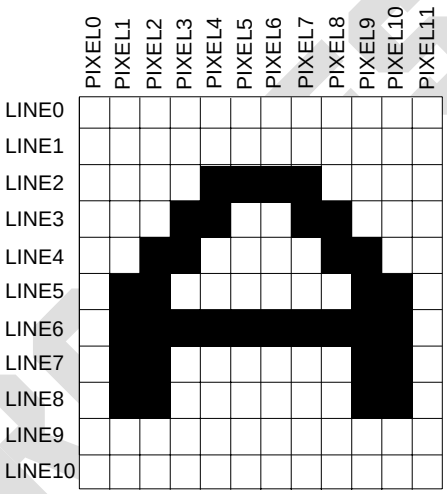


Fig. 2–18: Pixel allocation in the character matrix

Table 2–53: 1-Bit DRCS Characters

Char	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	DRC1POINT + 00_H	LINE 0							
		PIXEL 0	PIXEL 1	PIXEL 2	PIXEL 3	PIXEL 4	PIXEL 5	PIXEL 6	PIXEL 7
		BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0
	DRC1POINT + 01_H	LINE 0				LINE 1			
		PIXEL 8	PIXEL 9	PIXEL 10	PIXEL 11	PIXEL 0	PIXEL 1	PIXEL 2	PIXEL 3
		BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0
	DRC1POINT + 02_H	LINE 1							
		PIXEL 4	PIXEL 5	PIXEL 6	PIXEL 7	PIXEL 8	PIXEL 9	PIXEL 10	PIXEL 11
		BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0
	…	…							
	DRC1POINT + 10_H	LINE 10				left free			
		PIXEL 8	PIXEL 9	PIXEL 10	PIXEL 11				
		BIT 0	BIT 0	BIT 0	BIT 0				
2	DRC1POINT + 11_H	LINE 0							
		PIXEL 0	PIXEL 1	PIXEL 2	PIXEL 3	PIXEL 4	PIXEL 5	PIXEL 6	PIXEL 7
		BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0	BIT 0
…	…	…							

Table 2–54: 2-Bit DRCS Characters

Char	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	DRC2POINT + 00_H	LINE 0							
		PIXEL 0		PIXEL 1		PIXEL 2		PIXEL 3	
		BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1
	DRC2POINT + 01_H	LINE 0							
		PIXEL 4		PIXEL 5		PIXEL 6		PIXEL 7	
		BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1
	DRC2POINT + 02_H	LINE 0							
		PIXEL 8		PIXEL 9		PIXEL 10		PIXEL 11	
		BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1
	…	…							
	DRC2POINT + 20_H	LINE 10							
		PIXEL 8		PIXEL 9		PIXEL 10		PIXEL 11	
		BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1

Table 2–54: 2-Bit DRCS Characters, continued

Char	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2	DRC2POINT + 21_H	LINE 0							
		PIXEL 0		PIXEL 1		PIXEL 2		PIXEL 3	
		BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1	BIT 0	BIT 1
...	...	...							

Table 2–55: 4-Bit DRCS Characters

Char	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	DRC4POINT + 00_H	LINE 0							
		PIXEL 0				PIXEL 1			
		BIT 0	BIT 1	BIT 2	BIT 3	BIT 0	BIT 1	BIT 2	BIT 3
	DRC4POINT + 01_H	LINE 0							
		PIXEL 2				PIXEL 3			
		BIT 0	BIT 1	BIT 2	BIT 3	BIT 0	BIT 1	BIT 2	BIT 3
	DRC4POINT + 02_H	LINE 0							
		PIXEL 4				PIXEL 5			
		BIT 0	BIT 1	BIT 2	BIT 3	BIT 0	BIT 1	BIT 2	BIT 3
	...	...							
	DRC4POINT + 41_H	LINE 10							
		PIXEL 10				PIXEL 11			
		BIT 0	BIT 1	BIT 2	BIT 3	BIT 0	BIT 1	BIT 2	BIT 3
2	DRC4POINT + 42_H	LINE 0							
		PIXEL 0				PIXEL 1			
		BIT 0	BIT 1	BIT 2	BIT 3	BIT 0	BIT 1	BIT 2	BIT 3
...	...	...							

2.17.7. Memory Organization

The memory organization concept of the OSD is based on a flexible pointer concept. All display memory registers reside in the internal XRAM only.

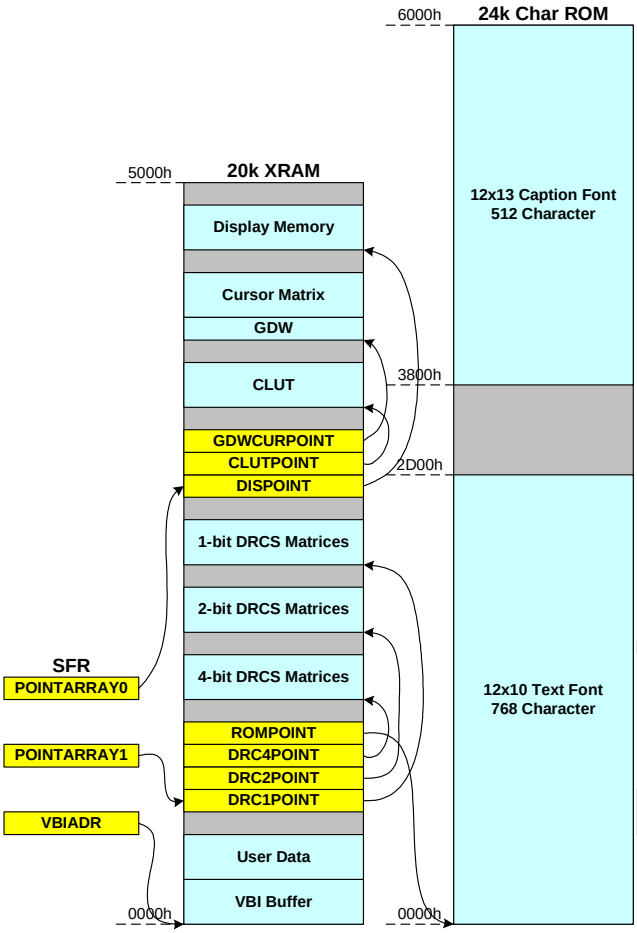


Fig. 2–19: Memory Organization of On-Screen Display

There are 4 bytes of SFR registers which define 2 16-bit pointers POINTARRAY0 and POINTARRAY1 pointing to tw separate pointer arrays inside the XRAM.

These 2 pointer arrays in XRAM contain pointers to the start addresses of the following memory areas:

– Start address of character display area memory
– Start address of CLUT
– Start address of 1-bit DRCS character matrices
– Start address of 2-bit DRCS character matrices
– Start address of 4-bit DRCS character matrices
– Start address of 1-bit ROM character matrices
– Start address of global display word / cursor matrix

User has to take care with the pointer definition, so that memory areas do not overlap each other on the one hand and that the definition is optimized so that no memory is wasted, on the other hand. The length of the global display word is fixed to 10 byte and the length of the CLUT is fixed to 2×48 byte. The length of all the other areas depend on the OSD requirements (see Section 2.17.7.1. to Section 2.17.7.4.).

Each pointer in the pointer array has a width of 16 bits and uses 2 bytes inside the XRAM. They are stored low byte first.

Table 2–56: Pointers of pointer array

Pointer Array	Offset	Name
0	0 = low byte 1 = high byte	DISPOINT
	2 = low byte 3 = high byte	CLUTPOINT
	4 = low byte 5 = high byte	GDWCURPOINT
1	0 = low byte 1 = high byte	DRC1POINT
	2 = low byte 3 = high byte	DRC2POINT
	4 = low byte 5 = high byte	DRC4POINT
	6 = low byte 7 = high byte	ROMPOINT

2.17.7.1. Character Display Area

The character display area consists of 3 bytes for each character position of the character display area. These three bytes are used to store the character display word as it is described in Section 2.17.4..

The array is sorted in a incremental serial order coming from the top left character throughout the bottom right character of the character display area. For further information see Section 2.17.3..

The length of this display memory area depends on the parameter settings of DISALH.

2.17.7.2. CLUT Area

The CLUT area consist of 48 × 2 Byte CLUT contents. The CLUT contents are stored in a serial incremental order.

For further information see Section 2.17.5.8..

2.17.7.3. Global Display Word/Cursor

The area of the global display word is fixed to 10 byte. All the global display relevant informations are stored inside global display word (see Section 2.17.5.). The cursor matrix for cursor display is stored after the global display word. The length of the memory area of cursor matrix depends on the settings of CHADRC.

2.17.7.4. 1-Bit/2-Bit/4-Bit DRCS Character

In this area the pixel information of the dynamically reconfigurable characters is stored. The length of these areas depends on the settings of DRCSB1 and DRCSB2. For further information on the memory format refer to Section 2.17.6.: DRCS Characters.

2.17.7.5. Overview of the SFR Registers

Other than the settings in the XRAM, SFR registers are used for OSD control.

2.17.8. On-Chip ROM Characters

Fig. 2–20: 12x10 ROM Character 000-07F

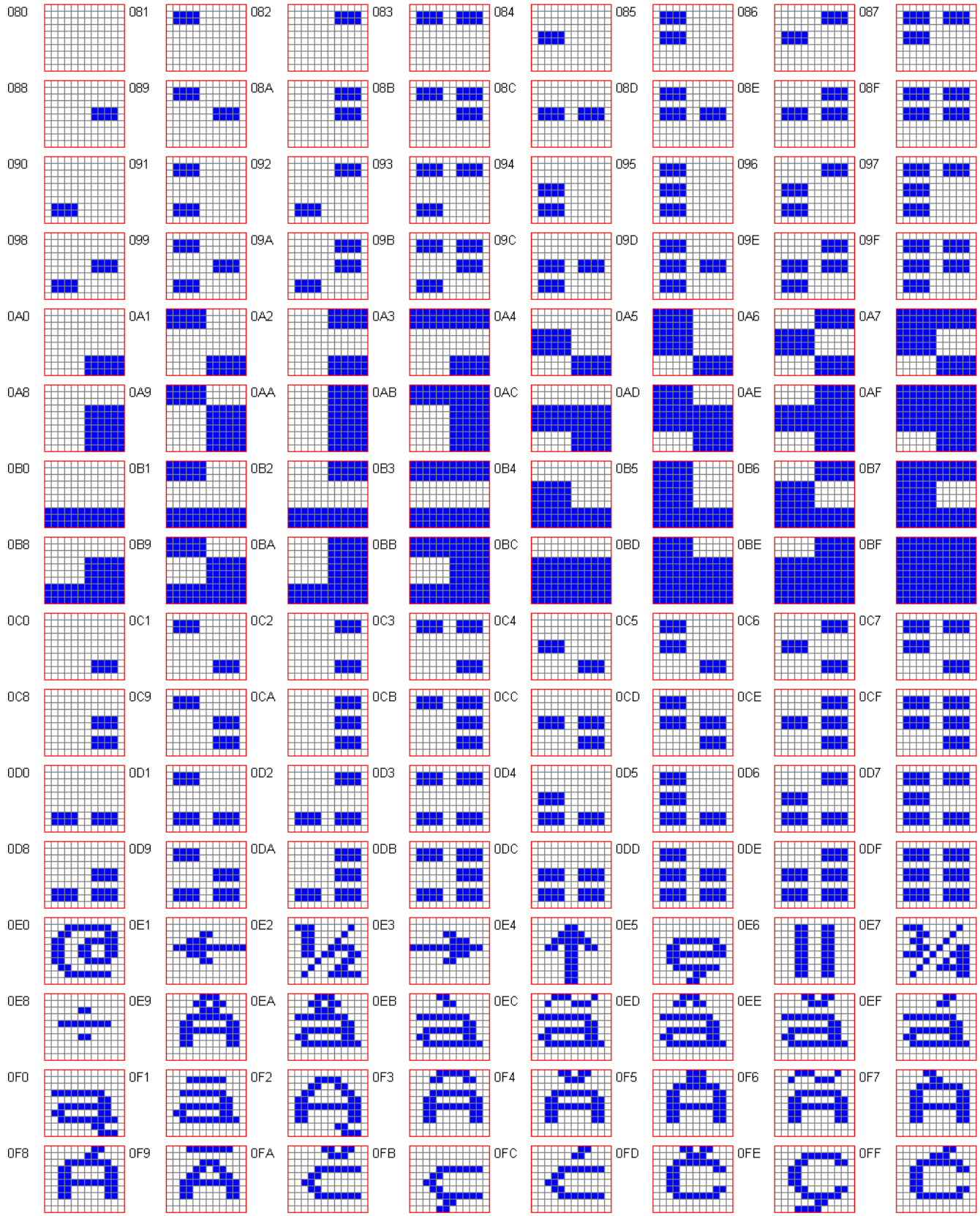


Fig. 2–21: 12x10 ROM Character 080-0FF

Fig. 2–22: 12x10 ROM Character 100-17F

Fig. 2–23: 12x10 ROM Character 180-1FF

Fig. 2–24: 12x10 ROM Character 200-27F

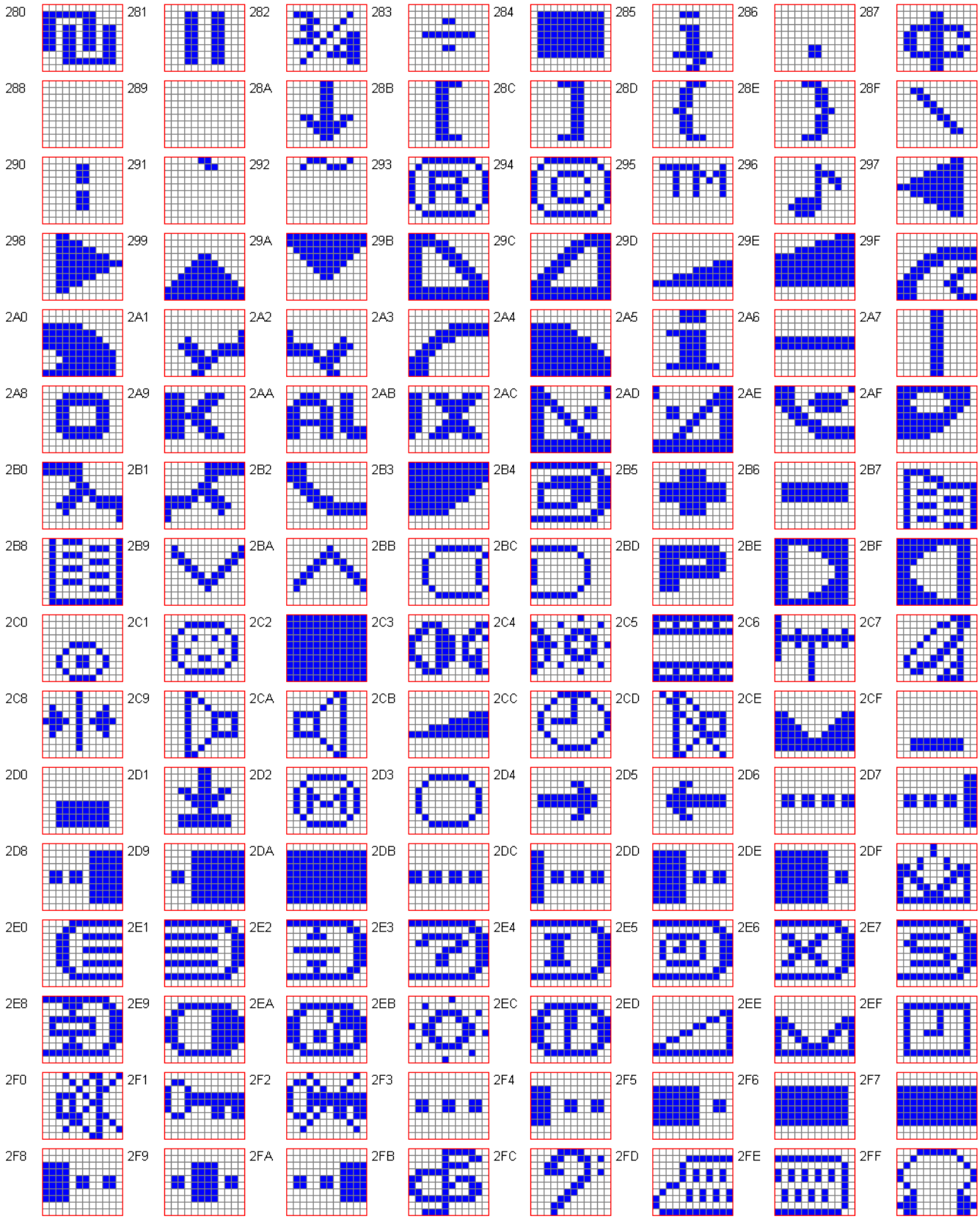


Fig. 2–25: 12x10 ROM Character 280-2FF

Fig. 2–26: 12x13 ROM Character 000-07F

Fig. 2–27: 12x13 ROM Character 080-0FF

Fig. 2–28: 12x13 ROM Character 100-17F

Fig. 2–29: 12x13 ROM Character 180-1FF

3. Special Function Register (SFR)

3.1. SFR Register Block Index

3.2. SFR Register Index

3.3. SFR Register Address Index

Table 3–1: SFR Subaddress Index

Sub	Data Bits								Reset
	7	6	5	4	3	2	1	0	
h80	P1[7:0]								h00FF
h81	SP[7:0]								h0007
h82	DPL[7:0]								h0000
h83	DPH[7:0]								h0000
h84						DPSEL[2:0]			h0000
h87	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE	h0000
h88	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	h0000
h89	GATE1	CNT1	M1[1:0]		GATE0	CNT0	M0[1:0]		h0000
h8A	TL0[7:0]								h0000
h8B	TL1[7:0]								h0000
h8C	TH0[7:0]								h0000
h8D	TH1[7:0]								h0000
h8E	RTCDATA[7:0]								h0000
h8F	RTCSUB[3:0]				RTCRW				h0000
h90	P2[7:0]								h00FF
h92	PMUX1[7:0]								h0000
h93	PMUX2[7:0]								h0000
h94	CB[19:16]				NB[19:16]				h0000
h95	MM	MB[18:16]			IB[19:16]				h0000
h96	MB[19]	UB3	UB4	MX[19]	MXM	MX[19]			h0000
h97	MXSP[7:0]								h0000
h98	SM[1:0]		SM2	REN	TB8	RB8	TI	RI	h0000
h99	SBUF[7:0]								h0000
h9A	LASTB	SCL	REPEAT	IGNACK	INTEN	MASTEN	FAST	PDOWN	h0000
h9B	I2CDATA[7:0]								h0000
h9C	LOSS	READDEV	FULL	EMPTY	BUSERROR	FIRSTB	SLAVE	MASTER	
h9D	DEVID[6:0]							SDA	h0000
h9E			DIS_FILTER	SDA_WEN	SDA_PIN	SCL_WEN	SCL_PIN	SOFTMODE	h0000
hA0	P3[7:0]								h00FF
hA1	PATAL[7:0]								h0000
hA2	PATAH[7:0]								h0000
hA3					PATAB[3:0]				h0000
hA4	PATD[7:0]								h0000
hA5	PATEN				PATSUB[3:0]				h0000
hA8	EAL		EAD	EU	ET1	EX1	ET0	EX0	h0000
hA9			EDV	EAV	EXX1	EWT	EXX0	EMSP	h0000
hAA			EDH	EAH	ECC	EPW		ERTC	h0000
hAB			EADW	E24	ESS	EI2C			h0000
hAC			G5P1	G4P1	G3P1	G2P1	G1P1	G0P1	h0000
hAD	EXX1R	EXX1F	EXX0R	EXX0F	EX1R	EX1F	EX0R	EX0F	h0005
hAE	PROGSTAT	XROM-QLEVEL			PUPDAC	PUPIO	PUPDIG	NMIEN	h0000
hB0	P4[7:0]								h00FF
hB1	WDT_REL[7:0]								h0000
hB2	WDT_IN	WDT_START	WDT_NARST	WDT_RST					
hB3	WDT_REF	WDT_TMR	WDT_TMR_STRT	WDT_TMR_OV					h0000

Table 3–1: SFR Subaddress Index, continued

Sub	Data Bits								Reset
	7	6	5	4	3	2	1	0	
hB4	WDT_LOW[7:0]								
hB5	WDT_HIGH[7:0]								
hB7	RELL[7:0]								h0000
hB8			G5P0	G4P0	G3P0	G2P0	G1P0	G0P0	h0000
hB9	RELH[7:0]								h0000
hBA	CAPL[7:0]								
hBB	CAPH[7:0]								
hBC	MINL[7:0]								h0000
hBD	MINH[7:0]								h0000
hBE	OVFLOW	PR	PLG	REL	RUN	RISE	FALL	SEL	h0000
hBF						PR1	FIRST	START	h0000
hC0	L24	ADC	WDT	AVS	DVS	PWM	AHS	DHS	h0000
hC1	PC80[7:0]								h0000
hC2	PC81[7:0]								h0000
hC3	PC82[7:0]								h0000
hC4	PC83[7:0]								h0000
hC5	PC84[7:0]								h0000
hC6	PC85[7:0]								h0000
hC7	PC140[7:0]								h0000
hC8	CC	ADW	SS	I2C	MSP	RTC	IEX1	IEX0	h0000
hC9	PC141[7:0]								h0000
hCA	PCX140[7:2]						PWM_PRE[1:0]		h0000
hCB	PCX141[7:2]								h0000
hCC	PWM_CL[7:0]								
hCD	PWM_TMR	PWM_TMR_OV	PWM_CH[5:0]						
hCE	PWM_EN[7:0]								h0000
hD0	CY	AC	F0	RS[1:0]		OV	F1	P	h0000
hD1	CADC0[7:0]								h0000
hD2	CADC1[7:0]								h0000
hD3	CADC2[7:0]								h0000
hD4	CADC3[7:0]								h0000
hD5			PS_ACK	ADWULE					h0000
hD8	SLI_ACQ	DISP	CADC	WAKUP	CLK_SRC	RST_XDFP	RST_CHIP	RST_EN	h00F4
hD9	ACQON		ACQ_STA	VBIADR[4:0]					h0000
hDA					PCLK1[3:0]				h0001
hDB	PCLK0[7:0]								h0048
hE0	A[7:0]								h0000
hE1					VSU[3:0]				h0000
hE2	RGB_D[1:0]		HP	VP	INT			MAST	h0000
hE3							SDV1[1:0]		h0000
hE4	SDV0[7:0]								h0020
hE5					SDH1[3:0]				h0000
hE6	SDH0[7:0]								h0048
hE7	EHCR[7:0]								h000A
hE8	ISP	XROM	INTSRC1	INTSRC0	PATCH	BOTTOM	NOMAP	TWENTY	h0000
hE9	BHCR[7:0]								h0000
hEA							BVCR1[1:0]		h0000
hEB	BVCR0[7:0]								h0000
hEC							EVCR1[1:0]		h0000

Table 3–1: SFR Subaddress Index, continued

Sub	Data Bits								Reset
	7	6	5	4	3	2	1	0	
hED	EVCR0[7:0]								h0004
hEE		ODD_EVEN	VSU2[3:0]				VLR1[1:0]		h0002
hEF	VLR0[7:0]								h0071
hF0	B[7:0]								h0000
hF1					HPR1[3:0]				h000A
hF2	HPR0[7:0]								h0020
hF3	POINT1_1[7:0]								h0000
hF4	POINT1_0[7:0]								h0006
hF5	POINT0_1[7:0]								h0000
hF6	POINT0_0[7:0]								h0000
hF8	FIT_STVAL	EN_FIT	EN_IT	EN_SS	EN_LD_GDW	EN_DG_OUT	DIS_COR	DIS_BLANK	h0060
hFE							CAPTION_DIS	TEXT_DIS	
hFF	BIT[7:0]								h000F

3.4. SFR Register Description

Note: For compatibility reasons, every undefined bit in a writeable register should be set to '0'. Undefined bits in a readable register should be treated as "don't care"!

Table 3–2: SFR Register Description

Name	Sub	Dir	Reset	Range	Function
PORT					
P1	h80	RW	h00FF		
P1[7:0]	h80[7:0]	RW	255	0..255	**Port 1** Port 1 is an 8-bit multifunctional input/output port
P2	h90	RW	h00FF		
P2[7:0]	h90[7:0]	RW	255	0..255	**Port 2** Port 2 is an 8-bit multifunctional input/output port
PMUX1	h92	RW	h0000		
PMUX1[7:0]	h92[7:0]	RW	0	0..255	**Port Mux 1** Defines behaviour of port pins P10-P23, SCL and SDA
PMUX2	h93	RW	h0000		
PMUX2[7:0]	h93[7:0]	RW	0	0..255	**Port Mux 2** Defines behaviour of port pins P24-P37
P3	hA0	RW	h00FF		
P3[7:0]	hA0[7:0]	RW	255	0..255	**Port 3** Port 3 is an 8-bit multifunctional input/output port
P4	hB0	RW	h00FF		
P4[7:0]	hB0[7:0]	RW	255	0..255	**Port 4** Port 4 is an 8-bit multifunctional input/output port
MICRO					
SP	h81	RW	h0007		
SP[7:0]	h81[7:0]	RW	7	0..255	**Stack Pointer**
DPL	h82	RW	h0000		
DPL[7:0]	h82[7:0]	RW	0	0..255	**Data Pointer Low Byte**
DPH	h83	RW	h0000		
DPH[7:0]	h83[7:0]	RW	0	0..255	**Data Pointer High Byte**
DPSEL	h84	RW	h0000		
DPSEL[2:0]	h84[2:0]	RW	0	0..7	**Data Pointer Select** selects one of eight data pointer
PCON	h87	RW	h0000		
SMOD	h87[7]	RW	0	0,1	**UART Baud Rate** 0: Normal baud rate. 1: Double baud rate.
PDS	h87[6]	RW	0	0,1	**Power Down Start** 0: Power Down Mode not started. 1: Power Down Mode started. The instruction that sets this bit is the last instruction before entering power down mode. Additionally, this bit is protected by a delay cycle. Power down mode is entered, if and only if bit PDE was set by the previous instruction. Once set, this bit is cleared by hardware and always reads out a 0. DAC, PLL and Oscillator are switched off during Power Down. The CADC is completely switched off (no wake up possible).
IDLS	h87[5]	RW	0	0,1	**Idle Start** 0: Idle Mode not started. 1: Idle Mode started. The instruction that sets this bit is the last instruction before entering idle mode. Additionally, this bit is protected by a delay cycle. Idle mode is entered, if and only if bit IDLE was set by the previous instruction. Once set, this bit is cleared by hardware and always reads out a 0.

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
SD	h87[4]	RW	0	0,1	**Slow Down** 0: Slow down mode is disabled. 1: Slow down mode is enabled. This bit is set to indicate the external clock generating circuitry to slow down the frequency. This bit is not protected by a delay cycle.
GF1	h87[3]	RW	0	0,1	**General Purpose Flag 1**
GF0	h87[2]	RW	0	0,1	**General Purpose Flag 0**
PDE	h87[1]	RW	0	0,1	**Power Down Mode Enable** When set, a delay cycle is started. The following instruction can then set the device into power down mode. Once set, this bit is cleared by hardware and always reads out a 0.
IDLE	h87[0]	RW	0	0,1	**Idle Mode Enable** When set, a delay cycle is started. The following instruction can then set the device into idle mode. Once set, this bit is cleared by hardware and always reads out a 0.
TCON	h88	RW	h0000		
TF1	h88[7]	R		0,1	**Timer Overflow 1** Set by hardware on timer/counter overflow. Cleared by hardware when interrupt service routine is entered.
TR1	h88[6]	RW	0	0,1	**Timer Run 1** 0: stop timer 1: run timer
TF0	h88[5]	R		0,1	**Timer Overflow 0** Set by hardware on timer/counter overflow. Cleared by hardware when interrupt service routine is entered.
TR0	h88[4]	RW	0	0,1	**Timer Run 0** 0: stop timer 1: run timer
IE1	h88[3]	R		0,1	**Interrupt Edge 1** Set by hardware when external interrupt edge detected. Cleared by hardware when interrupt service routine is entered.
IT1	h88[2]	RW	0	0,1	**Interrupt Trigger 1** 0: low level triggered external interrupt 1: falling edge triggered external interrupt
IE0	h88[1]	R		0,1	**Interrupt Edge 0** Set by hardware when external interrupt edge detected. Cleared by hardware when interrupt service routine is entered.
IT0	h88[0]	RW	0	0,1	**Interrupt Trigger 0** 0: low level triggered external interrupt 1: falling edge triggered external interrupt
TMOD	h89	RW	h0000		
GATE1	h89[7]	RW	0	0,1	**Timer 1 Gating** 0: timer 1 is enabled whenever TR1 control bit is set. 1: timer 1 is enabled only while INT1 pin is high and TR1 control pin is set.
CNT1	h89[6]	RW	0	0,1	**Timer/Counter 1 Selector** 0: timer operation (input from internal system clock) 1: counter operation (input from T1 pin)
M1[1:0]	h89[5:4]	RW	0	0..3	**Timer 1 Operating Mode** 00: 13-bit timer/counter (8048 compatible mode: TL1 serves as five-bit prescaler) 01: 16-bit timer/counter (TH1 and TL1 are cascaded, there is no prescaler) 10: 8-bit auto-reload timer/counter (TH1 holds a value which is to be reloaded into TL1 each time it overflows) 11: TL0 is an 8-bit timer/counter controlled by the standard timer 0 control bits. TH0 is an 8-bit timer/counter controlled by standard timer 1 control bits. TH1 and TL1 are held (Timer 1 is stopped).
GATE0	h89[3]	RW	0	0,1	**Timer 0 Gating** 0: timer 0 is enabled whenever TR0 control bit is set. 1: timer 0 is enabled only while INT0 pin is high and TR0 control pin is set.
CNT0	h89[2]	RW	0	0,1	**Timer/Counter 0 Selector** 0: timer operation (input from internal system clock) 1: counter operation (input from T0 pin)

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
M0[1:0]	h89[1:0]	RW	0	0..3	**Timer 0 Operating Mode** 00: 13-bit timer/counter (8048 compatible mode: TL0 serves as five-bit prescaler) 01: 16-bit timer/counter (TH0 and TL0 are cascaded, there is no prescaler) 10: 8-bit auto-reload timer/counter (TH0 holds a value which is to be reloaded into TL0 each time it overflows) 11: TL0 is an 8-bit timer/counter controlled by the standard timer 0 control bits. TH0 is an 8-bit timer/counter controlled by standard timer 1 control bits. TH1 and TL1 are held (Timer 1 is stopped).
TL0	h8A	RW	h0000		
TL0[7:0]	h8A[7:0]	RW	0	0..255	**Timer/Counter 0 Low Byte**
TL1	h8B	RW	h0000		
TL1[7:0]	h8B[7:0]	RW	0	0..255	**Timer/Counter 1 Low Byte**
TH0	h8C	RW	h0000		
TH0[7:0]	h8C[7:0]	RW	0	0..255	**Timer/Counter 0 High Byte**
TH1	h8D	RW	h0000		
TH1[7:0]	h8D[7:0]	RW	0	0..255	**Timer/Counter 1 High Byte**
MEX1	h94	RW	h0000		
CB[19:16]	h94[7:4]	R		0..15	**Current Bank** these bits are mapped to address lines A[19:16]
NB[19:16]	h94[3:0]	RW	0	0..15	**Next Bank** defines bank number for following LJMP and CALL instructions
MEX2	h95	RW	h0000		
MM	h95[7]	RW	0	0,1	**MOVC Bank Mode** 0: CB[19:16] are mapped to address lines A[19:16] 1: MB[19:16] are mapped to address lines A[19:16]
MB[18:16]	h95[6:4]	RW	0	0..7	**MOVC Bank** defines bank number for following MOVC instructions
IB[19:16]	h95[3:0]	RW	0	0..15	**Interrupt Bank** defines bank number for interrupt vectors
MEX3	h96	RW	h0000		
MB[19]	h96[7]	RW	0	0,1	**MOVC Bank 19** defines bank number for following MOVC instructions
UB3	h96[6]	RW	0	0,1	**User Bit 3** general purpose user bits
UB4	h96[5]	RW	0	0,1	**User Bit 4** general purpose user bits
MX[19]	h96[4]	RW	0	0,1	**MOVX Bank 19** defines bank number of data memory addressed by following MOVX instructions (only if MXM is set)
MXM	h96[3]	RW	0	0,1	**MOVX Bank Mode** 0: CB[19:16] are mapped to address lines A[19:16] 1: MX[19:16] are mapped to address lines A[19:16]
MX[18:16]	h96[2:0]	RW	0	0..7	**MOVX Bank** defines bank number of data memory addressed by following MOVX instructions (only if MXM is set)
MEXSP	h97	RW	h0000		
MXSP[7:0]	h97[7:0]	RW	0	0..255	**Memory Extension Stack Pointer** addresses 128byte on-chip stack memory
PSW	hD0	RW	h0000		
CY	hD0[7]	RW	0	0,1	**ALU Carry Flag**
AC	hD0[6]	RW	0	0,1	**ALU Auxiliary Carry Flag**
F0	hD0[5]	RW	0	0,1	**User Definable Flag 0**
RS[1:0]	hD0[4:3]	RW	0	0..3	**Register Bank Select** 00: RB0 (registers from 00h - 07h 01: RB1 (registers from 08h - 0Fh 10: RB2 (registers from 10h - 17h 11: RB3 (registers from 18h - 1Fh
OV	hD0[2]	RW	0	0,1	**ALU Overflow Flag**

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
F1	hD0[1]	RW	0	0,1	**User Definable Flag 1**
P	hD0[0]	RW	0	0,1	**Parity Flag** Set each instruction cycle to indicate odd/even parity in the accumulator
ACC	hE0	RW	h0000		
A[7:0]	hE0[7:0]	RW	0	0..255	**Accumulator**
B	hF0	RW	h0000		
B[7:0]	hF0[7:0]	RW	0	0..255	**B Register**
BONDOPTION	hFE	R			
CAPTION_DIS	hFE[1]	R		0,1	**Closed Caption Disable** 0: Closed Caption reception allowed 1: Closed Caption reception not allowed
TEXT_DIS	hFE[0]	R		0,1	**Teletext Disable** 0: teletext reception allowed 1: teletext reception not allowed
MSIZ	hFF	RW	h000F		
BIT[7:0]	hFF[7:0]	RW	15	0..255	**Scratch Pad Register**
RTC					
RTCDATA	h8E	RW	h0000		
RTCDATA[7:0]	h8E[7:0]	RW	0	0..255	**RTC Data**
RTCSUB	h8F	RW	h0000		
RTCSUB[3:0]	h8F[7:4]	RW	0	0..15	**RTC Subaddress**
RTCRW	h8F[3]	RW	0	0,1	**RTC Read/Write**
UART					
SCON	h98	RW	h0000		
SM[1:0]	h98[7:6]	RW	0	0..3	**Serial Mode** 00: 8-bit shift register, baud rate = Fosc / 12 01: 8-bit UART, baud rate = (SMOD + 1) * Fosc / (32 * 12 * (256 - TH1)) 10: 9-bit UART, baud rate = (SMOD + 1) * Fosc / 64 11: 9-bit UART, baud rate = (SMOD + 1) * Fosc / (32 * 12 * (256 - TH1))
SM2	h98[5]	RW	0	0,1	**Serial Mode 2** Enables the multiprocessor communication feature in modes 2 and 3. In mode 2 or 3, if SM2 is set then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 is set then RI will not be activated unless a valid stop bit is received. In mode 0, SM2 should be 0.
REN	h98[4]	RW	0	0,1	**Reception Enable** 0: disable 1: enable
TB8	h98[3]	RW	0	0,1	**Transmit Bit8** This is the 9th data bit that will be transmitted in modes 2 and 3. Set or cleared by software as desired.
RB8	h98[2]	RW	0	0,1	**Receive Bit8** In modes 2 and 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	h98[1]	RW	0	0,1	**Transmit Interrupt** Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	h98[0]	RW	0	0,1	**Receive Interrupt** Set by hardware at the end of the 8th bit time in mode 0, or halfway through stop bit time in the other modes, in any serial reception. Must be cleared by software.
SBUF	h99	RW	h0000		
SBUF[7:0]	h99[7:0]	RW	0	0..255	**Serial Data Buffer**
I2C					
I2CCON	h9A	RW	h0000		
LASTB	h9A[7]	RW	0	0,1	**Last Byte** 0: normal byte transmission 1: last byte transmission (generate stop condition)

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
SCL	h9A[6]	RW	0	0,1	**SCL Level** 0: SCL level low 1: SCL level high
REPEAT	h9A[5]	RW	0	0,1	**Repeat Start Condition** 1: generate a repeated start condition
IGNACK	h9A[4]	RW	0	0,1	**Ignore Acknowledge** 1: never check acknowledge, just report bus_error when no ack seen
INTEN	h9A[3]	RW	0	0,1	**Interrupt Enable** 0: no interrupt generation 1: enable interrupt generation
MASTEN	h9A[2]	RW	0	0,1	**Master Enable** 0: Slave Mode 1: Master Mode (set before starting a telegram, can be released after writing I2C address)
FAST	h9A[1]	RW	0	0,1	**Fast Mode Enable** 0: 100kHz 1: 400kHz
PDOWN	h9A[0]	RW	0	0,1	**Power Down Enable** 0: normal operation 1: power down mode
I2CDATA	h9B	RW	h0000		
I2CDATA[7:0]	h9B[7:0]	RW	0	0..255	**I2C Data** Writing a byte to the data register turns the I2C interface into master mode and issues a bus_request if the bus is currently free.
I2CSTAT	h9C	R			
LOSS	h9C[7]	RW	0	0,1	**Loss Of Arbitration** read 1: loss of arbitration or no response from any device write 1: reset interrupt
READDEV	h9C[6]	RW	0	0,1	**Read Device ID** read 1: read device ID was transmitted write 1: reset interrupt
FULL	h9C[5]	RW	0	0,1	**Buffer Full** read 1: buffer full (has received a new data byte) write 1: reset interrupt
EMPTY	h9C[4]	RW	0	0,1	**Buffer Empty** read 1: buffer empty (needs a new data byte to be sent) write 1: reset interrupt
BUSERROR	h9C[3]	RW	0	0,1	**Bus Error** read 1: bus error write 1: reset interrupt
FIRSTB	h9C[2]	R		0,1	**First Byte** 0: no byte received or transmitted 1: first byte received or transmitted
SLAVE	h9C[1]	R		0,1	**Slave Active** 0: slave interface not active 1: slave interface active
MASTER	h9C[0]	R		0,1	**Master Active** 0: master interface not active 1: master interface active
I2CDEVID	h9D	RW	h0000		
DEVID[6:0]	h9D[7:1]	RW	0	0..127	**I2C Device ID** Device ID of interface in slave mode
SDA	h9D[0]	RW	0	0,1	**SDA Level** 0: SDA level low 1: SDA level high
I2CSOFT	h9E	RW	h0000		
DIS_FILTER	h9E[5]	RW	0	0,1	**Disable Input Filter**
SDA_WEN	h9E[4]	RW	0	0,1	**SDA Write Enable**
SDA_PIN	h9E[3]	RW	0	0,1	**SDA Pin** 0: SDA pin low 1: SDA pin high
SCL_WEN	h9E[2]	RW	0	0,1	**SCL Write Enable**

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
SCL_PIN	h9E[1]	RW	0	0,1	**SCL Pin** 0: SCL pin low 1: SCL pin high
SOFTMODE	h9E[0]	RW	0	0,1	**Software Mode** 0: normal hardware operation 1: enable software mode and keep hardware in reset
PATCH					
PATAL	hA1	RW	h0000		
PATAL[7:0]	hA1[7:0]	RW	0	0..255	**Patch Address Low** Defines the low address byte of a ROM location which will be corrected.
PATAH	hA2	RW	h0000		
PATAH[7:0]	hA2[7:0]	RW	0	0..255	**Patch Address High** Defines the high address byte of a ROM location which will be corrected.
PATAB	hA3	RW	h0000		
PATAB[3:0]	hA3[3:0]	RW	0	0..15	**Patch Address Bank** Defines the bank address of a ROM location which will be corrected.
PATDATA	hA4	RW	h0000		
PATD[7:0]	hA4[7:0]	RW	0	0..255	**Patch Data** Defines the value to which the addressed ROM location will be corrected.
PATSUB	hA5	RW	h0000		
PATEN	hA5[7]	RW	0	0,1	**Patch Enable** Only enabled patch registers can correct ROM locations. 0: ignore patch data 1: enable patch data
PATSUB[3:0]	hA5[3:0]	RW	0	0..15	**Patch Subaddr** Selects 1 out of 16 patch registers, where address, data and enable are stored. PATA and PATD have to be written first.
INTERRUPT					
IEN0	hA8	RW	h0000		
EAL	hA8[7]	RW	0	0,1	**Enable All Interrupts** 0: all interrupts are disabled 1: interrupts are individually enabled/disabled according to their respective bit selection.
EAD	hA8[5]	RW	0	0,1	**Enable CADC Interrupt**
EU	hA8[4]	RW	0	0,1	**Enable UART Interrupt**
ET1	hA8[3]	RW	0	0,1	**Enable Timer 1 Overflow Interrupt**
EX1	hA8[2]	RW	0	0,1	**Enable External Interrupt 1**
ET0	hA8[1]	RW	0	0,1	**Enable Timer 0 Overflow Interrupt**
EX0	hA8[0]	RW	0	0,1	**Enable External Interrupt 0**
IEN1	hA9	RW	h0000		
EDV	hA9[5]	RW	0	0,1	**Enable Display V-Sync Interrupt**
EAV	hA9[4]	RW	0	0,1	**Enable Acquisition V-Sync Interrupt**
EXX1	hA9[3]	RW	0	0,1	**Enable External Extra Interrupt 1**
EWT	hA9[2]	RW	0	0,1	**Enable Watchdog Timer Interrupt**
EXX0	hA9[1]	RW	0	0,1	**Enable External Extra Interrupt 0**
EMSP	hA9[0]	RW	0	0,1	**Enable MSP Interrupt**
IEN2	hAA	RW	h0000		
EDH	hAA[5]	RW	0	0,1	**Enable Display H-Sync Interrupt**
EAH	hAA[4]	RW	0	0,1	**Enable Acquisition H-Sync Interrupt**
ECC	hAA[3]	RW	0	0,1	**Enable Channel Change Interrupt**
EPW	hAA[2]	RW	0	0,1	**Enable PWM Timer Interrupt**
ERTC	hAA[0]	RW	0	0,1	**Enable RTC Interrupt**
IEN3	hAB	RW	h0000		
EADW	hAB[5]	RW	0	0,1	**Enable CADC Wake-up interrupt**

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
E24	hAB[4]	RW	0	0,1	**Enable Line 24 Interrupt**
ESS	hAB[3]	RW	0	0,1	**Enable Softscroll Interrupt**
EI2C	hAB[2]	RW	0	0,1	**Enable I2C Interrupt**
IP1	hAC	RW	h0000		
G5P1	hAC[5]	RW	0	0,1	**Interrupt Group 5 Priority 1** Together with G5P0 a 4 level priority is defined: 00: Interrupt Group 5 is set to priority level 0 (lowest). 01: Interrupt Group 5 is set to priority level 1. 10: Interrupt Group 5 is set to priority level 2. 11: Interrupt Group 5 is set to priority level 3 (highest).
G4P1	hAC[4]	RW	0	0,1	**Interrupt Group 4 Priority 1** Together with G4P0 a 4 level priority is defined: 00: Interrupt Group 4 is set to priority level 0 (lowest). 01: Interrupt Group 4 is set to priority level 1. 10: Interrupt Group 4 is set to priority level 2. 11: Interrupt Group 4 is set to priority level 3 (highest).
G3P1	hAC[3]	RW	0	0,1	**Interrupt Group 3 Priority 1** Together with G3P0 a 4 level priority is defined: 00: Interrupt Group 3 is set to priority level 0 (lowest). 01: Interrupt Group 3 is set to priority level 1. 10: Interrupt Group 3 is set to priority level 2. 11: Interrupt Group 3 is set to priority level 3 (highest).
G2P1	hAC[2]	RW	0	0,1	**Interrupt Group 2 Priority 1** Together with G2P0 a 4 level priority is defined: 00: Interrupt Group 2 is set to priority level 0 (lowest). 01: Interrupt Group 2 is set to priority level 1. 10: Interrupt Group 2 is set to priority level 2. 11: Interrupt Group 2 is set to priority level 3 (highest).
G1P1	hAC[1]	RW	0	0,1	**Interrupt Group 1 Priority 1** Together with G1P0 a 4 level priority is defined: 00: Interrupt Group 1 is set to priority level 0 (lowest). 01: Interrupt Group 1 is set to priority level 1. 10: Interrupt Group 1 is set to priority level 2. 11: Interrupt Group 1 is set to priority level 3 (highest).
G0P1	hAC[0]	RW	0	0,1	**Interrupt Group 0 Priority 1** Together with G0P0 a 4 level priority is defined: 00: Interrupt Group 0 is set to priority level 0 (lowest). 01: Interrupt Group 0 is set to priority level 1. 10: Interrupt Group 0 is set to priority level 2. 11: Interrupt Group 0 is set to priority level 3 (highest).
IRCON	hAD	RW	h0005		
EXX1R	hAD[7]	RW	0	0,1	**EXX1 Rising Edge Interrupt** 0: EXX1 interrupt on low level at input pin 1: EXX1 interrupt on rising edge at input pin
EXX1F	hAD[6]	RW	0	0,1	**EXX1 Falling Edge Interrupt** 0: EXX1 interrupt on low level at input pin 1: EXX1 interrupt on falling edge at input pin
EXX0R	hAD[5]	RW	0	0,1	**EXX0 Rising Edge Interrupt** 0: EXX0 interrupt on low level at input pin 1: EXX0 interrupt on rising edge at input pin
EXX0F	hAD[4]	RW	0	0,1	**EXX0 Falling Edge Interrupt** 0: EXX0 interrupt on low level at input pin 1: EXX0 interrupt on falling edge at input pin
EX1R	hAD[3]	RW	0	0,1	**EX1 Rising Edge Interrupt** 0: EX1 interrupt on low level at input pin 1: EX1 interrupt on rising edge at input pin
EX1F	hAD[2]	RW	1	0,1	**EX1 Falling Edge Interrupt** 0: EX1 interrupt on low level at input pin 1: EX1 interrupt on falling edge at input pin
EX0R	hAD[1]	RW	0	0,1	**EX0 Rising Edge Interrupt** 0: EX0 interrupt on low level at input pin 1: EX0 interrupt on rising edge at input pin
EX0F	hAD[0]	RW	1	0,1	**EX0 Falling Edge Interrupt** 0: EX0 interrupt on low level at input pin 1: EX0 interrupt on falling edge at input pin

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
NMI	hAE	RW	h0000		
PROGSTAT	hAE[7]	R		0,1	**Program Status** 0: internal 1: external
XROMQLEVEL	hAE[6]	R		0,1	**XROMQ Pin Level**
PUPDAC	hAE[3]	RW	0	0,1	**Voltage Supervision VSUP3.3DAC** 0: supply voltage above threshold 1: supply voltage below threshold
PUPIO	hAE[2]	RW	0	0,1	**Voltage Supervision VSUP3.3IO** 0: supply voltage above threshold 1: supply voltage below threshold
PUPDIG	hAE[1]	RW	0	0,1	**Voltage Supervision VSUP1.8DIG** 0: supply voltage above threshold 1: supply voltage below threshold
NMIEN	hAE[0]	RW	0	0,1	**Enable NMI** 0: NMI disabled 1: NMI enabled
IP0	hB8	RW	h0000		
G5P0	hB8[5]	RW	0	0,1	**Interrupt Group 5 Priority 0** Together with G5P1 a 4 level priority is defined: 00: Interrupt Group 5 is set to priority level 0 (lowest). 01: Interrupt Group 5 is set to priority level 1. 10: Interrupt Group 5 is set to priority level 2. 11: Interrupt Group 5 is set to priority level 3 (highest).
G4P0	hB8[4]	RW	0	0,1	**Interrupt Group 4 Priority 0** Together with G4P1 a 4 level priority is defined: 00: Interrupt Group 4 is set to priority level 0 (lowest). 01: Interrupt Group 4 is set to priority level 1. 10: Interrupt Group 4 is set to priority level 2. 11: Interrupt Group 4 is set to priority level 3 (highest).
G3P0	hB8[3]	RW	0	0,1	**Interrupt Group 3 Priority 0** Together with G3P1 a 4 level priority is defined: 00: Interrupt Group 3 is set to priority level 0 (lowest). 01: Interrupt Group 3 is set to priority level 1. 10: Interrupt Group 3 is set to priority level 2. 11: Interrupt Group 3 is set to priority level 3 (highest).
G2P0	hB8[2]	RW	0	0,1	**Interrupt Group 2 Priority 0** Together with G2P1 a 4 level priority is defined: 00: Interrupt Group 2 is set to priority level 0 (lowest). 01: Interrupt Group 2 is set to priority level 1. 10: Interrupt Group 2 is set to priority level 2. 11: Interrupt Group 2 is set to priority level 3 (highest).
G1P0	hB8[1]	RW	0	0,1	**Interrupt Group 1 Priority 0** Together with G1P1 a 4 level priority is defined: 00: Interrupt Group 1 is set to priority level 0 (lowest). 01: Interrupt Group 1 is set to priority level 1. 10: Interrupt Group 1 is set to priority level 2. 11: Interrupt Group 1 is set to priority level 3 (highest).
G0P0	hB8[0]	RW	0	0,1	**Interrupt Group 0 Priority 0** Together with G0P1 a 4 level priority is defined: 00: Interrupt Group 0 is set to priority level 0 (lowest). 01: Interrupt Group 0 is set to priority level 1. 10: Interrupt Group 0 is set to priority level 2. 11: Interrupt Group 0 is set to priority level 3 (highest).
CISR0	hC0	RW	h0000		
L24	hC0[7]	RW	0	0,1	**Line24 Interrupt** Set by hardware, must be cleared by software.
ADC	hC0[6]	RW	0	0,1	**ADC Interrupt** Set by hardware, must be cleared by software.
WDT	hC0[5]	RW	0	0,1	**Watchdog Timer Interrupt** Set by hardware, must be cleared by software. On reset this bit is initialized to 0, however if timer mode is selected and timer is running, every over flow of timer will set this bit. Therefore software must clear this bit before enabling the corresponding interrupt.
AVS	hC0[4]	RW	0	0,1	**Acquisition Vsync Interrupt** Set by hardware, must be cleared by software.

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
DVS	hC0[3]	RW	0	0,1	**Display Vsync Interrupt** Set by hardware, must be cleared by software.
PWM	hC0[2]	RW	0	0,1	**PWM Timer Interrupt** Set by hardware, must be cleared by software. On reset this bit is initialized to 0, however if timer mode is selected and timer is running, every over flow of timer will set this bit. Therefore software must clear this bit before enabling the corresponding interrupt.
AHS	hC0[1]	RW	0	0,1	**Acquisition Hsync Interrupt** Set by hardware, must be cleared by software.
DHS	hC0[0]	RW	0	0,1	**Display Hsync Interrupt** Set by hardware, must be cleared by software.
CISR1	hC8	RW	h0000		
CC	hC8[7]	RW	0	0,1	**Channel Change Interrupt** Set by hardware, must be cleared by software.
ADW	hC8[6]	RW	0	0,1	**ADC Wakeup Interrupt** Set by hardware, must be cleared by software.
SS	hC8[5]	RW	0	0,1	**Softscroll Interrupt** Set by hardware, must be cleared by software.
I2C	hC8[4]	RW	0	0,1	**I2C Interrupt** Set by hardware, must be cleared by software.
MSP	hC8[3]	RW	0	0,1	**MSP Interrupt** Set by hardware, must be cleared by software.
RTC	hC8[2]	RW	0	0,1	**RTC Interrupt** Set by hardware, must be cleared by software.
IEX1	hC8[1]	RW	0	0,1	**External Extra Interrupt 1** Set by hardware, must be cleared by software. Port P3.7 must be in input mode to use this interrupt.
IEX0	hC8[0]	RW	0	0,1	**External Extra Interrupt 0** Set by hardware, must be cleared by software. Port P3.1 must be in input mode to use this interrupt.
WATCHDOG					
WDT_REL	hB1	RW	h0000		
WDT_REL[7:0]	hB1[7:0]	RW	0	0..255	**Watchdog Reload Value** This value is loaded in the upper 8 bit of the watchdog counter at WDT_START and WDT_REL and also at timer start.
WDT_CTRL	hB2	R			
WDT_IN	hB2[7]	RW	0	0,1	**Watchdog Prescaler** The prescaler divides the system clock clk40.5 and effects both watchdog and timer mode. Changes are synchronized to refresh, start and reset. 0: clk40.5 divided by 24 1: clk40.5 divided by 1536
WDT_START	hB2[6]	RW	0	0,1	**Watchdog Start** Watchdog can only be started when not in timer mode. It cannot be stopped by software, it can only be disabled by power-on reset. WDT_START also refreshes the watchdog when set immediately after WDT_REF. 0: watchdog is not started 1: watchdog started
WDT_NARST	hB2[5]	RW	0	0,1	**Watchdog Not All Reset** 0: WDT_REL, WDT_IN, WDT_LOW and WDT_HIGH are reset by watchdog 1: WDT_REL, WDT_IN, WDT_LOW and WDT_HIGH are not reset by watchdog
WDT_RST	hB2[4]	R		0,1	**Watchdog Reset** 0: no watchdog reset 1: watchdog triggered reset
WDT_REFRESH	hB3	RW	h0000		
WDT_REF	hB3[7]	RW	0	0,1	**Watchdog Refresh** Watchdog refresh is accomplished by setting WDT_REF, immediately followed by setting WDT_START. WDT_REF is cleared by hardware after 3 machine cycles.

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
WDT_TMR	hB3[6]	RW	0	0,1	**Watchdog Timer Mode** This bit cannot be set when watchdog has been started. This bit cannot be cleared when watchdog timer is running. 0: watchdog mode 1: timer mode
WDT_TMR_STRT	hB3[5]	RW	0	0,1	**Watchdog Timer Start** This bit can only be set when watchdog is in timer mode. When watchdog timer is started, it loads the preload value from WDT_REL, clears WDT_TMR_OV and starts counting up. 0: stop running watchdog timer (WDT_TMR_OV is not affected) 1: start watchdog timer
WDT_TMR_OV	hB3[4]	RW	0	0,1	**Watchdog Timer Overflow**
WDT_LOW	hB4	R			
WDT_LOW[7:0]	hB4[7:0]	R		0..255	**Watchdog Timer Low Byte**
WDT_HIGH	hB5	R			
WDT_HIGH[7:0]	hB5[7:0]	R		0..255	**Watchdog Timer High Byte**
CRT					
CRT_RELL	hB7	RW	h0000		
RELL[7:0]	hB7[7:0]	RW	0	0..255	**CRT Reload Low Byte**
CRT_RELH	hB9	RW	h0000		
RELH[7:0]	hB9[7:0]	RW	0	0..255	**CRT Reload High Byte**
CRT_CAPL	hBA	R			
CAPL[7:0]	hBA[7:0]	R		0..255	**CRT Capture Low Byte**
CRT_CAPH	hBB	R			
CAPH[7:0]	hBB[7:0]	R		0..255	**CRT Capture High Byte**
CRT_MINCAPL	hBC	RW	h0000		
MINL[7:0]	hBC[7:0]	RW	0	0..255	**CRT Minimum Capture Low Byte**
CRT_MINCAPH	hBD	RW	h0000		
MINH[7:0]	hBD[7:0]	RW	0	0..255	**CRT Minimum Capture High Byte**
CRT_CON0	hBE	RW	h0000		
OVFLOW	hBE[7]	RW	0	0,1	**Overflow** Will be set by hardware, if counter overflow has occurred; must be cleared by software.
PR	hBE[6]	RW	0	0,1	**Prescaler** 0: 2-bit prescaler 1: 3-bit prescaler
PLG	hBE[5]	RW	0	0,1	**Polling Mode** 1: Timer polling mode is selected, capture function is automatically disabled, reading capture registers will show current timer value.
REL	hBE[4]	RW	0	0,1	**Reload CRT** 1: counter will be reloaded simultaneously with capture event.
RUN	hBE[3]	RW	0	0,1	**Run CRT** 0: stop CRT 1: run CRT
RISE	hBE[2]	RW	0	0,1	**Rising Edge** Capture (and reload if REL = 1) on rising edge.
FALL	hBE[1]	RW	0	0,1	**Falling Edge** Capture (and reload if REL = 1) on falling edge.
SEL	hBE[0]	RW	0	0,1	**Capture Input Select** If set, P3.3 is selected for capture input, otherwise P3.2.
CRT_CON1	hBF	RW	h0000		
PR1	hBF[2]	RW	0	0,1	**Prescaler 1** 0: no additional prescaler 1: additional 3-bit prescaler
FIRST	hBF[1]	R		0,1	**First Capture Event** 0: not first capture event 1: first capture event

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
START	hBF[0]	RW	0	0,1	**Start** 0: no SSU mode 1: enter the SSU mode and wait for new telegram. When an event occurs the First bit will be set. Upon next event, hardware resets the First bit and CRT interrupt is generated based on MIN_CAP register.
PWM					
PWM_COMP8_0	hC1	RW	h0000		
PC80[7:0]	hC1[7:0]	RW	0	0..255	**PWM 8bit Value Channel 0** Defines output value of 8bit PWM channel 0. The register can be altered anytime, the change take effect when the current PWM cycle is finished (6-bit overflow of counter)
PWM_COMP8_1	hC2	RW	h0000		
PC81[7:0]	hC2[7:0]	RW	0	0..255	**PWM 8bit Value Channel 1** Defines output value of 8bit PWM channel 1. The register can be altered anytime, the change take effect when the current PWM cycle is finished (6-bit overflow of counter)
PWM_COMP8_2	hC3	RW	h0000		
PC82[7:0]	hC3[7:0]	RW	0	0..255	**PWM 8bit Value Channel 2** Defines output value of 8bit PWM channel 2. The register can be altered anytime, the change take effect when the current PWM cycle is finished (6-bit overflow of counter)
PWM_COMP8_3	hC4	RW	h0000		
PC83[7:0]	hC4[7:0]	RW	0	0..255	**PWM 8bit Value Channel 3** Defines output value of 8bit PWM channel 3. The register can be altered anytime, the change take effect when the current PWM cycle is finished (6-bit overflow of counter)
PWM_COMP8_4	hC5	RW	h0000		
PC84[7:0]	hC5[7:0]	RW	0	0..255	**PWM 8bit Value Channel 4** Defines output value of 8bit PWM channel 4. The register can be altered anytime, the change take effect when the current PWM cycle is finished (6-bit overflow of counter)
PWM_COMP8_5	hC6	RW	h0000		
PC85[7:0]	hC6[7:0]	RW	0	0..255	**PWM 8bit Value Channel 5** Defines output value of 8bit PWM channel 5. The register can be altered anytime, the change take effect when the current PWM cycle is finished (6-bit overflow of counter)
PWM_COMP14_0	hC7	RW	h0000		
PC140[7:0]	hC7[7:0]	RW	0	0..255	**PWM 14bit High Value Channel 0** Defines the higher order 8bit output value of 14bit PWM channel 0. The register can be altered anytime, the change take effect when the current PWM cycle is finished (8-bit overflow of counter)
PWM_COMP14_1	hC9	RW	h0000		
PC141[7:0]	hC9[7:0]	RW	0	0..255	**PWM 14bit High Value Channel 1** Defines the higher order 8bit output value of 14bit PWM channel 1. The register can be altered anytime, the change take effect when the current PWM cycle is finished (8-bit overflow of counter)
PWM_COMPEXT14_0	hCA	RW	h0000		
PCX140[7:2]	hCA[7:2]	RW	0	0..63	**PWM 14bit Low Value Channel 0** Defines the lower order 6bit output value of 14bit PWM channel 0. The register can be altered anytime, the change take effect when the current PWM cycle is finished (8-bit overflow of counter)
PWM_PRE[1:0]	hCA[1:0]	RW	0	0,1,2,3	**PWM Prescaler** This register affects all PWM channels and the PWM timer. The register can be altered anytime, the change take effect when the current PWM cycle is finished (8-bit overflow of counter). 00: count rate = 20.25MHz 01: count rate = 10.125MHz 1x: count rate = 40.5MHz
PWM_COMPEXT14_1	hCB	RW	h0000		
PCX141[7:2]	hCB[7:2]	RW	0	0..63	**PWM 14bit Low Value Channel 1** Defines the lower order 6bit output value of 14bit PWM channel 1. The register can be altered anytime, the change take effect when the current PWM cycle is finished (8-bit overflow of counter)

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
PWM_CL	hCC	R			
PWM_CL[7:0]	hCC[7:0]	R		0..255	**PWM Counter Low Byte**
PWM_CH	hCD	R			
PWM_TMR	hCD[7]	RW	0	0,1	**PWM Timer Start** This bit cannot be set if one of the PWM channels is enabled (PWM_EN != 0). PWM_EN cannot be set if the PWM_TMR bit is set. 0: PWM timer stopped 1: PWM timer reset and start
PWM_TMR_OV	hCD[6]	RW	0	0,1	**PWM Timer Overflow**
PWM_CH[5:0]	hCD[5:0]	R		0..63	**PWM Counter High Byte**
PWM_EN	hCE	RW	h0000		
PWM_EN[7:0]	hCE[7:0]	RW	0	0..255	**PWM Channel Enable** Can only be written when PWM_TMR=0. PWM_EN[5:0] are channels with 8-bit resolution, while PWM_EN[7:6] are channels with 14-bit resolution. 0: disable 1: enable
CADC					
CADC0	hD1	RW	h0000		
CADC0[7:0]	hD1[7:0]	RW	0	0..255	**ADC Result Channel 0** After finishing the A to D conversion the processor is informed by means of an interrupt. The interrupt service routine can now take the conversion result of channel 0 from CADC0. The result will be available for about 46 ms after the interrupt.
CADC1	hD2	RW	h0000		
CADC1[7:0]	hD2[7:0]	RW	0	0..255	**ADC Result Channel 1** After finishing the A to D conversion the processor is informed by means of an interrupt. The interrupt service routine can now take the conversion result of channel 1 from CADC1. The result will be available for about 46 ms after the interrupt.
CADC2	hD3	RW	h0000		
CADC2[7:0]	hD3[7:0]	RW	0	0..255	**ADC Result Channel 2** After finishing the A to D conversion the processor is informed by means of an interrupt. The interrupt service routine can now take the conversion result of channel 2 from CADC2. The result will be available for about 46 ms after the interrupt.
CADC3	hD4	RW	h0000		
CADC3[7:0]	hD4[7:0]	RW	0	0..255	**ADC Result Channel 3** After finishing the A to D conversion the processor is informed by means of an interrupt. The interrupt service routine can now take the conversion result of channel 3 from CADC3. The result will be stable for about 46 ms after the interrupt.
CADC_CONF	hD5	RW	h0000		
PS_ACK	hD5[5]	R		0,1	**ADC Power Save Acknowledge** Must be 1 before entering power-down mode.
ADWULE	hD5[4]	RW	0	0,1	**ADC Wakeup Level** Defines threshold level for wake up. A special wake up unit has been included to allow a system wake up as soon as the analog input signal on pin P1.x drops below a predefined level. 0: Threshold level corresponds to fullscale - 4 LSB. This means that if the digital input value drops below 255 - 4 = 251 an interrupt will be triggered. In voltages that is 3.3 V - 0.052 V = 3.248 V. 1: threshold level corresponds to fullscale - 16 LSB. This means that if the digital input value drops below 255 - 16 = 239 an interrupt will be triggered. In voltages that is 3.3 V - 0.206 V = 3.094 V.
RESET					
PSAVE	hD8	RW	h00F4		
SLI_ACQ	hD8[7]	RW	1	0,1	**Power Save Slicer and Acquisition** 0: no power save 1: slicer, sync unit and acquisition are disabled. All the pending bus requests are masked off.

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
DISP	hD8[6]	RW	1	0,1	**Power Save Display Generator** 0: no power save 1: display generator, pixel clock unit and display sync unit are disabled. All pending bus request are masked off. The OSD-DAC is also switched off and it outputs the values defined for DAC off.
CADC	hD8[5]	RW	1	0,1	**Power Save CADC** 0: no power save 1: CADC is disabled but the CADC-Wake-Up-Unit is active
WAKUP	hD8[4]	RW	1	0,1	**Power Save CADC-Wake-Up-Unit** 0: no power save 1: CADC-Wake-Up-Unit is disabled (only useful in saving power when CADC bit is also set)
CLK_SRC	hD8[3]	RW	0	0,1	**Clock Source** 0: system clock (40.5 MHz) is derived from 648 MHz clock PLL 1: system clock (5.125 MHz) is derived from 20.25 MHz clock oscillator. 648MHz PLL is bypassed . In this mode slicer, acquisition, DAC and display generator are disabled.
RST_XDFP	hD8[2]	RW	1	0,1	**Reset XDFP** 0: release XDFP reset signal 1: no action
RST_CHIP	hD8[1]	RW	0	0,1	**Reset Chip** 0: release global reset signal (RESQ pin high) 1: set global reset signal (RESQ pin low)
RST_EN	hD8[0]	RW	0	0,1	**Reset Enable** This bit has to be set before setting RST_XDFP or RST_CHIP. It is automatically cleared after writing RST_XDFP or RST_CHIP. 0: no software reset possible 1: software reset possible
SLICER					
STRVBI	hD9	RW	h0000		
ACQON	hD9[7]	RW	0	0,1	**Enable Acquisition** 0: The ACQ interface does not access memory (immediately inactive). 1: The ACQ interface is active and writes data to memory (switching on is synchronous to VSync).
ACQ_STA	hD9[5]	RW	0	0,1	**Acquisition Start Detection** 0: No framing code after vertical sync has been detected. 1: Framing code after vertical sync has been detected. The bit is set by hardware and must be cleared by software.
VBIADR[4:0]	hD9[4:0]	RW	0	0..31	**VBI Buffer Address** Defines the 5 MSBs of the start address of the VBI buffer (the LSBs are fixed to 0x000). The VBI buffer location can be aligned to any 1 kByte memory segment.
DISPLAY					
PCLK1	hDA	RW	h0001		
PCLK1[3:0]	hDA[3:0]	RW	1	0..15	**Pixel Clock High** This register defines the relation between the output pixel frequency and the frequency of the crystal. The pixel frequency does not depend on the line frequency. It can be calculated by the following formula: Fpixel = PCLK * 324 MHz / 8192 The pixel frequency can be adjusted in steps of 39.6 kHz. After power-on this register is set to 328d. So, the default pixel frequency is set to 12.97 MHz. Attention: Register values greater then 983d generate pixel frequencies which are outside of the specified boundaries.
PCLK0	hDB	RW	h0048		
PCLK0[7:0]	hDB[7:0]	RW	72	0..255	**Pixel Clock Low** see Pixel Clock High
SCR1	hE1	RW	h0000		
VSU[3:0]	hE1[3:0]	RW	0	0..15	**Vertical Set Up Time** The vertical sync signal is internally sampled with the next edge of the horizontal sync edge. The phase relation between V and H differs from application to application. To guarantee (vertical) jitter free processing of external sync signals, the vertical sync impulse can be delayed before it is internally processed. The following formula shows how to delay the external V-sync before it is internally latched and processed. tV_delay = VSU * 128 / 40.5MHz

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
SCR0	hE2	RW	h0000		
RGB_D[1:0]	hE2[7:6]	RW	0	0..3	**RGB/COR Delay** The RGB and the COR signals can be delayed in reference to the generated BLANK signal. 00: 0 pixel delay 01: 1 pixel delay 10: 2 pixel delay 11: 3 pixel delay
HP	hE2[5]	RW	0	0,1	**HSync Polarity** This bit defines the polarity of the Hsync signal (master and slave mode). 0: normal polarity (active high) 1: negative polarity
VP	hE2[4]	RW	0	0,1	**VSync Polarity** This bit defines the polarity of the Vsync signal (master and slave mode). 0: normal polarity (active high) 1: negative polarity
INT	hE2[3]	RW	0	0,1	**Interlace / Non-interlace** TVT can either generate an interlaced or a non-interlaced timing (master mode only). Interlaced timing can only be created if VPR is an odd number. 0: interlaced timing is generated 1: non-interlaced timing is generated
MAST	hE2[0]	RW	0	0,1	**Master/Slave Mode** This bit defines the configuration of the display sync system 0: slave mode 1: master mode
SDV1	hE3	RW	h0000		
SDV1[1:0]	hE3[1:0]	RW	0	0..3	**Vertical Sync Delay High** This register defines the delay (in lines) from the vertical sync to the first line of character display area on the screen.
SDV0	hE4	RW	h0020		
SDV0[7:0]	hE4[7:0]	RW	32	0..255	**Vertical Sync Delay Low** This register defines the delay (in lines) from the vertical sync to the first line of character display area on the screen.
SDH1	hE5	RW	h0000		
SDH1[3:0]	hE5[3:0]	RW	0	0..15	**Horizontal Sync Delay High** This register defines the delay (in pixels) from the horizontal sync to the first pixel character display area on the screen.
SDH0	hE6	RW	h0048		
SDH0[7:0]	hE6[7:0]	RW	72	0..255	**Horizontal Sync Delay Low** This register defines the delay (in pixels) from the horizontal sync to the first pixel character display area on the screen.
EHCR	hE7	RW	h000A		
EHCR[7:0]	hE7[7:0]	RW	10	0..255	**End of Horizontal Clamp Phase** This register defines the end of the horizontal clamp phase from the positive edge of the horizontal sync impulse (at normal polarity). The end of clamp phase can be calculated by the following formula: tH_clmp_e = EHCR * 16 / 40.5MHz
BHCR	hE9	RW	h0000		
BHCR[7:0]	hE9[7:0]	RW	0	0..255	**Beginning of Horizontal Clamp Phase** This register defines the start of the horizontal clamp phase from the positive edge of the horizontal sync impulse (normal polarity is assumed). The beginning of clamp phase can be calculated by the following formula: tH_clmp_b = BHCR * 16 / 40.5MHz
BVCR1	hEA	RW	h0000		
BVCR1[1:0]	hEA[1:0]	RW	0	0..3	**Beginning of Vertical Clamp Phase High** This register defines the beginning of the vertical clamp phase from the positive edge of the vertical sync impulse (at normal polarity) in count of lines.

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
BVCR0	hEB	RW	h0000		
BVCR0[7:0]	hEB[7:0]	RW	0	0..255	**Beginning of Vertical Clamp Phase Low** This register defines the beginning of the vertical clamp phase from the positive edge of the vertical sync impulse (at normal polarity) in count of lines.
EVCR1	hEC	RW	h0000		
EVCR1[1:0]	hEC[1:0]	RW	0	0..3	**End of Vertical Clamp Phase High** This register defines the end of the vertical clamp phase from the positive edge of the vertical sync impulse (at normal polarity) in count of lines.
EVCR0	hED	RW	h0004		
EVCR0[7:0]	hED[7:0]	RW	4	0..255	**End of Vertical Clamp Phase Low** This register defines the end of the vertical clamp phase from the positive edge of the vertical sync impulse (at normal polarity) in count of lines.
VLR1	hEE	RW	h0002		
ODD_EVEN	hEE[6]	RW	0	0,1	**Odd/Even Detection** 0: even field 1: odd field
VSU2[3:0]	hEE[5:2]	RW	0	0..15	**Vertical Set Up Time 2** To realize the odd/even detection of a field next to VSU a second vertical setup time is defined. This horizontal delay is used to recognize the VSYNC to another time than it is recognized at VSU. The field detection is realized by detecting if in between these two latching-points the VSync is rising or stable: tV_delay2 = VSU2 * 128 / 40.5MHz If VSYNC became active for both VSU and VSU2, an odd field is detected. If VSYNC became active only for VSU an even field is detected.
VLR1[1:0]	hEE[1:0]	RW	2	0..3	**Vertical Lines per Field High** In sync master mode the TVT generates vertical sync impulses. If for example a normal PAL timing should be generated, set this register to 625d and set the interlace bit to 0. The hardware will generate a vertical impulse periodically after 312.5 lines. If a non-interlace picture with 312 lines should be generated, set this register to 312d and set the interlace bit to 1. The hardware will generate a vertical impulse every 312 lines. A progressive timing can be generated by setting VPR to 625d and interlace to 0.
VLR0	hEF	RW	h0071		
VLR0[7:0]	hEF[7:0]	RW	113	0..255	**Vertical Lines per Field Low** see Vertical Lines per Field High
HPR1	hF1	RW	h000A		
HPR1[3:0]	hF1[3:0]	RW	10	0..15	**Horizontal Period High** In sync master mode the TVT generates horizontal sync pulses. This register allows to adjust the period of the horizontal sync signal. The horizontal period is independent from the pixel frequency and can be adjusted with the following resolution: tH-period = HPR / 40.5MHz
HPR0	hF2	RW	h0020		
HPR0[7:0]	hF2[7:0]	RW	32	0..255	**Horizontal Period Low** In sync master mode the TVT generates horizontal sync pulses. This register allows to adjust the period of the horizontal sync signal. The horizontal period is independent from the pixel frequency and can be adjusted with the following resolution: tH-period = HPR / 40.5MHz
POINTARRAY1_1	hF3	RW	h0000		
POINT1_1[7:0]	hF3[7:0]	RW	0	0..255	**Display Pointer 1 High**
POINTARRAY1_0	hF4	RW	h0006		
POINT1_0[7:0]	hF4[7:0]	RW	6	0..255	**Display Pointer 1 Low**
POINTARRAY0_1	hF5	RW	h0000		
POINT0_1[7:0]	hF5[7:0]	RW	0	0..255	**Display Pointer 0 High**
POINTARRAY0_0	hF6	RW	h0000		
POINT0_0[7:0]	hF6[7:0]	RW	0	0..255	**Display Pointer 0 Low**

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
OSD_CTRL	hF8	RW	h0060		
FIT_STVAL	hF8[7]	RW	0	0,1	**Fine Italics Start Value** 0: fine italics signal is set to 0 for the lowest character pixel line 1: fine italics signal is set to 1 for the lowest character pixel line
EN_FIT	hF8[6]	RW	1	0,1	**Enable Fine Italics** 0: disable half clock shift 1: enable half clock shift
EN_IT	hF8[5]	RW	1	0,1	**Enable Italics** 0: software italics, italics bit in CDW is used for font addressing 1: hardware italics, italics bit in CDW is used for pixel shifting
EN_SS	hF8[4]	RW	0	0,1	**Enable Softscroll** Used to vertically scroll the display area with every vsync. 0: softscroll disabled 1: softscroll start
EN_LD_GDW	hF8[3]	RW	0	0,1	**Enable Load GDW** Used to avoid the download of the parameter settings of the GDW from the RAM to the display generator. 0: download disabled 1: download enabled
EN_DG_OUT	hF8[2]	RW	0	0,1	**Enable Display Generator Output** If the display generator is disabled the RGB outputs of the TVT are set to black and the outputs BLANK=DIS_BLANK and COR=DIS_COR. If the display generator is enabled the display information RGB, COR and BLANK is generated according to the parameter settings in the XRAM. 0: Display generator is disabled 1: Display generator is enabled
DIS_COR	hF8[1]	RW	0	0,1	**Disabled COR Level** Defines the level of the COR output if display generator is disabled. 0: COR=0 1: COR=1
DIS_BLANK	hF8[0]	RW	0	0,1	**Disabled Blank Level** Defines the level of the BLANK output if display generator is disabled. 0: Blank=0 1: Blank=1
MEMORY					
MEMCON	hE8	RW	h0000		
ISP	hE8[7]	RW	0	0,1	**In System Programming** 0: normal mode 1: Flash can be accessed via MOVX
XROM	hE8[6]	RW	0	0,1	**External ROM** Defines location of program ROM. The switching is delayed until first LJMP opcode is executed, to ensure correct switching from internal to external program ROM. 0: internal ROM (but XROM pin has higher priority) 1: external ROM (independent from XROM pin)
INTSRC1	hE8[5]	RW	0	0,1	**Interrupt 1 Source** 0: Int1 is source 1: CRT is source
INTSRC0	hE8[4]	RW	0	0,1	**Interrupt 0 Source** 0: Int0 is source 1: CRT is source
PATCH	hE8[3]	RW	0	0,1	**Patch Modul Enable** 0: disable 1: enable
BOTTOM	hE8[2]	RW	0	0,1	**Bottom Mapping** Defines top or bottom mapping of internal XRAM. 0: XRAM mapped below bank address FFFFh 1: XRAM mapped below bank address 7FFFh
NOMAP	hE8[1]	RW	0	0,1	**No Mapping** Defines mapping of internal XRAM. 0: XRAM is mapped into each of 16 banks 1: XRAM is mapped into bank0 only

Table 3–2: SFR Register Description, continued

Name	Sub	Dir	Reset	Range	Function
TWENTY	hE8[0]	RW	0	0,1	**XRAM Size** Defines if 20K or 16K internal XRAM is mapped into XDATA address space. 0: 16K XRAM 1: 20K XRAM

4. Data Sheet History

1. Advance Information: “VCT 49xyl, VCT 48xyl Controller, OSD and Text Processing”, 14.11.2003, 6251-573-6-1AI. First release of the advance information

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5. VCT 49xxI Data Sheet History

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