MSM699215

HIGH PERFORMANCE DIGITAL SIGNAL PROCESSOR FAMILY

GENERAL OUTLINE

The MSM699215 is a digital signal processor same in architecture as the MSM699210, but has serial ports.

The MSM699215 is capable of high speed execution of floating-point arithmetic operations (16-bit mantissa and 6-bit exponent parts) and 16-bit fixed-point arithmetic operations. Devices will be available with 100 ns machine cycle time. The MSM699215 incorporates a 2K-word x 32-bit ROM program memory and two 256-word x 22-bit data RAMs. The program and data memories can both be expanded up to 64K words via dedicated data and address lines.

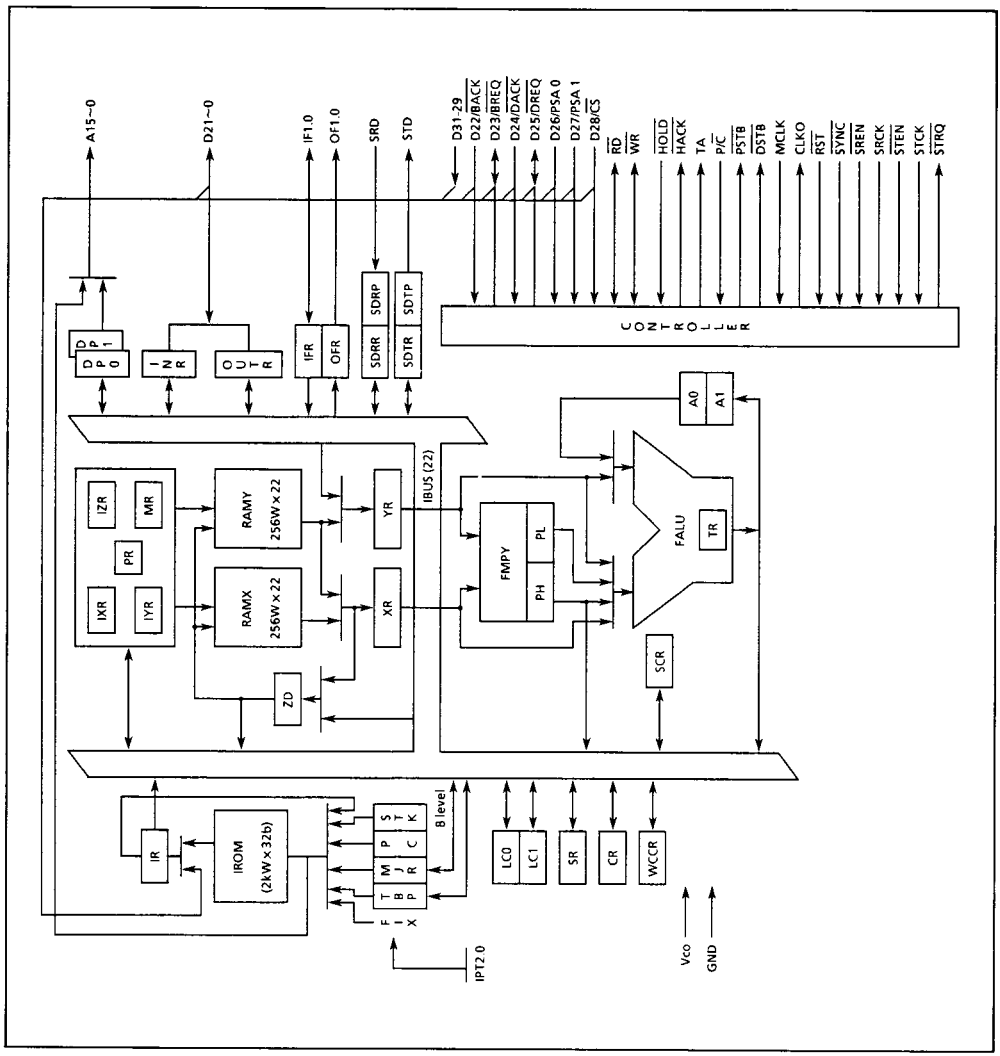
Like the MSM699210, the MSM699215 has processor and controller modes for external interface. The MSM699215 incorporates one serial port as well as a parallel interface and general-purpose input/output port. Thus the MSM699215 allows flexible system configuration. This device can also serve as a multiprocessor in a large scale system.

The MSM699215 applications include: image processors, speech processing equipment for speech recognition and speech analysis/synthesis, communication equipment such as high speed modems, codec and echo cancellers, instrumentation controllers, robotics, and in audio equipment.

KEY FEATURES

- Instruction cycle: 100 ns
- Arithmetic formats:
  - Floating-point arithmetic 16E6
  - Fixed-point arithmetic 16-bit
  - Logical arithmetic 22-bit
- Built-in 2K-word x 32-bit instruction ROM (Also usable as data ROM)
- Built-in 512-word x 22-bit data RAM
- 32-bit wide horizontal microinstruction
- 64K-word program memory area
- 64K-word data memory area
- Serial ports (one channel)
- Multiprocessor interface
- Microcomputer interface (8-bit and 16-bit)
- DMA controller connection capability
- Maximum 15-bit shift function (left or right)
- Double loop function
- Slower memory interface
- Power down mode
- Package: 84-pin PLCC
  100-pin FLAT
- 1.2 µm silicon gate CMOS

BLOCK DIAGRAM



SYMBOL	UNIT NAME	SIZE	SYMBOL	UNIT NAME	SIZE
IROM	Instruction ROM	2kW x 32b	FMPY	Floating-point Multiplier	
IR	Instruction Register	32b	PH	Product Register High	22b
TBP	Table Pointer	16b	PL	Product Register Low	15b
MJR	Map Jump Register	16b	FALU	Floating-point ALU	
PC	Program Counter	16b	TR	Temporary Register	22b
STK	Program Counter Stack	16b x 8 level	A0	Accumulator 0	22b
LC0	Loop Counter 0	12b	A1	Accumulator 1	22b
LC1	Loop Counter 1	4b	SCR	Shift Count Register	6b
CR	Control Register	12b	DP0	Data pointer 0	16b
SR	Status Register	10b	DP1	Data pointer 1	16b
WCCR	Wait Cycle Count Register	3b	INR	Input Register	22b
RAMX	Data RAM X	256w x 22b	OUTR	Output Register	22b
RAMY	Data RAM Y	256w x 22b	IFR	Input Flag Register	2b
XR	X Register	22b	OFR	Output Flag Register	2b
YR	Y Register	22b	SDRP	Serial Data Receive Port	
ZR	Z Register	22b	SDRR	Serial Data Receive Register	22b
IXR	Index Register X	8b	SDTP	Serial Data Transmit Port	
IYR	Index Register Y	8b	SDTR	Serial Data Transmit Register	22b
IZR	Index Register Z	8b			
MR	Mode Register	8b	IBUS	Internal Data Bus	22b
PR	Page Register	2b			

DIFFERENCES FROM MSM699210

The MSM699215 is upward compatible with the MSM699210 on the object level. In addition, the MSM699215 is enhanced with serial ports.

The following shows the different points with the MSM699215 from the MSM699210:

1. Added pins

Pin symbol	I/O	Function
SRCK	I	• Serial receive clock. • Receives data on the trailing edge of this clock.
SRD	I	• Serial receive data input pin.
$\overline{\text{SREN}}$	I	• Enables serial reception. • Terminating reception by the internal counter and making this signal active. →Making this signal inactive and enabling receive termination.
STCK	I	• Serial transmit clock. • Transmit data on the leading edge.
STD	O (3-state)	• Serial transmit data outputs pin. • In a Hz status when the $\overline{\text{STEN}}$ signal is inactive.
$\overline{\text{STEN}}$	I	• Enables serial transmission • Terminating transmission by the internal counter and making this signal active. →Making this signal inactive and enabling transmit termination.
$\overline{\text{STRQ}}$	O	• Serial transmission request. • Becomes active on data transfer to the serial transmirt port.

Note: The MSM699215 does not have $\overline{\text{IPT1}}$, IM, and IORQ provided for the MSM699210.

2. Serial Interface

The MSM699215 has the serial interface function for a transmission channel and a reception channel, providing the following features:

- One pair of port and register for transmission and the other for reception allow continuous transfer.

  SDRP: Port for reception
  SDRR: Register for reception (allowing reading/writing via IBUS)
  SDTP: Port for transmission
  SDTR: Register for transmission (allowing reading/writing via IBUS)

- Data format conversion function.

  Zero extension/two's complement code extension (only reception)
  Offset-binary to two's-complement (for reception)
  Straight-binary to two's-complement (for reception)
  Two's-complement to offset-binary conversion (for transmission)
  Two's-complement to straight-binary conversion (for transmission)

- Transfer bit mode:
  22-bit, 16-bit, or 8-bit mode can be selected to transfer the following bits by pin control ($\overline{SREN}$ and $\overline{STEN}$):

  22-bit mode: Transfer 2 to 22 bits.
  16-bit mode: Transfer 2 to 16 bits.
  8-bit mode: Transfer 2 to 8 bits.

  The seven-bit register SCTR performs the above data format conversion and transfer bit selection.

6	5	4	3	2	1	0
STM2	STM1	STM0	SRM3	SRM2	SRM1	SRM0

Serial reception (Using SRM3 to SRM0)

SRM3	SRM2	SRM1	SRM0	Mode	Operation Example
0	0	0	0	22-bit & MSB through mode	Interface between DSPs
1	0	0	0	8-bit & zero extension & MSB through mode	8-2-bit ADC (straight binary output)
1	0	1	0	8-bit & sign extension & MSB through mode	Codec, 8-2-bit ADC (two's complement output)
1	0	1	1	8-bit & sign extension & MSB reverse mode	8-2-bit ADC (offset binary output)
1	1	0	0	16-bit & zero extension & MSB through mode	16-9-bit ADC (straight binary output)
1	1	1	0	16-bit & zero extension & MSB through mode	16-9-bit ADC (two's complement output)
1	1	1	1	16-bit & sign extension & MSB reverse mode	16-9-bit ADC (offset binary output)

Serial transmission (Using STM2 to STM0)

STM2	STM1	STM0	Mode	Operation Example
0	0	0	22-bit mode	Interface between DSP's
1	0	0	8-bit & MSB through mode	Codec, 8-2-bit DAC (two's complement input)
1	0	1	8-bit & MSB reverse mode	8-2-bit DAC (offset binary input)
1	1	0	16-bit & MSB through mode	16-9-bit DAC (two's complement input)
1	1	1	16-bit & MSB reverse mode	16-9-bit DAC (offset binary input)

3. Instruction Type

The MSM699215 is added with some transfer and jump instructions to support the newly added serial interface function. The following fields are added:

JC field (Jump Condition)

MNEMONIC	D24	D23	D22	D21	D20	D19	CONDITION
T	0	0	0	0	0	0	ALWAYS TRUE
F	1	0	0	0	0	0	ALWAYS FALSE
MI	0	0	0	0	0	1	MINUS
PL	1	0	0	0	0	1	PLUS
Z22	0	0	0	0	1	0	ZERO 22-BIT
NZ22	1	0	0	0	1	0	NOT ZERO 22-BIT
Z	0	0	0	0	1	1	ZERO
NZ	1	0	0	0	1	1	NOT ZERO
OV	0	0	0	1	0	0	OVERFLOW
NOV	1	0	0	1	0	0	NOT OVERFLOW
CS	0	0	0	1	0	1	CARRY SET
CC	1	0	0	1	0	1	CARRY CLEAR
MV	0	0	0	1	1	0	MANTISSA OVERFLOW
NMV	1	0	0	1	1	0	NOT MARTISSA OVERFLOW
EV	0	0	0	1	1	1	EXPONENT OVERFLOW
NEV	1	0	0	1	1	1	NOT EXPONENT OVERFLOW
EU	0	0	1	0	0	0	EXPONENT UNDERFLOW
NEU	1	0	1	0	0	0	NOT EXPONENT UNDERFLOW
IR	0	0	1	0	0	1	INPUT READY
NIR	1	0	1	0	0	1	NOT INPUT READY
OR	0	0	1	0	1	0	OUTPUT READY
NOR	1	0	1	0	1	0	NOT OUTPUT READY
EVU	0	0	1	0	1	1	EXPONENT OVERFLOW OR UNDERFLOW
NEVU	1	0	1	0	1	1	NOT EXPONENT OVERFLOW OR UNDERFLOW
IF0S	0	0	1	1	0	0	IF0 FLAG SET
IF0C	1	0	1	1	0	0	IF0 FLAG CLEAR
IF1S	0	0	1	1	0	1	IF1 FLAG SET
IF1C	1	0	1	1	0	1	IF1 FLAG CLEAR
C1Z	1	0	1	1	1	0	LOOP COUNTER 1 ZERO
C1NZ	0	0	1	1	1	0	LOOP COUNTER 1 NOT ZERO
BE	0	0	1	1	1	1	BUS ENABLE
NBE	1	0	1	1	1	1	BUS NOT ENABLE
GE	1	1	0	0	0	0	GREATER THAN OR EQUAL
LT	0	1	0	0	0	0	LESS THAN
XRPL	1	1	0	0	1	1	XR PLUS
XRMI	0	1	0	0	1	1	XR MINUS
YRPL	1	1	0	1	0	0	YR PLUS
YRMI	0	1	0	1	0	0	YR MINUS
A0PL	1	1	0	1	0	1	A0 PLUS
A0MI	0	1	0	1	0	1	A0 MINUS
A1PL	1	1	0	1	1	0	A1 PLUS
A1MI	0	1	0	1	1	0	A1 MINUS
※ SRRF	0	1	0	0	1	0	SDRR DATA FULL
※ SRRE	1	1	0	0	1	0	SDRR DATA EMPTY
※ STRF	0	1	0	0	0	1	SDTR DATA FULL
※ STRE	1	1	0	0	0	1	SDTR DATA EMPTY

Note: Mnemonics marked by ※ are neither provided for MSM6992 nor MSM699210.

DST field (Destination IBUS)

MNEMONIC	D20	D19	D18	D17	D16	SELECT REGISTER
–	0	0	0	0	0	NON SELECT
LC1	0	0	0	0	1	LOOP COUNTER 1
MJR	0	0	0	1	0	MAP JUMP REGISTER
OFR	0	0	0	1	1	OUTPUT LFAG REGISTER
IXR	0	0	1	0	0	INDEX REGISTER X
IYR	0	0	1	0	1	INDEX REGISTER Y
IZR	0	0	1	1	0	INDEX REGISTER Z
MR	0	0	1	1	1	MODE REGISTER
TBP	0	1	0	0	0	TABLE POINTER
DP0	0	1	0	0	1	DATA POINTER 0
DP1	0	1	0	1	0	DATA POINTER 1
LC0	0	1	0	1	1	LOOP COUNTER 0
SCR	0	1	1	0	0	SHIFT COUNT REGISTER (D3~D0)
SR	0	1	1	0	1	STATUS REGISTER
CR	0	1	1	1	0	CONTROL REGISTER
SCR6	0	1	1	1	1	SHIFT COUNT REGISTER (D21~D16)
* INR	1	0	0	0	1	INPUT REGISTER
* A0	1	0	0	1	0	ACCUMULATOR 0
ZR	1	0	1	0	0	Z REGISTER
* A1	1	0	1	1	0	ACCUMULATOR 1
YR	1	1	0	0	0	Y REGISTER
* WCCR	1	1	0	1	0	WAIT CYCLE COUNT REGISTER
OUTR	1	1	1	0	0	OUTPUT REGISTER
* PR	1	1	1	1	0	PAGE REGISTER
※ SCTR	1	0	1	0	1	SERIAL CONTROL REGISTER
※ SDRR	1	0	1	1	1	SERIAL DATA RECEIVE REGISTER
※ SDTR	1	1	0	0	1	SERIAL DATA TRANSMIT REGISTER

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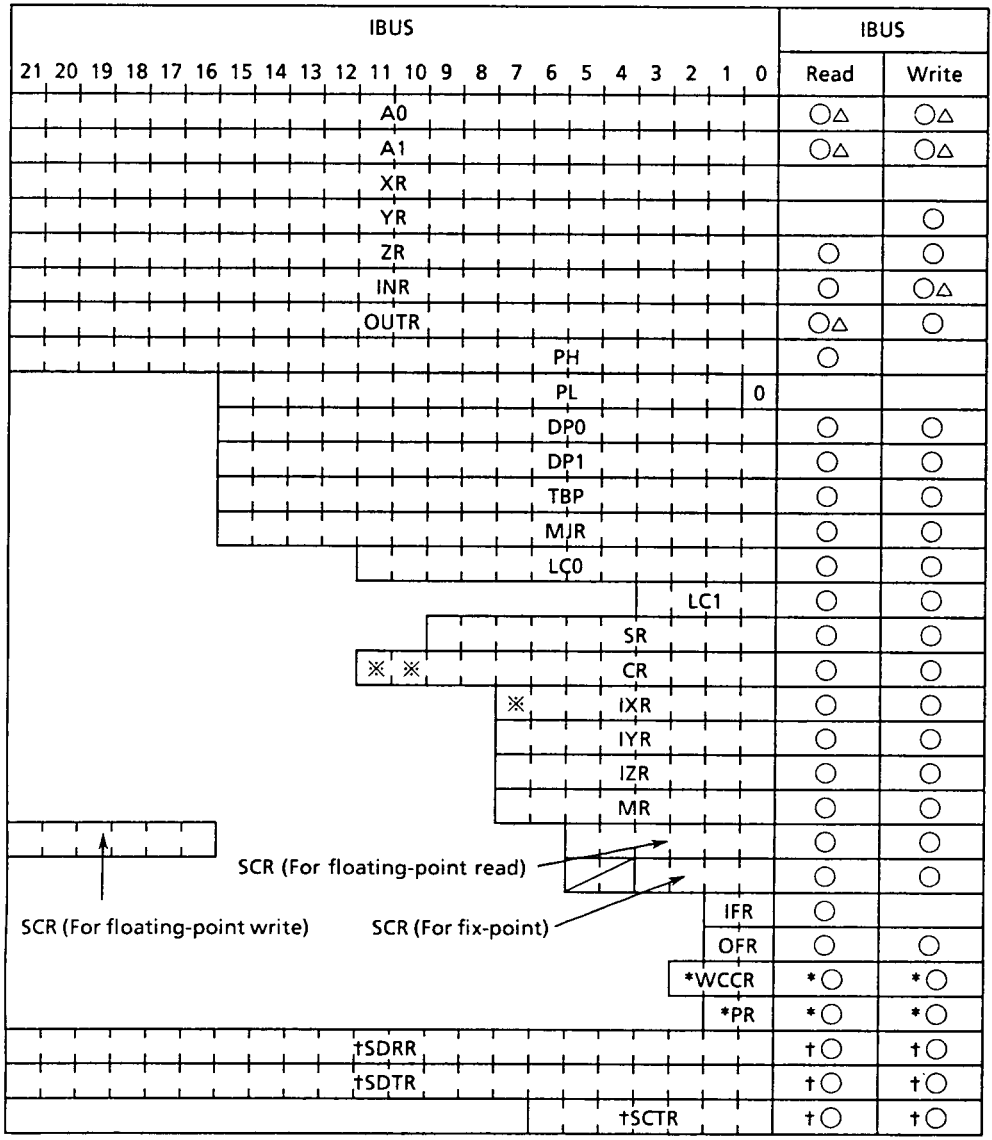
Mnemonics marked by * are not provided for MSM6992.

SRC field (Source IBUS)

MNEMONIC	D26	D25	D24	D23	D23	SELECT REGISTER
PH	0	0	0	0	0	PRODUCT REGISTER HIGH
ALU	0	0	0	0	1	FALU OUTPUT (PSEUDO REGISTER)
INR	0	0	0	1	0	INPUT REGISTER
TBL	0	0	0	1	1	TABLE OUTPUT (PSEUDO REGISTER)
IXR	0	0	1	0	0	INDEX REGISTER X
IYR	0	0	1	0	1	INDEX REGISTER Y
IZR	0	0	1	1	0	INDEX REGISTER Z
MR	0	0	1	1	1	MODE REGISTER
TBP	0	1	0	0	0	TABLE POINTER
DP0	0	1	0	0	1	DATA POINTER 0
DP1	0	1	0	1	0	DATA POINTER 1
LC0	0	1	0	1	1	LOOP COUNTER 0
SCR	0	1	1	0	0	SHIFT COUNT REGISTER
SR	0	1	1	0	1	STATUS REGISTER
CR	0	1	1	1	0	CONTROL REGISTER
ZR	0	1	1	1	1	Z REGISTER
MJR	1	0	0	0	0	MAP JUMP REGISTER
IFR	1	0	0	0	1	INPUT FLAG REGISTER
OFR	1	0	0	1	0	OUTPUT FLAG REGISTER
LC1	1	0	0	1	1	LOOP COUNTER 1
* A0	1	0	1	0	0	ACCUMULATOR 0
* A1	1	0	1	0	1	ACCUMULATOR 1
* WCCR	1	0	1	1	0	WAIT CYCLE COUNT REGISTER
* PR	1	0	1	1	1	PAGE REGISTER
* OUTR	1	1	0	1	1	OUTPUT REGISTER
※ SCTR	1	1	0	0	0	SERIAL CONTROL REGISTER
※ SDTR	1	1	0	0	1	SERIAL DATA TRANSMIT REGISTER
※ SDRR	1	1	0	1	0	SERIAL DATA RECEIVE REGISTER

Note: Mnemonics marked by ※ are neither provided for MSM6992 nor MSM699210.
Mnemonics marked by * are not provided for MSM6992.

Register Read/Write List

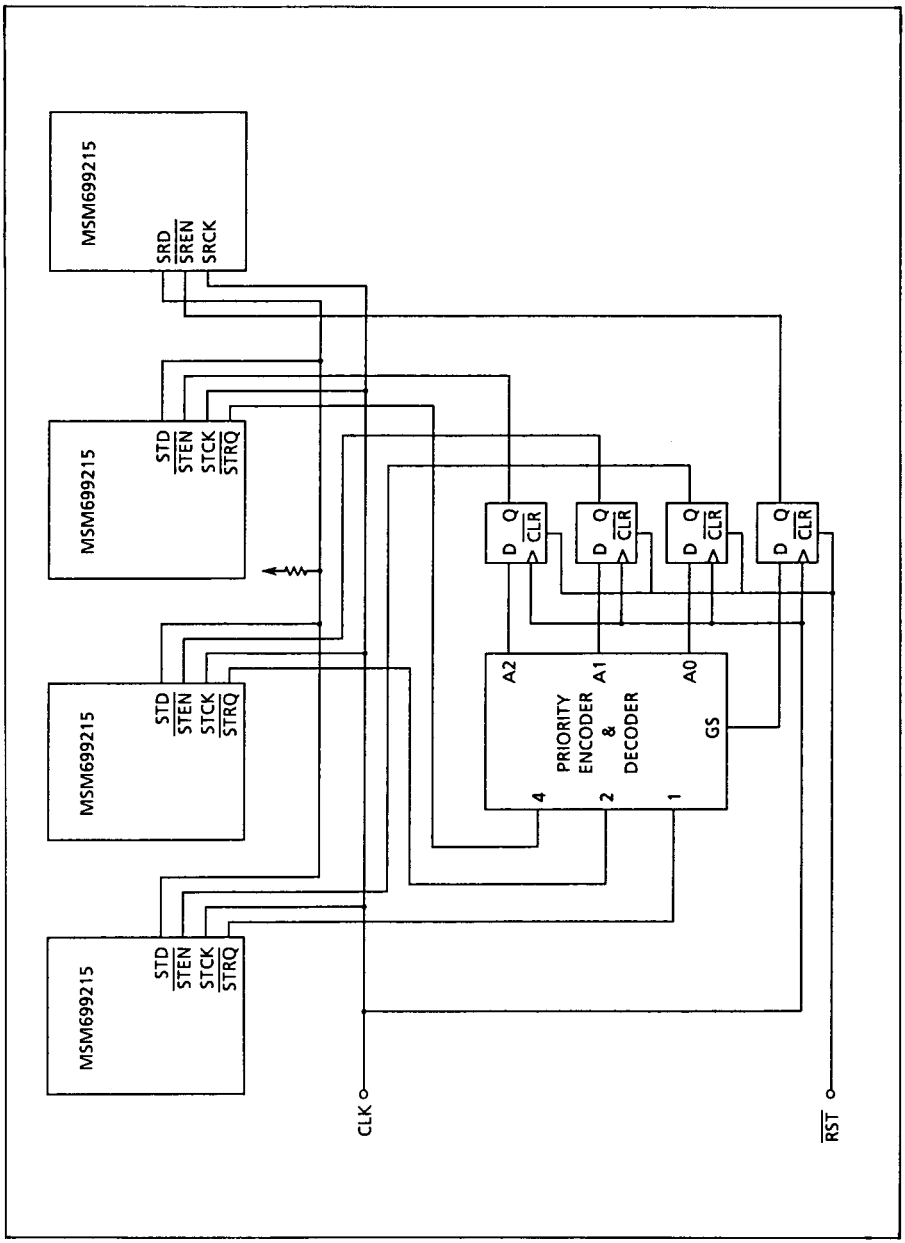


Note:

- The MSM6992 dose not have the functions marked by *, △ and †.
- The MSM6992 dose not have the bits marked by ※.
- The MSM699210 dose not have the functions marked by †.

SYSTEM CONFIGURATION

- Multi-DSP Serial Interface (between 3 transmitters and 1 receivers)



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