STANDARD MICROSYSTEMS CORPORATION

4100 Series
CG4103

CHARACTER GENERATOR

2240-Bit Programmable (ROM) 64 Characters of 5 x 7 Bits

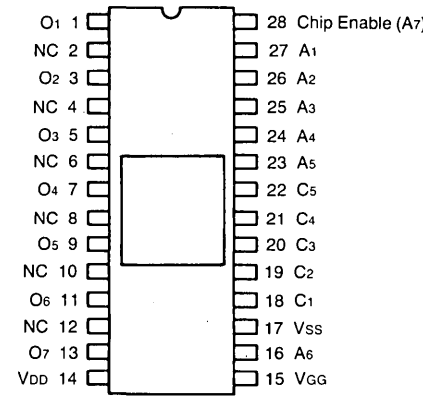
FEATURES

- ☐ Static Operation, no clocks required.
- ☐ 2240-Bit Capacity, fully decoded
- ☐ 64 Characters of 35 Bits (5 x 7)
- ☐ Column by Column Output—Column Scan
- ☐ TTL Compatible
- ☐ Wired "OR" Capability for memory expansion
- ☐ Power Supplies: +14v, −14v or +12v, −12v, or +5v, −12v
- ☐ Eliminates need for +12v power supply
- ☐ Single mask custom programming

APPLICATIONS

- ☐ Matrix Printers
- ☐ Vertical Scan Alphanumeric Displays
- ☐ Billboard and Stock Market Displays
- ☐ Strip Printer
- ☐ LED Matrix Arrays

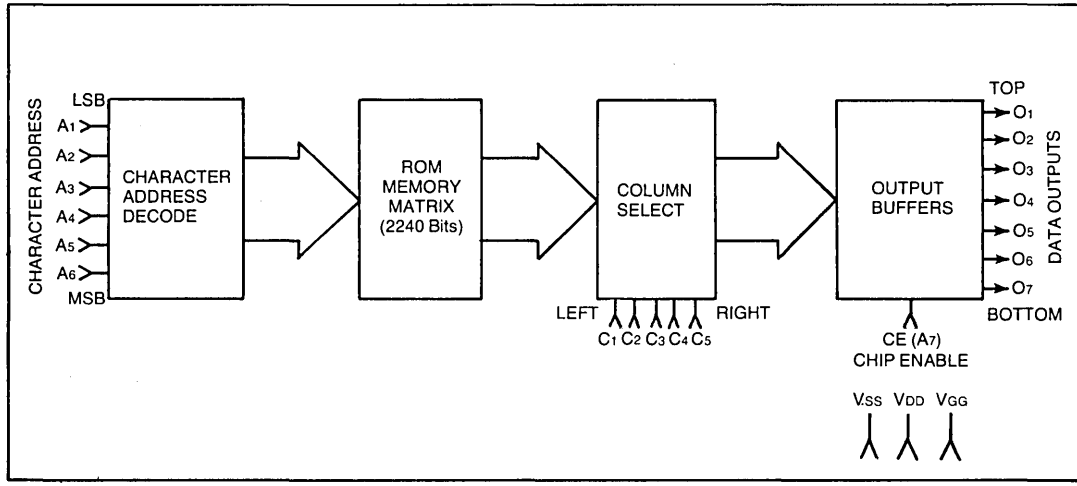
PIN CONFIGURATION



NC = No Connection

SECTION VII

BLOCK DIAGRAM



General Description

The CG4100 Series MOS Read Only Memories (ROMs) are designed specifically for dot-matrix character generation where column by column output data is desired. Each ROM contains 2240 bits of programmable storage, organized as 64 characters, each having 5 columns of 7 bits.

The output word appears as a 5 word sequence on each of the output lines. Sequence is controlled by the 5 Column Select lines. By strobing the first select line, the first group of 7 bits (first column) is obtained at the output. By sequentially strobing C_1 through C_5 the font of the addressed character would be displayed. The character address may remain fixed while the column select changes.

Since only 6 address bits are required in order to decode the 64 stored characters, the seventh bit (A_7) may be used as a chip enable. The chip enable (CE) in conjunction with the single ended open drain output buffers allow for memory expansion through wired "OR" connection.

The CG4100 Series contains an USASCII character font. Custom memory patterns are provided through the use of customer provided encoding sheets, tapes, or card decks.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	−25°C to + 85°C
Storage Temperature Range	−55°C to +150°C
Voltage on any Pin, with respect to V_{SS}	+0.3V to −30V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

RECOMMENDED OPERATING CONDITIONS ($-25°C \leq T_A \leq +85°C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Suppy Voltage	V_{SS}		0.0		V
Supply Voltage	V_{DD}	−12.0	−14.0	−16.0	V
Supply Voltage	V_{GG}	−24.0	−28.0	−29.0	V
Input Voltage, logic "O" Logic "O"=most positive level	V_{IH}	V_{SS} −1.5	V_{SS}		V
Input Voltage, logic "I" Logic "I"=most negative level	V_{IL}		V_{DD}	V_{SS}−11	V

Note: The design of the CG4100 permits a broad range of operation that allows the user to take advantage of readily available power supplies; e.g. +5V, −12V. See "Operational Interface—To/From TTL logic" diagram.

ELECTRICAL CHARACTERISTICS (V_{SS}=+14v, V_{GG}=−14v, V_{DD}=Ground, T_A=25°C, unless otherwise noted)

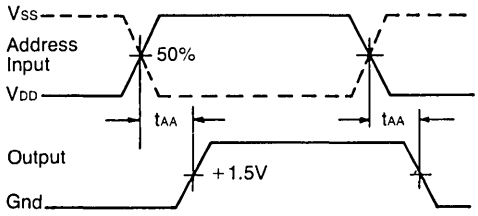
Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output Blank Current	I_{OB}	—	—	10	μa	V_{DD} applied to output see Note 1.
Output Dot Current	I_{OD}	2.5	—	—	ma	V_{DD} applied to output see Note 1.
Input Leakage Current	I_{IN}	—	—	10	μa	V_{IN}=OV
Output Voltage	V_O	—	2.0	—	V	I_O=0.5ma
		—	5.0	—	V	I_O=2.0ma
Address Access Time	t_{AA}	—	—	1200	ns	
Column Select Access Time	t_{CA}	—	—	600	ns	
Chip Enable Access Time	t_{CE}	—	—	400	ns	
Power Dissipation		—	—	400	mw	Output unconnected

Note 1: An output dot is defined as the ON state of the MOS output transmitter. An output blank is defined as the OFF state.

Description of Pin Functions

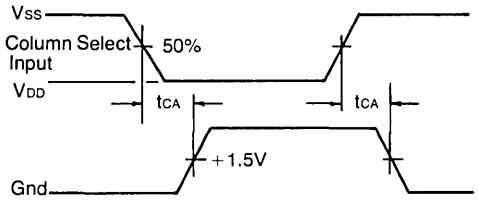
Pin No.	Symbol	Name	Function
1, 3, 5, 7 9, 11, 13	O_1, O_2, O_3, O_4 O_5, O_6, O_7	Outputs	7 Data Outputs
14	V_{DD}	V_{DD}	Usually connected to Ground
15	V_{GG}	V_{GG}	Negative power supply: −14v or −12v
16	A_6	Address	Bit 6 of the character address
17	V_{SS}	V_{SS}	Positive power supply: +14v or +12v or +5v
18-22	C_1-C_5	Column Select	Column Select inputs
23-27	A_5-A_1	Address	Bits 1 through 5 of the character address
28	CE(A_7)	Chip Enable	Chip Enable for memory expansion

ADDRESS ACCESS TIMING



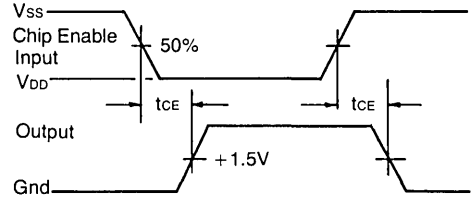
Only one of the five Column Select inputs is at logic "1."
Chip Enable input is at logic "1."

COLUMN SELECT ACCESS TIMING



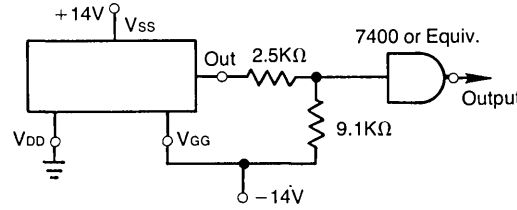
All Column Select inputs are at logic "0" except one under test.
Address inputs are set in a dc state.
Chip Enable input is at logic "1."

CHIP ENABLE ACCESS TIMING



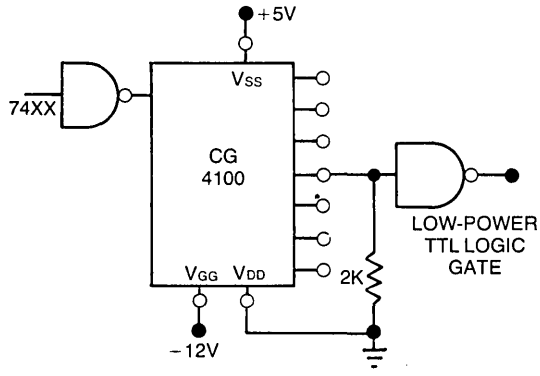
Only one of the five Column Select inputs is a logic "1."
Address inputs are set in a dc state.

AC TEST CIRCUIT

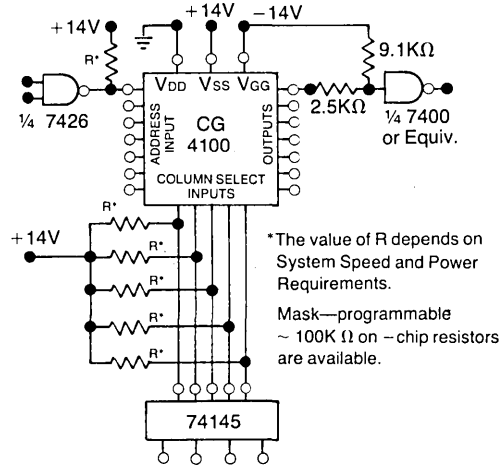


$t_r = t_f < 50$ ns for all timing diagram forcing functions.
All output waveforms are measured at the output of the 7400 TTL gate.

OPTIONAL INTERFACE TO/FROM TTL LOGIC



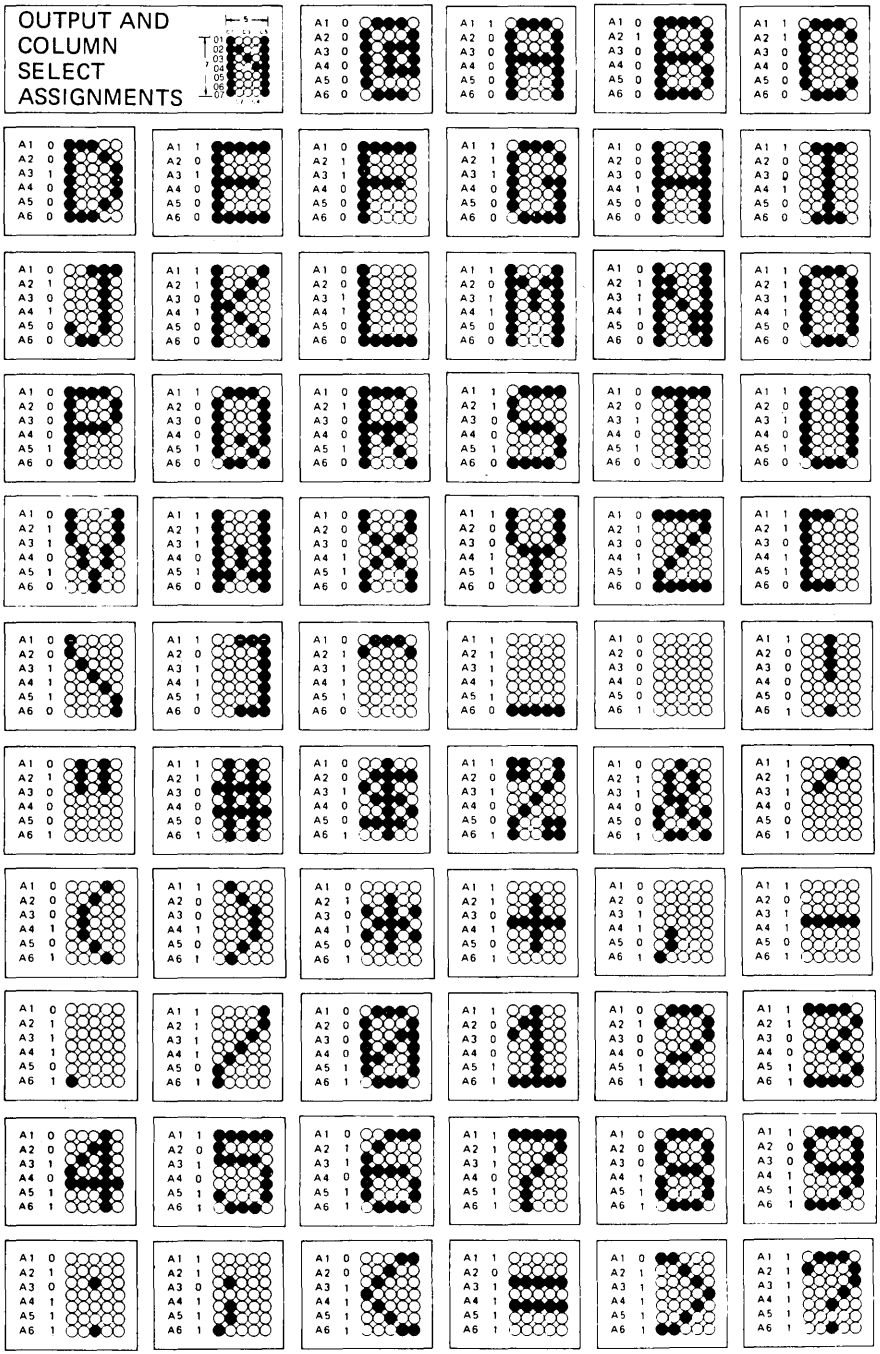
INTERFACE TO TTL LOGIC



*The value of R depends on System Speed and Power Requirements.

Mask—programmable ~ 100K Ω on −chip resistors are available.

SECTION VII



Pin-for-Pin Equivalent for: TMS 4103 MK2002 S8499.

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