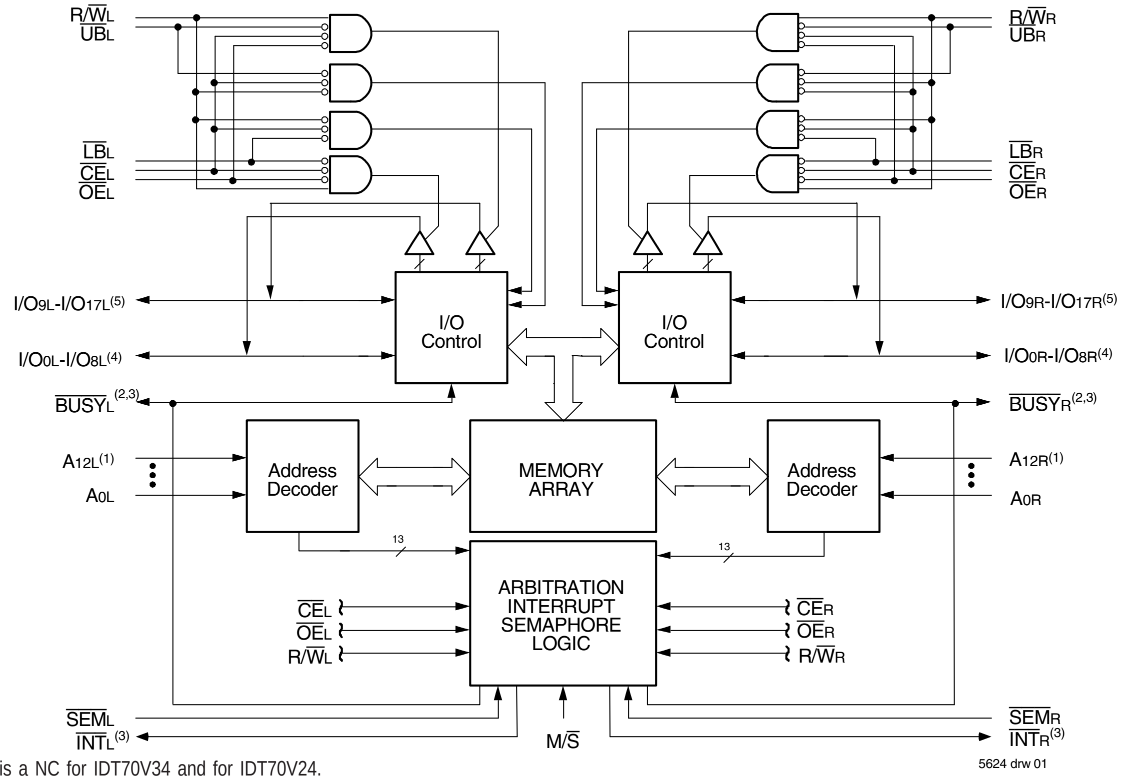
HIGH-SPEED 3.3V
8/4K x 18 DUAL-PORT
8/4K x 16 DUAL-PORT
STATIC RAM

70V35/34S/L
70V25/24S/L

Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **High-speed access**
  - **IDT70V35**
    - *Commercial: 15ns (max.)*
    - *Industrial: 20ns*
  - **IDT70V34**
    - *Commercial: 15ns (max.)*
  - **IDT70V25**
    - *Commercial: 15/35ns (max.)*
    - *Industrial: 20/25ns*
  - **IDT70V24**
    - *Commercial: 15//35/55ns (max.)*
    - *Industrial: 15/20ns*
- **Low-power operation**
  - ***IDT70V35/34L***
    Active: 415mW (typ.)
    Standby: 660µW (typ.)
  - ***IDT70V25/24S***
    Active: 400mW (typ.)
    Standby: 3.3mW (typ.)
  - ***IDT70V25/24L***
    Active: 380mW (typ.)
    Standby: 660µW (typ.)
- **Separate upper-byte and lower-byte control for multiplexed bus compatibility**
- **IDT70V35/34 (IDT70V25/24) easily expands data bus width to 36 bits (32 bits) or more using the Master/Slave select when cascading more than one device**
- **M/$\overline{\text{S}}$ = V_{IH} for $\overline{\text{BUSY}}$ output flag on Master**
  M/$\overline{\text{S}}$ = V_{IL} for $\overline{\text{BUSY}}$ input on Slave
- **$\overline{\text{BUSY}}$ and Interrupt Flag**
- **On-chip port arbitration logic**
- **Full on-chip hardware support of semaphore signaling between ports**
- **Fully asynchronous operation from either port**
- **LVTTL-compatible, single 3.3V (±0.3V) power supply**
- **Available in a 100-pin TQFP (IDT70V35/34) & (IDT70V25/24), and 84-pin PLCC (IDT70V24)**
- **Industrial temperature range (-40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram



NOTES:
1. A_{12} is a NC for IDT70V34 and for IDT70V24.
2. (MASTER): $\overline{\text{BUSY}}$ is output; (SLAVE): $\overline{\text{BUSY}}$ is input.
3. $\overline{\text{BUSY}}$ outputs and $\overline{\text{INT}}$ outputs are non-tri-stated push-pull.
4. I/O_{0X} - I/O_{7X} for IDT70V25/24.
5. I/O_{8X} - I/O_{15X} for IDT70V25/24.

OCTOBER 2019

Description

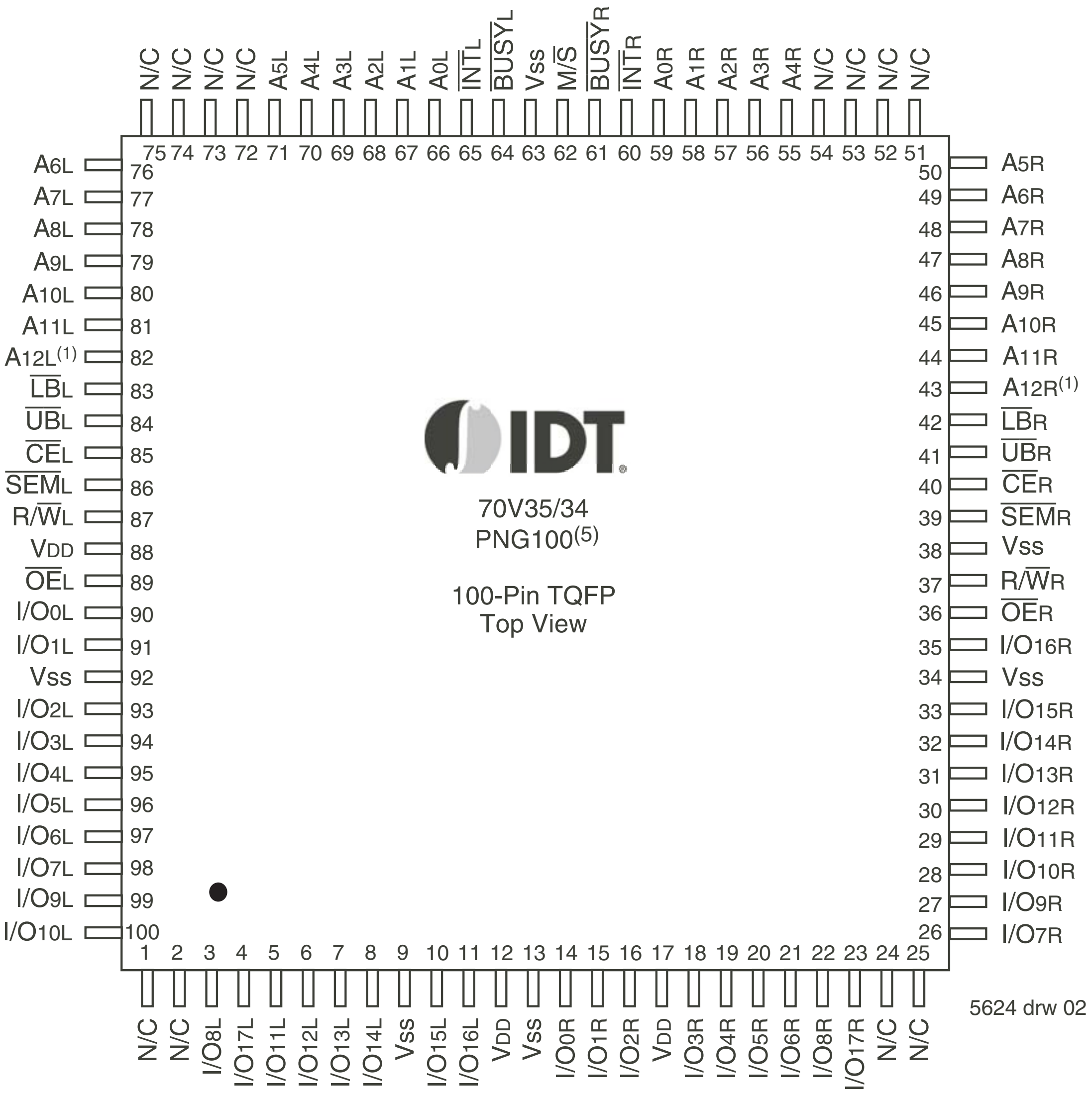
The IDT70V35/34 (IDT70V25/24) is a high-speed 8/4K x 18 (8/4K x16) Dual-Port Static RAM. The IDT70V35/34 (IDT70V25/24) is designed to be used as a stand-alone Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 36-bit (32-bit) or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 430mW (IDT70V35/34) and 400mW (IDT70V25/24) of power.

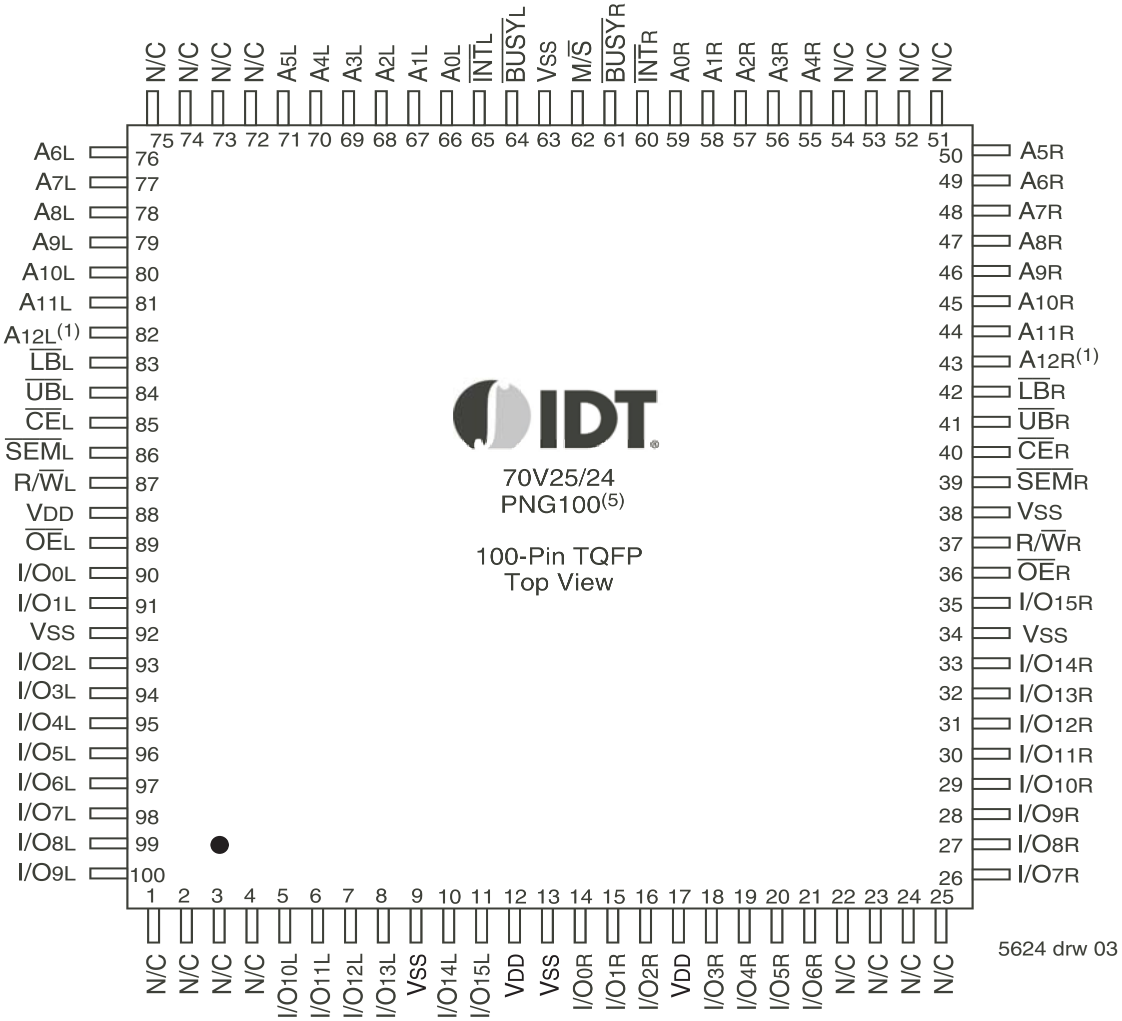
The IDT70V35/34 (IDT70V25/24) is packaged in a plastic 100-pin Thin Quad Flatpack. The IDT70V24 is packaged in a 84-Pin PLCC.

Pin Configurations[1,2,3,4]



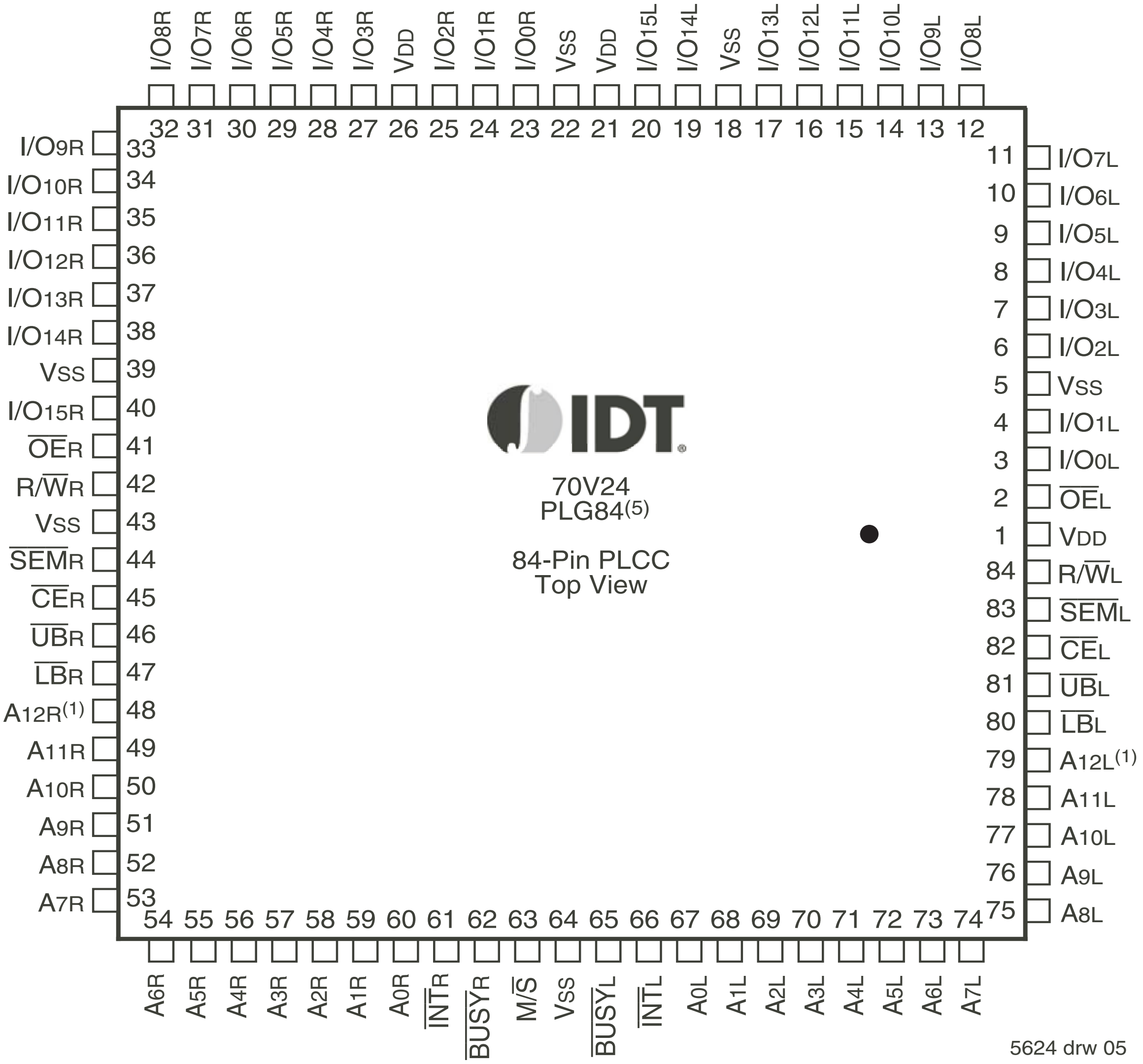
NOTES:
1. A_{12} is a NC for IDT70V34.
2. All V_{DD} pins must be connected to power supply.
3. All V_{SS} pins must be connected to ground.
4. PNG100 package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.

Pin Configurations[1,2,3,4] (con't)



NOTES:
1. A_{12} is a NC for IDT70V24.
2. All V_{DD} pins must be connected to power supply.
3. All V_{SS} pins must be connected to ground.
4. PNG100 package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.

Pin Configurations[1,2,3,4] (con't)



NOTES:
1. A12 is a NC for IDT70V24.
2. All VDD pins must be connected to power supply.
3. All VSS pins must be connected to ground.
4. PLG84 package body is approximately 1.15 in x 1.15 in x .17 in.
5. This package code is used to reference the package diagram.

Pin Names

Left Port	Right Port	Names
$\overline{\text{CE}}_\text{L}$	$\overline{\text{CE}}_\text{R}$	Chip Enable
$\text{R}/\overline{\text{W}}_\text{L}$	$\text{R}/\overline{\text{W}}_\text{R}$	Read/Write Enable
$\overline{\text{OE}}_\text{L}$	$\overline{\text{OE}}_\text{R}$	Output Enable
$\text{A}_{0\text{L}}$ - $\text{A}_{12\text{L}}$[1]	$\text{A}_{0\text{R}}$ - $\text{A}_{12\text{R}}$[1]	Address
$\text{I/O}_{0\text{L}}$ - $\text{I/O}_{17\text{L}}$[2]	$\text{I/O}_{0\text{R}}$ - $\text{I/O}_{17\text{R}}$[2]	Data Input/Output
$\overline{\text{SEM}}_\text{L}$	$\overline{\text{SEM}}_\text{R}$	Semaphore Enable
$\overline{\text{UB}}_\text{L}$	$\overline{\text{UB}}_\text{R}$	Upper Byte Select[3]
$\overline{\text{LB}}_\text{L}$	$\overline{\text{LB}}_\text{R}$	Lower Byte Select[4]
$\overline{\text{INT}}_\text{L}$	$\overline{\text{INT}}_\text{R}$	Interrupt Flag
$\overline{\text{BUSY}}_\text{L}$	$\overline{\text{BUSY}}_\text{R}$	Busy Flag
$\text{M}/\overline{\text{S}}$		Master or Slave Select
V_DD		Power (3.3V)
V_SS		Ground (0V)

5624 tbl 01

NOTES:
1. A_{12} is a NC for IDT70V34 and for IDT70V24.
2. $\text{I/O}_{0\text{X}}$ - $\text{I/O}_{15\text{X}}$ for IDT70V25/24.
3. Upper Byte Select controls pins 9-17 for IDT70V35/34 and controls pins 8-15 for IDT70V25/24.
4. Lower Byte Select controls pins 0-8 for IDT70V35/34 and controls pins 0-7 for IDT70V25/24.

Truth Table I: Non-Contention Read/Write Control

Inputs[1]						Outputs		
$\overline{\text{CE}}$	$\text{R}/\overline{\text{W}}$	$\overline{\text{OE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	$\overline{\text{SEM}}$	$\text{I/O}_{9\text{-}17}$[3]	$\text{I/O}_{0\text{-}8}$[2]	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATA_IN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATA_IN	Write to Lower Byte Only
L	L	X	L	L	H	DATA_IN	DATA_IN	Write to Both Bytes
L	H	L	L	H	H	DATA_OUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATA_OUT	Read Lower Byte Only
L	H	L	L	L	H	DATA_OUT	DATA_OUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

5624 tbl 02

NOTES:
1. $\text{A}_{0\text{L}}\text{-}\text{A}_{12\text{L}} \neq \text{A}_{0\text{R}}\text{-}\text{A}_{12\text{R}}$ for IDT70V35/34 and $\text{A}_{0\text{L}}\text{-}\text{A}_{11\text{L}} \neq \text{A}_{0\text{R}}\text{-}\text{A}_{11\text{R}}$ for IDT70V25/24.
2. Outputs listed in the table are for IDT70V35/34. Outputs for IDT70V25/24 are $\text{I/O}_{0\text{X}}$-$\text{I/O}_{7\text{X}}$.
3. Outputs listed in the table are for IDT70V35/34. Outputs for IDT70V25/24 are $\text{I/O}_{8\text{X}}$-$\text{I/O}_{15\text{X}}$.

Truth Table II: Semaphore Read/Write Control[1]

Inputs						Outputs		
$\overline{\text{CE}}$	$\text{R}/\overline{\text{W}}$	$\overline{\text{OE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	$\overline{\text{SEM}}$	$\text{I/O}_{9\text{-}17}$[1]	$\text{I/O}_{0\text{-}8}$[1]	Mode
H	H	L	X	X	L	DATA_OUT	DATA_OUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATA_OUT	DATA_OUT	Read Data in Semaphore Flag
H	↑	X	X	X	L	DATA_IN	DATA_IN	Write I/O_0 into Semaphore Flag
X	↑	X	H	H	L	DATA_IN	DATA_IN	Write I/O_0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

5624 tbl 03

NOTE:
1. There are eight semaphore flags written to via I/O_0 and read from all of the I/O's (I/O_0-I/O_{17} for IDT70V35/34) and (I/O_0-I/O_{15} for IDT70V25/24). These eight semaphores are addressed by A_0-A_2.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	50	mA

5624 tbl 04

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq V_{DD}$ + 0.3V.

Capacitance[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	9	pF
C_{OUT}[2]	Output Capacitance	V_{OUT} = 0V	10	pF

5624 tbl 07

NOTES:

1. This parameter is determined by device characterization but is not production tested.
2. C_{OUT} also references $C_{I/O}$.

Maximum Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0^{O}C to $+70^{O}$C	0V	3.3V $\pm$ 0.3V
Industrial	-40^{O}C to $+85^{O}$C	0V	3.3V $\pm$ 0.3V

5624 tbl 05

NOTE:

1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3[2]	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

5624 tbl 06

NOTES:

1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{DD} + 0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V35/34/25/24S		70V35/34/25/24L		Unit
			Min.	Max.	Min.	Max.	
$\lvert I_{LI} \rvert$	Input Leakage Current[1]	V_{DD} = 3.6V, V_{IN} = 0V to V_{DD}	—	10	—	5	µA
$\lvert I_{LO} \rvert$	Output Leakage Currentt[1]	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{DD}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

5624 tbl 08

NOTE:

1. At $V_{DD} \leq$ 2.0V leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V35/34(1) (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V35/34X15 Com'l Only Typ.(2)	70V35/34X15 Com'l Only Max.	70V35/34X20 Com'l & Ind Typ.(2)	70V35/34X20 Com'l & Ind Max.	70V35/34X25 Com'l Only Typ.(2)	70V35/34X25 Com'l Only Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{\text{CE}}$ = V_{IL}, Outputs Disabled $\overline{\text{SEM}}$ = V_{IH} f = f_{MAX}(3)	COM'L	S L	150 140	215 185	140 130	200 175	130 125	190 165	mA
			IND	S L	— —	— —	140 130	225 195	— —	— —	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{\text{CE}}_R$ and $\overline{\text{CE}}_L$ = V_{IH} $\overline{\text{SEM}}_R$ = $\overline{\text{SEM}}_L$ = V_{IH} f = f_{MAX}(3)	COM'L	S L	25 20	35 30	20 15	30 25	16 13	30 25	mA
			MIL & IND	S L	— —	— —	20 15	45 40	— —	— —	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{\text{CE}}_{"A"}$ = V_{IL} and $\overline{\text{CE}}_{"B"}$ = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(3) $\overline{\text{SEM}}_R$ = $\overline{\text{SEM}}_L$ = V_{IH}	COM'L	S L	85 80	120 110	80 75	110 100	75 72	110 95	mA
			MIL & IND	S L	— —	— —	80 75	130 115	— —	— —	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{\text{CE}}_L$ and $\overline{\text{CE}}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0(4) $\overline{\text{SEM}}_R$ = $\overline{\text{SEM}}_L$ ≥ V_{DD} - 0.2V	COM'L	S L	1.0 0.2	5 2.5	1.0 0.2	5 2.5	1.0 0.2	5 2.5	mA
			MIL & IND	S L	— —	— —	1.0 0.2	15 5	— —	— —	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{\text{CE}}_{"A"}$ ≤ 0.2V and $\overline{\text{CE}}_{"B"}$ ≥ V_{DD} - 0.2V(5) $\overline{\text{SEM}}_R$ = $\overline{\text{SEM}}_L$ ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled, f = f_{MAX}(3)	COM'L	S L	85 80	125 105	80 75	115 100	75 70	105 90	mA
			MIL & IND	S L	— —	— —	80 75	130 115	— —	— —	

5624 tbl 09

NOTES:

1. 'X' in part number indicates power rating (S or L)
2. V_{DD} = 3.3V, T_A = +25°C, and are not production tested. $I_{DD\ DC}$ = 115mA (typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

5624 tbl 10

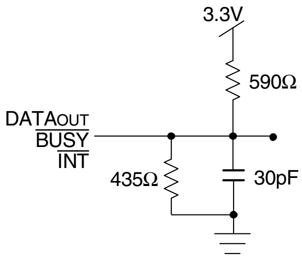
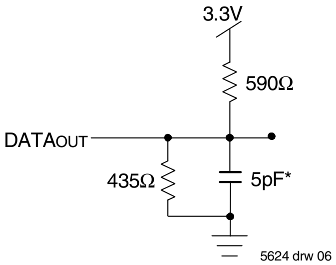


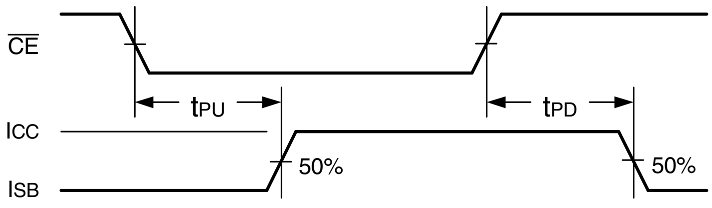
Figure 1. AC Output Test Load



5624 drw 06

Figure 2. Output Test Load (For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig.

Timing of Power-Up Power-Down



5624 drw 07

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V25/24(1) (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V24L15 Ind Only		70V25/24X15 Com'l Only		70V25/24X20 Com'l & Ind		70V25X25 Com'l & Ind		70V24X25 Com'l Only		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$, Outputs Open $\overline{SEM} = V_{IH}$ $f = f_{MAX}$(3)	COM'L	S L	— —	— —	150 140	215 185	140 130	200 175	130 125	190 165	130 125	190 165	mA
			IND	S L	— 140	— 205	— —	— —	140 130	225 195	— 125	— 180	— —	— —	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R$ and $\overline{CE}_L = V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$ $f = f_{MAX}$(3)	COM'L	S L	— —	— —	25 20	35 30	20 15	30 25	16 13	30 25	16 13	30 25	mA
			MIL & IND	S L	— 20	— 45	— —	— —	20 15	45 40	— 13	— 40	— —	— —	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"} = V_{IL}$ and $\overline{CE}_{"B"} = V_{IH}$(5) Active Port Outputs Open, $f=f_{MAX}$(3) $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$	COM'L	S L	— —	— —	85 80	120 110	80 75	110 100	75 72	110 95	75 72	110 95	mA
			MIL & IND	S L	— 80	— 125	— —	— —	80 75	130 115	— 72	— 110	— —	— —	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$(4) $\overline{SEM}_R = \overline{SEM}_L \geq V_{DD} - 0.2V$	COM'L	S L	— —	— —	1.0 0.2	5 2.5	1.0 0.2	5 2.5	1.0 0.2	5 2.5	1.0 0.2	5 2.5	mA
			MIL & IND	S L	— 0.2	— 5	— —	— —	1.0 0.2	15 5	— 0.2	— 5	— —	— —	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"} \leq 0.2V$ and $\overline{CE}_{"B"} \geq V_{DD} - 0.2V$(5) $\overline{SEM}_R = \overline{SEM}_L \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Open, $f = f_{MAX}$(3)	COM'L	S L	— —	— —	85 80	125 105	80 75	115 100	75 70	105 90	75 70	105 90	mA
			MIL & IND	S L	— 80	— 120	— —	— —	80 75	130 115	— 70	— 105	— —	— —	

5624 tbl 09c

Symbol	Parameter	Test Condition	Version		70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$, Outputs Open $\overline{SEM} = V_{IH}$ $f = f_{MAX}$(3)	COM'L	S L	120 115	180 155	120 115	180 155	mA
			IND	S L	— —	— —	— —	— —	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R$ and $\overline{CE}_L = V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$ $f = f_{MAX}$(3)	COM'L	S L	13 11	25 20	13 11	25 20	mA
			MIL & IND	S L	— —	— —	— —	— —	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"} = V_{IL}$ and $\overline{CE}_{"B"} = V_{IH}$(5) Active Port Outputs Open, $f=f_{MAX}$(3) $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$	COM'L	S L	70 65	100 90	70 65	100 90	mA
			MIL & IND	S L	— —	— —	— —	— —	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$(4) $\overline{SEM}_R = \overline{SEM}_L \geq V_{DD} - 0.2V$	COM'L	S L	1.0 0.2	5 2.5	1.0 0.2	5 2.5	mA
			MIL & IND	S L	— —	— —	— —	— —	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"} \leq 0.2V$ and $\overline{CE}_{"B"} \geq V_{DD}- 0.2V$(5) $\overline{SEM}_R = \overline{SEM}_L \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Open, $f = f_{MAX}$(3)	COM'L	S L	65 60	100 85	65 60	100 85	mA
			MIL & IND	S L	— —	— —	— —	— —	

5624 tbl 09b

NOTES:

1. 'X' in part number indicates power rating (S or L)
2. V_{DD} = 3.3V, T_A = +25°C, and are not production tested. $I_{DD\ DC}$ = 115mA (typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using “AC Test Conditions” of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

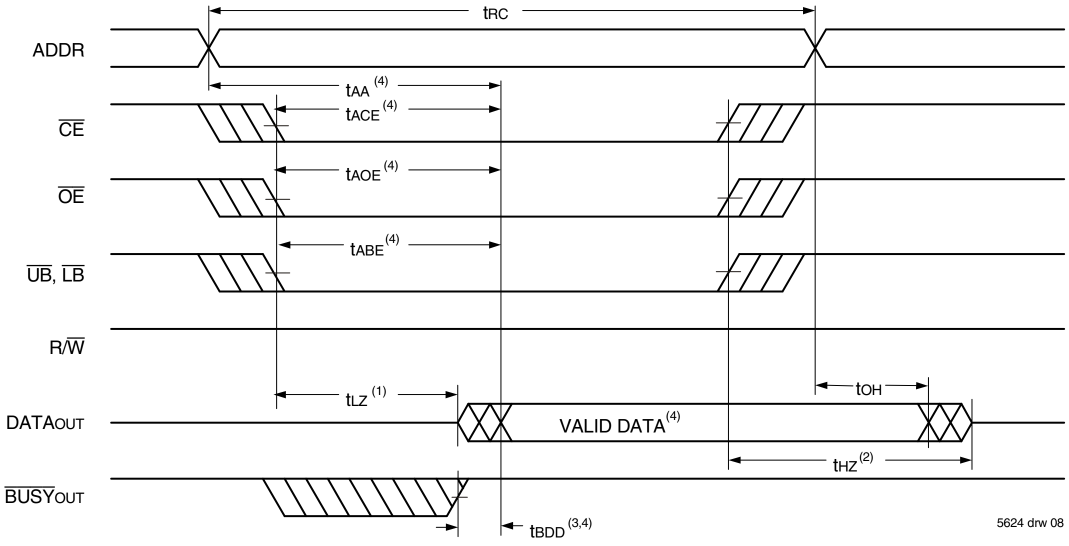
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V35/34(4)

Symbol	Parameter	70V35/34X15 Com'l Only		70V35/34X20 Com'l & Ind		70V35/34X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time(3)	—	15	—	20	—	25	ns
t_{ABE}	Byte Enable Access Time(3)	—	15	—	20	—	25	ns
t_{AOE}	Output Enable Access Time(3)	—	10	—	12	—	13	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	ns
t_{PU}	Chip Enable to Power Up Time(1,2)	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(1,2)	—	15	—	20	—	25	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	ns
t_{SAA}	Semaphore Address Access(3)	—	15	—	20	—	25	ns

5624 tbl 11

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ & $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}.
4. 'X' in part number indicates power rating (S or L).

Waveform of Read Cycles(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first, $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. t_{BDD} delay is required only in case where opposite port is completing a write operation to the same address location for simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{ABE}, t_{AOE}, t_{ACE}, t_{AA} or t_{BDD}.
5. $\overline{SEM}$ = V_{IH}.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V25/24[4]

Symbol	Parameter	70V25/24X15 Com'l & Ind		70V25/24X20 Com'l & Ind		70V25X25 Com'l & Ind		70V24X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	25	ns
t_{ACE}	Chip Enable Access Time(3)	—	15	—	20	—	25	—	25	ns
t_{ABE}	Byte Enable Access Time(3)	—	15	—	20	—	25	—	25	ns
t_{AOE}	Output Enable Access Time(3)	—	10	—	12	—	13	—	13	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	—	15	ns
t_{PU}	Chip Enable to Power Up Time(1,2)	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(1,2)	—	15	—	20	—	25	—	25	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	10	—	ns
t_{SAA}	Semaphore Address Access(3)	—	15	—	20	—	25	—	25	ns

5624 tbl 11d

Symbol	Parameter	70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	35	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time(3)	—	35	—	55	ns
t_{ABE}	Byte Enable Access Time(3)	—	35	—	55	ns
t_{AOE}	Output Enable Access Time(3)	—	20	—	30	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	15	—	25	ns
t_{PU}	Chip Enable to Power Up Time(1,2)	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(1,2)	—	35	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
t_{SAA}	Semaphore Address Access(3)	—	35	—	55	ns

5624 tbl 11c

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ & $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}.
4. 'X' in part number indicates power rating (S or L).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage for 70V35/34 (5)

Symbol	Parameter	70V35/34X15 Com'l Only		70V35/34X20 Com'l & Ind		70V35/34X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	15	—	15	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	10	—	12	—	15	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

5624 tbl 12

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access SRAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ & $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the SRAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part number indicates power rating (S or L).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage for 70V25/24 (5)

Symbol	Parameter	70V25/24X15 Com'l & Ind		70V25/24X20 Com'l & Ind		70V25X25 Com'l & Ind		70V24X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15	—	20	—	25	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	12	—	15	—	20	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	20	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	15	—	15	—	15	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	—	15	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	10	—	12	—	15	—	15	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	5	—	ns

5624 tbl 12c

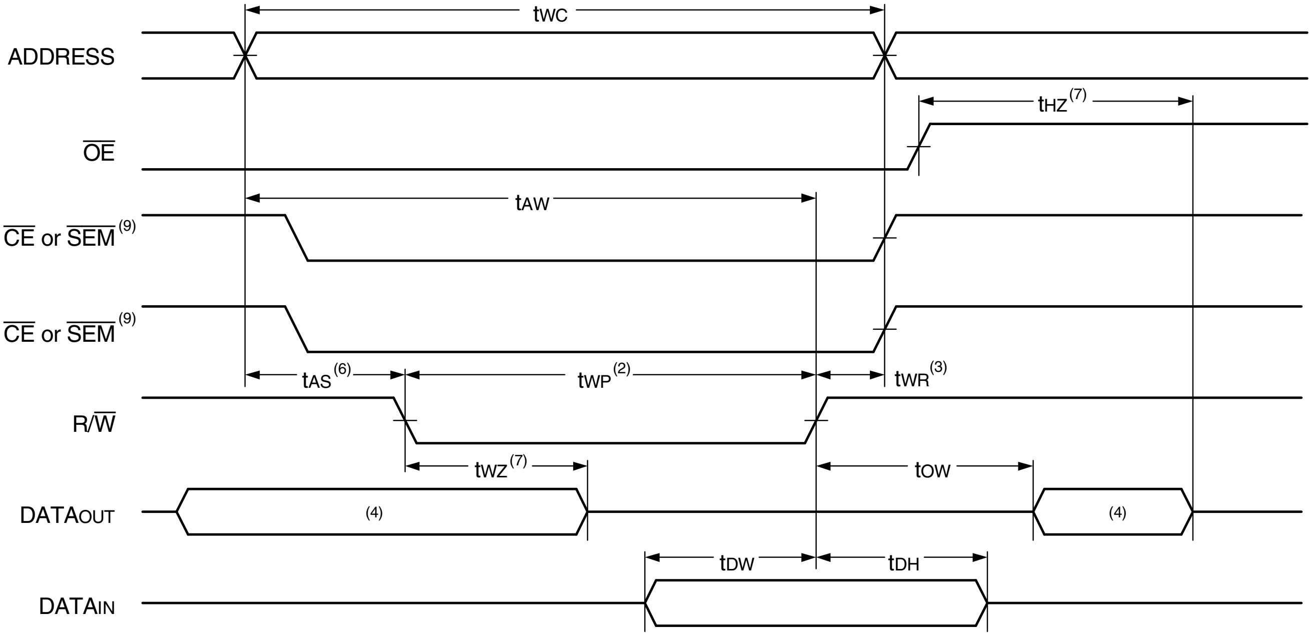
Symbol	Parameter	70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write(3)	30	—	45	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	ns
t_{AS}	Address Set-up Time(3)	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	30	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	15	—	25	ns
t_{DH}	Data Hold Time(4)	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1,2)	—	15	—	25	ns
t_{OW}	Output Active from End-of-Write(1,2,4)	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

5624 tbl 12b

NOTES:

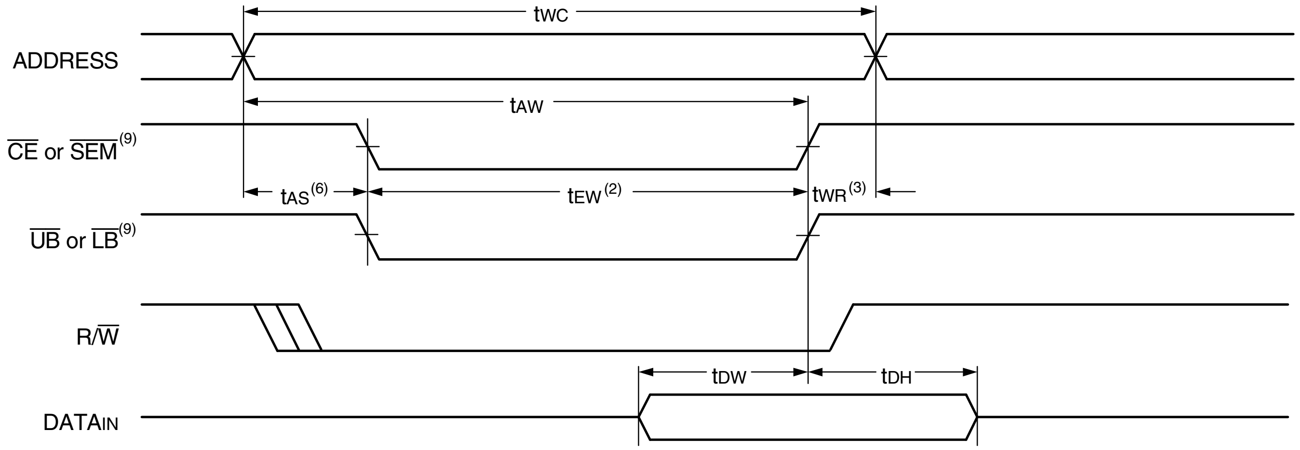
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access SRAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ & $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the SRAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part number indicates power rating (S or L).

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



5624 drw 09

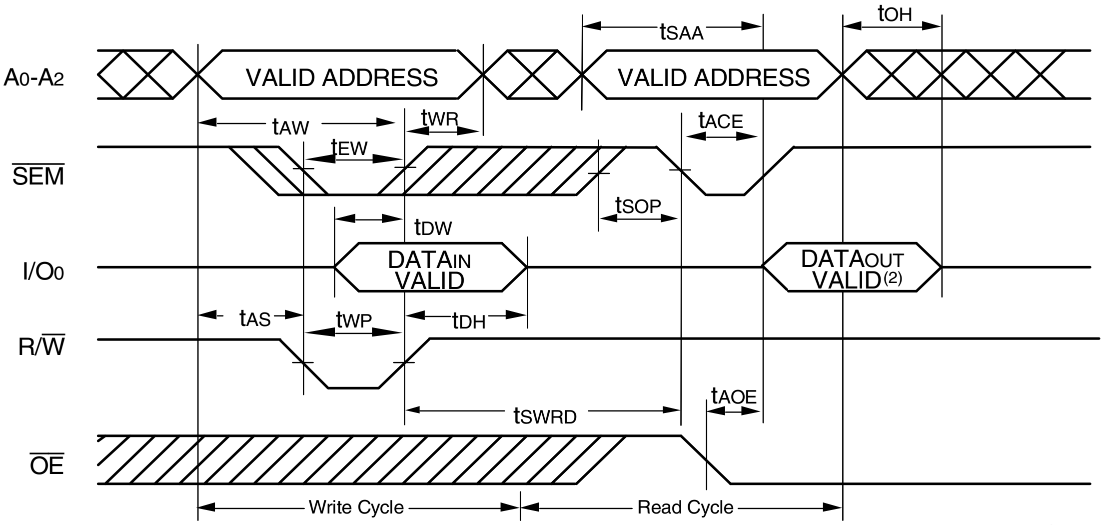
Timing Waveform of Write Cycle No. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ Controlled Timing(1,5)



5624 drw 10

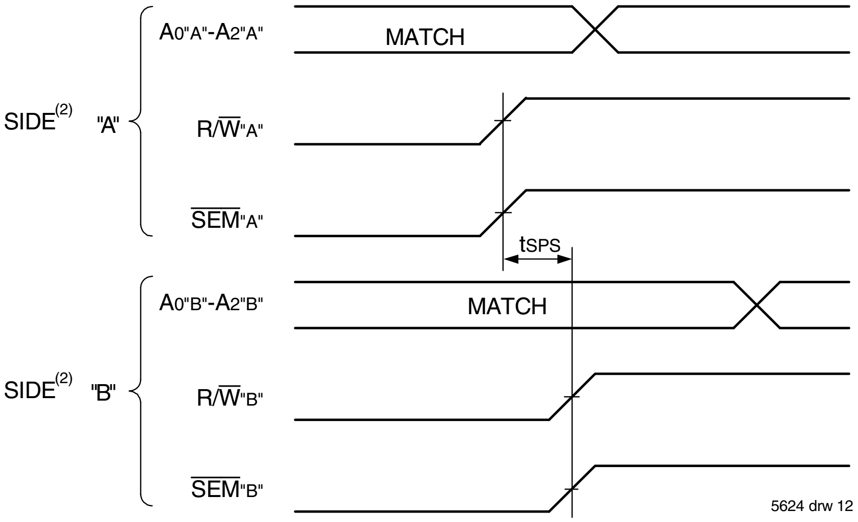
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ & $\overline{LB}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a LOW $\overline{UB}$ or $\overline{LB}$ and a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end-of-write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition the outputs remain in the HIGH-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$, or $\overline{UB}$ or $\overline{LB}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access SRAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, and $\overline{SEM}$ = V_{IH}. To access Semaphore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ and $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}. t_{EW} must be met for either condition.

Timing Waveform of Semaphore Read after Write Timing, Either Side[1]



NOTES:
1. $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle).
2. "DATAOUT VALID" represents all I/O's (I/O0-I/O17 for IDT70V35/34) and (I/O0-I/O15 for IDT70V25/24) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention(1,3,4)



NOTES:
1. DOR = DOL = VIL, $\overline{CE}$R = $\overline{CE}$L = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH.
2. All timing is the same for left and right port. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going HIGH to R/$\overline{W}$"B" or $\overline{SEM}$"B" going HIGH.
4. If tSPS is not satisfied, there is no guarantee which side will obtain the semaphore flag.

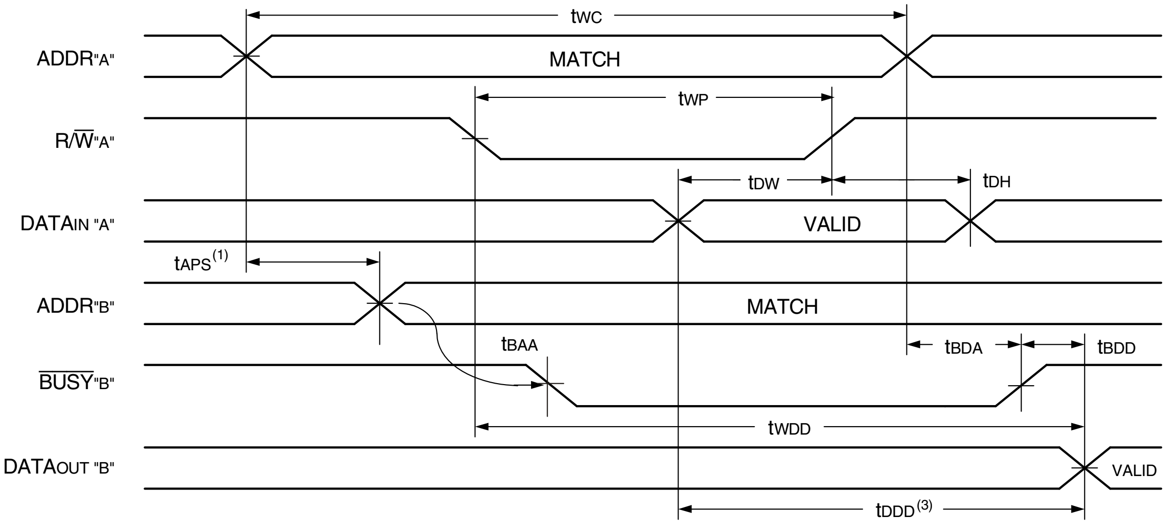
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V35/34(6)

Symbol	Parameter	70V35/34X15 Com'l Ony Min.	70V35/34X15 Com'l Ony Max.	70V35/34X20 Com'l & Ind Min.	70V35/34X20 Com'l & Ind Max.	70V35/34X25 Com'l Only Min.	70V35/34X25 Com'l Only Max.	Unit
$\overline{\text{BUSY}}$ TIMING (M/$\overline{\text{S}}$ = V_{IH})								
t_{BAA}	$\overline{\text{BUSY}}$ Access Time from Address Match	—	15	—	20	—	20	ns
t_{BDA}	$\overline{\text{BUSY}}$ Disable Time from Address Not Matched	—	15	—	20	—	20	ns
t_{BAC}	$\overline{\text{BUSY}}$ Access Time from Chip Enable LOW	—	15	—	20	—	20	ns
t_{BDC}	$\overline{\text{BUSY}}$ Disable Time from Chip Enable HIGH	—	15	—	17	—	17	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
t_{BDD}	$\overline{\text{BUSY}}$ Disable to Valid Data(3)	—	18	—	30	—	30	ns
t_{WH}	Write Hold After $\overline{\text{BUSY}}$(5)	12	—	15	—	17	—	ns
$\overline{\text{BUSY}}$ TIMING (M/$\overline{\text{S}}$ = V_{IL})								
t_{WB}	$\overline{\text{BUSY}}$ Input to Write(4)	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{\text{BUSY}}$(5)	12	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING								
t_{WDD}	Write Pulse to Data Delay(1)	—	30	—	45	—	50	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	25	—	35	—	35	ns

5624 tbl 13

NOTES:
1. Port-to-port delay through SRAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF WRITE PORT-TO-PORT READ AND $\overline{\text{BUSY}}$ (M/$\overline{\text{S}}$ = V_{IH})".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} – t_{WP} (actual) or t_{DDD} – t_{DW} (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. 'X' in part number indicates power rating (S or L).

Timing Waveform of Write Port-to-Port Read and $\overline{\text{BUSY}}$(2,4,5) (M/$\overline{\text{S}}$ = V_{IH})



5624 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. t_{APS} is ignored for M/$\overline{\text{S}}$ = V_{IL} (slave).
2. $\overline{\text{CE}}_L$ = $\overline{\text{CE}}_R$ = V_{IL}.
3. $\overline{\text{OE}}$ = V_{IL} for the reading port.
4. If M/$\overline{\text{S}}$ = V_{IL} (slave), $\overline{\text{BUSY}}$ is an input. Then for this example $\overline{\text{BUSY}}_{“A”}$ = V_{IH} and $\overline{\text{BUSY}}_{“B”}$ input is shown above.
5. All timing is the same for both left and right ports. Port “A” may be either the left or right port. Port “B ” is the port opposite from port “A”.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V25/24(6)

Symbol	Parameter	70V25/24X15 Com'l & Ind		70V25/24X20 Com'l & Ind		70V25X25 Com'l & Ind		70V24X25 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/S = V_{IH})										
t_{BAA}	BUSY Access Time from Address Match	—	15	—	20	—	20	—	20	ns
t_{BDA}	BUSY Disable Time from Address Not Matched	—	15	—	20	—	20	—	20	ns
t_{BAC}	BUSY Access Time from Chip Enable LOW	—	15	—	20	—	20	—	20	ns
t_{BDC}	BUSY Disable Time from Chip Enable HIGH	—	15	—	17	—	17	—	17	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	5	—	ns
t_{BDD}	BUSY Disable to Valid Data(3)	—	18	—	30	—	30	—	30	ns
t_{WH}	Write Hold After BUSY(5)	12	—	15	—	17	—	17	—	ns
BUSY TIMING (M/S = V_{IL})										
t_{WB}	BUSY Input to Write(4)	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After BUSY(5)	12	—	15	—	17	—	17	—	ns
PORT-TO-PORT DELAY TIMING										
t_{WDD}	Write Pulse to Data Delay(1)	—	30	—	45	—	50	—	50	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	25	—	35	—	35	—	35	ns

5624 tbl 13c

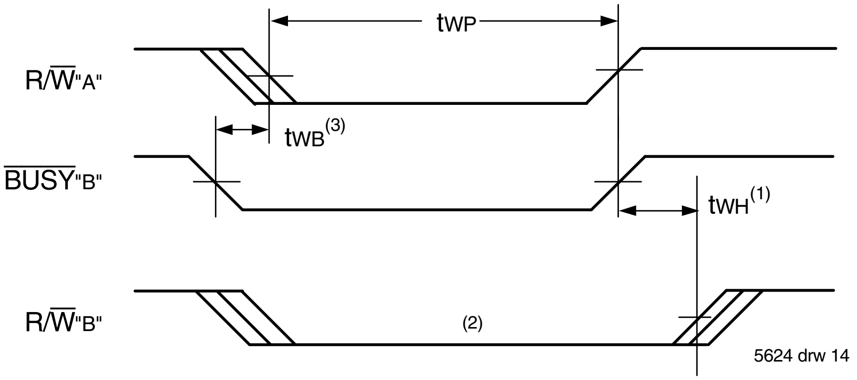
Symbol	Parameter	70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (M/S = V_{IH})						
t_{BAA}	BUSY Access Time from Address Match	—	20	—	45	ns
t_{BDA}	BUSY Disable Time from Address Not Matched	—	20	—	40	ns
t_{BAC}	BUSY Access Time from Chip Enable LOW	—	20	—	40	ns
t_{BDC}	BUSY Disable Time from Chip Enable HIGH	—	20	—	35	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
t_{BDD}	BUSY Disable to Valid Data(3)	—	35	—	40	ns
t_{WH}	Write Hold After BUSY(5)	25	—	25	—	ns
BUSY TIMING (M/S = V_{IL})						
t_{WB}	BUSY Input to Write(4)	0	—	0	—	ns
t_{WH}	Write Hold After BUSY(5)	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
t_{WDD}	Write Pulse to Data Delay(1)	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	45	—	65	ns

5624 tbl 13b

NOTES:

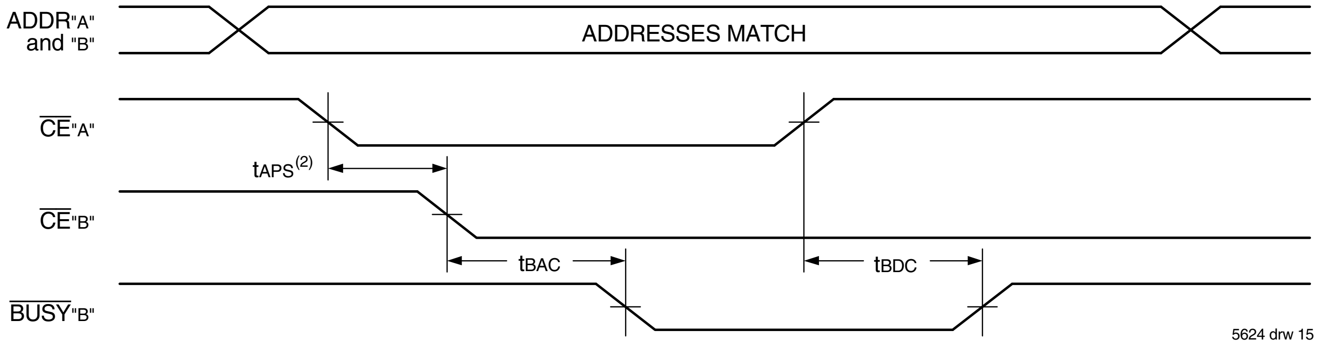
1. Port-to-port delay through SRAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF WRITE PORT-TO-PORT READ AND BUSY (M/S = V_{IH})".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. 'X' in part number indicates power rating (S or L).

Timing Waveform of Write with $\overline{\text{BUSY}}$



NOTES:
1. tWH must be met for both master $\overline{\text{BUSY}}$ input (slave) and output (master).
2. $\overline{\text{BUSY}}$ is asserted on port "B" blocking R/$\overline{\text{W}}$"B", until $\overline{\text{BUSY}}$"B" goes HIGH.
3. tWB is only for the slave version.

Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by $\overline{\text{CE}}$ Timing(1) (M/$\overline{\text{S}}$ = VIH)



Waveform of $\overline{\text{BUSY}}$ Arbitration Cycle Controlled by Address Match Timing(1) (M/$\overline{\text{S}}$ = VIH)

NOTES:
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
2. If tAPS is not satisfied, the $\overline{\text{BUSY}}$ signal will be asserted on one side or another but there is no guarantee on which side $\overline{\text{BUSY}}$ will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V35/34[(1)]

		70V35/34X15 Com'l Only		70V35/34X20 Com'l & Ind		70V35/34X25 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	15	—	20	—	20	ns
t_{INR}	Interrupt Reset Time	—	15	—	20	—	20	ns

5624 tbl 14

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range for 70V25/24[(1)]

		70V25/24X15 Com'l & Ind		70V25/24X20 Com'l & Ind		70V25X25 Com'l & Ind		70V24X25 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING										
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	15	—	20	—	20	—	20	ns
t_{INR}	Interrupt Reset Time	—	15	—	20	—	20	—	20	ns

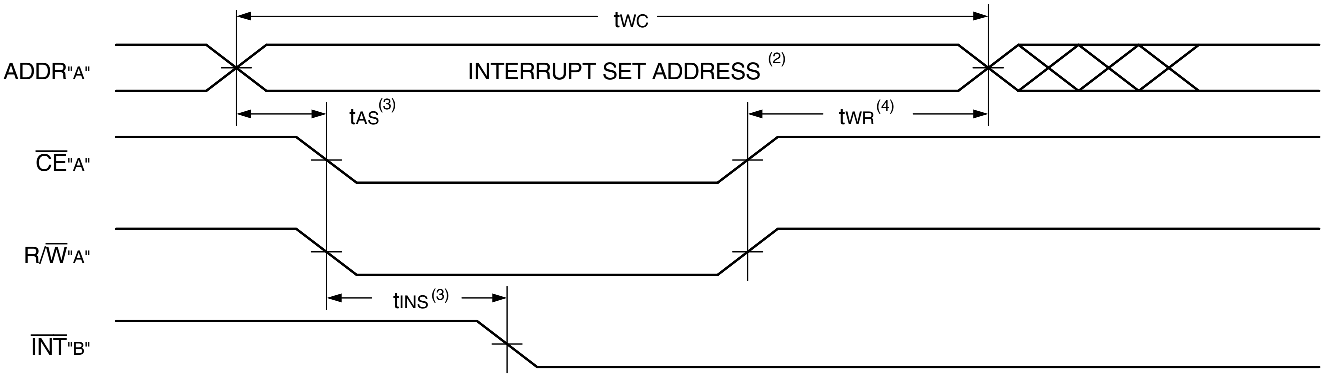
5624 tbl 14c

		70V25/24X35 Com'l Only		70V25/24X55 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING						
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	40	ns
t_{INR}	Interrupt Reset Time	—	25	—	40	ns

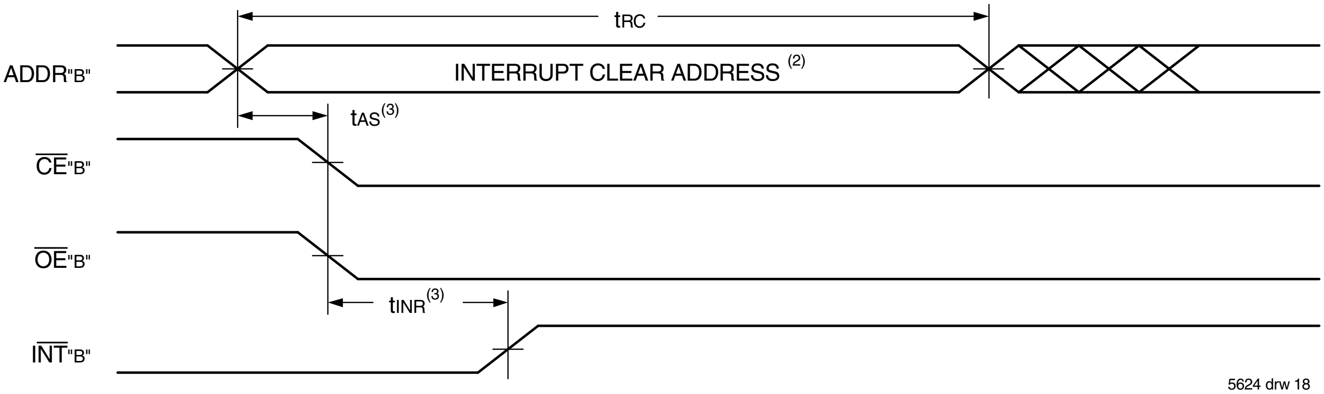
5624 tbl 14b

NOTES:
1. 'X' in part number indicates power rating (S or L).

Waveform of Interrupt Timing(1)



5624 drw 17



5624 drw 18

NOTES:

1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
2. See Interrupt Flag Truth Table III.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

Truth Table III — Interrupt Flag(1)

Left Port					Right Port					Function
R/$\overline{\text{W}}_L$	$\overline{\text{CE}}_L$	$\overline{\text{OE}}_L$	A_{12L}-A_{0L}(4)	$\overline{\text{INT}}_L$	R/$\overline{\text{W}}_R$	$\overline{\text{CE}}_R$	$\overline{\text{OE}}_R$	A_{12R}-A_{0R}(4)	$\overline{\text{INT}}_R$	
L	L	X	1FFF(4)	X	X	X	X	X	L(2)	Set Right $\overline{\text{INT}}_R$ Flag
X	X	X	X	X	X	L	L	1FFF(4)	H(3)	Reset Right $\overline{\text{INT}}_R$ Flag
X	X	X	X	L(3)	L	L	X	1FFE(4)	X	Set Left $\overline{\text{INT}}_L$ Flag
X	L	L	1FFE(4)	H(2)	X	X	X	X	X	Reset Left $\overline{\text{INT}}_L$ Flag

5624 tbl 15

NOTES:

1. Assumes $\overline{\text{BUSY}}_L$ = $\overline{\text{BUSY}}_R$ = V_{IH}.
2. If $\overline{\text{BUSY}}_L$ = V_{IL}, then no change.
3. If $\overline{\text{BUSY}}_R$ = V_{IL}, then no change.
4. A_{12} is a NC for IDT70V34 and for IDT70V24, therefore Interrupt Addresses are FFF and FFE.

Truth Table IV — Address $\overline{\text{BUSY}}$ Arbitration

Inputs			Outputs		Function
$\overline{\text{CE}}_L$	$\overline{\text{CE}}_R$	A_{12L}-A_{0L}(4) A_{12R}-A_{0R}	$\overline{\text{BUSY}}_L$(1)	$\overline{\text{BUSY}}_R$(1)	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	Note(2)	Note(2)	Write Inhibit(3)

5624 tbl 16

NOTES:

1. Pins $\overline{\text{BUSY}}_L$ and $\overline{\text{BUSY}}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{\text{BUSY}}$ outputs on the IDT70V35/34 (IDT70V25/24) are push pull, not open drain outputs. On slaves the $\overline{\text{BUSY}}$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. V_{IH} if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{\text{BUSY}}_L$ or $\overline{\text{BUSY}}_R$ = LOW will result. $\overline{\text{BUSY}}_L$ and $\overline{\text{BUSY}}_R$ outputs cannot be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{\text{BUSY}}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{\text{BUSY}}_R$ outputs are driving LOW regardless of actual logic level on the pin.
4. A_{12} is a NC for IDT70V34 and for IDT70V24. Address comparison will be for A_0 - A_{11}.

Truth Table V — Example of Semaphore Procurement Sequence(1,2,3)

Functions	D_0 - D_{17} Left(2)	D_0 - D_{17} Right(2)	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

5624 tbl 17

NOTES:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V35/34 (IDT70V25/24).
2. There are eight semaphore flags written to via I/O_0 and read from all I/O's (I/O_0-I/O_{17} for IDT70V35/34) and (I/O_0-I/O_{15} for IDT70V25/24). These eight semaphores are addressed by A_0-A_2.
3. $\overline{\text{CE}}$ = V_{IH}, $\overline{\text{SEM}}$ = V_{IL} to access the semaphores. Refer to the Semaphore Read/Write Control Truth Tables.

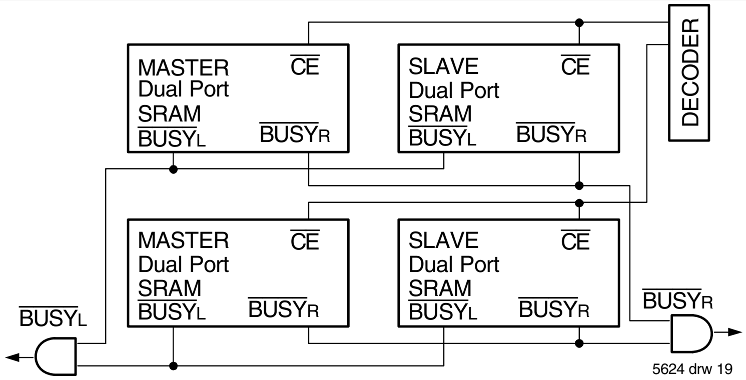


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V35/34 (IDT70V25/24) SRAMs.

Functional Description

The IDT70V35/34 (IDT70V25/24) provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V35/34 (IDT70V25/24) has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 1FFE (HEX) (FFE for IDT70V34 and IDT70V24), where a write is defined as the $\overline{CE}_R = R/\overline{W}_R = V_{IL}$ per Truth Table III. The left port clears the interrupt on the IDT70V35 and IDT70V25 by an address location 1FFE (FFE for IDT70V34 and IDT70V24) access when $\overline{CE}_L = \overline{OE}_L = V_{IL}$, $R/\overline{W}_L$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF for IDT70V35 and IDT70V25 (HEX) (FFF for IDT70V34 and IDT70V24) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF for IDT70V35 and IDT70V25 (FFF for IDT70V34 and IDT70V24). The message (16 bits) at 1FFE or 1FFF for IDT70V35 and IDT70V25 (FFE or FFF for IDT70V34 and IDT70V24) is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFE and 1FFF for IDT70V35 and IDT70V25 (FFE and FFF for IDT70V34 and IDT70V24) are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the SRAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the SRAM is "busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of $\overline{BUSY}$ logic is not desirable, the $\overline{BUSY}$ logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the IDT70V35/34 (IDT70V25/24) SRAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these SRAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array requires the use of an external AND gate.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70V35/34 (IDT70V25/24) SRAM array in width while using $\overline{BUSY}$ logic, one master part is used to decide which side of the SRAM array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the $\overline{BUSY}$ signal as a write inhibit signal. Thus on the IDT70V35/34 (IDT70V25/24) SRAM the $\overline{BUSY}$ pin is an output if the part is used as a master (M/$\overline{S}$ pin = V_{IH}), and the $\overline{BUSY}$ pin is an input if the part used as a slave (M/$\overline{S}$ pin = V_{IL}) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{BUSY}$ on one side of the array and another master indicating $\overline{BUSY}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{BUSY}$ arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{BUSY}$ flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT70V35/34 (IDT70V25/24) is an extremely fast Dual-Port 8/4K x 18 (8/4K x 16) CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port SRAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port SRAM or any other shared resource.

The Dual-Port SRAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be accessed at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port SRAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port SRAM enable, and SEM, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where $\overline{CE}$ and $\overline{SEM}$ are both HIGH.

Systems which can best use the IDT70V35/34 (IDT70V25/24) contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V35/34 (IDT70V25/24)'s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V35/34 (IDT70V25/24) does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port SRAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V35/34 (IDT70V25/24) in a separate memory space from the Dual-Port SRAM. This address space is accessed by placing a LOW input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 – A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table V). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch. The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V35/34 (IDT70V25/24)'s Dual-Port SRAM. Say the 8K x 18 SRAM was to be divided into two 4K x 18 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port SRAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port SRAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port SRAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

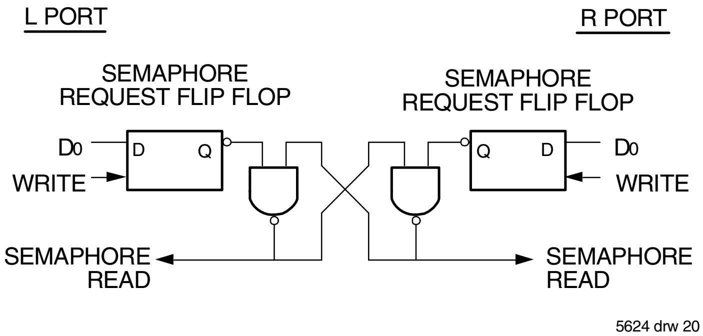
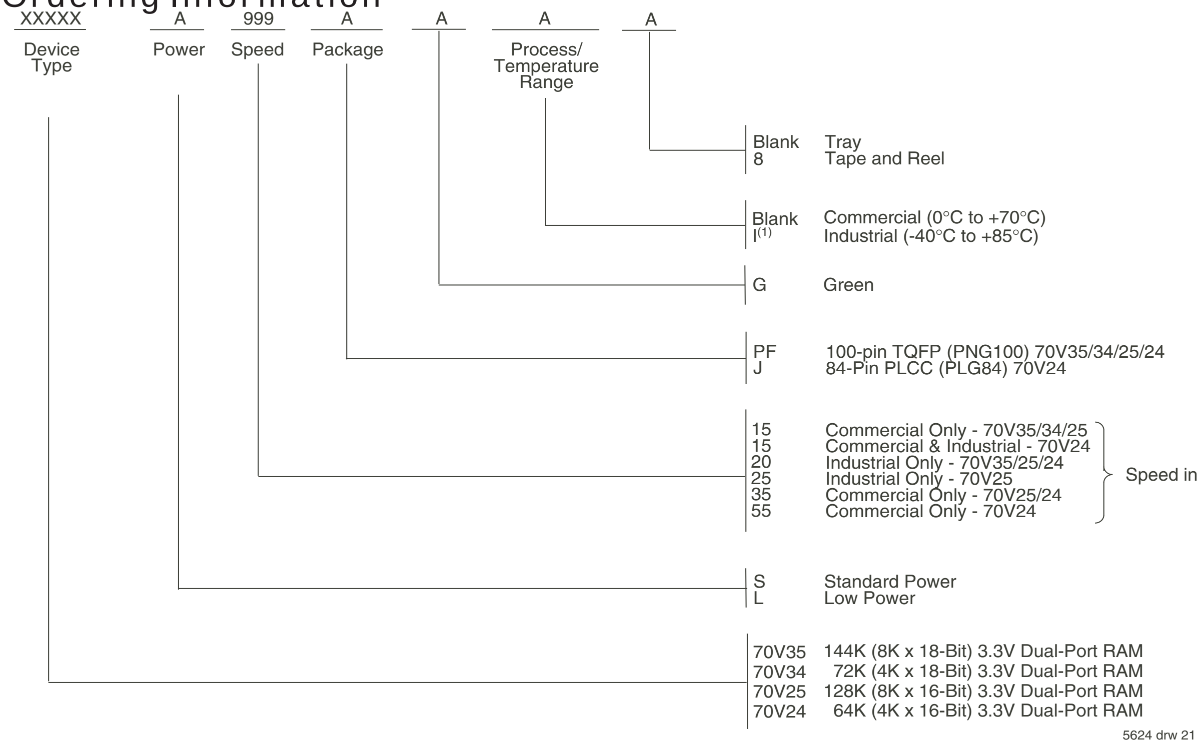


Figure 4. IDT70V35/34 (IDT70V25/24) Semaphore Logic

Ordering Information



Blank	Tray	
8	Tape and Reel	
Blank	Commercial (0°C to +70°C)	
I[1]	Industrial (-40°C to +85°C)	
G	Green	
PF	100-pin TQFP (PNG100) 70V35/34/25/24	
J	84-Pin PLCC (PLG84) 70V24	
15	Commercial Only - 70V35/34/25	Speed in Nanoseconds
15	Commercial & Industrial - 70V24	
20	Industrial Only - 70V35/25/24	
25	Industrial Only - 70V25	
35	Commercial Only - 70V25/24	
55	Commercial Only - 70V24	
S	Standard Power	
L	Low Power	
70V35	144K (8K x 18-Bit) 3.3V Dual-Port RAM	
70V34	72K (4K x 18-Bit) 3.3V Dual-Port RAM	
70V25	128K (8K x 16-Bit) 3.3V Dual-Port RAM	
70V24	64K (4K x 16-Bit) 3.3V Dual-Port RAM	

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NOTES:

1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.

LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02

Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	70V35L15PFG	PNG100	TQFP	C
	70V35L15PFG8	PNG100	TQFP	C
20	70V35L20PFGI	PNG100	TQFP	I
	70V35L20PFGI8	PNG100	TQFP	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	70V34L15PFG	PNG100	TQFP	C
	70V34L15PFG8	PNG100	TQFP	C

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	70V25L15PFG	PNG100	TQFP	C
	70V25L15PFG8	PNG100	TQFP	C
20	70V25L20PFGI	PNG100	TQFP	I
	70V25L20PFGI8	PNG100	TQFP	I
25	70V25L25PFGI	PNG100	TQFP	I
	70V25L25PFGI8	PNG100	TQFP	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
25	70V25S25PFGI	PNG100	TQFP	I
	70V25S25PFGI8	PNG100	TQFP	I
35	70V25S35PFG	PNG100	TQFP	C

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	70V24L15JG	PLG84	PLCC	C
	70V24L15JG8	PLG84	PLCC	C
	70V24L15PFG	PNG100	TQFP	C
	70V24L15PFG8	PNG100	TQFP	C
	70V24L15PFGI	PNG100	TQFP	I
	70V24L15PFGI8	PNG100	TQFP	I
20	70V24L20JGI	PLG84	PLCC	I
	70V24L20JGI8	PLG84	PLCC	I
	70V24L20PFGI	PNG100	TQFP	I
	70V24L20PFGI8	PNG100	TQFP	I
35	70V24L35PFG	PNG100	TQFP	C
	70V24L35PFG8	PNG100	TQFP	C

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
55	70V24S55PFG	PNG100	TQFP	C
	70V24S55PFG8	PNG100	TQFP	C

Datasheet Document History

06/08/00: Initial Public Offering
08/09/01: Page 1 Corrected I/O numbering
Page 5-7, 10 & 12 Removed Industrial temperature range offering for 25ns from DC & AC Electrical Characteristics
Page 17 Removed Industrial temperature range offering for 25ns speed from the ordering information
Added Industrial temperature offering footnote
07/02/02: Page 2 Added date revision for pin configuration
Added 70V34 to datasheet (4K x 18)
06/22/04: Consolidated 70V25/24 datasheets (8/4K x 16) into 70V35/34 (8/4K x 18) datasheet
Removed Preliminary status from datasheet
Page 2 & 3 Changed naming convention from V_{CC} to V_{DD} and from GND to V_{SS} for PN100 packages
Page 7 Updated Conditions in Capacitance table
Page 7 Added Junction Temperature to Absolute Maximum Ratings table
Page 9, 11, 13, 17 &, 19 Added DC and AC Electrical Characteristics tables for 70V25/24 data
Page 21 & 22 Changed Interrupt flag table, footnotes and Interrupts text to reflect 70V25/24 data
Page 1 & 15 Replaced old ® logo with new TM logo
10/28/04: Page 25 Added stepping indicator to ordering information
04/05/05: Page 1 Added green availability to features
Page 25 Added green indicator to ordering information
10/23/08: Page 25 Removed "IDT" from orderable part number
08/26/15: Page 1 Updated the 70V25 & 70V24 high speed access offerings in Features, removed 70V24X25 industrial temp
Page 2 Removed the IDT in reference to fabrication
Pages 2, 3, 4 & 5 Removed the date from the PN100, G84 & J84 pin configurations
Page 6 Updated footnotes 2 & 3 for Truth Table I: Non-Contention Read/Write Control
Pages 9,11,13,17 & 19 Removed 25ns Industrial temp offering from the DC Chars and AC Chars tables for the 70V24
Page 25 Added Tape & Reel indicator and removed the stepping indicator from the ordering information
Page 25 The package code for PN100-1 changed to PN100, G84-3 changed to G84 and J84-1 changed to J84 respectively in the ordering information to match the standard package codes
11/13/17: Page 1, 2 & 4 G84 is no longer offered and it has been removed completely from the entire datasheet and specifically from the features, description and pin configuration
Page 8 Added 70V24L15 Ind Only column and added the Typ. & Max data to this Ind speed grade offering only in the 70V25/24 DC Electrical Characteristics Table
Page 8,10,12,16 & 18 Specifically updated all of the AC Electrical Characteristics Tables pertaining to 70V25/24X15 speed grade which includes both the Com'l and Ind temps for the READ CYCLE, WRITE CYCLE, and TIMING FOR $\overline{\text{BUSY}}$, PORT-TO-PORT DELAY & INTERRUPT respectively
11/13/17: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018
10/23/19: Pages 1 & 24 Updated speed grade offerings
Pages 2,3 & 4 Rotated PNG100 TQFP and PLG84 PLCC pin configurations to accurately reflect pin 1 orientation
Page 24 Added Orderable Part Information table

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