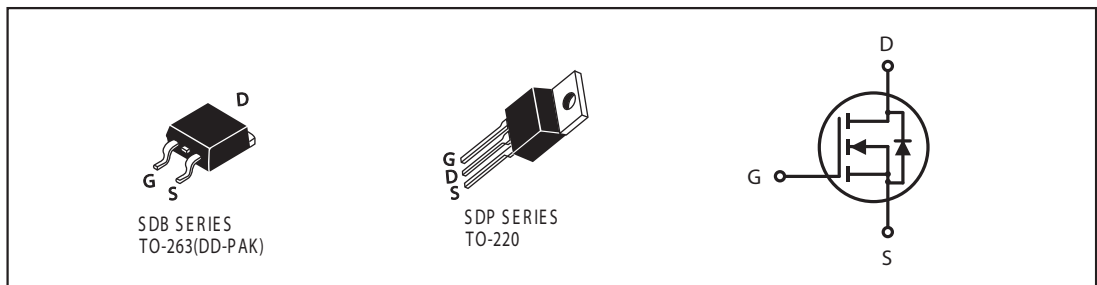


## N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(on)</sub> (mΩ) TYP
30V	55A	12.5 @ V <sub>GS</sub> = 10V
		20 @ V <sub>GS</sub> = 4.5V

## FEATURES

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- TO-220 & TO-263 package.

ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous @ T <sub>J</sub> =125°C -Pulsed <sup>a</sup>	I <sub>D</sub>	55	A
	I <sub>DM</sub>	140	A
Drain-Source Diode Forward Current	I <sub>S</sub>	55	A
Maximum Power Dissipation @ T <sub>C</sub> =25°C Derate above 25°C	P <sub>D</sub>	75	W
		0.5	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to 175	°C

## THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			10	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±16V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	1.5	3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =27A		12.5	14	m ohm
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =22A		20	23	m ohm
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V	60			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =27A		32		S
<b>DYNAMIC CHARACTERISTICS<sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V f=1.0MHz		930		pF
Output Capacitance	C <sub>OSS</sub>			340		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			120		pF
<b>SWITCHING CHARACTERISTICS<sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V, R <sub>GEN</sub> =60 ohm		17	16	ns
Rise Time	t <sub>r</sub>			23	250	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			37	90	ns
Fall Time	t <sub>f</sub>			20	200	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =27.5A, V <sub>GS</sub> =10V		26.1	35	nC
		V <sub>DS</sub> =15V, I <sub>D</sub> =27.5A, V <sub>GS</sub> =4.5V		13.7	16.5	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =27.5A, V <sub>GS</sub> =10V		5.4		nC
Gate-Drain Charge	Q <sub>gd</sub>			4.6		nC

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## ELECTRICAL CHARACTERISTICS ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS <sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{V}, I_s = 26\text{A}$		0.9	1.3	V

### Notes

- a. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

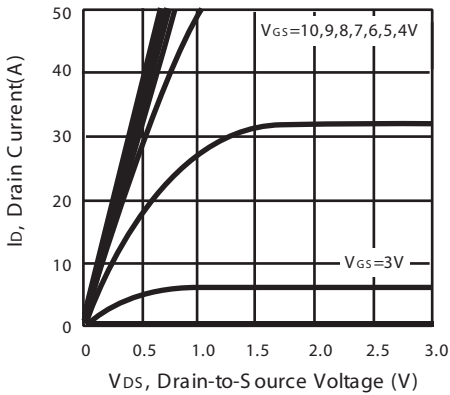


Figure 1. Output Characteristics

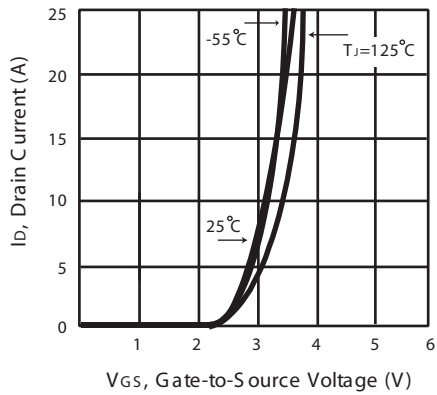


Figure 2. Transfer Characteristics

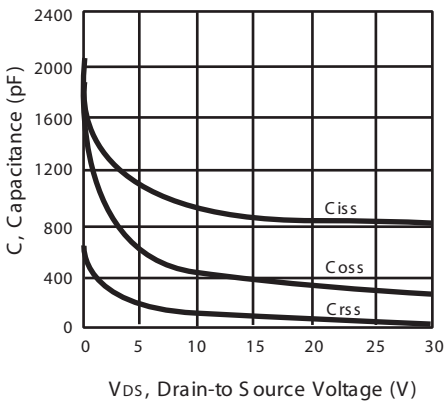


Figure 3. Capacitance

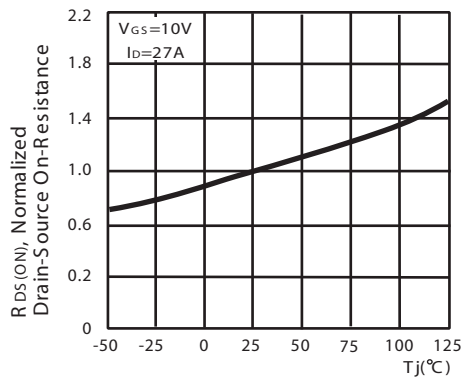


Figure 4. On-Resistance Variation with Temperature

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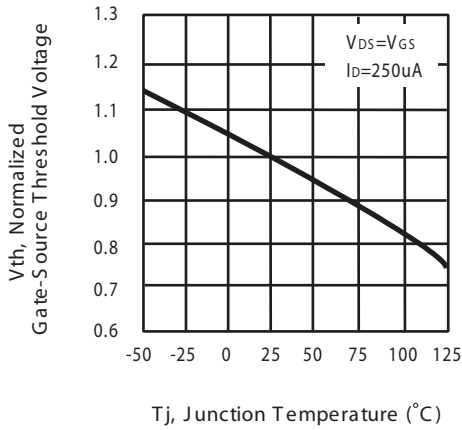


Figure 5. Gate Threshold Variation with Temperature

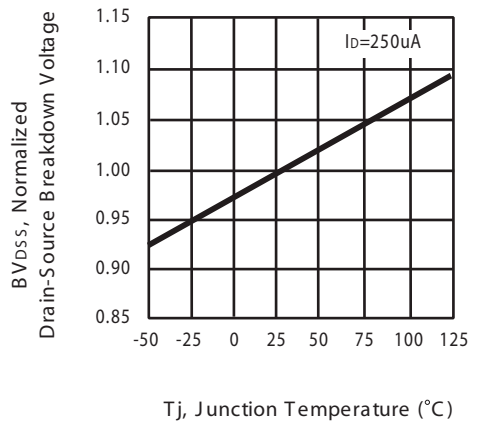


Figure 6. Breakdown Voltage Variation with Temperature

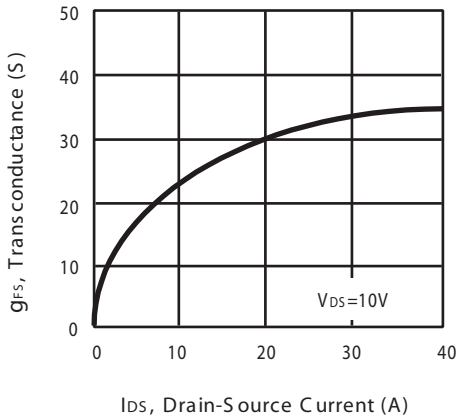


Figure 7. Transconductance Variation with Drain Current

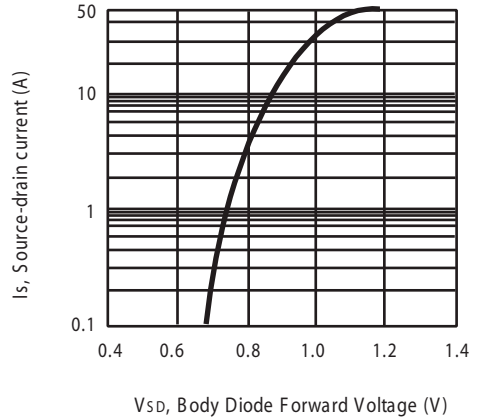


Figure 8. Body Diode Forward Voltage Variation with Source Current

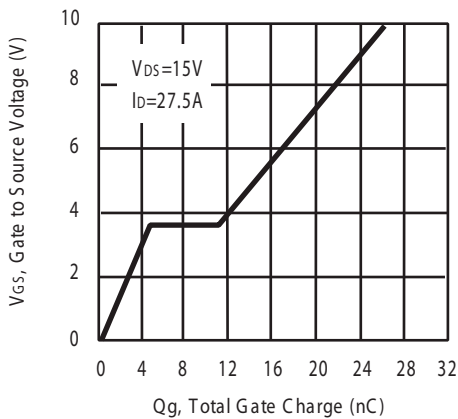


Figure 9. Gate Charge

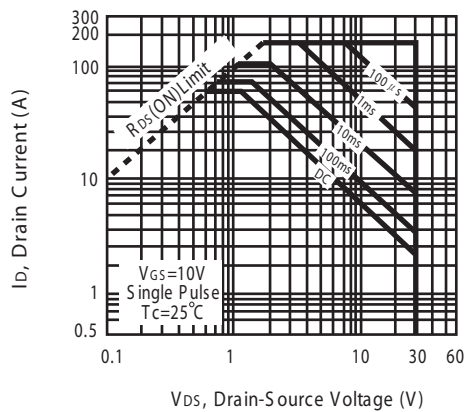


Figure 10. Maximum Safe Operating Area

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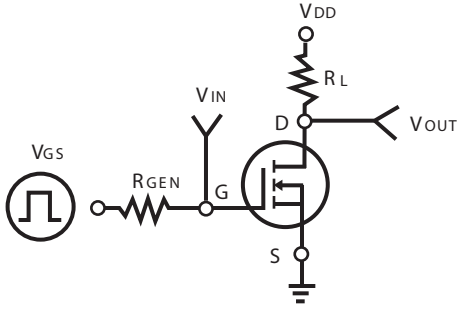


Figure 11. S switching Test Circuit

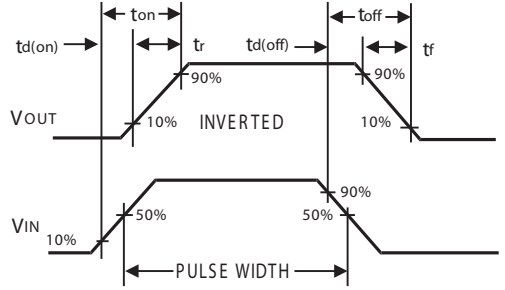


Figure 12. S switching Waveforms

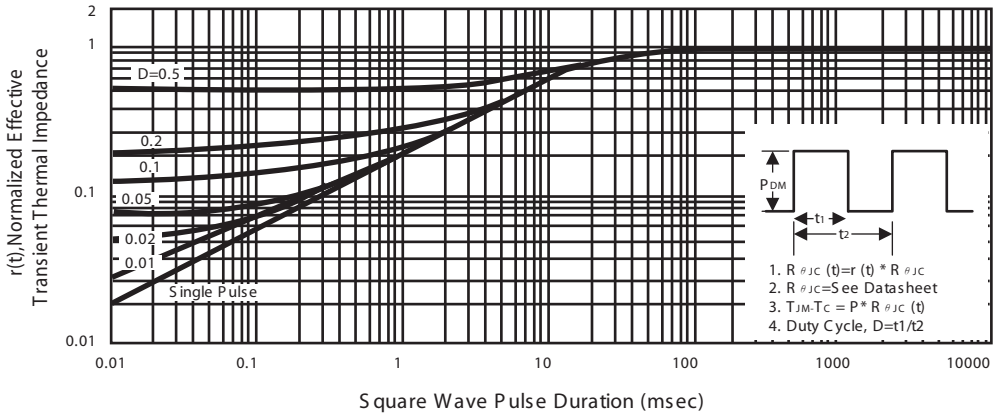


Figure 13. Normalized Thermal Transient Impedance Curve