MAX71315C/MAX71314C/ MAX71335C/MAX71334C

ZON M3S/M3SL and P3S/P3SL Single-Phase/Polyphase Electricity Meter SoC

General Description

The ZON™ M3S/M3SL and P3S/P3SL (MAX71315C/MAX71314C and MAX71335C/MAX71334C) integrate dual 32-bit processors and security engines for demanding single phase (MAX71315C/MAX71314C) and poly-phase (MAX71335C/MAX71334C) metering applications with up to 256KB flash, 21KB RAM, and a single-cycle 32x32 + 64 multiplier. The application processor (MPU) is a 32-bit MAXQ®30 core. The metrology processor (or Compute Engine, CE) is a 32-bit fixed-point processor dedicated to computing the metering parameters from voltage and current samples. The integrated security engines (AES-128/192/256, AES-GCM-128, DES, TRNG) provide fast data encryption and decryption for secure smart grid communications. Integrated 38kHz encoding and decoding functions saves BOM cost and reduces board space. Two touch switch pins enable capacitive touch detection.

The device family also integrates all the essential metering function blocks: LCD controller supporting up to 8 common planes with a maximum of 288 segments, real-time-clock (RTC) with automatic temperature compensation, and multiple serial communication ports (UART, I^2C, and SPI).

Applications

- Single- or Poly-Phase AMI Metering
- Energy Monitoring

Benefits and Features

- Advanced Metrology Provides the Best-In-Class Performance
  - Up to Seven Metrology Channels for Polyphase Metering and Up to Four Channels for Single-/ Two-Phase Metering
  - 0.1% Typical Accuracy Over 5000:1 Current Range with Integrated Metrology ADCs
  - Integrated ADCs Support Current Transformers, Rogowski Coils, and Shunts
  - Three Remote ADC Interfaces for Current Sensing with Remote Shunts

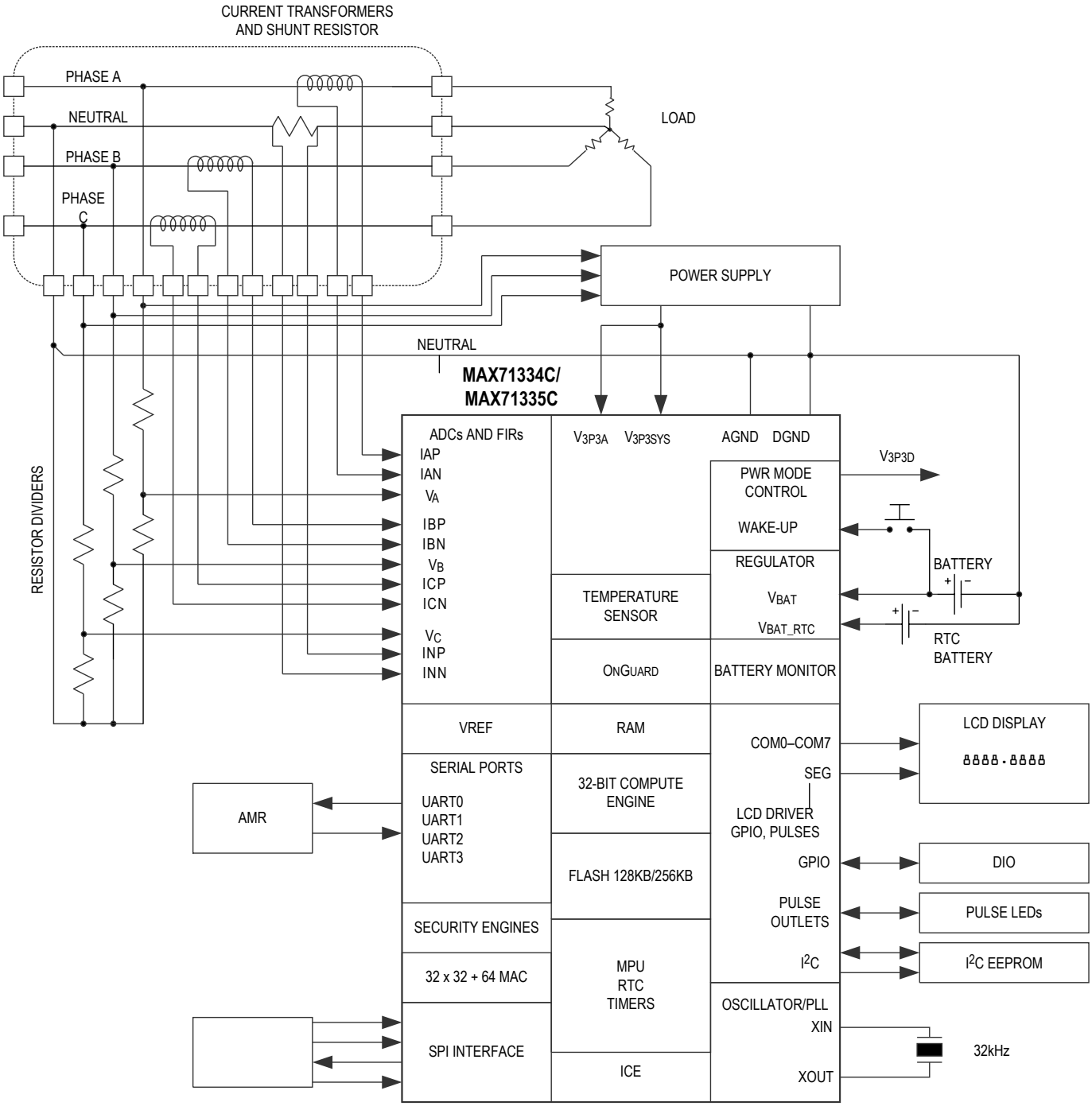
Benefits and Features (Continued)

- Dedicated RTC Circuit Ensures Accurate Timekeeping
- Integrated Security Engines for Secure Smart Metering
  - AES-128/192/256, and AES-GCM-128
  - True Random Number Generator
  - 3DES
  - On-Chip CE-OnGuard Protects Metering Operations from Unauthorized Access, and Ensuring Authenticity of Peripheral Operations
  - Supports Welmec/MID
- Rich Peripherals Support Reduces Board Space and Lowers BOM Cost
  - Low-Power ADC for Environmental Monitoring
  - LCD Controller Supporting Up to Eight Common Planes: 8x36 / 6x38 / 4x40
  - Up to 52 (ZON P3S/P3SL) or 54 (ZON M3S/M3SL) GPIO pins
  - SPI (Master and Slave), Master I^2C, 4x UARTs, Two Smart Card Ports, Two Touch Switch Inputs
  - 38kHz IR Encoder/Decoder
  - Single-Cycle 32x32 + 64 Multiply-Accumulate Unit for Demanding Signal Processing
- Dual 32-Bit Programmable Cores Provide High Processing Power and Flexibility
  - Metering Core (Compute Engine) with up to 20MIPS at 20MHz, and up to 8KB RAM for Data and Code
  - Application Core with up to 20MIPS at 20MHz, 256KB/128KB Flash Code Space, 12KB Data RAM plus 1KB NVRAM
- Configurable Operation Modes Save Power
  - 1.6µA SLP Mode (V_{BAT_RTC})
  - 14.6µA LCD Mode (V_{BAT_RTC} and V_{BAT})
  - 1KB NVRAM in SLP Mode, Optional 8KB NVRAM Backup in LCD Mode (with V_{BAT} active)
- LQFP-100 Package

***Ordering Information* appears at end of data sheet.**

Rev 8; 12/2019

Typical Application Circuit



Absolute Maximum Ratings

Voltage, Current Supplies and GND Pins

V_{3P3SYS}, V_{3P3A} .....-0.5V to +3.6V

V_{BAT}, V_{BAT_RTC} .....-0.5V to +3.8V

V_{LCD5} 7.0V

Crystal Pins

XIN, XOUT .....-10mA to +10mA, -0.5V to +3.0V

Digital Pins

Inputs (MSN/BRN/LCD_ONLY mode).....
.....-10mA to +10mA, -0.5V to +6V

Inputs (SLP mode).....
.....-10mA to +10mA, -0.5V to V_{3P3D} + 0.5V

Outputs .....-8mA to +8mA, -0.5V to V_{3P3SYS} + 0.5V

Maximum Combined Current into DIO Pins

Sink 100mA

Source 66mA

Temperature and ESD Stress

Operating Junction Temperature (pk., 100ms).....+140°C

Operating Junction Temperature (continuous).....+125°C

Storage Temperature Range: .....-45°C to +165°C

Lead Temperature (soldering, 10s)..... +300°C

Soldering Temperature (reflow): .....+250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

LQFP

Junction-to-Ambient Thermal Resistance (θ_{JA}).....48°C/W Junction-to-Case Thermal Resistance (θ_{JC}).....11°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{3P3A} Current + V_{3P3SYS} Current	I_{V3P3_1}	V_{LS} = LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 5MHz, staring ADC clock = 1.67MHz, MPU clock = 20MHz, standard CE code pass		15.6	18.5	mA
	I_{V3P3_2}	V_{LS} = LOW_BIAS = 0, preamp off, muxed ADC CLK = 5MHz, staring ADC clock = 1.67MHz, MPU clock = 20MHz, standard CE code pass		15.4	18.2	
	I_{V3P3_3}	V_{LS} = LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 2.5MHz, staring ADC clock = 0.83MHz, MPU clock = 20MHz, standard CE code pass		13.5	16.2	
	I_{V3P3_4}	V_{LS} = LOW_BIAS = 0, preamp off, muxed ADC CLK = 2.5MHz, staring ADC clock = 0.83MHz, MPU clock = 20MHz, standard CE code pass		13.45	16.1	
	I_{V3P3_5}	V_{LS} = 1, LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 1MHz, staring ADC clock = 0.33MHz, MPU clock = 4MHz, standard CE code pass		5	6.8	
	I_{V3P3_6}	V_{LS} = 1, LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 0.5MHz. staring ADC clock = 0.08MHz. MPU clock= 0.25MHz, standard CE code pass		2.9	3.6	
	I_{V3P3_7}	Metering off, CE off, ADCs disabled, MPU clock = 20MHz		10.8	16	
	I_{V3P3_9}	Metering off, CE off, ADCs disabled, MPU clock = 1.25MHz		4.6	6.25	
	I_{V3P3_10}	V_{LS} = 1, LOW_BIAS = 0, preamp off, muxed ADC CLK = 0.5MHz, staring ADC clock = 0.08MHz. MPU clock = 0.25MHz, standard CE code pass		2.9	3.5	
	I_{V3P3_11}	V_{LS} = 1, LOW_BIAS = 0, preamp off, muxed ADC CLK = 1MHz, staring ADC clock = 0.33MHz, MPU clock = 4MHz, standard CE code pass		5	6.75	

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES (continued)						
V_{BAT} Current (2.8-3.8V), BRN mode, standard CE code pass, $V_{3P3SYS/A}$ off	I_{BAT1}	V_{LS} = LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 5MHz, staring ADC clock = 1.67MHz, MPU clock = 20MHz		15.6	18.5	mA
	I_{BAT3}	V_{LS} = LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 0.5MHz, staring ADC clock = 0.42MHz, MPU clock = 1.25MHz		6.8	8.5	
	I_{BAT4}	V_{LS} = 1, LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 1MHz, staring ADC clock = 0.33MHz, MPU clock = 4MHz		5	6.75	
	I_{BAT5}	V_{LS} = 1, LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 1MHz, staring ADC clock = 0.166MHz, MPU clock = 2MHz		4.2	5.75	
	I_{BAT6}	V_{LS} = 1, LOW_BIAS = 0, preamp gain = 8, muxed ADC CLK = 0.5MHz, staring ADC clock = 0.08MHz, MPU clock = 0.25MHz		3.1	4	
V_{BAT} Current MSN Mode	I_{BAT10}			0	100	nA
V_{BAT} Current LCD_ONLY Mode	I_{BAT12}	LCD CLK (min), LCD DAC off, no LCD SRAM access, $V_{3P3SYS/A}$ off		3	6.4	µA
	I_{BAT13}	LCD CLK (min), LCD DAC on, no LCD SRAM access, $V_{3P3SYS/A}$ off, V_{BAT} = 2.8V to 3.8V		15	25	
V_{BAT} Current MSN, SLP				0	100	nA
V_{BAT_RTC} Current, MSN	$I_{VBATRTC1}$			0	100	nA
V_{BAT_RTC} Current BRN	$I_{VBATRTC2}$			1.6	3.0	nA
V_{BAT_RTC} Current LCD_ONLY	$I_{VBATRTC3}$			1.6	3.0	nA
V_{BAT_RTC} Current SLP (Note 1, except $I_{VBATRTC4}$)	$I_{VBATRTC4}$	RTC compensation off		1.6	3.0	µA
	$I_{VBATRTC5}$	TRANGE = 00, TEMPPER = 5		21	41	
	$I_{VBATRTC6}$	TRANGE = 00, TEMPPER = 6		11	25	
	$I_{VBATRTC7}$	TRANGE = 1F, TEMPPER = 5		7	16	

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SPIKE WIDTH TOLERANCE						
t_{SPIKE}, RSTN, and TEST		Positive spike, spike < 200ns is ignored			1100	ns
LOGIC LEVELS						
Digital High-Level Input Voltage	V_{IH}		2			V
Digital Low-Level Input Voltage	V_{IL}				+0.6	V
Input Pullup Current	I_{IL}	RSTN	5		175	µA
		All digital inputs except RSTN	40		175	
Input Pulldown Current, JTAG_E	I_{IH}	$V_{IN} = V_{3P3SYS}$	30		160	µA
Digital High-Level Output Voltage	V_{OH}	I_{LOAD} = 1mA	V_{3P3D} -0.4			V
		I_{LOAD} = 5mA	V_{3P3D} - 0.6			
Digital Low-Level Output Voltage	V_{OL}	I_{LOAD} = -1mA			0.4	V
		I_{LOAD} = -15mA			0.9	
Maximum Combined Current MSN Mode		V_{3P3SYS} = 3.0V, pull I out of V_{3P3D} until V_{3P3D} = 2.4V	66			mA
V3P3D SWITCH						
On-Resistance (V_{3P3SYS} to V_{3P3D})		$I(V_{3P3D}) \leq 1mA$		6	11	Ω
On-Resistance (V_{BAT} to V_{3P3D})		$I(V_{3P3D}) \leq 1mA$, $V_{BAT} \geq 2.2V$.		6	11	Ω
VREF						
V_{REF} Voltage		T_A = +22°C	1.225	1.228	1.231	V
V_{REF} PSRR		$\Delta V_{REF}/\Delta V_{3P3A}$, V_{3P3A} = 2.8V to 3.6V	-1.5		+1.5	mv/V
V_{NOM} Definition		$V_{NOM(T)} = V_{REF(22)} + (T-22) TC1 + (T-22)^2 TC2$				V
V_{NOM} Temperature Coefficient TC1 (non H)		$TC1 = -8.164\ 10^{-5} - 6.267\ 10^{-6} \times TRIMT$				V/°C
V_{NOM} Temperature Coefficient TC2 (non H)		$TC2 = -2.667\ 10^{-7} + 4.6386\ 10^{-9} \times TRIMT$				V/°C^2
V_{REF} Deviation from $V_{NOM(T)}$ (non-H, Note 1)		$[(V_{REF(T)} - V_{NONM(T)}) \times 10^6] / [V_{NOM(T)} \times 62)]$	-43.5		+43.5	ppm/°C

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER FAULT COMPARATORS						
V_{3AOK} Response Time, Including Filters		100mV overdrive falling	100		400	µs
		100mV overdrive rising	100		400	
V_{3OK} Response Time, Including Filters		100mV overdrive falling	100		400	
V_{3P3DOK} Response Time, Including Filters		100mV overdrive, rising	75		350	
V_{3OK} Response Time, Including Filters		100mV overdrive, falling	100		400	
V_{3P3DOK} Response Time, Including Filters		100mV overdrive, falling	75		350	
V_{DDOK} Response Time, Including Filters.		100mV overdrive, rising	75		350	
		100mV overdrive, falling	100		425	
Falling Threshold, V_{3AOK}		V_{3P3SYS} falling	2.81	2.9	2.99	V
Falling Threshold, V_{3OK}		V_{3P3SYS} falling	2.46		2.60	V
Falling Threshold, V_{DDOK}		V_{3P3D} falling, measure V_{DD}	1.4		1.76	V
Falling Threshold, V_{3P3DOK}		V_{3P3D} falling	2.1	2.26	2.42	V
VBAT/VBAT_RTC VOLTAGE MONITOR						
Measurement Resolution	V_{LSB}		24			mV/LSB
Nominal Value	BNOM	V_{3P3} = 3.3V, T_A = +22°C	121	125	130	LSB
Measurement Error		V_{BAT}/V_{BAT_RTC} = 2.0V to 4.0V	4.6			%
BinZ		In FBAT test mode, (battery frequency is output on TMUX)	250	390	535	kΩ
BCURR load		[I(V_{BAT}) with BCURR=1] - [I(V_{BAT}) with BCURR = 0]	80	100	130	µA
TEMPERATURE MONITOR						
Temperature Error		T_A = +22°C,	±3.6			°C
Relative Temperature Error (Note 1)		-40°C ≤ T_A ≤ +85°C,	-1.75		+1.75	°C
T_{LSB}			0.0811			°C/LSB
Temperature Equation			T=21.24 + 0.0811*STEMP – 1.83 10^{-6}*STEMP^2			°C
TETIME: Measurement time		Duration of activity on TEMP_VCO from TXUXOUT on TEMP_VCO, (temp measurement only)	20	35	60	ms

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STARING ADCs						
Usable Input Range		Preamp off	-250		+250	mV
		Preamp gain = 4	-62		+62	
		Preamp gain = 8	-31		+31	
		Preamp gain = 16	-15		+15	
Input Impedance		Preamp off	140		450	kΩ
		Preamp gain = 4	2.5		10	
		Preamp gain = 8	2.5		10	
		Preamp gain = 16	2.5		10	
LSB Size		FIR_LEN = 15		97		nV/LSB
Digital Full Scale				±3,375,000		LSB
Input Offset Preamp Off		Preamp off	-10		+10	mV
Input Offset		Preamp Gain = 4	-5.5		+5.5	mV
Input Offset		Preamp Gain = 8	-3		+3	mV
Input Offset Preamp		Gain = 16	-2		+2	mV
Preamp Gain		Gain = 4	3.9		4.1	V/V
Preamp Gain		Gain = 8	7.8		8.2	V/V
Preamp Gain		Gain = 16	15.6		16.4	V/V
Preamp Phase Shift				12		m°
Preamp Phase Shift Variation with Temperature (Note 1)			-0.27		+0.27	m°/°C
Channel Gain Variation vs. Supply		Variation of gain (both preamp and ADC), over supply	-40		+40	ppm/%
Channel Gain Variation vs. Temp (Note 1)		Variation of gain, (both preamp and ADC), over temperature	-55		+55	ppm/°C
ADC Gain Error vs. Supply		V_{IN} = 200mV$_{PK}$, 55Hz, V_{3P3A} = 2.8V to 3.6V		90		ppm/%
THD, Preamp + ADC Preamp Gain = 4		V_{IN} = 62.5mV$_{PK}$, 55Hz		-85		dB
THD, Preamp + ADC Preamp Gain = 8		V_{IN} = 31.25mV$_{PK}$, 55Hz		-85		dB
THD, Preamp + ADC Preamp Gain = 16		V_{IN} = 15.6mV$_{PK}$, 55Hz		-85		dB
THD, Bypass Preamp, 20mV$_{PK}$ Input		55Hz		-85		dB
THD, bypass Preamp, 250mV$_{PK}$ Input		55Hz		-85		dB

Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Preamp Input Equivalent Noise Density		Preamp gain = 8, V_{IN} = 20mV_{PK}, 55Hz, FIR_LEN = 11		300		$\frac{nV}{\sqrt{Hz}}$
ADC Noise (Bypass Preamp)		V_{IN} = 20mV_{PK}, 55Hz, FIR_LEN = 11		425		LSB
MUXED ADC						
Usable Input Range			-250		250	mV
Input Impedance			50		130	kΩ
LSB Size		FIR_LEN = 15		123		nV/LSB
Digital Full Scale				2,621,400		LSB
Input Offset			-10		+10	mV
ADC Gain Error vs. Supply		V_{IN} = 200mV_{PK}, 55Hz, V_{3P3A} = 2.8V to 3.6V			90	ppm/%
THD 20mVpk input				-85		dB
THD 250mVpk input				-85		dB
ADC Noise		V_{IN} = 20mV_{PK}, 55Hz, FIR_LEN = 11		400		LSB
ADC Input Equivalent Noise Density		V_{IN} = 20mV_{PK}, 55Hz, FIR_LEN = 11		2000		$\frac{nV}{\sqrt{Hz}}$
AUXILLARY ADC						
Resolution				10		Bits
ADC Clock Frequency	f_{ACLK}			4.92		MHz
Integral Nonlinearity	INL			±1.2		LSB
Differential Nonlinearity	DNL			±1		%LSB
Input Impedance				525		kΩ
Conversion Time				1024		Cycles
LCD DRIVERS						
V_{LCD} Current, V_{LCD} = 3.3V		LCD_E = 1, LCD_MODE = 110, LCD_ON = 1, LCD_CLK = 00, LCD_ VMODE = 11, all map bits = 0			4	µA

Electrical Characteristics (continued)

EXTERNAL CRYSTAL OSCILLATOR						
RTC Oscillator Frequency	F_{XTAL}			32.768		kHz
Maximum Crystal Power					1	µW
XIN to XOUT Capacitance	C_{XIN_XOUT}				3	pF
XIN Capacitance to DGND	C_{XIN_DGND}	X_{IN} = 100mV_{P-P}			5	pF
XOUT Capacitance to DGND	C_{XOUT_DGND}	X_{OUT} = 0V			5	pF
Frequency Variation with Voltage, V_{BAT_RTC} = 3.8V		Reference frequency V_{3P3} = 3.3V			0	ppm
Frequency Variation with Voltage, V_{BAT_RTC} = 3V		Reference frequency V_{3P3} = 3.3V			0	ppm
Frequency Variation with Voltage, V_{BAT_RTC} = 2.5V		Reference frequency V_{3P3} = 3.3V		0		ppm
Frequency Variation with Voltage, V_{BAT_RTC} = 2V		Reference frequency V_{3P3} = 3.3V		0		ppm
Frequency Variation with Voltage, V_{BAT_RTC} = 1.8V		Reference frequency V_{3P3} = 3.3V		0		ppm
Maximum Output Voltage		V_{IN} = .2V_{P-P} on XIN, sine wave 32kHz, no test load		1.5		V
HF frequency (Master Clock, Before Prescaler/ Divider)		PLL output frequency		58.98		MHz
INTERNAL 32K OSCILLATOR						
Nominal Frequency	f_{OSC}			32.768		kHz
Frequency Error			-2		+2	%

Electrical Characteristics (continued)

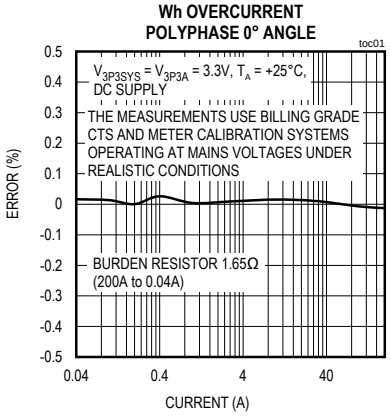
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING (Note 1)						
SPI Master Operating Frequency	$1/t_{MCK}$				$\frac{f_{CPU}}{2}$	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$				$\frac{f_{CPU}}{4}$	MHz
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$\frac{f_{MCK}}{2} - 35$			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$\frac{f_{MCK}}{2} - 35$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$\frac{f_{MCK}}{2} - 35$			ns
MISO Input Valid to SCLK Sample Edge Rise/Fall Setup	t_{MIS}		35			ns
MISO Input to SCLK Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}		$\frac{t_{SCKU}}{2}$			ns
SSEL Active to First Shift Edge	t_{SSE}			50		ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		35			ns
MOSI Input from SCLK SampleEdge Transition Hold	t_{SIH}		35			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				70	ns

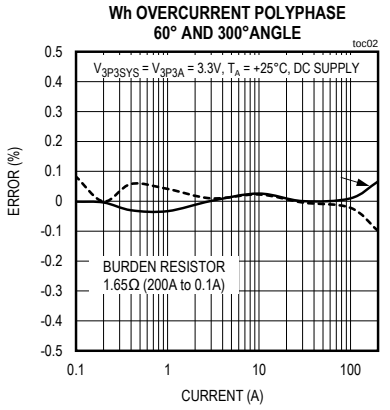
Electrical Characteristics (continued)

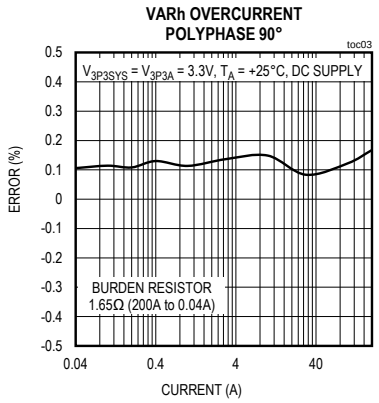
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I2C TIMING 400kHz (Note 1)						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP (P)and a START (S) Condition	t_{BUF}		1300			ns
Hold Time, Repeated START Condition, (Sr)	$t_{HD, STA}$		600			ns
Low Period of the SCL Clock	t_{LOW}		1300			ns
High Period of the SCL Clock	t_{HIGH}		600			ns
Setup Time for a Repeated START Condition (Sr)	$t_{SU, STA}$		600			ns
Data Hold Time	$t_{HD, DAT}$		0		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R			300		ns
Fall Time of SDA Transmitting	t_F			300		ns
Setup Time for STOP (P) Condition	$t_{SU, STO}$		600			ns
Capacitive Load for Each Bus Line	CB				400	pF
FLASH MEMORY						
Flash Write Cycles (Minimum Endurance)			100,000			Cycles
Flash Data Retention		T_A = +25°C	100			Years
		T_A = +85°C	25			
Page, (Sector), Erase Time			50			µs
Mass, (Chip), Erase Time			20		40	ms
Flash Write Time, Word Program Time)			6		7.5	µs

Note 1: Parameter not production tested, guaranteed by design to six-sigma.

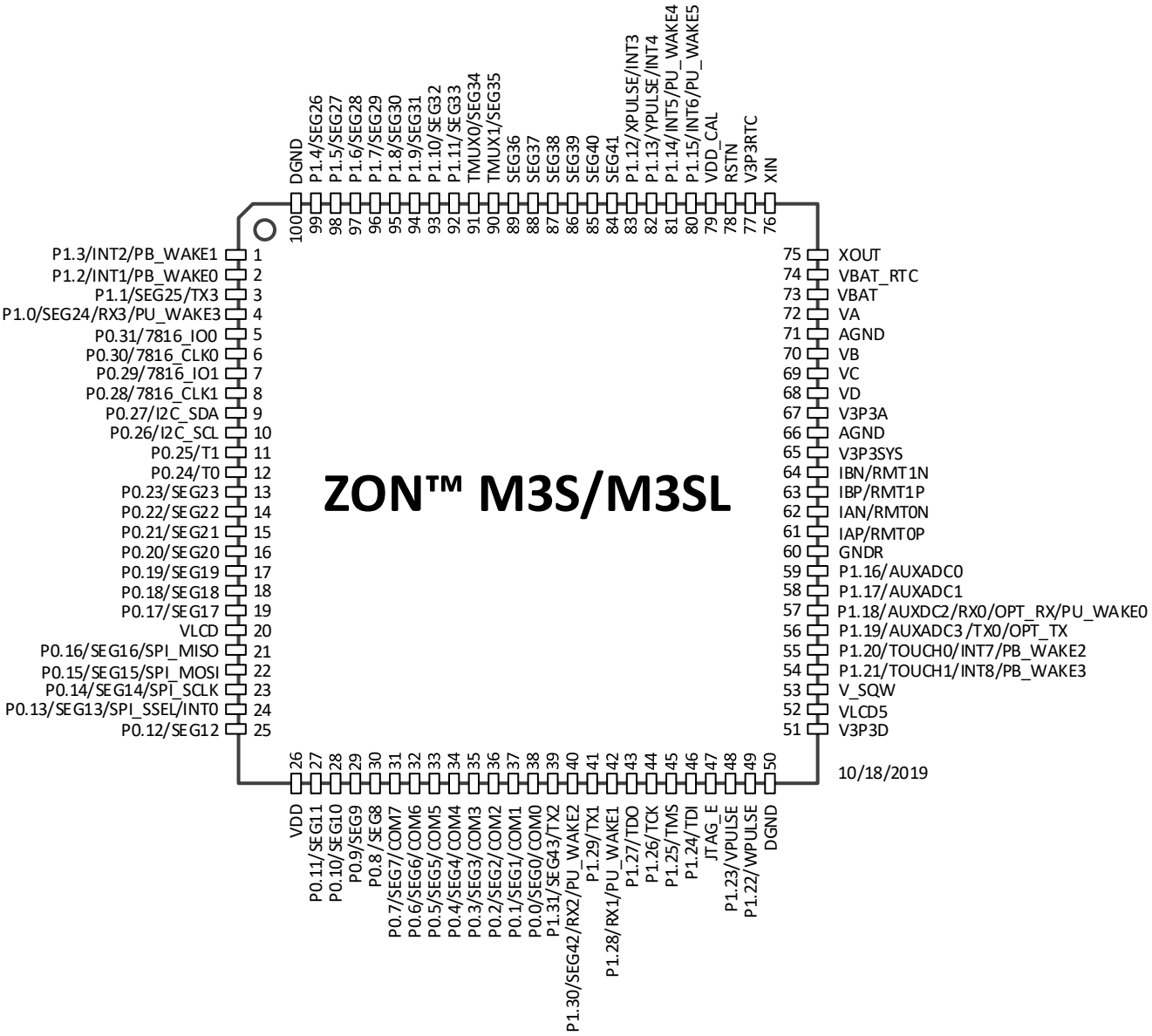
Typical Operating Characteristics



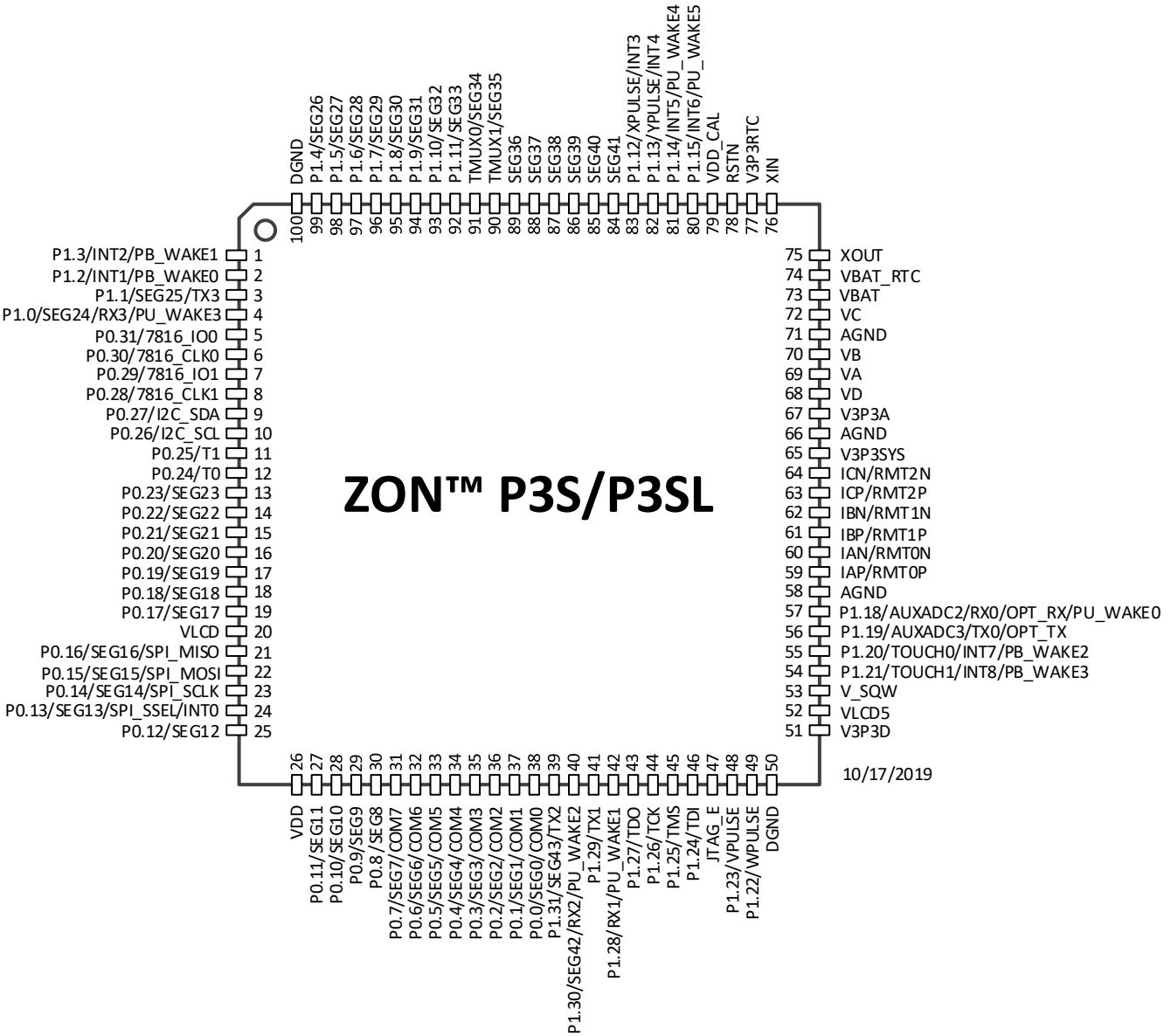




Pin Configuration



Pin Configurations (continued)



Pin Description

PIN		NAME	FUNCTION
MAX7133xC P3S/P3SL	MAX7131xC M3S/M3SL		
1	1	P1.3/INT2/ PB_WAKE1	GPIO Port 1 Bit 3 External Interrupt 2 Level-Triggered Wake Input 1
2	2	P1.2/INT1/ PB_WAKE0	GPIO Port 1 Bit 2 External Interrupt 1 Level-Triggered Wake Input 0
3	3	P1.1/SEG25/TX	GPIO Port 1 Bit 1 LCD Segment 25 UART3 TxD
4	4	P1.0/SEG24/ RX3/PU_WAKE	GPIO Port 1 Bit 0 LCD Segment 24 UART3 RxD Edge Triggered Wake Input 3
5	5	P0.31/7816_IO	GPIO Port 0 Bit 31 ISO UART0 I/O
6	6	P0.30/7816_CL	GPIO Port 0 Bit 30 ISO UART0 Clock
7	7	P0.29/7816_IO	GPIO Port 0 Bit 29 ISO UART1 I/O
8	8	P0.28/7816_CL	GPIO Port 0 Bit 28 ISO UART1 Clock
9	9	P0.27/I2CSDA	GPIO Port 0 Bit 27 I^2C SDA
10	10	P0.26/I2CSCL	GPIO Port 0 Bit 26 I^2C SCL
11	11	P0.25/T1	GPIO Port 0 Bit 25 Timer Channel 1 Output
12	12	P0.24/T0	GPIO Port 0 Bit 24 Timer Channel 0 Output
13	13	P0.23/SEG23	GPIO Port 0 Bit 23 LCD Segment 23
14	14	P0.22/SEG22	GPIO Port 0 Bit 22LCD Segment 22
15	15	P0.21/SEG21	GPIO Port 0 Bit 21LCD Segment 21
16	16	P0.20/SEG20	GPIO Port 0 Bit 20LCD Segment 20
17	17	P0.19/SEG19	GPIO Port 0 Bit 19LCD Segment 19
18	18	P0.18/SEG18	GPIO Port 0 Bit 18LCD Segment 18
19	19	P0.17/SEG17	GPIO Port 0 Bit 17LCD Segment 17
20	20	V_{LCD}	V_{LCD}
21	21	P0.16/SEG16/ SPI_MISO	GPIO Port 0 Bit 16 LCD Segment 16 SPI Peripheral—Master In, Slave Out
22	22	P0.15/SEG15/ SPI_MOSI	GPIO Port 0 Bit 15 LCD Segment 1 SPI Peripheral—Master Out, Slave In
23	23	P0.14/SEG14/ SPI_SCLK	GPIO Port 0 Bit 14 LCD Segment 14 SPI Peripheral—Serial Clock
24	24	P0.13/INT0/SEG13/ SPI_SSEL	GPIO Port 0 Bit 13 External Interrupt 0 LCD Segment 13 SPI Peripheral— Slave Select
25	25	P0.12/SEG12	GPIO Port 0 Bit 12 LCD Segment 12
26	26	V_{DD}	Bypass Point for the Internal Core Regulated Power Rail.
27	27	P0.11/SEG11	GPIO Port 0 Pin 11 LCD Segment 11
28	28	P0.10/SEG10	GPIO Port 0 Bit 10 LCD Segment 10
29	29	P0.9/SEG9	GPIO Port 0 Bit 9 LCD Segment 9
30	30	P0.8/SEG8	GPIO Port 0 Bit 8 LCD Segment 8
31	31	P0.7/SEG7/CO	GPIO Port 0 Bit 7 LCD Segment 7 LCD Common 7

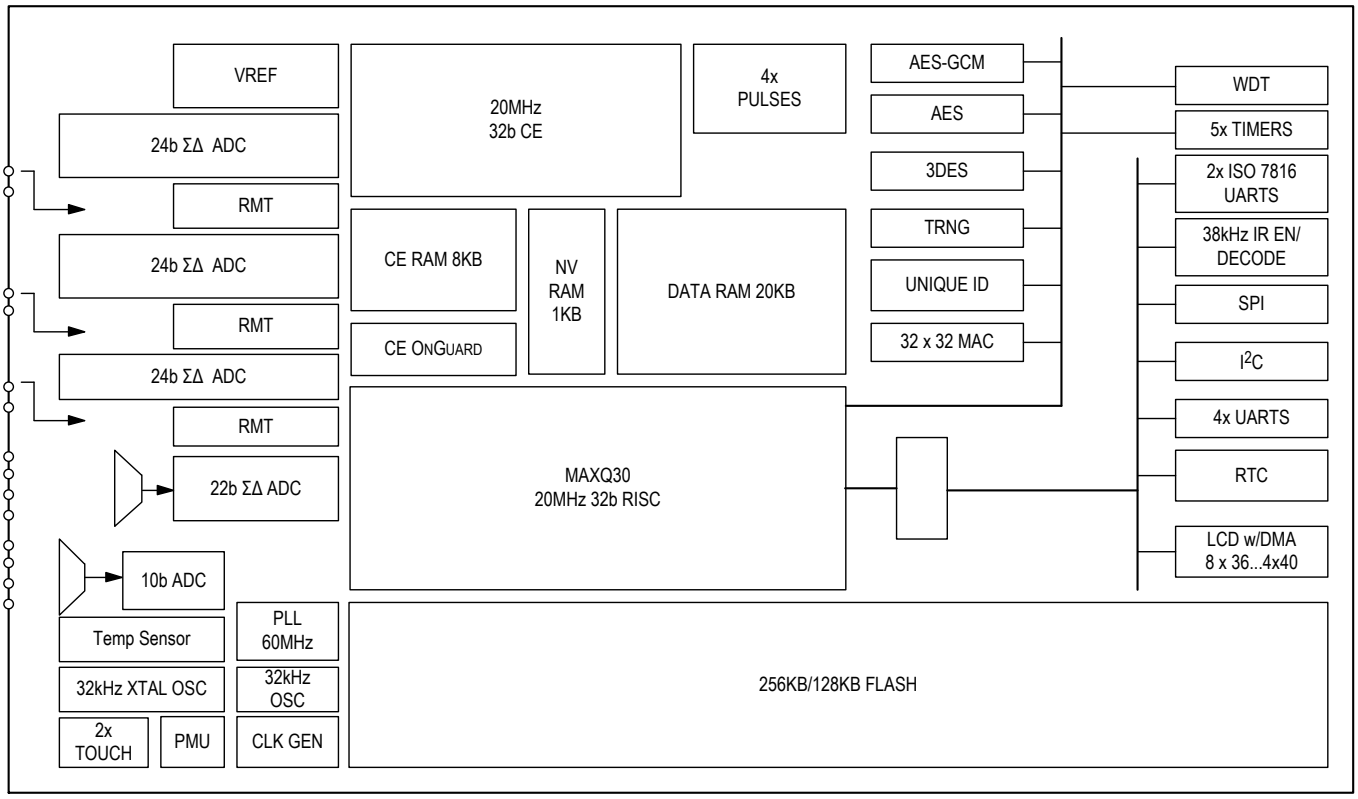
Pin Description (continued)

PIN		NAME	FUNCTION
MAX7133xC P3S/P3SL	MAX7131xC M3S/M3SL		
32	32	P0.6/SEG6/ COM6	GPIO Port 0 Bit 6 LCD Segment 6 LCD Common 6
33	33	P0.5/SEG5/ COM5	GPIO Port 0 Bit 5 LCD Segment 5 LCD Common 5
34	34	P0.4/SEG4/COM4	GPIO Port 0 Bit 4 LCD Segment 4 LCD Common 4
35	35	P0.3/SEG3/COM3	GPIO Port 0 Bit 3 LCD Segment 3 LCD Common 3
36	36	P0.2/SEG2/COM2	GPIO Port 0 Bit 2 LCD Segment 2 LCD Common 2
37	37	P0.1/SEG1/COM1	GPIO Port 0 Bit 1 LCD Segment 1 LCD Common 1
38	38	P0.0/SEG0/COM0	GPIO Port 0 Bit 0 LCD Segment 0 LCD Common 0
39	39	P1.31/SEG43/TX2	GPIO Port 1 Bit 31LCD Segment 43UART2 TxD
40	40	P1.30/SEG42/RX2/ PU_WAKE2	GPIO Port 1 Bit 30 LCD Segment 42 UART2 RxD Edge Triggered Wake Input 2
41	41	P1.29/TX1	GPIO Port 1 Bit 29 UART1 TxD
42	42	P1.28/RX1/PU_ WAKE1	GPIO Port 1 Bit 28 UART1 RxD Edge Triggered Wake Input 1
43	43	P1.27/TDO	GPIO Port 1 Bit 27 JTAG Test Data Out
44	44	P1.26/TCK	GPIO Port 1 Bit 26 JTAG Test Clock
45	45	P1.25/TMS	GPIO Port 1 Bit 25 JTAG Test Mode Select
46	46	P1.24/TDI	GPIO Port 1 Bit 24 JTAG Test Data In
47	47	JTAG_E	JTAG_E. JTAG Enable. If high, pins 43–46 are configured as JTAG test pins. If low, pins 43–46 are configured as GPIO.
48	48	P1.23/VPULSE	GPIO Port 1 Bit 23 CE Meter Pulse—Reactive Energy
49	49	P1.22/WPULSE	GPIO Port 1 Bit 22 CE Meter Pulse—Real Power
50	50	GNDD1	Digital Ground
51	51	V3P3D	Internal Switch Output. Provides power to internal blocks and the core regulator. Primarily used to bypass the power supply, it can also be used to provide a small amount of battery-backed power for external devices.
52	52	VLCD5	5V Input for Boosted LCD Voltage. The MAX71315C contains no charge pump, but it includes a square-wave output to charge an external storage capacitor.
53	53	V_SQW	Dedicated square-wave output to drive an external charge pump to generate 5V for LCD glass that requires this voltage.
54	54	P1.21/TOUCH/ INT8/PB_WAKE3	GPIO Port 1 Bit 21 Touch Switch 1 Input External Interrupt 8 Level-Triggered Wake Input 3

PIN		NAME	FUNCTION
MAX7133xC P3S/P3SL	MAX7131xC M3S/M3SL		
55	55	P1.20/TOUCH/ INT7/ PB_WAKE2	GPIO Port 1 Bit 20 Touch Input 0 Interrupt Input 7 Level-Triggered Wake Input 2
56	56	P1.19/ADC3/ TX0/ OPT_TX	GPIO Port 1 Bit 19 Auxiliary ADC Input 3 UART0 Tx D, Optical Driver Output
57	57	P1.18/ADC2/ RX0/OPT_RX/ PU_WAKE0	GPIO Port 1 Bit 18 Auxiliary ADC Input 2 UART0 RxD, Optical receiver Input Edge Triggered Wake Input 0
58	—	GNDR	Ground Connection
—	58	P1.17/ADC1	GPIO Port 1 Bit 17, Auxiliary ADC Input 1
59	61	IAP/RMT0P	Current Channel A Positive Input, Remote Channel 0 Positive Input
—	59	P1.16/ADC0	GPIO Port 1 Bit 16 Auxiliary ACD Input 0
60	62	IAN/RMTON	Current Channel A Negative Input, Remote Channel 0 Negative Input
—	60	GNDR	Ground Connection
61	63	IBP/RMT1P	Current Channel B Positive Input, Remote Channel 1 Positive Input
62	64	IBN/RTM1N	Current Channel B Negative Input, Remote Channel 1 Negative Input
63	—	ICP/RMT2P	Current Channel C Positive Input, Remote Channel 2 Positive Input
64	—	ICN/RMT2N	Current Channel C Negative Input, Remote Channel 2 Negative Input
65	65	V_{3P3SYS}	Primary Power Input for Digital Sections of the Device.
66	66	GNDA	Analog Ground
67	67	V_{3P3A}	Primary Power Input for the Analog Section of the Device.
68	68	VD/INP	Single-Ended Analog Input/Neutral Current Channel Input (Single-Ended)
69	69	V_A (VC in M3S/ M3SL)	Single-Ended Analog Input/Voltage Channel A Input (Single-Ended Analog Input/Voltage Channel C Input in M3S/M3SL)
70	70	V_B	Voltage Channel B Input
71	71	GNDA	Analog Ground
72	72	V_C (VA in M3S/ M3SL)	Voltage Channel C Input (Voltage Channel A input in M3S/M3SL)
73	73	V_{BAT}	Primary Battery Power
74	74	V_{RTC_BAT}	Secondary Battery Power (RTC/NVRAM Only)
75	75	XOUT	Crystal Oscillator Out. Connect to either a 32,768kHz tuning fork crystal or to a 16MHz AT-cut microprocessor crystal.
76	76	XIN	Crystal Oscillator Input. Connect to a 32.768kHz tuning fork crystal or to a 16MHz AT-cut microprocessor crystal.
77	77	V_{3P3RTC}	Bypass Point for RTC Power Supply Rail
78	78	RSTN	Device Reset
79	79	V_{DD_CAL}	RTC Calibration Bypass
80	80	P1.15/INT6/ PU_WAKE5	GPIO Port 1 Bit 15 External Interrupt 6 Edge Triggered WAKE 5
81	81	P1.14/INT5/ PU_WAKE4	GPIO Port 1 Bit 14 External Interrupt 5 Edge Triggered WAKE 4

PIN		NAME	FUNCTION
MAX7133xC P3S/P3SL	MAX7131xC M3S/M3SL		
82	82	P1.13/YPULSE/ INT4	GPIO Port 1 Bit 13 Meter Pulse Y External Interrupt 4
83	83	P1.12/XPULSE/ INT3	GPIO Port 1 Bit 12 Meter Pulse X External Interrupt 3
84	84	SEG41	LCD Segment 41
85	85	SEG40	LCD Segment 40
86	86	SEG39	LCD Segment 39
87	87	SEG38	LCD Segment 38
88	88	SEG37	LCD Segment 37
89	89	SEG36	LCD Segment 36
90	90	TMUX1/SEG35	Test Multiplexer Output 1 LCD Segment 35
91	91	TMUX0/SEG34	Test Multiplexer Output 0 LCD Segment 34
92	92	P1.11/SEG33	GPIO Port 1 Bit 11 LCD Segment 33
93	93	P1.10/SEG32	GPIO Port 1 Bit 10 LCD Segment 32
94	94	P1.9/SEG31	GPIO Port 1 Bit 9 LCD Segment 31
95	95	P1.8/SEG30	GPIO Port 1 Bit 8 LCD Segment 30
96	96	P1.7/SEG29	GPIO Port 1 Bit 7 LCD Segment 29
97	97	P1.6/SEG28	GPIO Port 1 Bit 6 LCD Segment 28
98	98	P1.5/SEG27	GPIO Port 1 Bit 5 LCD Segment 27
99	99	P1.4/SEG26	GPIO Port 1 Bit 4 LCD Segment 26
100	100	GNDD	Digital Ground

Simplified Block Diagram



Recommended Operating Conditions

PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{3P3SYS}, V_{3P3A} Supply Voltage—Mission Mode*	V_{BAT} = 0V to 3.8V V_{RTC} = 0V to 3.8V	3.0	3.6	V
V_{BAT} Voltage—BRN Mode	V_{3PSYS} < 2.8V and V_{RTC} V_{3P3SYS} (max) > 2.0V	2.5	3.8	V
V_{3P3SYS} Slew Rate			0.1	V/ms
V_{BAT_RTC} Voltage	V_{3P3SYS} < 2.0V	2.0	3.8	V
Operating Temperature		-40	+85	°C

**V3P3SYS and V3P3A pins must be tied together.*

Detailed Description

Hardware Overview

The MAX71334C (ZON P3SL)/MAX71335C (ZON P3S) poly-phase and MAX71314C (ZON M3SL)/MAX71315C (ZON M3S) single-phase electricity meter SOCs incorporate a 2-bit MAXQ30 microcontroller core, delivering approximately one MIPS/MHz of clock (nominally, 9.83MHz), a 32-bit dedicated metrology Compute Engine, high-precision ADCs, multichannel metrology AFE, inter- faces for remote sensors, and a complete set of peripherals onto a single device. The devices are available in a 100-pin LQFP package.

The devices offer a display controller that supports 8-way multiplexing of LCD segments. Up to 36 available segment pins provide up to 288 controllable display segments in the 8-way multiplexing configuration. Measurement results can be displayed on an LCD, either 3.3V glass commonly used in low-temperature environments, or 5V glass used in more demanding environments using an external 5V power supply. An oscillator pin allows the use of an external charge pump to create the 5V LCD voltage. Flexible mapping of LCD display segments facilitate integration of existing custom LCDs.

The devices integrate four high-precision 24-bit delta-sigma ADCs for measuring three current channels (differential inputs) and three voltage channels (single-ended multiplexed inputs). A fixed-point Compute Engine (CE) processes the ADC samples. The code for the CE resides in RAM and is shared with the MAXQ30 Core.

The devices also contain two (three for polyphase) remote interfaces capable of supporting up to four (six for polyphase) metrology channels. Typically, these channels are assigned to measure the primary parameters of interest, such as line voltage, line current, and neutral cur- rent, plus any other analog signal of interest. The remote channels are self-contained and provide inherent isolation to protect the devices from line potentials. In the current channels, select any sensor including current transformers, shunts, or Rogowski coils.

The devices include a separate ADC subsystem (the auxiliary ADC) to monitor slow-moving environmental conditions. This ADC samples at a 5kHz rate and can be multiplexed between any of four pins.

The devices are clocked by one 32,768Hz tuning-fork-type crystal that is used as a reference for the RTC. A phase-locked loop multiplies this clock to provide the 9.83MHz required by the core, the 19.66MHz required by the CE, and other clocks required by the system.

In a typical application, the CE of the devices processes the samples from its metrology input channels and performs calculations to measure real energy and reactive energy, as well as volt-ampere hours, A2h, and V2h for four-quadrant metering. These measurements are then accessed by the MAXQ30 Core, processed further, and output using the peripheral devices available to the MPU.

The devices feature a real-time clock to record time-of- use (TOU) metering information for multi-rate applications, and to time-stamp tamper or other events.

The devices include a precision voltage reference. A temperature-correction mechanism guarantees conformance to accuracy standards over temperature. Temperature- dependent external components such as crystal oscillator, current transformers and their corresponding signal-conditioning circuits, can be characterized, with their correction factors programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

The devices have two pins that are configurable as touch-detect inputs. When configured for touch detect, the pins self-oscillate at a frequency dependent on the capacitive load on the pins. A low-power timer circuit measures the oscillation frequency and alerts the CPU when the frequency falls below a certain threshold (indicating an increase in the capacitive loading). If desired, these inputs can wake the processor.

The devices have four UART channels with independent baud-rate generators. These UART channels can connect to driver/receiver chips for RS-232 or, with an additional GPIO pin for transmit enable, for RS-422/RS-485. One of the four UART channels can be dedicated for infrared I/O. In this configuration, transmitted data combines with a carrier signal so that the modulated carrier can be applied to an IR transmitter; the received modulated carrier is applied to a filter to extract the modulation waveform before being applied to the UART input.

The devices include two ports for smart cards for prepay metering applications. In many applications, the pins can connect directly to the smart card sockets. It is also possible to use external transceivers to achieve full ISO 7816 compliance.

The devices include standard peripherals for interfacing serial memory devices and complex display subsystems, among other devices. These devices include one SPI port and one I^2C port.

The devices contain the essential security accelerators for fast and secure data encryption, decryption, and authentication. The true random number generator (TRNG) generates a FIPSx compliant random number in x1 clock cycles. The AES engine supports three key lengths: 128 bits, 192 bits, and 256 bits. It completes encryption in 2x clock cycles and decryption 3x clock cycles. The AES- GCM supports 128-bits mode only.

Analog Front End

The devices contain three staring delta-sigma ADC converters and one delta-sigma ADC converter that can be configured to multiplexed up to four inputs. In a typical polyphase meter application, the three staring converters monitor line current and the fourth multiplexed converter monitors the line voltages with neutral current. In a single-phase meter application, the three staring converters monitor line current and line voltage. Three ADCs contain preamplifiers that provide a gain of 1, 4, 8, or 16, as required.

Analog inputs sample at up to 5MHz. The samples decimate in a FIR filter with an oversampling ratio of up to 512. Finished samples are available to the CE at up to 10.92ksps per channel.

Inputs to the ADC channels are referenced to AGND and must be scaled so that the signal is no greater than $250mV_{PK}$ above or below AGND.

Metering

The devices contain two separate metrology subsystems. The first subsystem is a set of four DC modulators and associate decimation filters. These four modulators are typically configured to monitor line current, neutral current and line current, with the fourth modulator responsible for monitoring other conditions, such as a second voltage channel, temperature or a magnetic sensor for tamper detection. The second subsystem is a pair of remote interfaces that interface to Silergy's remote sensors. These remote sensors can be configured to measure line and neutral current using current shunts rather than transformer or Rogowski coils, with isolation in both the measurement channels and the power circuit provided by inexpensive pulse transformers

The analog section of the devices consists of four analog-to-digital converters:

ADC0: Dedicated to current channel A (line current). An optional preamplifier can be inserted into the circuit for additional gain.

ADC1: Dedicated to current channel B (line current). An optional preamplifier can be inserted into the circuit for additional gain.

ADC2: Dedicated to current channel C (line current). An optional preamplifier can be inserted into the circuit for additional gain.

ADC3: Can be configured to multiplex among the three voltage inputs VA, VB, VC, or IN.

Remote Channels

The devices support the use of two remote interfaces for isolating the current channels. There are two generic types of remote interface supported, one is the 71M6000 series single-channel isolated remote interface, and the other is the MAX7107X 2-channel isolated remote interface. Both types of remote interface ICs use a pulse transformer to provide power to the device and to communicate ADC data and status information back to the device.

The pulse transformer effectively isolates the remote sensor interface and its attached sensors that typically operate at line potential (the hot side) from the ZON M3SL/ M3S microcontroller (the cold side).

The devices provide a pulse stream that traverses the transformer and is rectified by the remote interface to provide power. The devices also transmit control data in the forward direction (ZON P3S/P3SL/ M3S/M3SL to remote), and the remote interface provides a stream of ADC data, as well status information, in the reverse direction (remote to P3S/ P3SLM3S/M3SL).

Compute Engine (CE)

The Compute Engine (CE) is a dedicated 32-bit fixed-point RISC processor. It performs the signal processing necessary to accurately measure energy.

The CE is a programmable device, for which Silergy provides binary code modules. The flexibility of the CE code allows for adaptation of the meter to various metering requirements or sensor types without having to change hardware. It is possible to store more than one CE code image in flash and load the CE image dynamically during meter operation. The CE calculations and processes can include:

- Scaling of the processed samples based on calibration coefficients and MAXQ30 Core temperature compensation information
- DC removal
- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time)
- Combination of intermediate energy results per the implemented meter equation
- 90° phase shifter (for VAR calculations)
- Pulse generation, based on CE internal data or based on data provided by the MAXQ30 Core
- Measurement of the input signal frequency (for frequency and phase information)
- Measurement of the phase angles between the various phases
- Monitoring of the input signal amplitude (for sag and/ or swell detection)
- Extraction, suppression, or filtering of harmonics for special functions
- Variable phase compensation for adjustment of the phase angle generated by CTs or VTs

Compute Engine RAM

The Compute Engine uses a single 4K x 16 block of RAM for both code and data storage.

CE code is written to the RAM block by the MAXQ30 processor core during system initialization. After that, the MAXQ30 Core releases the CE to begin executing. The RAM space is shared by the MAXQ30 Core, the CE, and the ADC/FIR block by means of interleaved cycles.

Because of the time interleaving the CE data RAM can be accessed apparently simultaneously by the CE and the MAXQ30 Core. The CE can access any location in the shared SRAM. The MAXQ30 Core reads and writes the SRAM as the primary means of data communication between the two processors.

The CE deals with all data on a 64-bit or 32-bit basis and has no concept of single bytes. The shared memory controller stores 32-bit words from the CE in the same way that the MAXQ30 Core reads and writes so that the byte order of the MAXQ30 Core aspects is preserved.

Associated with the CE is a real-time monitor (RTM), a hardware block that reads up to four selected location in CE RAM and streams the data out on the TMUX pins.

The CE data RAM can be accessed by the ADC/FIR block, the RTM, the CE, and the MAXQ30 Core. Assigned time slots are reserved for MAXQ30 Core and metering so that memory accesses to shared RAM do not collide. FIR data is written one clock cycle after the FIR completes its calculation. RTM data is read from the locations specified by RTM0, RTM1, RTM2, and RTM3 in the scheduled time slots to avoid collision with MAXQ30 Core accesses.

CE Registers

CE registers provide the means of communication between CE and MAXQ30 Core. CE registers are not physical locations, but RAM locations defined by the CE code. Typical CE codes provide essential metrology data in a set of 32-bit wide output registers that can be accessed by the MAXQ30 Core after an accumulation interval is completed. Examples for CE registers are:

- Real energy collected per phase
- Real energy combined per implemented meter equation
- Fundamental content of real energy collected per phase
- Fundamental content of real energy combined per implemented meter equation
- Reactive energy collected per phase
- Reactive energy combined per implemented meter equation

- Summed squares of currents per phase
- Summed squares of voltages per phase, including neutral current
- Mains frequency
- Wh pulse count
- VARh pulse count

Voltage phase angle A/B and A/C Inputs from the MAXQ30 Core to the CE are also provided in CE registers and comprise the following:

- CE code configuration (selection of phases to be monitored, type of pulse generation, etc.)
- Pulse rate
- Number of samples per accumulation interval
- Sag/swell thresholds and time limits
- Pulse source registers
- Magnitude and phase adjustments from calibration
- Noise cancelling

A complete description of all CE registers, functionality, LSB values, and general code performance can be found in the CE Code Reference Manual for the particular CE Code.

Meter Equations

Typical CE codes can implement the equations listed in Table 1. The ZON P3S/P3SL standard polyphase CE codes implement only equation 5. The ZON M3S/M3SL standard single-phase CE codes implement equations 0, 1, and 2 only. For other configurations, contact the factory.

Pulse Generators

The devices' pulse generator hardware supports the primary pulses (VPULSE and WPULSE) and the secondary pulse outputs (XPULSE and YPULSE). During each CE code pass, the hardware stores exported sign bits in an 8-bit FIFO and outputs them at a specified interval. This permits the CE code to calculate all the pulse generator outputs at the beginning of its code pass and to rely on hardware to spread them evenly over the sample frame. The FIFO resets at the beginning of each sample frame. The pulse generator outputs are available as alternate functions on P1.12, P1.13, P1.22, and P1.23. The devices provide four pulse generators (VPULSE, WPULSE, XPULSE, and YPULSE). The XPULSE and YPULSE generators are used by standard CE code to output CE status indicators, such as sag detection, to the GPIO pins. All pulses are configurable to generate interrupts to the MAXQ30 Core. The polarity of the pulses can be inverted with PINV. When this bit is set, the pulses are active high, rather than the more usual active low. PINV inverts all the pulse outputs. The pulse rate of the CE can be adjusted within a wide range using a dedicated CE register located in the CE RAM. The meter constant (Kh) of the meter can be changed dynamically (e.g., to provide fast calibration).

XPULSE and YPULSE

Pulses generated by the CE can be exported to the XPULSE and YPULSE pulse outputs. Generally, the XPULSE and YPULSE outputs are updated once on each pass of the CE code. Standard CE code permits the signaling of a sag event for the YPULSE output. The XPULSE output indicates zero crossings of the main voltage that can be used to synchronize PLC modems or other equipment.

Table 1. Metering Equations

EQU	CALCULATION METHOD FOR WH AND VARH	DESCRIPTION
0	$V_A \times I_A$	(1 element, 2-W)
1	$V_A \times (I_A - I_B)/2$	(2 element, 3-W)
2	$V_A \times I_A + V_B \times I_B$	(2 element, 3-W, 3φ Delta)
3	$V_A \times (I_A - I_B)/2 + V_C \times I_C$	(2 element, 4W 3φ Delta)
4	$V_A \times (I_A - I_B)/2 + V_B \times (I_C - I_B)/2$	(2 element, 4W 3φ Wye)
5	$V_A \times IA + V_B \times I_B + V_C \times I_C$	(3 element, 4W 3φ Wye)

Compute Engine—MAXQ30 Communication

The Compute Engine alerts the MAXQ30 Core to changes in its condition over six circuits:

- **CE_BUSY:** This signal indicates that the CE is actively processing data. The trailing edge of this signal can interrupt the MAXQ30 Core for events that must be processed on each sample.
- **XFER_BUSY:** This signal indicates that the CE is updating the output region of the CE RAM with data for the MAXQ30 Core. This update typically includes the result of energy and squared-sample summations, and it occurs after the number of samples specified in the SAMPLE field of the CECN register has been processed. This signal can interrupt the MAXQ30 Core for those events that must be processed every accumulation interval.
- **VPULSE, WPULSE:** These output pulses can be configured to interrupt the MAXQ30 Core. Typically, WPULSE indicates a certain amount of real energy has been accumulated, and VPULSE indicates a certain amount of reactive energy has been accumulated. These signals can be routed directly to DIO pins to provide direct outputs to pulse LEDs or alert other external equipment.

Metrology ADCs Control

The metrology ADC channels operate essentially autonomously, depositing samples into RAM belonging to the CE and alerting the CE that a cycle is required to accumulate the new samples. However, the metrology subsystem must be configured to operate properly.

MAXQ30 Core

The devices use a MAXQ30 32-bit CPU core as the administrative processor.

The MAXQ30 Core is a 32-bit RISC core. It is unique because all instructions can be coded as a simple MOVE instruction, yielding high efficiency in both time and power.

The MAXQ30 Core has the following characteristics:

- Instructions typically execute in a single cycle
- All peripherals are first-class data objects
- Flexible data pointers make block data moves simple
- Dedicated 32 x 32 single-cycle multiplier

The MAXQ Family User's Guide contains information on the MAXQ30 architecture.

Multiply-Accumulate Unit

The devices provide a 32 x 32 fixed-point, multiply-accumulate unit to assist in mathematical operations. The multiplier provides a 64-bit result in a single cycle, and sums the product to a 64-bit accumulator in the same cycle. The multiplier is ready for another operation two cycles later. If the MAXQ30 Core is running at 10MHz, the multiplier can perform five million 32 x 32 multiply cycles per second, in theory (in practice, the throughput is slowed by the requirement of loading and unloading the multiplier registers). The multiplier contains two input registers and two sets of two output registers.

The multiplier also contains a control register that configures the multiplier for various purposes. It manages the following functions and features:

Signed-unsigned multiplication: 32-bit unsigned values or 2's complement values.

Multiply-accumulate enable: Selects either multiply plus accumulate operation or multiply only operation.

Multiply accumulate negate: Negates the result of the multiply operation before being added to the accumulator

Operand count select: A multiply-accumulate operation can occur after either operand has been loaded

Square function enable: In this mode, any write to *either* input register triggers a multiply operation using the register that was written as both the multiplier and the multiplicand, effectively squaring the value written.

Clear data operation: Clears all registers and flags.

Overflow flag

Multiplier and accumulation results are available in the cycle after the last operand is written. However, the results are available for a second multiply-accumulate cycle only in the following cycle. That means it is possible to overrun the multiply-accumulate unit if successive single-operand operations or square operations are performed without intervening delay cycles (two-operand operations are not restricted in this way).

Register Complement

The MAXQ30 Core supports 512 32-bit registers. Not all these register addresses are used in all core implementations. Registers are divided into two blocks:

- System registers (called special-purpose registers, consisting of accumulators, memory pointers, and other core registers)
- Peripheral registers (called special-function registers)

The 512 registers are divided into blocks of register modules. A register module is a group of up to 32 related registers. The MAXQ30 architecture supports up to 16 register modules. Register modules 0–5 are dedicated to special-function registers (peripherals), while registers 7–15 are dedicated to special-purpose registers (system registers). I/O is typically performed using registers. The MAXQ30 architecture supports up to 512 registers in 16 register modules. Each register can be up to 32 bits in length. Registers are first-class data objects, so peripheral objects can take part in ALU transactions, be tested for values, or any other operation that a CPU register can do in other architectures.

All registers are described in detail in the ZON P3S/P3SL/M3S/M3SL hardware reference manual). In demo code and in the hardware reference manual, register locations are sometimes called out using a hexadecimal address, for example 0x154. In this format, 4 is the module and 0x15 is the register address.

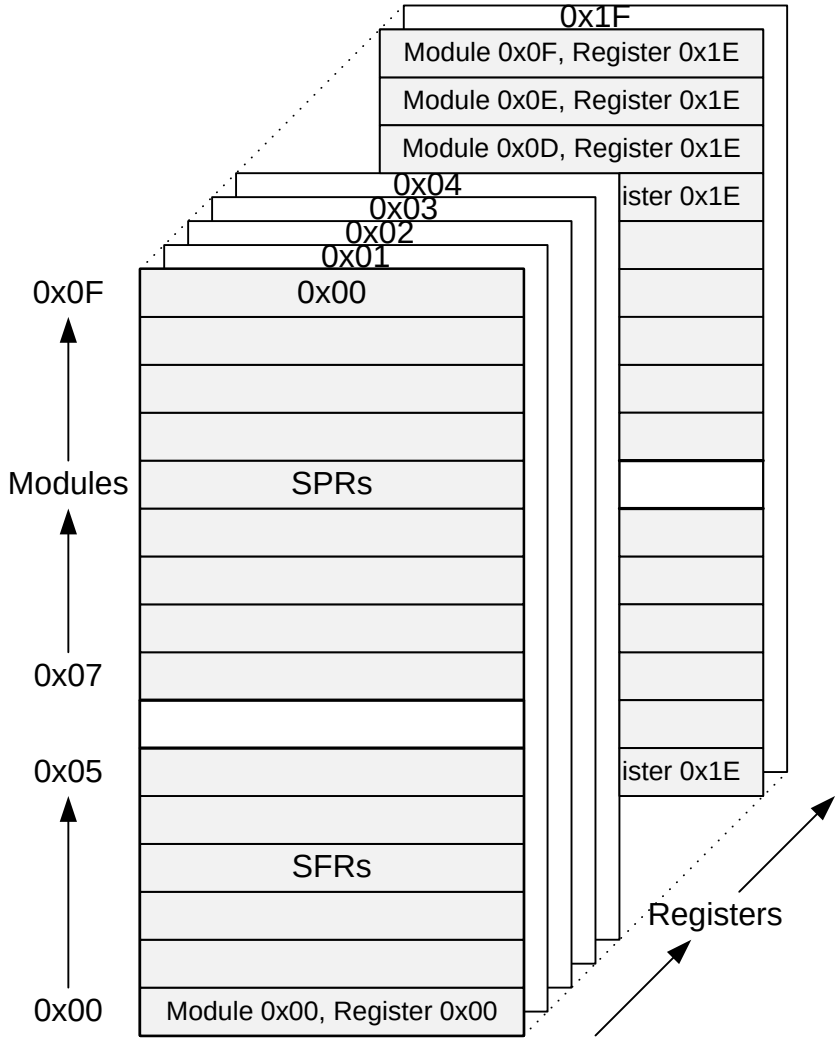


Figure 1. MAXQ30 Core Register Organization

System Registers

All system registers (SFR and SPR) are described in detail in the ZON PS3/PS3L/M3S/M3L hardware reference manual). Table 2 contains the addresses for the system registers.

Table 2. System Registers

	MODULE INDEX					
REGISTER INDEX	**(0h)**	**(1h)**	**(2h)**	**(3h)**	**(4h)**	**(5h)**
00h	I2CCN	PO0	MCNT	SCON0	MUXCN	RTCI
01h	I2CINT	PO1	MA	SBUF0	RMTCN	LCDINDADDR+
02h	I2CST	EIF0	MB	SCON1	RMTCMD	LCDINDDATA+
03h	I2CDATA	TB0CN	—	SBUF1	ADCN	TSW0CMP
04h	I2CMCN	TB1CN	MC0	SCON2	ADCFG	TSW0CN
05h	SPICN	TB2CN	MC1	SBUF2	U1CNT	TSW0CNT
06h	SPIST	TB3CN	U0CNT	SCON3	U1TR	TSW1CMP
07h	SPIB	TB4CN	U0TR	SBUF3	CEPCN	TSW1CN
08h	I2CRX	PI0	U0ST	DEMCN	U1ST	TSW1CNT
09h	I2CRXCFG	PI1	U0CK	DEMSAMP	U1CK	TMUXSEL
0Ah	I2CTX	EIE0	U0GT	SMD0	U1GT	RTCSEC
0Bh	I2CTXCFG	EIES0	MC0R	PR0	CECN	RTCSUB
0Ch	I2CSLA	CRCNT	MC1R	SMD1	CEI	RTCCAL
0Dh	I2CCKH	CRC1	UDESD	PR1	RMTDATA	RTCALARM
0Eh	I2CCKL	CRC2	UDESC	SMD2	RMTERR	TEMPCNTL
0Fh	I2CHSCK	TB0V	AESCTRL	PR2	ADCLK	RTCWAKE
10h	I2CTO	PD0	AESDATA	SMD3	ADMUX3	TEMP
11h	I2CFIFO	PD1	—	PR3	FIRLEN	TEMPALARM
12h	SPICF	TB0R	—	DEMTHR0	—	TCAB
13h	SPICK	TB0C	—	DEMTHR1	—	TCCD
14h	SYSCN	TB1V	—	DEMINT	—	WAKEFROM
15h	—	TB1R	—	—	RTM0	RTCCONT
16h	—	TB1C	—	—	RTM1	—
17h	TM2	TB2V	—	—	RTM2	—
18h	ICDT0	TB2R	—	—	RTM3	—
19h	ICDT1	TB2C	—	—	RMTTMP	—
1Ah	ICDC	TB3V	SWINT	—	RMTCTL0	TMPFPAR1
1Bh	ICDF	TB3R	FPARTN	—	RMTCTL1	LCDMAP0++
1Ch	ICDB	TB3C	MMOARY	—	RMTCTL2	LCDMAP1++
1Dh	ICDA	TB4V	MMO	TRNG	RMTCTL3	TMPFPAR2
1Eh	ICDD	TB4R	FCNTL	—	RMTSTAT	LCDMODE++
1Fh	TM	TB4C	FDATA	—	RMTRG	LCDCTL++

Memory Organization and Addressing

The MAXQ30 Core is a Harvard machine. As such, it has separate code and data memory spaces. In the MAXQ30 Core, each memory space is 32MB in length. When accessed as code, memory is organized as 16MB x 16 bits; when accessed as data, the memory space can appear as 32MB x 8, 16MB x 16, or 8MB x 32.

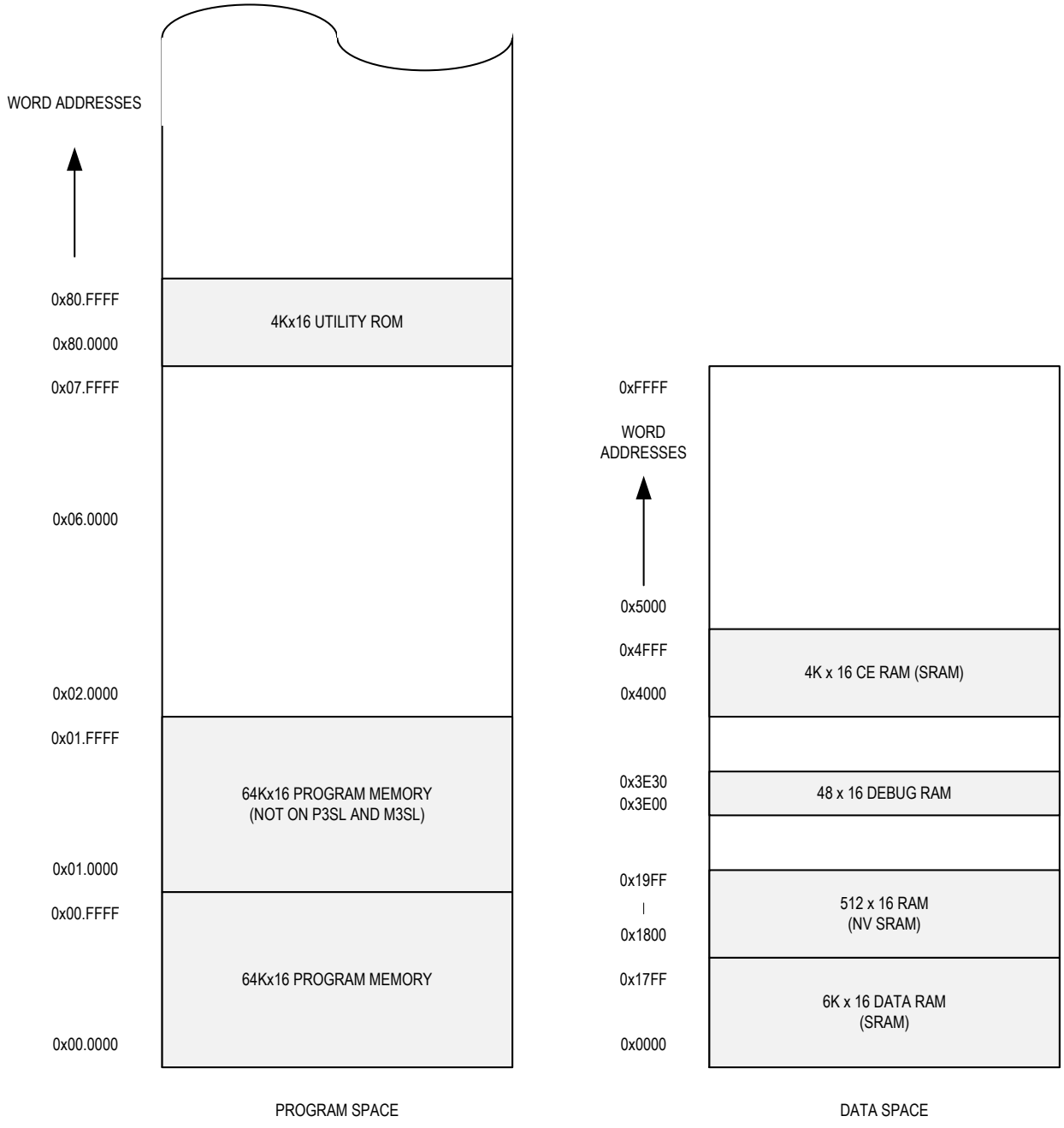


Figure 2. Memory Organization

Interrupts and Exceptions

The MAXQ30 processor supports multiple interrupts that transfer control to fixed vectors. Interrupt priority can be changed through programmable registers (see Table 3).

Table 3. Interrupts

MPU ADDRESS	NAME	DESCRIPTION
0x00 0000	MAIN	This is the main entry point. The utility ROM jumps here after performing device initialization and checks for loader mode or debug mode.
0x00 0008	PF	Power-Fail Warning. Activated when V_{3P3A} falls below the power-fail threshold.
0x00 0010	EI	External Interrupts. Activated when any enabled external interrupt pin becomes active. Software in the interrupt service routine must poll the available interrupt sources to determine which of the external interrupt sources caused the interrupt.
0x00 0018	CE	Compute Engine. Activated to alert the MAXQ30 Core when the Compute Engine has completed an accumulation cycle.
0x00 0020	I2C	I^2C. Activated when the I^2C peripheral detects an event: START completed, STOP completed, transmit buffer empty, receive character available or timeout fault.
0x00 0028	SPI	SPI. Activated when the SPI peripheral has clocked in/out one character.
0x00 0030	UART	UART. Activated when any UART has an exception condition: receive character avail- able, transmit buffer empty, parity fault or framing error.
0x00 0038	ISO0	ISO UART 0. Activated whenever an exception condition is detected on the smart card channel 0.
0x00 0048	WDT	Watchdog Timer. Activated when the watchdog timer is about to reset the device. This interrupt provides the MAXQ30 an opportunity to either reset the watchdog timer or to save status before the watchdog resets the MAXQ30 MPU core.
0x00 0050	TB	Timer B. Activated when an interrupt condition occurs on any timer channel. Inter- rupts can be an expiration of the timer or can indicate that a measurement is com- plete in pulse-width measurement mode.
0x00 0058	TRIM	Trim Check. Set if the fuse bits become corrupted for any reason. See the RTCI register in the RTC block for more information.
0x00 0060	RTC	Real-Time Clock. Activated when any interrupt source in the RTC block is activated, including alarm, voltage status, or temperature range.
0x00 0070	TOUCH	Touch Switch Interrupt. If enabled, this interrupt becomes active when the touch switch input is activated.
0x00 0078	CRYPTO	Crypto Interrupt. If enabled, this interrupt becomes active at the end of any crypto operation with interrupts enabled.
0x00 0080	REMOTE	Remote Interrupt. If enabled, becomes active when a remote interface has a sample ready or detects an error.
0x00 0088	TRAP	General Interrupt Trap. Activated whenever an interrupt not covered by any other condition occurs.

Debug

The MAXQ30 Core has an integrated debugger that allows real-time debugging of the code running on the MAXQ30 Core. The debugger contains a hardware component that connects to the JTAG port, and a software component that is contained in the utility ROM. The debugger supports multiple breakpoints, register inspection and modification, RAM dump and modify, and other functions.

Flash Memory

The ZON P3S/M3SL contains 128KB and the ZON P3S/M3S contains 256KB of on-chip flash memory that serves as program store for the MAXQ30 Core. The use of flash memory as program store allows the firmware to be easily updated. Because flash write and erase operations cannot be performed while code is executing from flash, code in the utility ROM mediates all flash write and erase operations. Because the MAXQ30 Core is a Harvard architecture processor, the core cannot access the memory block as data from which code is executing. This means that user code executing in flash space can- not directly access data stored in flash memory. However, facilities provided in the utility ROM allow access to data stored in the flash memory.

Utility ROM

The devices contain an 8KB ROM organized as 4K x 16 to provide boot services and utility functions to the application program running in flash. This block of memory resides at 0x80 0000 in code space. The utility ROM man- ages the following functions:

Boot: Execution begins from reset at the base of the utility ROM. Under normal circumstances, a jump is executed to the base of flash memory, but under special circumstances, some other code block can take the execution thread (e.g., boot loader, debug, etc.).

Debug: The utility ROM contains routines that assist the built-in hardware debugger to communicate with ICE software on a PC.

Bootloader: The bootloader provides in-system programming facilities. Integrated debug-environment software with the appropriate drivers can invoke the bootloader directly to write code blocks to the flash memory.

Utility Functions: Functions such as flash programming and block moves are provided in the utility ROM to assist user software.

Test: Functions used to perform unit test of the devices are included in the utility ROM.

Boot Sequence

At power on, the MAXQ30 MPU core begins executing the Utility ROM boot code at location 0x80 0000. Broadly, the device performs the following actions before branch- ing to user code:

Determine if the loader has requested control. The loader is invoked by setting a bit in a register through the JTAG interface. If this bit is set, the utility ROM does not jump to user code, but begins running the loader.

If the loader is not to be invoked, the utility ROM reads the 32-bit value at byte address 0x00 0000 and loads this value into the stack pointer.

The utility ROM then reads the 32-bit value at byte address 0x00 0004 and loads that value into the PC register, effectively performing a jump to the address.

User code must contain code at addresses 0x00 0000 and 0x00 0004 that corresponds to the desired stack location and the main entry point, respectively

Table 4. MAXQ30 Memory Spaces

MPU ADDRESS	NAME	DESCRIPTION
CODE SPACE (Word Addresses)		
0x00 0000	FLASH	128K x 16 flash program memory (P3S/M3S) 64K x 16 flash program memory (P3SL/ M3SL)
0x80 0000	UROM	4K x 16 utility ROM
DATA SPACE (Word Addresses)		
0x00 0000	DRAM	6K x 16 static RAM for MCU data
0x00 1800	NVDRAM	512 x 16 static, nonvolatile RAM for MCU data (supported by V_{BAT_RTC})
0x00 3E00	DBRAM	48 x 16 MAXQ30 debug RAM
0x00 4000	CERAM	4K x 16 shared memory for CE data (non-volatile if V_{BAT} and V_{BAT_RTC} present in LCD_ONLY mode)

Binary Loader

The utility ROM includes a binary loader module that can be used to load, verify, dump and erase the code image in flash memory. In general, it is unnecessary for a developer to directly interact with the loader. Development software and associated drivers communicate directly with the loader and provide a simplified interface to the developer.

Details on the loader commands and on the utility ROM in general can be found in the P3S/P3SL/M3S/M3SL HRM (Hardware Reference Manual).

RAM

The devices contain a total of 21KB of RAM (not including the 96 bytes of RAM dedicated for the debug function). Of this total, 12KB is dedicated to the MAXQ30 Core for its internal operation. This RAM block is maintained in the absence of primary power by the V_{BAT} power supply. An 8KB RAM block is dedicated for CE code and data RAM, and it is accessible at will by the CE and by the MAXQ30 Core through interleaved access; it is backed up in LCD_ONLY mode if both V_{BAT} and V_{BAT_RTC} are present. Implemented as static RAM, all accesses to internal memory require only one clock cycle.

A 1KB block of RAM is non-volatile and supported by V_{BAT_RTC} in SLP mode.

Power

ZON P3S/P3SLM3S/M3SL require a single 3.3V supply for operation. In most cases, two battery supplies are attached to the device as well: a battery that provides operational power when primary power fails, and a second battery that maintains internal RAM and clock facilities. How these supplies interact and what blocks are powered at what times is covered in the *Operational Modes* section.

Operational Modes

The devices support four operational modes:

Mission Mode: The devices are in mission (MSN) mode when the primary power supply is in specification. Primary power is supplied through the V_{3P3SYS} and V_{3P3A} pins. Comparators on the V_{3P3SYS} pin monitor the voltage level on this bus. If the level falls below a set threshold, the part automatically switches to brownout mode.

Brownout Mode: In brownout (BRN) mode, V_{3P3SYS} has failed and main power for the I/O and other circuits automatically switches to the V_{BAT} input. Since there is no path for power to flow from V_{BAT} to the metrology blocks, these blocks are effectively turned off. The core continues to operate at full speed until firmware switches to another mode.

LCD Only: In LCD-only mode, the core is halted, and the core voltage regulator is disabled, and the LCD operates independent of software control. The LCD can take its power from either V_{BAT}, the V_{LCD5} pin (from an external charge pump), or from an external V_{LCD} supply, depending on the LCD configuration.

SLP: SLP mode shuts down power to all logic blocks except the RTC and nonvolatile memory blocks. Internal events plus four level-sensitive pins (PB_WAKE) and six edge-sensitive pins (PU_WAKE) can take the part from SLP mode to BRN mode.

There are 10 pins that are used to provide power or to provide a bypass point for internal power nodes:

V_{3P3A}: This is the primary analog power input for the device. It provides power to the ADC blocks, the voltage comparator blocks, and to the bandgap voltage reference and its output buffer. This block is not directly backed up by any on-chip battery.

V_{3P3SYS}: This is the primary digital power input for the device. It is typically connected to the same supply as V_{3P3A}, but separately bypassed.

V_{BAT}: The primary battery supply input. This input is selected to provide system power when the V_{3P3SYS} circuit falls below its threshold level.

V_{3P3D}: The output from an internal switch that selects either V_{3P3SYS} (if the primary supply is above threshold) or V_{BAT} (if the primary supply is below threshold). It should always be bypassed, but it can also be used to provide power to low-power external devices such as serial memory during brownout conditions.

V_{LCD}: Usually, this is a bypass point for the LCD supply. Frequently the supply is the LCD DAC, although it can also be the currently selected V_{BAT} or V_{3P3SYS} supply, directly. This pin can also be used as an input to provide an external V_{LCD}.

V_{LCD5}: An input from a charge pump if operation with 5V-compatible LCD glass is desired. In one LCD mode, a square wave is available to drive a charge pump so that only an external RC circuit and two diodes are required to provide a 5V supply.

V_{BAT_RTC}: This pin provides the RTC and nonvolatile memory backup power. It is frequently connected to a lithium battery to maintain the RTC and NV memory elements.

V_{3P3RTC}: The bypass for the nonvolatile power bus.

V_{DD_CAL}: The bypass point for the internal calibration power bus.

V_{DD}: The bypass point for the internal regulated core power supply. Internally, there are four voltage regulators and eight power switches that control the power distribution system. Some of the switches are controlled by software and the others are controlled by internal logic that senses the voltage on the external pins and makes automatic decisions about the appropriate configuration. Internally, there is a set of power busses: four primary busses that provide power to various parts of the device logic, two busses dedicated to the LCD functions, and two dedicated to the ADC section and to the remote interfaces.

Power Status Registers

The power status that the device is in is reflected in the

VSTAT field of the RTCI register.

VSTAT: This field reflects the status of the supply voltage level comparators (Table 6)

When the value of VSTAT changes, the RTC_I_VS bit is set. If the RTC_M_VS bit is also set (and interrupts are enabled globally) the MPU is interrupted. In this way, the MPU is notified both when power is failing and when power is restored.

Clock System

ZON M3S/P3S is normally clocked by an external 32,768Hz watch crystal that serves as the sole time base for the device. An internal PLL multiplies the reference frequency by 1800 to generate the 58.9824MHz master clock. A prescaler with multiple taps is used to generate the clock for the various on-chip peripherals and subsystems.

The device includes an internal backup oscillator. A failure detection block ensures that, upon loss of the 32kHz crystal, one internal oscillator provides the device a backup clock of a 32kHz oscillator.

The clock rate for the MAXQ30 MPU core and the peripherals is selectable through the CD field in the CKCN register. Table 7 shows the selectable clock rates.

An additional stop mode for the MAXQ30 code and associated peripherals in also featured. By setting the STOP bit in the CKCN register, the MAXQ30 clock is halted. The normal operation can be resumed upon a power-on or reset. The STOP mode can be exited utilizing digital I/O properly configured.

The Compute Engine (CE) operates at a fixed clock rate of 1/3 of the PLL master clock or 19,660,800Hz. The main ADC clock setting is selectable through the CKSPD field in the ADCLK register. Table 8 shows the selectable clock rates.

Table 6. Power Status

VSTAT VALUE	MEANING
0b00000	Power is good, all systems can function.
0b00001	Metrology is inaccurate, but all digital functions can operate.
0b00011	Low power warning. Power supply is below detection threshold, but digital operation is still reliable. Code should begin taking steps to conserve power.
0b00111	SLP bit shortly. No flash memory writes from this point. Final power warning to MAXQ30 MPU. The V_{DD} regulator is at the limit of regulation and regulated power will begin to sag from this point. The MAXQ30 MPU must set the SLP bit shortly. No flash memory writes from this point.
0b01111	V_{DD} out of range. The MAXQ30 MPU will never see this value. The power management system declares BADVDD if this state is reached before the MAXQ30 MPU sets the SLP mode.

Table 7. MAXQ30 Clock Speed

CD[1:0]	DIVIDER	CLOCK SPEED (MHz)
0	1	19.6608
1	2	9.8304
2	8	2.4576
3	16	1.2288 MHz

Table 8. ADC Main Clock Speed

CKSPD[1:0]	*FREQUENCY*
0	*Reserved*
1	*491.52kHz (ADCVLS = 1)*
2	*983.04kHz (ADCVLS = 1)*
3	*Reserved*

Peripherals

UART

The ZON P3S/P3SL/M3S/M3SL SoCs contain four UART channels. All channels are directly controlled by the MAXQ30 Core and feature independent baud rate generators. These baud rate generators are independent from any timer, and they are independent from each other.

UART0 is unique in that it contains an option to modulate its output with a high-frequency carrier (nominally 38kHz) and contains a photodiode amplifier and detector that allows the channel to sense high-frequency carrier and demodulate serial data contained on the carrier.

Each UART features:

- Double-buffered transmitter and receiver
- Odd, even, or no parity
- 1, 1½, or 2 stop bits
- Maskable interrupts for receive buffer full or transmit buffer empty

The UART modes of operation are summarized in Table 9.

I²C

The ZON P3S/P3SL/M3S/M3SL SoCs include an I²C peripheral that can act as an I²C master or slave. The I²C bus is a bidirectional two-wire serial bus inter- face. It has the following characteristics:

- Information is transferred over a serial data circuit (SDA) and serial clock circuit (SCL).
- The peripheral can operate in either a master mode or a slave mode.
- The peripheral supports either standard (7-bit) ad- dressing or extended (10-bit) addressing.
- The peripheral operates in three modes to support multiple transfer rates.
- Standard mode: 100kbps
- Fast mode: 400kbps
- Fast mode plus: 1Mbps
- The peripheral contains an on-chip filter to reject spikes on the data circuit.

The I²C port of the device offers the following features:

- Single-master, multi-master, or slave operation
- Clock stretching
- Timeout detection
- Separate transmit FIFO (TX_FIFO) and receive FIFO (RX_FIFO) with selectable thresholds
- Automatic response to general call address (0000 0000) used for broadcasting
- Interactive receive (Rx) mode
- Direct control of SCL and SDA signals
- Interrupt on errors

SPI

The serial peripheral interface (SPI) provides an independent serial communication channel to communicate synchronously with peripheral devices in a multiple master or multiple slave system. The interface provides access to a four-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection is provided when two or more masters attempt a data transfer at the same time. The maximum data rate of the SPI is up to the system reference clock frequency for master mode. For slave mode, the maximum frequency is a function on the I/O driver, character length and the system clock.

The main element in the SPI module is the block containing the shift register, the transmit FIFO and the receive FIFO. The shift register is double buffered and serves as temporary data storage. The receive FIFO holds received data from the network. The transmit FIFO contains data ready to be transmitted out.

The SPIB SFR provides access for both transmit and receive data. Reads are directed to the read FIFO. Writes are directed to the shift register automatically if the transmit FIFO is empty; otherwise, write operations store data into the transmit FIFO.

The four interface signals used by the SPI are MISO, MOSI, SCLK, and SSEL:

Table 9. UART Operational Modes

SM0:SM1	MODE	FUNCTION	BAUD CLOCK	LENGTH	FRAMING	THE 9TH BIT
00	0	Synchronous	4 of 12 clocks	8	None	None
01	1	Asynchronous	BRG	10	1 start, 1 stop	None
10	2	Asynchronous	32 or 64 clocks	11	1 start, 1 stop	0, 1, parity
11	3	Asynchronous	BRG	11	1 start, 1 stop	0, 1, parity

MISO – Master In/Slave Out. This signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. Data is transferred most significant bit first. The slave device places the MISO pin in an input state with a weak pullup when it is not selected.

MOSI – Master Out /Slave In. This signal is an output from a master device and an input to the slave devices. It is used to serially transfer data from the master to the selected slave. Data is transferred most significant bit first.

SCLK – SPI Clock. This serial clock is an output from the master device and an input to the slave devices. It is used to synchronize the transfer of data between the master and the slave on the data bus.

SSEL – Slave Select. The slave select signal enables a SPI slave when activated by a master device. The slave can be configured to select the active state of SSEL. When the master asserts SSEL it is signaling the beginning of an SPI transfer. SSEL should remain asserted for the duration of the transfer. Normally, this signal has no function in master mode and its port pin can be used as a general-purpose I/O. However, the SSEL can optionally be used as a mode fault detection in master mode.

The SPI peripheral is enabled by setting the SPI enable bit (SPIEN in the SPICN register). The master mode bit (MSTM in the SPICN register) selects the operating mode – either master or slave – and the source of the SCLK signal.

The slave select (SSEL) input of a slave device must be externally asserted by a master before the master device can exchange data with the slave device. The active state of SSEL is determined by the slave active select bit (SAS in the SPICF register). If SAS is cleared, SSEL is active low and must be held low for the duration of the transaction. If SAS is set, SSEL is active high and must be held high for the duration of the transaction. De-asserting the SSEL signal during a transfer cycle aborts the transaction.

The SPI transfer format is determined by the SPI clock polarity bit (CKPOL) and the clock phase bit (CKPHA). CKPOL selects an active polarity of SCLK. CKPHA selects which edge of the clock—the leading or trailing edge—is used to clock data into the shift register. Together, the clock polarity bit and the clock phase bit provide the flexibility for direct interfacing of most existing synchronous serial peripheral devices.

The SPI specification describes four data transfer modes:

Mode 0 (CKPOL = 0, CKPHA = 0): The SCLK circuit idles in the low state. Data is transferred on the leading edge of the clock (the rising edge.) Data may change on the falling edge of the clock (the trailing edge). Since the first clock edge transfers data, data must be set up prior to the first clock edge (typically coincident with the assertion of the SSEL signal).

Mode 1 (CKPOL = 0, CKPHA = 1): The SCLK circuit idles in the low state. Data is transferred on the trailing edge of the clock (the falling edge.) Data may change on the rising edge of the clock (the leading edge). Since the first clock edge does not transfer data, data can be set up on the leading edge of the clock.

Mode 2 (CKPOL = 1, CKPHA = 0): The SCLK circuit idles in the high state. Data is transferred on the leading edge of the clock (the falling edge). Data may change on the rising edge of the clock (the trailing edge). Since the first clock edge transfers data, data must be set up prior to the first clock edge (typically coincident with the assertion of the SSEL signal).

Mode 3 (CKPOL = 1, CKPHA = 1): The SCLK circuit idles in the high state. Data is transferred on the trailing edge of the clock (the rising edge). Data may change on the falling edge of the clock (the leading edge). Since the first clock edge does not transfer data, data can be set up on the leading edge of the clock.

Note that it is not advisable to change the SPI operation mode or configuration when the SPI peripheral is in operation. Software should disable the SPI peripheral (clear SPIEN) before changing the mode of operation (CKPOL, CKPHA, CHR, MSTM, and SAS). Unpredictable behavior will result if the SPI operation mode is changed while the SPI peripheral is enabled.

Set the SPI peripheral in master mode when the micro- controller needs to manage an external peripheral or memory device. The master establishes the transfer rules and the transfer rate.

Only an SPI master device can initiate a data transfer. Master transfer starts when the SPI master writes to SPI buffer register (SPIB). The SPI master immediately shifts out the data serially on the MOSI pin, most significant bit first, while driving the serial clock on SCLK. New data is simultaneously gated in on the MISO pin into the least significant bit of the shift register.

The data transfer rate for the network is determined by the divider ratio set in the SPI clock register (SPICK).

In master mode, the SSEL pin of the master defaults to general-purpose I/O pin. However, the SSEL can be used for mode fault detection input, if the mode fault enable bit (MODFE in the SPICF register) is set. When the SPI is configured as a master and the SSEL pin is used as mode fault detection input, a mode fault condition occurs if an active signal is detected on SSEL. This indicates that some other device on the network is attempting to be a master

The active state of the SSEL pin is defined by the slave active select (SAS) bit. When MODFE is set and SAS is cleared, an active low signal on SSEL triggers a mode fault. If MODFE is set to 1 and SAS is set, an active-high signal on SSEL indicates a mode fault condition. Either way, the master device senses the error and immediately disable the SPI device to avoid bus contentions.

The mode fault error is usually caused by two SPI devices attempting to function as master at the same time. In the case where more than one device is configured as master at the same time, the resulting bus contention may cause permanent damage to push-pull CMOS drivers. Mode fault error detection is provided to protect to the device by disabling the bus drivers. When a mode fault is detected, the following actions are taken immediately:

- The MSTM bit is forced to 0 to reconfigure the SPI device as a slave.
- The SPIEN bit is forced to 0 to disable the SPI device.
- The mode fault bit (MODF) status flag is set. When set, the MODF bit can generate an interrupt if the mode fault interrupt enable bit (MODFIE) is set to 1.

The application software must correct the system conflicts before resuming normal operation. The MODF flag is set automatically by hardware, but it must be cleared by software or a reset once set. Setting the MODF bit to a 1 by software causes an interrupt if enabled.

To avoid unintentional mode fault error, software should check the status of SSEL prior to enabling the SPI peripheral as master. Otherwise, if the SSEL signal is in the active state a mode fault error occurs, disabling the SPI peripheral and clearing master mode.

Note that the mode fault mechanism does not provide full protection from bus contention for multiple master systems. For example, if two devices are configured as master at the same time, the mode fault detect circuitry does not help to protect either device driver unless one of them selects the other as slave by asserting its SSEL signal. Also, if a master activates more than one slave (e.g., due to a software fault) and those devices try to simultaneously drive their output pins, bus contention can occur without generating a mode fault error.

Select slave mode when another device is configured as the master and the role of the device is as a peripheral to another device. The SPI is in slave mode when the MSTM bit is cleared. In slave mode, the SPI controller is dependent on the SCLK sourced from the master to control the data transfer.

The slave select (SSEL) input of a slave device must be externally asserted by a master before data exchange can take place. SSEL must be asserted before the data transaction begins and must remain asserted for the duration of the transaction. If data is to be transmitted by the slave device, it must be written to its shift register before the beginning of a transfer cycle, otherwise the character already in the slave's shift register is transferred. For the slave device, a transfer begins with the first clock edge or the active SSEL edge, dependent on the state of CKPHA.

The active edge of SSEL is determined by the slave active select bit (SAS in the SPICF register). When SAS is cleared the falling edge of SSEL edge is the active edge. If SAS is set, the rising edge of SSEL is the active edge.

The SPI master transfers data to a slave on the MOSI pin, most significant bit first, and the selected slave device simultaneously transfers the contents of its shift register to the master on the MISO pin, also most significant bit first. Data received from the master replaces data in the slave's shift register at the completion of a transfer. Just as in the master mode, received data is loaded into the receive FIFO and the SPI receive interrupt flag is set at the end of the transfer. The setting of the SPIRXI flag can cause an interrupt if enabled.

When SSEL is not asserted, the slave device ignores the SCLK clock and the shift register is disabled. In this condition, the device is idle, no data is shifted out from the shift register and no data is sampled from the MOSI pin. The MISO pin is placed in input mode with a weak pullup to allow other devices on the bus to drive the bus. De-asserting the SSEL signal by the master during a transfer indicates that the current process is aborted, and it causes the slave logic and its bit counter to be reset, no data is loaded to the receive FIFO.

In slave mode, the clock divide ratio bits in the SPI clock register (SPICK) have no function. However, the transfer format and the character length selection for the slave device should match the selection of the master for proper communication.

For master mode operation, the data rate is determined by the clock divide ratio specified in the SPI clock register (SPICK). The SPI module supports 256 different clock divide ratios for serial clock generation.

For a standard system frequency of 9.8304MHz, the fastest SPI data rate is 9.8304Mbps and the slowest data rate is 9.8304MHz/(2 x 256) = 19.2kbps.

If the SPI peripheral is configured as a slave, it receives the SPI clock on the SCLK pin from the master device. The setting of the SPICK register has no effect on the data rate of the network. The maximum slave SCLK is:

$SCLK_{max} = f_{SYSCLK}/4$

The character length bit (CHR in the SPICN register) specifies either a 8-bit or 16-bit data character for a transfer cycle. When CHR is clear, the character length is 8 bits; when CHR is set, the character length is 16 bits.

The FIFO depth depends on the value of CHR. The FIFO is 64 bits, so it can accommodate 8 characters of 8-bit character length before overrun (CHR = 0), or 4 characters of 16-bit character length before overrun (CHR = 1).

The SPI buffer register (SPIB) is 16 bits wide to accommodate 16-bit characters. When operating in 8-bit character width mode (CHR = 0) software must write to the lower 8 bits and read from the lower 8 bits. The upper byte is not used when CHR = 0.

At the end of a character transfer, the received data is loaded into the receive FIFO for reading by the MAXQ30 MPU core and the SPI receive interrupt (SPIRXI) is set. This generates an interrupt if the SPI receive FIFO interrupt enable bit (SPIRXIE) is set. Software can retrieve the received character by reading from SPIB. If no more characters are available in the receive FIFO, the SPIRXI flag automatically clears. If there are more characters available, the SPIRXI flag remains set.

The SPI port supports the following features related to receive operation:

- Indication of the number of characters received
- FIFO half-full and full flags with interrupt generation
- FIFO overrun flag with interrupt generation
- FIFO reset function

Software writes data to be transmitted to the SPI data buffer register (SPIB). If the shift register is empty, data is written directly to the shift register. Once the shift register is busy transmitting data, additional writes to the SPIB register is transferred into the transmit FIFO.

The transmit FIFO full flag (SPITXFI) is set when the transmit FIFO is full. This generates an interrupt if the SPI transmit FIFO full interrupt enable bit (SPITXFIE) is also set. The SPITXFI flag is automatically cleared when data is loaded from the transmit FIFO into the shift register.

The SPI port supports the following features related to transmit operation:

- Transmit FIFO overrun flag with interrupt generation
- FIFO transmit interrupt
- FIFO empty flag with interrupt generation
- FIFO clear register

After the SPI controller loads the last data byte from the transmit FIFO to the shift register the transmit FIFO empty flag (SPITXEI) is set. This generates an interrupt if the SPI transmit FIFO empty interrupt enable bit (SPITXEIE) is set. The SPITXEI flag is automatically cleared when the transmit FIFO is no longer empty (that is, software provides more transmit data) or by software writing ‘0’ to the SPITXEI flag. Since the SPITXEI flag is set when the last character is loaded into the shift register, it does not indicate that the SPI buffer is empty; there is still one more character to shift out. To ensure that the SPI buffer is empty, software should monitor the SPITXI flag.

ISO 7816 UARTs

The ZON P3S/P3SL/M3S/M3SL SoCs contain two ISO7816 compatible UART channels for connection to a smart card interface. The ISO UART provides a bidirectional I/O circuit and a separate clock circuit. The ISO UART has the following features:

- Supports half-duplex asynchronous transmission.
- Programmable baud rate.
- Eight-character FIFO with parity detect/transmit.
- Error management for T = 0 protocol (stream).
- Extra guard time between characters on transmit.

Touch Sensor Inputs—General Description

The ZON P3S/P3SL/M3S/M3SL SoCs contain two capacitive touch switch inputs. These inputs are designed to operate with a wide range of quiescent capacitance values and are generally immune from most noise sources.

As a finger approaches the touch plate, the capacitance of the touch plate increases, and the frequency decreases. In some cases, the change in capacitance (and frequency) can be as much as two orders of magnitude. Note that the touch plate itself is never actually touched. The plate is covered by a dielectric (e.g., plastic) and the finger only touches the exterior of the dielectric. This makes the switch more of a proximity switch than a touch switch.

Digital logic is used to sense the change in frequency. To do this, the touch switch oscillator is gated on for a known period, and the pulses from the oscillator clock a ripple counter. As the capacitance increases, the frequency of the oscillator decreases, and the count recorded also decreases.

Because the system must sense the decrease in the count, a reference count is needed to determine when the frequency falls below some threshold and to determine when a finger is near the touch sensor. This reference count is stored in a compare register loaded by software running on the MAXQ30 Core. A digital comparator determines whether the count is above or below the compare register threshold and emits an interrupt if the count is below the threshold.

A block of logic clocked by the 32kHz RTC oscillator manages the touch switch process. The state machine runs every 250ms. This is sufficient to manage a touch switch but would be too slow for (for example) a typewriter keyboard. By performing a scan so slowly, energy is saved.

Before the touch switch is used, the compare register must be calibrated. To do this, the MAXQ30 Core enables the touch switch and reads the count register after the first measurement cycle without a finger near the touch plate. The MAXQ30 Core then reduces this value by some amount (possibly through one shift right to reduce the value by half) and store that reduced value into the compare register. From that point, an interrupt to the host occurs only when the count register contains a value less than the compare register.

A two-bit period value is included in the IP block. This value selects one of several sample periods for the oscillator:

The sample period is variable to account for different touch plate arrangements that may have a capacitance different from the nominal value.

The enable input enables the state machine logic to operate. When enable is inactive, gate is held low, clear is held active and read is held inactive. When enable is active, the state machine logic runs every 8192 of the 32kHz clock cycles.

Table 10. Touch Switch Sampling Timing

PERIOD VALUE	SAMPLE PERIOD
0	2 (61µs)
1	4 (122µs)
2	8 (244µs)
3	16 (488µs)

The overflow indication informs the host MAXQ30 Core that an overflow event has occurred. Under an overflow condition, the count does not accurately reflect whether a touch event has occurred. The host should recalibrate the system with a shorter sample period.

The touch switch can interrupt and wake the MAXQ30 MPU as well. The CMPIE bit in the TSWxCN register must be set to enable the interrupt and establish the CMPI bit as a wake source.

Hardware Considerations

The touch sensor is a capacitance sensor. That means the sensor will respond to any change in capacitance, whether it is from a finger or from any other source. It is important that the conductors from the sensor pin to the sensor plate be kept short and direct and generally far away from other conductors.

Another consideration is the nominal capacitance of the circuit. Broadly speaking, the smaller the stray capacitance can be, the more sensitive and more accurate the touch sensor will be. If the nominal stray capacitance is (for example) 1000pF, and the change due to a finger presence is 200pF, it is much more difficult to sense this reliably then if the nominal stray capacitance is, say, 10pF.

A final consideration is oscillator drift due to elements unrelated to the plate capacitance. The oscillator is relatively stable, but still has some variation due to temperature and supply voltage variations. It might be prudent to recalibrate the sensor from time to time.

Temperature Sensor

The device contains a temperature sensor that is characterized at the factory at +22°C. The value of the temperature sensor at this temperature is stored in a reserved area of the device.

The final value in the accumulator is the temperature sensor value at +22°C. Since the raw temperature sensor returns a value in its STEMP register that is proportional to absolute temperature, one can use this value to determine the proportionality constant for the temperature sensor.

The STEMP value is a two's complement value; values less than zero reflect temperatures below +22°C.

Optical Demodulator

The optical demodulator uses the multiplexer, the modulator and decimator blocks of the auxiliary ADC. When the optical demodulator is active the auxiliary ADC is therefore unavailable. The optical receive input is selected by setting the AUX_ADC_SEL bits in the LCDCTL register to 3 and by clearing the DEM_AUX_B bit.

The signal from the auxiliary ADC is first decimated, and the decimator output is mixed with a local oscillator operating at 38kHz. The correlation output of the mixer is then filtered and passed to a discriminator with variable hysteresis limits. The output of the discriminator is then passed to UART0. UART0 can also be supplied directly from the RX0 pin by setting DEMOD_DIS bit to 1. See the description of the auxiliary ADC for details.

Optical Modulator

The optical modulator is available on UART0. If enabled, the output of timer 0 is logically summed with the UART transmit data output before being presented to the transmit data pin.

The modulator is enabled by setting the EIR bit in the SMD0 register. When this bit is set, a SPACE condition is represented as a modulated output, and a MARK condition can be a logic low or high, depending on the setting of the OFS bit in the SMD0 register.

In virtually all IR transmitter configurations, the desire is to modulate the output during SPACE and to emit no IR during a MARK condition. This is because that traditional asynchronous communications idles in a MARK condition, and it is desirable to emit no radiation in the idle state. Consequently, all IR modes transmit IR during a SPACE condition.

Table 11. UART0 Operation Modes

UART OUTPUT	EIR	OFS	PIN OUTPUT
0	0	X	0
1	0	X	1
0	1	0	Modulated
1	1	0	1
0	1	1	Modulated
1	1	1	0

OFS = 1 should be used for connecting an LED directly to the port pin. In this configuration, the cathode of the LED is connected to the port pin and the anode of the LED to 3.3V through an appropriate current limiting resistor. Since the current sink capability of the port pin is able to drive high-efficiency IRED devices, this is the least expensive way to implement the IR transmitter.

If more output power is required, an NPN driver can be used to buffer the port output. In this case, the OFS register is set to 0 and the base of an NPN transistor is driven from the port pin. The LED is in the collector circuit, again, with the appropriate current limiting resistor.

Timer channel 0 controls the modulation frequency. Software must configure the timer to operate at twice the expected modulation frequency since the timer output is squared by one additional flip-flop stage.

Auxiliary ADC

In addition to the metrology channels, the ZON P3S/P3SL/M3S/M3SL SoCs contain a 10-bit auxiliary ADC with up to four multiplexed inputs. This block is also used for to condition the optical receiver input.

The auxiliary ADC is a 10-bit ΔΣ converter operating at a modulator rate of 5MHz and a fixed oversampling rate that provides a final conversion rate of 4,800 samples per second. Any one of two pins (pins 57 and 56) can be used as AUX ADC inputs for P3S/P3SL. Any one of four pins (pins 56–59) can be used as AUX ADC inputs for M3S/M3SL.

Seven pins can be configured to be used as auxiliary ADC inputs, and one pin at a time is selected with a multiplexer that is controlled with the AUX_ADC_SEL bits in the LCDCTL register. Table 12 shows the allocation of ADC inputs to device pins and the AUX_ADC_SEL field.

Writing the value 1–4 into the AUX_ADC_SEL field selects the indicated pin as the ADC input. Any value other than 1–4 disables all ADC inputs, and all pins revert to their alternate functions.

Table 12. Auxiliary ADCs

AUX ADC INPUT	PIN	AUX_ADC_SEL[2:0]	ALTERNATE PIN FUNCTION(S)
—	—	0	—
0	59	1	GPIO port 1 bit 16
1	58	2	GPIO port 1 bit 17
2	57	3	Optical receive (Rx), wake input 3
3	56	4	Optical transmit (Tx)

Configuring the AUX ADC

If the optical demodulator is not in use, software should clear the DEM_AUX_B bit. When the optical demodulator is used, this bit must be set. Clearing the DEM_AUX_B bit will route the incoming modulator bits to a $sinc^3$ filter, the output of which will be the finished samples that can be read from the AADCDATA register.

Using the AUX ADC

Bit 15 in the RTMCN register selects the clock for the auxiliary ADC. In addition, bit 0 in the DEMINT register must be set. A conversion of the auxiliary ADC is started by setting bit 0 in the AADCST register. The most recent finished sample is available in the DEMSAMP register. The AUXDONE bit in the DEMCN register indicates that a sample is available in the AUXOUT[20:0] bits of the DEMSAMP register. To use the AUXDONE bit, software must clear the bit after each sample. Software cannot set this bit. Only the ADC hardware can set the bit when a new sample has arrived.

The formula for determining the measured voltage V from the ADC value n is:

If n > 2,097,152

$$V = 3.684\left(\frac{n}{2097152} - 1.5\right)$$

else

$$V = 3.684\left(\frac{n}{2097152} + 0.5\right)$$

CRC Generator

The ZON P3S/P3SL/M3/M3SL contains a CRC generator for computing check words for most popular communication protocols. It generates 16-bit CRC with a polynomial of 0x8005 ($x^{16} + x^{15} + x^2 + 1$) or a 32-bit CRC with a polynomial of 0x04C11DB7 ($x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$).

There are three registers that pertain to the CRC generator. The *CRCNT* register provides control to the CRC generator peripheral, and the *CRC1* and *CRC2* registers provide the input and output ports for the CRC generator.

A configuration bit selects either byte or word interface mode for reads from and writes to the CRC generator peripheral.

GPIO General Description

The ZON P3S/P3SL/M3S/M3SL contains several pins that can be configured as digital I/O, either as peripheral pins or as direct-write general-purpose I/O. When assigned to a peripheral, these pins are automatically configured for the selected peripheral. When assigned for general-purpose I/O, the user can select from different configurations.

Table 13. DIO Registers

REGISTER	ACCESS	DESCRIPTION
PO	R/W	Port Output register
PI	R/W	Port Input register
PD	R/W	Port Direction register

In the P3S/P3SL/M3S/M3SL, there are two 32-bit GPIO ports each of which can be controlled by three registers. Each bit is individually configurable for input, output or bidirectional modes.

The GPIO pins can be operated in the following configurations:

- Output: The GPIO pin either pulls low or high (totem pole configuration) to control an external component.
- Input: The GPIO pin is unconnected, and an external source can drive the pin low or high

GPIO pins can also be operated in open-drain mode. In this mode, and external source can pull the voltage at the pin up, if it is not driven low by the ZON P3S/P3SL/M3S/ M3SL. This mode is not selectable as a separate operation mode, but open drain GPIO pins can be implemented as follows:

- The Port Output register (PO) is configured as zero.
- The Port Direction register (PD) is set to output (1) for the GPIO pin to pull low.
- The Port Direction register (PD) is set to input (0) for the GPIO pin to be unconnected.

GPIO Interrupts

Port 0 bits 7:0 also support external interrupt. All external interrupts of the device are edge triggered, and the active edge is configurable.

To enable external interrupts, set the bits in the EIE0 register that correspond to the pins you wish to cause an interrupt. One can also set the bits in the EIES0 register to select the active edge: write a '0' to enable the rising edge and write a '1' to enable the falling edge.

When the selected edge occurs on a pin configured for an interrupt, and if the interrupt is enabled, the corresponding bit will be set in the interrupt flag register (IEF0). If interrupts are globally enabled (that is, IGE = 1), an interrupt is generated to the MAXQ30 Core.

Hardware Watchdog Timer

An independent, robust, fixed-duration, watchdog timer (WDT) is included in the ZON P3SX/M3SX SoCs. It uses the RTC crystal oscillator as its time base and must be refreshed by the MAXQ30 Core firmware at least every 1.5s. When not refreshed on time, the WDT overflows and the part is reset as if the RSTN pin were pulled low, except that the I/O RAM bits are in the same state as after a wake-up from SLP modes. After the WDT reset, the MAXQ30 MPU core is launched from program address 0x80 0000.

The watchdog timer is also reset when the internal signal WAKE = 0. The WDT is disabled when the JTAG_E pin is pulled high. The watchdog timer is enabled only in MSN and BRN modes.

Timers

The ZON P3S/P3SL/M3/M3SL contains five timer channels. Each timer channel can be configured as counter, timer and PWM modulator and includes capture and compare functions. They can be used for timing, pulse generation, pulse width modulation, pulse timing etc.

Inside the timer logic, multiple sources can be selected to generate an interrupt to the MAXQ30 Core.

The timers have the following features:

MAXQ30 Core interrupts: The timers can interrupt the MAXQ30 Core on overflow or when the timer matches some preset value.

Pulse measurement: The timers can be triggered by an external pulse.

Pulse width modulation: The timers can be used to generate a PWM signal with selectable characteristics.

Counters: The timers can be configured to count the number of external pulse edges.

When configured as timers, the clocks are derived from the system clock. A prescaler system allows the system clock to be scaled up to 1024 before being used as the timer clock.

The timers can be operated in auto-reload mode, capture mode, up/down count auto-reload mode, and offer a PWM output function where the output signal is provided to the P0.24 and P0.25 pins that can be configured for PWM output. For the PWM mode, the sub-modes RESET, SET, and TOGGLE are available.

LCD System

The ZON P3S/P3SL/M3S/M3SL SoCs include an LCD controller that supports up to eight common planes and up to 44 segments. You can attach bare LCD glass natively operating up to 3.3V, or with an external boost circuit, up to 5V. The LCD controller supports many operating modes, including:

- Static, with up to 43 segments.
- Two common planes with up to 42 segment circuits for a total of 84 segments operating at ½ bias.
- Three common planes with up to 41 segment circuits for a total of 123 segments operating at ½ or ⅓ bias.
- Four common planes with up to forty segment circuits for a total of 160 segments operating at ⅓ bias.
- Five common planes with up to 39 segment circuits for a total of 195 segments operating at ⅓ bias.
- Six common planes with up to 38 segment circuits for a total of 228 segments operating at ⅓ bias.
- Eight common planes with up to 36 segment circuits for a total of 288 segments operating at ⅓ bias.

Additionally, the LCD controller has test features that allow all segments to be turned on or off without disturbing LCD data, a reset feature that quickly clears all LCD data, and a built-in DAC for contrast adjustment. Two segment circuits (SEG22 and SEG23) can be configured to blink. Blinking is defined as causing any segment that is set ON to alternate between the on and off states. Blinking works in any LCD mode and at either pattern frequency.

Each pin that is to serve as an LCD segment or common output must be configured in the LCDMAP registers. There are two such registers: LCDMAP0 and LCDMAP1. LCDMAP0 and LCDMAP1 control the assignments of segments to pins.

Table 14. LCD Register Segment Assignments

ELEMENT	PIN	REGISTER	BIT
SEG0/COM0	38	LCDMAP1	0
SEG1/COM1	37	LCDMAP1	1
SEG2/COM2	36	LCDMAP1	2
SEG3/COM3	35	LCDMAP1	3
SEG4/COM4	34	LCDMAP1	4
SEG5/COM5	33	LCDMAP1	5
SEG6/COM6	32	LCDMAP1	6
SEG7/COM7	31	LCDMAP1	7
SEG8	30	LCDMAP1	8

Table 14. LCD Register Segment Assignments (continued)

SEG9	29	LCDMAP1	9
SEG10	28	LCDMAP1	10
SEG11	27	LCDMAP1	11
SEG12	25	LCDMAP1	12
SEG13	24	LCDMAP1	13
SEG14	23	LCDMAP1	14
SEG15	22	LCDMAP1	15
SEG16	21	LCDMAP1	16
SEG17	19	LCDMAP1	17
SEG18	18	LCDMAP1	18
SEG19	17	LCDMAP1	19
SEG20	16	LCDMAP1	20
SEG21	15	LCDMAP1	21
SEG22	14	LCDMAP1	22
SEG23	13	LCDMAP1	23
SEG24	4	LCDMAP1	24
SEG25	3	LCDMAP1	25
SEG26	99	LCDMAP1	26
SEG27	98	LCDMAP1	27
SEG28	97	LCDMAP1	28
SEG29	96	LCDMAP1	29
SEG30	95	LCDMAP1	30
SEG31	94	LCDMAP1	31
SEG32	93	LCDMAP0	0
SEG33	92	LCDMAP0	1
SEG34	91	LCDMAP0	2
SEG35	90	LCDMAP0	3
SEG36	89	LCDMAP0	4
SEG37	88	LCDMAP0	5
SEG38	87	LCDMAP0	6
SEG39	86	LCDMAP0	7
SEG40	85	LCDMAP0	8
SEG41	84	LCDMAP0	9
SEG42	40	LCDMAP0	10
SEG43	39	LCDMAP0	11

When a pin is configured for LCD, its alternate function is completely disabled. Alternately, if a pin is configured for an alternate function (such as GPIO or a peripheral function) the contents of the LCD data register associated with that segment have no effect.

The LCD data is accessed through an indirect register mechanism. Two registers are used: the LCDINDADDR register is used to point to a specific LCD data element, and the LCDINDDATA register is used to access the data element for read or write. Each LCD data element is 32 bits wide, and it represents the eight possible backplane assignments for four of the LCD segment pins. Because there are 44 possible segment pins and there may be up to eight time slots, there are 44 bytes of LCD data arranged as eleven 32-bit words.

For example, to set the state of SEG0, the MAXQ30 Core writes 0x00 to LCDINDADDR and then writes bits 31:24 of LCDINDDATA. Each bit of the SEGxx field controls the state of the SEG pin relative to one of the eight common planes per to the Table 15.

For segment pins not configured for LCD output (LCDMAP = 0) the indirect data in the SEGxx field configures the pin for digital I/O. You can use the LCDINDDATA bits to directly control the I/O state of the pins, or software can set SEGxx for pins that are not being used for the LCD display to 0x04. This defers control of the pin to the I/O logic of the MAXQ30 MPU core.

For example, pin 38 is configurable as LCD segment 16, GPIO0.16, or MISO for the SPI port. If the LCDMAP bit for this pin is set, then the LCD function is selected and neither the MAXQ30 GPIO nor the SPI peripheral can affect the state of the pin. If the LCDMAP bit for this pin is clear, then the pin is configured per bits 2:0 of the SEGxx field in the LCDINDDATA RAM array. If bit 2 of the SEGxx field is set, then control of the pin is passed to the MAXQ30 Core port logic. In this case, if the SPI peripheral is enabled, the pin serves as SPI MISO; if the SPI peripheral is disabled, then the MAXQ30 Core GPIO logic controls the pin.

Table 15. LCD Data Assignments

LCDINDADDR	BYTE 3 (MSB)	BYTE 2	BYTE 1	BYTE 0 (LSB)
0	SEG0	SEG1	SEG2	SEG3
1	SEG4	SEG5	SEG6	SEG7
2	SEG8	SEG9	SEG10	SEG11
3	SEG12	SEG13	SEG14	SEG15
4	SEG16	SEG17	SEG18	SEG19
5	SEG20	SEG21	SEG22	SEG23
6	SEG24	SEG25	SEG26	SEG27
7	SEG28	SEG29	SEG30	SEG31
8	SEG32	SEG33	SEG34	SEG35
9	SEG36	SEG37	SEG38	SEG39
10	SEG40	SEG41	SEG42	SEG43

Table 16. LCD Commons

BIT	LCDMAP = 0	LCDMAP = 1
SEGxx.7	—	LCD segment value relative to COM7
SEGxx.6	—	LCD segment value relative to COM6
SEGxx.5	—	LCD segment value relative to COM5
SEGxx.4	—	LCD segment value relative to COM4
SEGxx.3	—	LCD segment value relative to COM3
SEGxx.2	MAXQ30 control	LCD segment value relative to COM2
SEGxx.1	Pin direction (0 = input, 1 = output)	LCD segment value relative to COM1
SEGxx.0	Pin input or output value	LCD segment value relative to COM0

The LCD controller can operate in any one of eight multiplex and bias modes, as controlled by the LCD_MODE field (Table 17)

The final factor to be considered when configuring the LCD waveforms is the LCD clock frequency. In general, you should choose the lowest frequency that gives good results with your chosen LCD glass: the power consumption of an LCD system is almost directly proportional to the operating frequency. The scan frequency is selected by the LCD_CLK field in the LCDMODE register (Table 18).

By default, the LCD_CLK field is set to 64Hz, which is sufficient for most applications. For some displays, especially displays with high multiplex rates (eight-way multiplexing, for example) a higher clock frequency may be necessary.

The LCD voltage (V_{LCD}) is critical to successfully using the LCD controller. Broadly, the V_{LCD} level controls the contrast of the display.

The LCD glass has a recommended operating voltage, frequently 3V or 5V. The specified operating voltage assumes a typical set of LCD waveforms: a 3V LCD glass expects to see voltages at 0, 1, 2 and 3 volts with a total differential peak-to-peak voltage of 6V maximum (that is, backplane at 0V and segment at 3V, followed by backplane at 3V and segment at 0V).

Table 17. LCD Controller Modes

LCD_MODE[2:0]	NUMBER OF STATES	BIAS
0	4	⅓
1	3	⅓
2	2	½
3	3	½
4	Static	—
5	5	⅓
6	6	⅓
7	8	⅓

Table 18. LCD Clock Frequency

LCD_CLK[1:0]	LCD CLOCK FREQUENCY (Hz)
0	64
1	128
2	256
3	512

Four V_{LCD} sources can be selected that make use of the internal resources of the device. The selection is made by writing the LCD_VMODE field in the LCDMODE register. The following section describes the choices available.

LCD_VMODE = 0b00 (V_{LCD} = 3.3V): In this mode, V_{LCD} is connected to V_{3P3SYS} in MSN mode and to V_{BAT} in LCD ONLY mode. The LCD DAC is bypassed, meaning there is no contrast adjustment available.

LCD_VMODE = 0b01 (V_{LCD} from LCD DAC): In mode 1, V_{LCD} is the output of the LCD DAC. The input of the LCD DAC is V_{3P3SYS} in MSN mode and V_{BAT} in LCD ONLY mode. The DAC scales its input based on the digital code written to the LCD_DAC field of the LCDCTL register.

V_{DACOUT} = V_{DACIN} x (LCD_DAC[4:0]/31): User software can configure the contrast of the display be writing a value to the *LCD_DAC* register.

LCD_VMODE = 0b10 (V_{LCD} boost): In mode 2, V_{LCD} is once again the output of the LCD DAC, but the input of the LCD DAC is taken from the V_{LCD5} pin. The V_{LCD5} pin is typically sourced from an external charge pump. The device provides a pin that supplies a continuous square wave at 32kHz. The V_{SQW} pin is enabled by setting the V_SQ_EN bit in the LCDCTL register. Using this circuit, the device can use 5V as well as 3V glass.

LCD_VMODE = 0b11 (V_{LCD} external): In this final mode, V_{LCD} is disconnected from any internal source. The V_{LCD} pin is connected directly to the LCD waveform generator. This allows the application circuit to generate its own V_{LCD} voltage and provide it to the waveform generator. In this mode, it is the responsibility of external circuitry to regulate the LCD voltage for optimum LCD contrast.

In addition to blinking, the LCD display can be configured to display up to 31 pages of data stored in CE_RAM in continuous programmed intervals without intervention by the MAXQ30 Core when LCD page DMA mode is enabled. To use this mode, load the CE_RAM with 11 rows of LCD data per page. Then, program the first row address in CE_RAM into LCD_DMA_ADDR and set the number of pages to display in PAGE_NUM both in the LCDINDADDR register. Set PAGE_DMA_EN in the LCD_CTRL register prior to enabling the LCD to properly enter the LCD page DMA mode. Note, the contents programmed in LCD_DATA registers are lost after PAGE_DMA mode activated if they are different than what stored CE_RAM for page mode.

To automatically switch between the main and secondary pages, set the PAGE_TIME bit in the LCDCTRL register. Now the display alternates between the main and secondary pages at a time determined by the PAGE_TIME_SET field in the LCDCTRL register (Table 19). No further intervention by the MAXQ30 Core is required until data on one or the other pages needs to be updated.

By default, the pages alternate between the main and secondary pages at four seconds per page. For some applications, this may be too fast, so other rates can be selected by setting the PAGE_TIME_SET field in the LCDCTRL register. Note, the display will rollover to first page after the last page indicated by PAGE_NUM displayed.

Bits in the LCDMODE register support the following special LCD modes:

- When the LCD_ON bit is set in the LCDMODE register, all segments are unconditionally turned on. Note that this setting does not disturb the information in the LCD data registers. Software can set this bit to test segments and then clear it to restore the previous display.

Table 19. LCD Page Timing

PAGE_TIME_SET[1:0]	HOLD TIME (s)
0	4
1	8
2	16
3	32

- When the LCD_OFF bit is set in the LCDMODE register, all segments are unconditionally turned off. Note that this setting does not disturb the information in the LCD data registers. Software can set this bit to test segments and then clear it to restore the previous display.
- Setting the LCD_RST bit in the LCDMODE register clears all data from the LCD controller (all segment data and all configuration information). All pins are returned to their alternate functions. The LCD_RST bit itself is cleared automatically.

A quick way to configure all segment pins that can also be configured as common pins is to configure the segments in LCDMAP0/1 and then set the LCD_ALLCOM bit in the LCDMODE register. All eight pins, if they are configured for LCD use in LCDMAP, are assigned as common pins. Common pins that are not used in the cur- rent multiplex scheme (as defined in LCD_MODE) receive an idle signal.

Real-Time Clock (RTC) General Description

The ZON P3S/P3SL/M3/M3SL real-time clock (RTC) block includes a time-of-day clock plus a set of ancillary features to keep the clock accurate and to provide additional services to the system. The RTC includes:

- 32-bit seconds register
- 8-bit sub-seconds register
- 32-bit alarms register

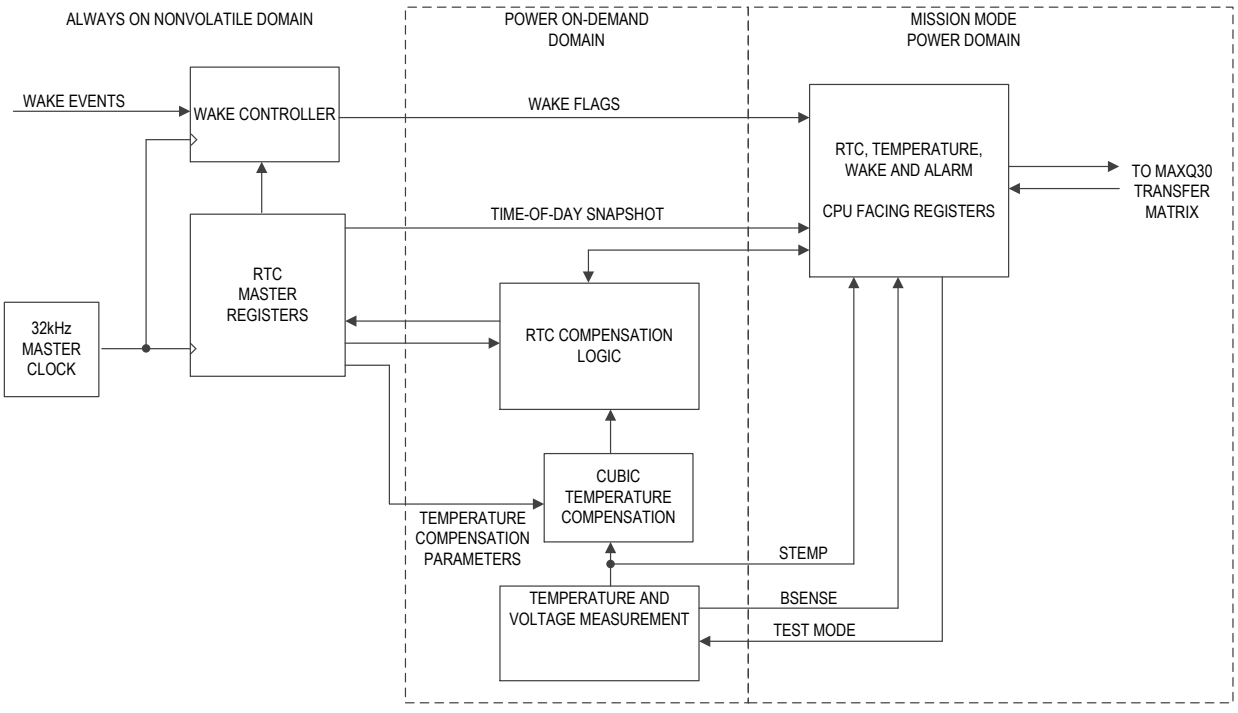


Figure 3. Real-Time Clock Block Diagram

- Wake CPU from SLP mode on a variety of events
- Temperature measurement
- Third-order (cubic) temperature compensation hardware
- Battery condition monitor.

The RTC block resides across three power domains. The real-time clock and the oscillator that drives it reside in the non-volatile power domain to maintain functionality during power failures. The wake controller and power management unit also reside in this power domain so that the MAXQ30 Core can be notified of power and other wake events even when the MAXQ30 Core is in SLP mode and power to the MAXQ30 Core is turned off.

Other RTC logic, such as the temperature measurement and temperature compensation logic, resides in an on-demand power domain. Chip logic can turn this power domain on and off as required, so from time to time the nonvolatile domain can turn on power to the on-demand domain, perform a compensation cycle, and then turn off power.

The final power domain is the MSN mode domain. It has power only when the MAXQ30 Core is active. This domain contains the MAXQ30 Core facing registers and associated interface logic. By keeping this domain off unless the MAXQ30 Core is active battery power is saved.

RTC Temperature Compensation

The real-time clock contains a temperature compensation mechanism that is automatically applied to the clock oscillator. Details on temperature compensation can be found in the *Applications Information* section of this data sheet.

Security Engines

The ZON P3S/P3SL/M3/M3SL includes two peripherals that provide cryptographic services to user software.

The first of these peripherals performs encryption and decryption per the data encryption standard (DES). The DES standard was originally published as a standard in 1977, but since that time has been shown to be less secure than modern applications demand. Nonetheless, DES is still widely used in many industries.

The second security peripheral performs encryption and decryption per the advanced encryption standard (AES). The AES standard was chosen in 2001 as a replacement for DES as its limitations came to light.

DES

The DES algorithm encrypts and decrypts data in 64-bit blocks using a 56-bit key. A more secure use of DES runs the algorithm three times: first encrypting under one key, then decrypting under a different key, then encrypting again under either the original key (two-key TDES) or a third key (three-key TDES). The DES peripheral in ZON P3S/P3SL/M3/M3SL supports all modes of operation.

AES

The advanced encryption system is a block cipher that operates on a 128-bit block of data under a 128-, 192-, or 256-bit encryption key. AES-GCM is supported in this advanced encryption system.

Random Number Generator

The true random generator (TRNG) generates true random numbers for use in encryption.

OnGuard

The ZON P3S/P3SL/M3S/M3SL SoCs comprise the OnGuard feature that reliably protects the legally relevant resources of the meter. The OnGuard feature sup- ports straight forward implementation of the Welmec/MID requirements by shielding the legally relevant data and processes from any interference from the general application processes.

The implementation provides a meter mode bit. This bit operates in a very similar manner to the supervisor mode bit present in some microprocessor-based systems. The meter mode bit, which is referred to as the MMO bit, is a one-way bit. The microprocessor itself can only clear this bit. Once cleared, only the hardware can set the bit through an interrupt. The microprocessor can never set it. The MMO bit is set upon entry into the XFER interrupt service routine (ISR) (or any other CE interrupt) using the SWINT register. The XFER ISR then explicitly clears the bit before exiting, thus ensuring that only the XFER ISR can run with the MMO bit set. In this way, the code executed in the meter servicing XFER ISR is segregated in terms of capability from the rest of the code executed by the MAXQ30 MPU.

The scheme protects the metrology subsystem from the following:

- Memory corruption
- Code corruption
- Stack corruption, overflow, or manipulation
- Configuration corruption
- Microprocessor cycle starvation

Reset Behavior

The ZON P3S/P3SL/M3S/M3SL SoCs contain a MAXQ30 Core. Like with most MAXQ30 processors, execution begins in a utility ROM located at address 0x80 0000 in code space. Starting code execution at this ROM allows the MAXQ30 Core to check for special modes, such as boot loader or debug mode before branching to user code located at 0x00 0000.

Table 20: Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNIT
C_{SYS}	V_{3P3SYS}	DGND	Bypass capacitor for V_{3P3SYS}	≥ 0.1 ±20%*	µF
C_A	V_{3P3A}	AGND	Bypass capacitor for V_{3P3A}	≥ 0.1 ±20%	µF
C_D	V_{3P3D}	DGND	Bypass capacitor for V_{3P3D}	≥ 10**	µF
C_{VDD}	V_{DD}	DGND	Bypass capacitor for V_{DD}	0.1 ±20%	µF
C_{VLCD}	V_{VLCD}	DGND	Bypass capacitor for V_{LCD}	0.1 ±20%	µF
C_B	V_{BAT}	DGND	Bypass capacitor for V_{BAT}	0.1 ±20%	µF
C_{BRTC}	V_{BAT_RTC}	DGND	Bypass capacitor for V_{BAT_RTC}	1.0 ±20%	µF
XTAL	XIN	XOUT	32.768kHz crystal—electrically similar to ECS .327-12.5-17x, Vishay XT26T, or Suntsu SCP6—32.768kHz TR (load capacitance 12.5pF).	32.768	kHz
C_{XS}	XIN	AGND	Load capacitor values for crystal depend on crystal specifications and board parasitics. Nominal values are based on 4pF board capacitance and include an allowance for chip capacitance.	20 ±10%	pF
C_{XL}	XOUT	AGND		20 ±10%	pF
C_3	V_{3P3_RTC}	DGND	Bypass capacitor for V_{3P3_RTC}	≥ 1	µF
C_{DDCL}	V_{DD_CAL}	DGND	Bypass capacitor for V_{DD_CAL}	0.1 ±20%	µF
L_V	V_{3P3SYS}	V_{3P3A}	Ferrite from analog-to-digital supply pin	600***	Ω
D_{RTC}	V_{3P3_RTC}	Super-Cap	Diode between V_{3P3_RTC} and battery or super capacitor	****	

**Capacitor values must ensure that V_{3P3SYS} slew rate is < 0.1V/ms.*

***Recommended value is 22µF.*

****For certain use cases, a ferrite bead (600Ω at 100MHz is recommended. If no ferrite bead is used, V_{3P3SYS} and V_{3P3A} must be tied together.)*

*****For certain cases. Consult factory for details.*

Applications Information

Temperature Compensation

The ZON P3S/P3SL/M3S/M3SL SoCs support temperature compensation for both metrology and for the RTC.

Temperature Compensation for Metrology Temperature compensation for metrology is based on the behavior of the V_{REF} reference voltage (bandgap voltage). The nominal voltage can be described with the following formula:

$$V_{NOM(T)} = V_{REF(22)} + (T - 22) \times TC_1 + ((T - 22)^2) \times TC_2$$

In this formula, T is the temperature in °C. The linear coefficient TC_1 and the quadratic coefficient TC_2 can be obtained from trim information using the formulae given in the VREF part of the Electrical Specification.

TRIMT is the value of the bandgap trim and is stored in the info block of the device. It can be accessed using a function in the utility ROM. Once the MAXQ30 Core has obtained the value for TRIMT at startup, it calculates TC1 and TC2 per the equations given in the Electrical Specification and copies TC1 and TC2 into the appropriate CE register locations where the CE can use them for internal temperature compensation. In internal temperature compensation mode, the CE autonomously controls gain adjustment registers for the metrology values based on the anticipated deviation of the bandgap voltage. It is also possible for the MAXQ30 Core to use the TC1 and TC2 coefficients in combination with system-related coefficients to implement system-wide temperature compensation. This type of compensation can adjust for sensor characteristics over temperature and other temperature-related effects. In that case, the CE is operating in external temperature compensation mode, leaving access to the gain adjustment registers to the MAXQ30 Core. For details on temperature compensation, refer to the ZON P3S/P3SL/M3S/M3SL hardware reference manual.

Temperature Compensation for the RTC

To facilitate RTC compensation for the effects of temperature on the crystal oscillator, the ZON P3S/P3SLM3S/M3SL provide a temperature measurement circuit that is independent of the metrology ADCs, the auxiliary ADC and the MAXQ30 Core. The TEMP_PER register can be used to schedule periodic automatic temperature measurements that will happen even if the device is in SLP or LCD modes. The result of the last temperature measurement is contained in the STEMP register. The value is trimmed such that room temperature results in an STEMP value of zero. STEMP changes by one LSB for approximately each 0.3°C.

To improve the resolution of the RTC timekeeping, the RTC keeps time based on the 32.768kHz crystal oscillator multiplied by a factor of six hundred (19.660800MHz). This frequency is compensated for temperature using a cubic equation. The coefficients of this equation are set in registers TC_A through TC_D to form the equation:

$$f_{\pi} = \mathrm{RTC\_CAL} + \mathrm{TC\_D} + \frac{\mathrm{TC\_C}}{2^{11}} \times \mathrm{STEMP} + \frac{\mathrm{TC\_B}}{2^{21}} \times \mathrm{STEMP}^2 + \frac{\mathrm{TC\_A}}{2^{31}} \times \mathrm{STEMP}^3$$

The RTC_CAL register sets the nominal frequency of the crystal. The temperature compensation represented by the cubic equation is then added to the value in RTC_ CAL to determine the number of multiplied clock cycles needed to represent a single second in the RTC. The RTC_SEC register increments by one each time the number of multiplied clock cycles is equal to the value derived in the equation above. For a perfect 32.768kHz crystal, the value of RTC_CAL is 32768 x 600 = 19660800.

TC_D is the constant deviation of the crystal frequency from ideal at room temperature and can be determined by measuring the raw frequency of the crystal. TC_B is the quadratic coefficient that reflects the inverse-parabolic variation with temperature that most low-frequency tuning fork crystals have. TC_B can be obtained from the data sheet of the crystal in use. Linear (TC_C) and cubic (TC_A) coefficients are zero or near zero for most crystals.

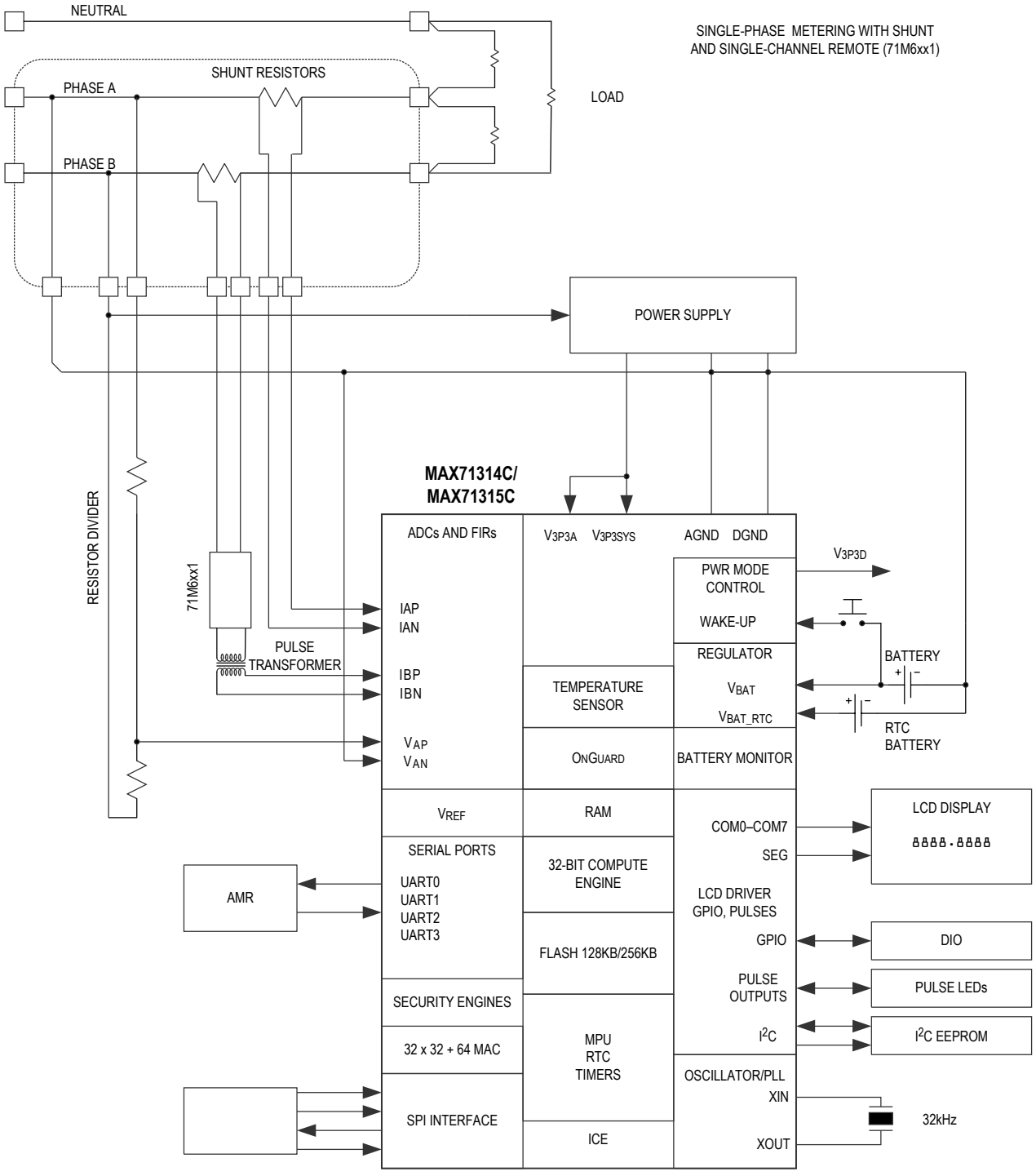
When the device is not in SLP or LCD mode, every temperature measurement results in compensation to the RTC calibration, meaning the internal cubic equation is re-evaluated. When the device is in SLP or LCD mode, to save power, any temperature measurement will only result in compensation if the temperature has changed by more than some minimum amount, defined by the TEMP_RANGE register. If the new STEMP value is less than TEMP_RANGE different from the last STEMP used to evaluate the compensation equation, then the new STEMP is discarded and no action is taken. RTC compensation is further supported by the following features:

- High temperature alarm limit: If the most recent temperature measurement exceeds a predefined value, the MPU is awakened if in SLP mode
- Low temperature alarm limit: If the most recent temperature measurement is less than a predefined

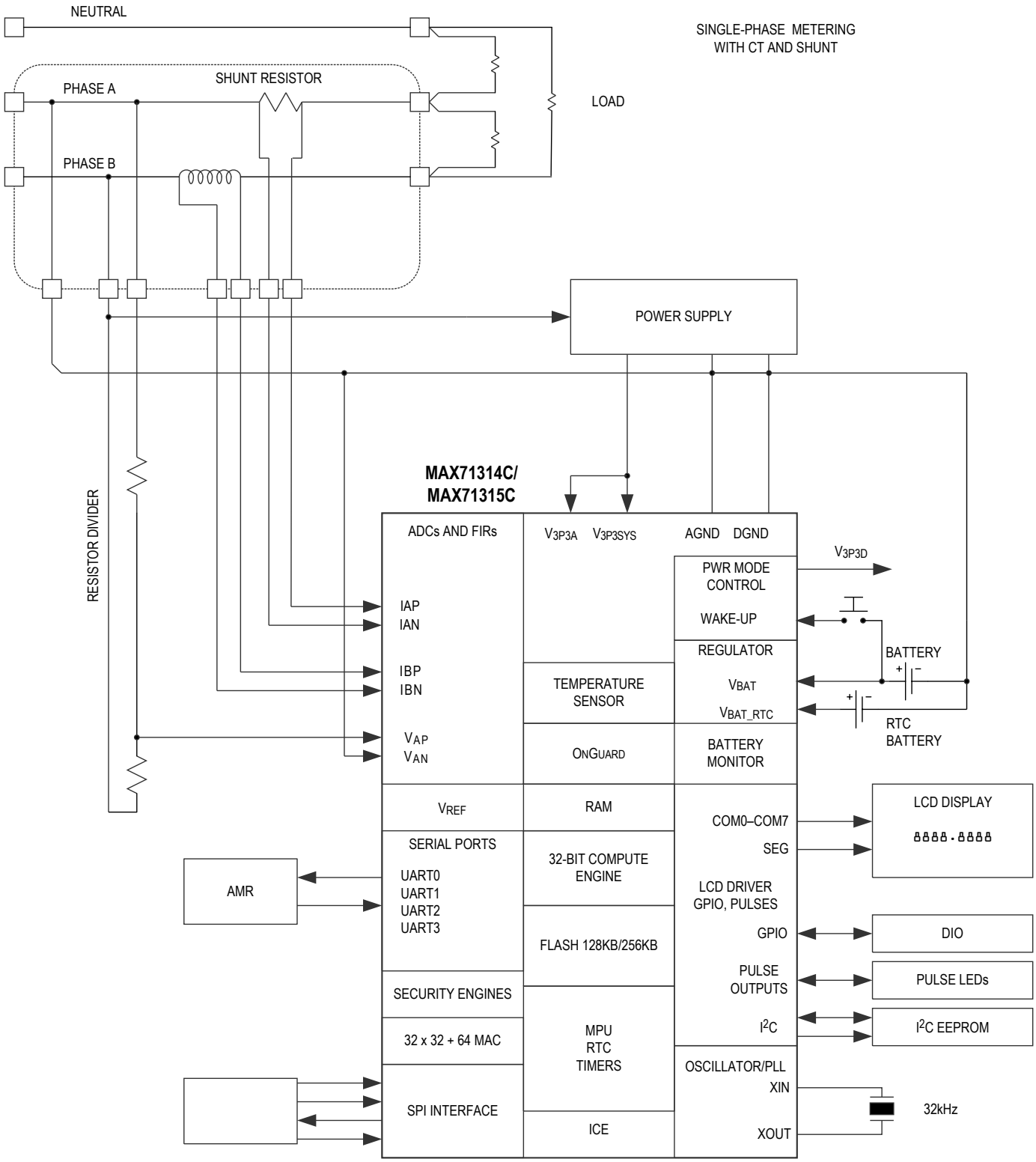
The achievable accuracy of the temperature compensation is determined by two factors:

- Accuracy of the temperature measurement
- Repeatability of the crystal characteristics (inversion temperature, quadratic coefficient

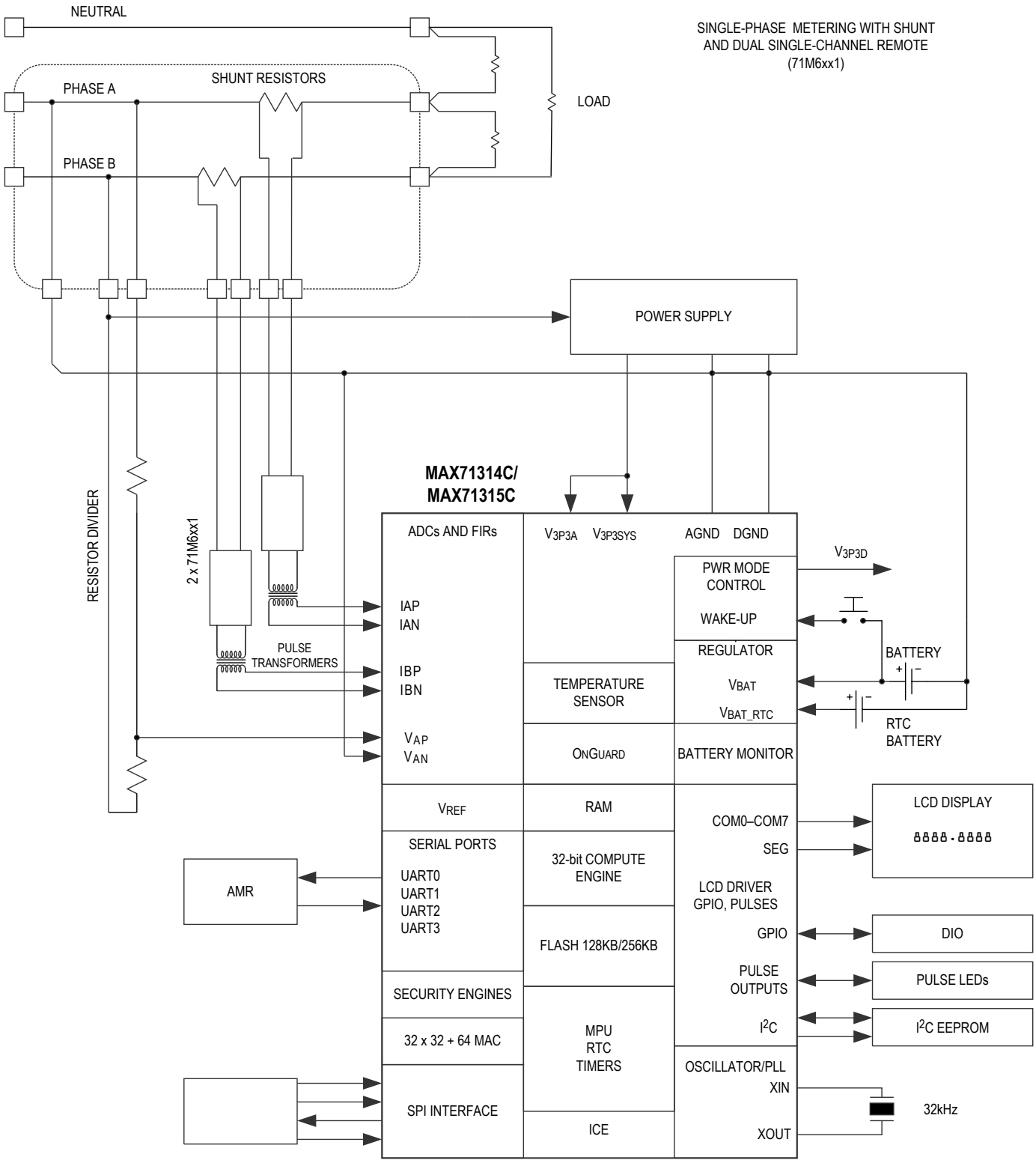
Typical Application Circuits



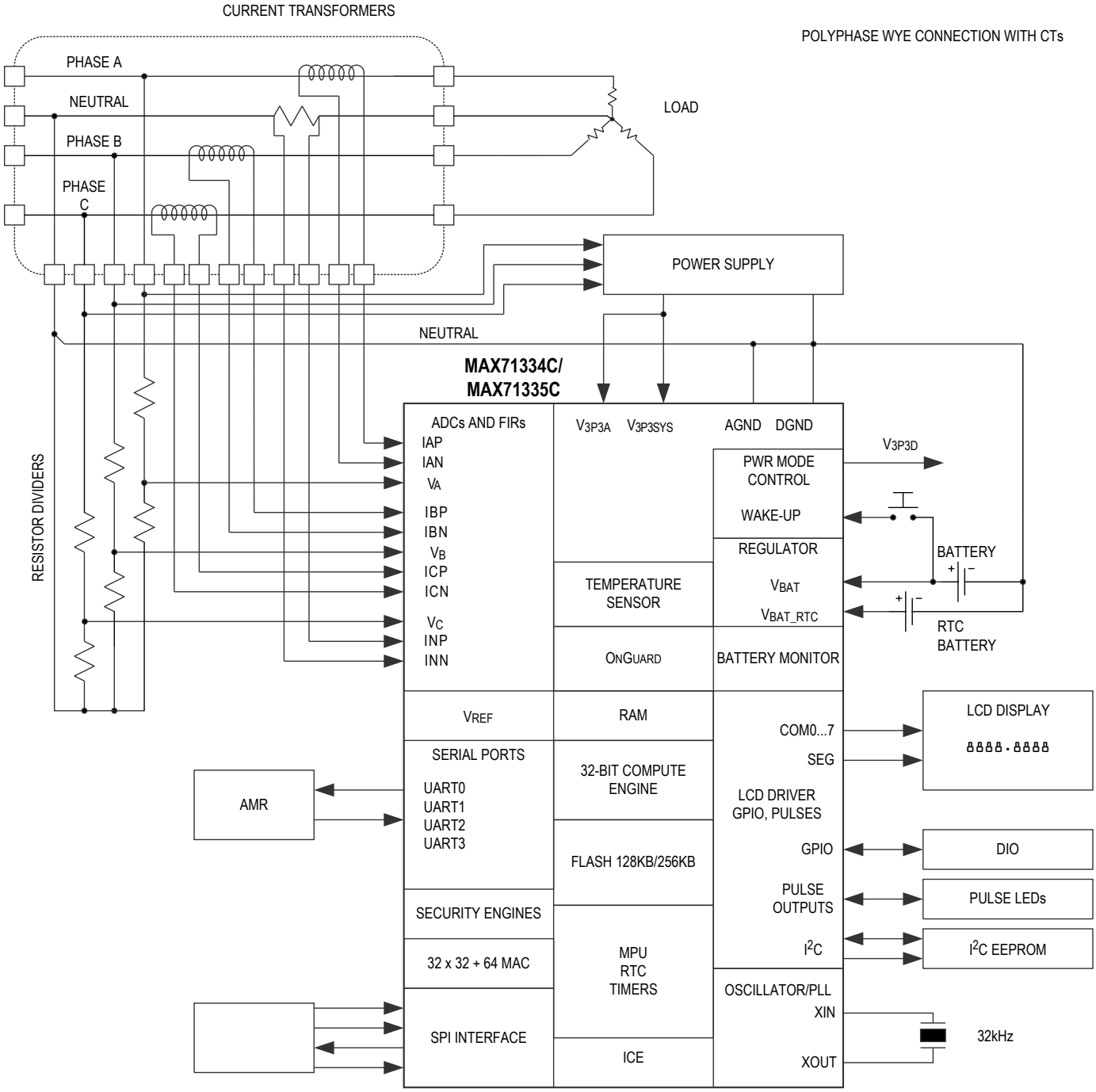
Typical Application Circuits (continued)



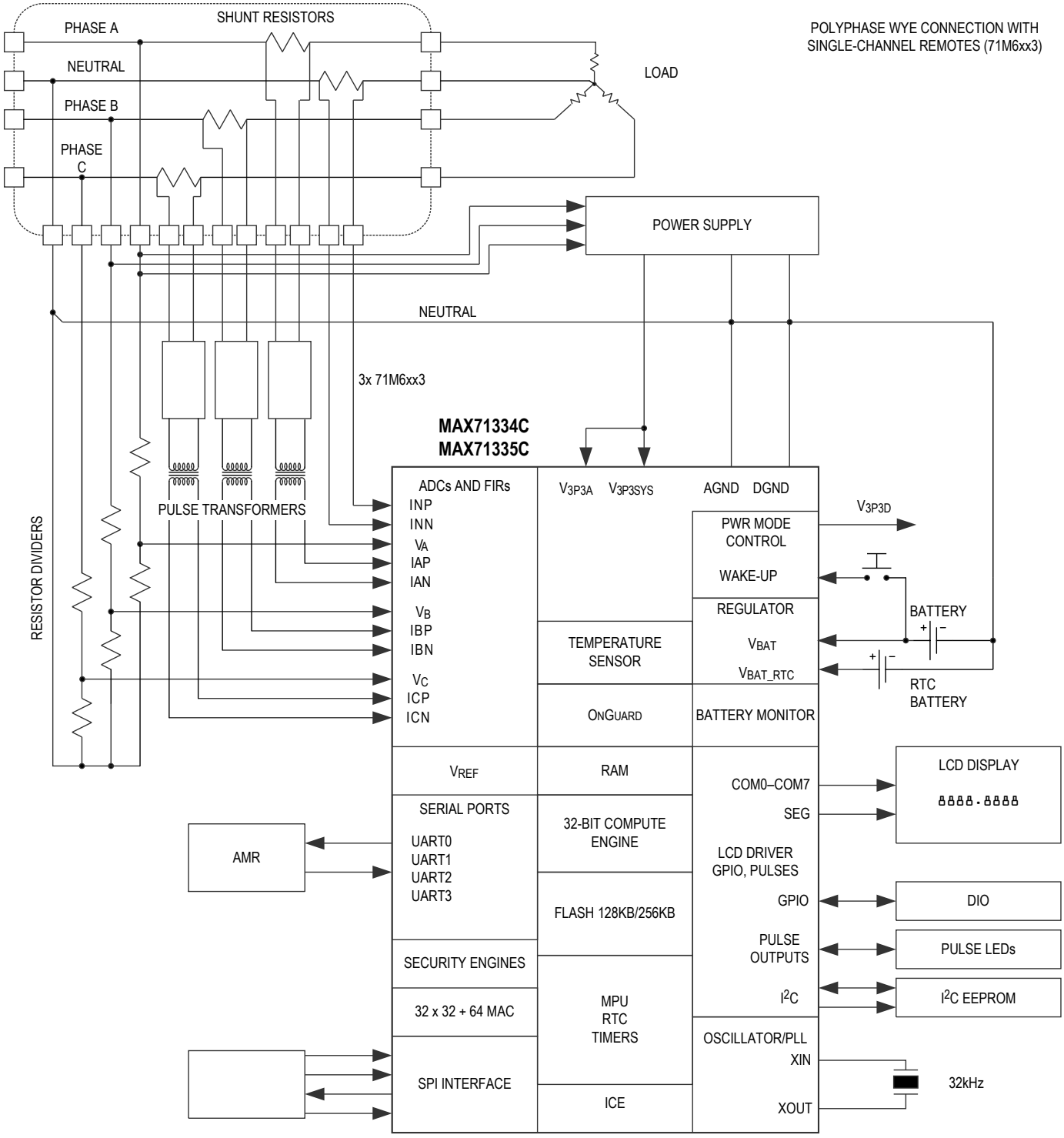
Typical Application Circuits (continued)



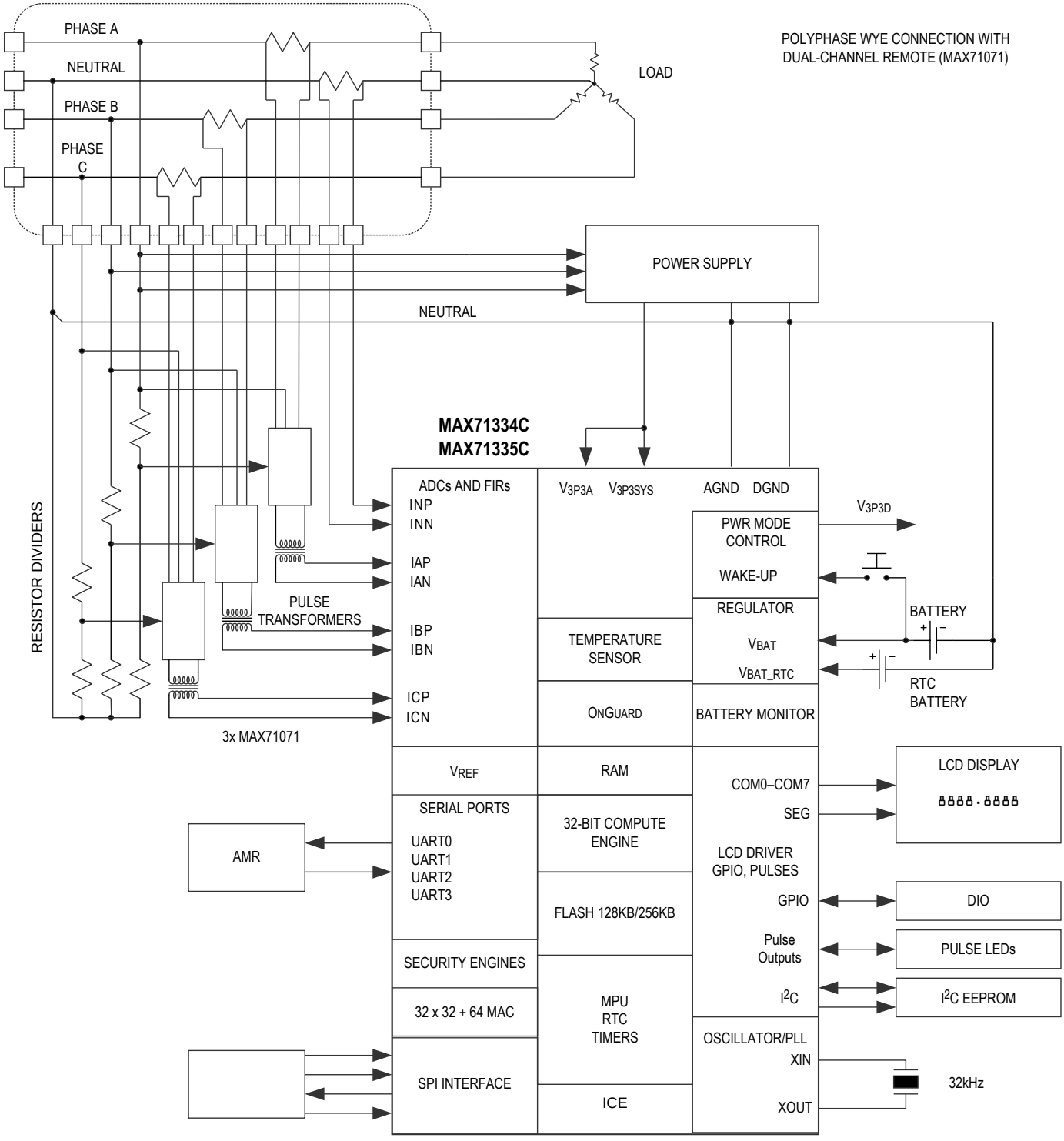
Typical Application Circuits (continued)



Typical Application Circuits (continued)



Typical Application Circuits (continued)



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	PROGRAM MEMORY	DATA MEMORY	NVRAM	METROLOGY CHANNELS
MAX71315CECQ+*	-40°C to +85°C	100-LQFP, bulk	256KB	20KB	1KB	4
MAX71314CECQ+*		100-LQFP, bulk	128kB	20KB	1KB	4
MAX71315CECQ+T*		100-LQFP, tape and reel	256kB	20KB	1KB	4
MAX71314CECQ+T*		100-LQFP, tape and reel	128kB	20KB	1KB	4
MAX71335CECQ+		100-LQFP, bulk	256KB	20KB	1KB	7
MAX71334CECQ+*		100-LQFP, bulk	128KB	20KB	1KB	7
MAX71335CECQ+T		100-LQFP, tape and reel	256KB	20KB	1KB	7
MAX71334CECQ+T*		100-LQFP, tape and reel	128KB	20KB	1KB	7

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = *Tape and reel.*

**Future product—contact future product for availability.*

Package Information

Package outline information and land patterns (footprints) are appended to this document.

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Revision History

REVISION NUMBER	DATE	DESCRIPTION	PAGES CHANGED
0	12/2015	Initial release	—
1	4/2016	Rebranding, Pinout Diagrams, Pin Descriptions, Battery Currents, LSB Size	1, 8, 12, 16-21
2	2/2017	TC_1 and TC_2 formulas, Pinout diagrams, Pin Descriptions	9, 48, 16-21
3	11/2017	Added VBAT SLP current to Electrical Characteristics table Corrected formula for TC_1 Added formula for temperature	8 6 7
4	8/2018	Updated RAM and NVRAM description on Title Page Updated block diagram Updated ADC description Updated Slave SPI clock frequency Updated the description for the auxiliary ADC Changed pin name BDME to JTAG_E, updated WDT description Removed value for TC1 from Temperature Compensation section Updated RAM description Corrected spelling and polarity of RSTN pin	1 20 22 36 39 40 46 31, 54 Various
5	2/2019	Added number of available GPIO pins Corrected typos (“starting ADC” vs. “staring ADC”) Corrected value for C3 in Table 20 Corrected formatting and hyphenation in all text and tables	Title page 4, 5 45 all
6	7/2019	Corrected formatting in Table 20	45
7	10/2019	Updated Silergy logo Updated tables with electrical specifications Updated pin-out diagrams Updated pin description with respect to INTx and WAKEx signals Added explanation to SLP mode Added legal notice	1 4 – 12 14, 15 16 – 19 31 55
8	12/2019	Corrected pin names for PWM output (P0.24. P0.25) Fixed font colors	40 all