

Description

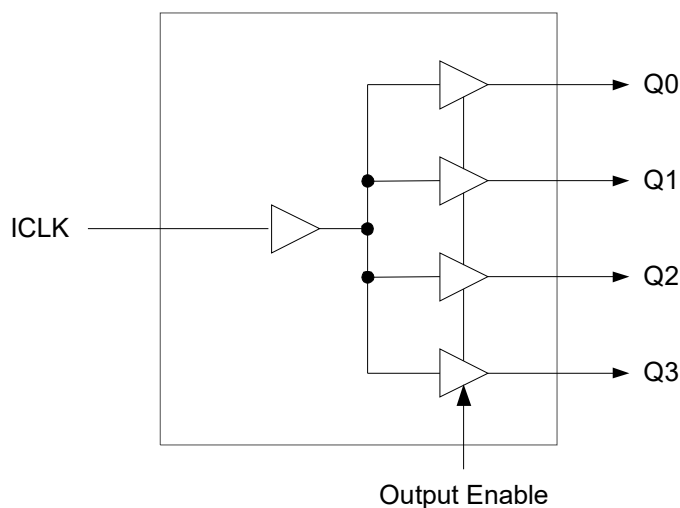
The 553S is a low skew, single input to four output, clock buffer. The 553S has best in class additive phase Jitter of sub 50 fsec.

Renesas makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact Renesas for all of your clocking needs.

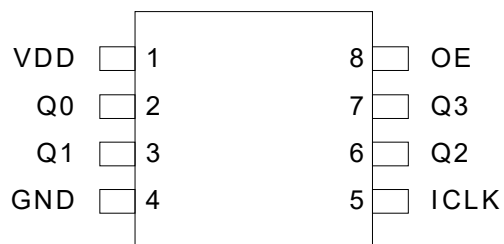
Features

- Low additive phase jitter RMS: 50fs
- Extremely low skew outputs (50ps)
- Low cost clock buffer
- Packaged in 8-SOIC and small 8-DFN packages, Pb-free
- Input/Output clock frequency up to 200MHz
- Ideal for networking clocks
- Operating voltages: 1.8V to 3.3V
- Output Enable mode tri-states outputs
- Advanced, low power CMOS process
- Extended temperature range (-40°C to +105°C)
- 3.3V tolerant input clock

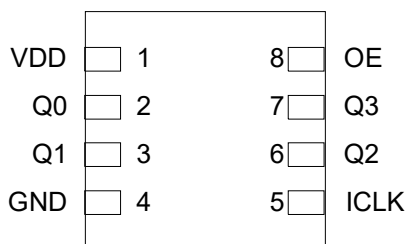
Block Diagram



Pin Assignments



8-pin SOIC



8-pin DFN

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Connect to +1.8V, +2.5V, or +3.3V.
2	Q0	Output	Clock output 0.
3	Q1	Output	Clock output 1.
4	GND	Power	Connect to ground.
5	ICLK	Input	Clock input.
6	Q2	Output	Clock output 2.
7	Q3	Output	Clock output 3.
8	OE	Input	Output Enable. Tri-states outputs when low. Connect to VDD for normal operation.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01μF should be connected between VDD on pin 1 and GND on pin 4, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 553S is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 553S. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.8V
Output Enable and All Outputs	-0.5 V to VDD + 0.5 V
ICLK	3.465V
Ambient Operating Temperature (extended)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
Input ESD Protection (Human Body Model)	2500V

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature (extended)	-40	-	+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71	-	+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

V_{DD} = 1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		1.71	-	1.89	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7xVDD	-	3.45	V
Input Low Voltage, ICLK	V _{IL}	Note 1	-	-	0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD	-	VDD	V
Input Low Voltage, OE	V _{IL}		-	-	0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -10mA	1.3	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 10mA	-	-	0.35	V
Operating Supply Current	IDD	No load, 135MHz	-	15	-	mA
Nominal Output Impedance	Z _O		-	17	-	Ω
Input Capacitance	C _{IN}	ICLK, OE pin	-	5	-	pF

Notes: 1. Nominal switching threshold is VDD/2.

V_{DD} = 2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		2.375	-	2.625	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7xVDD	-	3.45	V
Input Low Voltage, ICLK	V _{IL}	Note 1	-	-	0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD	-	VDD	V
Input Low Voltage, OE	V _{IL}		-	-	0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -16mA	1.8	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 16mA	-	-	0.5	V
Operating Supply Current	IDD	No load, 135MHz	-	18	-	mA
Nominal Output Impedance	Z _O		-	17	-	Ω
Input Capacitance	C _{IN}	ICLK, OE pin	-	5	-	pF

Notes: 1. Nominal switching threshold is VDD/2.

V_{DD} = 3.3 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		3.135	-	3.465	V
Input High Voltage, ICLK	V _{IH}	Note 1	0.7xVDD	-	3.45	V
Input Low Voltage, ICLK	V _{IL}	Note 1	-	-	0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD	-	VDD	V
Input Low Voltage, OE	V _{IL}		-	-	0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -25mA	2.2	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 25mA	-	-	0.7	V
Operating Supply Current	IDD	No load, 135MHz	-	22	-	mA
Nominal Output Impedance	Z _O		-	17	-	Ω
Input Capacitance	C _{IN}	ICLK, OE pin	-	5	-	pF

Notes: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency			0	-	200	MHz
Output Rise Time	t _{OR}	0.36 to 1.44V, C _L = 5pF	-	0.6	1.0	ns
Output Fall Time	t _{OF}	1.44 to 0.36V, C _L = 5pF	-	0.6	1.0	ns
Propagation Delay	Note 1		2.5	3	3.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz–20MHz	-	-	0.05	ps
Output to Output Skew	Note 2	Rising edges at VDD/2	-	50	65	ps
Device to Device Skew		Rising edges at VDD/2	-	-	200	ps
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up	-	-	2	ms
Output Enable Time	t _{EN}	C _L ≤ 5pF	-	-	3	cycles
Output Disable Time	t _{DIS}	C _L ≤ 5pF	-	-	3	cycles

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency			0	-	200	MHz
Output Rise Time	t _{OR}	0.5 to 2.0 V, C _L = 5pF	-	0.6	1.0	ns
Output Fall Time	t _{OF}	2.0 to 0.5 V, C _L = 5pF	-	0.6	1.0	ns
Propagation Delay	Note 1		3	3.5	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz–20MHz	-	-	0.05	ps
Output to Output Skew	Note 2	Rising edges at VDD/2	-	40	65	ps
Device to Device Skew		Rising edges at VDD/2	-	-	200	ps
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up	-	-	2	ms
Output Enable Time	t _{EN}	C _L ≤ 5pF	-	-	3	cycles
Output Disable Time	t _{DIS}	C _L ≤ 5pF	-	-	3	cycles

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Frequency			0	-	200	MHz
Output Rise Time	t _{OR}	0.66 to 2.64 V, C _L = 5pF	-	0.6	1.0	ns
Output Fall Time	t _{OF}	2.64 to 0.66 V, C _L = 5pF	-	0.6	1.0	ns
Propagation Delay	Note 1		2.5	3	3.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz–20MHz	-	-	0.05	ps
Output to Output Skew	Note 2	Rising edges at VDD/2	-	25	65	ps
Device to Device Skew		Rising edges at VDD/2	-	-	200	ps
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up	-	-	2	ms
Output Enable Time	t _{EN}	C _L ≤ 5pF	-	-	3	cycles
Output Disable Time	t _{DIS}	C _L ≤ 5pF	-	-	3	cycles

Notes:

1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

Phase Noise Plots

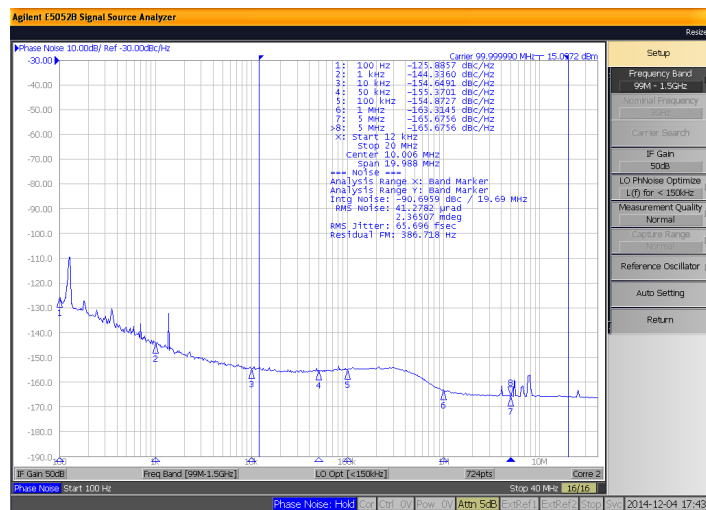


Figure 1. 553S Reference Phase Noise 66fs (12kHz to 20MHz)

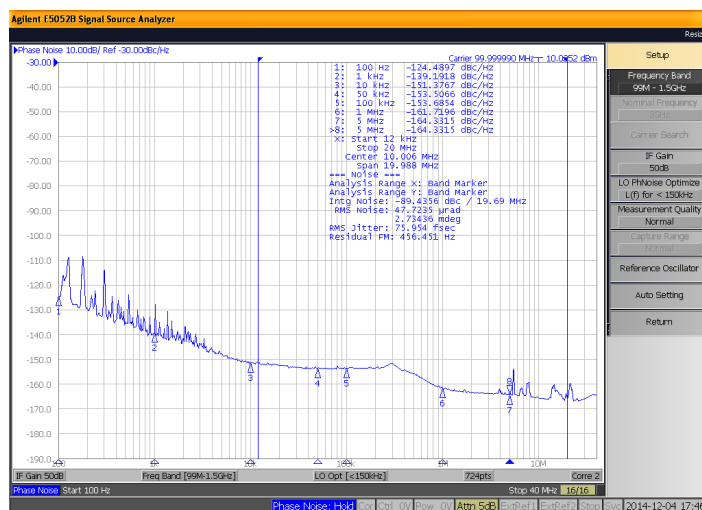
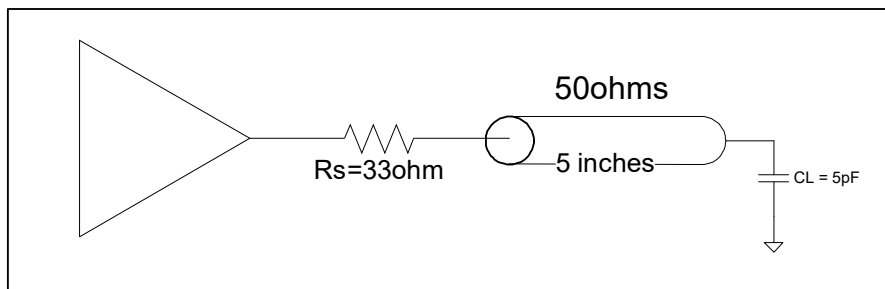


Figure 2. 553S Output Phase Noise 76fs (12kHz to 20MHz)

The phase noise plots above show the low Additive Jitter of the 553S high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 66fs of RMS phase jitter while the output of 553S has about 76fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 37fs.

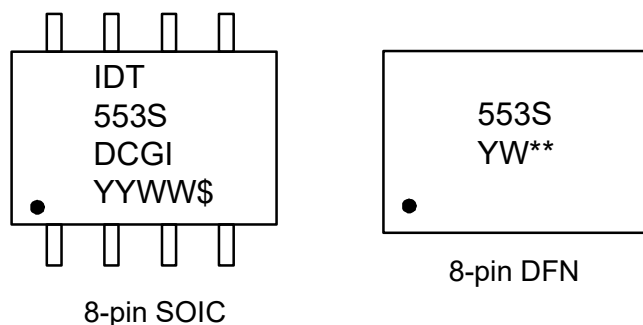
Test Load and Circuit



Thermal Characteristics (8SOIC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air	-	150	-	°C/W
	θ_{JA}	1 m/s air flow	-	140	-	°C/W
	θ_{JA}	3 m/s air flow	-	120	-	°C/W
Thermal Resistance Junction to Case	θ_{JC}		-	40	-	°C/W

Marking Diagrams



Notes:

1. “**” is the lot number.
2. “YYWW” or “YW” are the last digits of the year and week that the part was assembled.
- 3 “G” denotes RoHS compliant package.
4. “\$” denotes mark code.
5. “I” denotes extended temperature range device.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the links below. The package information is the most current data available.

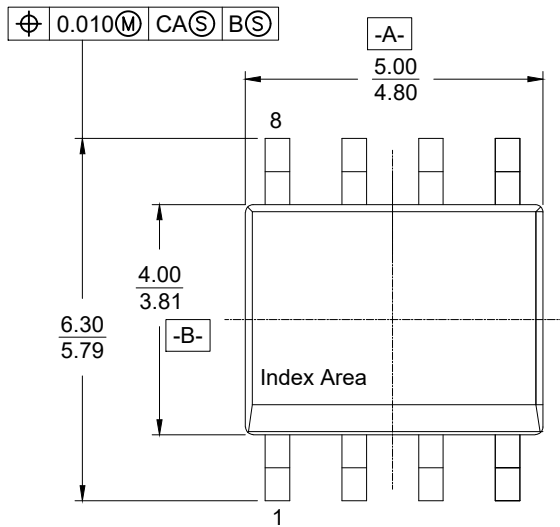
Ordering Information

Part Number	Shipping Packaging	Package	Temperature Range
553SDCGI	Tubes	8-pin SOIC	-40°C to +105°C
553SDCGI8	Tape and Reel	8-pin SOIC	-40°C to +105°C
553SCMGI	Cut Tape	8-pin DFN	-40°C to +105°C
553SCMGI8	Tape and Reel	8-pin DFN	-40°C to +105°C

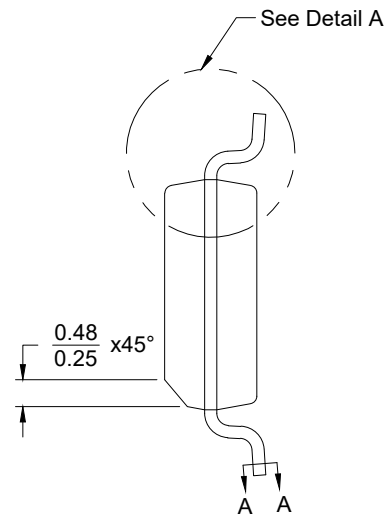
“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

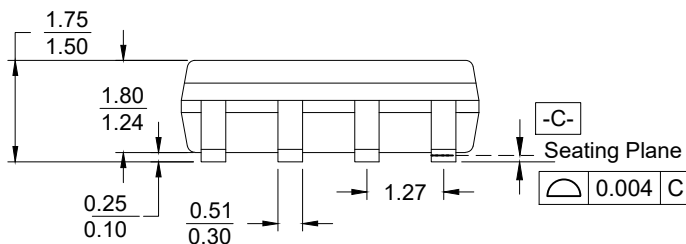
Date	Description of Change
December 13, 2023	Update POD link to the latest drawing for 8-DFN (CMG8D1).
September 29, 2023	Changed "Input High Voltage, ICLK" maximum parameter in DC Electrical Characteristics 3.3V table to 3.45V from VDD.
February 3, 2023	Updated package drawings links in Package Outline Drawings .
January 6, 2020	Added "Input ESD Protection" information in Absolute Maximum Ratings table.
October 5, 2018	- Added "3.3V tolerant input clock" bullet to Features section. - Updated voltage ratings in DC Electrical Characteristics tables. - Updated Package Outline Drawings section. - Updated legal disclaimer.
March 18, 2015	Initial release.



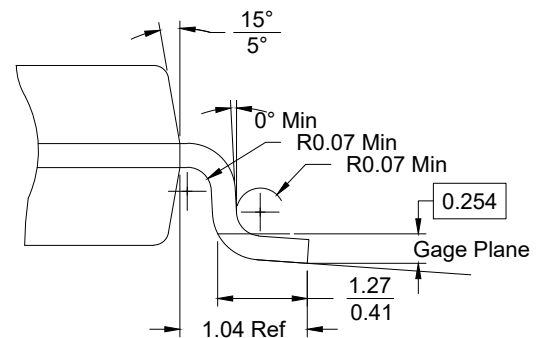
Top View



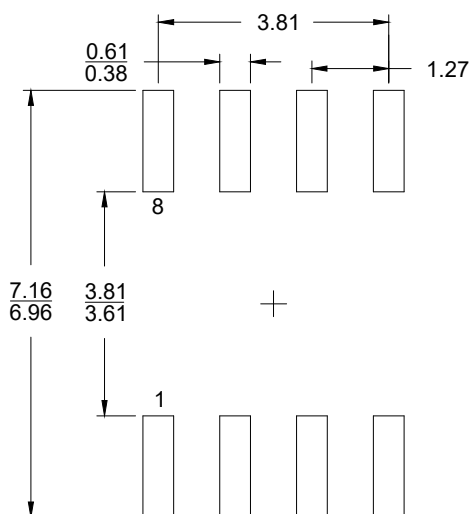
Side View



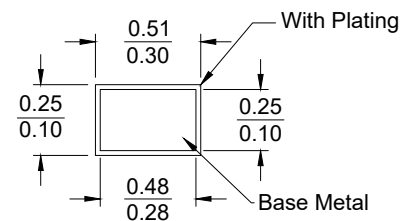
Side View



Detail A
(Rotated 90° CW)



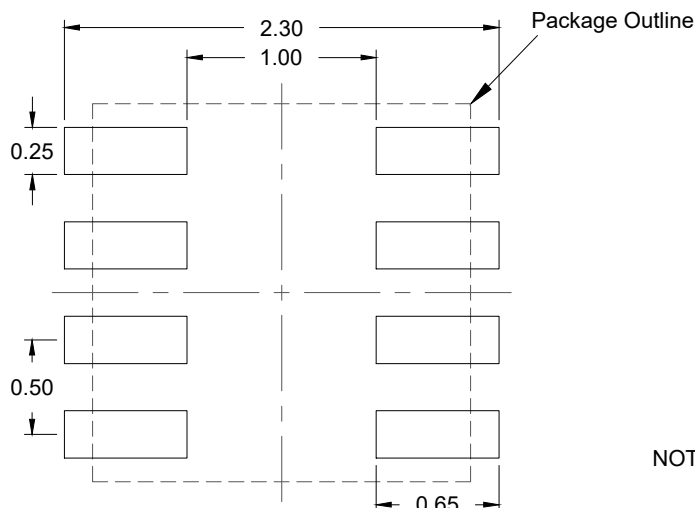
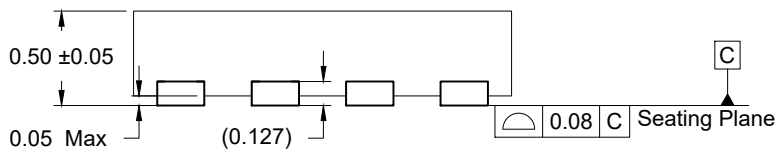
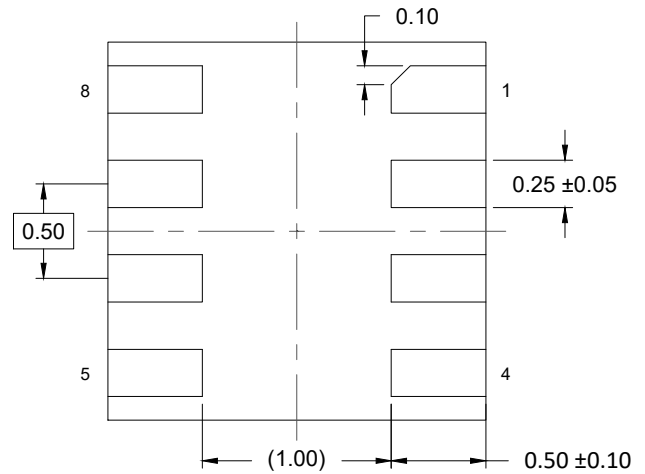
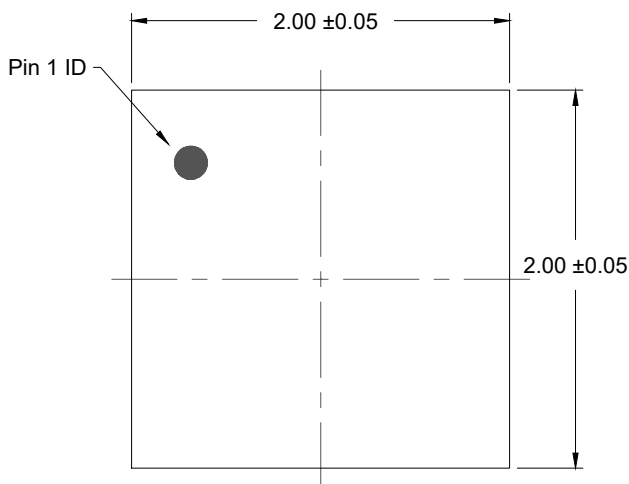
RECOMMENDED LAND PATTERN
(PCB Top View, SMD Design)



Section A-A

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.