1.4W Mono Audio Low-Voltage Audio Power Amplifier

Features

- Operating Voltage: 2.5V-5.5V
- Supply Current
  – I_{DD}=1.5mA at V_{DD}=5V
  – I_{DD}=1.2mA at V_{DD}=3.6V
  – I_{DD}=1mA at V_{DD}=2.5V
- Low Shutdown Current
  – I_{DD}=0.5μA at V_{DD}=5V
- Low Distortion
  – 0.85W, at V_{DD}=5V, R_L=8Ω THD+N=0.05%
  – 0.43W, at V_{DD}=3.6V, R_L=8Ω THD+N=0.05%
  – 0.6W, at V_{DD}=3.6V, R_L=4Ω THD+N=0.09%
  – 0.2W, at V_{DD}=2.5V, R_L=8Ω THD+N=0.09%
  – 0.26W, at V_{DD}=2.5V, R_L=4Ω THD+N=0.1%
- Output Power

  at 1% THD+N
  – 1.2W, at V_{DD}=5V, R_L=8Ω
  – 0.6W, at V_{DD}=3.6V, R_L=8Ω
  – 0.82W, at V_{DD}=3.6V, R_L=4Ω
  – 0.27W, at V_{DD}=2.5V, R_L=8Ω
  – 0.36W, at V_{DD}=2.5V, R_L=4Ω

  at 10% THD+N
  – 1.4W, at V_{DD}=5V, RL=8Ω
  – 0.75W, at V_{DD}=3.6V, R_L=8Ω
  – 1.05W, at V_{DD}=3.6V, R_L=4Ω
  – 0.35W, at V_{DD}=2.5V, R_L=8Ω
  – 0.46W, at V_{DD}=2.5V, R_L=4Ω
- Depop Circuitry Integrated
- Thermal Shutdown Protection and Over Current Protection Circuitry
- High supply voltage ripple rejection
- Surface-Mount Packaging
  - 9 bump WLCSP
- Lead Free Available (RoHS Compliant)

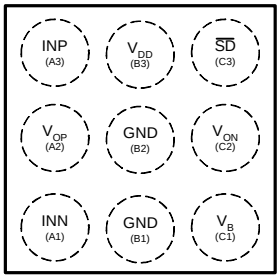
General Description

The APA0712 is a mono BTL audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 5V supply, the APA0712 can deliver 1.4W of continuous power into a BTL 8Ω load at 10% THD+N throughout voice band frequencies. Although this device is characterized out to 20kHz, its operation is optimized for narrow band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power-sensitive applications with special depop circuitry to eliminate speaker noise when exiting shutdown mode. The APA0712 is available in 9 bumps WLCSP.

Applications

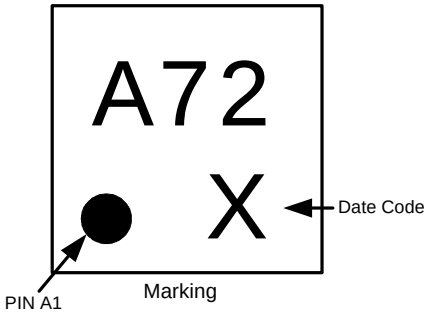
- Mobil Phones
- PDAs
- Digital Camera
- Portable Electronic Devices

Pin Configuration



Top View

WLCSP-9

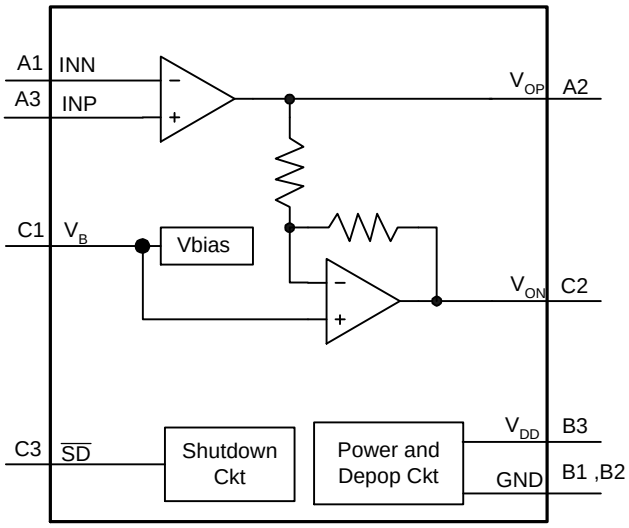


Ordering and Marking Information

APA0712 □□□-□□ □ Lead Free Code Handling Code Temp. Range Package Code	Package Code HA: WLCSP-9 Operating Ambient Temp. Range I : -40 to 85° C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device
APA0712 HA : A72 / X	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram



Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6	V
V_{IN},$\overline{SD}$	Input Voltage	-0.3 to 6	V
T_A	Operating Junction Temperature Range	-40 to 85	℃
T_J	Maximum Junction Temperature	150	℃
T_{STG}	Storage Temperature Range	-65 to +150	℃
T_{SDR}	Lead Soldering Temperature Range	260, 10 seconds	℃
P_D	Power Dissipation	Internally Limited	W

Notes : Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient WLCSP-9	165	^{o}C /W

Recommended Operating Conditions

		Min.	Max.	Unit
Supply Voltage V_{DD}		2.5	5.5	V
High level threshold voltage, V_{IH}	$\overline{SD}$	2		V
Low level threshold voltage, V_{IL}	$\overline{SD}$		0.8	V

Electrical Characteristics

V_{DD}=5V, GND=0V, T_A= 25 ℃ (unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.5		5.5	V
I_{DD}	Supply Current			1.5	2.5	mA
I_{SD}	Shutdown Current	$\overline{SD}$ = 0V		1		μA
I_I	Input current	$\overline{SD}$		0.1		μA
V_{DD}=5V,T_A=25 ℃						
Po	Output Power	THD+N = 1%, f = 1KHz R_L = 8Ω	1	1.1		W
		THD+N = 10%, f = 1KHz R_L = 8Ω		1.4		
THD+N	Total Harmonic Distortion Pulse Noise	f = 1KHz P_O = 0.85W, R_L = 8Ω		0.05		%
PSRR	Power Supply Rejection Ratio	C_B = 2.2μF, R_L = 8Ω, f = 120Hz		90		dB
Vos	Output Offset Voltage	R_L = 8Ω			20	mV
S/N		With A-weighted Filter P_O = 0.85W, R_L = 8Ω		99		dB
Vn	Noise Output Voltage	C_B = 2.2μF		20		μV (rms)
V_{DD}=3.6V,T_A=25 ℃						
Po	Output Power	THD+N = 1%, f = 1KHz R_L = 4Ω R_L = 8Ω		0.8 0.6		W
		THD+N = 10%, f = 1KHz R_L = 4Ω R_L = 8Ω		1 0.7		
THD+N	Total Harmonic Distortion Pulse Noise	f = 1KHz P_O = 0.6W, R_L = 4Ω P_O = 0.43W, R_L = 8Ω		0.09 0.05		%
PSRR	Power Supply Rejection Ratio	C_B = 1μF, R_L = 8Ω, f = 120Hz		80		dB
Vos	Output Offset Voltage	R_L = 8Ω			20	mV
S/N		With A-weighted Filter P_O= 0.43W, R_L = 8Ω,		96		dB
Vn	Noise Output Voltage	C_B = 2.2μF		20		μV (rms)

Electrical Characteristics (Cont.)

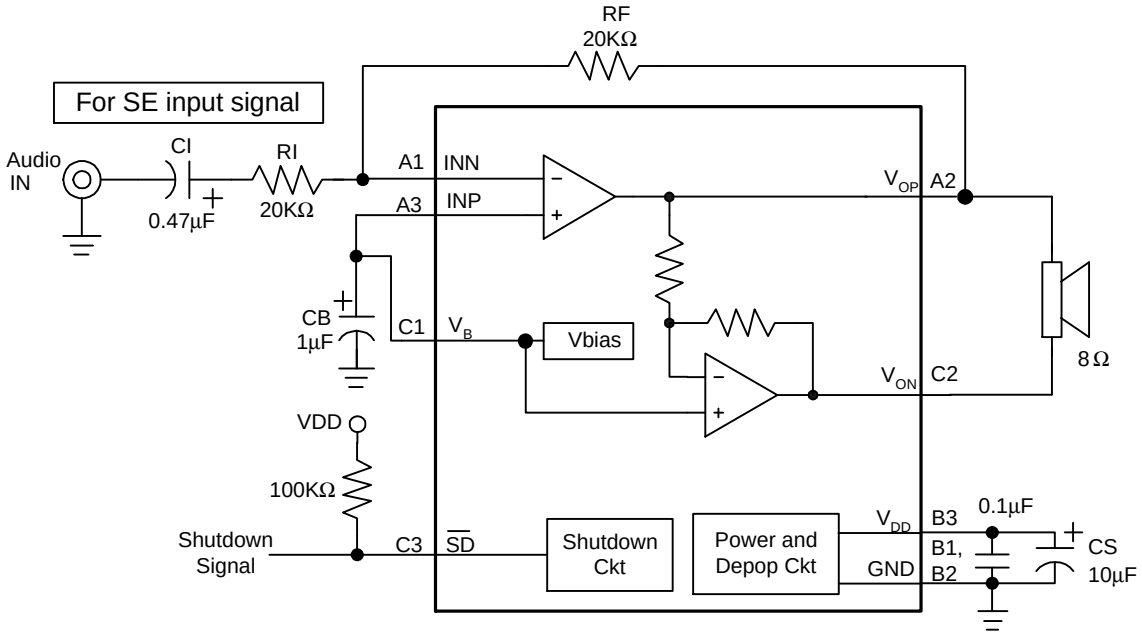
V_{DD}=5V, GND=0V, T_A= 25 ℃ (unless otherwise noted)

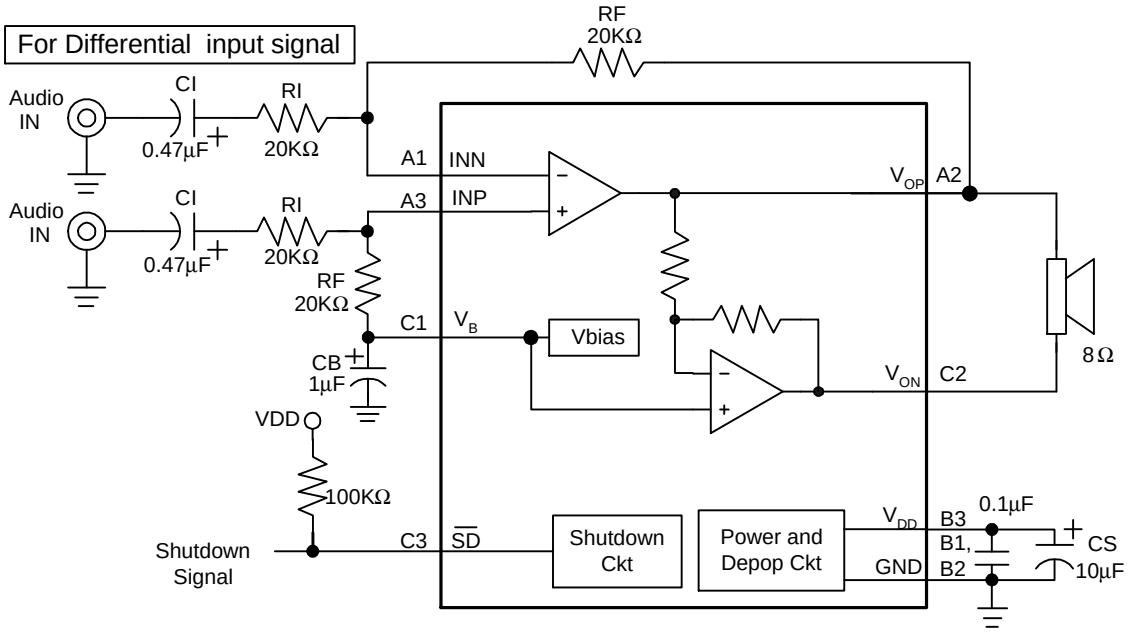
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}=2.5V,T_A=25 ℃						
Po	Output Power	THD+N = 1%, f = 1KHz R_L = 4Ω R_L = 8Ω		0.36 0.27		W
		THD+N = 10%, f = 1KHz R_L = 4Ω R_L = 8Ω		0.46 0.34		
THD+N	Total Harmonic Distortion Pulse Noise	f = 1KHz P_O = 0.26W, R_L = 4Ω P_O = 0.2W, R_L = 8Ω		0.1 0.08		%
PSRR	Power Supply Rejection Ratio	C_B = 2.2μF, R_L = 8Ω, f = 120Hz		58		dB
Vos	Output Offset Voltage	R_L = 4Ω			20	mV
S/N		With A-weighted Filter P_O = 0.2W, R_L = 8Ω		93		dB
Vn	Noise Output Voltage	C_B = 2.2μF		20		μV (rms)

Pin Descriptions

Pin		I/O	Function Description
NO.	Name		
A1	INN	I	The inverting input of amplifier. INN is used as audio input terminal, typically.
A2	V_{OP}	O	The positive output terminal of BTL amplifier.
A3	INP	I	The non-inverting input of amplifier. INP is tied to VB terminal for single-end (SE) input signal.
B1	GND	-	Ground connection for circuitry.
B2	GND	-	Ground connection for circuitry.
B3	V_{DD}	-	Supply voltage input pin
C1	V_B	-	Bypass pin
C2	V_{ON}	O	The negative output terminal of BTL amplifier.
C3	$\overline{SD}$	I	Shutdown mode control signal input, place entire IC in shutdown mode when held low.

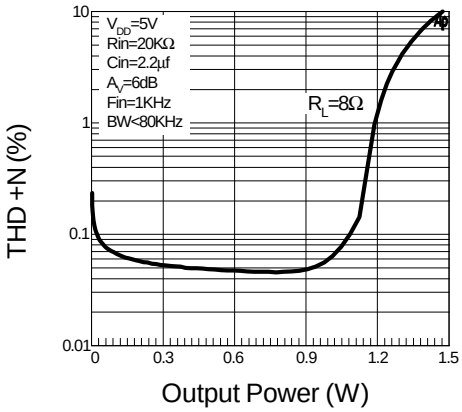
Typical Application Circuit



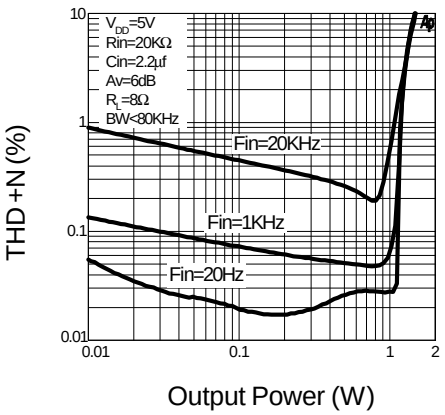


Typical Operating Characteristics

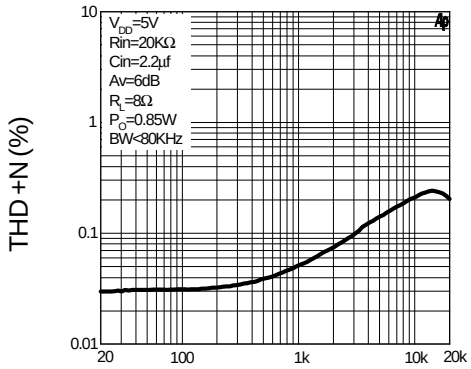
THD +N vs. Output Power



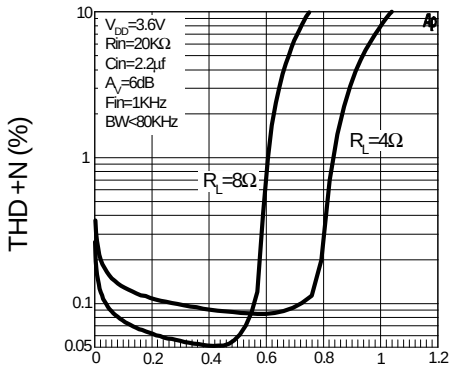
THD +N vs. Output Power



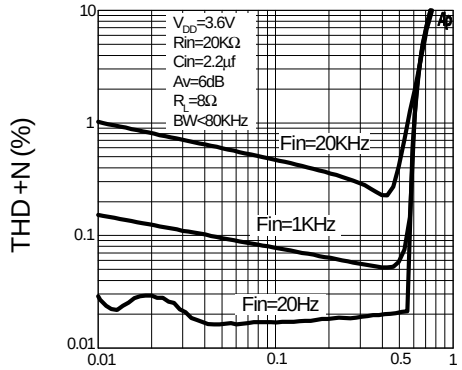
THD +N vs. Frequency



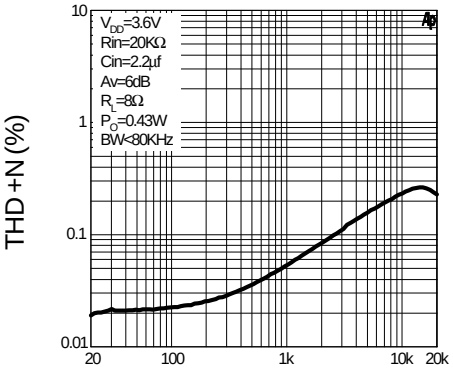
THD +N vs. Output Power



THD +N vs. Output Power

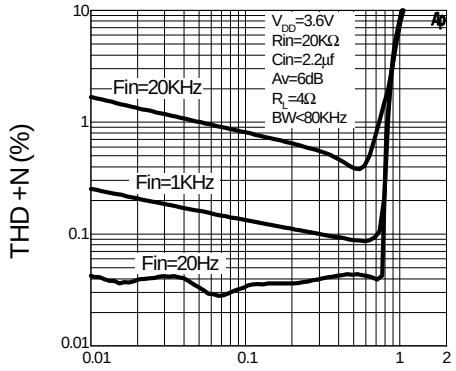


THD +N vs. Frequency

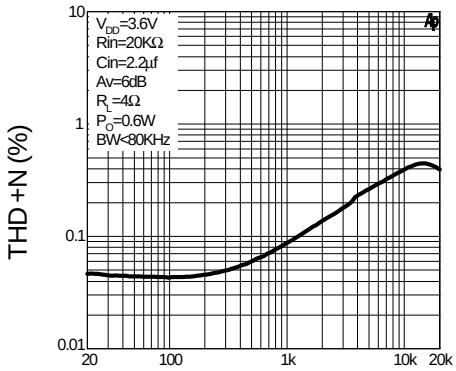


Typical Operating Characteristics (Cont.)

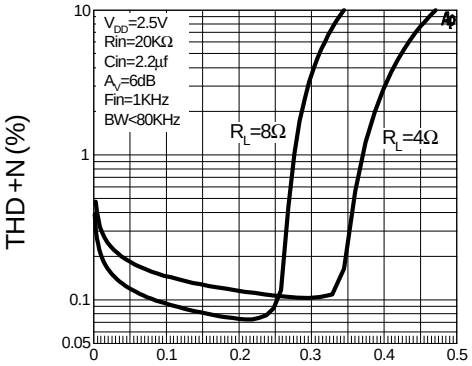
THD +N vs. Output Power



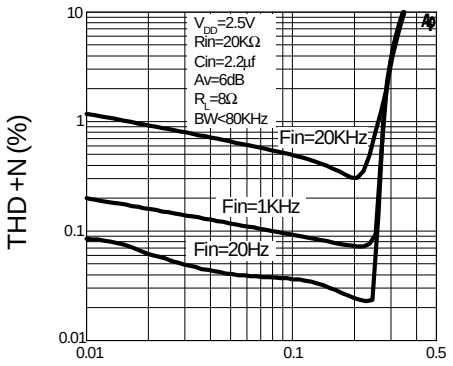
THD +N vs. Frequency



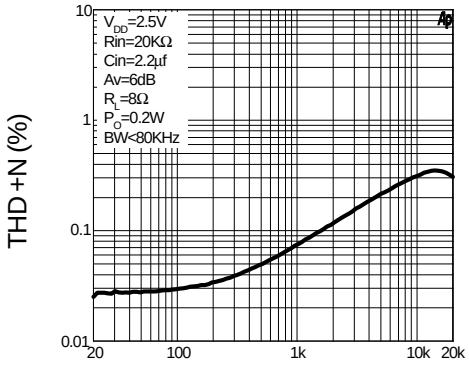
THD +N vs. Output Power



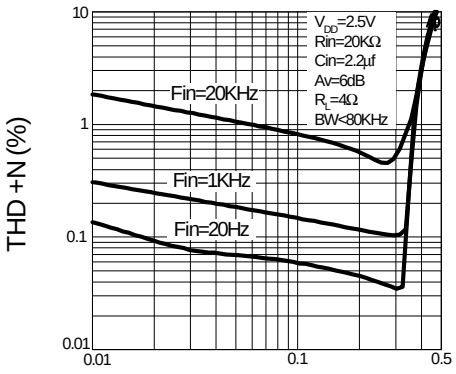
THD +N vs. Output Power



THD +N vs. Output Power

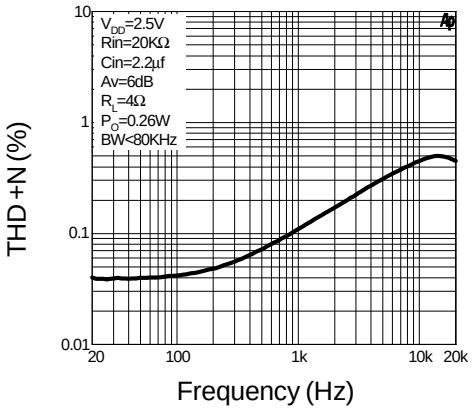


THD +N vs. Output Power

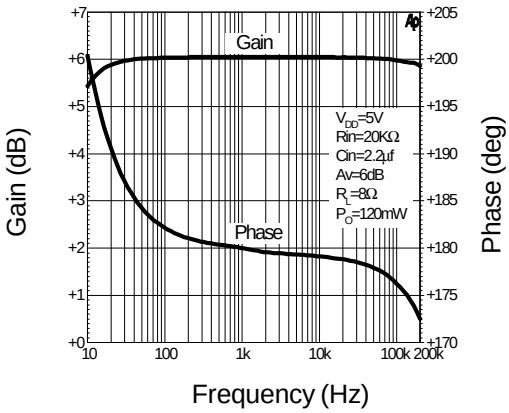


Typical Operating Characteristics (Cont.)

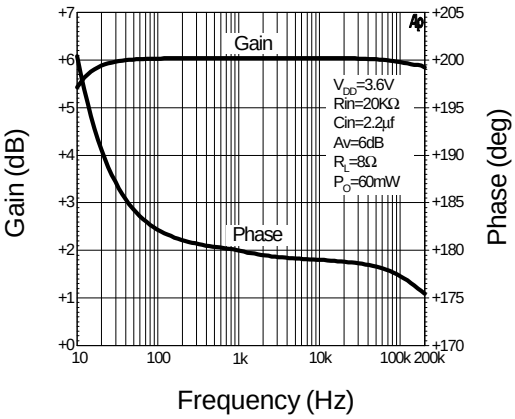
THD +N vs. Frequency



Frequency Response



Frequency Response



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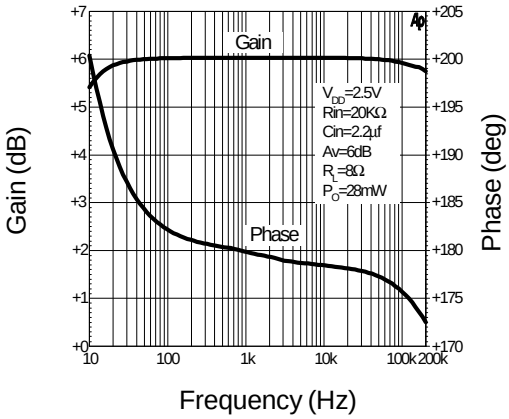
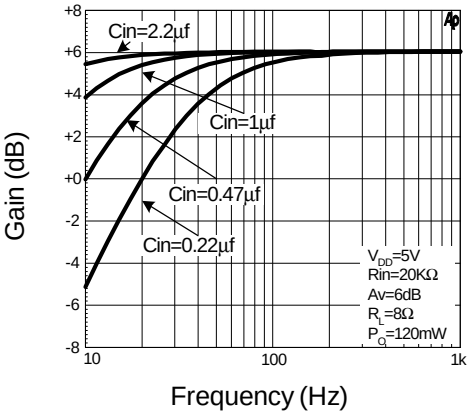
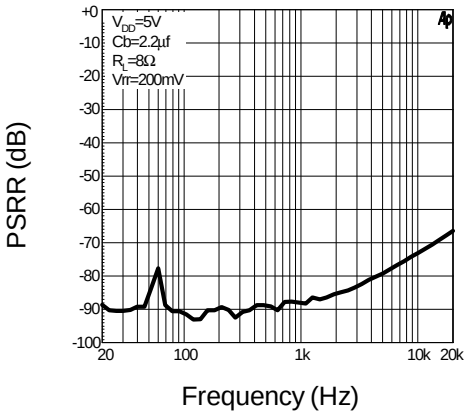


THD +N vs. Output Power

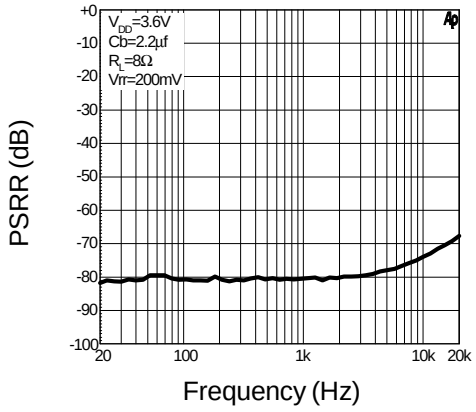


PSRR vs. Frequency

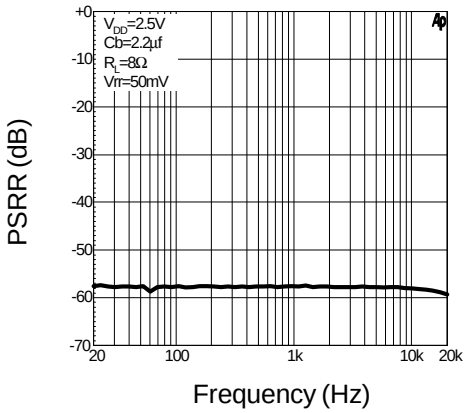


Typical Operating Characteristics (Cont.)

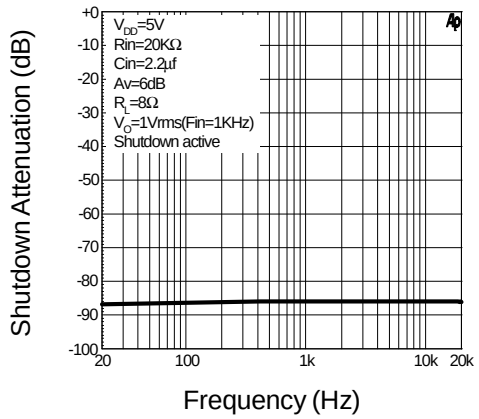
PSRR vs. Frequency



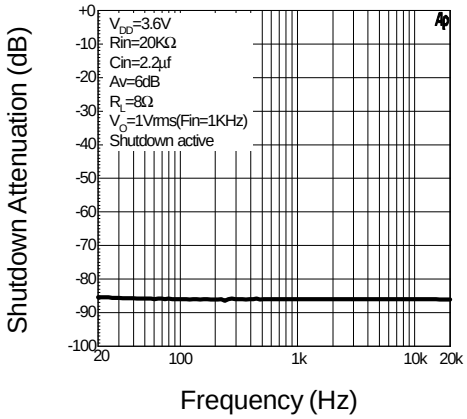
PSRR vs. Frequency



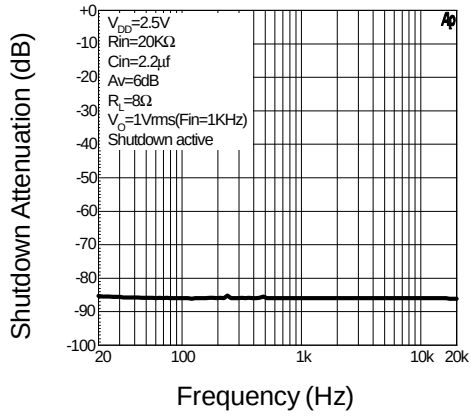
Shutdown Attenuation vs. Frequency



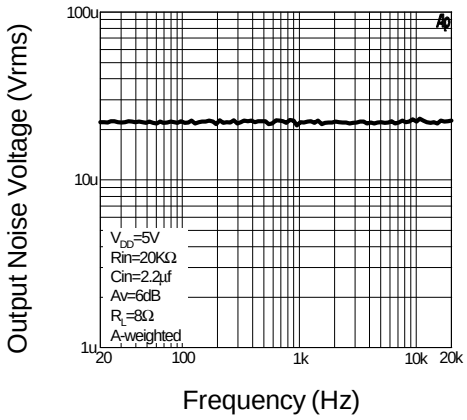
Shutdown Attenuation vs. Frequency



Shutdown Attenuation vs. Frequency

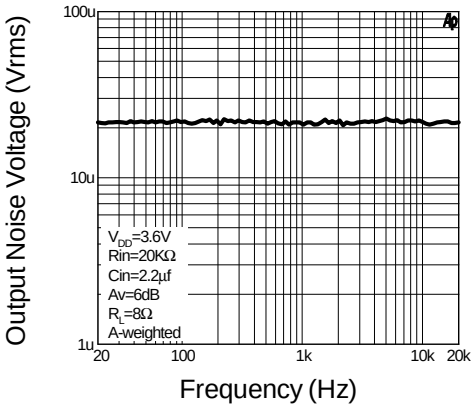


Output Noise Voltage vs. Frequency

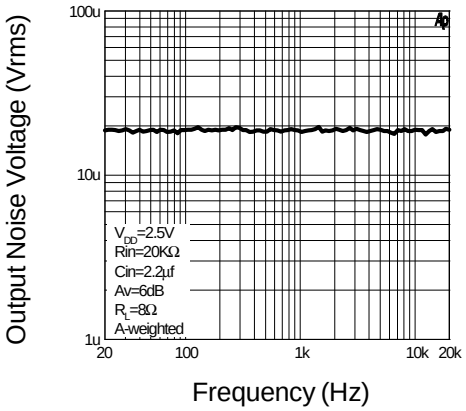


Typical Operating Characteristics (Cont.)

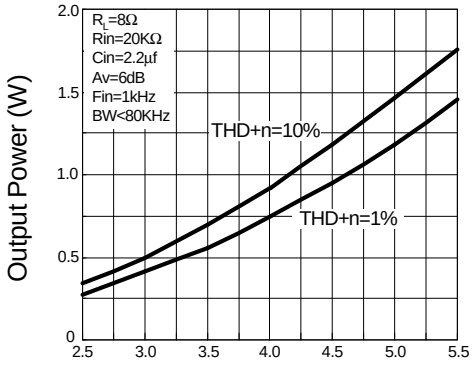
Output Noise Voltage vs. Frequency



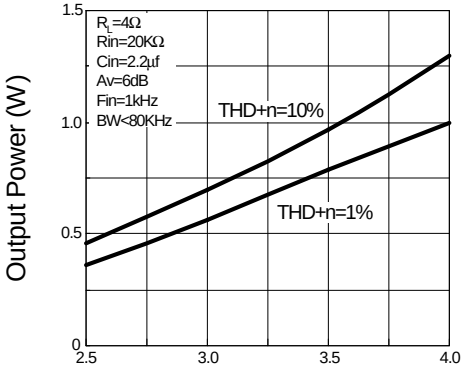
Output Noise Voltage vs. Frequency



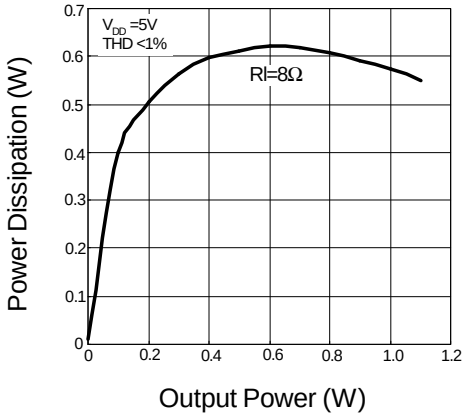
Output Power vs. Supply Voltage



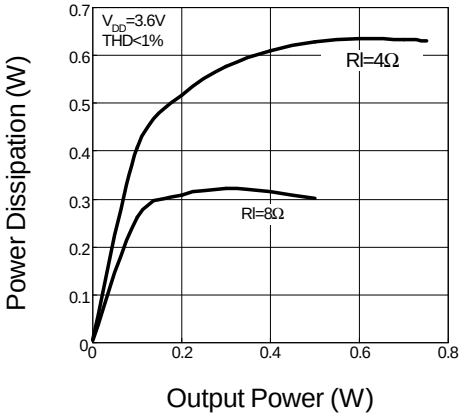
Output Power vs. Supply Voltage



Power Dissipation vs. Output Power

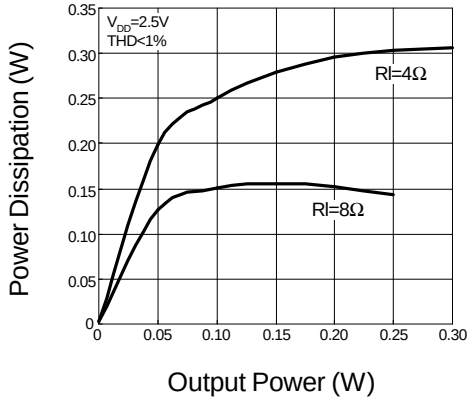


Power Dissipation vs. Output Power

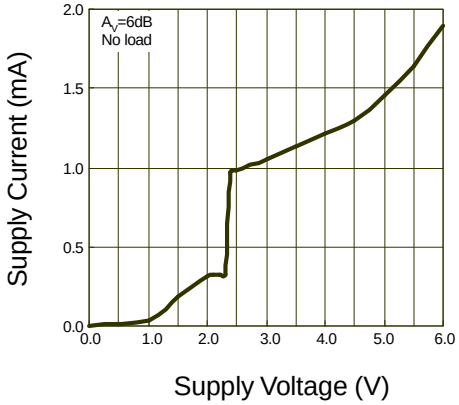


Typical Operating Characteristics (Cont.)

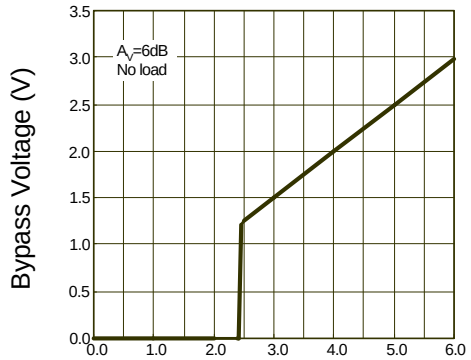
Power Dissipation vs. Output Power



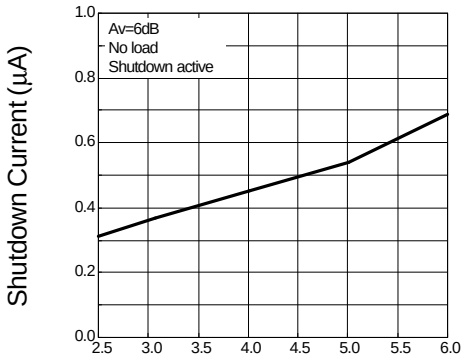
Supply Current vs. Supply Voltage



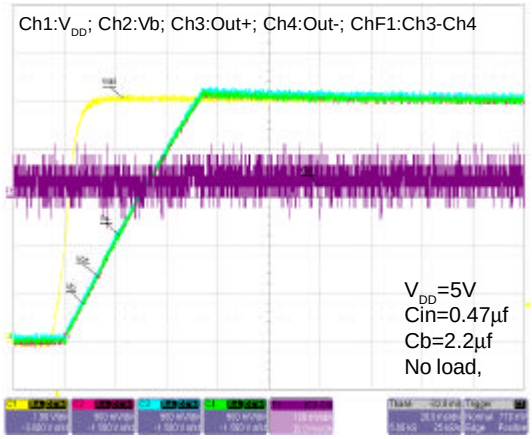
Bypass Voltage vs. Supply Voltage



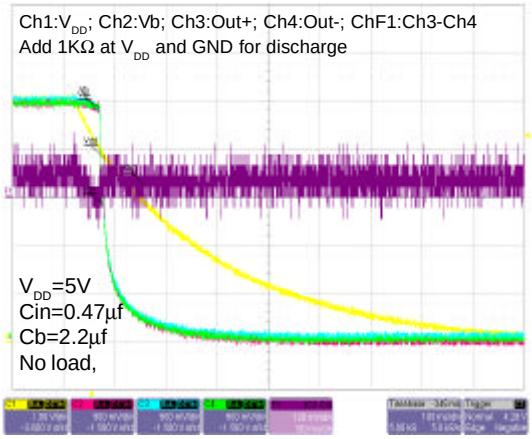
Shutdown Current vs. Supply Voltage



Power On Waveform



Power Off Waveform



Application Descriptions

BTL Operation

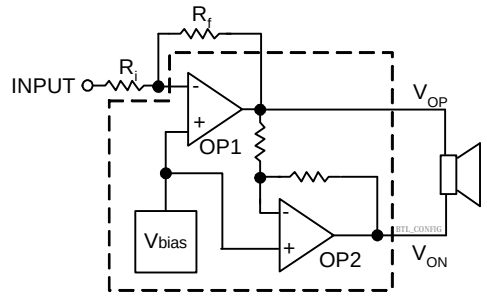


Figure1: APA0712 power amplifier internal configuration

The power amplifier OP1 gain is set by external gain setting, while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2X (Gain of SE mode).

By driving the load differentially through outputs V_{OP} and $V_{ON,}$ an amplifier configuration commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage. Four times the output power is possible as compared to a SE amplifier under the same conditions.

A BTL configuration, such as the one used in APA0712, also creates a second advantage over SE amplifiers. Since the differential outputs, V_{OP}, V_{ON} are biased at half supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor, which is required in a single supply, SE configuration.

Input Resistance, R_i

The gain of the APA0712 is set by the external resistors (R_i and R_f).

$$\text{BTL Gain} = -2 \times \frac{R_f}{R_i} \qquad (1)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. The input resistance will affect the low frequency performance of audio signal.

Input Capacitor, C_i

In the typical application an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i from a high-pass filter with the corner frequency determined in the follow equation:

$$F_{C(highpass)} = \frac{1}{2\pi R_i C_i} \qquad (2)$$

The value of C_i is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where R_i is 20kΩ and the specification calls for a flat bass response down to 40Hz. Equation is reconfigured as follow:

$$C_i = \frac{1}{2\pi R_i F_c} \qquad (3)$$

Consider to input resistance variation, the C_i is 0.2µF so one would likely choose a value in the range of 0.22µF to 1.0µF.A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held

Application Descriptions (Cont.)

Input Capacitor, C_i (Cont.)

at $V_{DD}/2$, which is likely higher that the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_B

As other power amplifiers, proper supply by- passing is critical for low noise performance and high power supply rejection.

The capacitors located on the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor will improve PSRR due to increased half-supply stability. Typical application employ a 5V regulator with 1.0µF and a 0.1µF bypass as supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA0712. The selection of bypass capacitors, especially C_B, is thus dependent upon desired PSRR requirements, click and pop performance.

To avoid start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (4) should be maintained

$$C_B \frac{V_B}{65\mu A} + 50mS > 2\pi (R_i + R_f) C_i \qquad (4)$$

The bypass capacitor is fed from an 80kΩ resistor inside the amplifier. Bypass capacitor, C_B, values of 1µF to 2.2µF ceramic or tantalum low-ESR capacitors are recommended for the best THD+N and noise performance. The bypass capacitance also effects to the start up time. It is determined in the following equation

$$T_{start\,up} = C_B \frac{V_B}{65\mu A} + 50mS \qquad (5)$$

Power Supply Decoupling, C_s

The APA0712 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the APA0712 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on.

Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry. The value of C_i will also affect turn-on pops (refer to Effective Bypass Capacitance). The bypass voltage rise up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of C_B can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of C_B, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_B and the turn-on time.

In the most cases, choosing a small value of C_i in the

Application Descriptions (Cont.)

Optimizing Depop Circuitry (Cont.)

range of 0.22µF to 0.47µF, C_B being equal to 2.2µF should produce a virtually click-less and pop-less turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. So it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption while not in use, the APA0712 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin for APA0712. The trigger point between a logic high and logic low level is typically $0.4V_{DD}$. It is best to switch between ground and the supply voltage V_{DD} to provide maximum device performance. By switching the $\overline{SD}$ pin to low level, the amplifier enters a low-consumption-current state, I_{DD} for APA0712 is in shutdown mode. On normal operating, APA0712's $\overline{SD}$ pin should pull to high level to keeping the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state changes.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (6)$$

Where:

$$P_O = \frac{V_{O.RMS}^{\ 2}}{R_L} = \frac{V_P^{\ 2}}{2R_L} \quad (7)$$

$$V_{O.RMS} = \frac{V_P}{\sqrt{2}} \quad (8)$$

$$P_{SUP} = V_{DD} \times I_{DD.AVG} = V_{DD}\frac{2V_P}{\pi R_L} \quad (9)$$

Efficiency of a BTL configuration:

$$\frac{P_O}{P_{SUP}} = \frac{\frac{V_P^{\ 2}}{2R_L}}{V_{DD} \times \frac{2V_P}{\pi R_L}} = \frac{\pi V_P}{4V_{DD}} \quad (10)$$

Table 1 employs equation10 to calculate efficiencies for four different output power levels when load is 8Ω. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a near flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a mono 1.4W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 1.5W.

Po (W)	Efficiency (%)	I_{DD}(A)	V_{PP}(V)	P_D (W)
0.2	28.34	0.14	1.79	0.55
0.5	44.94	0.22	2.83	0.55
0.7	53.12	0.26	3.35	0.50
1.0	63.59	0.32	4.00	0.35

****High peak voltages cause the THD+N to increase**.

Table 1. Efficiency Vs Output Power in 5-V/8Ω Differential Amplifier Systems

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation10, V_{DD} is in the denominator.

This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equa-

Application Descriptions (Cont.)

Power Dissipation (Cont.)

tion11 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode:}\quad P_{D.MAX} = \frac{V_{DD}^{2}}{2\pi^{2}R_{L}} \qquad (11)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode:}\quad P_{D.MAX} = 2\frac{V_{DD}^{2}}{\pi^{2}R_{L}} \qquad (12)$$

Even with this substantial increase in power dissipation, the APA0712 does not require extra heat-sink. The power dissipation from equation12, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation13:

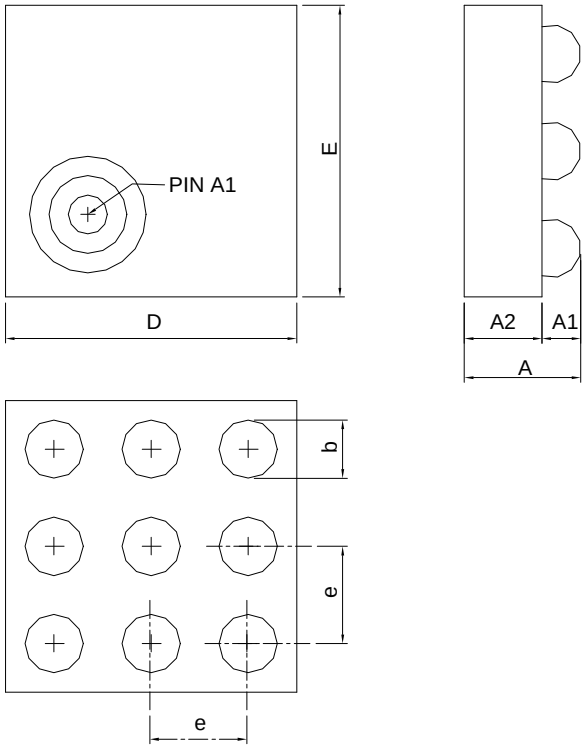
$$P_{D.MAX} = \frac{T_{J.MAX} - T_{A}}{\theta_{JA}} \qquad (13)$$

For WLCSP-9, the thermal resistance (θ_{JA}) is equal to 165°C/W.

Since the maximum junction temperature ($T_{J.MAX}$) of APA0712 is 150°C and the ambient tem- perature (T_A) is defined by the power system design, the maximum power dissipation, which the IC package is able to handle, can be obtained from equation13. Once the power dissipation is greater than the maximum limit ($P_{D.MAX}$), the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

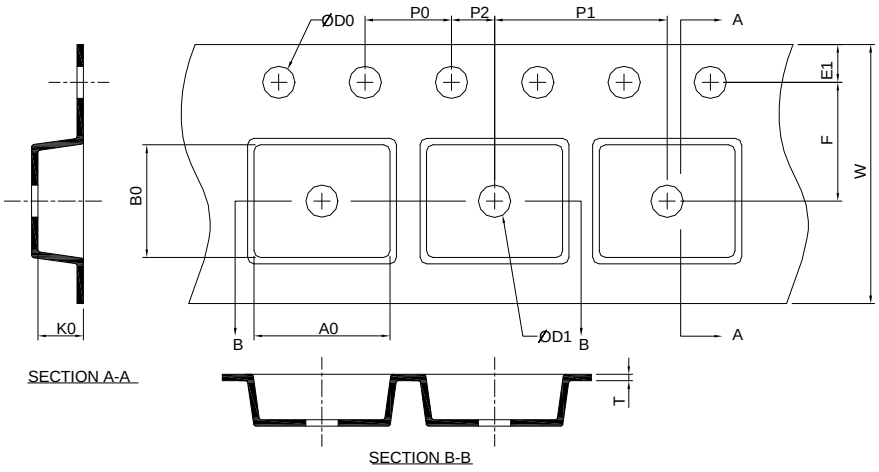
Package Information

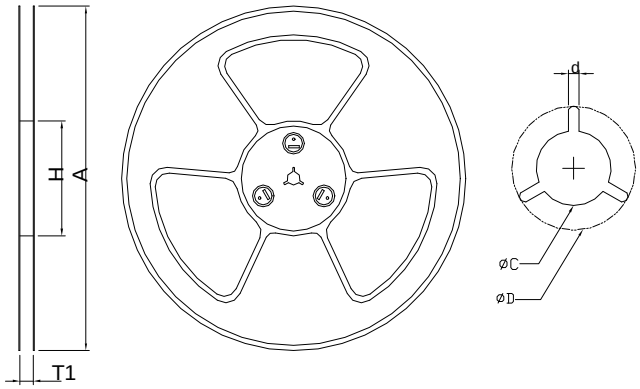
WLCSP - 9



SYMBOL	WLCSP1.5x1.5-9			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.53	0.67	0.021	0.026
A1	0.20	0.24	0.008	0.009
A2	0.33	0.43	0.013	0.017
b	0.29	0.31	0.011	0.012
D	1.47	1.53	0.058	0.060
E	1.47	1.53	0.058	0.060
e	0.50 BSC		0.020 BSC	

Carrier Tape & Reel Dimensions





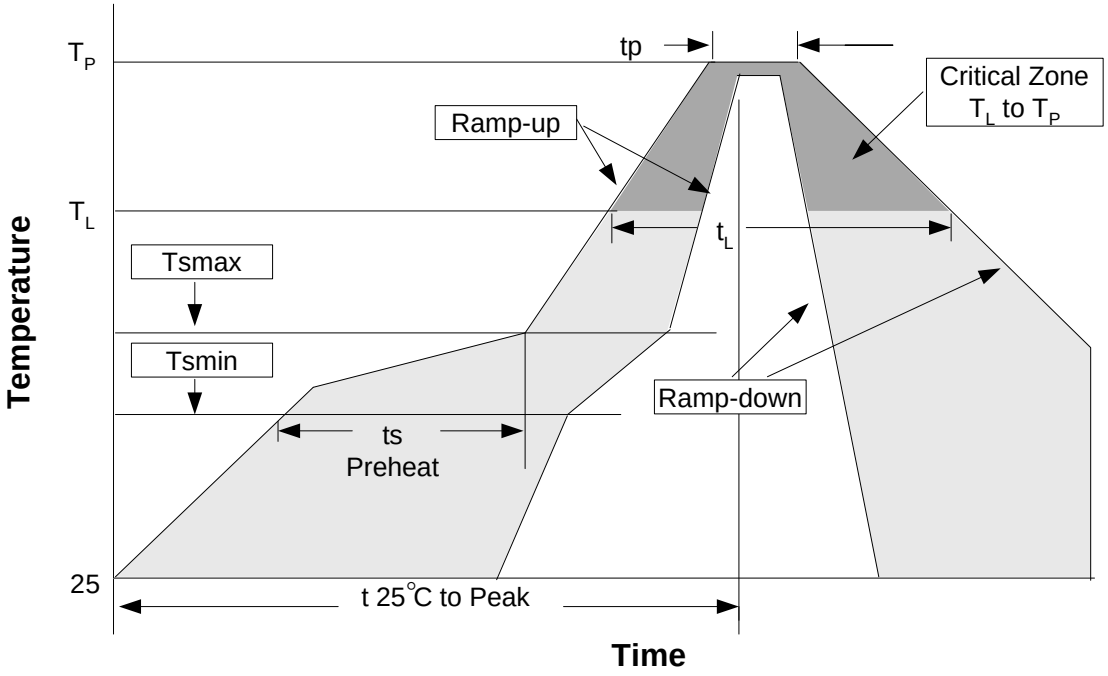
Application	A	H	T1	C	d	D	W	E1	F
WLCSP-9 (1.5*1.5)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	7.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.70±0.10	1.70±0.10	0.90±0.10

(mm)

Devices Per Unit

Package Type	Unit	Devices Per Reel
WLCSP-9	Tape & Reel	3000

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY*	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

* Solderability test doesn't apply to "WLCSP-9".

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

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