

OptiMOS™ 3 Power-Transistor
Features

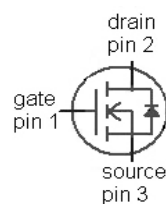
- Fast switching MOSFET for SMPS
- Optimized technology for DC/DC converters
- Qualified according to JEDEC¹⁾ for target applications
- N-channel, logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Avalanche rated
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	14.7	mΩ
I_D	20	A



Type	IPP147N03L G	IPB147N03L G
		
Package	PG-TO220-3-1	PG-TO263-3
Marking	147N03L	147N03L



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	20	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	20	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	20	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	20	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	140	
Avalanche current, single pulse ³⁾	I_{AS}	$T_C=25\text{ °C}$	20	
Avalanche energy, single pulse	E_{AS}	$I_D=10\text{ A}, R_{GS}=25\text{ Ω}$	20	mJ
Reverse diode dv/dt	dv/dt	$I_D=20\text{ A}, V_{DS}=24\text{ V}, di/dt=200\text{ A/μs}, T_{j,max}=175\text{ °C}$	6	kV/μs
Gate source voltage	V_{GS}		±20	V

¹⁾ J-STD20 and JESD22

Maximum ratings, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	$T_c=25\text{ }^{\circ}\text{C}$	31	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	4.9	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁴⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	30	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\text{ }\mu\text{A}$	1	-	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ }^{\circ}\text{C}$	-	0.1	1	μA
		$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ }^{\circ}\text{C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance ⁵⁾	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}, I_{\text{D}}=20\text{ A}$	-	17.4	21.7	m Ω
		$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=20\text{ A}$	-	12.3	14.7	
Gate resistance	R_{G}		-	1.2	-	Ω
Transconductance	g_{fs}	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=20\text{ A}$	17	34	-	S

²⁾ See figure 3 for more detailed information

³⁾ See figure 13 for more detailed information

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁵⁾ Measured from drain tab to source pin

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	770	1000	pF
Output capacitance	C_{oss}		-	350	470	
Reverse transfer capacitance	C_{rss}		-	16	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=1.6\ \Omega$	-	3.1	-	ns
Rise time	t_r		-	2.4	-	
Turn-off delay time	$t_{d(off)}$		-	12	-	
Fall time	t_f		-	2.0	-	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	2.7	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.2	-	
Gate to drain charge	Q_{gd}		-	1.2	-	
Switching charge	Q_{sw}		-	2.7	-	
Gate charge total	Q_g		-	4.8	-	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V
Gate charge total	Q_g	$V_{DD}=15\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	10	-	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	4.2	-	
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	9.0	-	

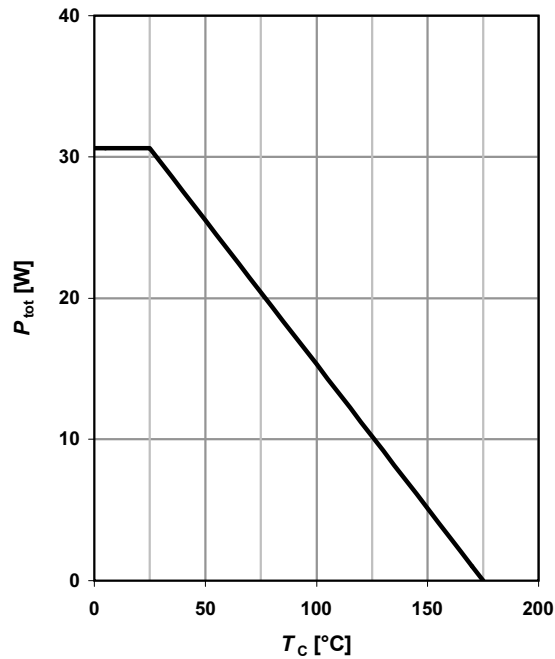
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	20	A
Diode pulse current	$I_{S,pulse}$		-	-	140	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=20\text{ A},$ $T_j=25\text{ °C}$	-	0.95	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

⁵⁾ See figure 16 for gate charge parameter definition

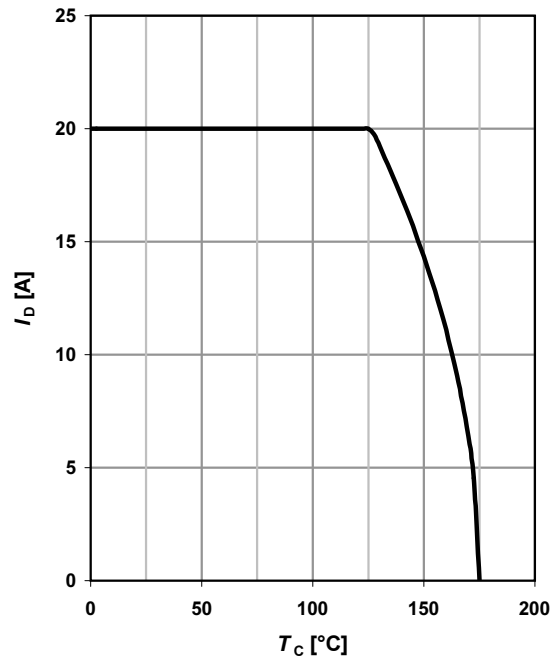
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

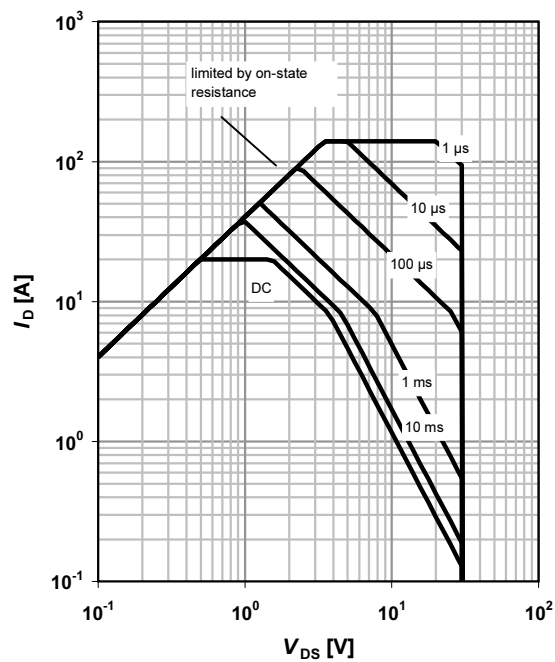
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^{\circ}\text{C}; D = 0$$

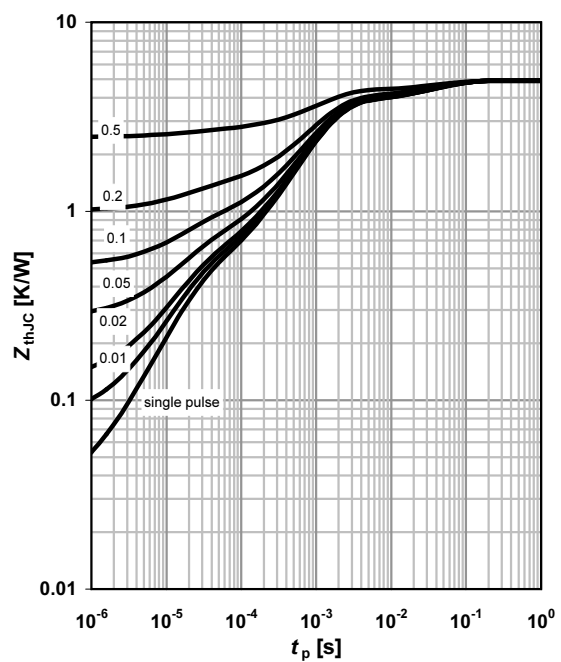
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

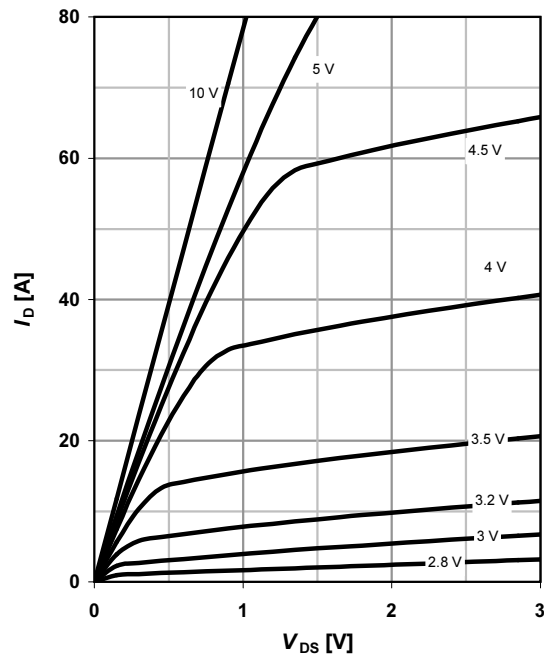
parameter: $D = t_p/T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_J = 25^\circ\text{C}$$

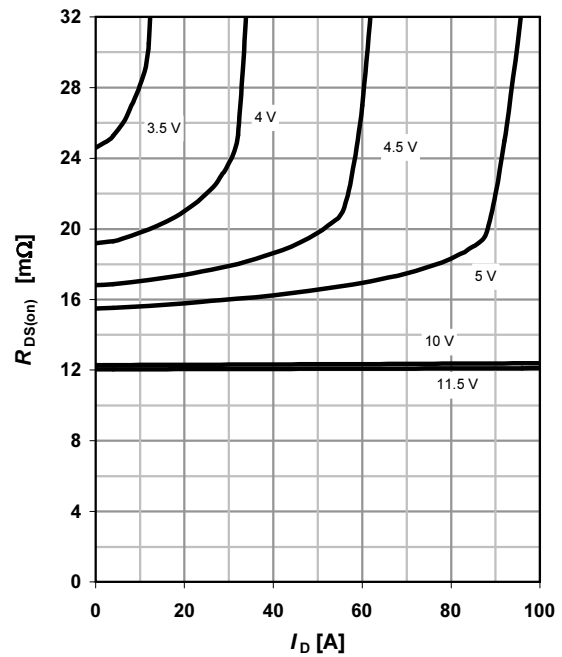
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_J = 25^\circ\text{C}$$

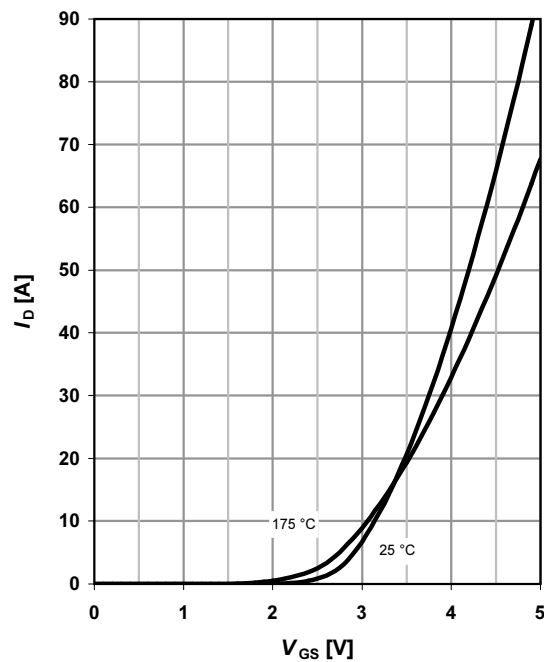
parameter: V_{GS}



7 Typ. transfer characteristics

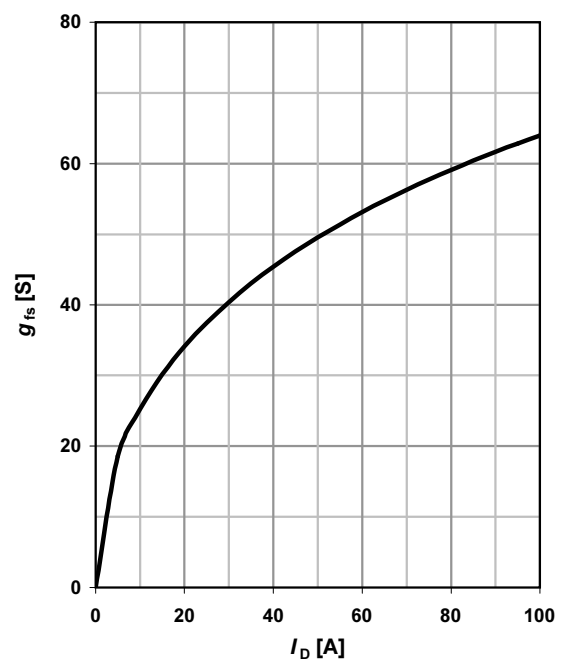
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

parameter: T_J



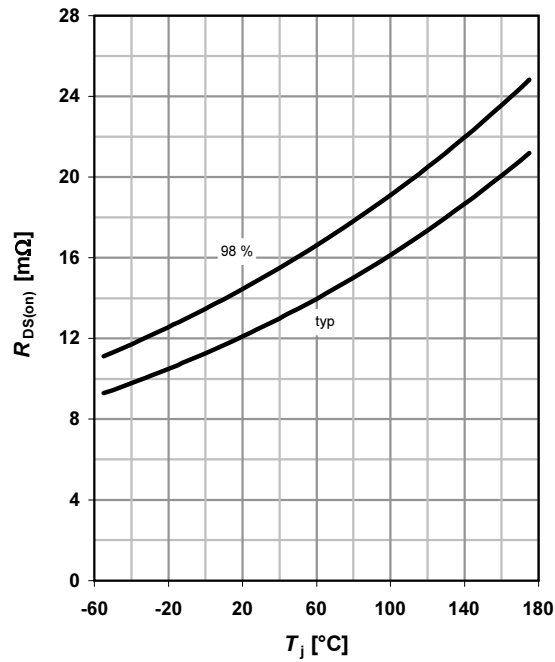
8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_J = 25^\circ\text{C}$$



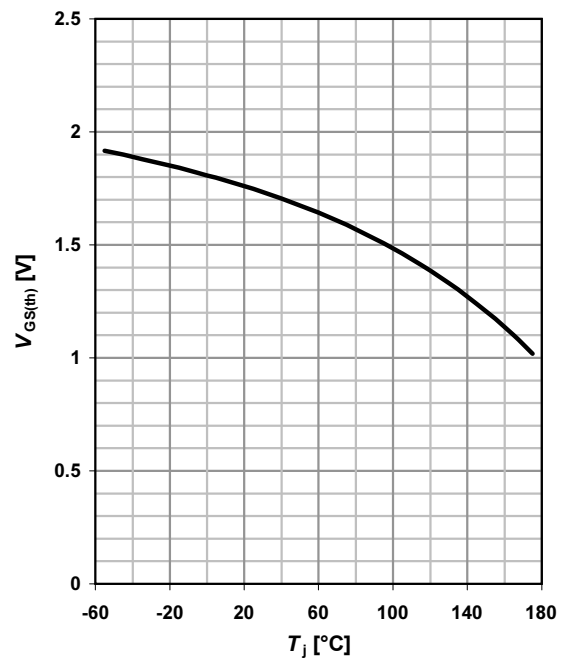
9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 20 \text{ A}; V_{GS} = 10 \text{ V}$$



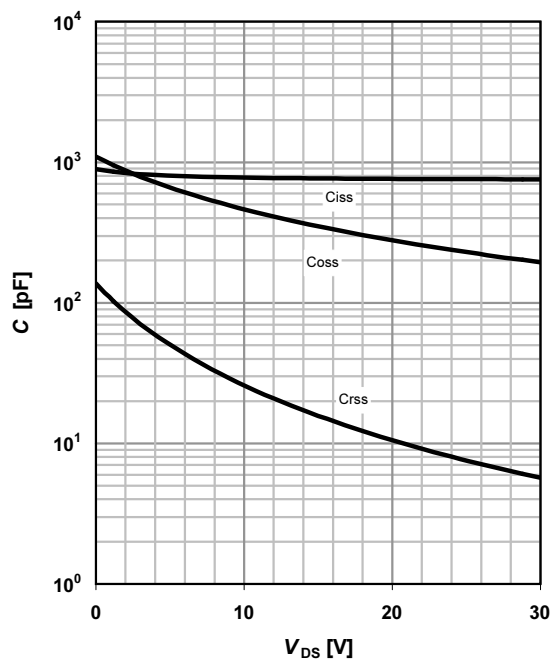
10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \text{ μA}$$



11 Typ. capacitances

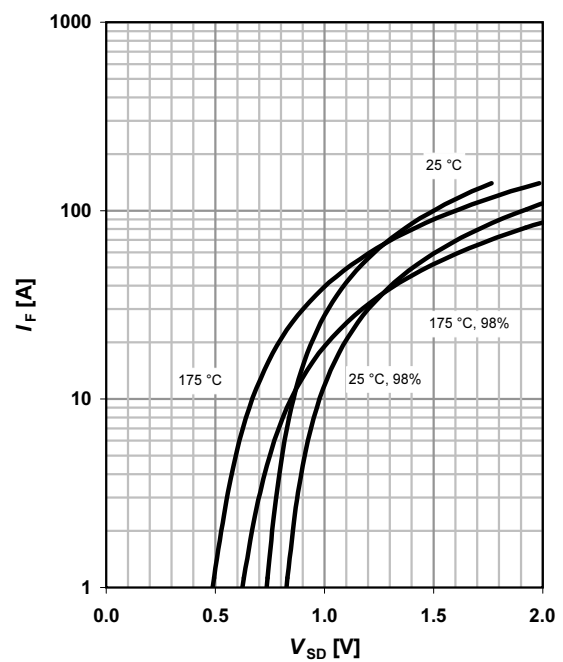
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

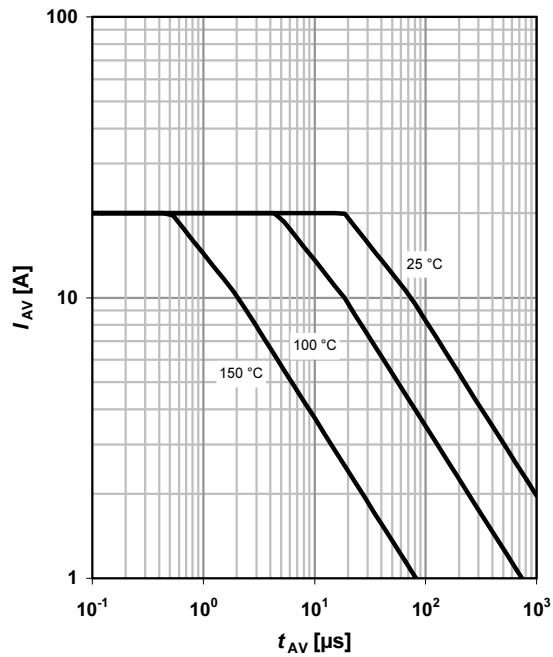
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

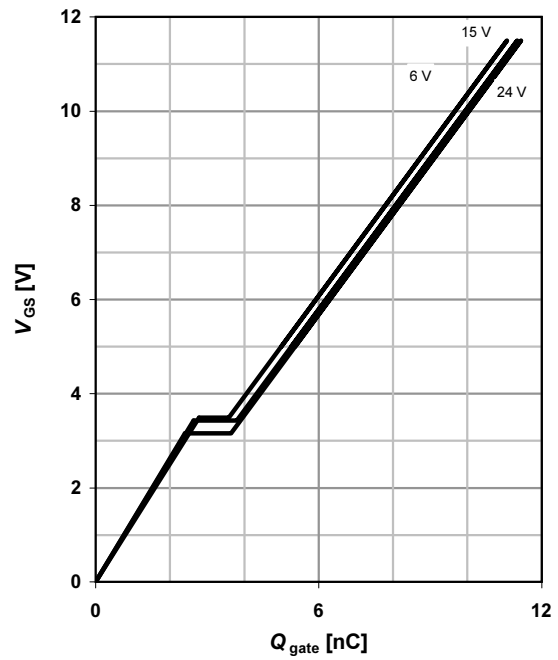
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

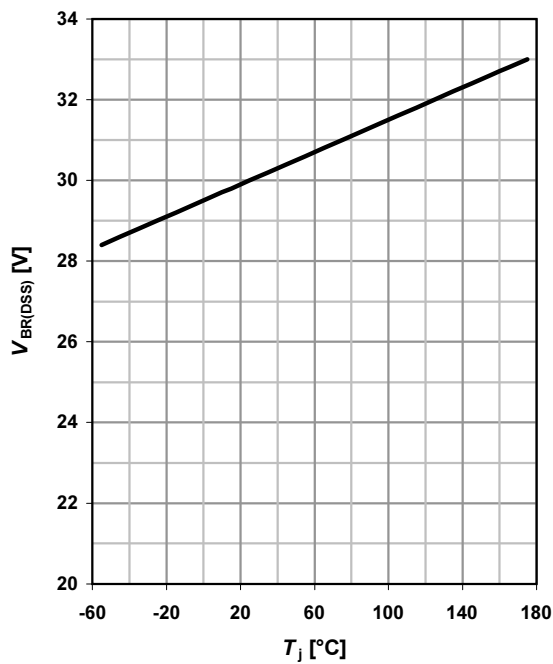
$$V_{GS}=f(Q_{\text{gate}}); I_D=20\ \text{A pulsed}$$

parameter: V_{DD}

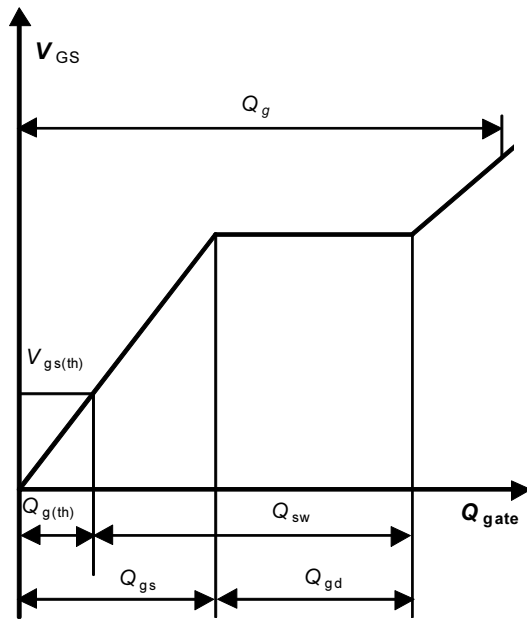


15 Drain-source breakdown voltage

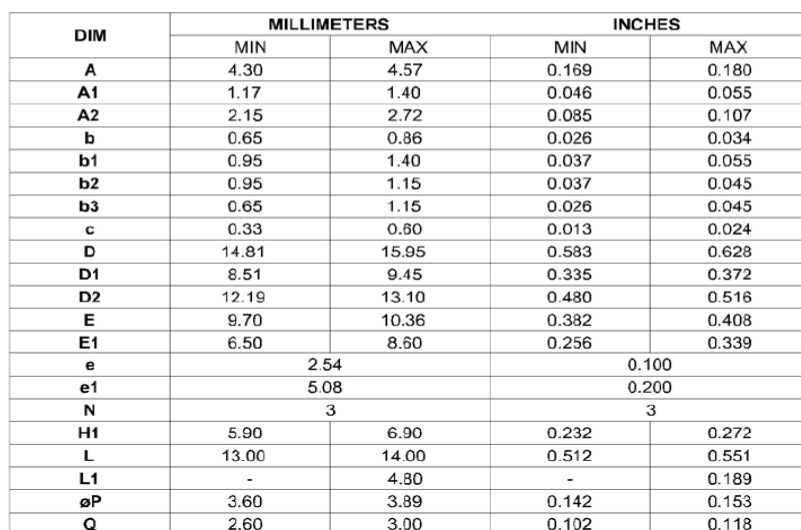
$$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$$



16 Gate charge waveforms

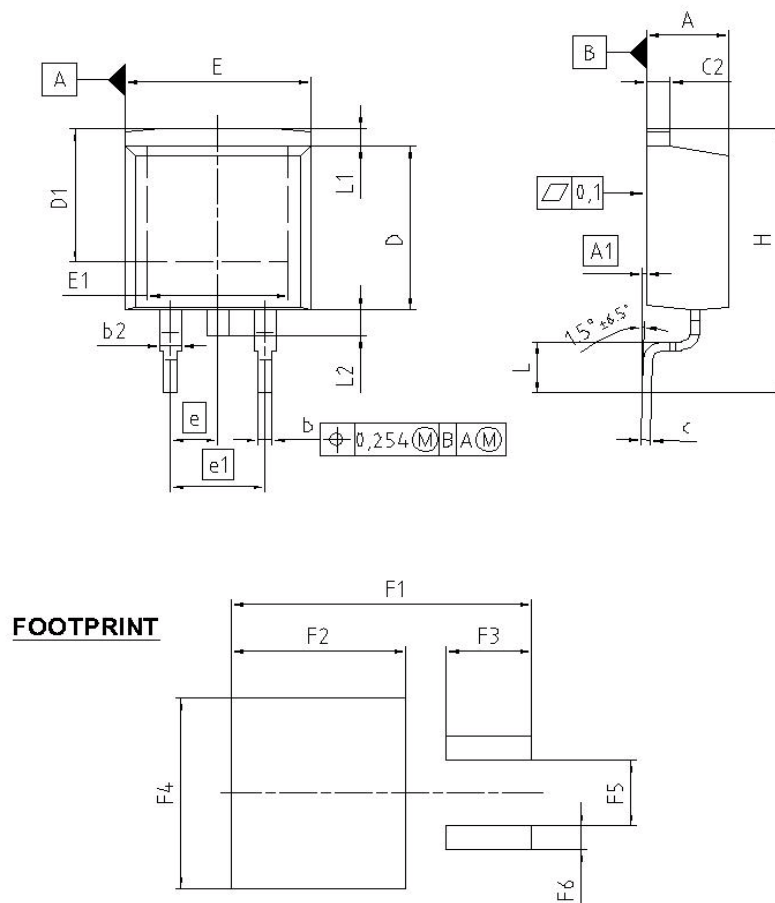


PG-TO220-3-1

2010-04-27

Package Outline

PG-TO263-3



FOOTPRINT

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	0.000	0.254	0.000	0.010
b	0.650	0.850	0.026	0.033
b2	0.950	1.321	0.037	0.052
c	0.330	0.650	0.013	0.026
c2	0.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	7.100	-	0.280	-
E	9.800	10.312	0.386	0.406
E1	6.500	-	0.256	-
e	2.540		0.100	
e1	5.080		0.200	
N	2		2	
H	14.605	15.875	0.575	0.625
L	2.200	3.000	0.087	0.118
L1	-	1.600	-	0.063
L2	1.000	1.778	0.039	0.070
F1	16.050	16.250	0.632	0.640
F2	9.300	9.500	0.366	0.374
F3	4.500	4.700	0.177	0.185
F4	10.700	10.900	0.421	0.429
F5	3.630	3.830	0.143	0.151
F6	1.100	1.300	0.043	0.051

REFERENCE JEDEC TO263
SCALE 0 5 10 7.5mm
EUROPEAN PROJECTION 
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FILE TO263_2

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