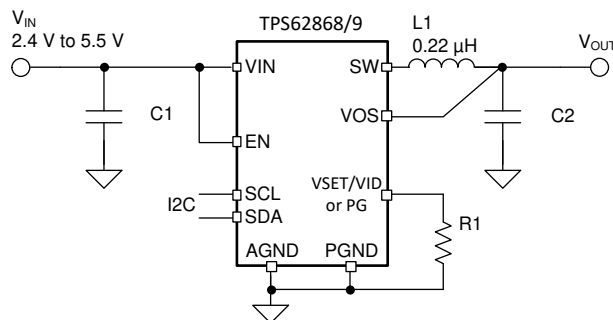


# TPS62868x 2.4-V to 5.5-V Input, 4-A/6-A Synchronous Step-Down Converter with I<sup>2</sup>C Interface in QFN Package

## 1 Features

- 11-mΩ and 10.5-mΩ internal power MOSFETs
- >90% efficiency (0.9-V output)
- DCS-Control topology for fast transient response
- Available output voltage ranges for dynamic voltage scaling (DVS) through I<sup>2</sup>C
  - Output voltage range from 0.2-V to 0.8375-V with 2.5-mV step size
  - Output voltage range from 0.4-V to 1.675-V with 5-mV step size
  - Output voltage range from 0.8-V to 3.35-V with 10-mV step size
- 1% output voltage accuracy
- 2.4-MHz switching frequency
- Selection by external resistor
  - Start-up output voltage
  - I<sup>2</sup>C slave address
- Selection by I<sup>2</sup>C interface
  - Power save mode or forced PWM mode
  - Output discharge
  - Hiccup or latching short-circuit protection
  - Output voltage ramp speed
- Thermal pre-warning and thermal shutdown
- Power good indicator pin option with window comparator
- I<sup>2</sup>C-compatible interface up to 3.4 Mbps
- Available in 1.5-mm x 2.5-mm x 1.0-mm 9-pin QFN package with 0.5-mm pitch
- Also available in WCSP package: [TPS62866, 6-A synchronous step-down converter with I<sup>2</sup>C interface in 1.05-mm x 1.78-mm WCSP package](#)
- Create a custom design using with TPS62868/9 with the [WEBENCH® Power Designer](#)



Typical Application

## 2 Applications

- [Core supply for FPGAs, CPUs, ASICs, or video chipsets](#)
- [IP network camera](#)
- [Solid-state drives](#)
- [Optical modules](#)
- LPDDR5 VDDQ rail supply

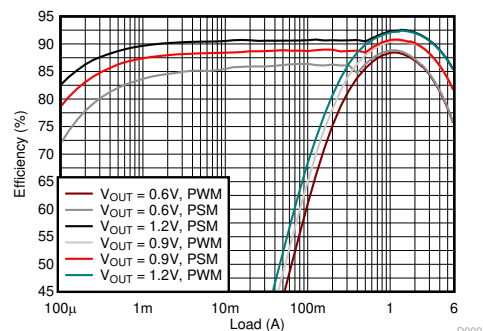
## 3 Description

The TPS62868 and TPS62869 devices are high-frequency synchronous step-down converters with I<sup>2</sup>C interface which provide an efficient, adaptive, and high power-density solution. At medium to heavy loads, the converter operates in PWM mode and automatically enters Power Save Mode operation at light load to maintain high efficiency over the entire load current range. The device can also be forced in PWM mode operation for smallest output voltage ripple. Together with its DCS-Control architecture, excellent load transient performance and tight output voltage accuracy are achieved. Through the I<sup>2</sup>C interface and a dedicated VID pin, the output voltage is quickly adjusted to adapt the power consumption of the load to the ever-changing performance needs of the application.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TPS62868	QFN (9)	1.5 x 2.5 x 1.0 mm
TPS62869		

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency at V<sub>IN</sub> = 3.3 V



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

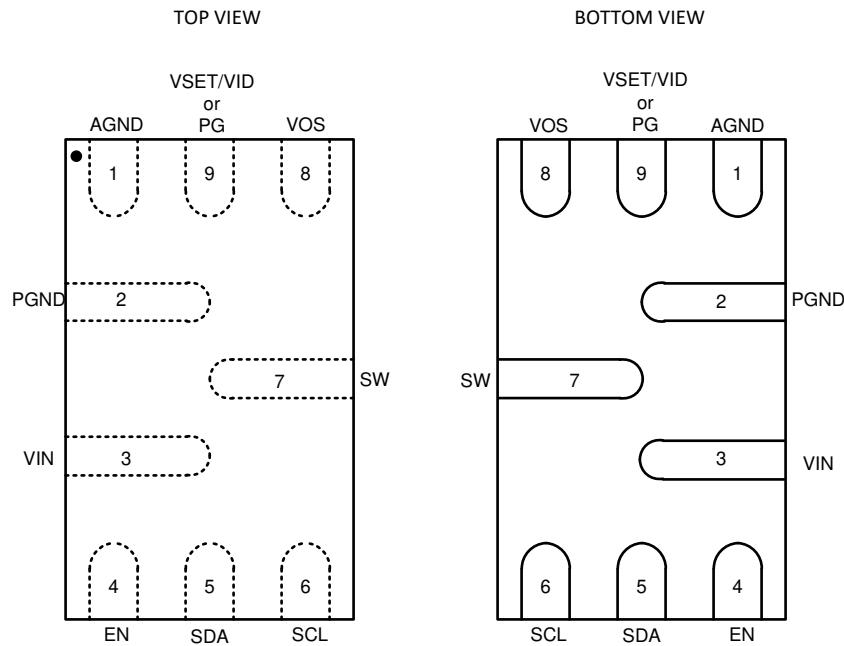
Changes from Revision * (September 2020) to Revision A (December 2020)	Page
• Changed device status from Advance Information to Production Data.....	1

## 5 Device Options

PART NUMBER <sup>(1)</sup>	FULL OUTPUT VOLTAGE RANGE	START-UP OUTPUT VOLTAGE	DVS STEP SIZE	OUTPUT CURRENT	VID OR PG PIN
TPS628680ARQY	0.2 V to 0.8375 V	0.2 V to 0.575 V, Selectable	2.5 mV	4 A	VID
TPS628680CRQY					PG
TPS628681ARQY	0.4 V to 1.675 V	0.4 V to 1.15 V, Selectable	5 mV		VID
TPS628681CRQY					PG
TPS628682ARQY	0.8 V to 3.35 V	0.8 V to 2.3 V, Selectable	10 mV		VID
TPS628682CRQY					PG
TPS628690ARQY	0.2 V to 0.8375 V	0.2 V to 0.575 V, Selectable	2.5 mV	6 A	VID
TPS628690CRQY					PG
TPS628691ARQY	0.4 V to 1.675 V	0.4 V to 1.15 V, Selectable	5 mV		VID
TPS628691CRQY					PG
TPS628692ARQY	0.8 V to 3.35 V	0.8 V to 2.3 V, Selectable	10 mV		VID
TPS628692CRQY					PG

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 6 Pin Configuration and Functions



**Figure 6-1. 9-Pin RQY QFN Package (Top View)**

**Table 6-1. Pin Functions**

PIN		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground pin
VSET/VID	9	Start-up output voltage and device address selection pin. An external resistor must be connected. After start-up, the pin can be used to select the $V_{OUT}$ registers for the output voltage (Low = $V_{OUT}$ register 1; high = $V_{OUT}$ register 2). See <a href="#">Section 8.4.4</a> . This pin is pulled to GND when the device is in shutdown. The function after start-up depends on the device option. See the <a href="#">Device Options</a> .
PG	9	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave it floating. This pin is pulled to GND when the device is in shutdown. The function after start-up depends on the device option. See <a href="#">Section 5</a> .
VOS	8	Output voltage sense pin. This pin must be directly connected to the output capacitor.
PGND	2	Power ground pin
SW	7	Switch pin of the power stage
VIN	3	Power supply input voltage pin
EN	4	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
SDA	5	I <sup>2</sup> C serial data pin. Do not leave it floating. Connect it to AGND if not used.
SCL	6	I <sup>2</sup> C serial clock pin. Do not leave it floating. Connect it to AGND if not used.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	VIN, EN, SDA, SCL, VOS, VSET/VID, VSET/PG	-0.3	6	V
	SW (DC)	-0.3	V <sub>IN</sub> + 0.3	
	SW (AC, less than 10ns) <sup>(3)</sup>	-2.5	10	
I <sub>SOURCE_PG</sub>	Source current at VSET/PG		1	mA
I <sub>SINK_SDA,SCL</sub>	Sink current at SDA, SCL		2	mA
T <sub>J</sub>	Junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) While switching.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	2.4		5.5	V
t <sub>F_VIN</sub>	Falling transition time at VIN <sup>(1)</sup>			10	mV/μs
I <sub>OUT</sub>	Output current, TPS62868 <sup>(2)</sup>	0		4	A
	Output current, TPS62869 <sup>(3)</sup>	0		6	
T <sub>J</sub>	Junction temperature	-40		125	°C

- (1) The falling slew rate of V<sub>IN</sub> should be limited if V<sub>IN</sub> goes below V<sub>UVLO</sub>.
- (2) Lifetime is reduced when operating continuously at 4-A output current and the junction temperature is higher than 105 °C.
- (3) Lifetime is reduced when operating continuously at 6-A output current and the junction temperature is higher than 85 °C.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS62868/ TPS62869 RQY		UNIT
		JEDEC 51-7	TPS62869RQYEVN-118	
		15 PINS	15 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	90.9	60.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	68.2	n/a <sup>(2)</sup>	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	25.0	n/a <sup>(2)</sup>	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.9	3.3	°C/W

THERMAL METRIC <sup>(1)</sup>		TPS62868/ TPS62869 RQY		UNIT
		JEDEC 51-7	TPS62869RQYEVM-118	
		15 PINS	15 PINS	
$\Psi_{JB}$	Junction-to-board characterization parameter	24.7	31.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Not applicable to an EVM.

## 7.5 Electrical Characteristics

$T_J = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ , and  $V_{IN} = 2.4\text{ V}$  to  $5.5\text{ V}$ . Typical values are at  $T_J = 25\text{ }^\circ\text{C}$  and  $V_{IN} = 5\text{ V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_Q$	Quiescent current	EN = High, no load, device not switching		4	10	$\mu\text{A}$
$I_{Q,VOS}$	Operating quiescent current into VOS pin	EN = High, no load, device not switching, $V_{VOS} = 1.8\text{ V}$ , TPS6286x1A/C		18		$\mu\text{A}$
$I_{SD}$	Shutdown current	EN = Low, $T_J = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$		0.24	1	$\mu\text{A}$
$V_{UVLO}$	Under voltage lock out threshold	$V_{IN}$ rising	2.2	2.3	2.4	V
		$V_{IN}$ falling	2.1	2.2	2.3	V
$T_{JW}$	Thermal warning threshold	$T_J$ rising		130		$^\circ\text{C}$
	Thermal warning hysteresis	$T_J$ falling		20		$^\circ\text{C}$
$T_{JSD}$	Thermal shutdown threshold	$T_J$ rising		150		$^\circ\text{C}$
	Thermal shutdown hysteresis	$T_J$ falling		20		$^\circ\text{C}$
<b>LOGIC INTERFACE EN, SDA, SCL</b>						
$V_{IH}$	High-level input threshold voltage at EN, SCL, SDA, VSET/VID		1.0			V
$V_{IL}$	Low-level input threshold voltage at EN, SCL, SDA, VSET/VID				0.4	V
$I_{SCL,LKG}$	Input leakage current into SCL pin			0.01	0.8	$\mu\text{A}$
$I_{SDA,LKG}$	Input leakage current into SDA pin			0.01	0.1	$\mu\text{A}$
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	0.1	$\mu\text{A}$
$C_{SCL}$	Parasitic capacitance at SCL			1		pF
$C_{SDA}$	Parasitic capacitance at SDA			2.4		pF
<b>STARTUP, POWER GOOD</b>						
$t_{Delay}$	Enable delay time	Time from EN high to device starts switching, $R1 = 249\text{ k}\Omega$	420	700	1100	$\mu\text{s}$
$t_{Ramp}$	Output voltage ramp time	Time from device starts switching to power good	0.85	1	1.5	ms
$V_{PG}$	Power good lower threshold	$V_{VOS}$ referenced to $V_{OUT}$ nominal	85	91	96	%
	Power good upper threshold	$V_{VOS}$ referenced to $V_{OUT}$ nominal	103	111	120	%
$t_{PG,DLY}$	Power good deglitch delay	Rising and falling edges		34		$\mu\text{s}$
<b>OUTPUT</b>						
$V_{OUT}$	Output voltage accuracy	FPWM, no Load, $T_J = 0\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$	-1		1	%
		FPWM, no Load	-2		2	%
$I_{VOS,LKG}$	Input leakage current into VOS pin	EN = Low, Output discharge disabled, $V_{VOS} = 1.8\text{ V}$ , TPS6286x1A/C		0.2	2.5	$\mu\text{A}$
$R_{DIS}$	Output discharge resistor at VOS pin			3.5		$\Omega$
	Load regulation	$V_{OUT} = 0.9\text{ V}$ , FPWM		0.04		%/A
<b>POWER SWITCH</b>						
$R_{DS(on)}$	High-side FET on-resistance			11		m $\Omega$
	Low-side FET on-resistance			10.5		m $\Omega$
$I_{LIM}$	High-side FET forward current limit	TPS62868	5	5.5	6	A
		TPS62869	7	7.7	8.5	A
	Low-side FET forward current limit	TPS62868		4.5		A
		TPS62869		6.5		A
Low-side FET negative current limit	TPS62868, TPS62869		-3		A	
$f_{SW}$	PWM switching frequency	$I_{OUT} = 1\text{ A}$ , $V_{OUT} = 0.9\text{ V}$		2.4		MHz

## 7.6 I<sup>2</sup>C Interface Timing Characteristics

PARAMETER (1) (2)		TEST CONDITIONS	MIN	MAX	UNIT
f <sub>(SCL)</sub>	SCL Clock Frequency	Standard mode		100	kHz
f <sub>(SCL)</sub>	SCL Clock Frequency	Fast mode		400	kHz
f <sub>(SCL)</sub>	SCL Clock Frequency	Fast mode plus		1	MHz
f <sub>(SCL)</sub>	SCL Clock Frequency	High-speed mode (write operation), C <sub>B</sub> – 100 pF max		3.4	MHz
f <sub>(SCL)</sub>	SCL Clock Frequency	High-speed mode (read operation), C <sub>B</sub> – 100 pF max		3.4	MHz
f <sub>(SCL)</sub>	SCL Clock Frequency	High-speed mode (write operation), C <sub>B</sub> – 400 pF max		1.7	MHz
f <sub>(SCL)</sub>	SCL Clock Frequency	High-speed mode (read operation), C <sub>B</sub> – 400 pF max		1.7	MHz
t <sub>BUF</sub>	Bus Free Time Between a STOP and START Condition	Standard mode	4.7		μs
t <sub>BUF</sub>	Bus Free Time Between a STOP and START Condition	Fast mode	1.3		μs
t <sub>BUF</sub>	Bus Free Time Between a STOP and START Condition	Fast mode plus	0.5		μs
t <sub>HD</sub> , t <sub>STA</sub>	Hold Time (Repeated) START condition	Standard mode	4		μs
t <sub>HD</sub> , t <sub>STA</sub>	Hold Time (Repeated) START condition	Fast mode	600		ns
t <sub>HD</sub> , t <sub>STA</sub>	Hold Time (Repeated) START condition	Fast mode plus	260		ns
t <sub>HD</sub> , t <sub>STA</sub>	Hold Time (Repeated) START condition	High-speed mode	160		ns
t <sub>LOW</sub>	LOW Period of the SCL Clock	Standard mode	4.7		μs
t <sub>LOW</sub>	LOW Period of the SCL Clock	Fast mode	1.3		μs
t <sub>LOW</sub>	LOW Period of the SCL Clock	Fast mode plus	0.5		μs
t <sub>LOW</sub>	LOW Period of the SCL Clock	High-speed mode, C <sub>B</sub> – 100 pF max	160		ns
t <sub>LOW</sub>	LOW Period of the SCL Clock	High-speed mode, C <sub>B</sub> – 400 pF max	320		ns
t <sub>HIGH</sub>	HIGH Period of the SCL Clock	Standard mode	4		μs
t <sub>HIGH</sub>	HIGH Period of the SCL Clock	Fast mode	600		ns
t <sub>HIGH</sub>	HIGH Period of the SCL Clock	Fast mode plus	260		ns
t <sub>HIGH</sub>	HIGH Period of the SCL Clock	High-speed mode, C <sub>B</sub> – 100 pF max	60		ns
t <sub>HIGH</sub>	HIGH Period of the SCL Clock	High-speed mode, C <sub>B</sub> – 400 pF max	120		ns
t <sub>SU</sub> , t <sub>STA</sub>	Setup Time for a Repeated START Condition	Standard mode	4.7		μs
t <sub>SU</sub> , t <sub>STA</sub>	Setup Time for a Repeated START Condition	Fast mode	600		ns
t <sub>SU</sub> , t <sub>STA</sub>	Setup Time for a Repeated START Condition	Fast mode plus	260		ns
t <sub>SU</sub> , t <sub>STA</sub>	Setup Time for a Repeated START Condition	High-speed mode	160		ns
t <sub>SU</sub> , t <sub>DAT</sub>	Data Setup Time	Standard mode	250		ns
t <sub>SU</sub> , t <sub>DAT</sub>	Data Setup Time	Fast mode	100		ns
t <sub>SU</sub> , t <sub>DAT</sub>	Data Setup Time	Fast mode plus	50		ns
t <sub>SU</sub> , t <sub>DAT</sub>	Data Setup Time	High-speed mode	10		ns
t <sub>HD</sub> , t <sub>DAT</sub>	Data Hold Time	Standard mode	0	3.45	μs
t <sub>HD</sub> , t <sub>DAT</sub>	Data Hold Time	Fast mode	0	0.9	μs
t <sub>HD</sub> , t <sub>DAT</sub>	Data Hold Time	Fast mode plus	0		μs
t <sub>HD</sub> , t <sub>DAT</sub>	Data Hold Time	High-speed mode, C <sub>B</sub> – 100 pF max	0	70	ns
t <sub>HD</sub> , t <sub>DAT</sub>	Data Hold Time	High-speed mode, C <sub>B</sub> – 400 pF max	0	150	ns



## 7.6 I<sup>2</sup>C Interface Timing Characteristics (continued)

PARAMETER <sup>(1)</sup> <sup>(2)</sup>		TEST CONDITIONS	MIN	MAX	UNIT
t <sub>RCL</sub>	Rise Time of SCL Signal	Standard mode		1000	ns
t <sub>RCL</sub>	Rise Time of SCL Signal	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
t <sub>RCL</sub>	Rise Time of SCL Signal	Fast mode plus		120	ns
t <sub>RCL</sub>	Rise Time of SCL Signal	High-speed mode, C <sub>B</sub> – 100 pF max	10	40	ns
t <sub>RCL</sub>	Rise Time of SCL Signal	High-speed mode, C <sub>B</sub> – 400 pF max	20	80	ns
t <sub>RCL1</sub>	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	20 + 0.1 C <sub>B</sub>	1000	ns
t <sub>RCL1</sub>	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
t <sub>RCL1</sub>	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Fast mode plus		120	ns
t <sub>RCL1</sub>	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	High-speed mode, C <sub>B</sub> – 100 pF max	10	80	ns
t <sub>RCL1</sub>	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	High-speed mode, C <sub>B</sub> – 400 pF max	20	160	ns
t <sub>FCL</sub>	Fall Time of SCL Signal	Standard mode	20 + 0.1 C <sub>B</sub>	300	ns
t <sub>FCL</sub>	Fall Time of SCL Signal	Fast mode		300	ns
t <sub>FCL</sub>	Fall Time of SCL Signal	Fast mode plus		120	ns
t <sub>FCL</sub>	Fall Time of SCL Signal	High-speed mode, C <sub>B</sub> – 100 pF max	10	40	ns
t <sub>FCL</sub>	Fall Time of SCL Signal	High-speed mode, C <sub>B</sub> – 400 pF max	20	80	ns
t <sub>RDA</sub>	Rise Time of SDA Signal	Standard mode		1000	ns
t <sub>RDA</sub>	Rise Time of SDA Signal	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
t <sub>RDA</sub>	Rise Time of SDA Signal	Fast mode plus		120	ns
t <sub>RDA</sub>	Rise Time of SDA Signal	High-speed mode, C <sub>B</sub> – 100 pF max	10	80	ns
t <sub>RDA</sub>	Rise Time of SDA Signal	High-speed mode, C <sub>B</sub> – 400 pF max	20	160	ns
t <sub>FDA</sub>	Fall Time of SDA Signal	Standard mode		300	ns
t <sub>FDA</sub>	Fall Time of SDA Signal	Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
t <sub>FDA</sub>	Fall Time of SDA Signal	Fast mode plus		120	ns
t <sub>FDA</sub>	Fall Time of SDA Signal	High-speed mode, C <sub>B</sub> – 100 pF max	10	80	ns
t <sub>FDA</sub>	Fall Time of SDA Signal	High-speed mode, C <sub>B</sub> – 400 pF max	20	160	ns
t <sub>SU, t<sub>STO</sub></sub>	Setup Time of STOP Condition	Standard mode	4		μs
t <sub>SU, t<sub>STO</sub></sub>	Setup Time of STOP Condition	Fast mode	600		ns
t <sub>SU, t<sub>STO</sub></sub>	Setup Time of STOP Condition	Fast mode plus	260		ns
t <sub>SU, t<sub>STO</sub></sub>	Setup Time of STOP Condition	High-Speed mode	160		ns
C <sub>B</sub>	Capacitive Load for SDA and SCL	Standard mode		400	pF
C <sub>B</sub>	Capacitive Load for SDA and SCL	Fast mode		400	pF
C <sub>B</sub>	Capacitive Load for SDA and SCL	Fast mode plus		550	pF
C <sub>B</sub>	Capacitive Load for SDA and SCL	High-Speed mode		400	pF

(1) All values referred to V<sub>IL</sub> MAX and V<sub>IH</sub> MIN levels in [ELECTRICAL CHARACTERISTICS](#) table.

- (2) For bus line loads  $C_B$  between 100 pF and 400 pF, the timing parameters must be linearly interpolated.

## 7.7 Typical Characteristics

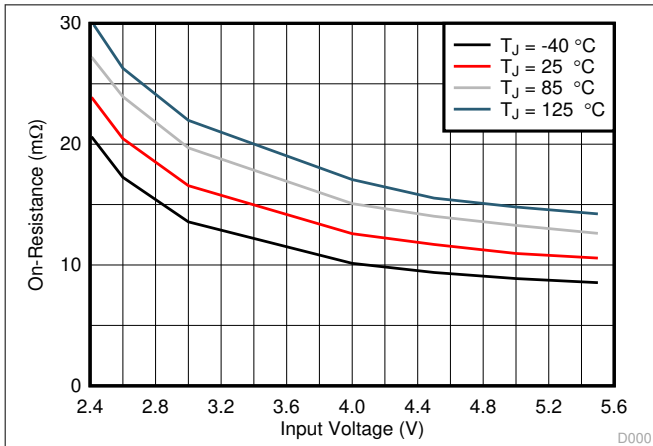


Figure 7-1. High-Side FET On-Resistance

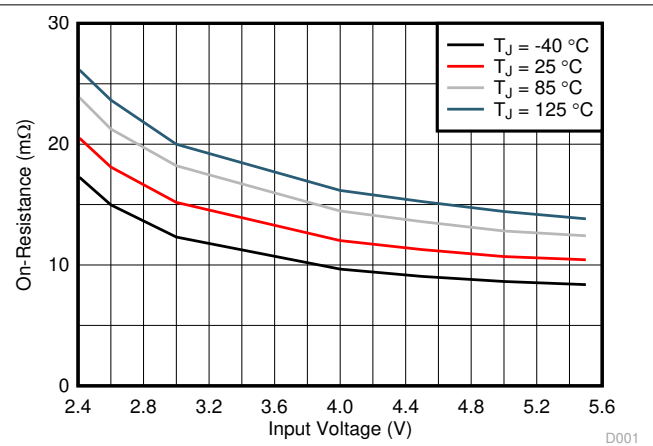


Figure 7-2. Low-Side FET On-Resistance

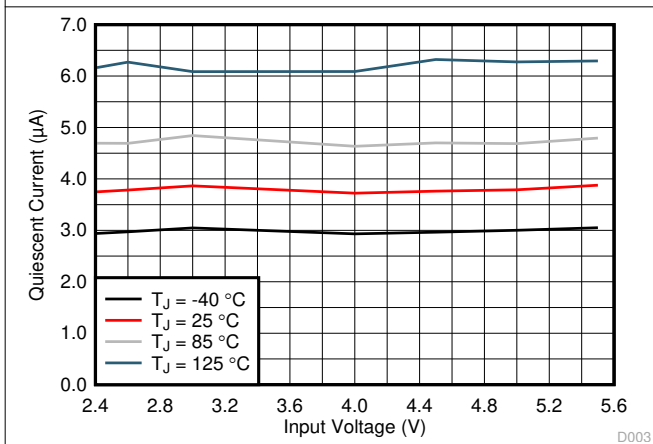


Figure 7-3. Quiescent Current

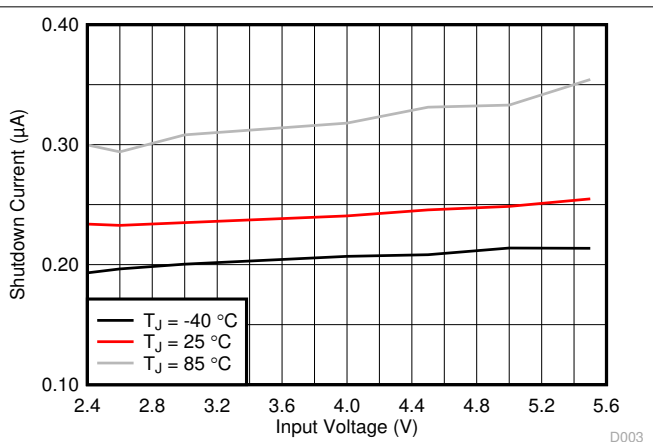


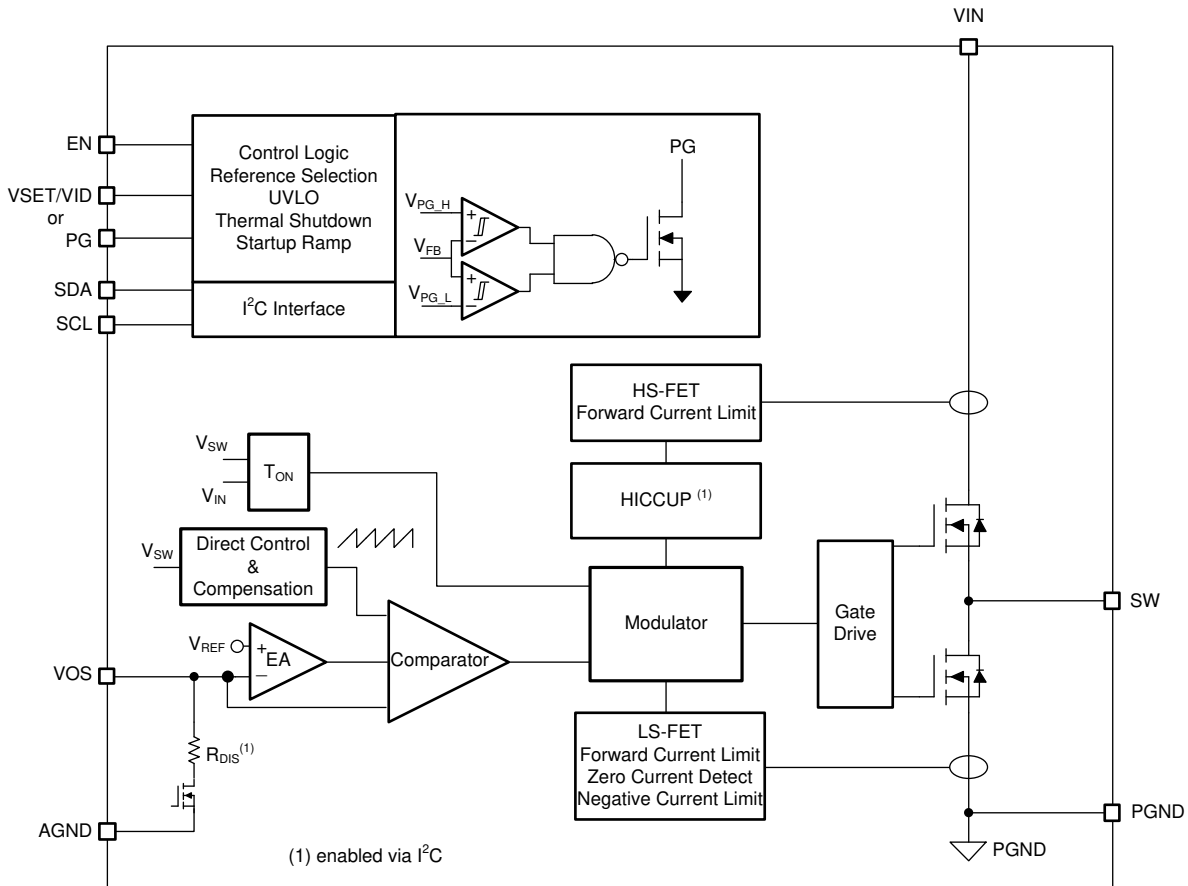
Figure 7-4. Shutdown Current

## 8 Detailed Description

### 8.1 Overview

The DCS-Control™ topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.4 MHz, having a controlled frequency variation over the input voltage range. Because DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage. The devices offer both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Power Save Mode

As the load current decreases, the device enters Power Save Mode (PSM) operation. PSM occurs when the inductor current becomes discontinuous, which is when it reaches 0 A during a switching cycle. Power Save Mode is based on a fixed on-time architecture, as shown in Equation 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 416\text{ns} \tag{1}$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

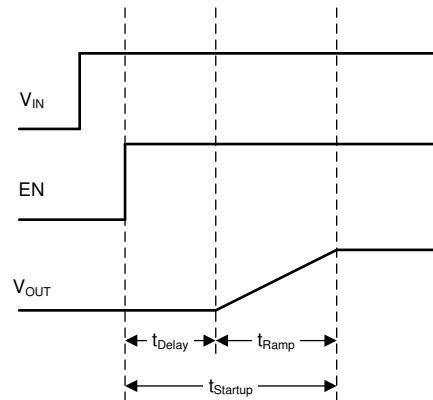
When  $V_{IN}$  decreases to typically 15% above the  $V_{OUT}$ , the TPS6286x does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

### 8.3.2 Forced PWM Mode

With I<sup>2</sup>C, set the device in forced PWM (FPWM) mode by the CONTROL register. The device switches at 2.4 MHz, even with a light load. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications. Efficiency at light load is lower in FPWM mode.

### 8.3.3 Start-up

After enabling the device, there is an enable delay ( $t_{Delay}$ ) before the device starts switching. During this period, the device sets the internal reference voltage, and determines the start-up output voltage through the resistor connected to the VSET/VID pin. After  $t_{Delay}$ , all registers can be read and written by the I<sup>2</sup>C interface.



**Figure 8-1. Start-up Sequence**

After the enable delay, an internal soft start-up circuitry ramps up the output voltage with a period of 1 ms ( $t_{Ramp}$ ). This avoids excessive inrush current and creates a smooth output voltage rising-slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The device is able to start into a pre-biased output capacitor. It starts with the applied bias voltage and ramps the output voltage to its nominal value.

### 8.3.4 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold  $I_{LIM}$ , cycle by cycle, the high-side MOSFET is turned off and the low-side MOSFET is turned on, while the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 32 times, the device stops switching. The device then automatically re-starts, with an internal soft start-up, after a typical delay time of 128  $\mu$ s has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

The HICCUP is disabled by the CONTROL register bit Enable HICCUP. Disabling HICCUP changes the overcurrent protection to latching protection. The device stops switching after the high-side MOSFET current limit is triggered 32 times. Toggling the EN pin, removing and reapplying the input voltage, or writing to the CONTROL register bit Software Enable Device unlatches the device.

### 8.3.5 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, undervoltage lockout (UVLO) is implemented when the input voltage is lower than  $V_{UVLO}$ . The device stops switching and the output voltage discharge is active (if enabled through I<sup>2</sup>C) when the device is in UVLO. When the input voltage recovers, the device automatically returns to operation with an internal soft start-up. During UVLO, the internal register values are kept.

The UVLO bit in the STATUS Register is set when the input voltage is less than the UVLO falling threshold. When the input voltage is below 1.8 V (typ.), all registers are reset.

### 8.3.6 Thermal Warning and Shutdown

When the junction temperature goes up to  $T_{JW}$ , the device gives a pre-warning indicator in the STATUS register. The device keeps running.

When the junction temperature exceeds  $T_{JSD}$ , the device goes into thermal shutdown, stops switching, and activates the output voltage discharge. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically with an internal soft start-up. During thermal shutdown, the internal register values are kept.

## 8.4 Device Functional Modes

### 8.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic High. In shutdown mode (EN = Low), the internal power switches as well as the entire control circuitry are turned off, and all the registers are reset, except for the Enable Output Discharge bit. Do not leave the EN pin floating.

In shutdown mode (EN = Low), all registers cannot be read and written by the I<sup>2</sup>C interface.

The typical threshold value of the EN pin is 0.61 V for rising input signals, and 0.51 V for falling input signals.

The device is also enabled or disabled by setting the bit, Software Enable Device in CONTROL register while EN = High. After being disabled/enabled by this bit, the device stops switching and has a new start-up beginning with  $t_{Ramp}$ . There is no  $T_{Delay}$  time and the registers are not reset.

### 8.4.2 Output Discharge

An internal MOSFET switch smoothly discharges the output through the VOS pin in shutdown mode (EN = Low or Software Enable Device bit = 0). The output discharge is also active when the device is in thermal shutdown and UVLO.

When the Enable Output Discharge bit is set to 0, the output discharge function is disabled. The input voltage must remain higher than 1 V (typ.) to keep the output discharge function operational and the status of the Enable Output Discharge bit retained. The Enable Output Discharge bit is reset on the rising edge of the EN pin.

### 8.4.3 Start-up Output Voltage and I<sup>2</sup>C Slave Address Selection (VSET)

During the enable delay ( $t_{Delay}$ ), the start-up output voltage and device I<sup>2</sup>C slave address are set by an external resistor connected to the VSET/VID pin through an internal R2D (resistor to digital) converter. [Table 8-1](#) shows the options.

**Table 8-1. Start-up Output Voltage and I<sup>2</sup>C Slave Address Options**

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/VID	START-UP OUTPUT VOLTAGE (TYP)	I <sup>2</sup> C SLAVE ADDRESS
249 kΩ	Voltage Factor * 1.15 V	1000 110
205 kΩ	Voltage Factor * 1.10 V	1000 101
162 kΩ	Voltage Factor * 1.05 V	1000 100
133 kΩ	Voltage Factor * 1.00 V	1000 011
105 kΩ	Voltage Factor * 0.95 V	1000 010
86.6 kΩ	Voltage Factor * 0.90 V	1000 001
68.1 kΩ	Voltage Factor * 0.85 V	1001 000
56.2 kΩ	Voltage Factor * 0.80 V	1001 001
44.2 kΩ	Voltage Factor * 0.75 V	1001 010
36.5 kΩ	Voltage Factor * 0.70 V	1001 011
28.7 kΩ	Voltage Factor * 0.65 V	1001 100
23.7 kΩ	Voltage Factor * 0.60 V	1001 101
18.7 kΩ	Voltage Factor * 0.55 V	1001 110

**Table 8-1. Start-up Output Voltage and I<sup>2</sup>C Slave Address Options (continued)**

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/VID	START-UP OUTPUT VOLTAGE (TYP)	I <sup>2</sup> C SLAVE ADDRESS
15.4 kΩ	Voltage Factor * 0.50 V	1001 111
12.1 kΩ	Voltage Factor * 0.45 V	1000 000
10 kΩ	Voltage Factor * 0.40 V	1000 111

**Table 8-2. Device Option Voltage Factors**

DEVICE OPTION	VOLTAGE FACTOR
TPS628680A/C	0.5
TPS628690A/C	0.5
TPS628681A/C	1
TPS628691A/C	1
TPS628682A/C	2
TPS628692A/C	2

The R2D converter has an internal current source which applies current through the external resistor, and an internal ADC which reads back the resulting voltage level. Depending on the level, the correct start-up output voltage and I<sup>2</sup>C slave address are set. Once this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Ensure that there is no additional current path or capacitance greater than 30 pF from this pin to GND during R2D conversion. Otherwise a false value is set.

During the ramp up period ( $t_{Ramp}$ ), the output voltage ramps to the target value set by VSET first, then ramps up or down to the new value when the value of the output register is changed by I<sup>2</sup>C interface commands.

#### 8.4.4 Select Output Voltage Registers (VID)

After the start-up period ( $t_{Startup}$ ), the output voltage can be selected between two output voltage registers by the VID pin. When VID is pulled low, the output voltage is set by Table 8-5. When VID is pulled high, the output voltage is set by Table 8-6. This is also called dynamic voltage scaling (DVS).

During an output voltage change through I<sup>2</sup>C or the VSET/VID pin, the device can be set in FPWM by the Enable FPWM Mode during Output Voltage Change bit in CONTROL register. The output voltage change speed is set by the Voltage Ramp Speed bit.

#### 8.4.5 Power Good ( PG)

The TPS62868 and TPS62869 families provide device options with the PG pin instead of a VSET/VID pin. Refer to Section 5 to see the according device options.

The PG pin goes high impedance once the output voltage is above 91% and less than 110% of the nominal voltage, and is driven low once the voltage is out of the range. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

The PG has a deglitch time, before the signal goes high or low, during normal operation.

**Table 8-3. PG Pin Logic**

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH	LOW
Enable	$0.91 \times V_{OUT\_NOM} \leq V_{VOS} \leq 1.11 \times V_{OUT\_NOM}$	√	
	$V_{VOS} < 0.91 \times V_{OUT\_NOM}$ or $V_{VOS} > 1.11 \times V_{OUT\_NOM}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.8 V < V_{IN} < V_{UVLO}$		√

**Table 8-3. PG Pin Logic (continued)**

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH	LOW
Power Supply Removal	$V_{IN} < 1.8\text{ V}$	undefined	

## 8.5 Programming

### 8.5.1 Serial Interface Description

I<sup>2</sup>C™ is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives or transmits data on the bus under control of the master device, or both.

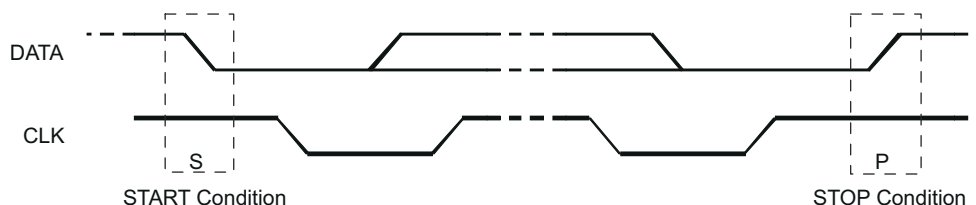
The device works as a *slave* and supports the following data transfer *modes*, as defined in the I<sup>2</sup>C-Bus Specification: standard mode (100 kbps) and fast mode (400 kbps), fast mode plus (1 Mbps), and high-speed mode (3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.8 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as HS-mode.

It is recommended that the I<sup>2</sup>C master initiates a STOP condition on the I<sup>2</sup>C bus after the initial power up of SDA and SCL pullup voltages to ensure reset of the I<sup>2</sup>C engine.

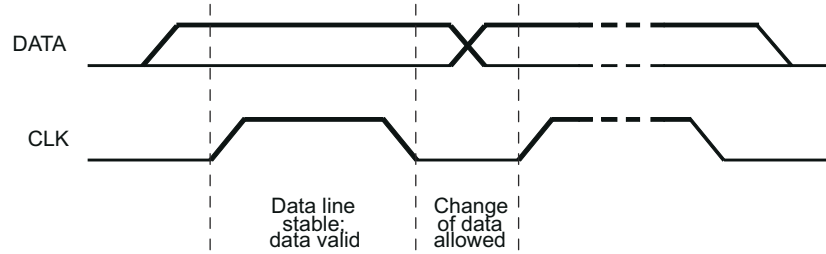
### 8.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 8-2. All I<sup>2</sup>C-compatible devices recognize a start condition.

**Figure 8-2. START and STOP Conditions**

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 8-3). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 8-4) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.



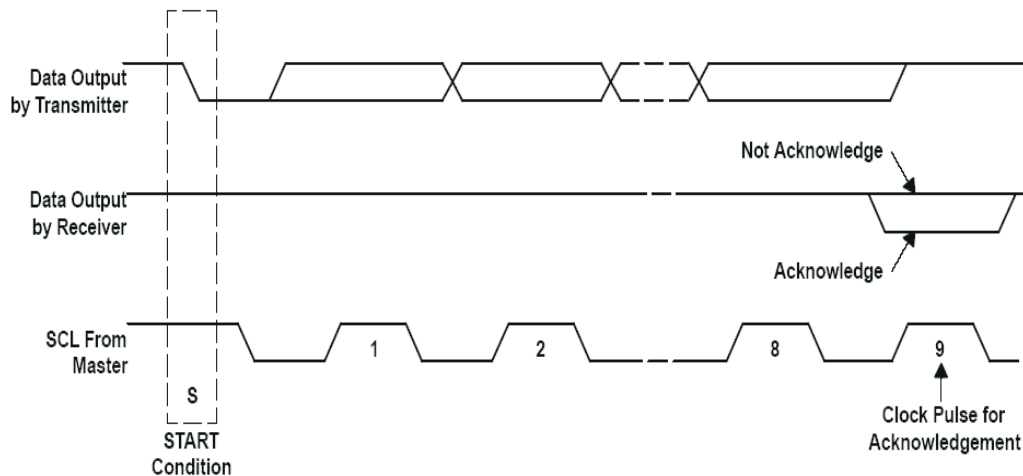


**Figure 8-3. Bit Transfer on the Serial Interface**

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see [Figure 8-2](#)). This releases the bus and stops the communication link with the addressed slave. All I<sup>2</sup>C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.



**Figure 8-4. Acknowledge on the I<sup>2</sup>C Bus**

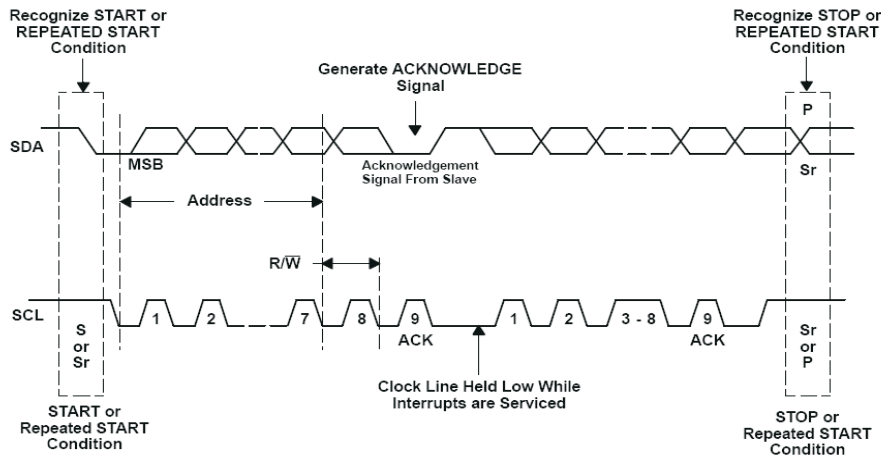


Figure 8-5. Bus Protocol

8.5.3 HS-Mode Protocol

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4 Mbps operation.

The master then generates a *repeated start condition* (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions must be used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

8.5.4 I<sup>2</sup>C Update Sequence

The sequence requires a start condition, a valid I<sup>2</sup>C slave address, a register address byte, and a data byte for a single update. After the receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the device. The device performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

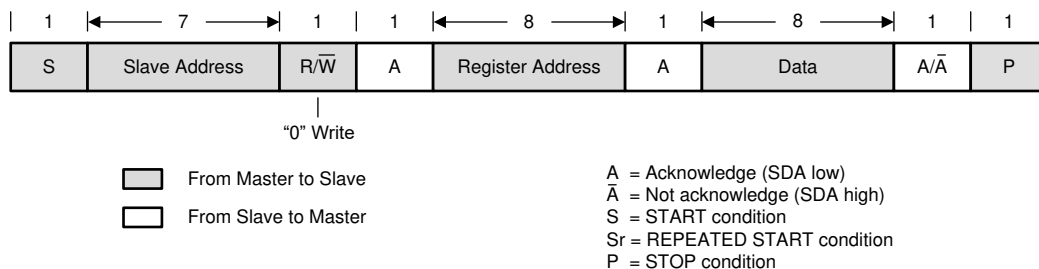


Figure 8-6. “Write” Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

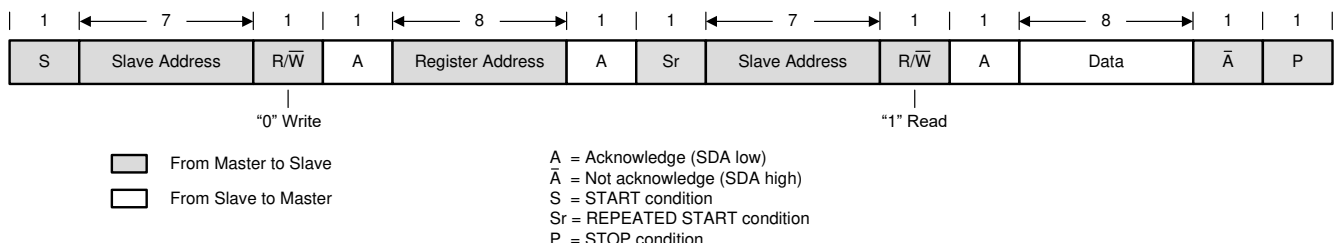


Figure 8-7. “Read” Data Transfer Format in Standard-, Fast, and Fast-Plus Modes

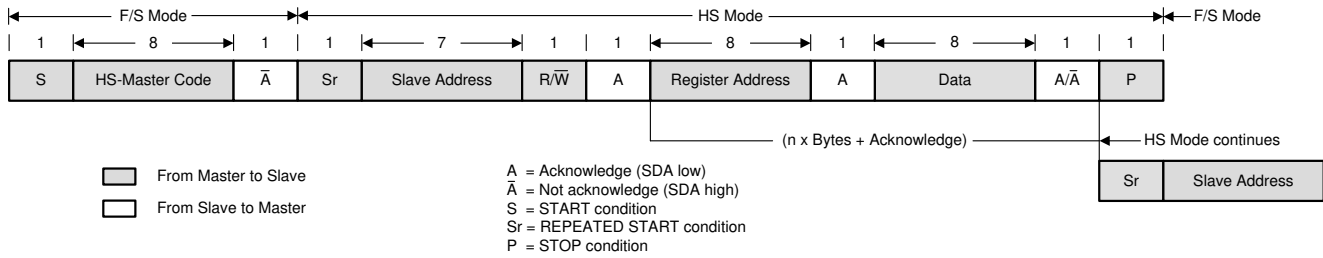


Figure 8-8. Data Transfer Format in HS-Mode

### 8.5.5 I<sup>2</sup>C Register Reset

The I<sup>2</sup>C registers can be reset by:

- Pulling the input voltage below 1.8 V (typ.)
- A high to low transition on EN
- Setting the Reset bit in the CONTROL register. When Reset is set to 1, all registers are reset to the default values and a new start-up is begun immediately. After  $t_{Delay}$ , the I<sup>2</sup>C registers can be programmed again.

## 8.6 Register Map

Table 8-4. Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	FACTORY DEFAULT (HEX)	DESCRIPTION
0x01	V <sub>OUT</sub> Register 1	0x64	Sets the target output voltage
0x02	V <sub>OUT</sub> Register 2	0x64	Sets the target output voltage
0x03	CONTROL Register	0x6F	Sets miscellaneous configuration bits
0x05	STATUS Register	0x00	Returns status flags

### 8.6.1 Slave Address Byte

7	6	5	4	3	2	1	0
1	x	x	x	x	x	x	R/W

The slave address byte is the first byte received following the START condition from the master device. The slave addresses can be assigned by an external resistor, see [Table 8-1](#).

### 8.6.2 Register Address Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	D2	D1	D0

Following the successful acknowledgment of the slave address, the bus master sends a byte to the device, which contains the address of the register to be accessed.

### 8.6.3 V<sub>OUT</sub> Register 1

**Table 8-5. V<sub>OUT</sub> Register 1 Description**

REGISTER ADDRESS 0X01 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYP)
7:0	VO1_SET	0x00	Voltage Factor * 400 mV
		0x01	Voltage Factor * 405 mV
		...	
		0x64	Voltage Factor * 900 mV
		...	
		0xFE	Voltage Factor * 1670 mV
		0xFF	Voltage Factor * 1675 mV

### 8.6.4 V<sub>OUT</sub> Register 2

**Table 8-6. V<sub>OUT</sub> Register 2 Description**

REGISTER ADDRESS 0X02 READ/WRITE			
BIT	FIELD	VALUE (HEX)	OUTPUT VOLTAGE (TYP)
7:0	VO2_SET	0x00	Voltage Factor * 400 mV
		0x01	Voltage Factor * 405 mV
		...	
		0x64	Voltage Factor * <b>900 mV</b> (default value)
		...	
		0xFE	Voltage Factor * 1670 mV
		0xFF	Voltage Factor * 1675 mV

## 8.6.5 CONTROL Register

**Table 8-7. CONTROL Register Description**

REGISTER ADDRESS 0X03 WRITE ONLY				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	Reset	R/W	0	1 - Reset all registers to default.
6	Enable FPWM Mode during Output Voltage Change	R/W	1	0 - Keep the current mode status during output voltage change 1 - Force the device in FPWM during output voltage change.
5	Software Enable Device	R/W	1	0 - Disable the device. All registers values are still kept. 1 - Re-enable the device with a new start-up without the $t_{Delay}$ period.
4	Enable FPWM Mode	R/W	0	0 - Set the device in power save mode at light loads. 1 - Set the device in forced PWM mode at light loads.
3	Enable Output Discharge	R/W	1	0 - Disable output discharge. 1 - Enable output discharge.
2	Enable HICCUP	R/W	1	0 - Disable HICCUP. Enable latching protection. 1 - Enable HICCUP, Disable latching protection.
0:1	Voltage Ramp Speed	R/W	11	00 - 20mV/ $\mu$ s (0.25 $\mu$ s/step) 01 - 10 mV/ $\mu$ s (0.5 $\mu$ s/step) 10 - 5 mV/ $\mu$ s (1 $\mu$ s/step) 11 - 1 mV/ $\mu$ s (5 $\mu$ s/step, default)

## 8.6.6 STATUS Register

**Table 8-8. STATUS Register Description**

REGISTER ADDRESS 0X05 READ ONLY <sup>(1)</sup>				
BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	Reserved			
4	Thermal Warning	R	0	1: Junction temperature is higher than 130°C.
3	HICCUP	R	0	1: Device has HICCUP status once.
2	Reserved			
1	Reserved			
0	UVLO	R	0	1: The input voltage is less than UVLO threshold (falling edge).

(1) All bit values are latched until the device is reset, or the STATUS register is read. Then, the STATUS register is reset to its default values.

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

### 9.2 Typical Application

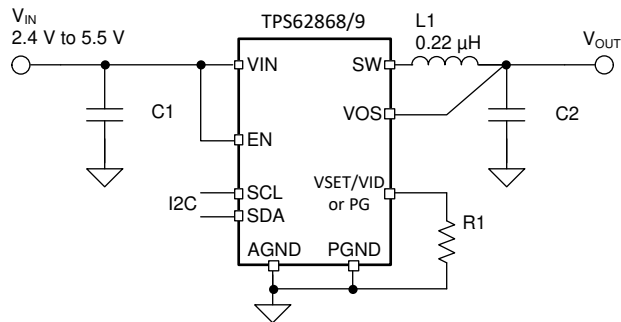


Figure 9-1. Typical Application

#### 9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1 as the input parameters.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4 V to 5.5 V
Output voltage	0.9 V
Maximum output current	6 A

Table 9-2 lists the components used for the example.

Table 9-2. List of Components of Table 9-1

REFERENCE	DESCRIPTION	MANUFACTURER <sup>(1)</sup>
C1	10 $\mu$ F, Ceramic capacitor, 6.3 V, X7R, size 0603, CL10B106MQ8NRNC	Samsung Electro-Mechanics
C2	2 x 22 $\mu$ F, Ceramic capacitor, 6.3 V, X7R, size 0805, GRM21BZ70J226ME44L	Murata
L1	0.22 $\mu$ H, Power inductor, XAL4020-221ME (12 A, 5.81 m $\Omega$ )	Coilcraft
R1	Depending on the start-up output voltage, size 0603	Std

(1) See [Third-party Products](#) disclaimer.

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Setting The Output Voltage

The initial output voltage is set by an external resistor connected to the VSET/VID pin, according to [Table 8-1](#). After the soft start-up, the output voltage can be changed in the V<sub>OUT</sub> Registers. Refer to [Table 8-5](#) and [Table 8-6](#).

### 9.2.2.2 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, [Table 9-3](#) outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

**Table 9-3. Matrix of Output Capacitor and Inductor Combinations**

NOMINAL L [ $\mu$ H] <sup>(2)</sup>	NOMINAL C <sub>OUT</sub> [ $\mu$ F] <sup>(3)</sup>			
	22	2 x 22 or 47	3 x 22	150
0.24		+(1)	+	+

- (1) This LC combination is the standard value and recommended for most applications.
- (2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
- (3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –30%.

### 9.2.2.3 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, [Equation 2](#) is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

where

- I<sub>OUT,MAX</sub> = maximum output current
- $\Delta I_L$  = inductor current ripple
- f<sub>SW</sub> = switching frequency
- L = inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than I<sub>L,MAX</sub>. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. [Table 9-4](#) lists recommended inductors.

**Table 9-4. List of Recommended Inductors**

INDUCTANCE [ $\mu$ H]	CURRENT RATING, I <sub>SAT</sub> [A]	DIMENSIONS [L x W x H mm]	DC RESISTANCE [m $\Omega$ ]	PART NUMBER
0.22	18.7	4 x 4 x 2	5.81	Coilcraft, XAL4020-221ME
0.24	6.6	2 x 1.6 x 1.2	13	Murata, DFE201612E-R24M

### 9.2.2.4 Capacitor Selection

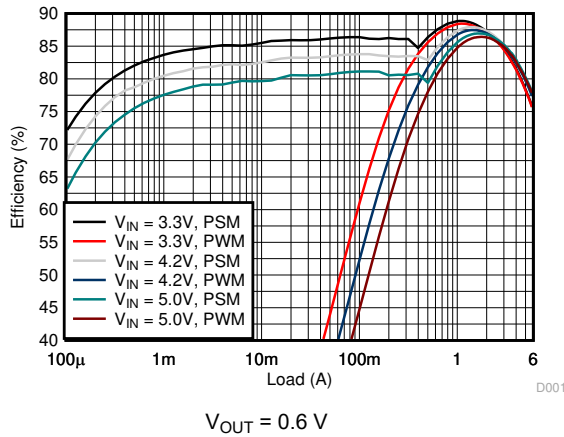
The input capacitor is the low-impedance energy source for the converter which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and PGND as close as possible to those pins. For most applications, 8  $\mu$ F is a sufficient value for the effective input capacitance, though a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended minimum output effective capacitance is 30  $\mu\text{F}$ ; this capacitance can vary over a wide range as outlined in the output filter selection table.

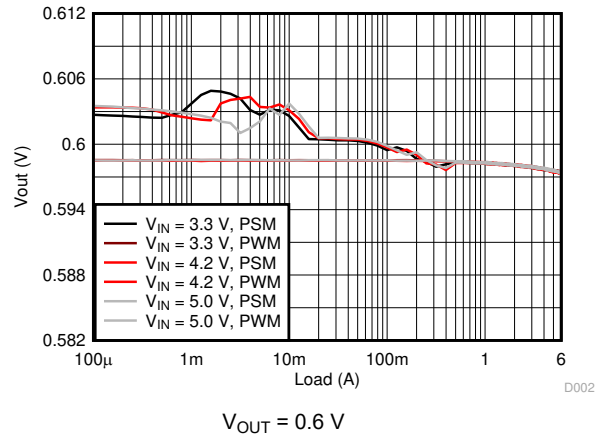


### 9.2.3 Application Curves

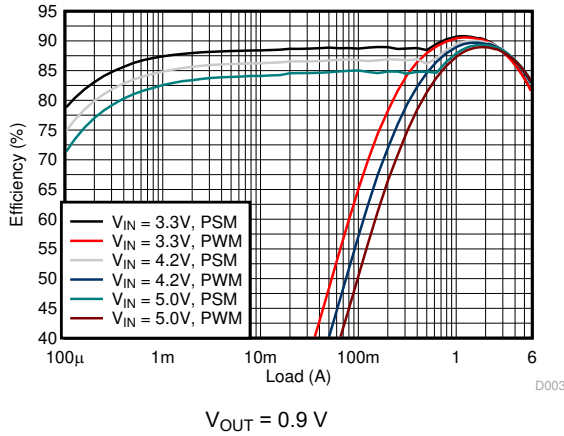
$V_{IN} = 5.0\text{ V}$ ,  $V_{OUT} = 0.9\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , BOM = [Table 9-2](#), unless otherwise noted.



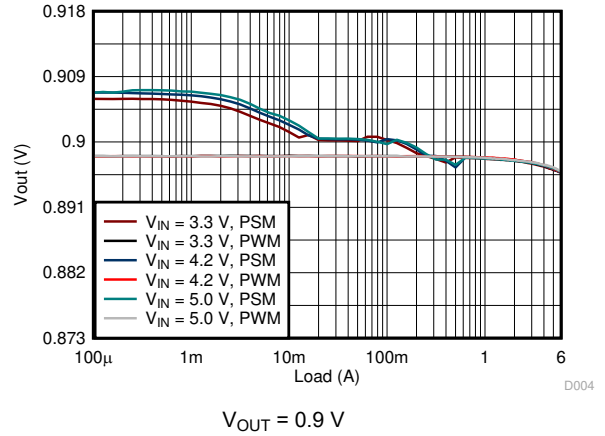
**Figure 9-2. Efficiency**



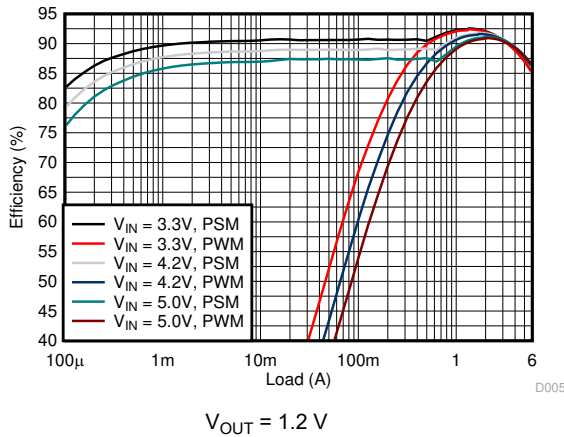
**Figure 9-3. Load Regulation**



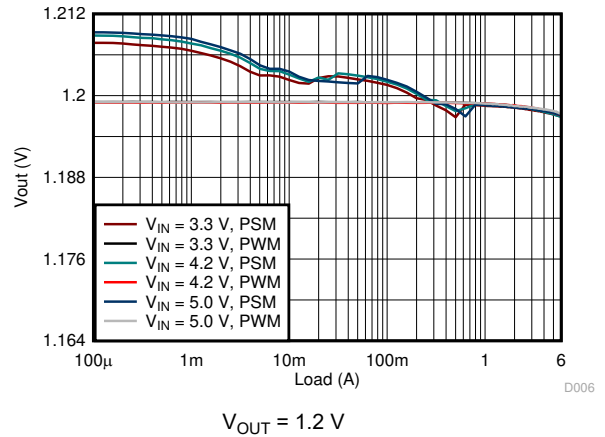
**Figure 9-4. Efficiency**



**Figure 9-5. Load Regulation**



**Figure 9-6. Efficiency**



**Figure 9-7. Load Regulation**

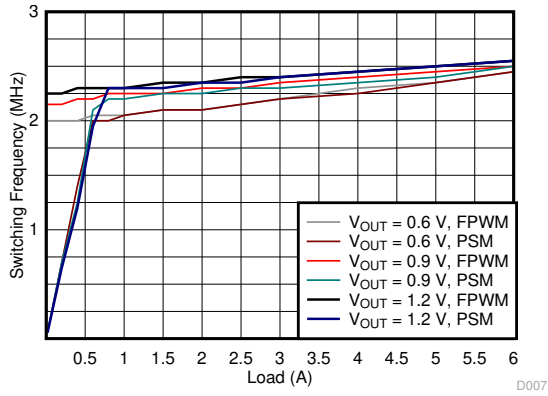


Figure 9-8. Switching Frequency

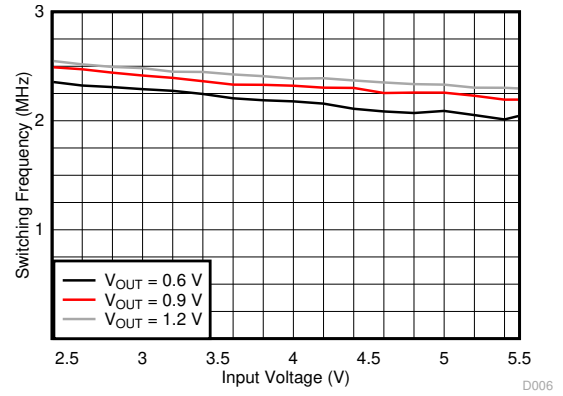


Figure 9-9. Switching Frequency

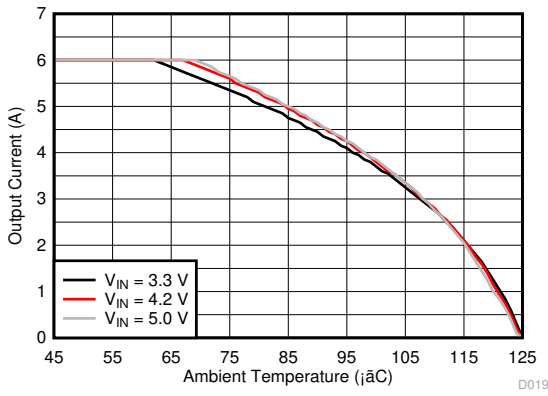


Figure 9-10. Thermal Derating

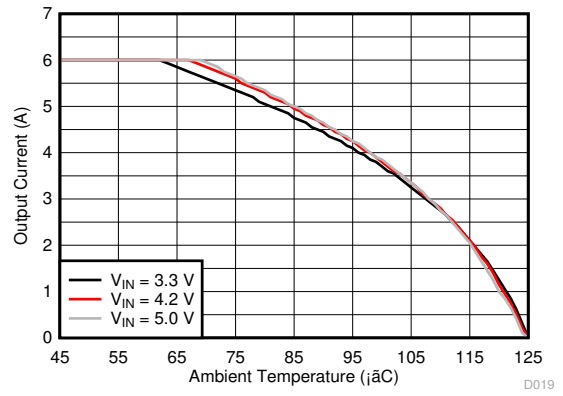


Figure 9-11. Thermal Derating

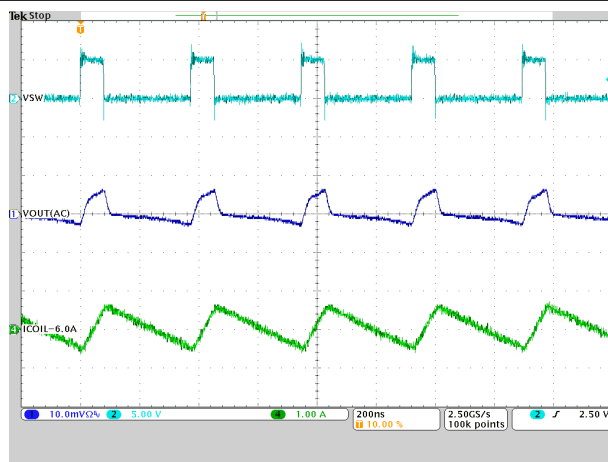


Figure 9-12. PWM Operation

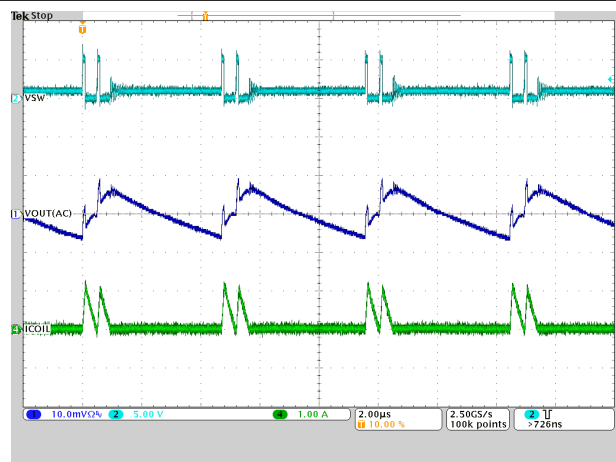
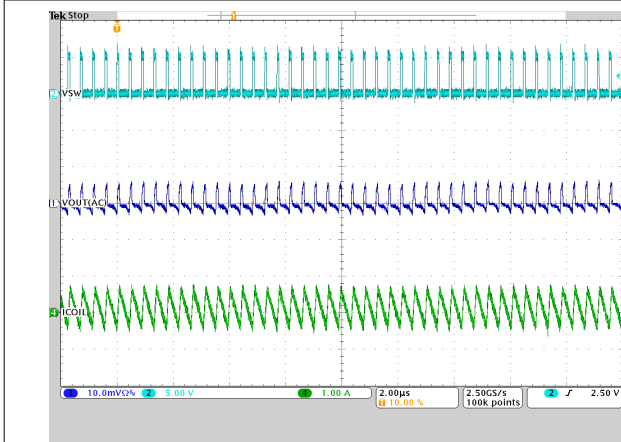
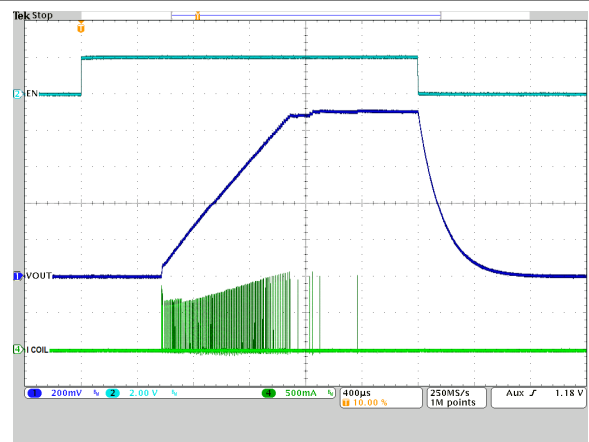


Figure 9-13. PSM Operation



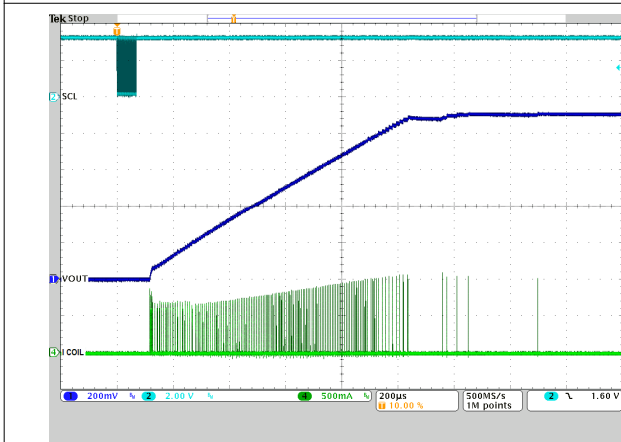
$I_{OUT} = 0.1 \text{ A}$

**Figure 9-14. Forced PWM Operation**



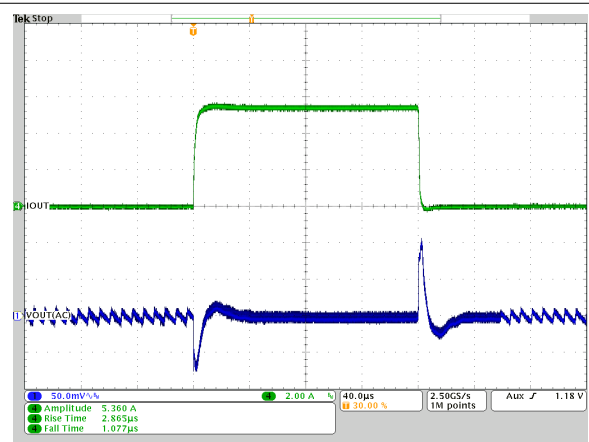
No Load

**Figure 9-15. Startup and Shutdown by EN Pin**



No Load

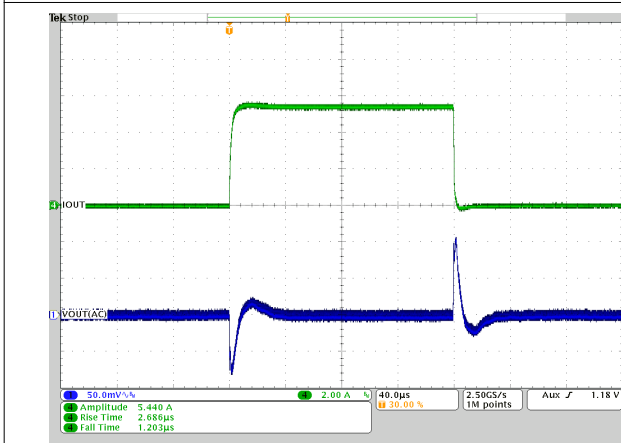
**Figure 9-16. Start-up by Software Enable Device Bit**



$I_{OUT} = 0.06 \text{ A to } 5.4 \text{ A}$

PSM

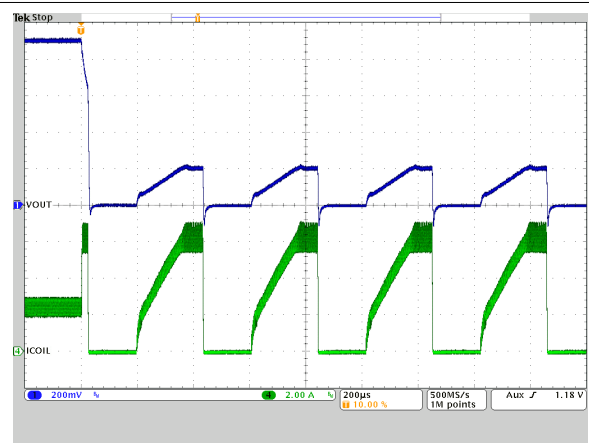
**Figure 9-17. Load Transient**



$I_{OUT} = 0.06 \text{ A to } 5.4 \text{ A}$

Forced PWM

**Figure 9-18. Load Transient**



$I_{OUT} = 2.5 \text{ A}$

**Figure 9-19. HICCU Protection**

## 10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application. The power supply must avoid a fast ramp down. The falling ramp speed must be slower than 10 mV/ $\mu$ s, if the input voltage drops below  $V_{UVLO}$ .

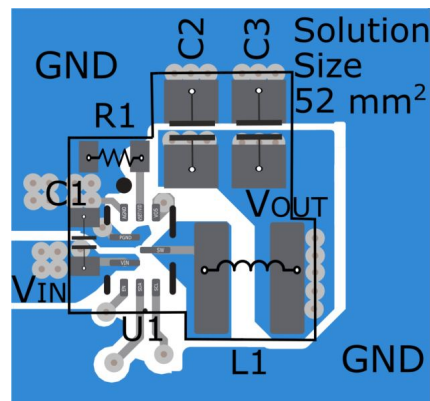
## 11 Layout

### 11.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device.

- The input/output capacitors and the inductor must be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the PGND to avoid a GND potential shift.
- The sense traces connected to the VOS pin is a signal trace. Special care must be taken to avoid noise being induced. Keep the trace away from SW.
- Refer to [Figure 11-1](#) for an example of component placement, routing, and thermal design.

### 11.2 Layout Example



**Figure 11-1. Layout Example**

#### 11.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are improving the power dissipation capability of the PCB design and introducing airflow in the system. For more details on how to use the thermal parameters, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, [Semiconductor and IC Package Thermal Metrics Application Report](#)

### 12.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

### 12.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS628681ARQYR	ACTIVE	VQFN-HR	RQY	9	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2ECH	<a href="#">Samples</a>
TPS628682ARQYR	ACTIVE	VQFN-HR	RQY	9	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2IAH	<a href="#">Samples</a>
TPS628690ARQYR	ACTIVE	VQFN-HR	RQY	9	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2I7H	<a href="#">Samples</a>
TPS628691ARQYR	ACTIVE	VQFN-HR	RQY	9	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2EBH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628681ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS628682ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS628690ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1
TPS628691ARQYR	VQFN-HR	RQY	9	3000	180.0	8.4	1.8	2.8	1.12	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

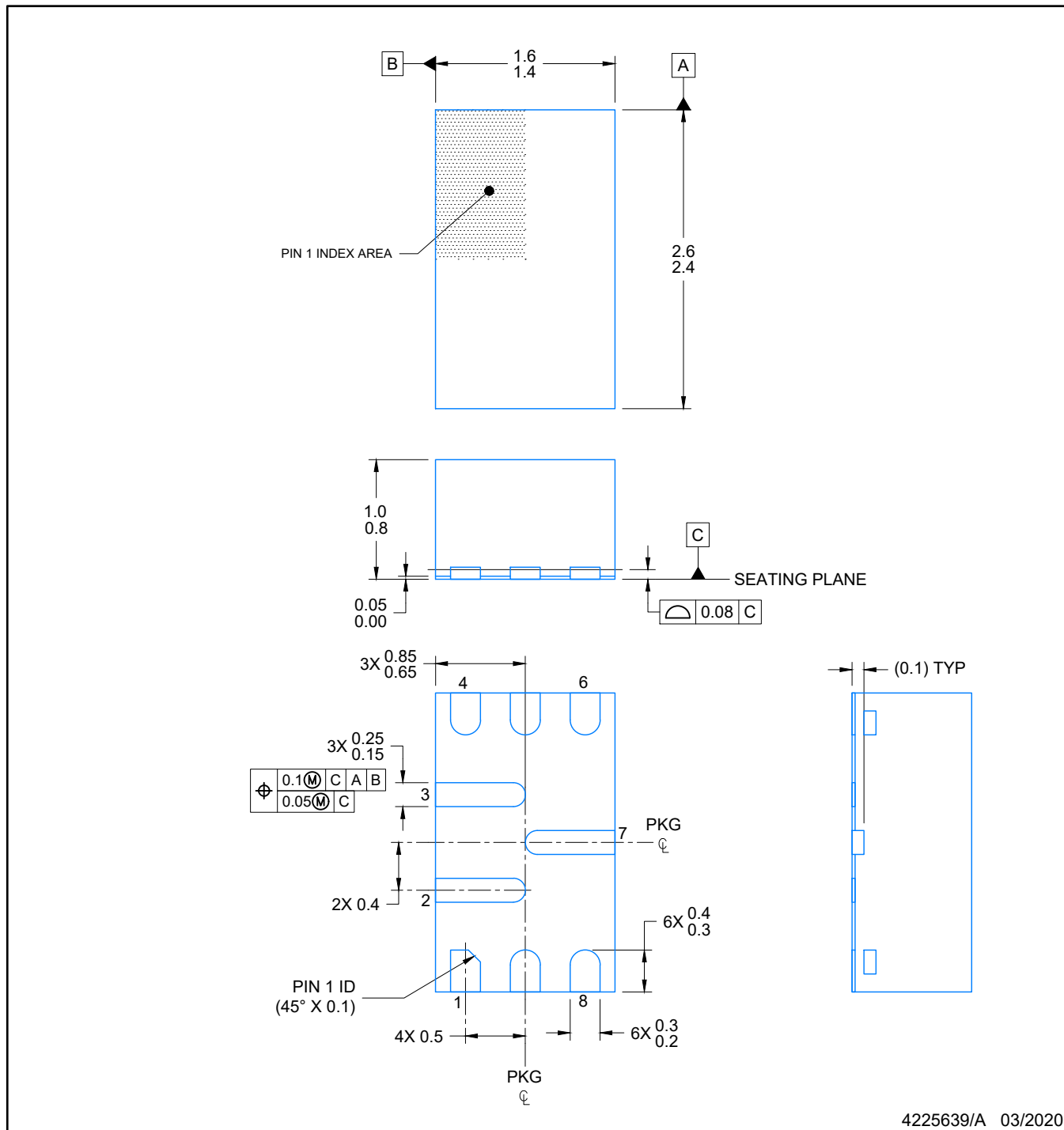
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628681ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628682ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628690ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0
TPS628691ARQYR	VQFN-HR	RQY	9	3000	210.0	185.0	35.0

# PACKAGE OUTLINE

## RQY0009A

## VQFN-HR - 1 mm max height

### PLASTIC QUAD FLATPACK- NO LEAD



#### NOTES:

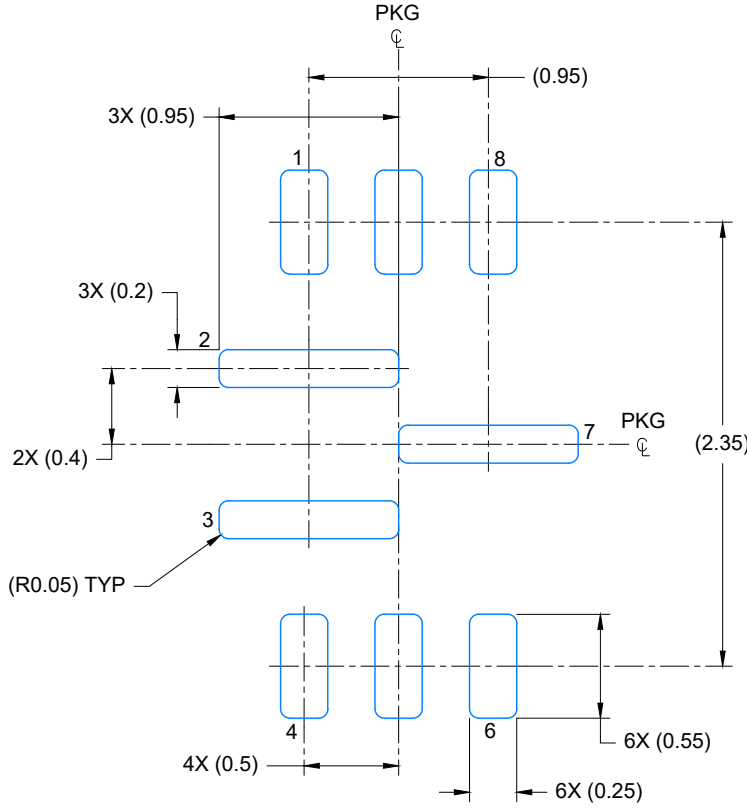
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

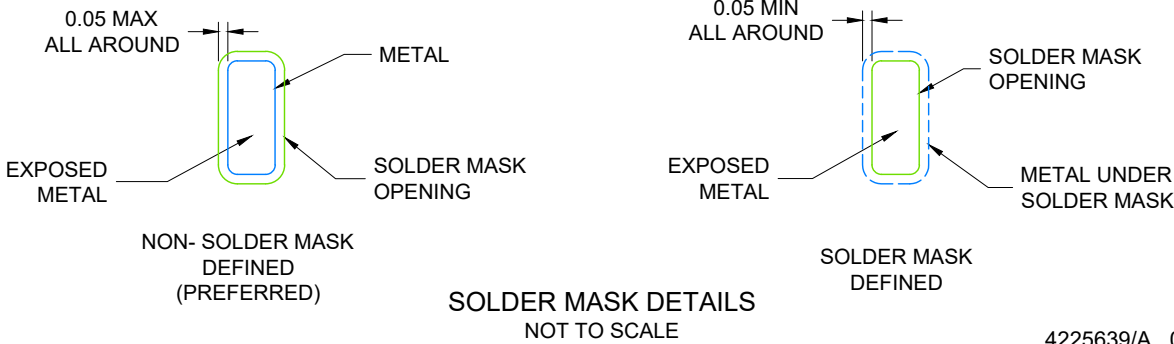
RQY0009A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



SOLDER MASK DETAILS  
NOT TO SCALE

4225639/A 03/2020

NOTES: (continued)

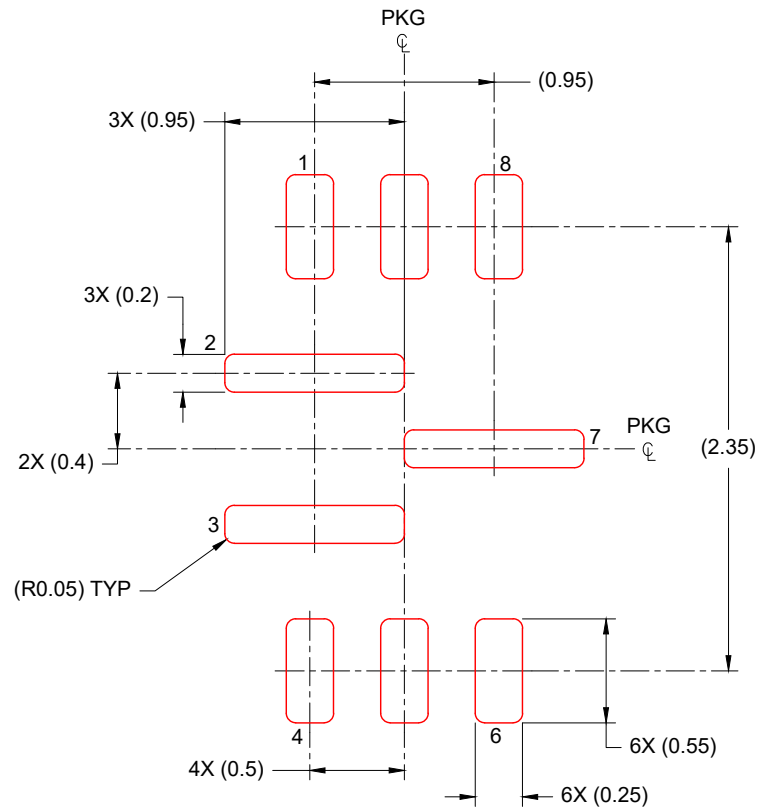
- 3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- 4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

RQY0009A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1mm THICK STENCIL  
SCALE: 25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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