

36V, 2μA I_Q, Peak 200mA Low Dropout Voltage Linear Regulator

1 General Description

The RT9069 is a low-dropout (LDO) voltage regulators with enable function offering the benefits of high input voltage, low-dropout voltage, low-power consumption, and miniaturized packaging.

The features of low quiescent current as low as 2μA and zero disable current is ideal for powering the battery equipment to a longer service life. The RT9069 is stable with the ceramic output capacitor over its wide input range from 3.5V to 36V and the entire range of output load current. The recommended junction temperature range is -40°C to 125°C, and the ambient temperature range is -40°C to 85°C.

2 Applications

- Portable, Battery Powered Equipments
- Extra Low Voltage Microcontrollers
- Notebook Computers

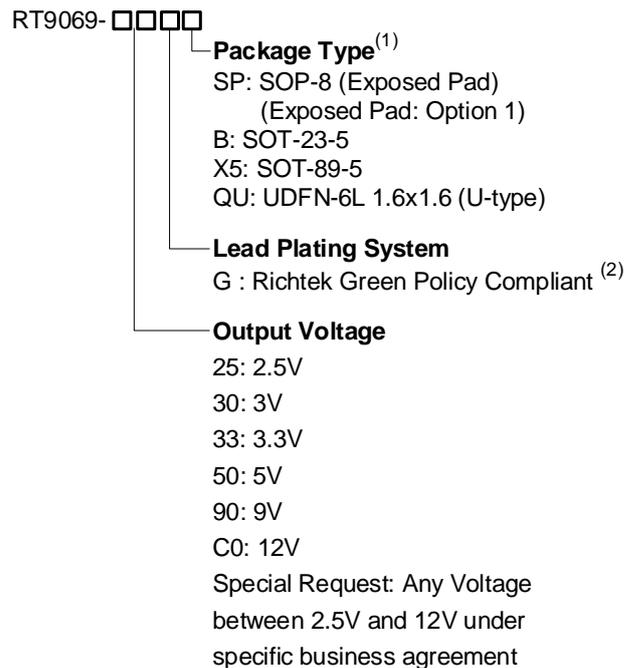
3 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

4 Features

- **2μA Ground Current at no Load**
- **±2% Output Accuracy**
- **100mA Continuous Output Current**
- **Zero Disable Current**
- **Maximum Operating Input Voltage 36V**
- **Dropout Voltage: 0.2V at 10mA/ VIN 5V**
- **Support Fixed Output Voltage 2.5V, 3V, 3.3V, 5V, 9V, 12V**
- **Stable with Ceramic or Tantalum Capacitor**
- **Current Limit Protection**
- **Over-Temperature Protection**

5 Ordering Information



Note 1.

- Marked with ⁽¹⁾ indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with ⁽²⁾ indicated: Richtek products are Richtek Green Policy compliant.

6 Simplified Application Circuit

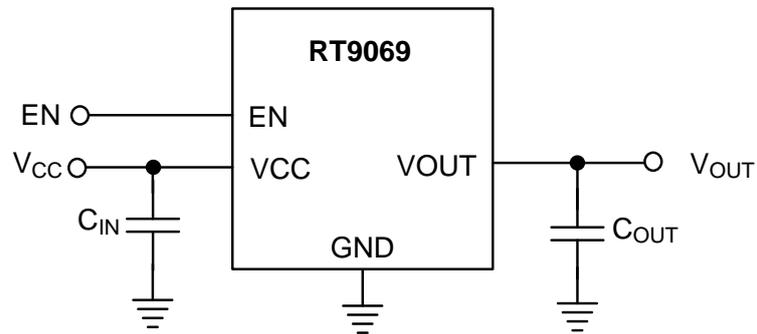
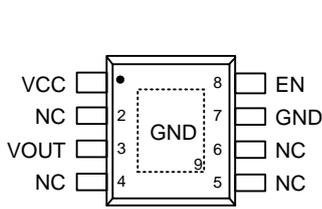


Table of Contents

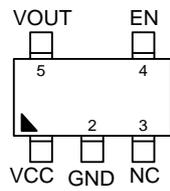
1	General Description	1			
2	Applications	1			
3	Marking Information	1			
4	Features	1			
5	Ordering Information	1			
6	Simplified Application Circuit	2			
7	Pin Configuration	4			
8	Functional Pin Description	4			
9	Functional Block Diagram	5			
10	Absolute Maximum Ratings	6			
11	Recommended Operating Conditions	7			
12	Electrical Characteristics	7			
13	Typical Application Circuit	8			
14	Typical Operating Characteristics	9			
15	Operation	13			
	15.1 Basic Operation-----	13			
	15.2 Output Transistor-----	13			
	15.3 Error Amplifier-----	13			
	15.4 Enable-----	13			
	15.5 Current Limit Protection-----	13			
	15.6 Over-Temperature Protection-----	13			
16	Application Information	14			
	16.1 Thermal Considerations-----	14			
17	Outline Dimension	15			
	17.1 SOP-8 (Exposed Pad)-----	15			
	17.2 SOT-23-5-----	16			
	17.3 SOT-89-5-----	17			
	17.4 UDFN-6L 1.6x1.6 (U-type)-----	18			
18	Footprint Information	19			
	18.1 SOP-8 (Exposed Pad)-----	19			
	18.2 SOT-23-5-----	20			
	18.3 SOT-89-5-----	21			
	18.4 UDFN-6L 1.6x1.6 (U-type)-----	22			
19	Packing Information	23			
	19.1 Tape and Reel Data-----	23			
	19.2 Tape and Reel Packing-----	27			
	19.3 Packing Material Anti-ESD Property-----	31			
20	Datasheet Revision History	32			

7 Pin Configuration

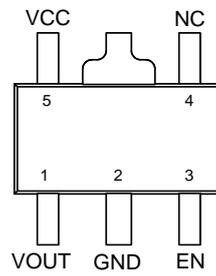
(TOP VIEW)



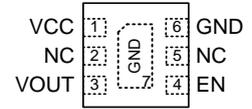
SOP-8 (Exposed Pad)



SOT-23-5



SOT-89-5

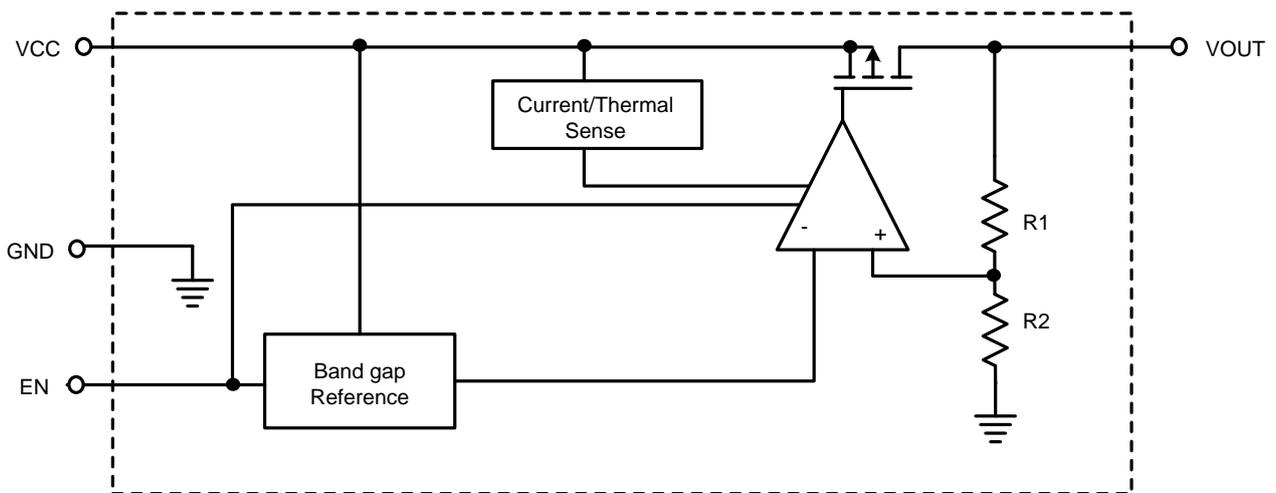


UDFN-6L 1.6x1.6

8 Functional Pin Description

Pin No.				Pin Name	Pin Function
SOP-8 (Exposed Pad)	SOT-23-5	SOT-89-5	UDFN-6L 1.6x1.6		
1	1	5	1	VCC	Supply voltage input.
2, 4, 5, 6	3	4	2, 5	NC	No internal connection.
3	5	1	3	VOUT	Output of the regulator.
7, 9 (Exposed Pad)	2	2	6, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
8	4	3	4	EN	Enable control input.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VCC, EN to GND ----- -0.3V to 40V
- VOUT to VCC ----- -40V to 0.3V
- VOUT to GND
 - RT9069-90/RT9069-C0 ----- -0.3V to 15V
 - RT9069-25/RT9069-30/RT9069-33/RT9069-50 ----- -0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
 - SOP-8 (Exposed Pad)----- 3.26W
 - SOT-23-5 ----- 0.45W
 - SOT-89-5 ----- 0.87W
 - UDFN-6L 1.6x1.6 ----- 2.15W
- Package Thermal Resistance (Note 3)
 - SOP-8 (Exposed Pad), θ_{JA} ----- 30.6°C/W
 - SOP-8 (Exposed Pad), θ_{JC} ----- 3.4°C/W
 - SOT-23-5, θ_{JA} ----- 218.1°C/W
 - SOT-23-5, θ_{JC} ----- 28.5°C/W
 - SOT-89-5, θ_{JA} ----- 113.9°C/W
 - SOT-89-5, θ_{JC} ----- 6.9°C/W
 - UDFN-6L 1.6x1.6, θ_{JA} ----- 46.5°C/W
 - UDFN-6L 1.6x1.6, θ_{JC} ----- 18.6°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 4)
 - HBM (Human Body Model) ----- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage----- 3.5V to 36V
- Junction Temperature Range----- -40°C to 125°C
- Ambient Temperature Range----- -40°C to 85°C

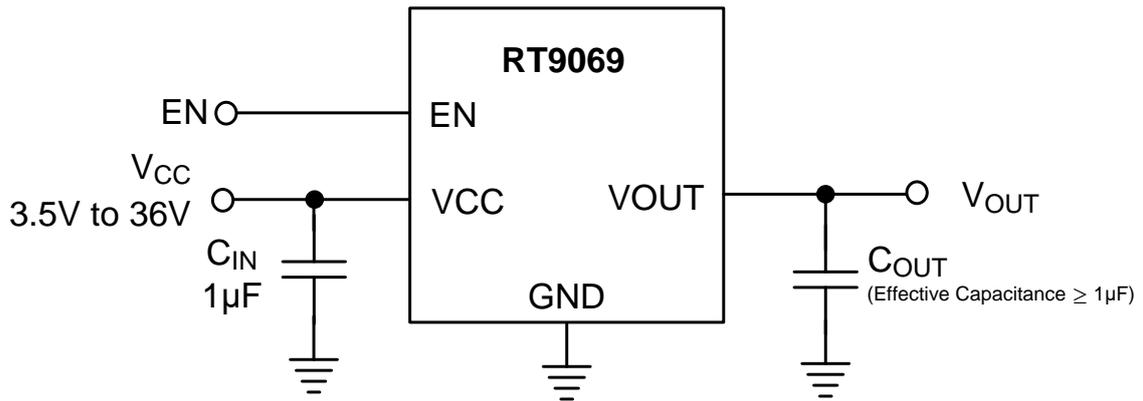
Note 5. The device is not guaranteed to function outside its operations conditions.

12 Electrical Characteristics

(C_{IN} = 1μF, T_A = 25°C, for each LDO unless otherwise specified.)

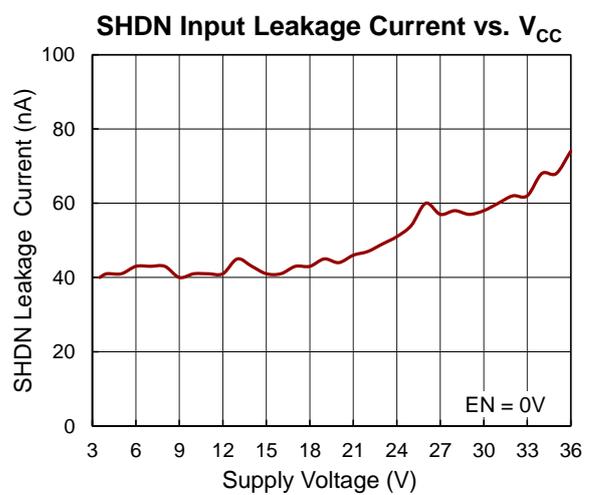
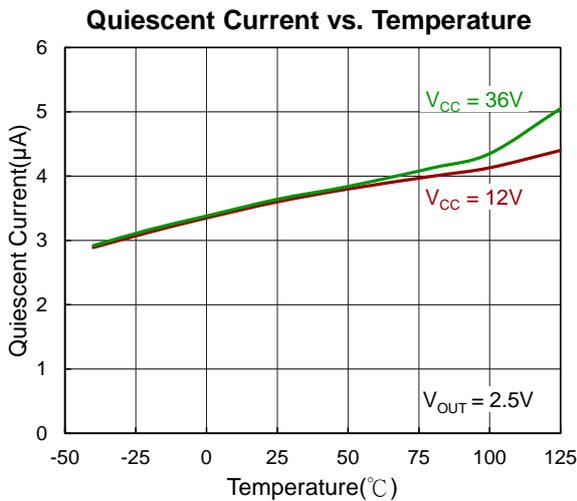
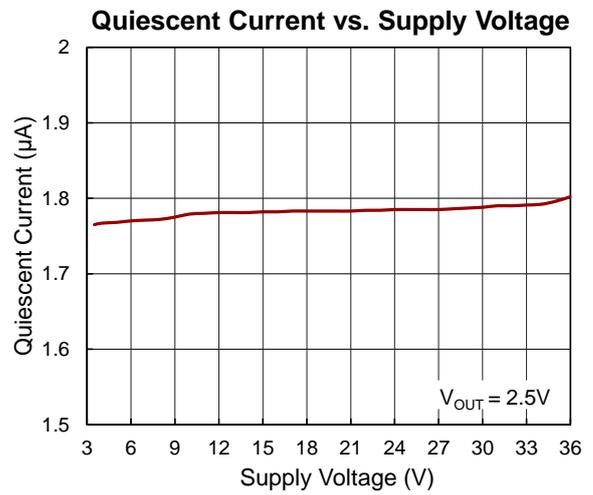
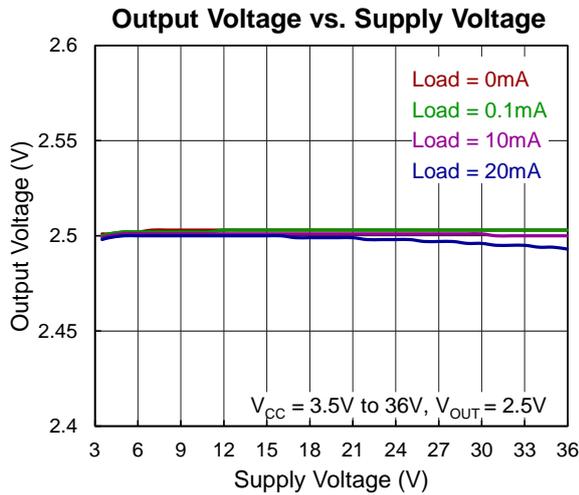
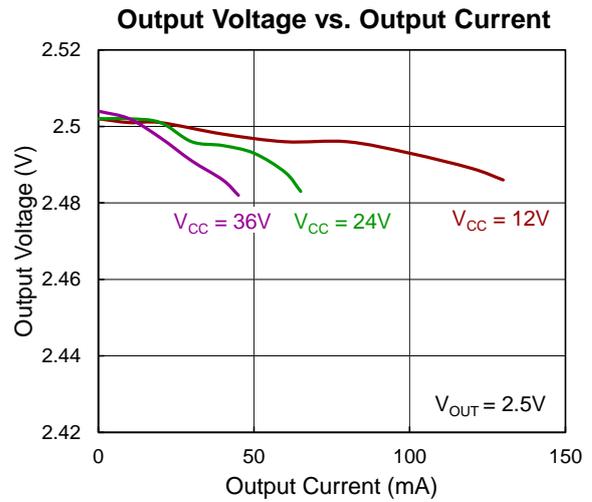
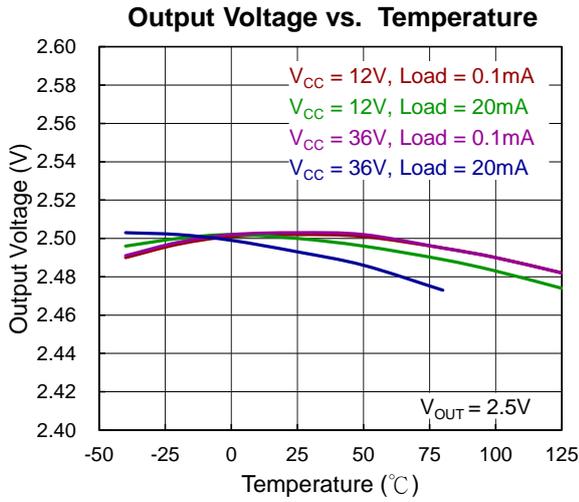
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V _{CC}		3.5	--	36	V
Output Voltage Range	V _{OUT}		2.5	--	12	V
DC Output Accuracy	ΔV _{OUT}	I _{LOAD} = 10mA	-2	--	+2	%
Dropout Voltage	V _{DROP}	I _{LOAD} = 10mA, V _{CC} > 5V	--	0.2	0.36	V
V _{CC} Consumption Current	I _Q	I _{LOAD} = 0mA, V _{OUT} ≤ 5.5V	--	2	3.5	μA
		I _{LOAD} = 0mA, V _{OUT} > 5.5V, V _{CC} = 15V	--	3.5	5	μA
Shutdown Current		V _{EN} = 0V	--	0.1	--	μA
Shutdown Leakage Current		V _{EN} = 0V, V _{OUT} = 0V	--	0.1	--	μA
EN Input Current	I _{EN}	V _{EN} = 36V	--	0.1	--	μA
Line Regulation	ΔV _{LINE}	I _{LOAD} = 1mA, V _{OUT} +1 < V _{CC} < 36V, V _{OUT} > 3.3V	--	0.04	0.5	%
		I _{LOAD} = 1mA, V _{OUT} +1 < V _{CC} < 36V, V _{OUT} ≤ 3.3V	--	0.04	0.6	
Load Regulation	ΔV _{LOAD}	0mA < I _{LOAD} < 100mA	-1	--	1	%
Output Current Limit	I _{LIM}	V _{OUT} = 0.5 x V _{OUT(normal)}	200	350	--	mA
Enable Input Voltage Rising Threshold	V _{EN_R}		1.6	--	--	V
Enable Input Voltage Falling Threshold	V _{EN_F}		--	--	0.6	
Over-Temperature Protection Threshold	T _{OTP}	I _{LOAD} = 30mA	--	150	--	°C
Over-Temperature Protection Hysteresis	T _{OTP_HYS}		--	20	--	°C

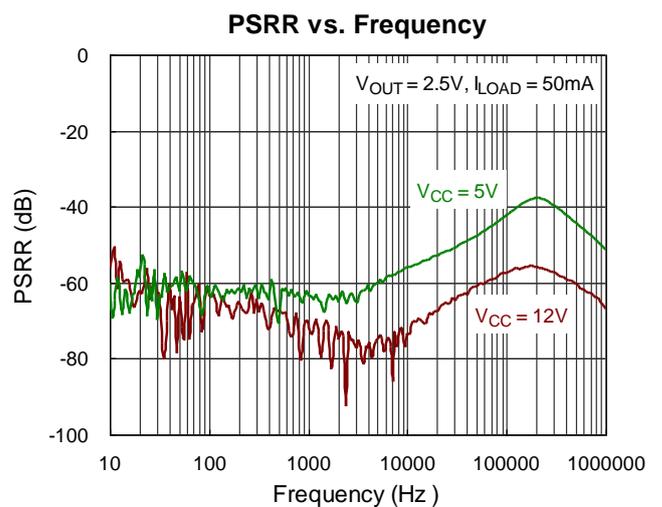
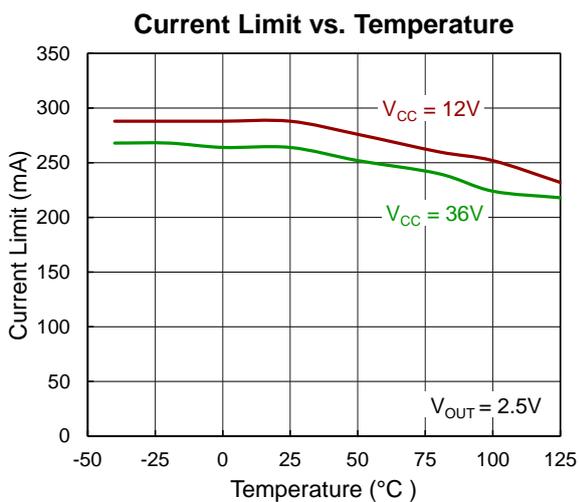
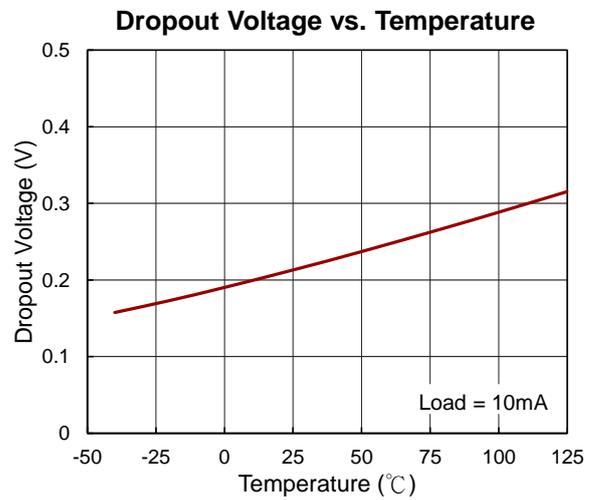
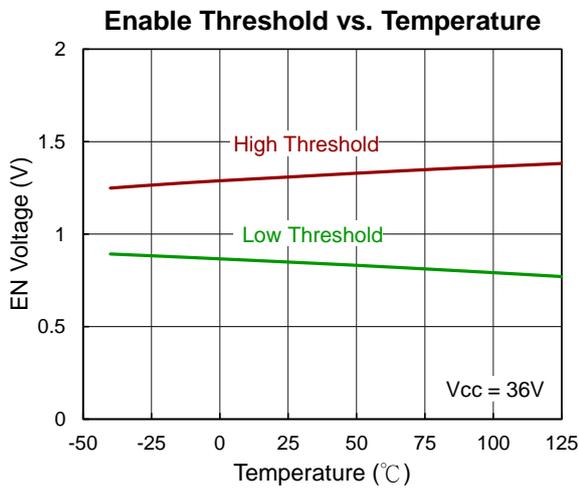
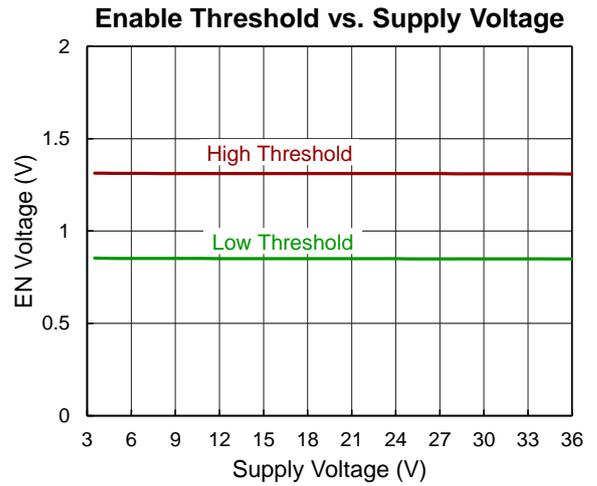
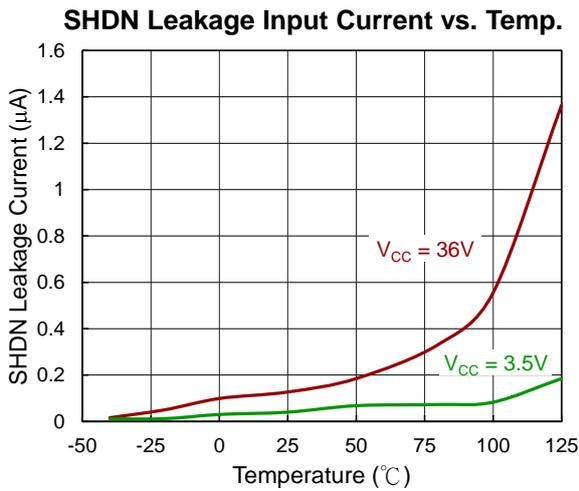
13 Typical Application Circuit

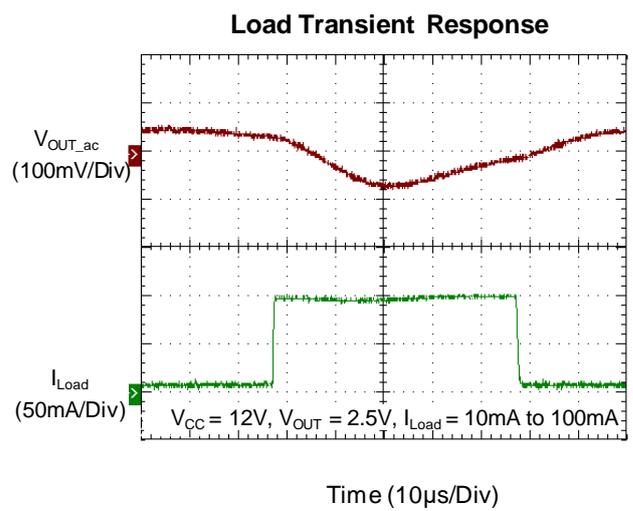
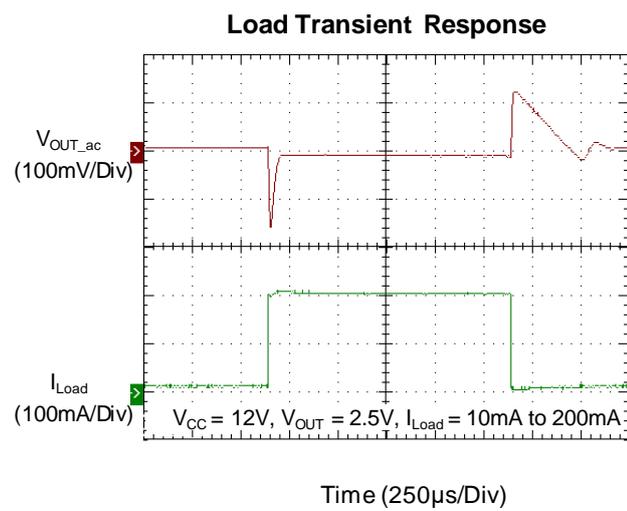
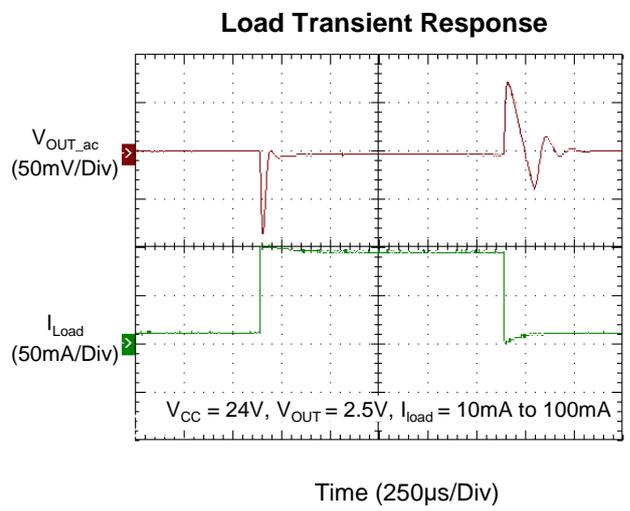
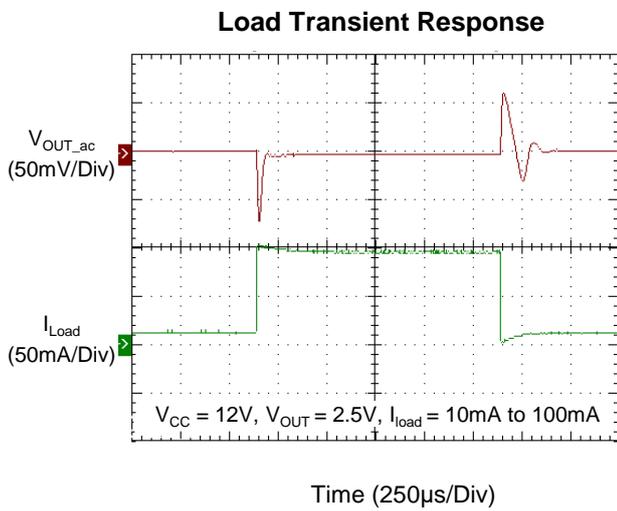
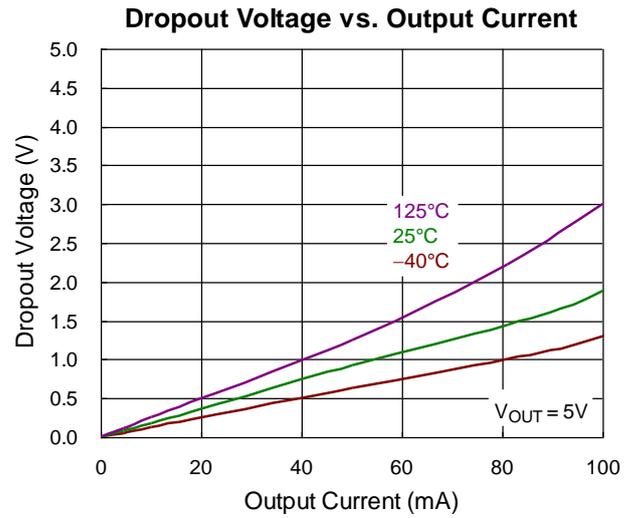
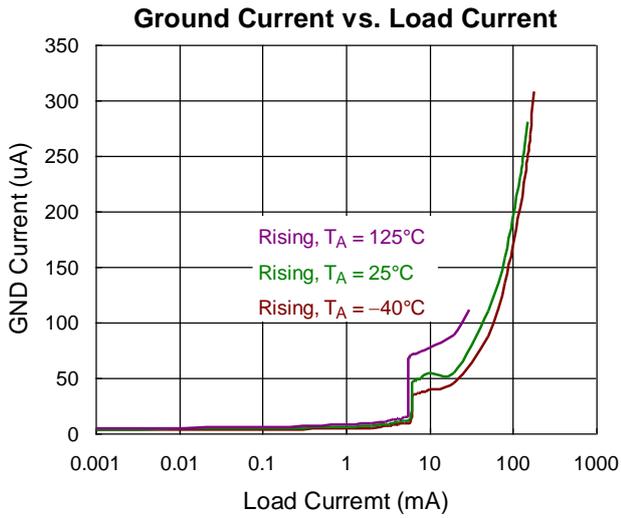


Note 6. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

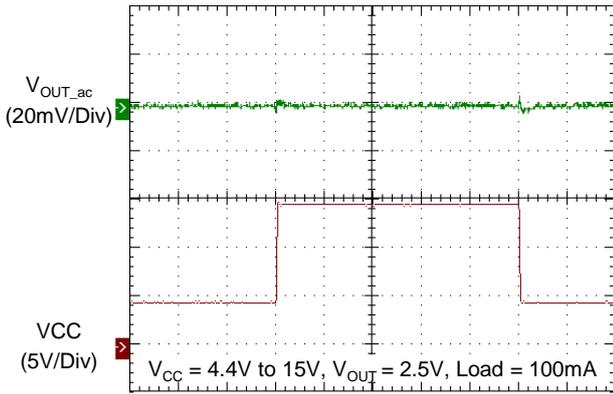
14 Typical Operating Characteristics





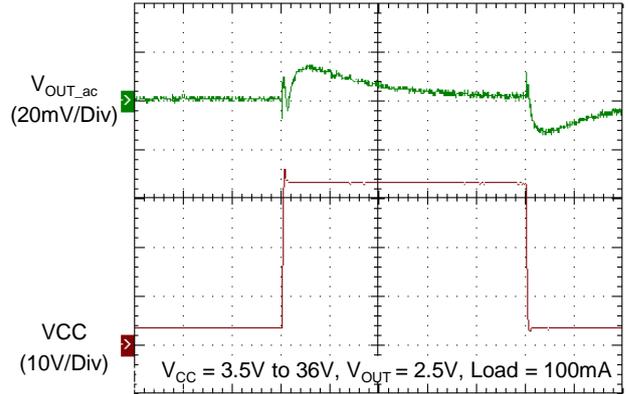


Line Transient Response



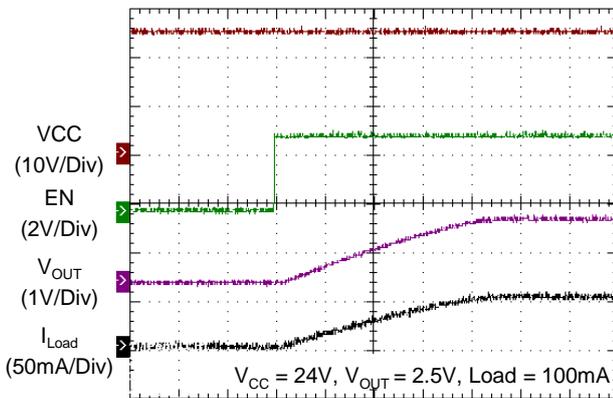
Time (100µs/Div)

Line Transient Response



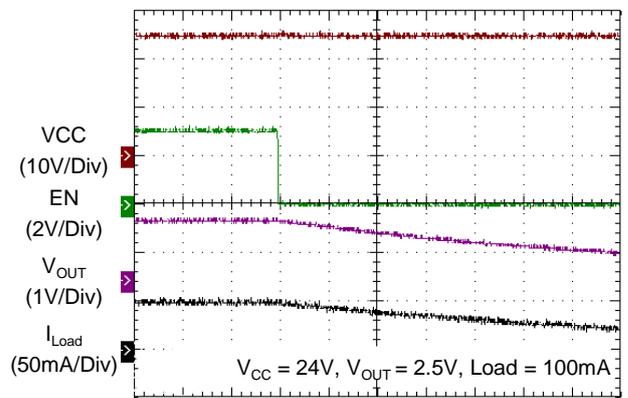
Time (100µs/Div)

Power On from EN



Time (25µs/Div)

Power Off from EN



Time (25µs/Div)

15 Operation

15.1 Basic Operation

The RT9069 is a high input voltage linear regulator designed especially for low external component systems. The input voltage range is from 3.5V to 36V.

The minimum required output capacitance for stable operation is 1 μ F effective capacitance after consideration of the temperature and voltage coefficient of the capacitor.

15.2 Output Transistor

The RT9069 builds in a P-MOSFET output transistor which provides a low switch-on resistance for low dropout voltage applications.

15.3 Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

15.4 Enable

The RT9069 delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is zero.

15.5 Current Limit Protection

The RT9069 provides current limit function to prevent the device from damage during over-load or shorted-circuit conditions. This current is detected by an internal sensing transistor.

15.6 Over-Temperature Protection

The over-temperature protection function turns off the P-MOSFET when the junction temperature exceeds 150°C (typ.) and the output current exceeds 4mA. Once the junction temperature cools down by approximately 20°C, the regulator automatically resumes operation.

16 Application Information

(Note 7)

16.1 Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance, θ_{JA} , is 30.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOT-23-5 package, the thermal resistance, θ_{JA} , is 218.1°C/W on a standard JEDEC 51-7 four-layer thermal test board. For SOT-89-5 package, the thermal resistance, θ_{JA} , is 113.9°C/W on a standard JEDEC 51-7 four-layer thermal test board. For UDFN-6L 1.6x1.6 package, the thermal resistance, θ_{JA} , is 46.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by the following formula:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (30.6^\circ\text{C/W}) = 3.2679\text{W for SOP-8 (Exposed Pad) package}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (218.1^\circ\text{C/W}) = 0.4585\text{W for SOT-23-5 package}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (113.9^\circ\text{C/W}) = 0.8779\text{W for SOT-89-5 package}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (46.5^\circ\text{C/W}) = 2.15\text{W for UDFN-6L 1.6x1.6 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . The derating curve in [Figure 1](#) allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

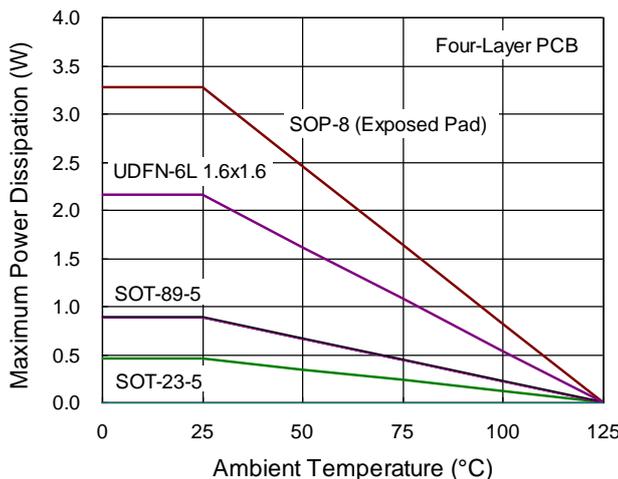
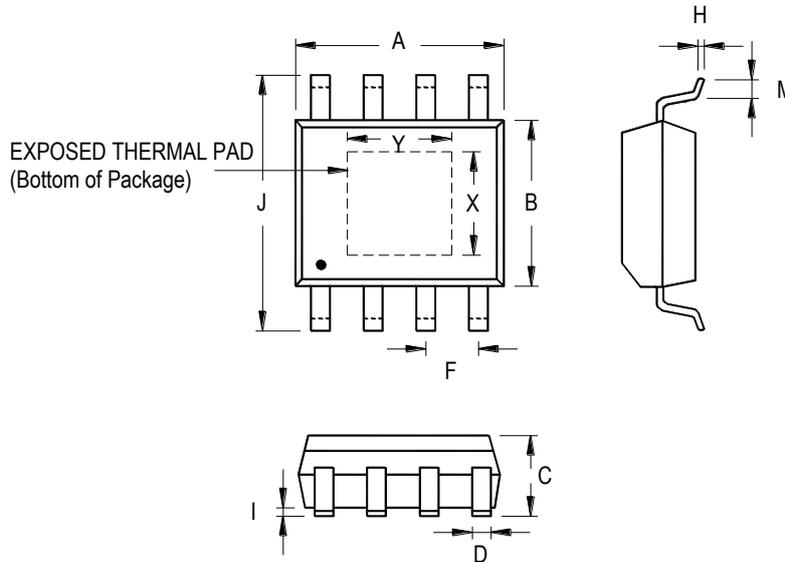


Figure 1. Derating Curve of Maximum Power Dissipation

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek’s product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension

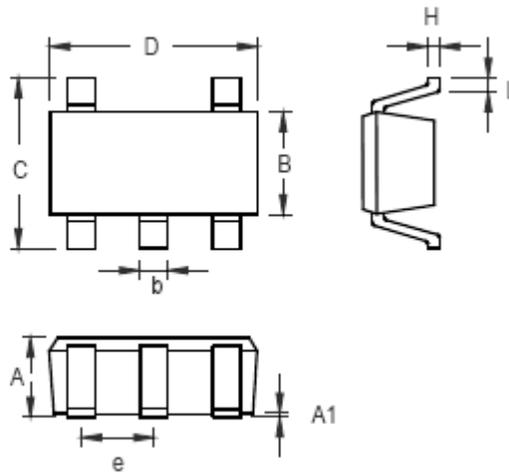
17.1 SOP-8 (Exposed Pad)



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	4.801	5.004	0.189	0.197	
B	3.810	4.000	0.150	0.157	
C	1.346	1.753	0.053	0.069	
D	0.330	0.510	0.013	0.020	
F	1.194	1.346	0.047	0.053	
H	0.170	0.254	0.007	0.010	
I	0.000	0.152	0.000	0.006	
J	5.791	6.200	0.228	0.244	
M	0.406	1.270	0.016	0.050	
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

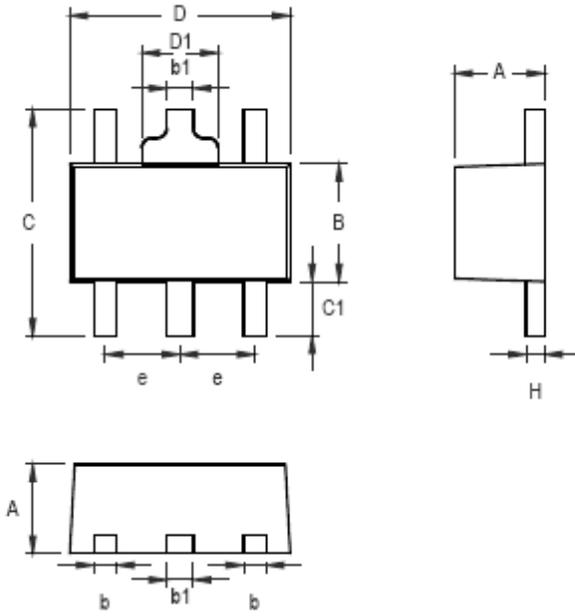
8-Lead SOP (Exposed Pad) Plastic Package

Note 8. The package of the RT9069 uses Option 1.



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

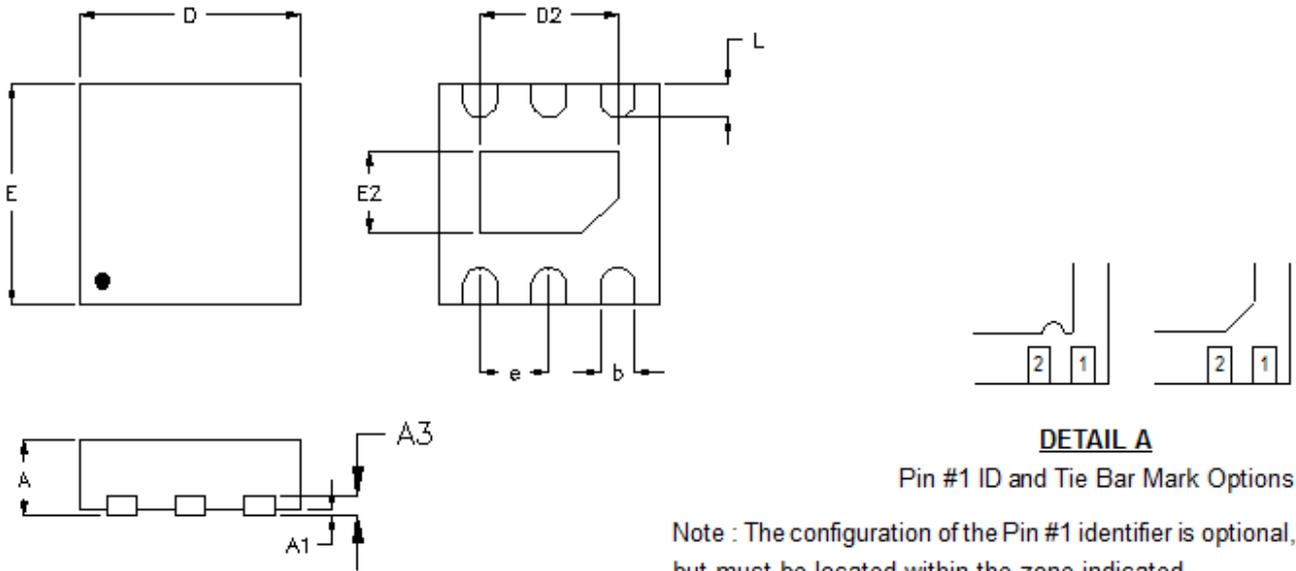
SOT-23-5 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.360	0.508	0.014	0.020
B	2.400	2.600	0.094	0.102
b1	0.406	0.533	0.016	0.021
C	3.937	4.250	0.155	0.167
C1	0.800	1.194	0.031	0.047
D	4.400	4.600	0.173	0.181
D1	1.397	1.700	0.055	0.067
e	1.400	1.600	0.055	0.063
H	0.356	0.430	0.014	0.017

5-Lead SOT-89 Surface Mount Package

17.4 UDFN-6L 1.6x1.6 (U-type)

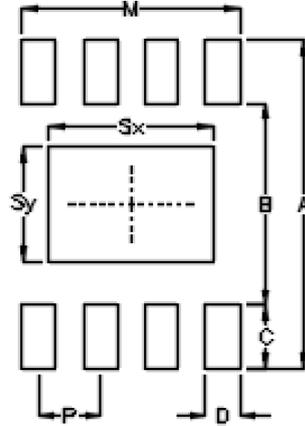


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.175	0.004	0.007
b	0.200	0.300	0.008	0.012
D	1.500	1.700	0.059	0.067
D2	0.950	1.050	0.037	0.041
E	1.500	1.700	0.059	0.067
E2	0.550	0.650	0.022	0.026
e	0.500		0.020	
L	0.200	0.300	0.008	0.012

U-Type 6L DFN 1.6x1.6 Package

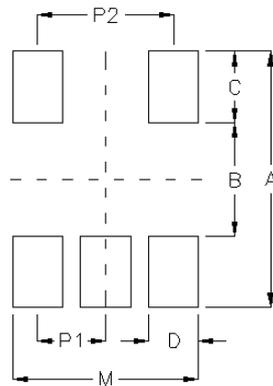
18 Footprint Information

18.1 SOP-8 (Exposed Pad)



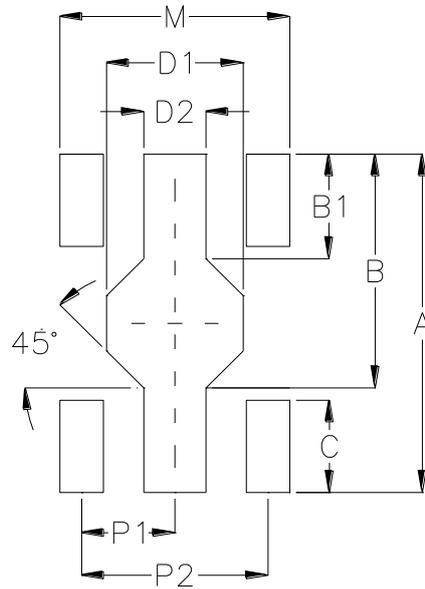
Package		Number of Pin	Footprint Dimension (mm)							Tolerance	
			P	A	B	C	D	Sx	Sy		M
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

Note 9. The package of the RT9069 uses Option 1.



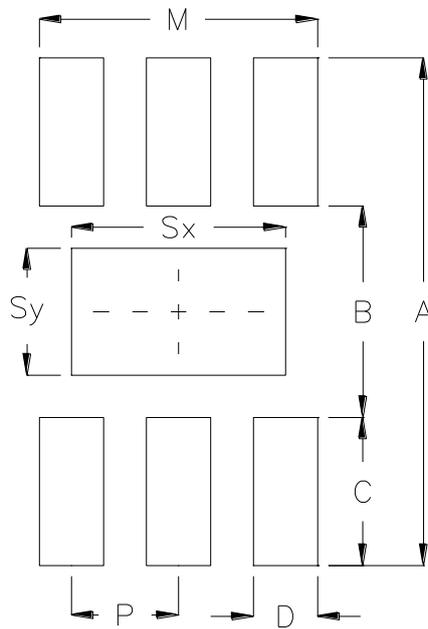
Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P1	P2	A	B	C	D	M	
TSOT-25/TSOT-25(FC)/SOT-25	5	0.95	1.90	3.60	1.60	1.00	0.70	2.60	±0.10

18.3 SOT-89-5



Package	Number of Pin	Footprint Dimension (mm)										Tolerance
		P1	P2	A	B	B1	C	D	D1	D2	M	
SOT-89-5	5	1.50	3.00	5.50	3.80	1.70	1.50	0.70	2.20	1.00	3.70	±0.10

18.4 UDFN-6L 1.6x1.6 (U-type)

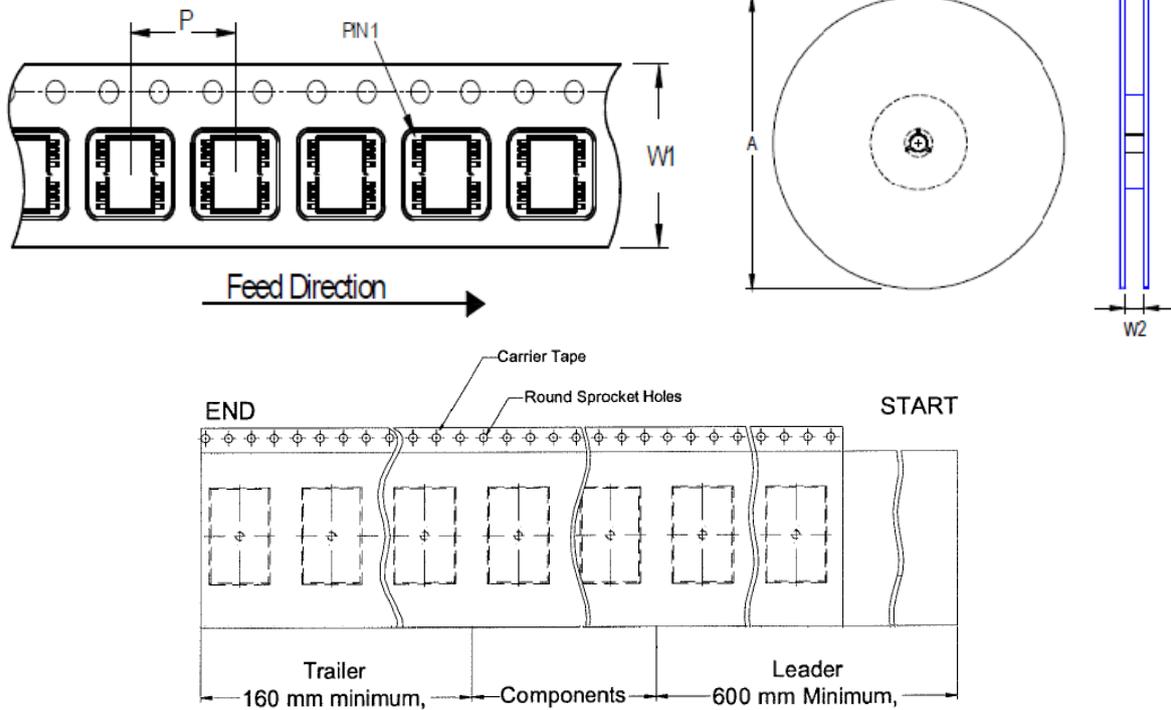


Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN1.6x1.6-6	6	0.50	2.40	1.00	0.70	0.30	1.00	0.60	1.30	±0.05

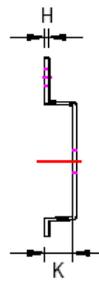
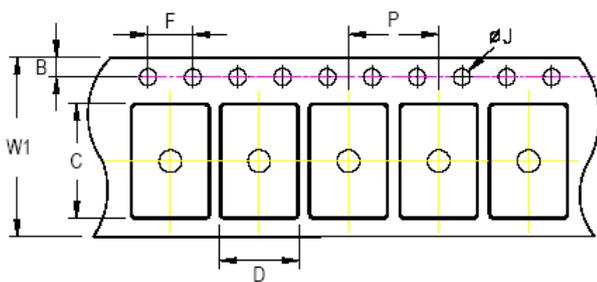
19 Packing Information

19.1 Tape and Reel Data

19.1.1 SOP-8 (Exposed Pad)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4



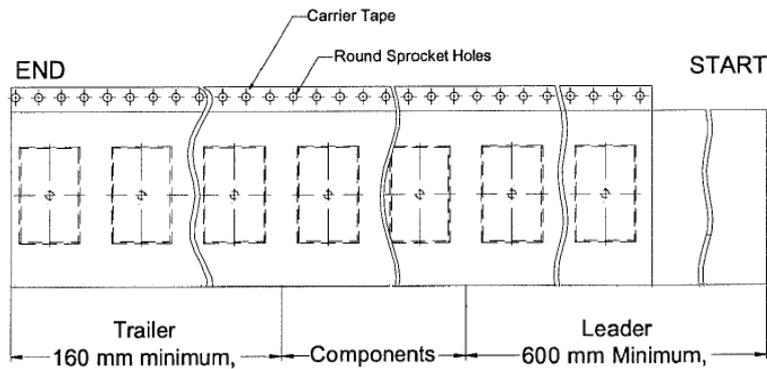
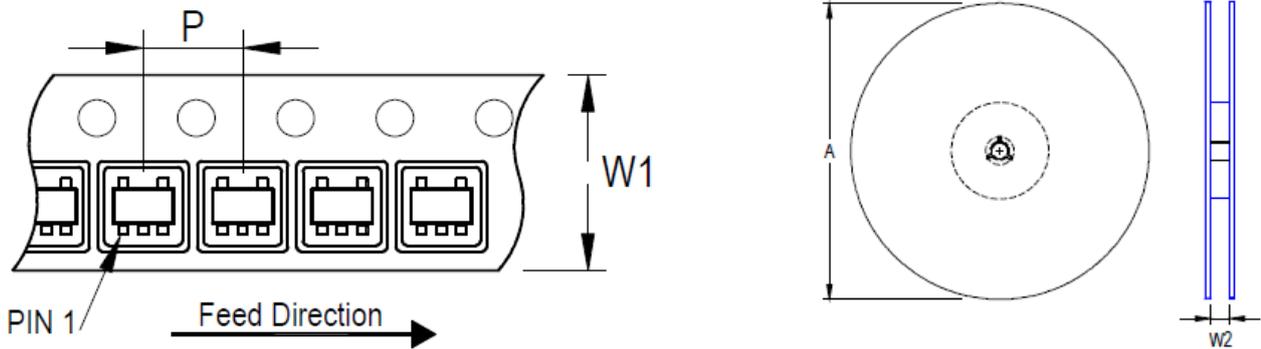
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

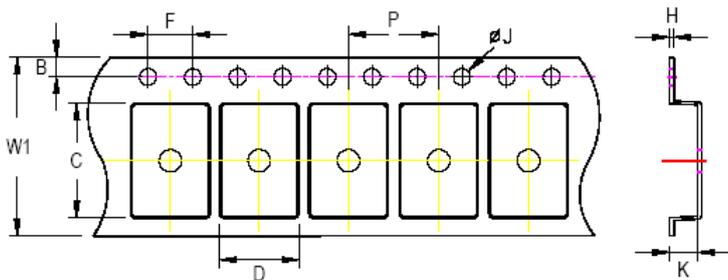
Tape Size	W1		P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.	
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.3mm	0.6mm	

19.1.2 SOT-23-5

SOT/TSOT-23-5



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT-23-5	8	4	180	7	3,000	160	600	8.4/9.9

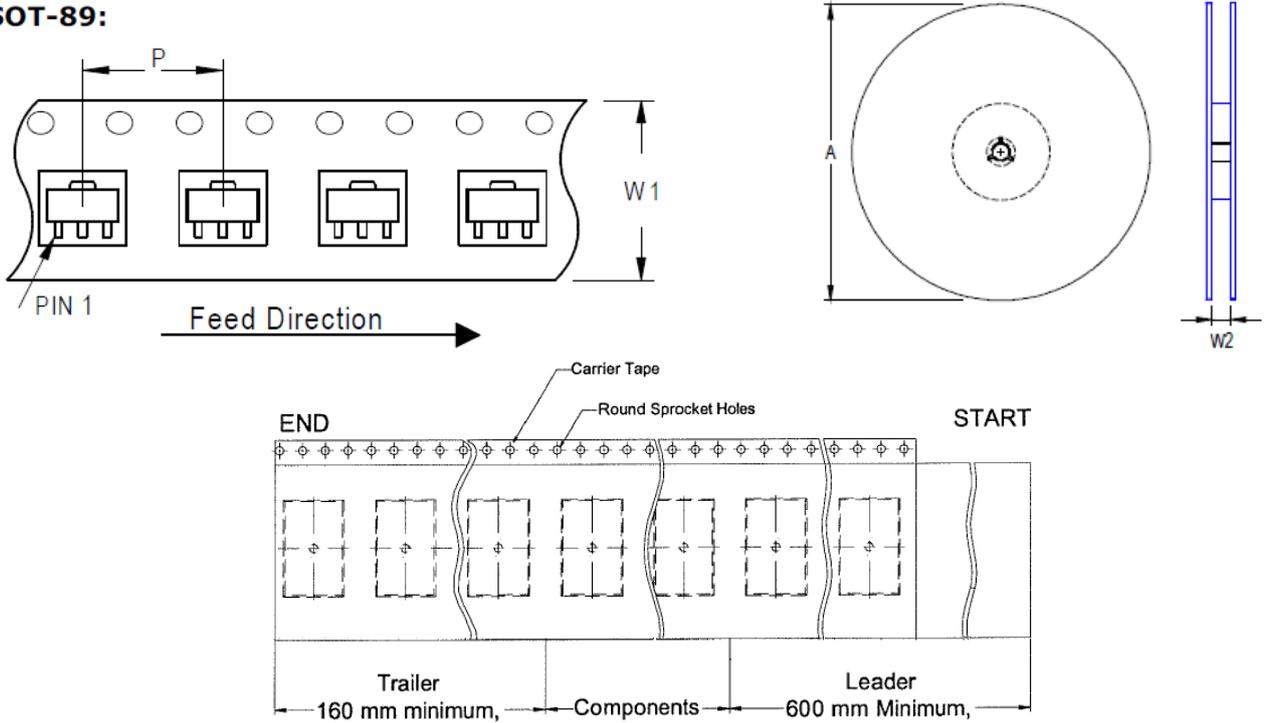


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
 - For 8mm carrier tape: 0.5mm max.

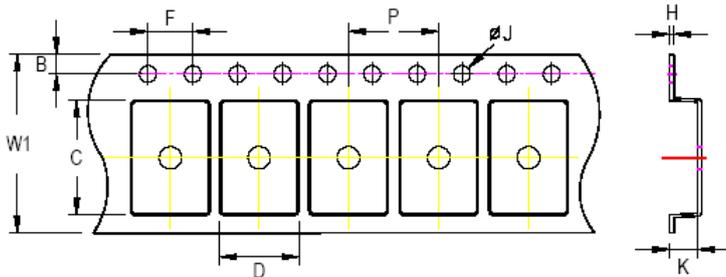
Tape Size	W1		P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max	
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.3mm	1.7mm	0.6mm	

19.1.3 SOT-89-5

SOT-89:



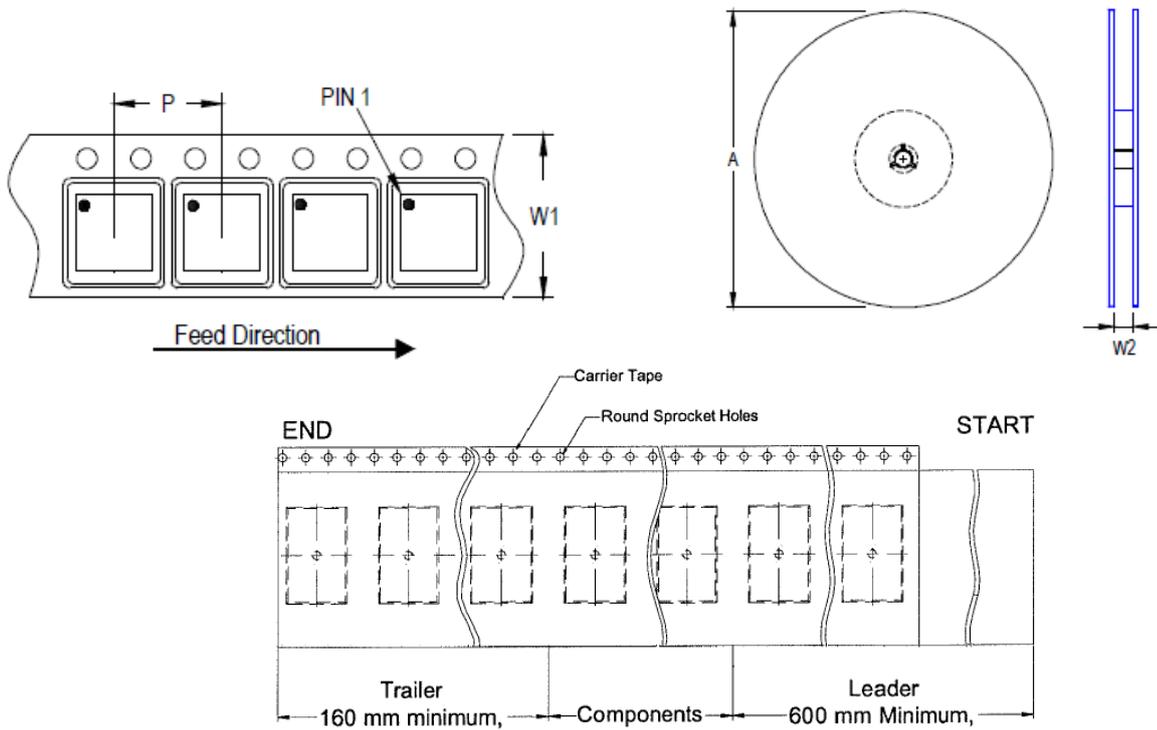
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT-89	12	8	180	7	1,000	160	600	12.4/14.4



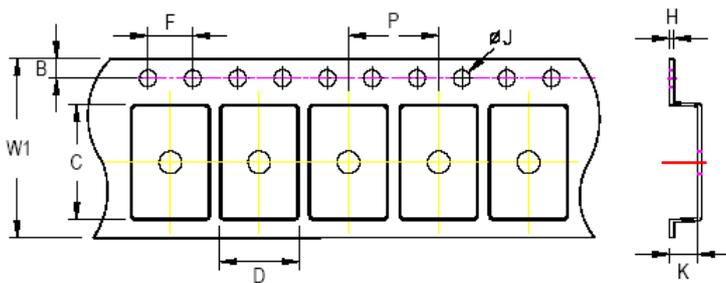
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.7mm	2.0mm	0.6mm

19.1.4 UDFN-6L 1.6x1.6 (U-type)



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
UQFN/DFN 1.6x1.6	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1		P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.	
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.9mm	0.6mm	

19.2 Tape and Reel Packing

19.2.1 SOP-8 (Exposed Pad)

Step	Photo/Description	Step	Photo/Description
1	 Reel 13"	4	 1 reel per inner box Box G
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box Carton A

Package	Container	Reel		Box			Carton		
		Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8		13"	2,500	Box G	1	2,500	Carton A	6	15,000

19.2.2 SOT-23-5

Step	Photo/Description	Step	Photo/Description
1	 Reel 7"	4	 3 reels per inner box Box A
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box Carton A

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-23-5	7"	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.2.3 SOT-89-5

Step	Photo/Description	Step	Photo/Description
1	 Reel 7"	4	 3 reels per inner box Box A
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box Carton A

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-89	7"	1,000	Box A	3	3,000	Carton A	12	36,000
			Box E	1	1,000	For Combined or Partial Reel.		

19.2.4 UDFN-6L 1.6x1.6 (U-type)

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>3 reels per inner box Box A</p>
2	 <p>HIC & Desiccant (1 Unit) inside</p>	5	 <p>12 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
UQFN & DFN 1.6x1.6	7"	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}					

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
 Hsinchu, Taiwan, R.O.C.
 Tel: (8863)5526789

RICHTEK

Richtek products are sold by description only. Richtek reserves the right to change the circuitry and/or specifications without notice at any time. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.

Copyright © 2025 Richtek Technology Corporation. All rights reserved. **RICHTEK** is a registered trademark of Richtek Technology Corporation.

20 Datasheet Revision History

Version	Date	Description	Item
10	2025/5/28	Modify	<p><i>General Description on page 1</i></p> <ul style="list-style-type: none"> - Added junction temperature range and ambient temperature range <p><i>Marking Information on page 1</i></p> <ul style="list-style-type: none"> - Deleted marking notes <p><i>Features on page 1</i></p> <ul style="list-style-type: none"> - Moved RoHS related information to the notes of Ordering Information <p><i>Ordering Information on page 1</i></p> <ul style="list-style-type: none"> - Updated representation - Added Note 1 <p><i>Absolute Maximum Ratings on page 6</i></p> <ul style="list-style-type: none"> - Updated description of Note 3 <p><i>Electrical Characteristics on page 7</i></p> <ul style="list-style-type: none"> - Modified values of Min and Max for Enable Input Voltage Rising Threshold and Enable Input Voltage Falling Threshold <p><i>Operation on page 13</i></p> <ul style="list-style-type: none"> - Moved from page 3 <p><i>Application Information on page 14</i></p> <ul style="list-style-type: none"> - Added Note 7 <p><i>Outline Dimension \ SOP-8 (Exposed Pad) on page 15</i></p> <ul style="list-style-type: none"> - Added note of package option <p><i>Footprint Information from page 19 to 22</i></p> <ul style="list-style-type: none"> - Added Chapter 18 <p><i>Packing Information from page 23 to 31</i></p> <ul style="list-style-type: none"> - Added Chapter 19