W35N01JWxxxG/T DATASHEET BRIEF

1.8V 1G-BIT
SERIAL SLC NAND FLASH MEMORY
OCTAL SPI WITH 166MHZ SDR & 120MHZ DDR
BUFFER READ & CONTINUOUS READ

This is a brief version of the W35N01JWxxxG/T datasheet. For complete information, please refer to the datasheet full version. To request access to the full version of the W35N01JWxxxG/T datasheet, please contact Winbond.

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Revision A

1. GENERAL DESCRIPTIONS

The W35N01JW (1G-bit) Serial SLC NAND Flash Memory provides a storage solution for systems with limited space, pins and power. The W35N SpiFlash family incorporates the popular Octal SPI interface which delivers the highest synchronous byte-wide (8-bit) data bandwidth on code and data storage memory solutions for embedded applications. The device operates on a single 1.70V to 1.95V power supply with current consumption as low as 25mA active and 10µA for standby.

The W35N01JW 1G-bit memory array is organized into 32,768 programmable pages of 4,096-Byte each. The entire page can be programmed at one time using the data from the 4,096-Byte internal buffer. Pages can be erased in groups of 64 (256KB block erase). The W35N01JW has 512 erasable blocks.

The W35N01JW supports Standard Serial Peripheral Interface (SPI) and 8-bit I/O (Octal) interface as well as Double Data Rate (DDR): Serial Clock (CLK), Chip Select (/CS), Serial Data (IO7, IO6, IO5, IO4, IO3, IO2 (/WP), IO1, IO0), /Reset, and Data Strobe (DS) for BGA packages. Clock frequencies of up to 120MHz is supported with DDR Data Strobe allowing equivalent clock rates of 240MHz x 8 for DDR Octal I/O Read instructions.

The W35N01JW provides a new Continuous Read Mode that allows for efficient access to the entire memory array with a single Read command. This feature is ideal for code shadowing applications.

For Read operations, configuration register values control the device operational settings such as the IO mode configuration, the number of dummy clock cycles, output buffer drive strength, and address mode configuration setting. In DDR IO mode, data transmission is on both clock edges (rising/falling) and on eight data lines, so legacy 8-bit (Byte) SPI commands are supported with only one clock cycle to latch in the command opcode. The Data Strobe (DS) pin optimizes the device operation when latching data with the DDR speed of up to the maximum frequency (120 MHz).

2. FEATURES

- **New Octal DDR Serial NAND Memories**
  - W35N01JW: 1G-bit / 128M-Byte
- **Supported Synchronous Bus I/F**
  - Byte-Wide (x8) Multiplexed Synchronous IO
  - Single Data Rate and Double Data Rate
  - DDR Bus Mode
  - Octal Double Data Rate (ODDR) protocol: CLK, /CS, IO[7:0], DS, /Reset
  - SDR Bus Mode
  - Octal SPI (OSPI) and OSPI DDR protocol: CLK, /CS, IO[7:0] /WP, /Reset
  - Standard SPI protocol (SPI): CLK, /CS, IO0, IO1, /WP, /Reset
- **Clock Frequency**
  - 166MHz SDR max (166MB/s)
  - 120MHz DDR max (240MB/s) with DS
- **Efficient "Continuous Read Mode"(1)**
  - Alternative method to the Buffer Read Mode
  - No need to issue "Page Data Read" between Read commands
  - Allows direct read access to the entire array
- **Flexible Architecture with 256KB blocks**
  - Uniform 256K-Byte Block Erase
  - Flexible page data load methods
- **Advanced Features**
  - On-chip 1-Bit ECC for memory array
  - ECC status bits indicate ECC results
  - Bad Block Management and LUT(2) access
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Unique ID and parameter pages
  - Ten 4KB OTP pages(3)
- **Space Efficient Packaging**
  - 24-ball TFBGA 8x6-mm
  - Contact Winbond for other package options

Notes:

1. Only the Read command structures are different between the "Continuous Read Mode (BUF=0)" and the "Buffer Read Mode (BUF=1)", all other commands are identical
   W35N01JWxxxG: Default BUF=1 after power up
   W35N01JWxxxT: Default BUF=0 after power up
2. LUT stands for Look-Up Table
3. OTP pages can only be programmed

3. PIN DESCRIPTIONS

3.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Data Input Output (IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and “Power-up Power-down Timing Requirements”). If needed, a pull-up resistor on the /CS pin can be used to accomplish this.

3.2 Serial Clock (CLK)

The Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations"). In SDR mode, data input are latched on the rising edge of CLK and data output are shifted out on the falling edge of CLK. In DDR mode, both data input and output are latched and shifted out on rising and falling edge of the CLK.

3.3 Data Input, Output (IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7)

The W35N01JW supports standard Single Data Rate (SDR) mode (using either SPI or Octal SPI), and Octal DDR operation. In SDR mode, Standard SPI instructions use the unidirectional IO0 (input) pin to serially write instructions, addresses, or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional IO1 (output) to read data or status from the device on the falling edge of CLK. Octal SPI instructions use the bi-directional IO[7:0] pins to serially write instructions (command input on IO0), addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.
Octal DDR mode operations also use bi-directional IO[7:0] pins using the rising and falling edge of CLK to latch in the input command, address, and data. Data output on IO[7:0] pins are shifted out on the falling and rising edge of CLK.

3.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect bits BP[3:0] and Status Register Protect SRP bits SRP[1:0], a portion as small as 256K-Byte or up to the entire memory array can be hardware protected. The WP-E bit in the Protection Register (SR-1) controls the functions of the /WP pin. When OSPI or ODDR mode, the /WP pin function is not available since this pin is used for IO2.

When WP-E=0, the device is in the Software Protection mode that only SR-1 can be protected. The /WP pin functions as a data I/O pin for the Octal SPI or Octal DDR operations, as well as an active low input pin for the Write Protection function for SR-1.

When WP-E=1, the device is in the Hardware Protection mode that /WP becomes a dedicated active low input pin for the Write Protection of the entire device. If /WP is tied to GND, all “Write/Program/Erase” functions are disabled. The entire device (including all registers, memory array and OTP pages) will become read-only. Octal SPI or Octal DDR read operations are also disabled when WP-E is set to 1.

3.5 Data Strobe (DS)

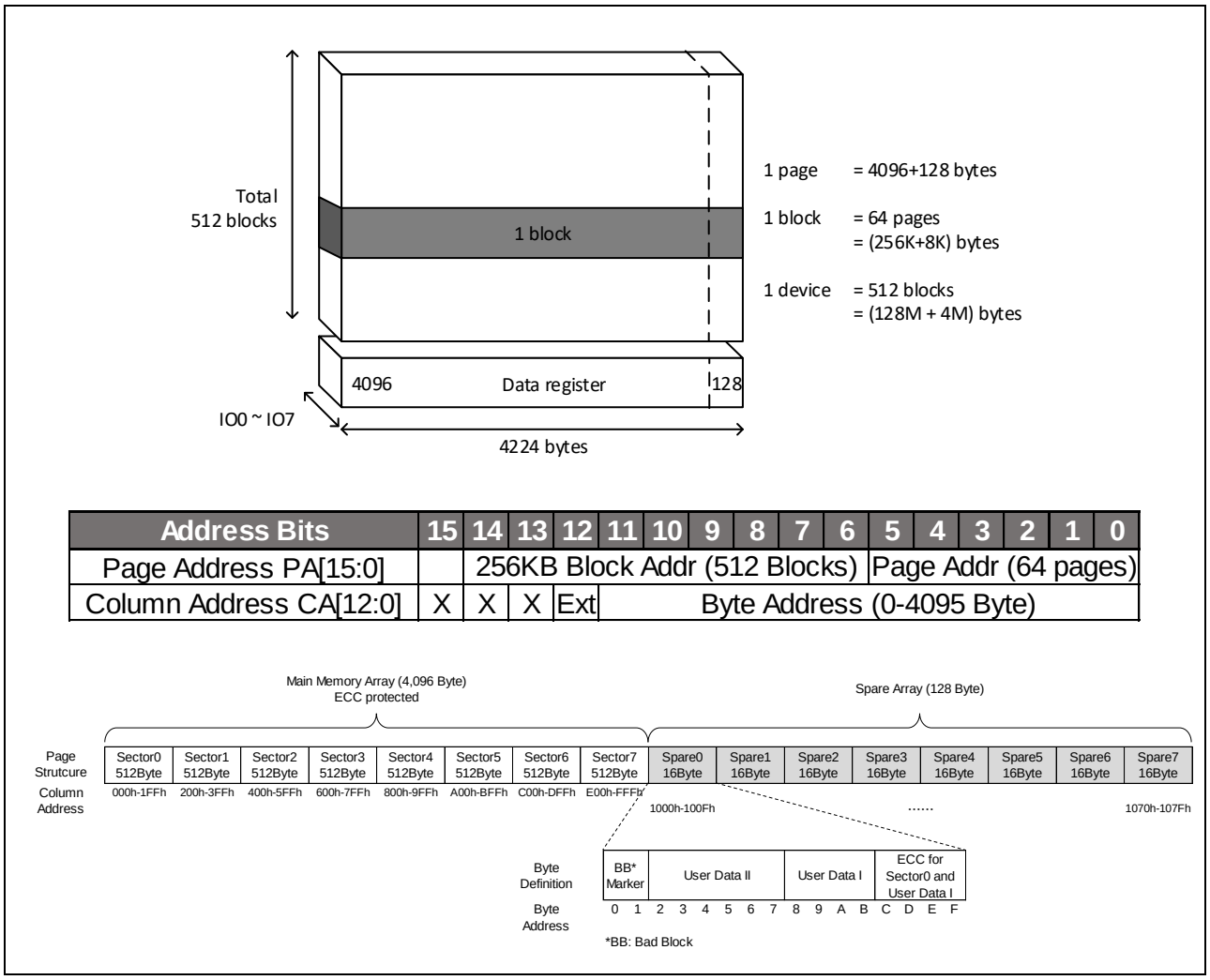
The Data Strobe (DS) pin is required to support high DDR clock speed of up to 120MHz. It is an output pin signal in aid of validating and synchronizing data output for the host. It is used during Standard SPI, OSPI and ODDR read operations and it is not used for program or erase operations. It is configured by Volatile Configuration Register Address 00h and Bit 5 (I/O Mode Configuration).

When enabled and used during Standard SPI, OSPI and ODDR reads, the device drives DS output pin low after inputting instruction code; and as the read sequence continues the device starts driving output data, where at the same time the DS pin toggles to synchronize data output transitions. DS pin is not driven when disabled.

3.6 Reset (/RESET)

The /RESET pin allows the device to be reset by the controller, and provides hardware level resetting. This is highest priority among all the input signals.

4. BLOCK DIAGRAM

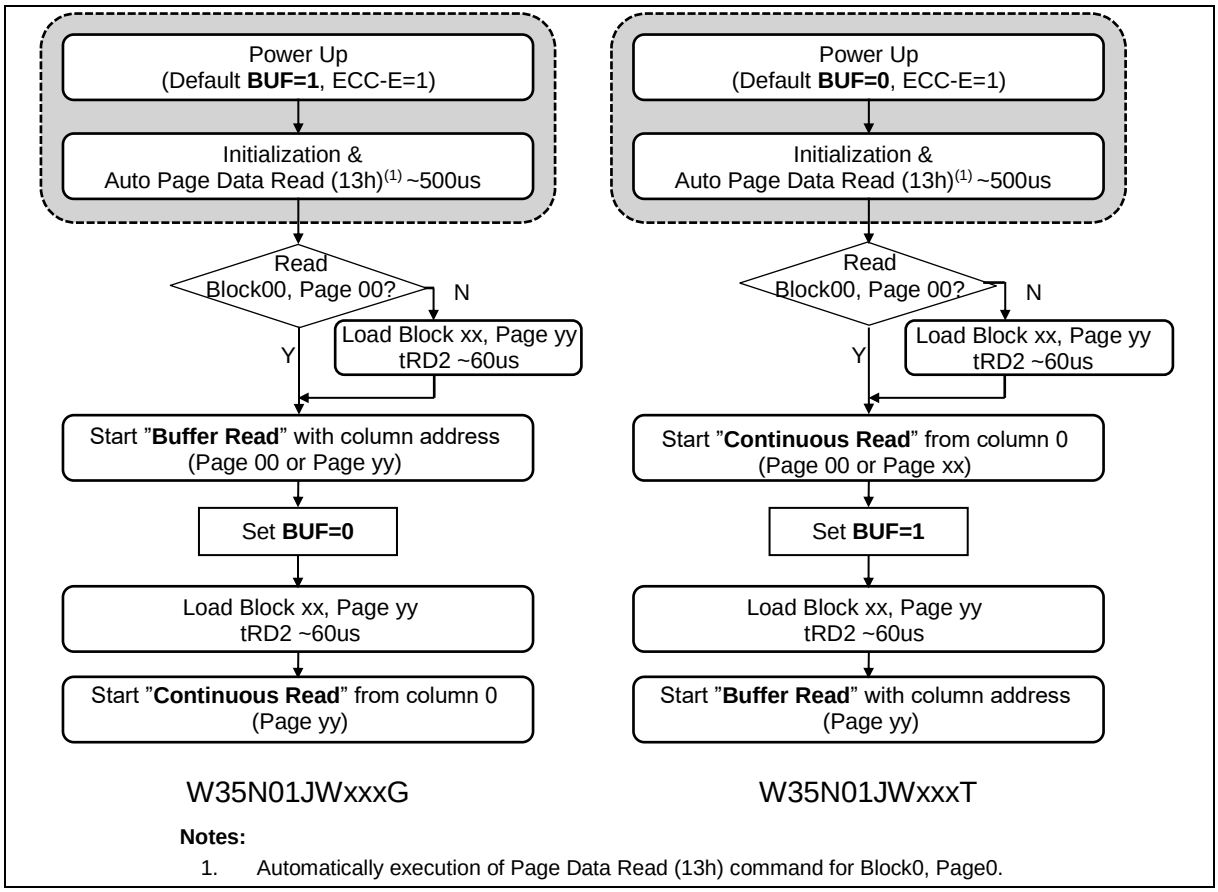


Address Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Page Address PA[15:0]		256KB Block Addr (512 Blocks)									Page Addr (64 pages)					
Column Address CA[12:0]	X	X	X	Ext	Byte Address (0-4095 Byte)											

Figure 4-1 W35N01JW Flash Memory Architecture and Addressing

5. FUNCTIONAL DESCRIPTIONS

5.1 Device Operation Flow



Notes:

1. Automatically execution of Page Data Read (13h) command for Block0, Page0.

Figure 5-1 W35N01JW Flash Memory Operation Diagram

5.2 Single Data Rate (SDR) Bus Interface

W35N01JW device supports standard SPI, Octal SPI, and Octal SPI with Address/Data Output DDR interfaces. The SDR protocols start with single bit SPI for command input then either transition to single, octal, or octal DDR during the address and data transmission depending on the instruction that is used. SDR Bus interface (SPI/OSPI/OSPI DDR) requires the Volatile Configuration Register Address 00h set to either FFh or DFh (see Volatile Configuration Register section for details).

5.2.1 Standard SPI Instructions

The W35N01JW is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (IO0 / Input only) and Serial Data Output (IO1 / Output only). Standard SPI instructions use the IO0 as input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The IO1 output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 is during the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

5.2.2 Octal SPI (OSPI) Instructions

W35N01JW supports Octal SPI (OSPI) operation when using instructions such as “Fast Read Octal Output (8Bh)”, and “Fast Read Octal I/O (CBh)”. These instructions allow data to be transferred to or from the device up to eight times the rate of ordinary SPI Serial Flash. The Octal Read instructions offer a significant improvement in transfer rates allowing fast code-shadowing to RAM. When using Octal SPI instructions the IO0 and IO1 become bidirectional IO pins; /WP pin becomes bidirectional IO2 pin; IO3, IO4, IO5, IO6, and IO7 pins also become bidirectional; that comprise to a total 8-pin (byte-wide) of synchronous data IO.

5.3 Octal Double Data Rate (ODDR) Bus Interface

The W35N01JW device supports Octal Double Data Rate (ODDR) bus interface. The ODDR protocol starts with 8-bit (byte-wide) synchronous bus interface on both rising and falling edge of the CLK (DDR) from the command input, address input and data input/output sequences. When in the ODDR mode, all the instructions are supported in DDR mode sequence that maximized the data transmission. ODDR Bus interface mode requires the Volatile Configuration Register Address 00h set to either E7h with DS or C7h without DS (see Volatile Configuration Register section for details).

5.3.1 DDR OSPI Read Instructions

To effectively improve the SPI/OSPI read operation throughput without increasing the serial clock frequency, W35N01JW introduces multiple Double Data Rate (DDR) Read during address input and data output phase of the instruction sequence supported in SPI/OSPI DDR Read instructions. The byte-wide single bit command code is still latched into the device on the rising edge of the serial clock similar to all other SPI/OSPI instructions. Once a DDR command code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock. The SPI DDR instruction is 8Bh. The OSPI DDR instruction is 9Dh.

5.4 Software Reset

5.4.1 Device Reset (FFh) instruction

The Device Reset (FFh) instruction terminates any on-going internal operations without initialization for all volatile writable bits in the Status Registers. If the command sequence is successfully accepted, the device will take approximately tRST to reset. No command will be accepted during the reset period. Please refer to “7.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detail information about command sequence and the value of each Status Registers after reset.

5.4.2 Enable Reset (66h) and Reset Device (99h) instructions

The W35N01JW can be reset to the initial state by Enable Reset (66h) & Reset (99h) instructions. If the command sequence is successfully accepted, the device will take approximately tRST to reset. No command will be accepted during the reset period. Please refer to “7.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detail information about command sequence and the value of each Status Registers after reset.

5.5 Hardware Reset

5.5.1 /RESET Pin

For the SOIC and TFBGA package types, the W35N01JW provides a dedicated /RESET pin. Drive /RESET pin low for a minimum period of 1us (tRESET) will reset the device to its initial power-on state. It takes same busy time with power-on (tVSL and tPUW) because Hardware Reset goes into the same state of after power-on. No command will be accepted during the tVSL period. Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum of 1us (tRESET) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and /HOLD). Please refer to “7.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)” for detail information about the value of each Status Registers after reset.

Notes:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on SOIC and TFBGA package. If the reset function is not used, this pin can be left floating in the system.

5.6 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W35N01JW provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Write enable/disable instructions and automatic write disable after erase or program or page data read or program execute for OTP pages
- Software and Hardware (/WP pin) write protection using Protection Register (SR-1)
- Lock Down write protection for Protection Register (SR-1) until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register (SR-1)
- Hardware write protection using /WP pin when WP-E is set to 1

Upon power-up or at power-down, while VCC is below VCC(min), (see “Power-up Power-down Timing Requirements”), all operations are disabled and no instructions are recognized. During power-up, after the VCC voltage exceeds VCC(min) and tVSL has elapsed, all program and erase related instructions are further disabled for a time delay of tPUW. This includes the Write Enable, Program Execute, Block Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute or Block Erase instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Protection Register section for further information.

The WP-E bit in Protection Register (SR-1) is used to enable the hardware protection. When WP-E is set to 1, bringing /WP low in the system will block any Write/Program/Erase command to the W35N01JW, the device will become read-only. The OSPI operations are also disabled when WP-E is set to 1. When OSPI mode, the Write Protection function is not available.

6. PROTECTION, CONFIGURATION AND STATUS REGISTERS

The W35N01JW device has Status Register1-3, and Volatile Configuration Register. The Status Registers provide status on the availability of the flash memory array: whether the device is write enabled or disabled; the state of write protection; Program or Erase status and error indicator; Illegal access monitor on Protected/OTP register.

The Internal Configuration Register is an internal register that is accessed only by the Volatile Configuration Register, and configuration related Instructions. The initial settings are transferred to the Volatile Configuration Register, which has identical configuration/parameter as the default setting. Any configuration update during normal operating mode can be performed instantly by initiating Write Volatile Configuration Register which will trigger update on Internal Configuration Register and device operating behavior.

The Read Status Register instruction (05h / 0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results and ECC usage/status.

The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes and enable/disable ECC, Protection Register/OTP area lock, enable/disable. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

6.1 Status Register-1 (Volatile Writable)

The Status Register contains the nonvolatile bits for write protection, volatile write enable required before any write commands, and write in progress flag. The Write Status Register instruction is used to configure the device write protection features of the nonvolatile Status Register SRP0/1, TB, and BP[3:0] bits. Write access to these Status Register bits is controlled by the Status Register Protect Bit Bit7 (SRP0), the Write Enable instruction, and state of /WP pin.

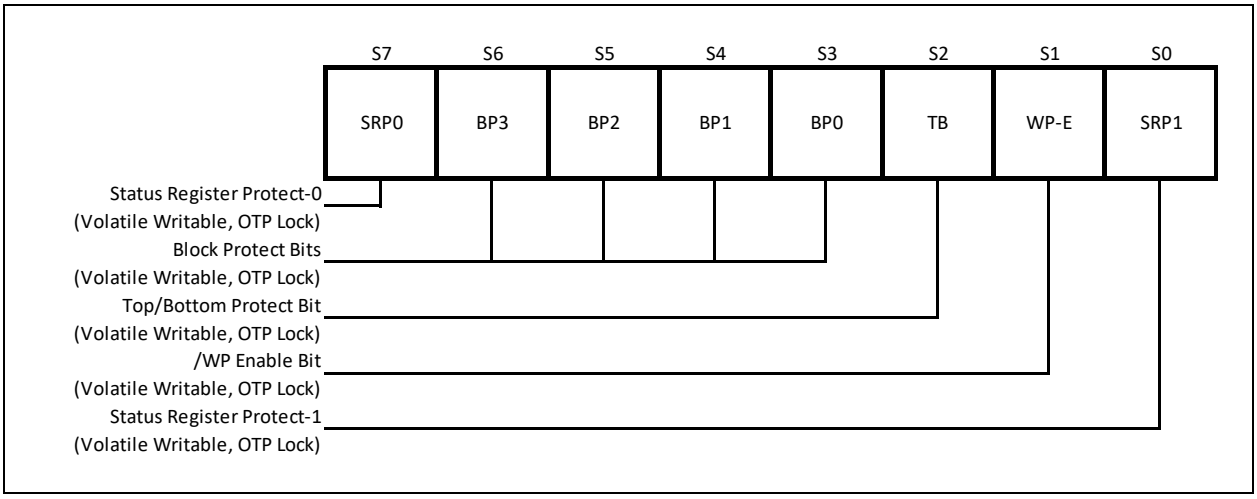


Figure 6-1 Protection Register / Status Register-1 (Address Axh)

6.1.1 Block Protect Bits (BP3, BP2, BP1, BP0, TB) – *Volatile Writable, OTP lockable*

The Block Protect bits (BP3, BP2, BP1, BP0 & TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The default values for the Block Protection bits are 1 after power up to protect the entire array. If the SR1-L bit in the Configuration Register (SR-2) is set to 1, the default values will the values that are OTP locked.

6.1.2 Write Protection Enable Bit (WP-E) – *Volatile Writable, OTP lockable*

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, /WP pin functionality, and Octal SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP pin is multiplexed as IO pins, and Octal program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Octal functions are disabled and /WP pin becomes dedicated control input pins.

6.1.3 Status Register Protect Bits (SRP1, SRP0) – *Volatile Writable, OTP lockable*

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Software Protection (Driven by Controller)				
SRP1	**SRP0**	**WP-E**	**/WP / IO2**	**Descriptions**
0	0	0	X	No /WP functionality */WP pin will always function as IO2*
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) */WP pin will function as IO2 for Octal operations* *Write SR-1 instruction with ODDR cannot be used*
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) */WP pin will function as IO2 for Octal operations* *Write SR-1 instruction with ODDR cannot be used*
1	0	0	X	Power Lock Down(1) SR-1 */WP pin will always function as IO2*
1	1	0	X	Enter OTP mode to protect SR-1 (allow SR1-L=1) */WP pin will always function as IO2*

Hardware Protection (System Circuit / PCB layout)				
SRP1	**SRP0**	**WP-E**	**/WP only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock-Down(1) SR-1
1	1	1	VCC	Enter OTP mode to protect SR-1 (allow SR1-L=1)
X	X	1	GND	All "Write/Program/Erase" commands are blocked Entire device (SRs, Array, OTP area) is read-only

Notes:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.
2. When WP-E=1, Octal functions have to be ignored.

6.2 Status Register-2 (Volatile Writable)

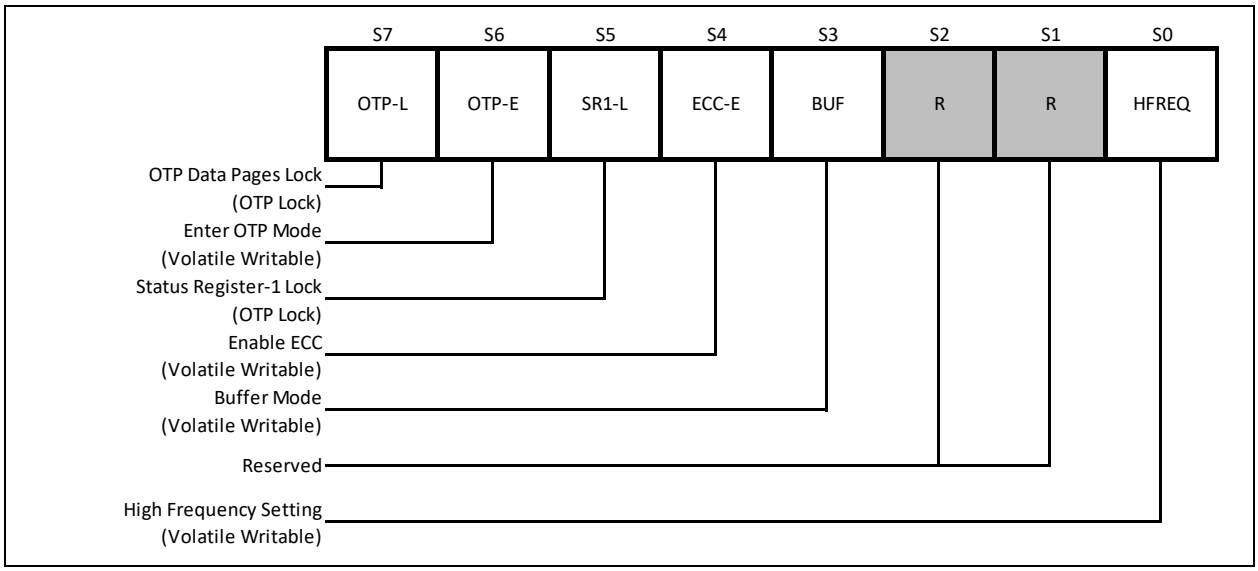


Figure 6-2 Configuration Register / Status Register-2 (Address Bxh)

6.2.1 One Time Program Lock Bit (OTP-L) – *OTP lockable*

In addition to the main memory array, W35N01JW also provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 10 pages of 4,224-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and data is not reversible ("0" to "1") by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data. In order to set OTP-L bit, the device must enter the "OTP Access Mode" (OTP-E=1) first, or set OTP-E=1 and OTP-L=1 simultaneously..

6.2.2 Enter OTP Access Mode Bit (OTP-E) – *Volatile Writable*

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up or a RESET command is 0.

6.2.3 Status Register-1 Lock Bit (SR1-L) – *OTP lockable*

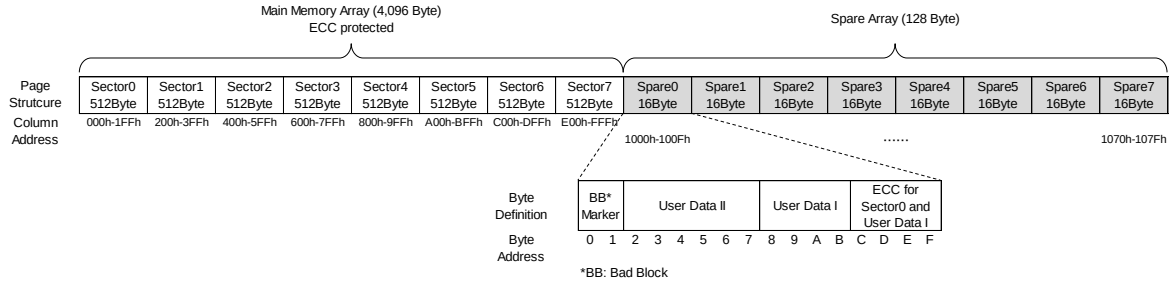
The SR1-L lock bit is used to OTP lock the values in the Protection Register (SR-1). Depending on the settings in the SR-1, the device can be configured to have a portion of or up to the entire array to be write-protected, and the setting can be OTP locked by setting SR1-L bit to 1. SR1-L bit can only be set to 1 permanently when SRP1 & SRP0 are set to (1, 1), and OTP Access Mode must be entered (OTP-E=1) to execute the programming.

6.2.4 ECC Enable Bit (ECC-E) – *Volatile Writable*

W35N01JW has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 128-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bit. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

The constraint when ECC-E=1 are as follows:

- The areas protected by ECC is shown in the table below. User Data I is protected by ECC, but User Data II is out of protected by ECC.
- The Number of Partial Page Program (NoP) is 4 for the entire page, including the spare area. Therefore the user needs to program one sector and optionally User Data 1 of pared spare area (example, main area-sector 0 and spare area-spare 0) at one time program to properly and automatically program the ECC parity code.



Area	Main area							
	Sector 0	Sector 1	Sector 2	Sector 3	Sector 4	Sector 5	Sector 6	Sector 7
Address (Start)	000h	200h	400h	600h	800h	A00h	C00h	E00h
Address (End)	1FFh	3FFh	5FFh	7FFh	9FFh	BFFh	DFFh	FFFh
Size	512B	512B	512B	512B	512B	512B	512B	512B

Area	Spare area											
	Spare 0			Spare 1			Spare 2			Spare 3		
	UD2	UD1	EPC	UD2	UD1	EPC	UD2	UD1	EPC	UD2	UD1	EPC
Address (Start)	1000h	1008h	100Ch	1010h	1018h	101Ch	1020h	1028h	102Ch	1030h	1038h	103Ch
Address (End)	1007h	100Bh	100Fh	1017h	101Bh	101Fh	1027h	102Bh	102Fh	1037h	103Bh	103Fh
Size	8B	4B	4B	8B	4B	4B	8B	4B	4B	8B	4B	4B

Area	Spare area											
	Spare 4			Spare 5			Spare 6			Spare 7		
	UD2	UD1	EPC	UD2	UD1	EPC	UD2	UD1	EPC	UD2	UD1	EPC
Address (Start)	1040h	1048h	104Ch	1050h	1058h	105Ch	1060h	1068h	106Ch	1070h	1078h	107Ch
Address (End)	1047h	104Bh	104Fh	1057h	105Bh	105Fh	1067h	106Bh	106Fh	1077h	107Bh	107Fh
Size	8B	4B	4B	8B	4B	4B	8B	4B	4B	8B	4B	4B

Notes:

1. UD2: User Data II
2. UD1: User Data I
3. EPC: ECC parity code
4. The gray area of the above table is protected by ECC

6.2.5 Buffer Read / Continuous Read Mode Bit (BUF) – *Volatile Writable*

W35N01JW provides two different modes for read operations, Buffer Read Mode (BUF=1) and Continuous Read Mode (BUF=0). Prior to any Read operation, a Page Data Read command is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power up, the data in page 0 will be automatically loaded into the Data Buffer and the device is ready to accept any read commands.

The Buffer Read Mode (BUF=1) requires a Column Address to start outputting the existing data inside the Data Buffer, and once it reaches the end of the data buffer (Byte 4,224), IO pins will become high-Z state.

The Continuous Read Mode (BUF=0) doesn't require the starting Column Address. Even though host issues CA to device after read instruction, the device ignore the input address, and will always start output the data from the first column (Byte 0) of the Data buffer, and once the end of the data buffer (Byte 4,096 for ECC=1, Byte 4,224 for ECC=0) is reached, the data output will continue through the next memory page. With Continuous Read Mode, it is possible to read out the entire memory array using a single read command. Please refer to respective command descriptions for the dummy cycle requirements for each read commands under different read modes.

For W35N01JWxxxG part number, the default value of BUF bit after power up is 1. BUF bit can be written to 0 in the Status Register-2 to perform the Continuous Read operation.

For W35N01JWxxxT part number, the default value of BUF bit after power up is 0. BUF bit can be written to 1 in the Status Register-2 to perform the Buffer Read operation.

BUF	ECC-E	Read Mode (Starting from Buffer)	ECC Status	Data Output Structure
1	0	Buffer Read	N/A	4,096 + 128
1	1	Buffer Read	Page based	4,096 + 128
0	0	Continuous Read	N/A	4,096 + 128
0	1	Continuous Read	Operation based	4,096

6.2.6 High Frequency Setting Bit (HFREQ) – *Volatile Writable*

W35N01JW can output data at max DDR 120MHz with Continuous Read Mode. When system uses 90MHz or more higher frequency for Octal SPI DDR with Continuous Read Mode, HFREQ bit needs to set to "1", then the internal data transfer method is changed and stable data output is executed during higher frequency. Furthermore, when HFREQ is set to "1", stopping the clock with /CS=L is prohibited, and operating with Single SPI or Octal SPI SDR is also prohibited. The default value of HFREQ is "0" and support all STR operation, Buffer Read mode operation, and lower than DDR 89MHz with Continuous Read Mode.

6.3 Status Register-3 (Status only)

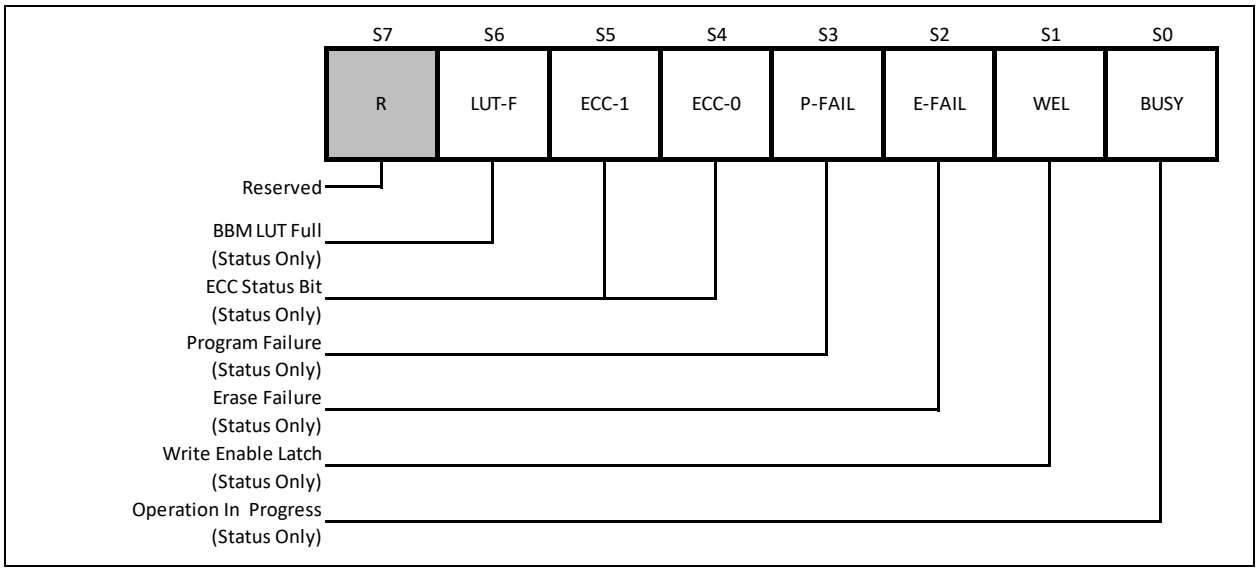


Figure 6-3 Status Register-3 (Address Cxh)

6.3.1 Look-Up Table Full (LUT-F) – *Status Only*

To facilitate the NAND flash memory bad block management, the W35N01JW is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 10 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 10 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 10 links are used, LUT-F will become 1, and no more memory block links may be established.

6.3.2 Cumulative ECC Status (ECC-1, ECC-0) – *Status Only*

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don't care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command or a Page Data Read command.

ECC Status		Descriptions
ECC-1	ECC-0	
0	0	The entire data output is provided without requiring any ECC correction.
0	1	The entire data output experienced a 1 bit correction event per 1 sector one or more times after reading either single or multiple pages.
1	0	The entire data output experienced a 2 bit error event per 1 sector one or more times in a single page that cannot be error corrected[2]. In the Continuous Read Mode, an additional command can be used to read out the Page Address (PA) that contains the error.
1	1	The entire data output experienced a 2 bit error event per 1 sector one or more times in multiple pages. In the Continuous Read Mode, the additional command can only provide the last Page Address (PA) that contain the 2 bit error. PAs for other pages with the 2 bit error is not available. The data read is not suitable for use[2, 3].

Notes:

1. As the ECC engine is based on Hamming code, the ECC status bits are applicable for 1 bit ECC correction and 2 bit ECC detection. This OctalNAND is not expected to experience 3 or more bits of error when used within the datasheet specifications. When there is a 1 bit error correction event, user may decide to erase and reprogram the associated block, based on the user's quality policy.
2. If the read operation contains both 1 and 2 bit error event, the 2 bit error condition will be used.
3. ECC-1, ECC-0 = (1, 1) is only applicable during Continuous Read operation (BUF=0).

6.3.3 Program Failure (P-FAIL) – *Status Only*

The Program Failure Bit is used to indicate whether the internally-controlled Program operation was executed successfully (P-FAIL=0) or timed out (P-FAIL=1). The P-FAIL bit is also set when the Program command is issued to a locked or protected memory array or OTP area. This bit is cleared at the beginning of the Program Execute instruction on an unprotected memory array or OTP area. Device Reset instruction can also clear the P-FAIL bit.

6.3.4 Erase Failure (E-FAIL) – *Status Only*

The Erase Failure Bit is used to indicate whether the internally-controlled Erase operation was executed successfully (E-FAIL=0) or timed out (E-FAIL=1). The E-FAIL bit is also set when the Erase command is issued to a locked or protected memory array. This bit is cleared at the beginning of the Block Erase instruction on an unprotected memory array. Device Reset instruction can also clear the E-FAIL bit.

6.3.5 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read and Program Execute for OTP pages.

6.3.6 Read/Erase/Program in Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, BBM Management, Program Execute, Block Erase and Program Execute for OTP area, OTP Locking or after a Continuous Read instruction. During this time the device will ignore further instructions except for the Read Status Register, Reset and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

6.4 Volatile Configuration Register

Volatile Configuration Register values is a separate volatile register and configurable content. Table below provides the configurable features and definition of the Volatile Configuration Register. From power up or reset, the Volatile Configuration Register gets its values transferred from default values and the default values are also transferred directly to the Internal Configuration Register for device initial configuration. After power up or reset, changes to the configuration of the Volatile Configuration Register via Write Volatile Configuration Register instruction are transferred directly to the Internal Configuration Register which will instantly reflect to the device operation. Reserved values on the Volatile Configuration Register are FFh. Attempts to write on the reserved addresses are ignored which will trigger the setting of clearing of WEL bit to '0'. When Status Register-1 S1 bit WP-E is "1", VCR address 00h IO mode is prohibited to set to ODDR. In order to set ODDR, it is necessary to be WP-E = 0.

Address	Name	Description	Function Settings	Default
255h:05h	Reserved	Reserved	Reserved	-
04h	Reserved	Reserved	Reserved	FFh
03h	Output Driver Strength Configuration	Output impedance setting at VDD/2 output voltage during read operations	FFh: 100% FEh: 75% FDh: 50% FCh: 25% Others: Reserved	FFh
02h	Reserved	Reserved	Reserved	FFh
01h	Dummy Clock Cycle Configuration	Number of dummy clock cycle setting between the address input and expected data output for all Fast Read commands(1)	08h: 8 Dummy Cycles 0Ch: 12 Dummy Cycles 10h: 16 Dummy Cycles 14h: 20 Dummy Cycles 18h: 24 Dummy Cycles 1Ch: 28 Dummy Cycles FFh: Default(1) Others: Reserved	FFh
00h	Input/Output (I/O) Mode Configuration	The device will operate from Standard SPI to Octal DDR mode along with or without data strobe (DS)	FFh: Single SPI SDR with DS DFh: Octal SPI SDR without DS E7h: Octal SPI DDR with DS C7h: Octal SPI DDR without DS Others: Reserved	FFh

Notes:

1. Refer to the Instruction Set Table for default number of dummy clock cycle values.

6.4.1 Clock Frequency with Required Dummy Clock Cycles

Number of Dummy Clock Cycle setting	Fast Read [MHz]	Fast Read Octal Output [MHz]		Fast Read Octal I/O [MHz]	Octal DDR (ODDR) [MHz]
	SDR (0Bh)	SDR (8Bh)	DDR (9Dh)	SDR (CBh)	
08h	166	133	105	86	86
0Ch	166	166	120	124	120
10h	166	166	120	162	120
14h	166	166	120	166	120
18h	166	166	120	166	120
1Ch	166	166	120	166	120

6.5 W35N01JW Status Register Memory Protection

STATUS REGISTER(1)					W35N01JW (1G-BIT / 128M-BYTE) MEMORY PROTECTION(2)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[15:0]	PROTECTED DENSITY	PROTECTED PORTION
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	7FC0h - 7FFFh	256KB	Upper 1/512
0	0	0	1	0	510 & 511	7F80h - 7FFFh	512KB	Upper 1/256
0	0	0	1	1	508 thru 511	7F00h - 7FFFh	1MB	Upper 1/128
0	0	1	0	0	504 thru 511	7E00h - 7FFFh	2MB	Upper 1/64
0	0	1	0	1	496 thru 511	7C00h - 7FFFh	4MB	Upper 1/32
0	0	1	1	0	480 thru 511	7800h - 7FFFh	8MB	Upper 1/16
0	0	1	1	1	448 thru 511	7000h - 7FFFh	16MB	Upper 1/8
0	1	0	0	0	384 thru 511	6000h - 7FFFh	32MB	Upper 1/4
0	1	0	0	1	256 thru 511	4000h - 7FFFh	64MB	Upper 1/2
1	0	0	0	1	0	0000h – 003Fh	256KB	Lower 1/512
1	0	0	1	0	0 & 1	0000h - 007Fh	512KB	Lower 1/256
1	0	0	1	1	0 thru 3	0000h - 00FFh	1MB	Lower 1/128
1	0	1	0	0	0 thru 7	0000h - 01FFh	2MB	Lower 1/64
1	0	1	0	1	0 thru 15	0000h - 03FFh	4MB	Lower 1/32
1	0	1	1	0	0 thru 31	0000h - 07FFh	8MB	Lower 1/16
1	0	1	1	1	0 thru 63	0000h - 0FFFh	16MB	Lower 1/8
1	1	0	0	0	0 thru 127	0000h - 1FFFh	32MB	Lower 1/4
1	1	0	0	1	0 thru 255	0000h - 3FFFh	64MB	Lower 1/2
X	1	0	1	X	0 thru 511	0000h - 7FFFh	128MB	ALL
X	1	1	X	X	0 thru 511	0000h - 7FFFh	128MB	ALL

Notes:

2. X = don't care
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7. INSTRUCTIONS

The full instruction set of the W35N01JW consists of basic instructions (See Instruction Set Table) that are all supported in SDR mode. All instructions are also supported in ODDR mode except for legacy SPI read instructions 03h. The instruction sequences use Command, Address, or Data sequence with DDR option either driven by specific command in SDR or by register setting in ODDR during write and read protocols.

Instructions vary in length from an 8-bit command code to several bytes and may be followed by address input either in 24-bit, data input/output, dummy cycles, or a combination of address, dummy cycles and data output. The data portion of the input varies can either be used partial page programming in 1K byte or full page in 4K byte for memory area, OTP Register, Device ID, others. For some of the reads, a preset number of dummy cycles is required with register reads and memory reads before the data output. The number of the dummy cycles for the read memory instructions with dummy cycles are programmable using the Volatile Configuration Register Address 01h.

Furthermore, the instruction sequence is represented by (C-A-D) or (Cd-Ad-Dd) instruction mode nomenclature format. These nomenclatures are used to indicate the number of active IO pins used for the Command (C), Address (A), Data (D) while DDR is represented by (d).

The writes sequences use the following input protocols:

- Command (C) Input only (1-0-0 in SDR or 8d-0-0 in ODDR)
- Command and Data (C-0-D) Input (1-0-1 in SDR or 8d-0-8d ODDR)
- Command, Address and Data (C-A-D) Input (1-1-1, 1-1-8, 1-8-8 in SDR or 8d-8d-8d in ODDR)

The read sequences use the command, address, dummy cycles and data output protocols (dummy cycle is not included in the instruction nomenclature):

- Command and Data Output (C-D) for register reads (1-0-1 in SDR or 8d-0-8d in ODDR)
- Command, Address, and Data Output (C-A-D) for memory reads (1-1-1, 1-1-8, 1-8-8, 1-1d-8d, 1-8d-8d in SDR or 8d-8d-8d in ODDR); Dummy Cycle is required after address input

Instructions are entered using the high to low transition of the Chip Select (/CS) pin, followed by the command opcode, address input/output, or data input/output if needed. The write instructions are initiated when /CS pin is de-asserted. Writes is instantaneous for register writes while writes involving internal program or erase time requires wait time before new read memory or write instructions are accepted. During the busy internal program or erase operation, only Read Status instruction, Read Status Register will be accepted and the other instructions are going to be ignored until the internal program or erase is completed or suspended and device is ready for the next instruction.

On the other hand as the valid read instructions are shifted in followed by address and dummy cycles if required in the sequence, transition from input to shifting data output either after the command, address or after a combination of command/address with dummy cycles. A low to high transition of the /CS pin during the read sequence brings the device to standby mode and ready to accept valid instructions.

In SDR input mode, the instruction input sequence (C-A-D) are latched in either the single bit IO0 or byte-wide IO[7:0] (depending I/O mode configuration – SPI or Octal SPI) on the rising edge of the clock starting with the most significant bit (MSB) first. Command input sequence will always be in single bit SPI on IO0 using 8 CLKs. All of the instruction set are in single bit SPI mode except for the 1-1-8 / 1-8-8 Read instructions (also the 1-1d-8d and 1-8d-8d DDR reads) and 1-1-8 / 1-8-8 Page Program

instructions that transitions from single bit SPI to Octal SPI either during the address input or data input/output. Address input can be set in 3-byte address mode.

In ODDR mode, the command, address, or data input sequences are latched in the byte-wide IO[7:0] on both rising and falling edges of the clock; the byte-wide data output is also ready on both edges of the clock. The byte command code is required to be latched in on both the rising and falling edge of the clock in ODDR. If a byte data is the size of the data input, it is also required to have the data input byte in the IO[7:0] bus on both the rising and falling edge of clock. ODDR mode is latched in on both rising and falling edges of the clock shifted-in byte increments (requiring 2 clocks).

The complete list of instructions supported by the W35N01JW device is listed on Instruction Set Table. Detailed timing diagrams and implementation for each instruction in both SDR and ODDR mode (if supported) are shown on the Instruction Cycles section.

Clock relative timing diagrams for each instruction are included in Figures 5 through 57. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

7.1 Device ID and Instruction Set Tables

7.1.1 Manufacturer and Device Identification

MANUFACTURER ID	**(MF7 - MF0)**
Winbond Serial Flash	EFh
Device ID	**(ID15 - ID0)**
W35N01JW	DC21h

7.1.2 Instruction Set Table (10), (11)

Instruction	Synchronous Bus Interface			Command Cycle Op code	Address Bytes [2,3]	Dummy Cycle [4]	Data Cycle [5]
	SDR (SPI) (C-A-D) [1]	SDR (OSPI) (C-A-D) [1]	ODDR (Cd-Ad-Dd) [1]				
VCR (Volatile Configulation Register) Address 00h value	FFh	DFh	E7h/C7h				
Software Reset Instructions							
Enable Reset	1-0-0	-	8d-0-0	66h	-	-	-
Reset Device	1-0-0	-	8d-0-0	99h	-	-	-
NAND Reset	1-0-0	-	8d-0-0	FFh	-	-	-
Read ID Instructions							
Read JEDEC ID	1-0-1	-	8d-0-8d	9Fh	-	8	1 to 3
Pre-Write Setup Instructions							
Write Enable	1-0-0	-	8d-0-0	06h	-	-	-
Write Disable	1-0-0	-	8d-0-0	04h	-	-	-
Configuration Instrucitons							
Read Status Register [9]	1-1-1	-	8d-8d-8d	0Fh/05h	8 (1)	- (7)	1 to ∞
Wirte Status Register [9]	1-1-1	-	8d-8d-8d	1Fh/01h	8 (1)	-	1
Volatile Configuration Register Read	1-1-1	-	8d-8d-8d	85h	3	8	1 to ∞
Write Volatile Configuration Register	1-1-1	-	8d-8d-8d	81h	3	-	1
Page Read Instruction							
Page Data Read	1-1-0	-	8d-8d-0	13h	2	-	-
SPI (1-1-1) Read Memory Only Instructions							
Read Data	1-1-1	-	-	03h	2	8	1 to ∞
Program Instructions							
Load Program Data	1-1-1	-	8d-8d-8d	02h	2	-	4224
Random Load Program Data	1-1-1	-	8d-8d-8d	84h	2	-	1 to 4224
8-Data Input Page Data	-	1-1-8	8d-8d-8d	82h	2	-	4224
8-Address-Input Load Program Data	-	1-8-8	8d-8d-8d	C2h	2	-	4224
Random 8-Address-Input Load Program Data	-	1-8-8	8d-8d-8d	C4h	2	-	1 to 4224
Program Execute	1-1-0	-	8d-8d-0	10h	2	-	4224
Erase Memory Instruction							
256KB Block Erase	1-1-0	-	8d-8d-0	D8h	2	-	-
Advanced Features							
Bad Block Management (Swap Blocks)	1-1-0	-	8d-8d-0	A1h	4	-	1 to 10
Read BBM LUT	1-0-1	-	8d-0-8d	A5h	-	8	1 to 10
Last ECC Failure Page Address	1-0-1	-	8d-0-8d	A9h	-	8	2

7.1.3 Instruction Set Table (Changeable dummy cycles by Volatile Configuration Register)

Instruction	Synchronous Bus Interface			Command Cycle Op code	Address Bytes [2,3]	Dummy Cycle [4]	Data Cycle [5]
	SDR (SPI) (C-A-D) [1]	SDR (OSPI) (C-A-D) [1]	ODDR (Cd-Ad-Dd) [1]				
VCR (Volatile Configulation Register) Address 00h value	FFh	DFh	E7h/C7h				
Read Instructions							
Fast Read	1-1-1	-	8d-8d-8d	0Bh	2	8	1 to ∞
Fast Read Octal-Output	-	1-1-8	8d-8d-8d	8Bh	2	8	1 to ∞
Fast Read Octal-I/O	-	1-8-8	8d-8d-8d	CBh	2	16	1 to ∞
DDR Fast Read Octal-Outut	-	1-1d-8d	8d-8d-8d	9Dh	2	8	1 to ∞

Notes:

1. Cd-Ad-Dd format: C stand for Command input; A stand for Address input; D stand for either Data input or Output; d stand for DDR.

2. The x(y) format is used to define the Address Bytes used for SDR and ODDR modes. x which is on the outside of the parenthesis is the number of dummy cycles for the SDR instruction, while y (inside the parenthesis) is for the number of dummy cycles for the ODDR instruction.

3. BUF=0, Continuous Read mode is ignored Address input.

4. The x(y) format is used to define the Dummy Cycles used for SDR and ODDR modes. x which is on the outside of the parenthesis is the number of dummy cycles for the SDR instruction, while y (inside the parenthesis)is for the number of dummy cycles for the ODDR instruction.

5. For all Read operations, Data Cycles in Continuous Read mode is no limitation (∞). Data Cycles in Buffer Read mode is up to page size.

6. Column Address (CA) only requires CA[12:0], CA[15:13] are considered as dummy bits.

7. Page Address (PA) requires 15 bits. PA[14:6] is the address for 256KB blocks (total 512 blocks), PA[5:0] is the address for 4KB pages (total 64 pages for each block).

8. Logical and Physical Block Address (LBA & PBA) each consists of 16 bits. LBA[8:0] & PBA[8:0] are effective Block Addresses. LBA[15:14] is used for additional information.

9. Status Register Addresses:

Status Register 1 / Protection Register:	Addr = Axh
Status Register 2 / Configuration Register:	Addr = Bxh
Status Register 3 / Status Register:	Addr = Cxh

10. All Octal Program/Read commands are disabled when WP-E bit is set to 1 in the Protection Register.

11. For all Read operations in the Continuous Read Mode, once the /CS signal is brought to high to terminate the read operation, the device will still remain busy for tRD3 (BUSY=1), and all the data inside the Data buffer will be lost and un-reliable to use. A new Page Data Read instruction must be issued to reload the correct page data into the Data Buffer.

12. For all Read operations in the Buffer Read Mode, as soon as /CS signal is brought to high to terminate the read operation, the device will be ready to accept new instructions and all the data inside the Data Buffer will remain unchanged from the previous Page Data Read instruction.

7.2 Instruction Descriptions

7.2.1 Device Reset (FFh), Enable Reset (66h) and Reset Device (99h)

Once the Reset instruction is accepted, any on-going internal operations will be terminated and will take approximately tRST to reset. It depending on the current operation the device is performing, tRST can be 5us~500us. During this period, no command will be accepted. After the execution of the Reset instruction is completed, the each bits of Status Register will follow the following table.

If there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device, data corruption may happen at only the address that is the target of the on-going operation. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

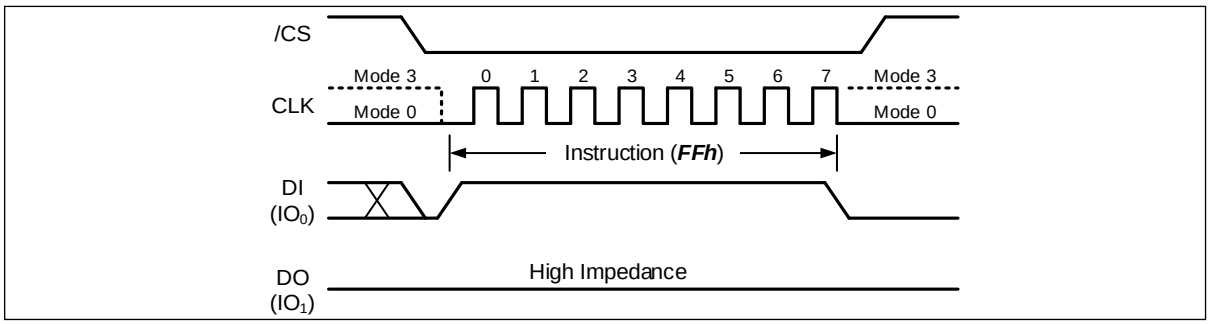


Figure 7-1 Device Reset Instruction (FFh) SDR mode

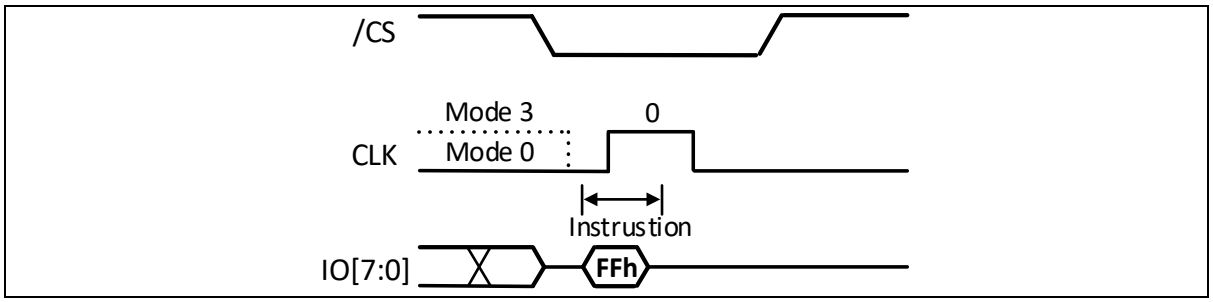


Figure 7-2 Device Reset Instruction (FFh) ODDR mode

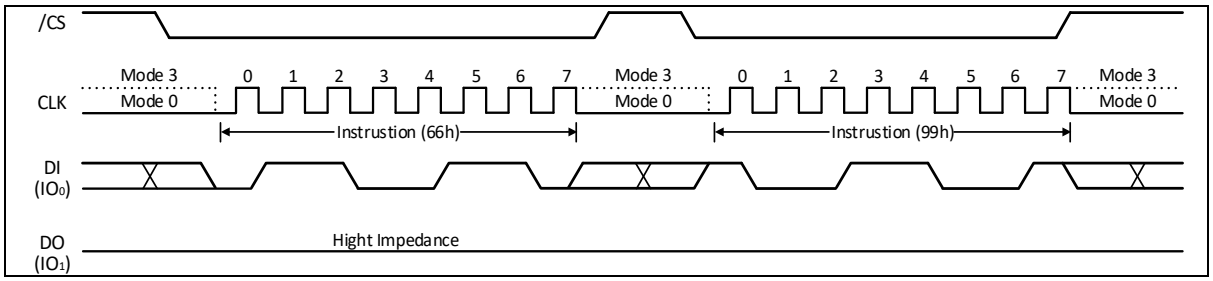


Figure 7-3 Device Reset Instruction (66h+99h) SDR mode

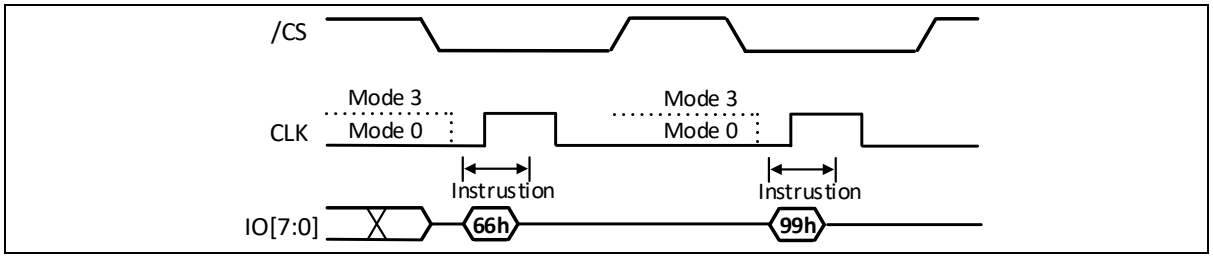


Figure 7-4 Device Reset Instruction (66h+99h) ODDR mode

Register	Address	Bits	Shipment Default	Power Up after LUT is full	Power Up after OTP area locked	Power Up after SR-1 locked	After FFh RESET command	After 66h+99h RESET command or HW RESET
Status Register-1	Axh	BP[3:0],TB	1111, 1	1111, 1	1111, 1	xxxx, x (locked)	No Change	1111, 1
		SRP[1:0]	0 0	0 0	0 0	11 (locked)	No Change	0 0
		WP-E	0	0	0	x (locked)	No Change	0
Status Register-2	Bxh	OTP-L	0	0	1	0	Clear to 0 before OTP set	Clear to 0 before OTP set
		OTP-E	0	0	0	0	0	0
		SR1-L	0	0	0	1	Clear to 0 before OTP set	Clear to 0 before OTP set
		ECC-E	1	1	1	1	No Change	1
		BUF (W35N01JWxxxG)	1	1	1	1	No Change	1
		BUF (W35N01JWxxxT)	0	0	0	0	No Change	0
		HFREQ	0	0	0	0	No Change	0
Status Register-3	Cxh	LUT-F	0	1	0	0	No Change	0 (1)
		ECC-1	0	0	0	0	0	0
		ECC-0	0	0	0	0	0	0
		P-FAIL	0	0	0	0	0	0
		E-FAIL	0	0	0	0	0	0
		WEL	0	0	0	0	0	0
		BUSY	0	0	0	0	0	0
Volatile Configuration Register	05h	-	FFh	FFh	FFh	FFh	No Change	FFh
	03h		FFh	FFh	FFh	FFh	No Change	FFh
	01h		FFh	FFh	FFh	FFh	No Change	FFh
	00h		FFh	FFh	FFh	FFh	No Change	FFh

Default values of the Status Registers after power up and Device Reset

Notes:

1. If LUT is full, the bit indicates to "1" after Reset command (66h+99h) and HW RESET.

	During Power Up sequence	After Reset cmd (FFh)	After Reset cmd (66h+99h) or HW RESET
Auto Page Data Read (13h) (1)	Execute	Execute	Execute

Auto Page Data Read (13h) execution during power up and after Device Reset

Notes:

1. Automatically execution of Page Data Read (13h) command for Block0, Page0.

7.2.2 Read JEDEC ID (9Fh)

The W35N01JW supports a Read JEDEC ID instruction with command code 9Fh to electronically determine the identity of the device. The Read JEDEC ID instruction is backward compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003 with the 3-byte ID output of Manufacturer ID, Memory Type and Memory Density.

In SDR mode, the instruction is initiated by driving the /CS pin low and shifting the command code '9Fh' on IO0 pin. The JEDEC assigned Manufacturer ID byte for Winbond (EFh) and two Device ID bytes, Memory Type and Capacity are shifted out, followed by the Unique ID on IO1 in on the falling edge of CLK with most significant bit (MSB) first in SDR mode. As long as /CS=L and CLK are inputted, 00h is outputted as invalid data after Byte 4 and later. The JEDEC Read ID command is ended by a low to high transition of the /CS pin.

In ODDR mode, Read JEDEC ID (Read ID) sequence is similar to the SDR mode except for the IO configuration used on ODDR mode read sequence. ODDR Read JEDEC ID is entered in the following sequence: driving /CS pin low; command code '9Fh' is shifted on IO[7:0] pin on the rising and falling edge of clock; followed by 8-clock dummy cycles; JEDEC ID data outputs on both edges of the clock. As long as /CS=L and CLK are inputted, 00h is outputted as invalid data after Byte 4 and later. The ODDR JEDEC Read ID operation is ended by low to high transition of /CS pin.

Read JEDEC ID (Read ID) sequence in SDR and ODDR mode is illustrated in Figure 8-5 and 8-6.

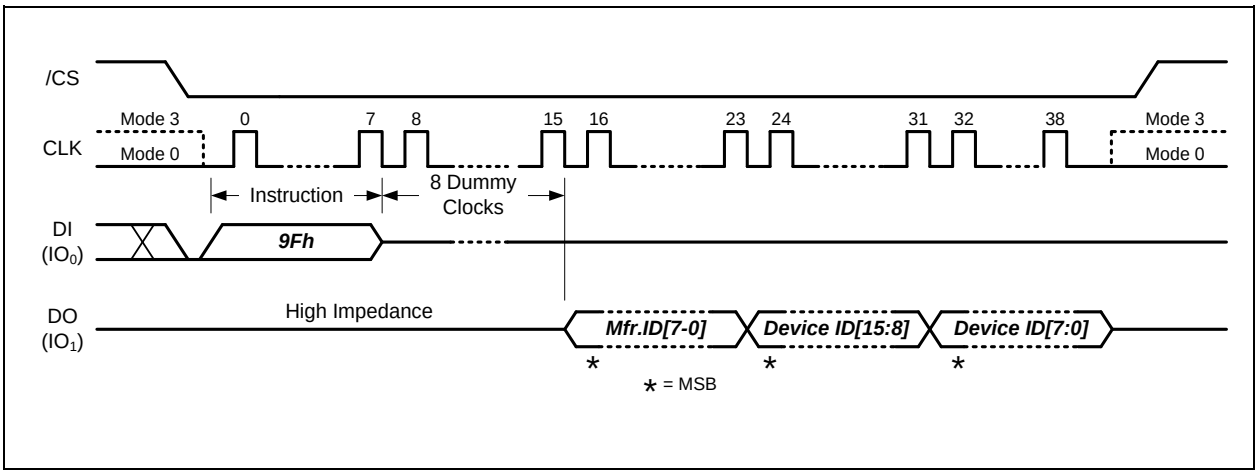


Figure 7-5 Read JEDEC ID Instruction SDR mode

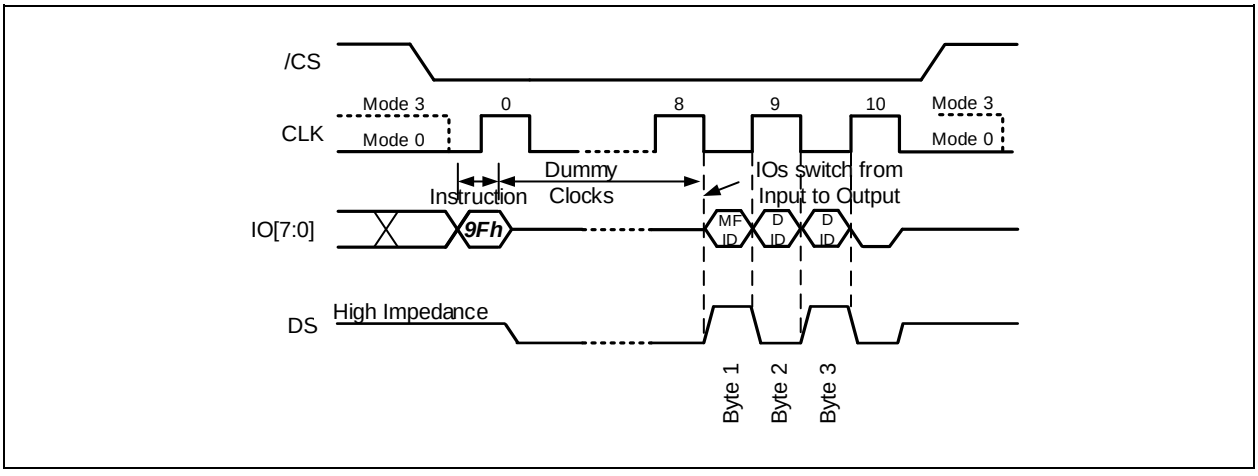


Figure 7-6 Read JEDEC ID Instruction ODDR mode

7.2.3 Read Status Register (0Fh / 05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving /CS pin low. In SDR mode, command code “0Fh” or “05h” for Status Register is shifted into the IO0 pin on the rising edge of CLK. The status register bits are then shifted out on the IO1 pin on the falling edge of CLK with most significant bit (MSB) first as illustrated on Figure 8-6. In DDR mode, command code “0Fh” or “05h” for Read Status Register is shifted into the IO[7:0] pins on both rising and falling edge of CLK. The Status Register bits state are then shifted out on the IO[7:0] pins on every rising and falling edge of CLK after 7- dummy clock cycles illustrated on Figure 8-7. Refer to section 7 for Status Register description.

The Read Status Register instruction may be used at any time, even while an internal program or erase is in progress. The BUSY bit of the Status Register provides the status when an internal program, erase or write operation is ongoing or completed. When the internal write is completed, the device is ready to accept another instruction. The Status Register can be read continuously, as illustrated on Figure 8-7, 8-8. The instruction is completed by driving /CS pin high.

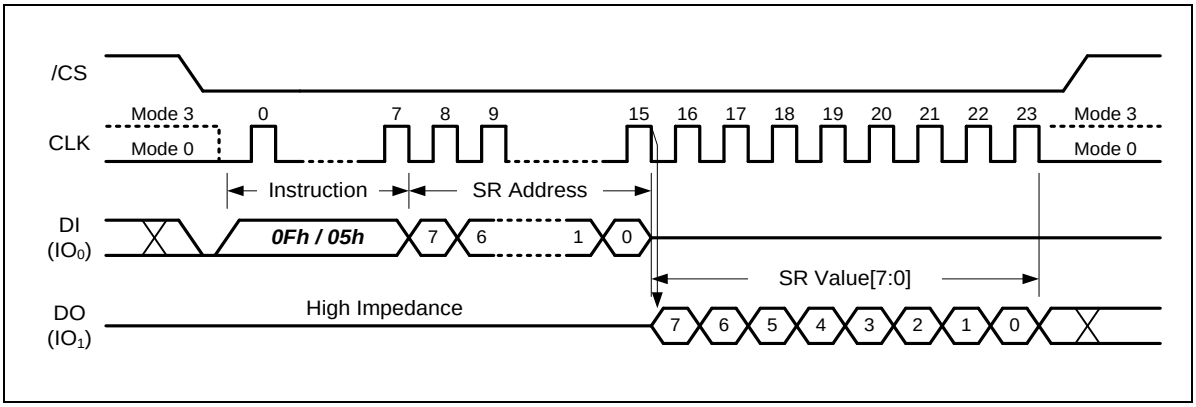


Figure 7-7 Read Status Register Instruction SDR mode

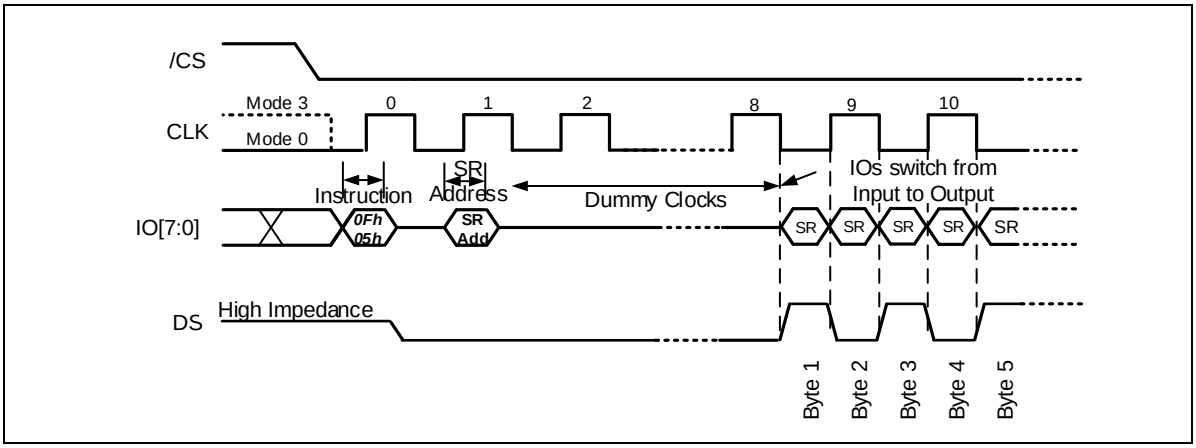


Figure 7-8 Read Status Register Instruction DDR mode

7.2.4 Write Status Register (1Fh / 01h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP[1:0], TB, BP[3:0] and WP-E bit in Status Register-1; OTP-L, OTP-E, SR1-L, ECC-E, BUF and HFREQ bit in Status Register-2. All other Status Register bits locations are read-only and will not be affected by the Write Status Register instruction.

To write the Status Register bits, the instruction is entered by driving /CS low, sending the instruction code “1Fh or 01h”, followed by 8-bits Status Register Address, and then writing the status register data byte. Refer to section 7 for Status Register descriptions. After power up, factory default for BP[3:0], TB, ECC-E bits are 1, while other bits are 0.

In ODDR mode, the Write Status Register sequence is similar to its SDR mode sequence except for the IO configuration and latch in sequence. Write Status Register instruction sequence is entered by driving /CS pin low, followed by the command code ‘1Fh/01h’ into IO[7:0] pins on both the rising and falling edge of CLK and by data byte value (setting) to be written to the Status Register into the IO[7:0] pins also on both the rising and falling edge of CLK. Write Status Register instruction is executed when /CS pin is driven high as illustrated on Figure 8-10.

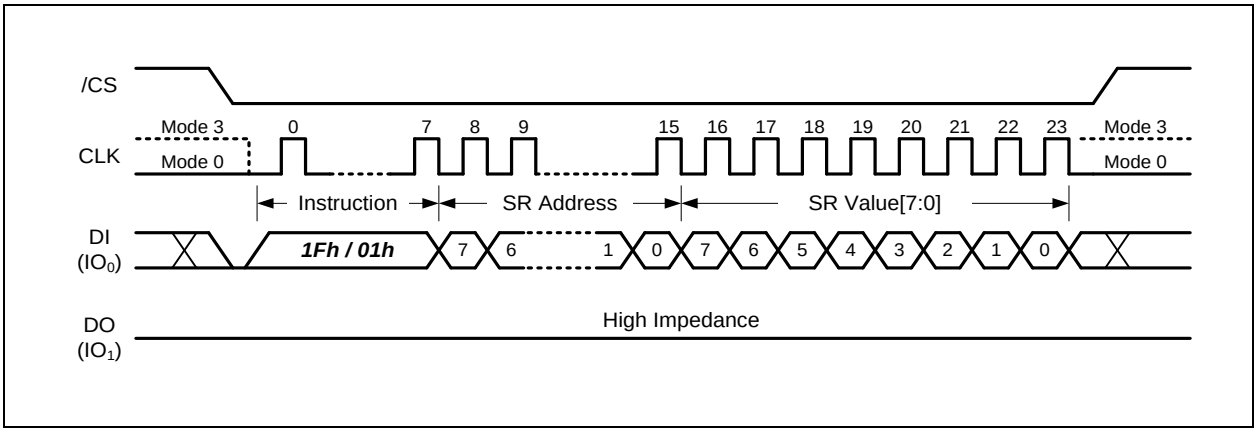


Figure 7-9 Write Status Register-1/2/3 Instruction SDR mode

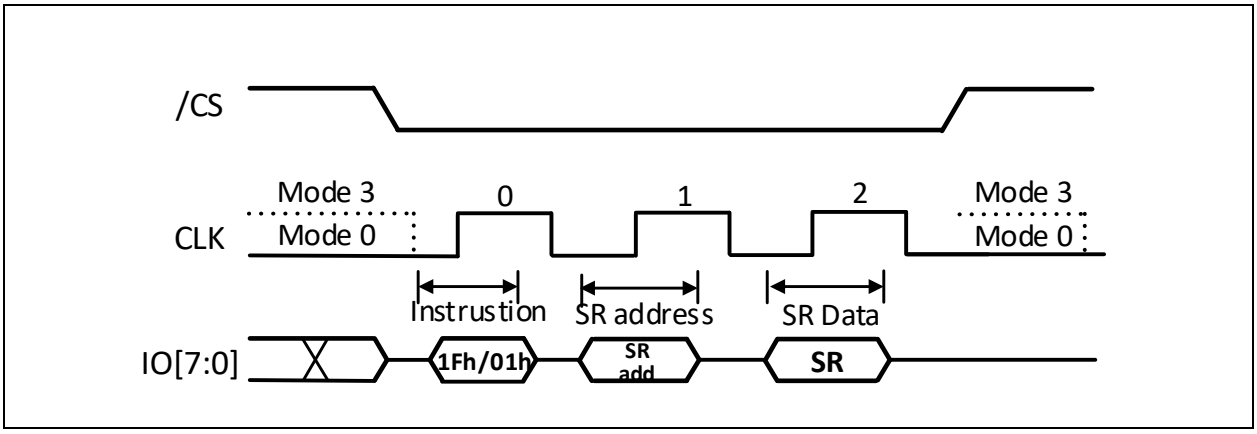


Figure 7-10 Write Status Register-1/2/3 Instruction ODDR mode

7.2.5 Read Volatile Configuration Register (85h)

The Read Volatile Configuration Register (Read-VCR) reads the 256-byte Volatile Configuration Register (VCR) used to configure or change device operational settings (IO Mode Configuration, Dummy Clock Cycle for memory read) after power up. The read data size is only one byte from the target address input sequence and the same data byte will output continuously. The Read-VCR is supported in either SDR or ODDR mode.

In SDR mode, the Read-VCR instruction sequence is initiated by the following sequence: Drive /CS pin low; shift-in Read-VCR command code “85h” into the IO0 pin on the rising edge of CLK; followed by shifting into IO0 pin on rising edge of CLK either the 24-bit address input and required 8-dummy CLK cycles input; and VCR data output value will start shifting out on IO1 pin on the falling edge of CLK with most significant bit (MSB) first from the target address as illustrated on Figure 8-10.

In ODDR mode, the Read-VCR instruction sequence is initiated by the following sequence: Drive /CS pin low; shift-in Read VCR command code “85h” into the IO[7:0] pins on both the rising and falling edge of CLK; followed by the 32-bit Address input also on both the rising and falling edge of CLK; an 8-dummy CLK cycles input; and VCR data output value will start shifting out on IO[7:0] pins on both the falling and rising edge of CLK from the target address as illustrated on Figure 8-11.

The Read VCR will shift-out the same data byte output continuously as illustrated on Figure 8-11. The instruction is completed by driving /CS pin high.

Refer to section 7 for Volatile Configuration Register description.

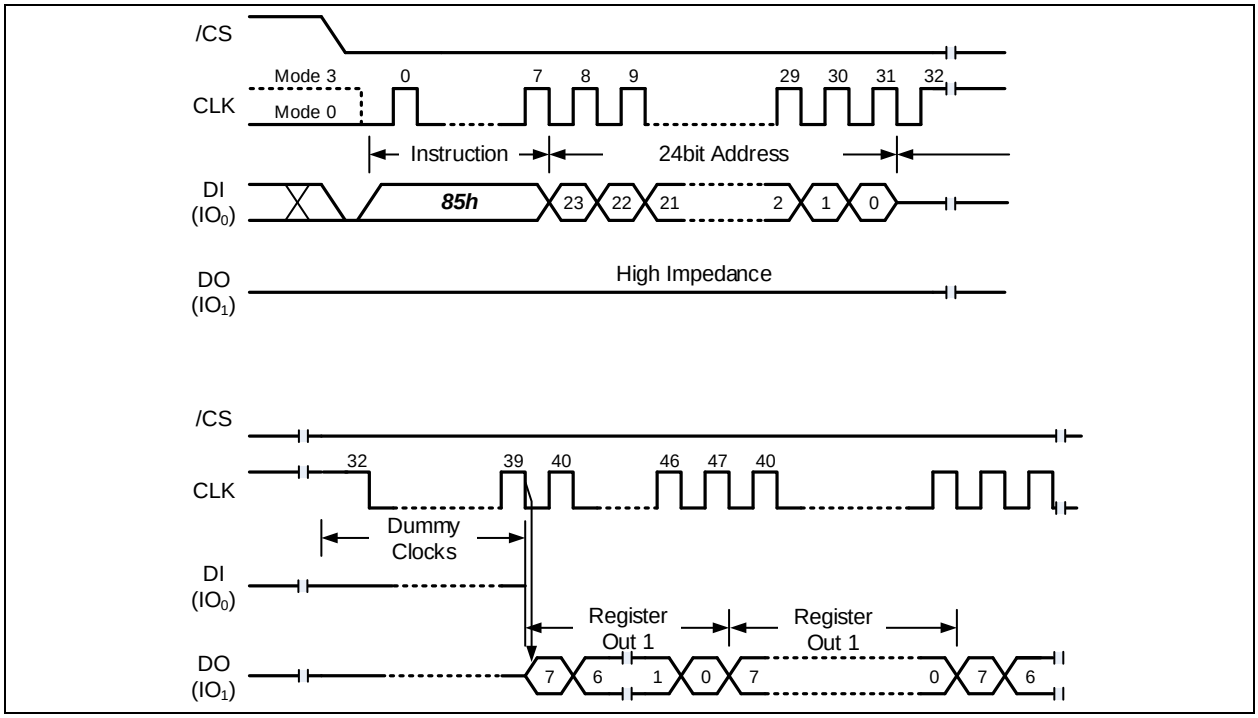


Figure 7-11 Read Volatile Configuration Register Instruction SDR mode

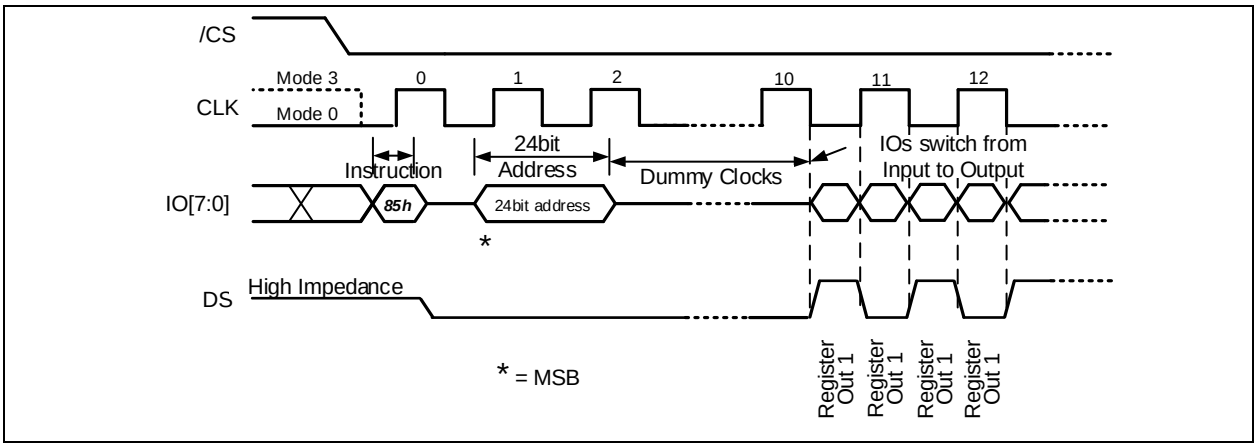


Figure 7-12 Read Volatile Configuration Register Instruction ODDR mode

7.2.6 Write Volatile Configuration Register (81h)

The Write Volatile Configuration Register (Write-VCR) instruction individually writes a byte data on a targeted address within the 256-byte Volatile Configuration Register. The writable Volatile Configuration Register addresses are as follows: Address 00h (IO mode), 01h (Dummy Clock Cycle Configuration), 03h (Output Driver Strength Configuration) and 05h (Address Mode Configuration Beyond 128Mb). Addresses 02h, 04h and [06h:FFh] are Reserved (FFh value) and these address locations are not writable. To write on the Volatile Configuration Register, a standard Write Enable (06h) instruction must be first executed for the device to accept the Write-VCR instruction (Status Register WEL bit must equal '1').

In SDR mode and once device is write enabled (WEL bit = 1) the instruction is entered by the following sequence: drive /CS pin low; shift-in on IO0 using the rising edge of CLK the command code '81h', 24-bit address and data byte setting sequence; and subsequently drive /CS pin high to execute the Write Volatile Configuration Register instruction as illustrated on 8-12.

In ODDR mode, the Write-VCR sequence is similar the Write-VCR SDR mode sequence except for the IO configurations and latch in sequence. ODDR Write-VCR instruction sequence is entered by the following sequence: drive /CS pin low; shift-in command code '81h' on IO[7:0] using both rising and falling edge of CLK; continue to shift-in 32-bit address on IO[7:0] pins using both rising and falling edge of CLK; followed by shifting-in byte data setting using both rising and falling edge of CLK; and subsequently drive /CS pin high to execute Write Volatile Configuration Register instruction.

The Write Volatile Configuration Register instruction is a write to a volatile register address location. A minimum tSHSL2 time of 50ns (see AC Characteristics) is needed to complete the write. After the Write Volatile Configuration Register cycle is completed, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

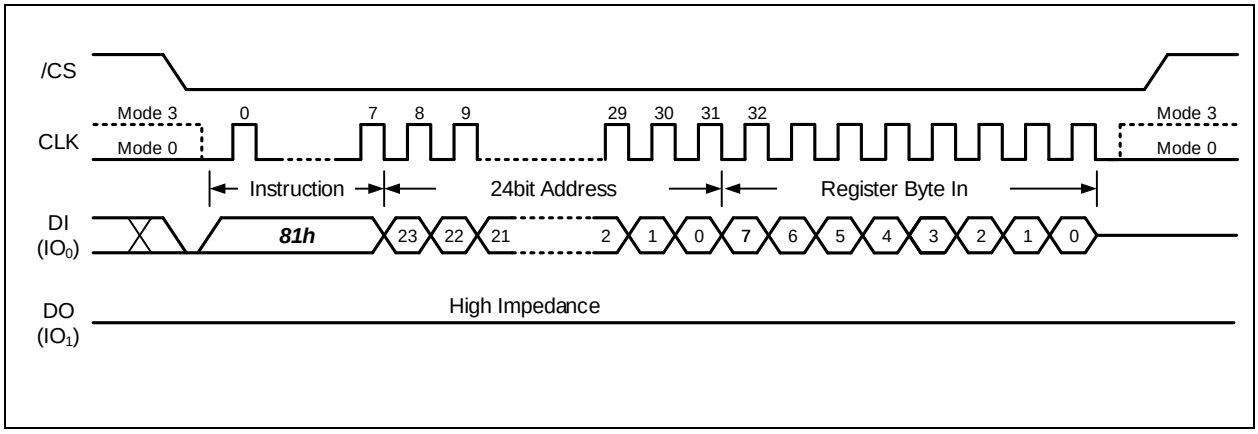


Figure 7-13 Write Volatile Configuration Register Instruction SDR mode

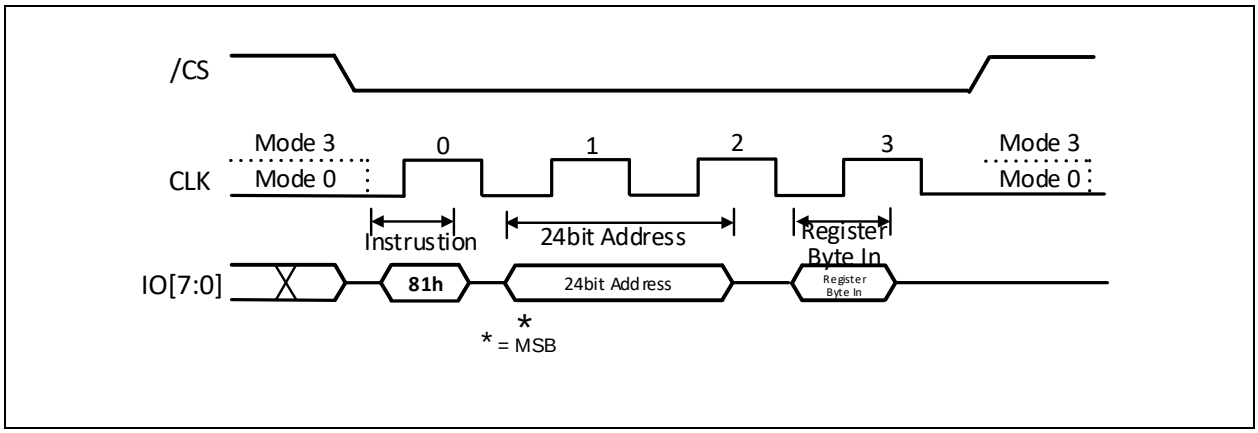


Figure 7-14 Write Volatile Configuration Register Instruction ODDR mode

7.3 Pre-Write Setup Instructions

The Write Enable Latch (WEL) bit of the Status Register is a bit indicator if the device is write enabled or disabled. If the WEL bit is '0', it is write disabled and will not accept program, erase or write to register instructions. If the WEL bit is set to '1', it is write enabled and device will acknowledge program, erase, or write to register instructions. After program, erase or write to register completion, WEL bit is automatically reset to '0'. Write Enable and Write Disable instructions directly sets and clears the WEL bit. Both instructions are supported in SDR and ODDR mode.

7.3.1 Write Enable (06h)

The Write Enable instruction sets the Write Enable Latch (WEL) bit in the Status Register to '1'. The WEL bit must be set prior to Page Program, Block Erase and Bad Block management instruction. In SDR mode, the Write Enable instruction is entered by driving /CS pin low, shifting the command code "06h" into the IO0 pin on the rising edge of CLK, and subsequently driving /CS pin high executes the instruction. In ODDR mode, the Write Enable instruction is entered by driving /CS low, shifting the command code '06h' into IO[7:0] pins on both the rising and falling edge of CLK, and subsequently driving /CS pin high executes the instruction. Figure 8-13 and 8-14 illustrates Write Enable instruction in SDR and ODDR mode.

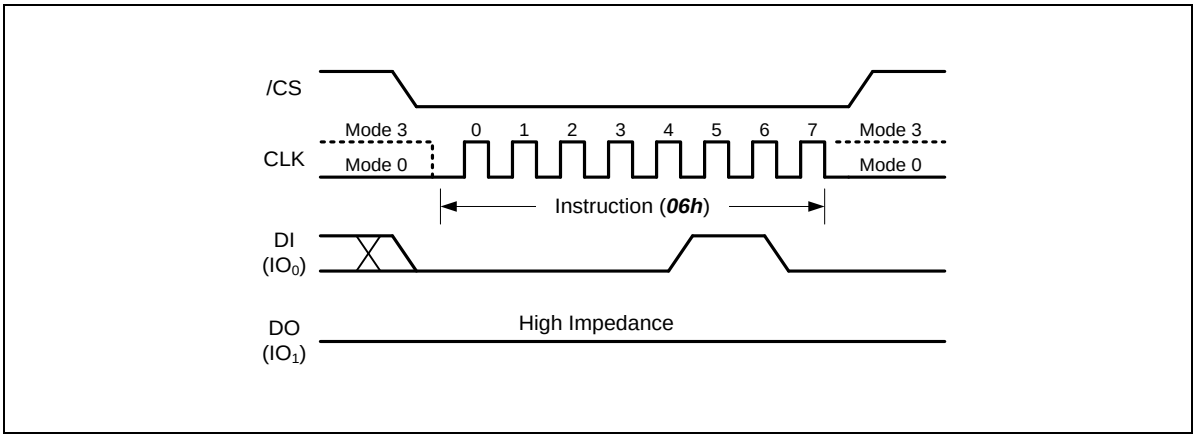


Figure 7-15 Write Enable Instruction SDR mode

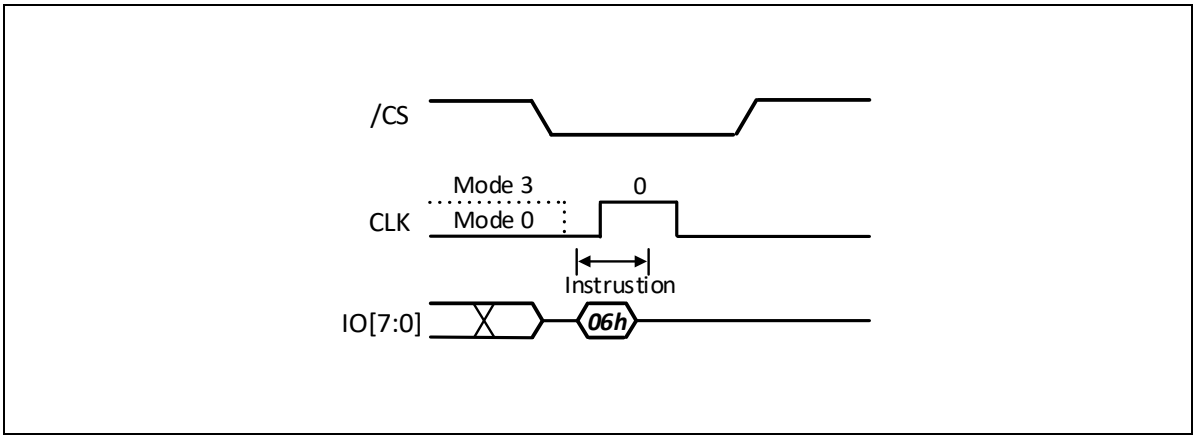


Figure 7-16 Write Enable Instruction ODDR mode

7.3.2 Write Disable (04h)

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to '0'. In SDR mode, the Write Disable instruction is entered by driving /CS pin low, shifting the command code '04h' into the IO0 pin, and subsequently driving /CS pin high to execute the instruction. In ODDR mode, the Write Disable instruction is entered by driving /CS low, shifting code '04h' into the IO[7:0] pins on both the rising and falling edge of CLK, and subsequently driving /CS pin high to execute the instruction. Figure 8-15 and 8-16 illustrates the Write Disable instruction sequence in SDR and ODDR mode.
The WEL bit is automatically reset after Power-up, Hardware or Software Reset sequence, and upon completion of internal program, erase, and write to register instructions. Hardware and Software Reset sequence will also reset this bit to '0'.

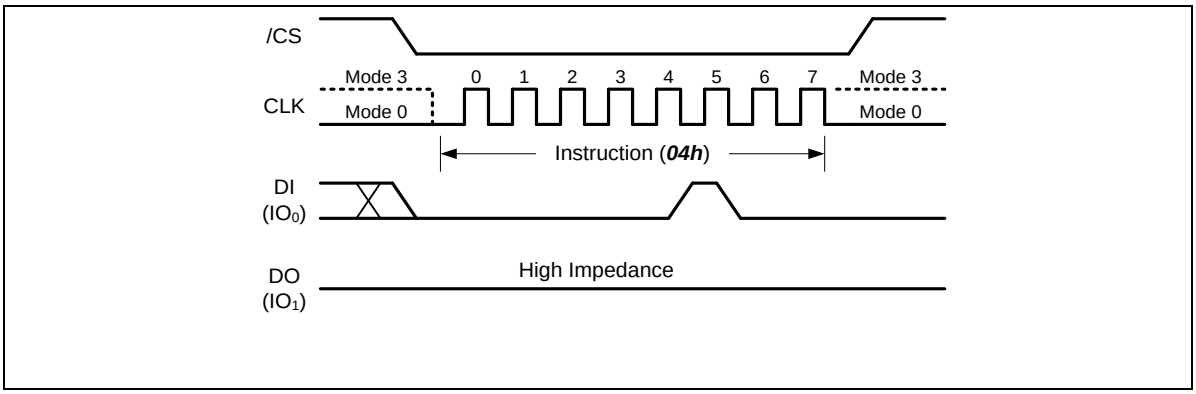


Figure 7-17 Write Disable Instruction SDR mode

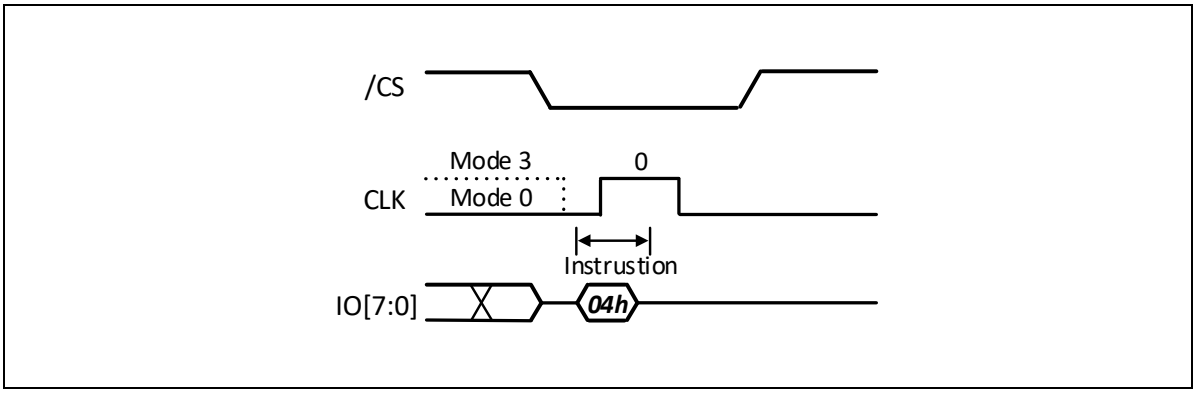


Figure 7-18 Write Disable Instruction ODDR mode

7.4 Block Management Instructions

Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of “Bad Blocks” found in the factory testing. Up to 2% of the memory blocks can be marked as “Bad Blocks” upon shipment, which is a maximum of 10 blocks for W35N01JW. In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A “Bad Block Marker” is a non-FFh data byte stored at Byte 0 of Page 0 for each bad block. An additional marker is also stored in the first two bytes of the 128-Byte spare area.

7.4.1 Bad Block Management (A1h)

W35N01JW offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The “Bad Block Management” command is initiated by shifting the instruction code “A1h” into the DI pin and followed by the 16-bits “Logical Block Address” and 16-bits “Physical Block Address”. The logical block address is the address for the “bad” block that will be replaced by the “good” block indicated by the physical block address.

Once a Bad Block Management command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 10 links can be established in the non-volatile LUT. If all 10 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management command, the LUT-F bit value can be checked or a “Read BBM Look Up Table” command can be issued to confirm if spare links are still available in the LUT.
To guarantee a continuous read operation on the first 500 blocks, the manufacturer may have used some of the BBM LUT entrees. It is advisable for the user to scan all blocks and keep a table of all manufacturer bad blocks prior to first erase/program operation.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

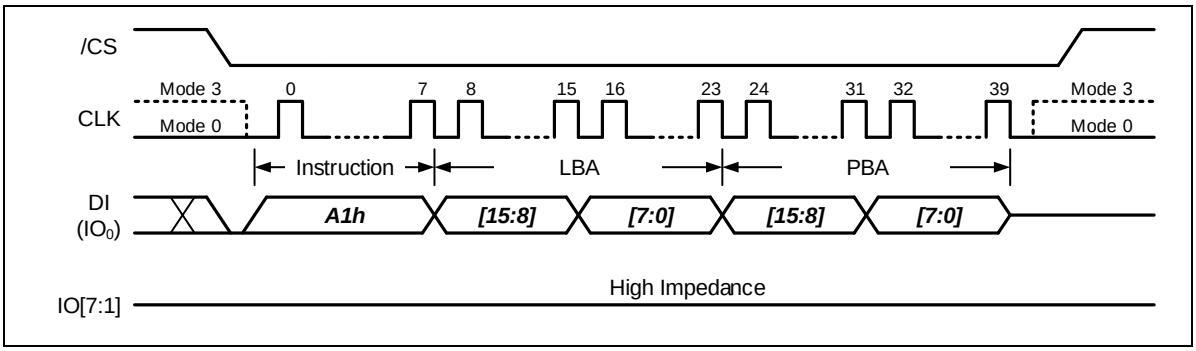


Figure 7-19 Bad Block Management Instruction SDR mode

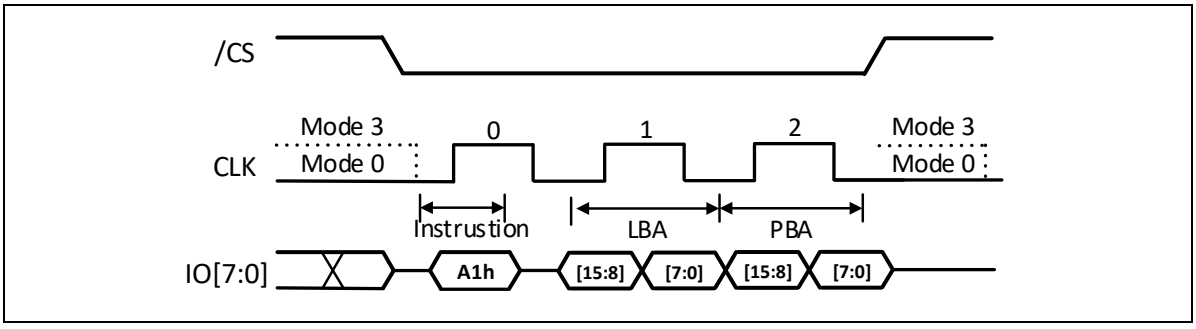


Figure 7-20 Bad Block Management Instruction ODDR mode

7.4.2 Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 10 Logical-Physical memory block links (from LBA0/PBA0 to LBA9/PBA9). The “Read BBM Look Up Table” command can be used to check the existing address links stored inside the LUT.

The “Read BBM Look Up Table” command is initiated by shifting the instruction code “A5h” into the DI pin and followed by 8-bits dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bits “Logical Block Address” and the 16-bits “Physical Block Address” as illustrated in Figure 8-19 and Figure 8-20. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all “00h” data.

The MSB bits LBA[15:14] of each link are used to indicate the status of the link.

LBA[15] (Enable)	LBA[14] (Invalid)	Descriptions
0	0	This link is available to use.
1	0	This link is enabled and it is a valid link.
1	1	This link was enabled, but it is not valid any more.
0	1	Not applicable.

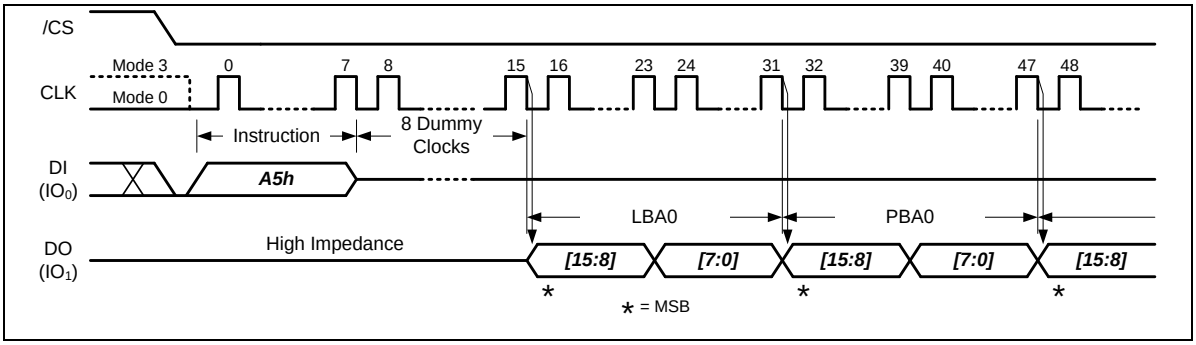


Figure 7-21 Read BBM Look Up Table Instruction SDR mode

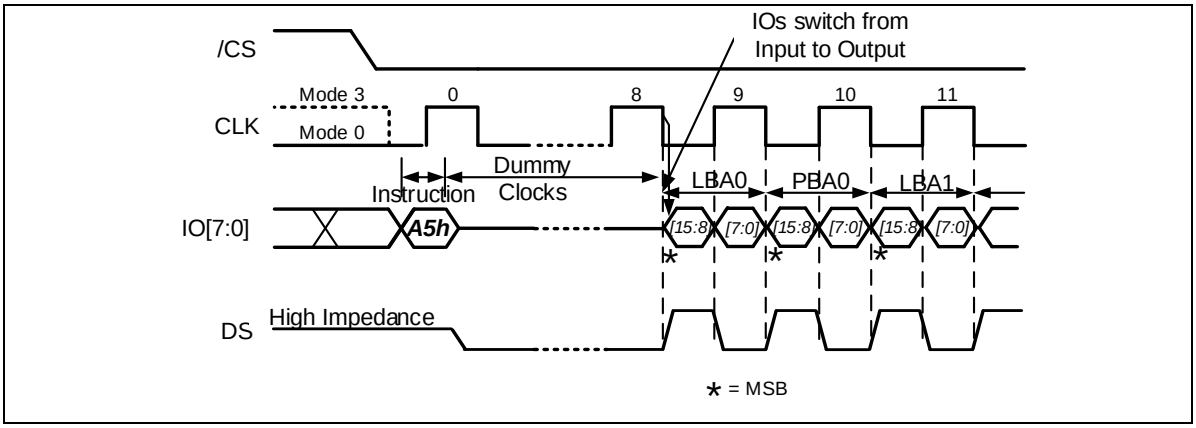


Figure 7-22 Read BBM Look Up Table Instruction ODDR mode

7.4.3 Last ECC Failure Page Address (A9h)

To better manage the data integrity, W35N01JW implements internal ECC correction for the entire memory array. When the ECC-E bit in the Status/Configuration Register is set to 1 (also power up default), the internal ECC algorithm is enabled for all Program and Read operations. During a “Program Execute” command for a specific page, the ECC algorithm will calculate the ECC information based on the data inside the 4K-Byte data buffer and write the ECC data into the extra 128-Byte ECC area in the same physical memory page.

During the Read operations, ECC information will be used to verify the data read out from the physical memory array and possible corrections can be made to limited amount of data bits that contain errors. The ECC Status Bits (ECC-1 & ECC-0) will also be set indicating the result of ECC calculation.

For the “Continuous Read Mode (BUF=0)” operation, multiple pages of main array data can be read out continuously by issuing a single read command. Upon finishing the read operation, the ECC status bits should be check to verify if there’s any ECC correction or un-correctable errors existed in the read out data. If ECC-1 & ECC-0 equal to (1, 0) or (1, 1), the previous read out data contain one or more pages that contain ECC un-correctable errors.

The failure page address (or the last page address if it’s multiple pages) can be obtained by issuing the “Last ECC failure Page Address” command. The 15-bits Page Address that contains un-correctable ECC errors will be presented on the DO pin following the instruction code “A9h” and 8-bits dummy clocks on the DI pin.

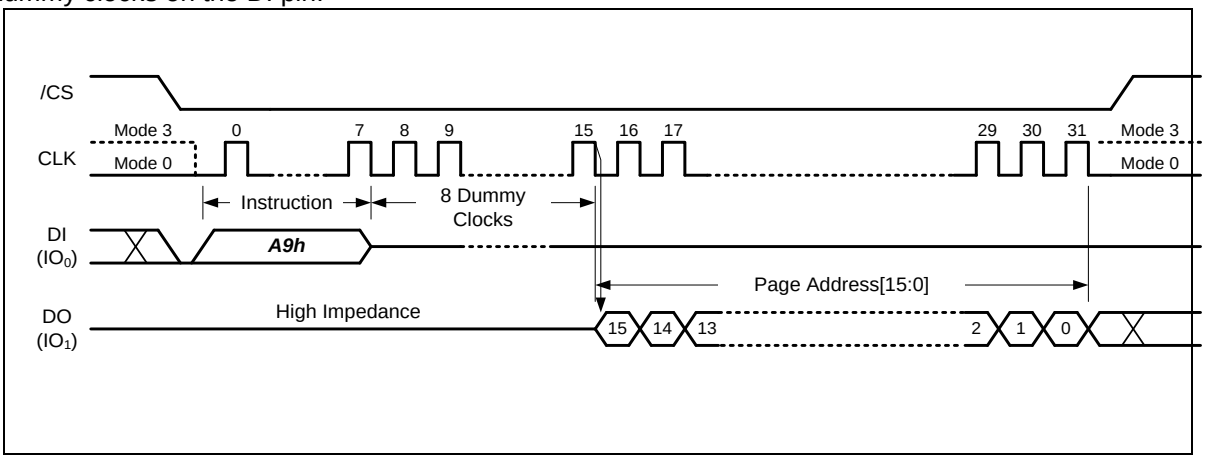


Figure 7-23 Last ECC Failure Page Address Instruction SDR mode

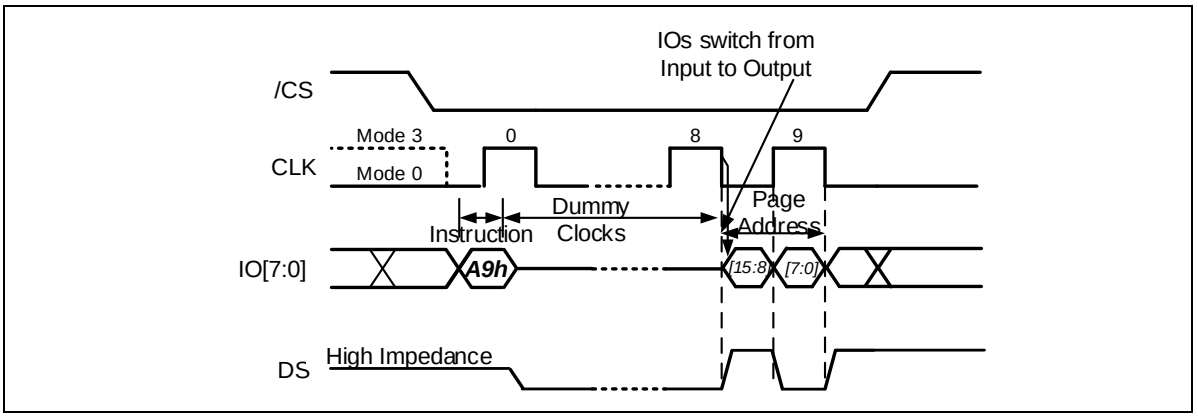


Figure 7-24 Last ECC Failure Page Address Instruction ODDR mode

7.5 Erase and Program Operations

7.5.1 256KB Block Erase (D8h)

The 256KB Block Erase instruction sets all memory within a specified block (64-Pages, 256K-Bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed by 8-bits dummy clocks and the 16-bits page address. The Block Erase instruction sequence is shown in below.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed block is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

In ODDR mode, either 256KB Block Erase command codes D8h are supported. In ODDR 256KB Block Erase sequence, command code is shifted-in on IO[7:0] pins on both the rising and falling edge of CLK. Address Mode Configuration in ODDR mode used only 24-bit Address (3-Byte Address Mode) input, initial input is ignored as dummy cycles. Address and Data also use IO[7:0] pins on both rising and falling edge of CLK to latch in data.

Once device is write enabled (WEL bit =1), the ODDR 256KB Block Erase instruction is initiated by the following sequence: drive the /CS pin low; shift-in the command code “D8h” on IO7:0 pins using both rising and falling edge of CLK; continue to shift-in 24-bit block address on IO[7:0] pins using both rising and falling edge of CLK; and subsequently drive /CS pin high to initiate the internal block erase cycle.

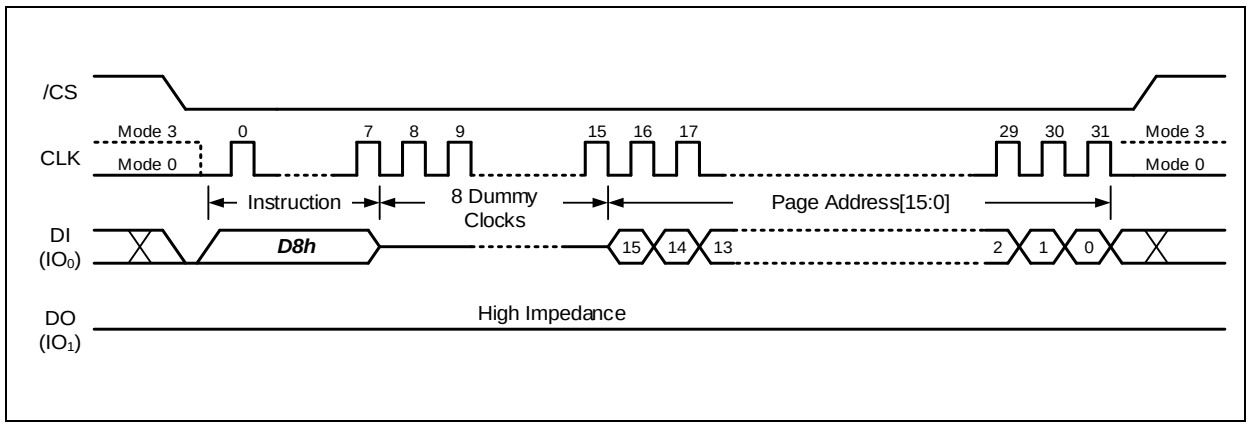


Figure 7-25 256KB Block Erase Instruction SDR mode

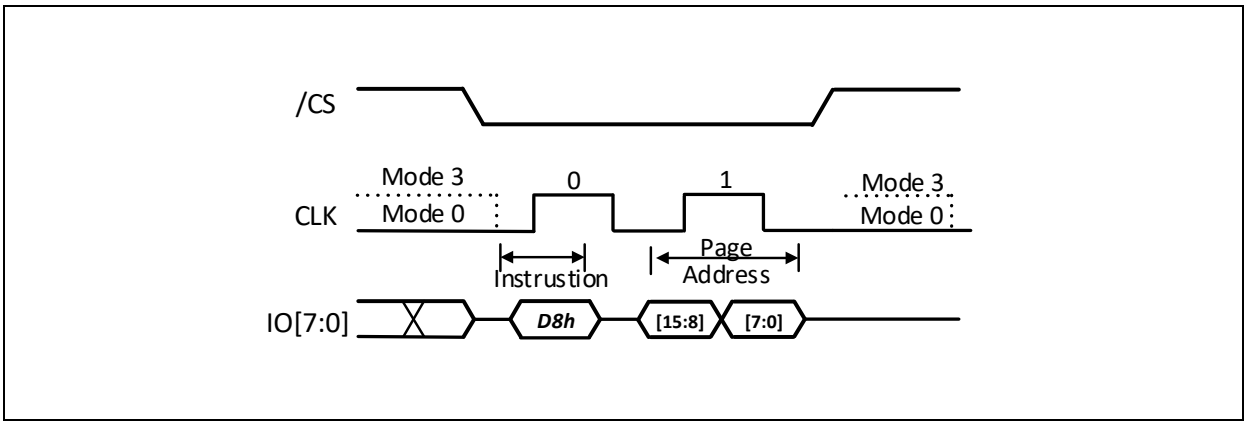


Figure 7-26 256KB Block Erase Instruction ODDDR mode

7.5.2 Load Program Data (02h) / Random Load Program Data (84h)

The Program operation allows from one byte to 4,224 bytes (a page) of data to be programmed at previously erased (FFh) memory locations.

A Program operation involves two steps:

1. Load the program data into the Data Buffer.
2. Issue “Program Execute” command to transfer the data from Data Buffer to the specified memory page.

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL=1). The “Load Program Data” or “Random Load Program Data” instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” or “84h” followed by a 16-bits column address (only CA[12:0] is effective). The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device. The Load Program Data instruction sequence is shown in below.

Both “Load Program Data” and “Random Load Program Data” instructions share the same command sequence. The difference is that “Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

If internal ECC algorithm is enabled, all 4,224 bytes of data will be accepted, but the bytes designated for ECC parity bits in the extra 128 bytes section will be overwritten by the ECC calculation. If the ECC-E bit is set to a 0 to disable the internal ECC, the extra 128 bytes section can be used for external ECC purpose or other usage.

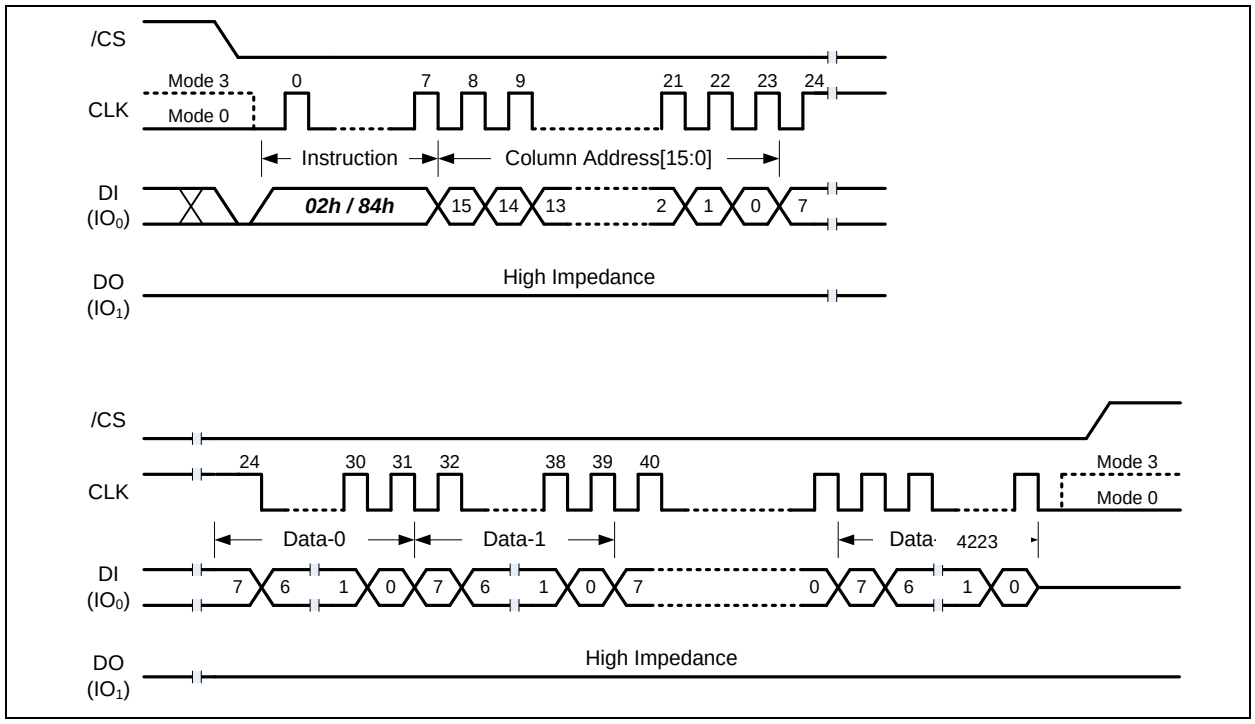


Figure 7-27 Load / Random Load Program Data Instruction

7.5.3 Octal Data-Input Load Page Data (82h)

The Octal Data-Input Page Program instruction allows up to 4,224 bytes of data to be programmed at previously erased (FFh) memory locations using IO0 pin during command/address input sequence and transitioning to IO[7:0] pins during the data input step in SDR mode.

Once device is write enabled (WEL bit =1), the instruction is initiated by the following sequence: drive the /CS pin low; shift-in the command code “82h” followed by a 16-bit on IO0 pin and on rising edge of CLK; transition to IO[7:0] and shift-in 1 to 4,224 bytes of data on rising edge of CLK; and subsequently drive /CS pin high to initiate the internal program cycle. In Octal Data-input load page data mode, 16-bits column address input after instruction code must be set to multiple address of four (x0h, x4h, x8h, xCh). The data size in this mode must be inputted minimum 4-Byte, and a multiple of 4-Byte.

The Octal Data-Input Page Program instruction sequence is illustrated on Figure 8-28.

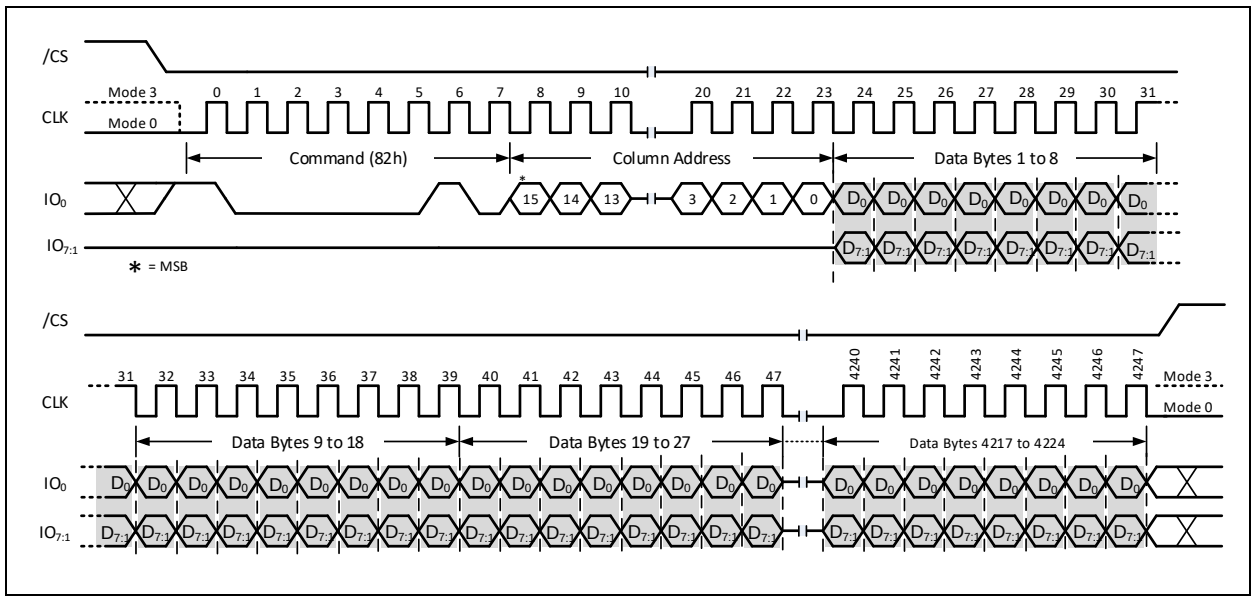


Figure 7-28 Octal Input Page Program Instruction SDR mode only

7.5.4 Octal Address-Input Load Program Data (C2h) / Random Octal Address-Input Load Program Data (C4h)

The Octal Address-Input Page Program instruction allows up to 4224 bytes of data to be programmed at previously erased (FFh) memory locations using IO0 pin during command code input sequence and transitioning to IO[7:0] pins during the address and data input phase in SDR mode.
Once device is write enabled (WEL bit =1), the instruction is initiated by the following sequence: drive the /CS pin low; shift-in the command code “C2h” on IO0 pin and on rising edge of CLK; transition to IO[7:0] when shifting in address/data input on rising edge of CLK, where address input is 16-bit and data input is 1 to 4224 bytes of data; and subsequently drive /CS pin high to initiate the internal program cycle. In Octal Address input load program data (C2h) and Random Octal Address input load program data (C4h) mode, 16-bits column address input after instruction code must be set to multiple address of four (x0h, x4h, x8h, xCh). The data size in these mode must be inputted minimum 4-Byte.The Octal Address-Input Page Program instruction sequence is illustrated on Figure 8-29.

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL=1). The “Octal Address-Input Load Program Data” or “Random Load Program Data” instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” or “84h” followed by a 16-bits column address (only CA[12:0] is effective). The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of

data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device. The Load Program Data instruction sequence is shown in below.

Both “Load Program Data” and “Random Load Program Data” instructions share the same command sequence. The difference is that “Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

If internal ECC algorithm is enabled, all 4,224 bytes of data will be accepted, but the bytes designated for ECC parity bits in the extra 128 bytes section will be overwritten by the ECC calculation. If the ECC-E bit is set to a 0 to disable the internal ECC, the extra 128 bytes section can be used for external ECC purpose or other usage.

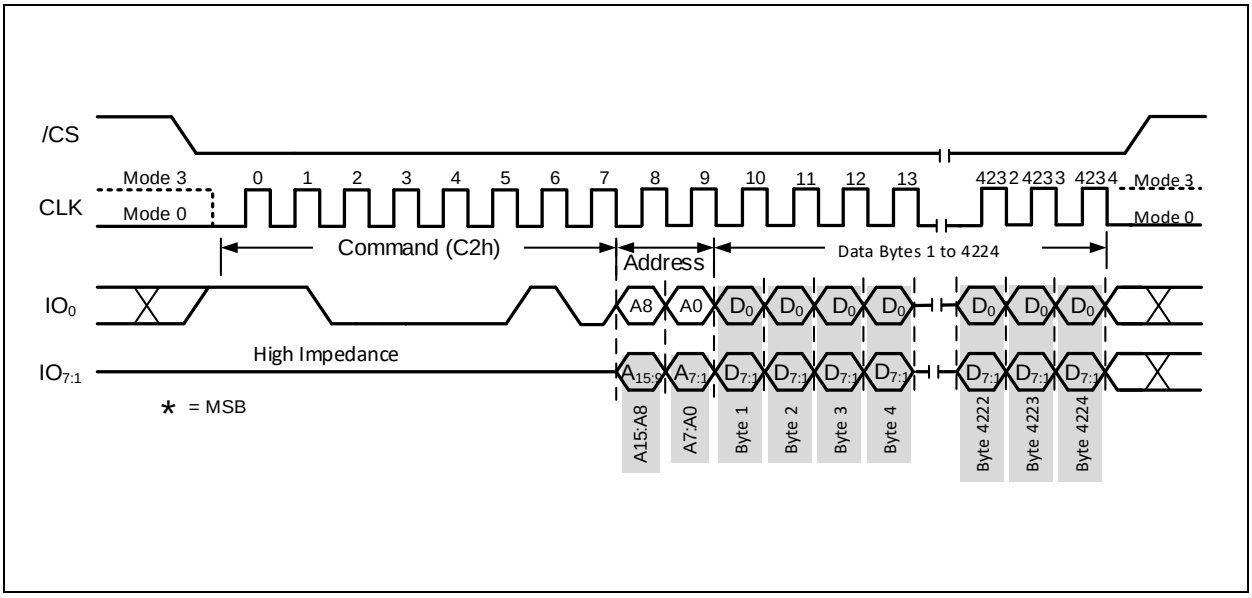


Figure 7-29 Octal Input Page Program Instruction SDR mode only

7.5.5 Octal DDR Instruction, Address and Data Input

When volatile configuration register (VCR) address 00h set to E7 or C7, the device mode changes from SDR to ODDR mode, and supports program data instructions of 02h, 84h, 82h, C2h and C4h. In ODDR program mode, 16-bits column address input after instruction code must be set to multiple address of four (x0h, x4h, x8h, xCh). The data size in this mode must be inputted minimum 4-Byte, and a multiple of 4-Byte.

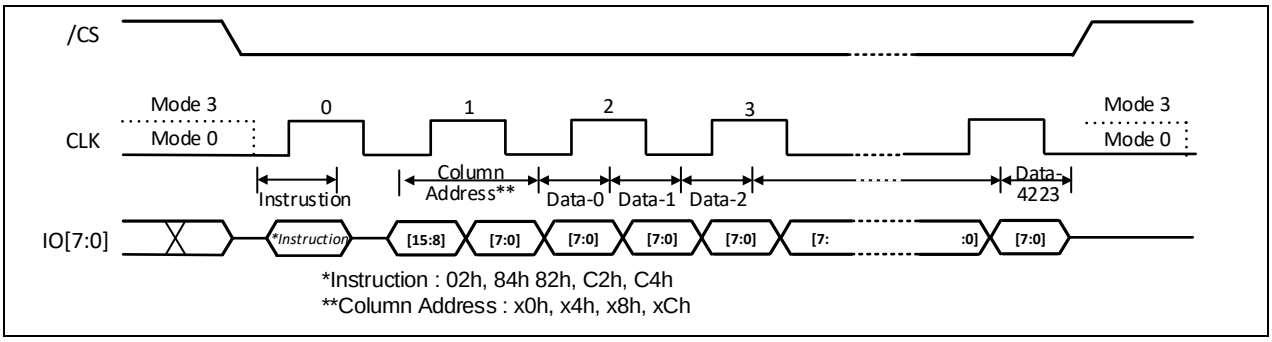


Figure 7-30 Octal DDR Page Program Instruction SDR

7.5.6 Program Execute (10h)

The Program Execute instruction is the second step of the Program operation. After the program data are loaded into the 4,224-Byte Data Buffer (or 4,096 bytes when ECC is enabled), the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the /CS pin low then shifting the instruction code “10h” followed by 8-bits dummy clocks and the 16-bits Page Address into the DI pin.

After /CS is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for a time duration of tPP (See AC Characteristics). While the Program Execute cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits.

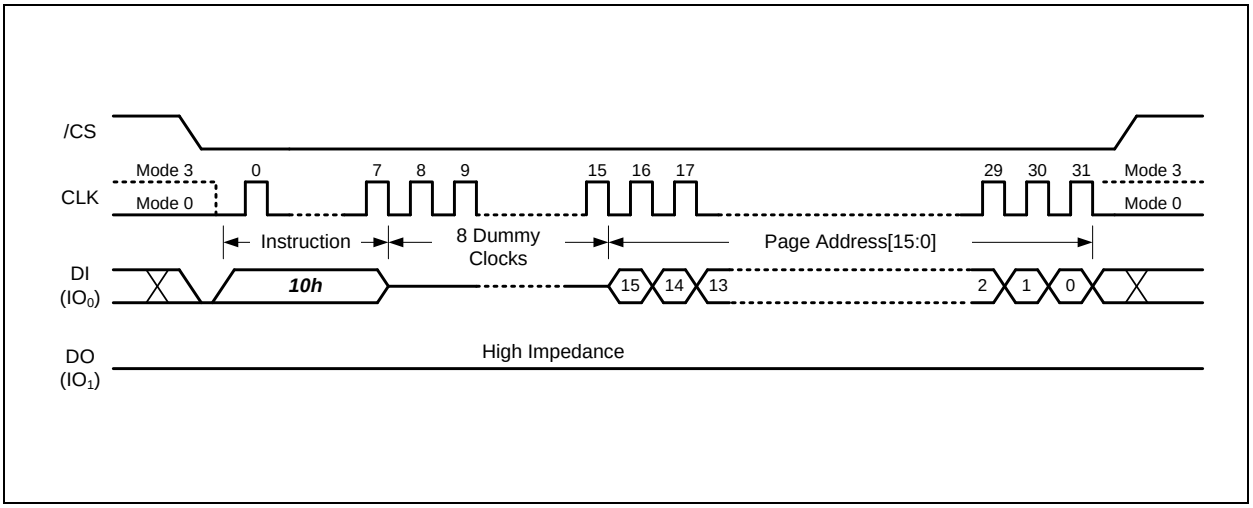


Figure 7-31 Program Execute Instruction SDR mode

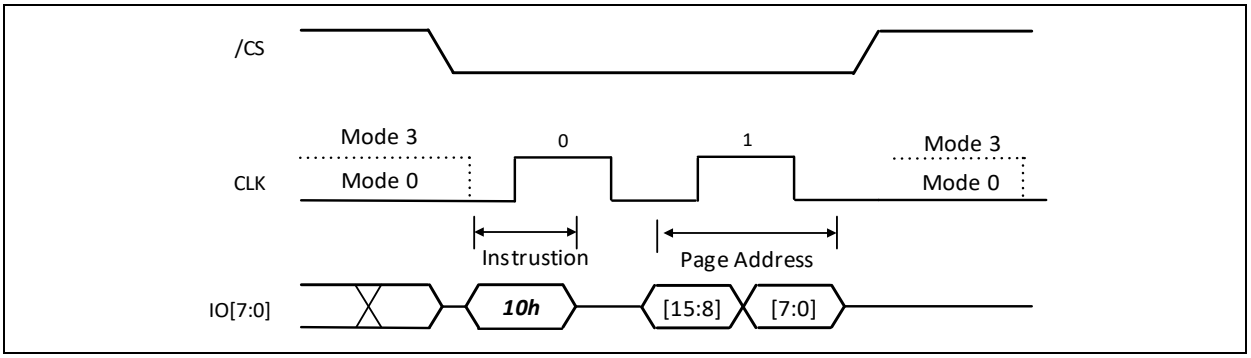


Figure 7-32 Program Execute Instruction ODDR mode

7.6 Read Operations

7.6.1 Page Data Read (13h)

The Page Data Read instruction will transfer the data of the specified memory page into the 4,224-Byte Data Buffer. The instruction is initiated by driving the /CS pin low then shifting the instruction code “13h” followed by 8-bits dummy clocks and the 16-bits Page Address into the DI pin.

After /CS is driven high to complete the instruction cycle, the self-timed Read Page Data instruction will commence for a time duration of tRD1 or tRD2 (See AC Characteristics). While the Read Page Data cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Read Page Data cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the 4,224 bytes of page data are loaded into the Data Buffer, several Read instructions can be issued to access the Data Buffer and read out the data. Depending on the BUF bit setting in the Status Register, either “Buffer Read Mode” or “Continuous Read Mode” may be used to accomplish the read operations. After the page data read operation has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

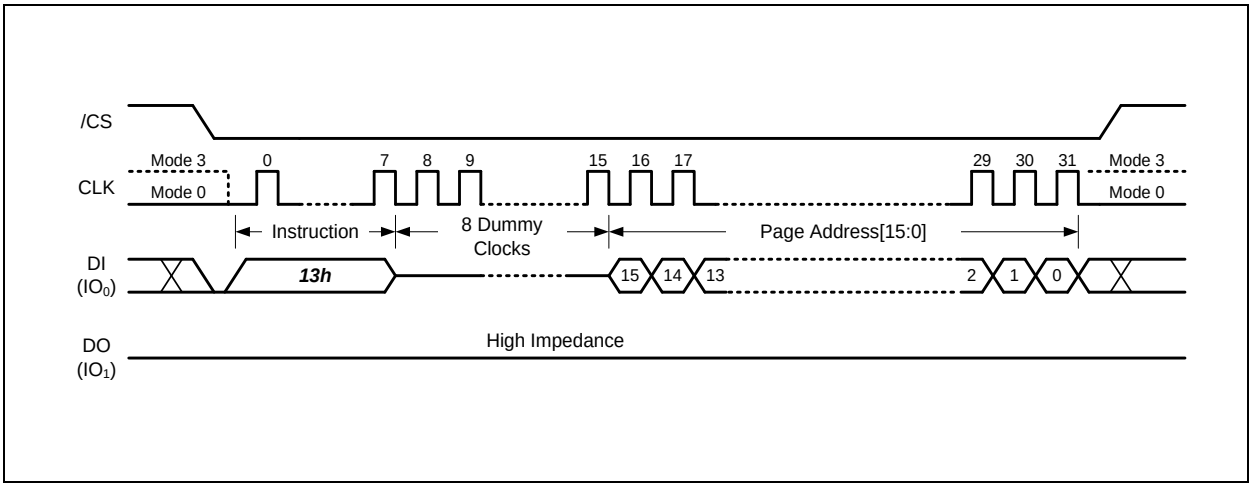


Figure 7-33 Page Data Read Instruction SDR mode

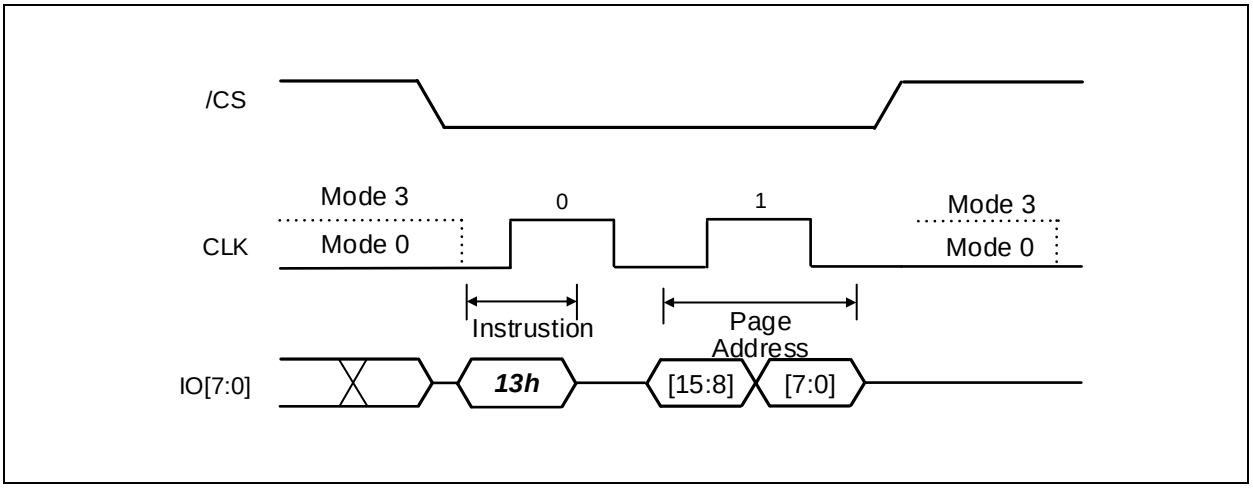


Figure 7-34 Page Data Read Instruction ODDR mode

7.6.2 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read Data instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by the 16-bits Column Address and 8-bits dummy clocks or a 24-bits dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array.

The Read Data (03h) instruction is only supported in SDR mode.

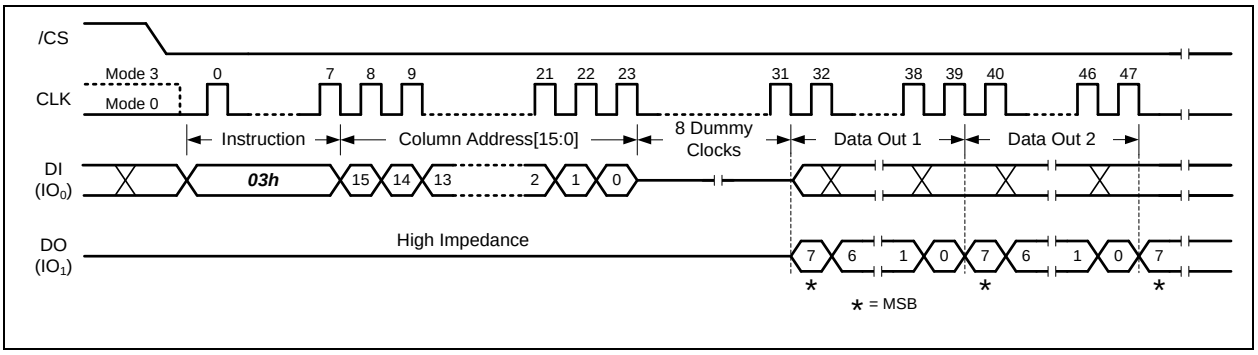


Figure 7-35 Read Data Instruction (Buffer Read Mode, BUF=1)

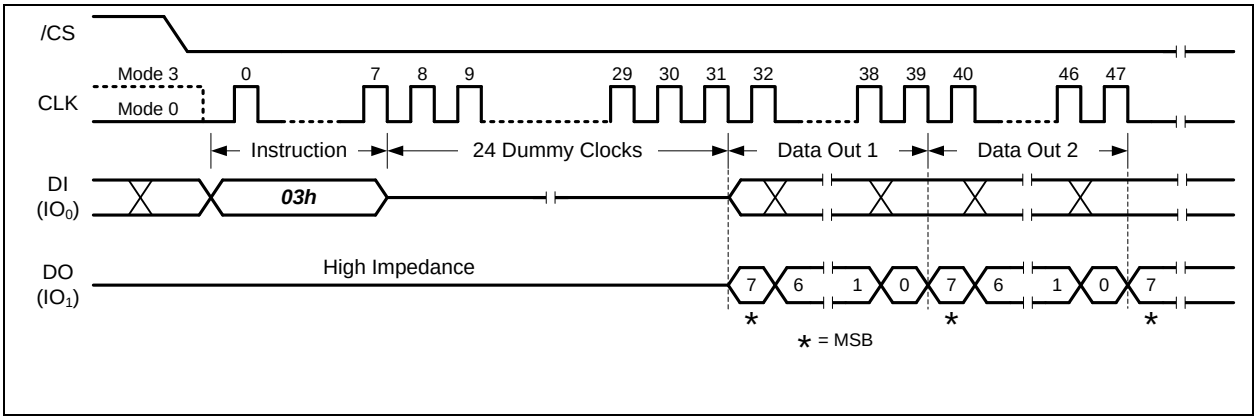


Figure 7-36 Read Data Instruction (Continuous Read Mode, BUF=0)

7.6.3 Fast Read (0Bh)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “0Bh” followed by the 16-bits Column Address into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array.

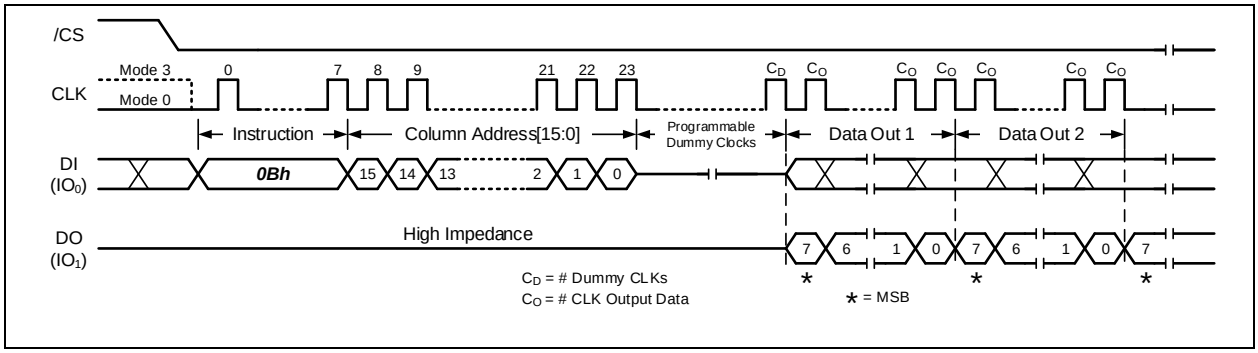


Figure 7-37 Fast Read Instruction SDR mode (Buffer Read Mode, BUF=1)

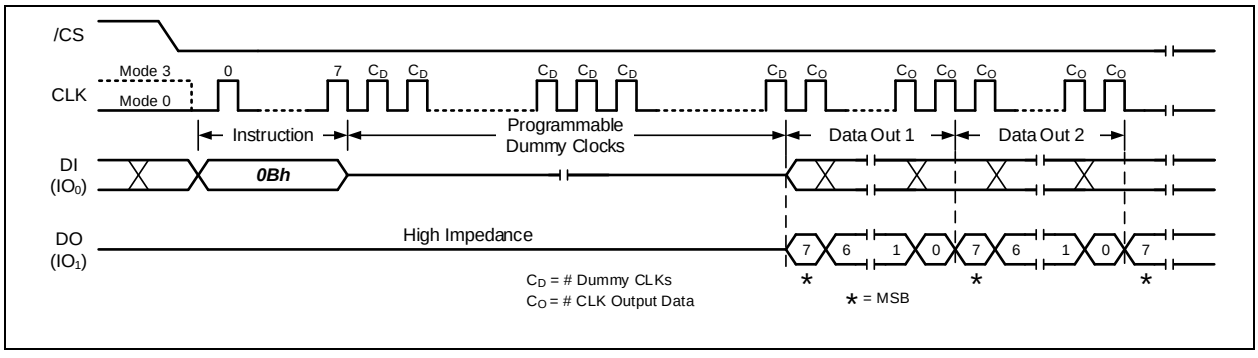


Figure 7-38 Fast Read Instruction SDR mode (Continuous Read Mode, BUF=0)

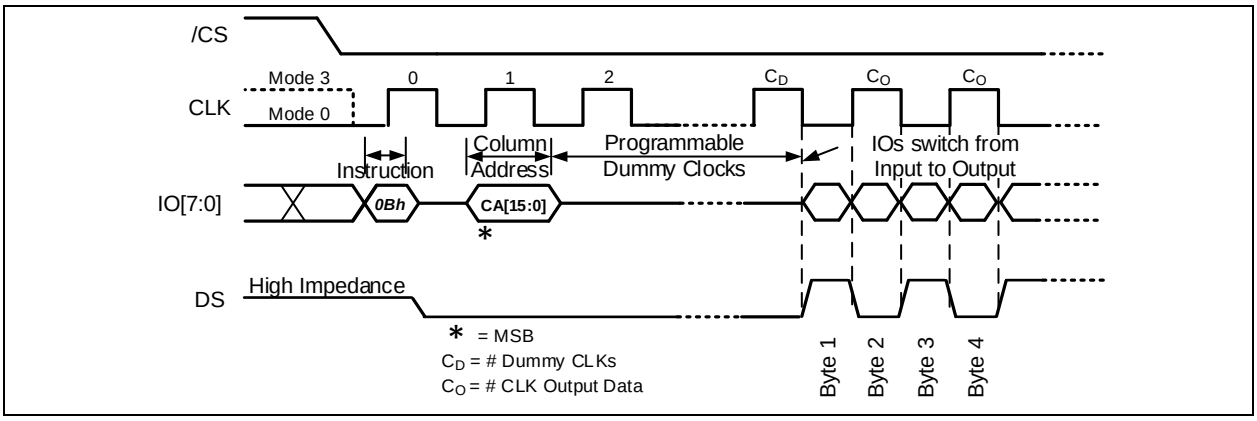


Figure 7-39 Fast Read Instruction ODDR mode (Buffer Read Mode, BUF=1)

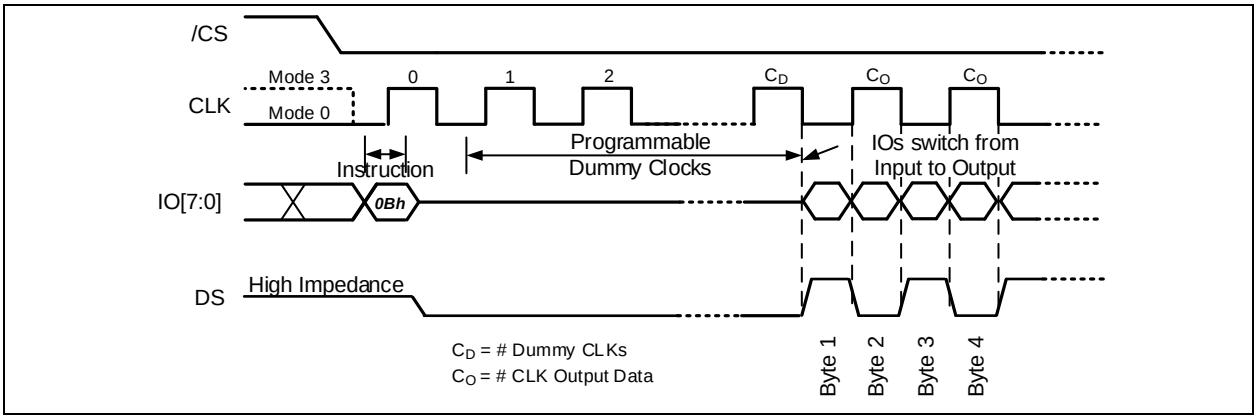


Figure 7-40 Fast Read Instruction ODDR mode (Continuous Read Mode, BUF=0)

7.6.4 Fast Read Octal Output (8Bh)

The Fast Read Octal Output instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on eight pins; IO_0 and IO_7. This allows data to be transferred at eighth the rate of standard SPI devices.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array.

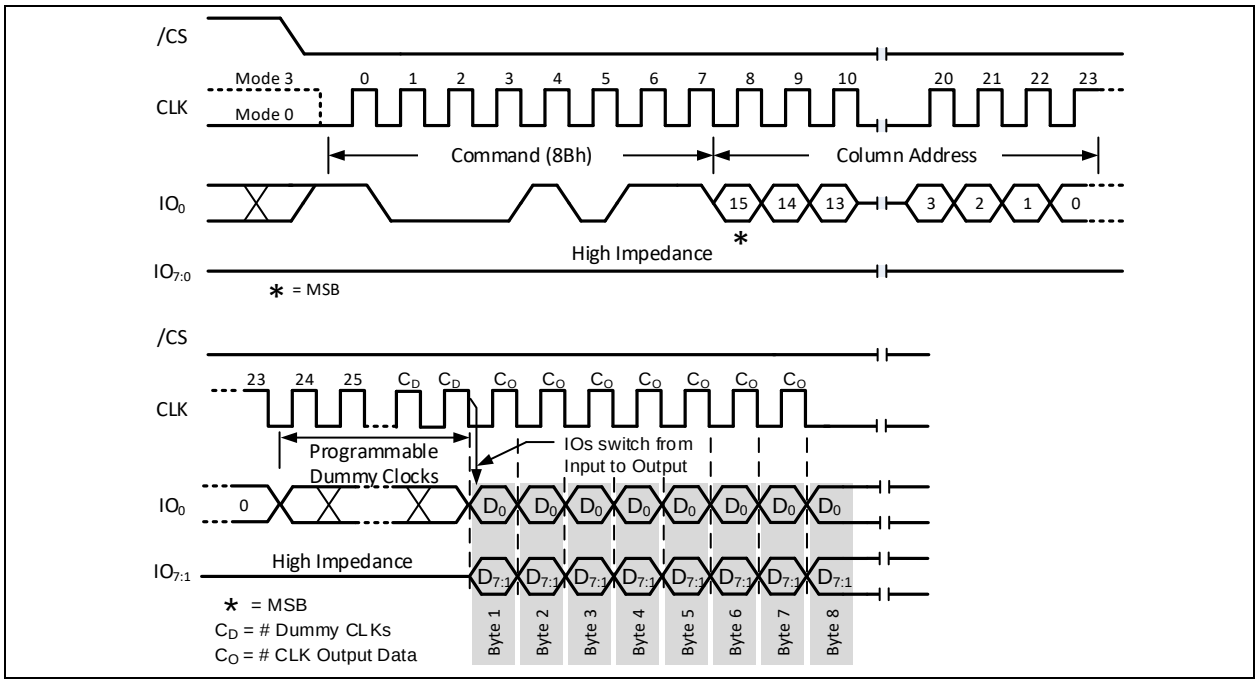


Figure 7-41 Fast Read Octal Output Instruction SDR mode (Buffer Read Mode, BUF=1)

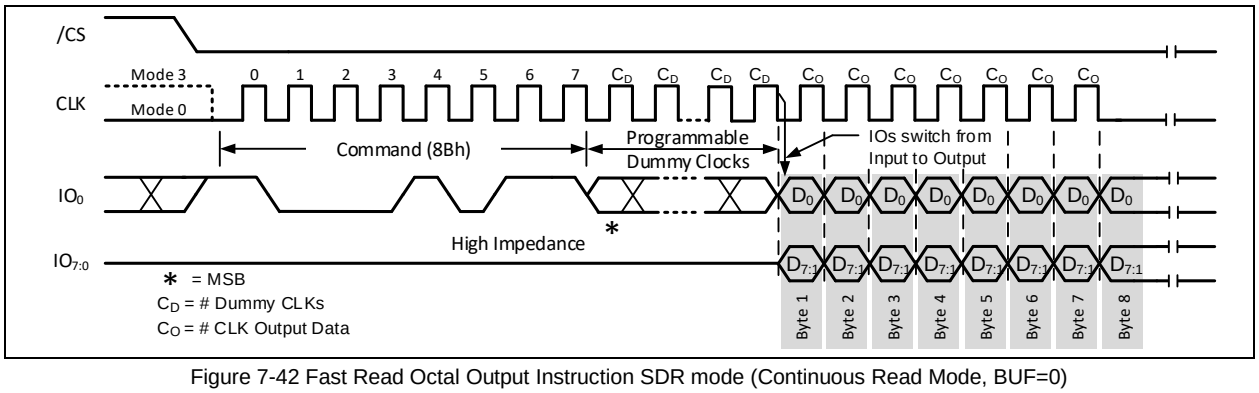


Figure 7-42 Fast Read Octal Output Instruction SDR mode (Continuous Read Mode, BUF=0)

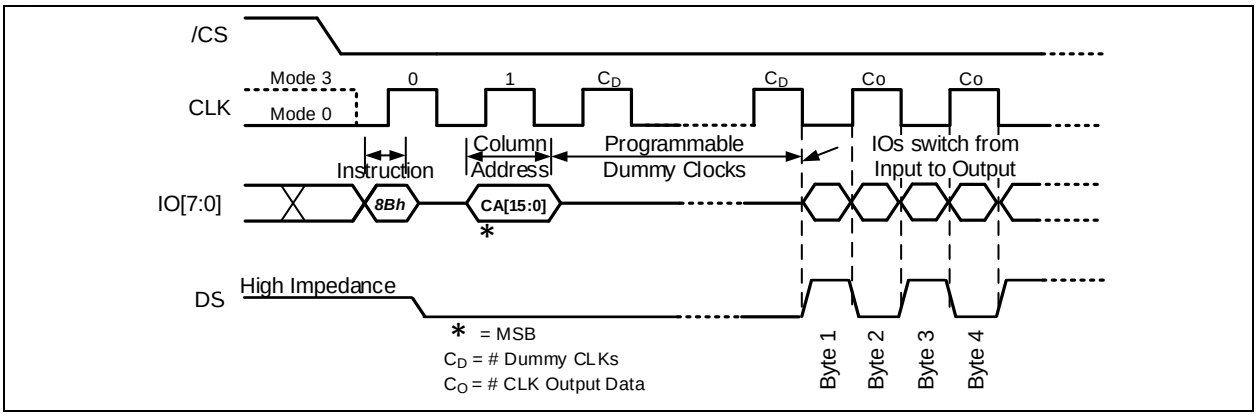


Figure 7-43 Fast Read Octal Output Instruction ODDR mode (Buffer Read Mode, BUF=1)

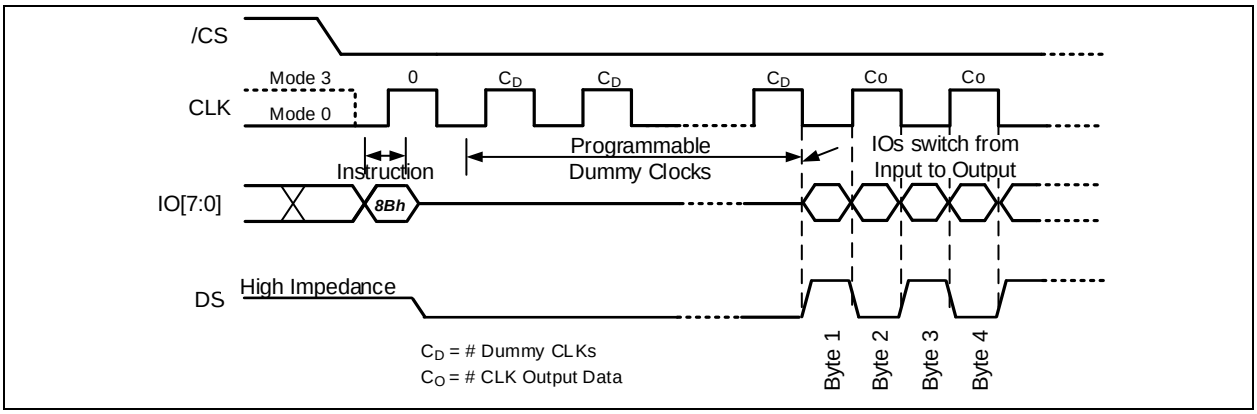


Figure 7-44 Fast Read Octal Output Instruction ODDR mode (Continuous Read Mode, BUF=0)

7.6.5 Fast Read Octal I/O (CBh)

The Fast Read Octal I/O instruction is similar to the SDR read instructions command code input with single bit SPI and transition to eight IO[7:0] pins during the address input, dummy cycles, and data output.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

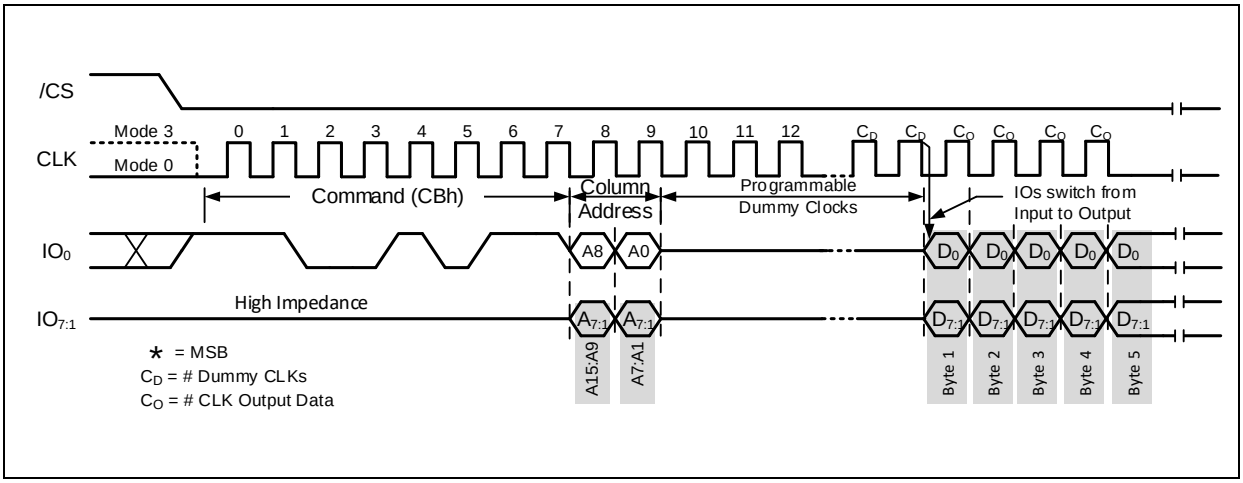


Figure 7-45 Fast Read Octal I/O Instruction SDR mode (Buffer Read Mode, BUF=1)

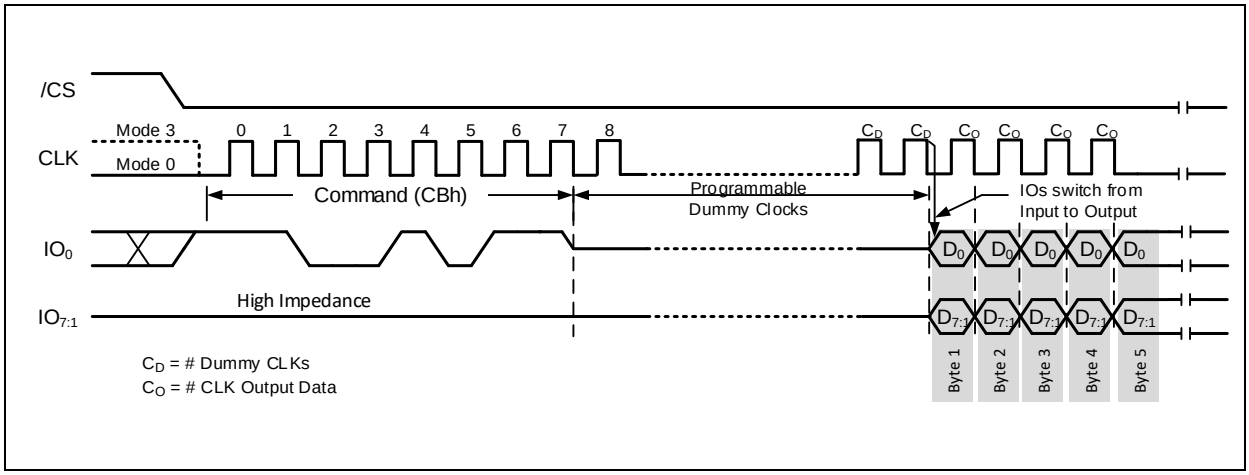


Figure 7-46 Fast Read Octal I/O Instruction SDR mode (Continuous Read Mode, BUF=0)

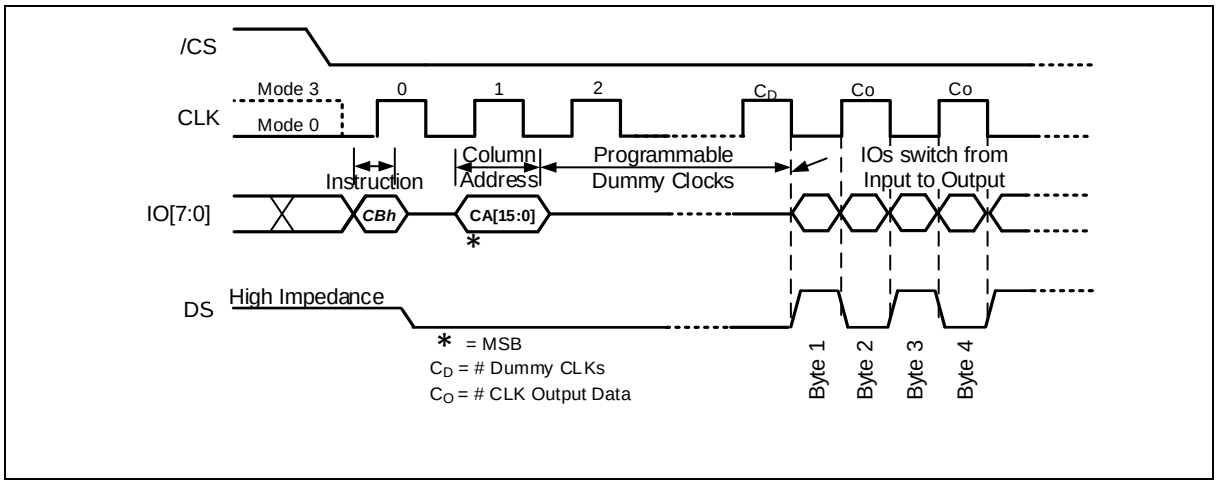


Figure 7-47 Fast Read Octal I/O Instruction ODDR mode (Buffer Read Mode, BUF=1)

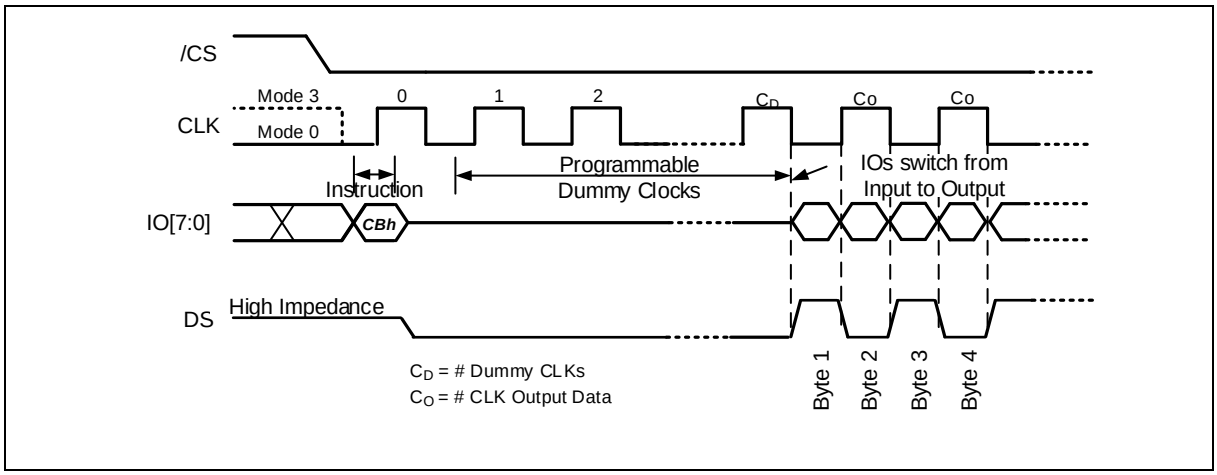


Figure 7-48 Fast Read Octal I/O Instruction ODDR mode (Continuous Read Mode, BUF=0)

7.6.6 DDR Fast Read Octal Output (9Dh)

The DDR Fast Read Octal instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The DDR Fast Read instruction is initiated by driving the /CS pin low and then shifting the instruction code “9Dh” followed by the 16-bits Column Address. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the both edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. The instruction is completed by driving /CS high.

If the Data Strobe (DS) pin is enabled by the VCR-IOC, DS pin is a synchronization signal supporting high speed data output. When instruction opcode is complete to input to the device, the device drives the DS pin low until the device transition from input sequence to output sequence and at this point the DS pin toggles simultaneously as the data output is shifted out on each CLK edge. When DS pin is not enabled, DS is in high impedance.

When BUF=1, the device is in the Buffer Read Mode. The data output sequence will start from the Data Buffer location specified by the 16-bits Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When BUF=0, the device is in the Continuous Read Mode, the data output sequence will start from the first byte of the Data Buffer and increment to the next higher address. When the end of the Data Buffer is reached, the data of the first byte of next memory page will be following and continues through the entire memory array. This allows using a single Read instruction to read out the entire memory array.

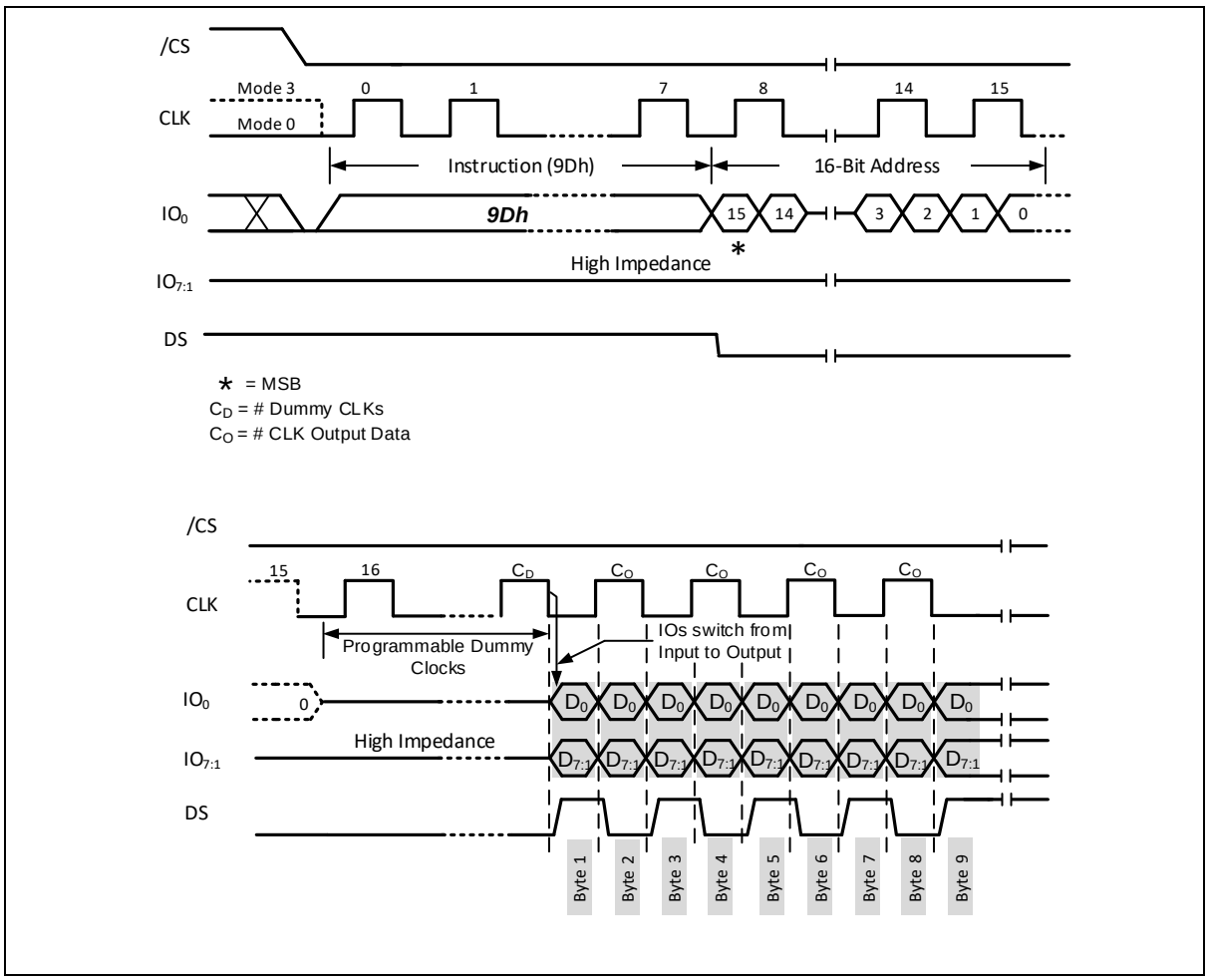


Figure 7-49 DDR Fast Read Instruction SDR mode (Buffer Read Mode, BUF=1)

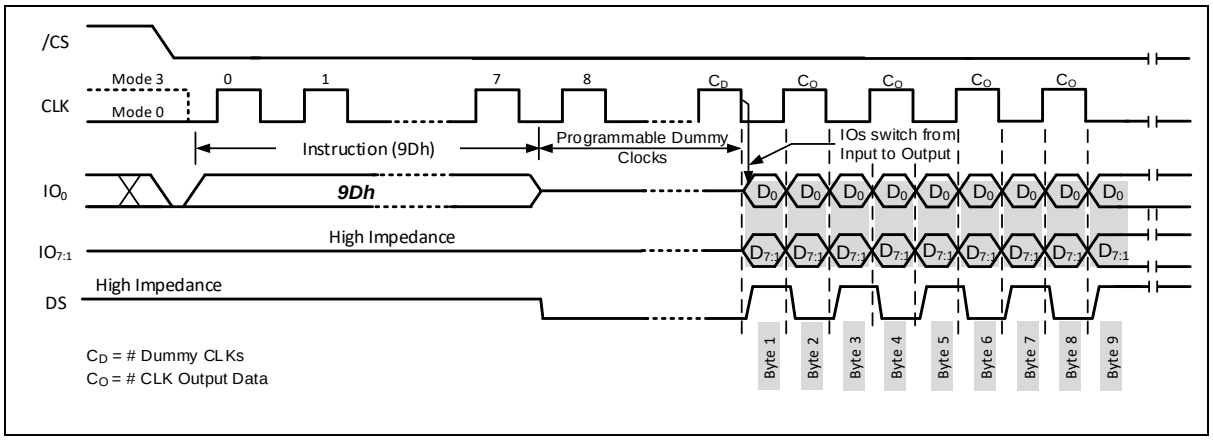


Figure 7-50 DDR Fast Read Instruction SDR mode (Continuous Read Mode, BUF=0)

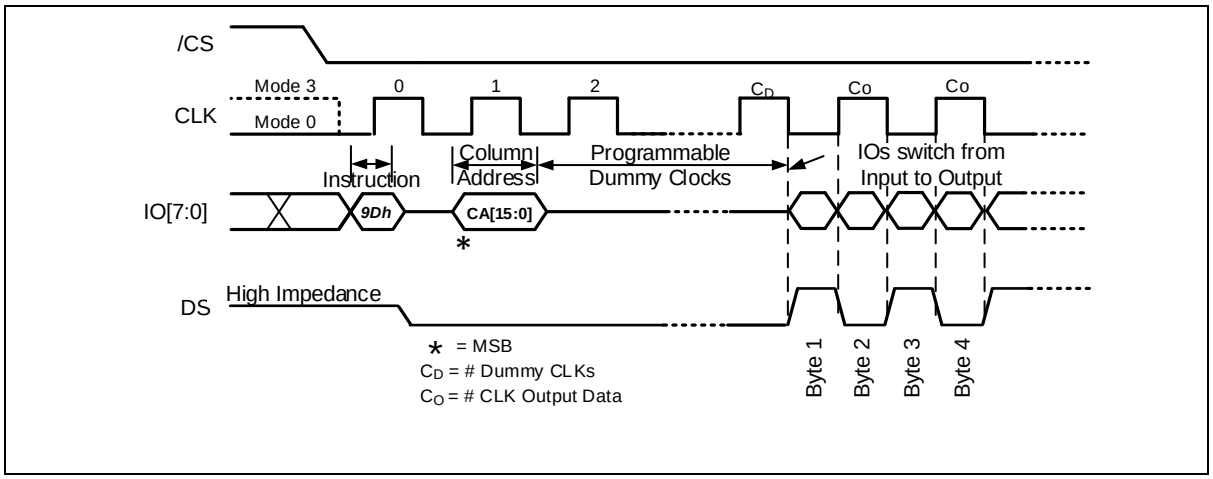


Figure 7-51 DDR Fast Read Instruction ODDR mode (Buffer Read Mode, BUF=1)

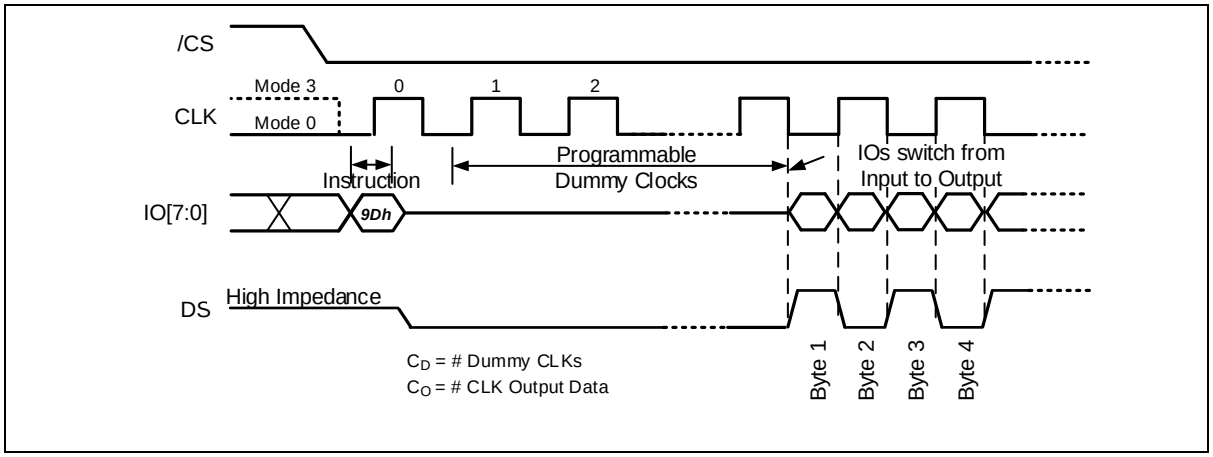


Figure 7-52 DDR Fast Read Instruction ODDR mode (Continuous Read Mode, BUF=0)

7.6.7 Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the W35N01JW is also equipped with one Unique ID Page, one Parameter Page, and ten OTP Pages.

Page Address	Page Name	Descriptions	Data Length
00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
02h	OTP Page [0]	Program Only, OTP lockable	4,224-Byte
…	OTP Pages [1:8]	Program Only, OTP lockable	4,224-Byte
0Bh	OTP Page [9]	Program Only, OTP lockable	4,224-Byte

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to “1” first. Then, Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it’s not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

Read Operations

A “Page Data Read” command must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read commands may be used to read the Data Buffer starting from any specified Column Address. Please note all Read commands must now follow the “Buffer Read Mode” command structure (CA[15:0], number of dummy clocks) regardless the previous BUF bit setting. ECC can also be enabled for the OTP page read operations to ensure the data integrity.

Program and OTP Lock Operations

OTP pages provide the additional space (4K-Byte x 10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed (change data from “1” to “0”) until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to “1” to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any “Program Data Load” commands. The “Program Execute” command followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page. When ECC is enabled, ECC calculation will be performed during “Program Execute”, and the ECC information will be stored into the 128-Byte spare area.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the “OTP Access Mode” (OTP-E=1), user needs to set OTP-L bit in the Configuration/Status Register-2 to “1”, and issue a “Program Execute” command. The page address following “program execute” is don’t care. After the device finishes the OTP lock setting (BUSY=0), the user can set OTP-E to “0” to return to the main memory array operation.

SR1-L OTP Lock Operation

The Protection/Status Register-1 contains protection bits that can be set to protect either a portion or the entire memory array from being Programmed/Erased or set the device to either Software Write Protection (WP-E=0) or Hardware Write Protection (WP-E=1). Once the BP[3:0], TB, WP-E bits are set correctly, SRP1 and SRP0 should also be set to “1”s as well to allow SR1-L bit being set to “1” to permanently lock the protection settings in the Status Register-1 (SR1). Similar to the OTP-L setting procedure above, in order to set SR1-L lock bit, the device must enter the “OTP Access Mode” (OTP-E=1) first, and SR1-L bit should be set to “1” prior to the “Program Execute” command without any Page Address. Once SR1-L is set to “1” (BUSY=0), the user can set OTP-E to “0” to return to the main memory array operation.

7.6.8 Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Byte Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

Byte Number	Descriptions	Values
0~3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h, 00h
6~7	Feature supported	00h, 00h
8~9	Optional command supported	00h, 00h
10~31	Reserved	All 00h
32~43	Device manufacturer	57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44~63	Device model	57h, 33h, 35h, 4Eh, 30h, 31h, 4Ah, 57h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	EFh
65~66	Date code	00h, 00h
67~79	Reserved	All 00h
80~83	Number of data bytes per page	00h, 10h, 00h, 00h
84~85	Number of spare bytes per page	80h, 00h
86~91	Reserved	All 00h
92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	00h, 02h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	0Ah, 00h
105~106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	00h, 00h
110	Number of programs per page	04h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115~127	Reserved	All 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	All 00h
133~134	Maximum page program time (us)	BCh, 02h
135~136	Maximum block erase time (us)	10h, 27h
137~138	Maximum page read time (us)	3Ch, 00h
139~163	Reserved	All 00h
164~165	Vendor specific revision number	00h, 00h
166~253	Vendor specific	All 00h
254~255	Integrity CRC	1Eh, 0Ah
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768~4223	Reserved	

8. INVALID BLOCK MANAGEMANT

8.1 Invalid Blocks

The W35N01JW may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks. An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	502	512	blocks

8.2 Initial Invalid Blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W35N01JW has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are permanently marked. The mark information cannot be erased. All initial invalid blocks are marked with non-FFh at the 1st byte of main array and the 1st two bytes of spare area on the 1st page. It should be checked for invalid blocks by reading the marked locations, and create a table of initial invalid blocks as following flow chart.

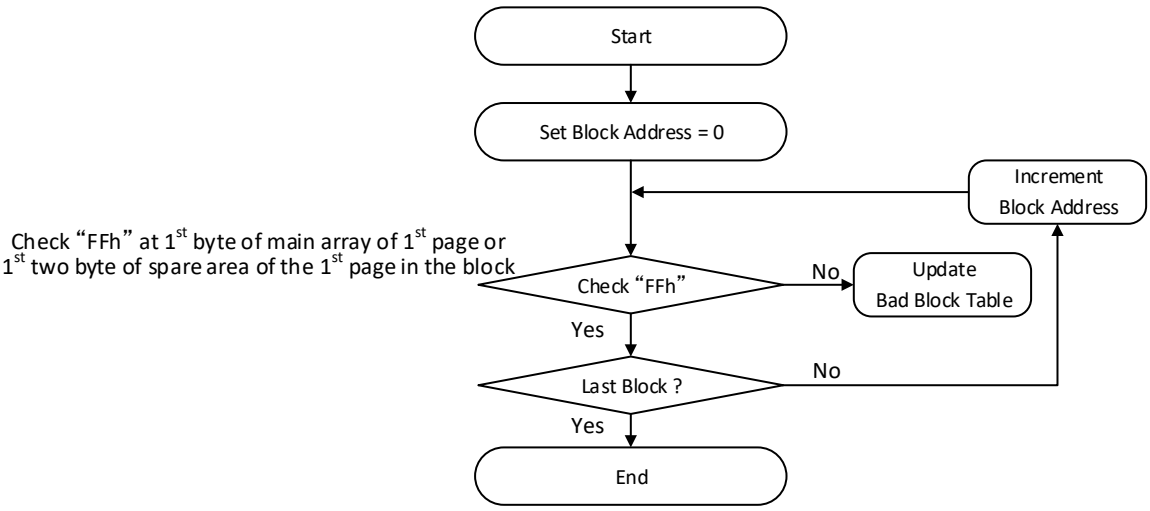


Figure 8-1 Flow Chart of Create Initial Invalid Block Table

8.3 Error in Operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the P-FAIL and E-FAIL bit to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction

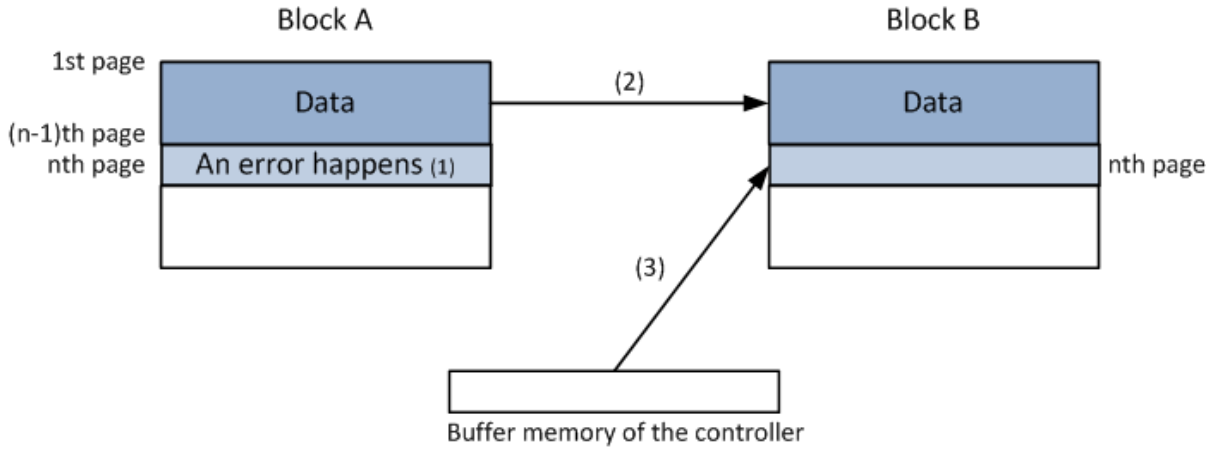


Figure 8-2 Bad Block Replacement

Notes:

1. An error happens in the nth page of block A during program or erase operation.
2. Copy the data in block A to the same location of block B which is valid block.
3. Copy the nth page data of block A in the buffer memory to the nth page of block B.
4. Creating or updating bad block table for preventing further program or erase to block A.

8.4 Addressing in Program Operation

The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	5/21/2021		New Create as Preliminary

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