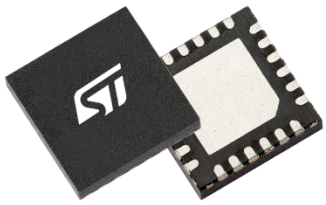
S2-LPS

Datasheet

Ultra-low power, high performance, sub-1 GHz transceiver



QFN24L (4x4 mm)

Product status link
S2-LPS

Features

- Frequency bands:
  - 433-434 MHz (S2-LPSQTR)
  - 868-870 MHz (S2-LPSQTR)
- Modulation schemes:
  - 2(G)FSK
  - OOK, ASK
- Air data rate from 0.1 to 500 kbps
- Ultra-low power consumption:
  - 7 mA RX
  - 10 mA TX @ +10 dBm
- Excellent performance of receiver sensitivity: down to -130 dBm
- Excellent receiver selectivity and blocking
- Programmable RF output power up to +16 dBm
- Programmable RX digital filter
- Programmable channel spacing
- Fast start-up and frequency synthesizer settling time
- Automatic frequency offset compensation, AGC and symbol timing recovery
- More than 145 dB RF link budget
- Battery indicator and low battery detector
- RX and TX 128 bytes FIFO buffers
- 4-wire SPI interface
- Embedded timeout protocol engine
- Excellent receiver selectivity (> 80 dB @ 2 MHz)
- ST companion integrated balun/filter chips are available
- Antenna diversity algorithm
- Fully integrated ultra-low power RC oscillator
- Wake-up driven by internal timer or external event
- Digital real time RSSI
- Flexible packet length with dynamic payload length
- Programmable preamble and SYNC word quality filtering and detection
- KNX-RF supported
- Suitable to build systems targeting:
  - **Europe**: ETSI EN 300 220, category 1.5 natively compliant, ETSI EN 303 131
  - **US**: FCC part 15 and part 90
  - **Japan**: ARIB STD T67, T108
  - **China**: SRRC
- Operating temperature range: -40 °C to +85 °C

Applications

- Sensors to Cloud

- Smart metering
- Home energy management systems
- Wireless alarm systems
- Smart home
- Building automation
- Industrial monitoring and control
- Smart lighting systems

Description

The S2-LPS is a high performance ultra-low power RF transceiver, intended for RF wireless applications in the sub-1 GHz band. It is designed to operate in both the license-free ISM and SRD frequency bands at 433, 868 MHz, but can also be programmed to operate at other additional frequencies in the 413-479 MHz, 826-958 MHz bands.

The S2-LPS supports different modulation schemes: 2(G)FSK, OOK and ASK. The air data rate is programmable from 0.1 to 500 kbps.

The S2-LPS can be used in systems with channel spacing down to 1 kHz enabling the narrow band operations.

The S2-LPS shows an RF link budget higher than 140 dB for long communication ranges and meets the regulatory requirements applicable in territories worldwide, including Europe, Japan, China and the USA.

1 Detailed functional description

The S2-LPS fully supports antenna diversity with an integrated antenna switching control algorithm.

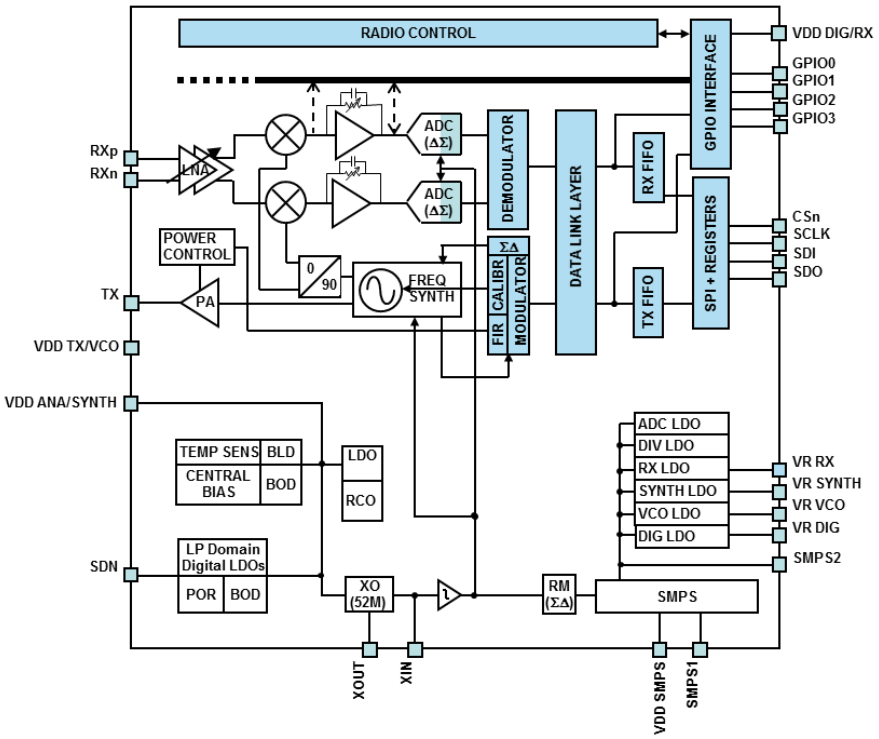
Transmitted/received data bytes are buffered in two different 128 bytes FIFOs (TX FIFO and RX FIFO), accessible via SPI interface for host processing.

In addition, the reduced number of external components enables a cost effective solution permitting a compact PCB footprint.

The S2-LPS targets volume applications like:

- Sensors to Cloud
- Smart metering
- Home energy management systems
- Wireless alarm systems
- Smart home
- Building automation
- Industrial monitoring and control

Figure 1. Simplified S2-LPS block diagram



The receiver architecture is low-IF conversion, the received RF signal is amplified by a two-stage low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). LNA and IF amplifiers make up the RX front-end (RXFE) and have programmable gain. At IF, the ADCs digitalize the I/Q signals. The demodulated data go to an external MCU either through the 128-byte RX FIFO, readable via SPI, or directly using a programmable GPIO pin.

The transmitter part of the S2-LPS is based on direct synthesis of the RF frequency. The power amplifier (PA) input is the LO generated by the RF synthesizer, while the output level can be configured between -30 dBm and +14 dBm (+16 dBm in boost mode), at antenna level with 0.5 dB steps.

The data to be transmitted can be provided by an external MCU either through the 128-byte TX FIFO writable via SPI, or directly using a programmable GPIO pin. The S2-LPS supports frequency hopping, TX/RX and antenna diversity switch control, extending the link range and improving performance.

The S2-LPS has a very efficient power management (PM) system. An integrated switched mode power supply (SMPS) regulator allows operation from a battery voltage ranging from +1.8 V to +3.6 V, and with power conversion efficiency of 90%.

A crystal must be connected between XIN and XOUT. It is digitally configurable to operate with different crystals. As an alternative, an external clock signal can be used to feed XIN for proper operation. The S2-LPS also has an integrated low-power RC oscillator, generating the 34.7 kHz signal used as a clock for the slowest timeouts.

A standard 4-pin SPI bus is used to communicate with the external MCU. Four configurable general purpose I/Os are available.

2 Typical application diagram and pin description

This section describes three different application diagrams for the S2-LPS. Two main configurations are available:

- HPM (high performance mode) configuration
- LPM (low power mode) configuration

In the LPM operating mode the LDOs are bypassed and the SMPS provides the regulator voltage at 1.2 V. Note that in LPM the PA is supplied from SMPS at 1.2 V (instead of 1.5 V as in HPM), so the max. output power is lower than HPM. The figure below shows the suggested configuration with discrete matching network and SMPS-ON.

Figure 2. Suggested application diagram (embedded SMPS used)

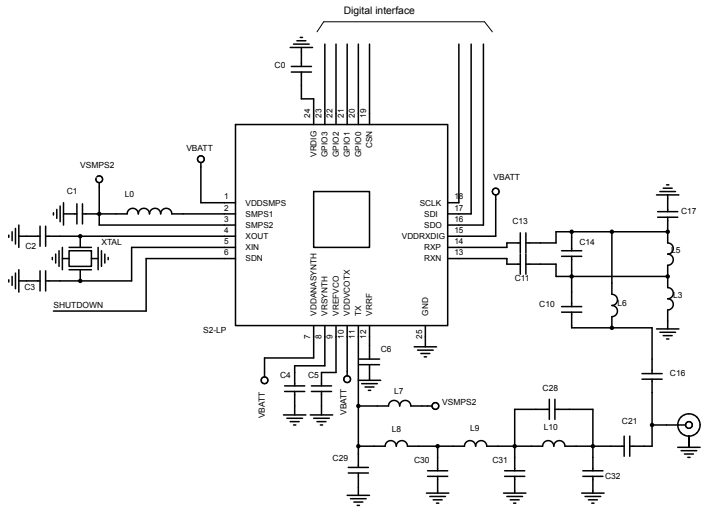


Figure 3. Suggested application diagram (embedded SMPS not used) shows the suggested configuration with discrete matching network and SMPS-OFF mode.

Figure 3. **Suggested application diagram (embedded SMPS not used)**

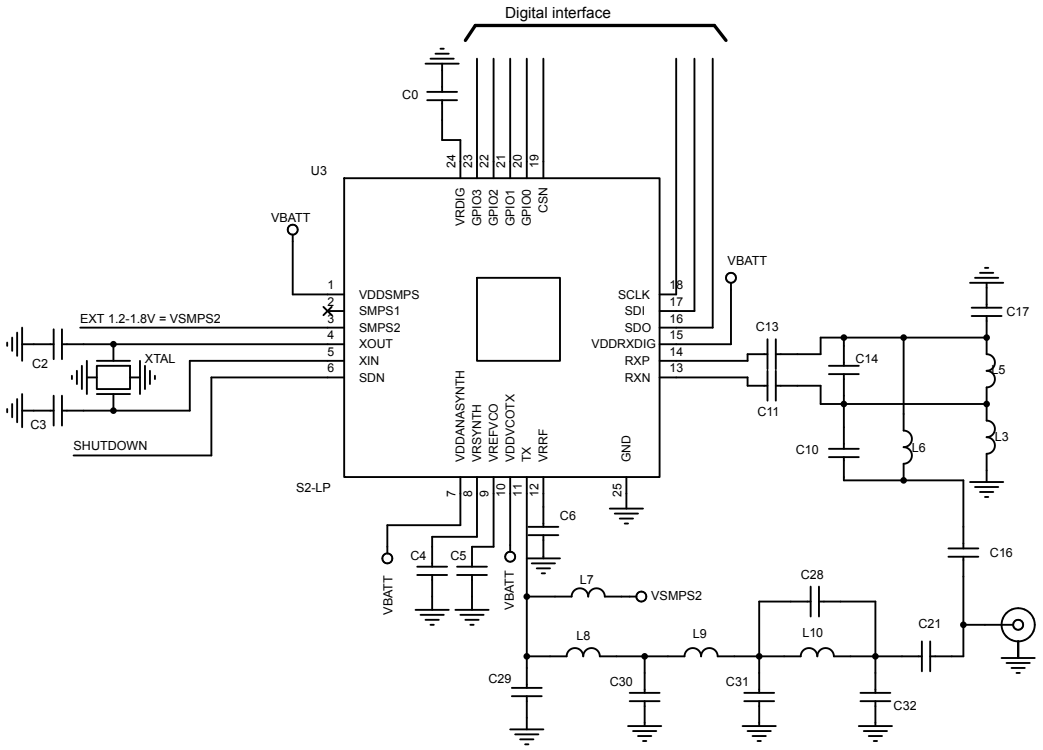


Figure 4. **Suggested application diagram HPM/LPM (integrated balun, embedded SMPS used)**

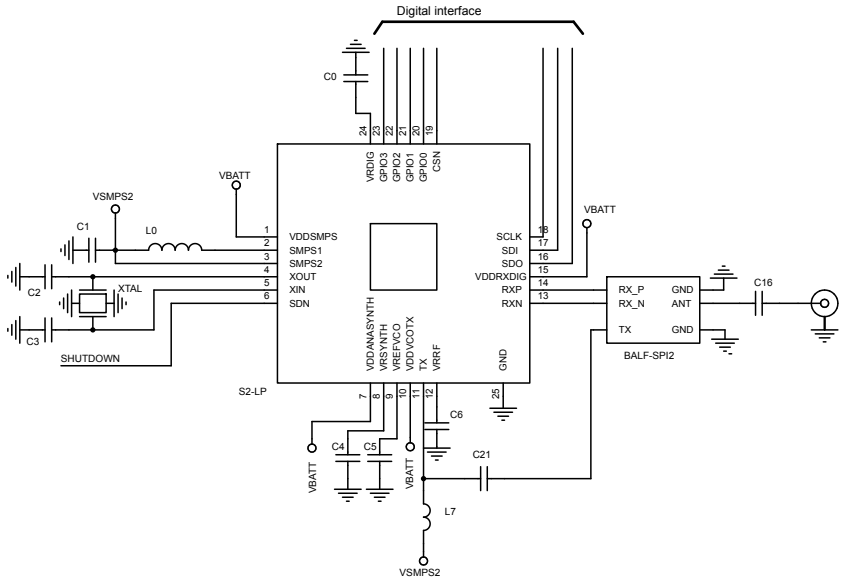
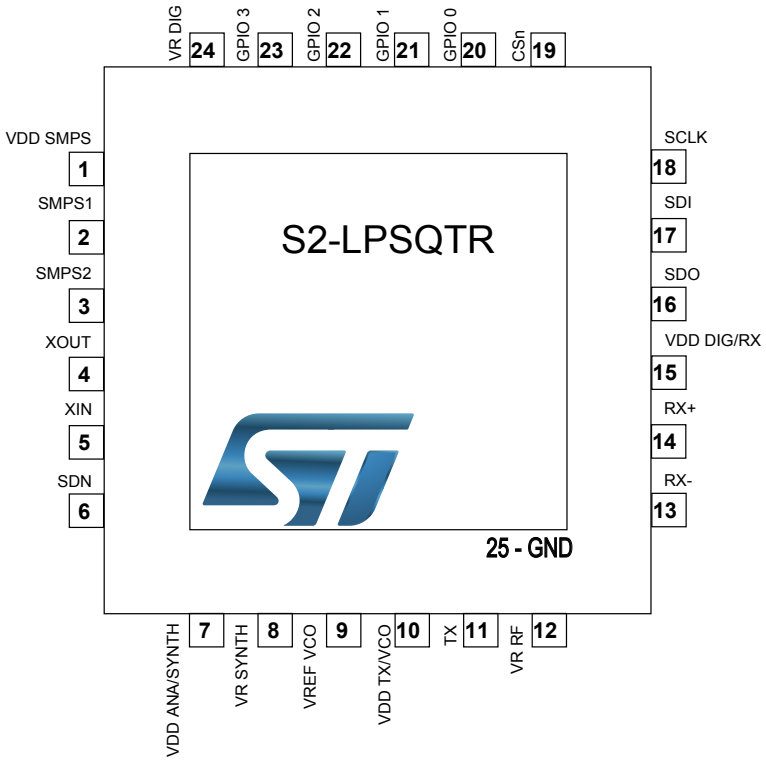


Table 1. Description of the external components of the typical application diagrams

Components	HPM/LPM discrete balun		HPM/LPM integrated balun	Description
	SMPS ON	SMPS OFF		
C0	X	X	X	Decoupling capacitor for on-chip voltage regulator to digital part
C1	X	-	X	SMPS LC filter capacitors
C2, C3	X	X	X	Crystal loading capacitors
C4	X	X	X	Decoupling capacitor for on-chip voltage regulator to synthesizer (LF part)
C5	X	X	X	Decoupling capacitor for band-gap voltage reference of VCO regulator
C6	X	X	X	Decoupling capacitor for on-chip voltage regulator to LNA-MIXER
C29, C30, C31, C32	X	X		TX LC filter/matching capacitors
C11, C13	X	X		DC blocking capacitors
C16, C21	X	X	X	
C10, C14, C17	X	X		RF balun/matching capacitors
L0	X	-	X	SMPS LC filter inductor
L7	X	X	X	RF choke inductor or resonating inductor (upon RF network topology)
L8, L9, L10	X	X		TX LC filter/matching inductors
L3, L5, L6	X	X		RX balun/matching inductors
XTAL	X	X	X	Crystal

2.1 Pin diagram

Figure 5. **Pin diagram, QFN24 (4x4 mm) package**



2.2 Pin description

Table 2. **Pinout**

Number	Pin name	Pin type	Description
1	VDD SMPS	Power	1.8 V to 3.6 V analog power supply for SMPS only.
2	SMPS1	Analog out	1.1 V to 1.8 V SMPS regulator output to be externally filtered
3	SMPS2	Analog in	1.1 V to 1.8 V SMPS voltage input after LC filtering applied to SMPS1 output
4	XOUT	Analog out	Crystal oscillator output. Connect to an external crystal or leave floating if driving the XIN pin with an external clock source
5	XIN	Analog in	Crystal oscillator input. Connect to an external crystal or to an external clock source. If using an external clock source, DC coupling with a minimum 0.2 VDC level is recommended and minimum AC amplitude of 400 mVpp (however, the instantaneous level at input cannot exceed the 0 – 1.4 V range)
6	SDN	Digital in	Shutdown input pin. SDN should be = ‘0’ in all modes, except shutdown mode
7	VDD ANA/ SYNTH	Power	1.8 V to 3.6 V power
8	VR SYNTH	Analog in/out	1.2 V SYNTH-LDO output for decoupling
9	VREF VCO	Analog out	1.2 V VCO-LDO band-gap reference voltage decoupling
10	VDD VCO/TX	Power	1.8 V to 3.6 V power supply
11	TX	RF output	RF output signal

Number	Pin name	Pin type	Description
12	VR RF	Analog in/out	1.2 V RX-LDO output for decoupling
13	RXn	RF in	Differential RF input signals for the LNA
14	RXp	RF in	
15	VDD RX/DIG	Power	1.8 V to 3.6 V power supply
16	SDO	Digital out	SPI slave data output
17	SDI	Digital in	SPI slave data input
18	SCLK	Digital in	SPI slave clock input
19	CSn	Digital in	SPI chip select
20	GPIO0	Digital I/O	General purpose I/O that may be configured through the SPI registers to perform various functions
21	GPIO1	Digital I/O	
22	GPIO2	Digital I/O	
23	GPIO3	Digital I/O	
24	VR DIG	Analog in/out	1.2 V digital power supply output for decoupling
25	GND	Ground	Exposed pad connected to the ground of the application board

3 Specifications

3.1 Absolute maximum ratings

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages refer to GND.

Table 3. Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
Supply and SMPS pins	-0.3		+3.9	V
DC voltage on VREG pins	-0.3		+3.9	
DC voltage on digital input pins	-0.3		+3.9	
DC voltage on digital output pins	-0.3		+3.9	
DC voltage on ground pins	-0.3		+3.9	
DC voltage on analog pins	-0.3		+1.8	
DC voltage on TX pin	-0.3		+3.9	
Storage temperature range	-40		+125	°C
VESD-HBM	-500		+500	V

3.2 Operating range

Table 4. Operating range

Parameter	Min.	Typ.	Max.	Unit
Operating battery supply voltage (V_{BAT})	1.8(1)	3.0	3.6	V
Operating ambient temperature range	-40	25	+85	°C

1. *2 V when the device works in boost mode with SMPS ON.*

3.3 Thermal properties

Table 5. Thermal data

Parameter	QFN24	Unit
Thermal resistance junction-ambient	66	°C/W

3.4 Power consumption

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to 25 °C temperature, V_{BAT} = 3.3 V. All performance is referred to the STEVAL-FKI433V2 or STEVAL-FKI868V2 with a 50 Ohm antenna connector.

Table 6. Low-power state power consumption

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	Shutdown	-	2.5	-	nA
	Standby		500		
	Sleep		700		
	Sleep (FIFOs retained)		0.95		µA
	Ready		350		

Table 7. Power consumption in reception T_A = 25 °C, VDD = 3.3 V, f_c = 868 MHz

Parameter	Test conditions	Min.	HPM typ.	LPM typ.	Max.	Unit
Supply current	RX @ sensitivity level	-	8.6	7.2	-	mA

Table 8. Power consumption in transmission f_c= 915 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm	-	22	-	mA
	TX CW @ 10 dBm(1)	-	12.5	-	
	TX CW @ 16 dBm in Boost (2)	-	32		

1. *SMPS output voltage 1.2 V, LDOs disable.*
2. *SMPS output voltage 1.8 V.*

Table 9. Power consumption in transmission f_c= 840-868 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm	-	20	-	mA
	TX CW @ 10 dBm(1)	-	11.5	-	
	TX CW @ 16 dBm in Boost (2)	-	29	-	-

1. *SMPS output voltage 1.2 V, LDOs disable.*
2. *SMPS output voltage 1.8 V.*

Table 10. Power consumption in transmission f_c= 434 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm(1)	-	21	-	mA
	TX CW @ 10 dBm(2)	-	11.5	-	

1. *SMPS output voltage 1.6 V.*
2. *SMPS output voltage 1.2 V, LDOs disable.*

Table 11. Power consumption in transmission f_c = 510 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm	-	19	-	mA
	TX CW @ 10 dBm(1)	-	12	-	
	TX CW @ 15 dBm(2)	-	27	-	

1. *SMPS output voltage 1.2 V, LDOs disable.*
2. *SMPS output voltage 1.8 V.*

3.5 General characterization

Table 12. General characteristics

Parameter		Typ.	Unit
Frequency range		413 - 479	MHz
		826 - 958	
Data rate DR	2-(G)FSK	0.1 - 250	kbps
	OOK/ASK	0.1 -125	
Data rate accuracy		±100	ppm
Frequency deviation FDEV		0.15 - 500	kHz

3.6 Frequency synthesizer

Table 13. Frequency synthesizer parameters

Parameter	Test conditions	50 MHz	Unit
Frequency step size	Out-loop divider ratio = 4	23.8	Hz
RF carrier phase noise 433 MHz	10 kHz	-109	dBc/Hz
	100 kHz	-110	
	1 MHz	-124	
	10 MHz	-141	
RF carrier phase noise 868 MHz	10 kHz	-102	
	100 kHz	-103	
	1 MHz	-117	
	10 MHz	-138	

3.7 Crystal oscillator

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.0 V.

The device supports crystals 26 MHz.

From now on in this document the XTAL oscillator will be indicated with f_{XO} and the digital clock with f_{dig}

- if a 26 MHz crystal is used, this bit must be 1 (digital divider disabled):

$$f_{dig} = f_{xo} \quad (1)$$

In order to avoid potential RF performance degradations, the crystal frequency should be chosen to satisfy the following equation:

$$\left| nF_{CH} - \mathrm{ROUND}\left(n\frac{F_{CH}}{f_{XO}}\right)f_{XO} \right| \geq 1\mathrm{MHz} \quad (2)$$

where n is an integer in the set [1-7, B] (B is the synthesizer's divider ratio).

Table 14. Crystal oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency		24	-	26	MHz
Frequency tolerance (1)	-	-	± 40	-	ppm
Minimum requirement on external reference phase noise mask $f_{XO} = 26$ MHz, to avoid degradation on synthesizer phase/noise	10 kHz	-	-	-135	dBc/Hz
	100 kHz	-	-	-140	
	1 MHz	-	-	-140	
	10 MHz	-	-	-140	
Programmable trans-conductance of the oscillator at start-up	-	13	-	43	mS
Start-up time (2)	VBAT=1.8 V, $f_{XO} = 26$ MHz	-	100	-	µs

1. *Including initial tolerance, crystal loading, aging, and temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.*
2. *Start-up times are crystal dependent. The crystal oscillator trans-conductance can be tuned to compensate the variation of crystal oscillator series resistance.*

Table 15. Ultra-low power RC oscillator

Parameter	Test conditions	Typ.	Unit
Calibrated frequency	Calibrated RC oscillator frequency is derived from crystal oscillator frequency.	33.3 (1)	kHz
Frequency accuracy after calibration	-	±1	%

1. *Depending on the crystal frequency, the reported value is referring to 50 MHz.*

3.8 RF receiver

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.3 V, no frequency offset in the RX signal. The whole performance is referred to the STEVAL-FKI433V2, STEVAL-FKI512V1 or STEVAL-FKI868V2 with a 50 Ohm antenna connector.

Table 16. RF receiver characteristics

Parameter	Test conditions		HPM/LPMSMPS on typ.	Unit
Receiver channel bandwidth CHF	-		1-800	kHz
RX input return loss	Max. RX gain, tied (RX + TX) matching networks	433 MHz	-15	dB
		868 MHz	-15	
Saturation 1% BER	2-FSK 1.2 kHz FDEV, DR = 1.2 kbps, CHF = 4 kHz	433 MHz	10	dBm
		868 MHz	10	
Input third order intercept point	Interferers are continuous wave @ 6 MHz and 12 MHz offset from carrier	433 MHz	-25	
		868 MHz	-25	
RX noise figure	Max. RX gain, tied (RX + TX) matching networks	433 MHz	8	dB
		868 MHz	8	
Differential input impedance at LNA	Max. RX gain R // C	433 MHz	200 // 1.5	Ω//pF
		868 MHz	200 // 1.5	

3.8.1 Blocking and selectivity at 433 MHz

Table 17. Blocking and selectivity at 433 MHz

Parameter	Test condition	HPM SMPS on (typ.)	LPM SMPS ON typ.	Unit
Selectivity and blocking 1% BER @ 2-GFSK BT=0.5 20 kHz FDEV, DR = 38.4 kbps, CHF = 100 kHz	+100 kHz (adjacent channel)	50	37	dB
	-100 kHz (adjacent channel)	50	37	
	+200 kHz (alternate channel)	51	45	
	-200 kHz (alternate channel)	51	45	
	Image rejection	56	58	
	±2 MHz	67	67	
	±10 MHz	69	72	

3.8.2 Sensitivity at 433 MHz

Table 18. Sensitivity at 433 MHz

Parameter	Test conditions	HPM/LPM SMPS on (typ.)	Unit
Sensitivity 1% BER @ 2-GFSK BT = 0.5	DR = 38.4 kbps, FDEV = 20 kHz, CHF = 100 kHz	-109	dBm
Sensitivity 1% BER @ OOK	DR = 0.3 kbps, CHF = 1 kHz	-120	dBm
	DR = 1.2 kbps, CHF = 4 kHz	-118	
	DR = 38.4 kbps, CHF = 100 kHz	-104	

3.8.3 Blocking and selectivity at 840-868 MHz

Table 19. Blocking and selectivity @ 840-868 MHz

Parameter	Test conditions	HPM SMPS on (typ.)	LPM SMPS on (typ.)	Unit
Selectivity and blocking 1% BER @ 2-GFSK BT = 0.5, 20 kHz FDEV, DR = 38.4 kbps, CHF = 100 kHz	+100 kHz (adjacent channel)	44	33	dB
	-100 kHz (adjacent channel)	44	33	
	+200 kHz (alternate channel)	45	39	
	-200 kHz (alternate channel)	45	39	
	Image rejection	50	55	
	± 2 MHz	67	70	
	± 10 MHz	69	73	

3.8.4 Sensitivity at 840-868 MHz

Table 20. Sensitivity at 840-868 MHz

Parameter	Test conditions	HPM/LPM/SMPS on typ.	Unit
Sensitivity 1% BER @ 2-GFSK BT = 0.5	DR = 38.4 kbps, FDEV = 20 kHz, CHF = 100 kHz	-109	dBm
Sensitivity 1% BER @ OOK	DR = 0.3 kbps, CHF = 1 kHz	-120	dBm
	DR = 1.2 kbps, CHF = 4 kHz	-118	
	DR = 38.4 kbps, CHF = 100 kHz	-104	

3.9 RF transmitter

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.3 V. All performance is referred to the STEVAL-FKI433V2 or STEVAL-FKI868V2 with a 50 Ω antenna connector.

Table 21. RF transmitter characteristics

Parameter	Test conditions	HPM typ.	LPM typ.	Unit
Maximum output power	CW @ antenna level	14	10	dBm
Maximum output power in boost mode	CW @ antenna level	16	12	
Minimum output power	CW @ antenna level	-30	-30	
Output power step	-10<=output power<=+10 dBm	0.5	0.5	dB
Output power step (1)	Output power>+10 dBm	1(1)		

1. *In this case the register 0x64 is set to 0x4A.*

Table 22. PA impedance

Parameter	Test conditions	Typ.	Unit
Optimum load impedance	433 MHz	56+25j	Ω
	868 MHz	30+24j	
Max permitted VSWR @ antenna level	433 MHz	2	
	868 MHz	5	

Table 23. Regulatory standards

Frequency band	Suitable for compliance with:
413 - 479 MHz	ETSI EN300 220 category 1.5
	FCC part 15, FCC part 90
826 - 958 MHz	ETSI EN300 220-2 category 1.5
	FCC part 15
	ARIB STD-T108
	Chinese SRRC

3.9.1 Harmonic emission at 433 MHz

Table 24. Harmonic emission at 433 MHz

Parameter	Test conditions	SMPS on	Unit
H1	CW	14	dBm
H2	CW	-51	
H3	CW	-56	
H4	CW	-39	
H5	CW	-34	
H6	CW	-46	
H7	CW	-44	

3.9.2 Harmonic emission at 840-868 MHz

Table 25. Harmonic emission at 840-868 MHz

Parameter	Test conditions	HPM/LPM/SMPS on	Unit
H1	CW	14	dBm
H2	CW	-38	
H3	CW	-54	
H4	CW	-52	
H5	CW	-52	
H6	CW	-43	
H7	CW	-51	

3.10 Digital interface specification

Table 26. Digital SPI input, output and GPIO specification

Parameter	Test conditions	Min.	Typ.	Max.	Unit
SPI clock frequency			8	10	MHz
Port I/O capacitance			1.4		pF
Rise time	From 0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		6.0		ns
	From 0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
Fall time	From 0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		7.0		ns
	From 0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
Logic high level input voltage		VDD/2 +0.3			V
Logic low level input voltage				VDD/8 +0.3	V
High level output voltage	IOH = -2.4 mA (-4.2 mA into high output current mode).	(5/8)*			V

Parameter	Test conditions	Min.	Typ.	Max.	Unit
		VDD+ 0.1			
Low level output voltage	IOL = +2.0 mA (+4.0 mA into high output current mode).			0.5	V
CSn low to positive edge on SCLK in low power mode state			40		µs
CSn low to positive edge on SCLK in ready state		30			ns

3.11 Battery indicator

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.0 V.

Table 27. Battery indicator and low battery detector

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Battery level thresholds #1			2.1		V
Battery level thresholds #2			2.3		
Battery level thresholds #3			2.5		
Battery level thresholds #4			2.7		
Brownout threshold	Measured in slow battery variation (static) conditions (inaccurate mode)		1.5		
	Measured in slow battery variation (static) conditions (accurate mode)		1.7		
Brownout threshold hysteresis			70		mV

Note: For battery-powered equipment, the TX does not transmit at a wrong frequency under low battery voltage conditions. It remains on either channel or stops transmitting. The latter can of course be realized by using a lock detect and/or by switching off the PA under control of the battery monitor. For testing reasons this control is enabled/disabled by SPI.

4 Block description

4.1 Power management

The S2-LPS integrates a high efficiency step-down converter cascaded with LDOs meant to supply both analog and digital parts. However, an LDO directly fed by the external battery provides a controlled voltage to the data interface block.

S2-LPS's power management (PM) strategy, besides the basic functionality of providing different blocks with proper supplies, faces two main constraints: the first one is to implement such a power distribution with maximum efficiency, and the second one is to guarantee the isolation among critical blocks.

The efficiency target is obtained by using a switch mode power supply (SMPS) which converts the battery voltage (1.8 V - 3.6 V) to a lower voltage (settable from 1.2 V to 1.8 V) with efficiency higher than 90%.

The SMPS output voltage can be controlled by the SET_SMPS_LVL field in the PM_CONF0 register. The relation between the SET_SMPS_LVL and the V_{OUT} of the SMPS is given by the following table:

Table 28. SMPS output voltage

SET_SMPS_LVL	SMPS output voltage
001b	1.2 V
010b	1.3 V
011b	1.4 V
100b	1.5 V
101b	1.6 V
110b	1.7 V
111b	1.8 V

The SMPS output voltage can be controlled in TX only or for both RX and TX according to the SMPS_LVL_MODE bit of the PM_CONF1 register.

- 1: SMPS output level depends upon the value in PM_CONFIG register just in TX state, while in RX state it is fixed to 1.4 V.
- 0: SMPS output level depends upon the value written in the PM_CONFIG0 register (SET_SMPS_LEVEL field) both in RX and TX state.

The SMPS switching frequency is settable by the 2 registers PM_CONF3 and PM_CONF2.

If the KRM_EN is 0, then the digital divider by 4 enabled. In this case SMPS' switching frequency is:

$$F_{sw} = \frac{f_{dig}}{4} \quad (3)$$

If the KRM_EN is 1, the SMPS' switching frequency can be set by the KRM word according to the formula:

$$F_{sw} = K_{rm}\frac{f_{dig}}{2^{15}} \quad (4)$$

As f_{dig} is the digital domain frequency (f_{XO} if it is 26 MHz).

All the RX measurements reported in this datasheet have been taken with a SMPS frequency set to 1.56 MHz.

From the formula reported with fdig = 25 MHz, PM_CONF3 = 0x87, PM_CONF2 = 0xFC, the F_{sw} is 1.56. It is possible to have a little improvement of the sensitivity reducing the SMPS switching frequency but having as drawback a higher current consumption.

The isolation target is reached by using, for each critical block, a dedicated linear low-dropout regulator (LDO), which provides typically 1.2 V output voltage, either from battery level or from SMPS level, depending from the operating mode.

If the output of the LDO is 1.2 V the minimum value of the SMPS, V_{out} must be at least 100 mV higher than the V_{out} of the LDO. This means that in HPM (SMPS+LDO) the minimum value of the SMPS_VOUT must be 1.3 V.

The S2-LPS PM can be configured by SPI (BYPASS_LDO field in PM_CONFIG [1] register) in two main modes:

1. High performance mode (HPM)
2. Low power mode (LPM)

In HPM all available LDOs supplied from SMPS are used, to get the best possible isolation and minimum low-frequency noise level and SMPS ripple. SMPS must be set to 1.4 V at least.

In LPM the LDOs connected to the SMPS are by-passed and SMPS must be configured to provide 1.2 V output level to increase the regulation efficiency but with reduced isolation and higher low-frequency noise and SMPS ripple.

The load inductor of the SMPS has to have the following characteristics:

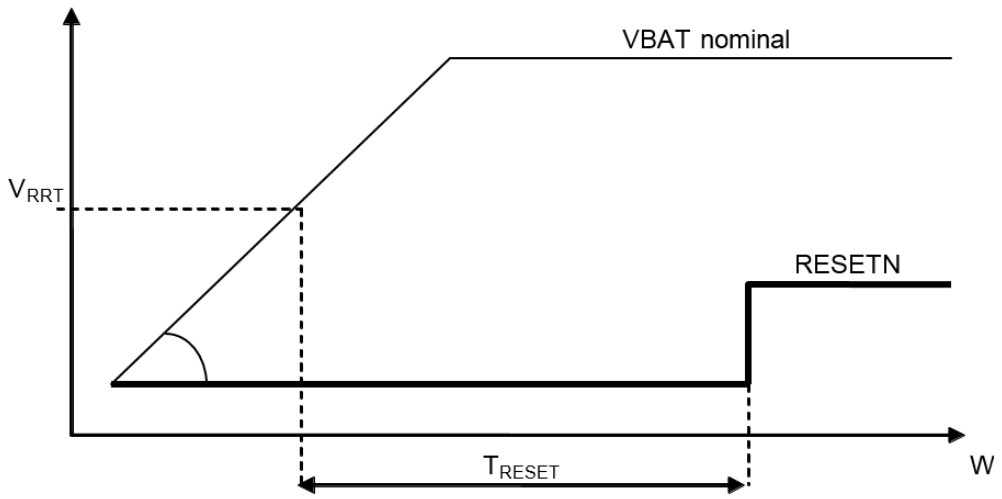
- A typical 10 µH nominal value +/-10%
- A rated current of 100 mA minimum
- A DC resistance as low as possible (to guarantee maximum efficiency of the SMPS block), around 1 Ohm is a typically good value, but the lower the better

4.2 Power-On-Reset

The Power-On-Reset (POR) circuit generates a reset pulse upon power-up which is used to initialize the entire digital logic. Power-on-reset senses V_{BAT} voltage.

The S2-LPS provides an automatic POR circuit, which generates an internal RESETN (active low) level for a time T_{RESET}, after the V_{BAT} reaches the reset release voltage threshold V_{RRT}, as shown in Figure 6. Power-On-Reset timing and limits. The same reset pulse is generated after a step-down on the input pin SDN (VDD>V_{RRT}). This signal is available on the GPIO0 pin.

Figure 6. Power-On-Reset timing and limits



The parameters VRRT and TRESET are fixed by design in order to guarantee a reliable reset procedure of the state machine. In addition, all the registers are initialized to their default values.

A software command SRES is also available, it generates an internal but partial resetting of the S2-LPS.

Table 29. POR parameters

Parameter	Comment	Min.	Typ.	Max.	Unit
Reset start-up threshold voltage			0.5		V
Hold pulse width (T_{hold}, figure below)	For SDN to be effective	1			µs

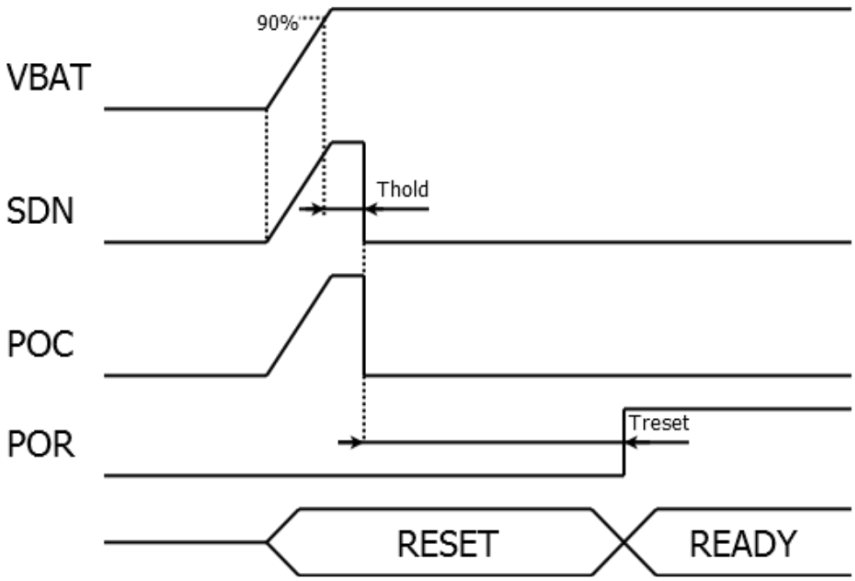
Parameter	Comment	Min.	Typ.	Max.	Unit
Reset pulse width (T_{reset}, figure below)			0.7	2	ms
Power-on VDD slope			2.0		V/ms

The following picture shows how the S2-LPS must be controlled, i.e. the SDN signal must be tied to VBAT pin in order to avoid two potential issues during the start-up phase:

1. A cross conduction can appear on the GPIO until an available command is present on it.
2. The ESD protection diode from the SDN pad can sink current from the external driver connected to the SDN.

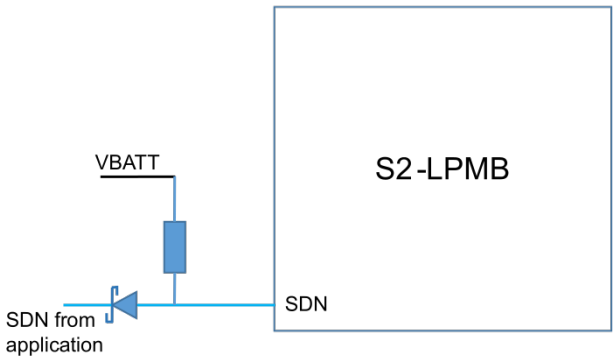
Also the SDN signal generates an internal signal (POC), which disables the digital I/Os when set to 1.

Figure 7. Start-up phase



Examples of possible connections

Figure 8. Examples of possible connections for SDN pin



4.3 RF synthesizer

A crystal connected to XIN and XOUT provides a clock signal to the frequency synthesizer. The allowed clock signal frequency is 26 MHz.

As an alternative, an external clock signal feeds XIN for proper operation. In this option, XOUT can be left either floating or tied to ground.

The integrated phase locked loop (PLL) is capable to synthesize a band of frequencies from 413 to 479 MHz, 826 to 958 MHz, providing the LO signal for the RX chain and the input signal for the PA in the TX chain.

Depending on the RF frequency and channel used, a very high accurate crystal or TCXO can be required.

The RF synthesizer implements fractional sigma delta architecture to allow fast settling and narrow channel spacing. It is fully integrated, and it uses a multi-band VCO to cover the whole frequency range. All internal calibrations are automatic.

According to the frequency synthesized the user must set the charge pump current according to the LO frequency variations, in order to have a constant loop bandwidth. The charge pump current is controlled by the PLL_CP_ISEL field (SYNT3 register) and the PLL_PFD_SPLIT_EN (SYNTH_CONFIG2). These fields should be set in the following way:

Table 30. Charge pump words

VCO Freq (MHz)	fxo (MHz)	PLL_CP_ISEL	PLL_PFD_SPLIT_EN	ICP (µA)
3760	25	001	1	200
3460	25	010	1	240

The S2-LPS provides an automatic and very fast calibration procedure for the frequency synthesizer. If not disabled, it performs the calibration each time the synthesizer is required to lock to the programmed RF channel frequency (transaction from READY to LOCK/TX/RX or from RX to TX and vice versa). After completion, the S2-LPS uses the calibration word and is stored in registers.

In order to get the synthesizer locked with the calibration procedure disabled, the correct calibration words must be previously stored in registers by user for TX and RX respectively. The advantage is reduce the LOCK setting time.

The transition time enables the S2-LPS for frequency hopping operation due to its reduced response time and very quick programming synthesizer.

4.3.1 RF channel frequency settings

The channel center frequency can be programmed as follows:

Center frequency setting

$$f_c = f_{base} + \left(\frac{f_{xo}}{2^{15}} \cdot CHSPACE\right) \cdot CHNUM \quad (5)$$

The f_{base} sets the main channel frequency; the value depends on the value of f_{xo} (the frequency of the XTAL oscillator, typically 26 MHz.

Base frequency setting

$$f_{base} = \frac{f_{xo}}{\frac{B}{2} \cdot D} \cdot \frac{SYNT}{2^{20}} \quad (6)$$

where:

SYNT is a programmable 28-bits integer (SYNT[3:0] registers).

B is the out-of-loop SYNTH divider (BS field of the SYNT3 register):

PLL divider

$$B = \begin{cases} 4 \; for \; the \; high \; band & (826 \; MHz \; to \; 1055 \; MHz, \; BS = 0) \\ 8 \; for \; the \; middle \; band & (413 \; MHz \; to \; 527 \; MHz, \; BS = 1) \end{cases} \quad (7)$$

D is the reference divider (REFDIV bit of XO_RCO_CONFIG0 register)

Reference divider

$$D = \begin{cases} 1 \; if \; REFDIV = 0 \; (\textbf{internal reference divider is disabled}) \\ 2 \; if \; REFDIV = 1 \; (\textbf{internal reference divider is enabled}) \end{cases} \quad (8)$$

The resolution in the programmed value of the base frequency depends on the actual band selected.

Table 31. **Resolution frequency**

fxo [MHz]	High band resolution [Hz]	Low band resolution [Hz]
26	12.4	6.2

The f_c is the frequency related to the channel specified. RF channels can be defined using the CHSPACE and CHNUM registers. In this way, it is possible to change faster the channel by changing just an 8-bits register, allowing the setting of 256 channels and frequency-hopping sequences. The actual channel spacing is from 793 Hz to 202342 Hz in 793 Hz steps for the 26 MHz configuration and from 1587 to 404685 Hz in 1587 Hz steps for the 52 MHz configuration.

Table 32. **Channel spacing resolution**

fxo [MHz]	Channel spacing resolution [Hz]
26	793.45

4.4 Digital modulator

The S2-LPS supports frequency modulation: 2-FSK, 4-FSK, 2-GFSK, 4-GFSK as well amplitude modulation OOK and ASK. Using register, the user can also program an unmodulated carrier for lab test and measurement.
A special mode, direct polar modulation, allows building specific modulation scheme controlling directly the amplitude and the frequency of the carrier synthesized. The register MOD_TYPE is used to select one of the following modulation scheme.

Table 33. **Modulation scheme**

MOD_TYPE	Modulation scheme
0000b	2-FSK
0001b	4-FSK
0010b	2-GFSK
0011b	4-GFSK
0101b	ASK/OOK
0110b	Direct polar (TX only)
0111b	CW

4.4.1 Frequency modulation

For frequency modulation 2-(G)FSK and 4-(G)FSK the frequency deviation can be tuned in wide range that depends on f_{xo} (XTAL frequency) according the following formula:

Frequency deviation

$$f_{dev} = \begin{cases} \frac{f_{XO}}{2^{19}} \cdot \frac{round\left(D \cdot FDEV\_M \cdot B/8\right)}{D \cdot B} & if\ FDEV\_E = 0 \\ \frac{f_{XO}}{2^{19}} \cdot \frac{round\left(D \cdot \left(256 + FDEV\_M\right) \cdot 2^{(FDEV\_E - 1)} \cdot B/8\right)}{D \cdot B} & if\ FDEV\_E > 0 \end{cases} \quad (9)$$

Where f_{xo} is the XTAL oscillation frequency, D is the reference divider and B is the band selector.

The frequency deviation programmed corresponds to the deviation of the outer constellation symbols. The deviation of the inner symbols is 1/3 of such programmed values, as reported in the table below, where 4 options are available.

Furthermore, since the payload is normally arranged in bytes, the arrangement can change the mapping for both 2-(G)FSK and 4-(G)FSK modulations, by using the CONST_MAP (register MOD1), in the following way:

Table 34. Constellation mapping 2-(G)FSK

Format	Symbol	CONST_MAP coding			
		0	1	2	3
2-(G)FSK	0	-FDEV	NA	+FDEV	NA
	1	+FDEV	NA	-FDEV	NA

Table 35. Constellation mapping 4-(G)FSK

Format	Symbol	CONST_MAP coding			
		0	1	2	3
4-(G)FSK	00	-FDEV/3	-FDEV	+FDEV/3	+FDEV
	01	-FDEV	-FDEV/3	+FDEV	+FDEV/3
	10	+FDEV/3	+FDEV	-FDEV/3	-FDEV
	11	+FDEV	+FDEV/3	-FDEV	-FDEV/3

Furthermore, in the 4-(G)FSK it is also possible to swap the symbols using the 4FSK_SYM_SWAP field (register PCKTCTRL3) as follows:

(10)

$$\text{When 4FSK\_SYM\_SWAP} = 0: \begin{cases} S0 = < b7b6 > \\ S1 = < b5b4 > \\ S2 = < b3b2 > \\ S3 = < b1b0 > \end{cases}$$

$$\text{When 4FSK\_SYM\_SWAP} = 1 \begin{cases} S0 = < b6b7 > \\ S1 = < b4b5 > \\ S2 = < b2b3 > \\ S3 = < b0b1 > \end{cases}$$

4.4.1.1 *Gaussian shaping*

In 2-GFSK or 4-GFSK mode, the Gaussian filter BT product can be set by using the register BT_SEL to 1 or 0.5.

The Gaussian filtering is implemented by poly-phase filtering with eight taps per symbol time. In order to further smooth the filter shape and improve spectral shaping, the output of the filter can be linearly interpolated by setting the register MOD_INTERP_EN.

A mathematical interpolation factor is applied at each sample of the Gaussian filter output. This factor is 64 for data rates corresponding to DATA_RATE_E < 5, it is automatically scaled as $\frac{64}{2^{DATA\_RATE\_E-5}}$ for 5 ≤ DATA_RATE_E < 11 and it is automatically disabled for DATA_RATE_E = 11.

Note: The actual interpolation factor achieved may be limited by the minimal frequency resolution of the frequency synthesizer.

4.4.1.2 *ISI cancellation 4-(G)FSK*

Since the 4-(G)FSK modulation format strongly suffers from the effect of inter symbol interference, an ISI cancellation equalizer has been introduced in the demodulator. An equalizer can be enabled, by using the EQU_CTRL register, with two modes: single pass equalization and dual pass equalization. The best performance is normally achieved using the dual pass equalizer.

4.4.2 Amplitude modulation

Amplitude modulation OOK and ASK are both supported by the S2-LPS. The ASK selection depends on power ramping enable.

When OOK is selected, a bit '1' is transmitted with a programmed power, set by register PA_POWER[PA_LEVEL_MAX_INDEX], and a bit '0' is transmitted without output power (PA off) and specified by the register PA_POWER[0].

In case PA_POWER[0] = 0 then the modulation will be OOK, otherwise when PA_POWER[0] is not set to zero the modulation will be ASK. The 0/1 mapping can be reversed by setting the CONST_MAP register to any value other than zero.

When ASK is selected, a bit '1' is transmitted with a power ramp increasing from the minimum value specified by register PA_POWER[0] to specified PA maximum level in register PA_POWER[PA_LEVEL_MAX_INDEX], vice versa for a bit '0'. The duration of each power step is a multiple of 1/8 of the symbol time, configurable with the register PA_RAMP_STEP_WIDTH. If more '1's are transmitted consecutively, the PA power maintains the output power at the programmed value. If more '0's are transmitted consecutively, the PA power remains at minimum power for all '0's following the first one.

In order to improve the spectral emission mask is ASK a digital interpolation optional features have been implemented. When this feature is enabled, thought the register PA_INTERP_EN, the modulator linearly interpolates the power values specified in the PA_POWER registers before being applied to the PA.

The interpolation factor of each ramp step is 64 time the data rate corresponding to DATA_RATE_E < 5 it is automatically scaled as $64/2^{(DATA\_RATE\_E-5)}$ for 5 ≤ DATA_RATE_E < 11 and it is automatically disabled for DATA_RATE_E=11.

Note that the number of clock cycles between successive PA ticks, for DATA_RATE_E≥5, is always between 8 and 4 (8 for DATA_RATE_M=0; 4 for DATA_RATE_M=65535).

OOK/ASK demodulation is controlled by the OOK_PEAK_DECAY parameter (recommended value is 3) in the RSSI_FLT register.

4.4.2.1 *OOK smoothing*

The OOK can be smoothed using a FIR filter added in the data path. This feature is activated by setting the FIR_EN bit at 1 inside register PA_CONFIG1.

The FIR filter is not fully customizable but it can be set in 3 different configurations that change the spectrum shape (and thus the bandwidth):

- **filter**: it is the proper FIR filtering function of the stream of bits 8 times oversampled;
- **ramp**: the FIR filter is optimized to perform a ramping between PA_POWER_MAX and PA_POWER_0 (for OOK should be set to 0).
- **switch**: logic 1s and 0s are associated with a single value of power and no transition between the 2 is envisaged.

When the FIR_EN bit is 1, the DIG_SMOOTH_EN (PA_POWER_0 register) must be set to 1.

Finally, a 2nd order Bessel analog filter can be used to smooth the output signal. The bandwidth of this filter should be set according to the data rate used by setting the PA_FC field of the register PA_CONFIG0 according to the following table:

Table 36. PA Bessel filter words

PA_FC bits	Cut-off frequency (kHz)	Max. data rate (kbit/s)
00	12.5	16
01	25	32
10	50	62.5
11	100	125

Note: The FIR ramping modes are used in a mutually exclusive way with the digital ramping. When the digital ramping is used, the FIR ramping should be disabled. Vice versa, if the FIR ramping is used, the digital one is not used.

4.4.3 Direct polar mode

The S2-LPS allows the user to drive the SYNTH and the PA at a very low level. The byte couples written in the TX_FIFO are sampled with a rate related to the DATARATE chip setting (sampling rate = 8*DATARATE).

The first byte of the couple drives the frequency synthesizer to obtain an instantaneous output frequency deviation given by the formula below:

Frequency deviation in polar mode

$$fdev = fdev\_programmed * \frac{fdev\_fifo\_sample}{128} \quad (11)$$

Where $fdev\_programmed$ is the frequency deviation programmed in the chip by the registers MOD[1:0] (see Section 4.4.1 Frequency modulation), $fdev\_fifo\_sample$ is the first byte of the bytes couple sampled from the TX_FIFO.

The $fdev\_fifo\_sample$ is interpreted as a 2-complement 8-bit number, thus it can be either a positive or a negative value.

The instantaneous frequency is given by the formula:

Instantaneous frequency in polar mode

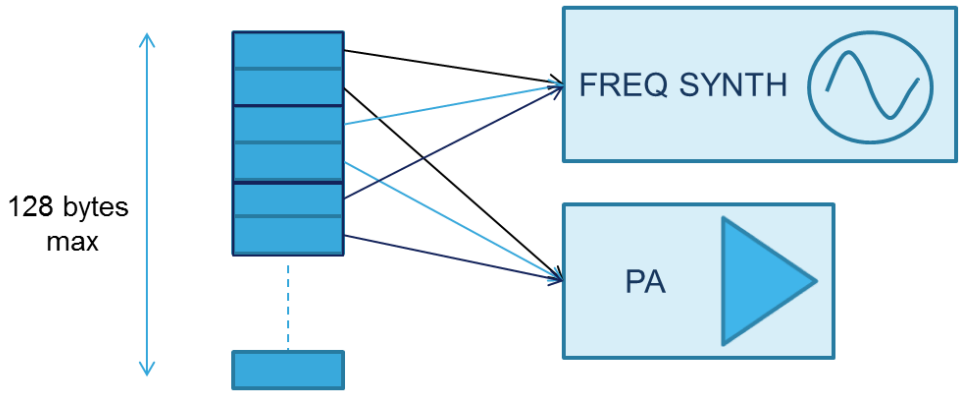
$$f = fc\_programmed + fdev \quad (12)$$

The second byte of the TX_FIFO couple drives the PA giving an instantaneous output power.

The output power will be generated according to this value following the same code as the PA_POWER registers (see Section 4.4.6.1 PA configuration).

Figure 9. Direct polar mode shows how the byte couples are sampled from the TX FIFO and sent to the SYNTH and PA blocks.

Figure 9. Direct polar mode



As for the normal TX operations, the TX_FIFO samples are consumed and a management of the TX_FIFO_THRESHOLD is needed to perform transmissions longer than 128 samples.

The transmission is never automatically stopped and a specific command SABORT should be given to terminate it.

4.4.4 Test modes

4.4.4.1 *Continuous wave*

The device can be programmed to generate a continuous wave carrier without any modulation. In this way, the carrier will be continuously transmitted until a SABORT command is sent to the device.

To set the continuous wave the MOD_TYPE field (of the MOD2 register) must be set to 0x77.

4.4.4.2 *PN9*

It is possible to set a pseudo random binary sequence 9 (PN9) as data source for the modulator. In this way, these data are continuously modulated until a SABORT command is sent to the device.

The TXSOURCE field (of the PCKTCTRL1 register) must be set to 0x03.

4.4.4.3 *Data rate*

The data rate programmable is from 0.1 kbps to 500 kbps (see Table 12. General characteristics) for further details).

The data rate formula that relates the value of the DATARATE_M and DATARATE_E registers to the data rate in symbol per second is the following:

Data rate formula

$$DataRate = \begin{cases} f_{dig} \cdot \frac{DATARATE\_M}{2^{32}} & if\ DATARATE\_E = 0 \\ f_{dig} \cdot \frac{\left(2^{16} + DATARATE\_M\right) \cdot 2^{DATARATE\_E}}{2^{33}} & if\ DATARATE\_E > 0 \\ \frac{f_{dig}}{8 \cdot DATARATE\_M} & if\ DATARATE\_E = 15 \end{cases} \quad (13)$$

where f_{dig} is the digital clock frequency.

In the cases where DATARATE_E<15, the actual modulator timing is generated by a fractional clock divider hence is affected by a certain amount of jitter. In order to have a jitter free data rate generation a specific mode the last equation must be used, DATARATE_E = 15 (for transmission only).

4.4.5 Receiver

The S2-LPS contains a low-power low-IF receiver able to amplify the input signal and provide it to the ADC with a proper signal to noise ratio. The RF antenna signal is converted to a differential one by an external balun, which performs an impedance transformation also. The receiver gain can be programmed to accommodate the ADC input signal within its dynamic range. After the down-conversion at IF, a first order filter is implemented to attenuate the out-of-band blockers.

4.4.5.1 Automatic frequency compensation

The automatic frequency compensation (AFC for short) algorithm allows compensating, within certain limits, a relative frequency error between the transmitting device and the receiving one caused by for example from crystal inaccuracies.

The AFC algorithm is operational only for frequency modulation such as 2-(G)FSK and 4-(G)FSK.

Due to the demodulation algorithm employed, any frequency error results in a DC offset in the demodulated signal before slicing.

The basic operating principle of the AFC is that the minimum and maximum signal frequencies are detected and a correction is calculated to remove the aforementioned offset.

Such correction is either applied at the slicer level in the form of offset compensation (default mode) or, optionally, is used to adjust the second IF conversion stage frequency. The former mode allows a quick recovery of the frequency error but does not prevent part of the received signal power to be cut by the channel filter; the latter mode adjusts the signal frequency before entering the channel filter thus avoiding power loss but requires a longer period to settle. The first mode is recommended for normal operation.

The AFC also provides the estimated frequency error through the AFC_CORR register. If the frequency error is known to be constant (for example communication always occurs between the same pair of devices), this value can directly be used to correct the programmed center frequency.

In order to guarantee both fast lock and smooth tracking, the AFC has a fast mode and a slow mode. The AFC will start in fast mode as soon as the RSSI threshold is passed and will switch to the slow mode after a programmable period.

The AFC is controlled by the following parameters:

- RSSI threshold: this parameter sets the minimum signal power above which the AFC algorithm is started (RSSI_TH register).
- AFC fast gain log2: this parameter sets the loop gain in the fast mode (AFC0 register), the range allowed is 0..15.
- AFC slow gain log2: this parameter sets the loop gain in the slow mode (AFC0 register), the range allowed is 0..15.
- AFC fast period: this parameter sets the length of the fast period in number of samples (AFC1 register), the range allowed is 0...255. The recommended setting for this parameter is such that the fast period equals the preamble length. Since the algorithm operates typically on 2 samples per symbol, the programmed value should be twice the number of preamble symbols. If this parameter is set to 0 then the switching from fast to slow mode is controlled by the sync word detection, for example the fast gain is used before the sync detection, the slow gain is used after sync detection.
- AFC mode: this parameter sets the AFC correction mode (AFC2 register. 0b: slicer correction, 1b: 2nd IF correction).
- AFC enable: this parameter enables the AFC algorithm (AFC2 register).

4.4.5.2 *Automatic gain control*

The automatic gain control (AGC for short) algorithm is designed to keep the signal amplitude at the input of the IF ADC within a specific range by controlling the gain of the RF chain in 6 dB steps, up to a maximum attenuation of 48 dB, starting at a received signal power of about -50 dBm.

From an implementation point of view, the (peak) signal amplitude is measured in the digital domain after the primary decimation filters chain and compared to a low threshold and to a high threshold. If the amplitude is above the high threshold, the attenuation is increased sequentially until the amplitude goes below the threshold; if the amplitude is below the low threshold, the attenuation is decreased sequentially until the amplitude goes above the threshold.

The AGC algorithm is controlled by the following parameters:

High threshold: this value sets the digital signal level above which the RF attenuation is increased (AGCCTRL1 register, allowed values 0...15). The recommended setting for such parameter is 0x5.

Low thresholds: this allows a better tuning of the low thresholds in case the analog attenuation steps have a significant spread around the nominal 6 dB attenuation. The threshold actually used for each step is selected through the bits of the LOW_THRESHOLD_SEL (AGCCTRL3) register. The recommended setting for Low Threshold 0 is 0x5, recommended setting for Low Threshold 1 is 0x4. The recommended value for LOW_THRESHOLD_SEL is 0x10.

Measure time: this parameter sets the measurement interval during which the signal level is monitored before the AGC attenuation is decreased. In particular, if the signal level is below the low threshold for all the duration of such period, then the attenuation is decreased.

The actual time is $T_{AGC\ meas} = \frac{12}{f_{dig}} \cdot 2^{MEAS\_TIME}$, ranging from about 0.5 µs to about 15 ms.

For frequency modulation, the measurement time is normally set to a few µs in order to achieve fast settling of the algorithm.

For amplitude, to avoid an unstable behavior, the measure time must be larger than the duration of the longest train of ‘0’ symbols expected during the preamble/synchronization word.

The default value for such parameter is 0x2.

Hold time: this parameter sets a wait time for the algorithm to let the signal level to settle after a change in the attenuation level.

The actual time is $T_{AGC\ hold} = \frac{12}{f_{dig}} \cdot HOLD\_TIME$, ranging from about 0.5 µs to about 32 µs.

The recommended setting for such parameter is 0x0C.

AGC enable: enables the AGC algorithm.

Freeze on sync: freeze the AGC level after when the sync word has been received.

The AGC algorithm works in the following way:

- If the amplitude is above the **high threshold,** the attenuation is increased sequentially until the amplitude goes below the threshold. In this case the T_{meas} is set to 0 and only the hold time is used. Thus, if the signal is above the high threshold, the AGC word is changed each T_{hold} seconds.
- If the amplitude is below the **low threshold,** the attenuation is decreased sequentially until the amplitude goes above the threshold. In this case the T_{meas} is set to the value: T_{hold} = (12*2MEAS_TIME)/f_{dig}. Thus, if the signal is below the low threshold, the AGC word is changed each T_{meas} + T_{hold} seconds.

The two operations are repeated in a loop until the input signal strength is between the high and the low threshold.

4.4.5.3 *Symbol timing recovery*

The S2-LPS supports two different algorithms for the timing recovery. The selection of the algorithm is done with the register CLOCK_REC_ALGO_SEL.

- If CLOCK_REC_ALGO_SEL = 0, then a simple first order algorithm is used (shortly referred to as DLL).
- If CLOCK_REC_ALGO_SEL = 1, then a second order algorithm is used (shortly referred to as PLL).

Besides the configuration parameters mentioned above, the setting of the following registers also affects the behavior of the clock recovery algorithms.

- Post-filter length: this parameter controls the length of the demodulator post-filter (CLOCKREC register). Setting this value to 1B may improve demodulation performance but requires a slower recovery. The recommended value for such parameter is 0B.

- RSSI threshold: this parameter sets the minimum signal power above which the timing recovery is started (RSSI_TH register).

4.4.5.3.1 DLL mode

The DLL algorithm, being based on a first order loop, is only able to control the delay of the local bit-timing generator in order to align it to the received bit period. If there is an error between the actual received bit period and the nominal one, the relative edges will drift over time and the algorithm will periodically apply a delay correction to recover. Since in presence of long sequences of zeroes or ones it is not possible to estimate any timing error, the loop tends to lose lock if the period error is large (greater than 3%).

The convergence speed of the loop is controlled by the CLK_REC_P_GAIN_FAST/SLOW parameter (KP) in the CLOCKREC1 and CLOCKREC2 registers with a smaller value yielding a faster loop. Allowed values for KP are from 0 to 7. The optimal values obtained for all modulations and data rates are KP = 1 or KP = 2.

4.4.5.3.2 PLL mode

The PLL algorithm tracks the phase error of the local timing generator relative to received bit period and controls both frequency and phase to achieve the timing lock. Once that the relative period error has been estimated and corrected for example during the preamble phase, then even in presence of long sequences of zeroes or ones, the loop is able to keep lock.

In order to improve the performance of the algorithm, two sets of gain coefficients can be configured to be used before and after the sync word detection.

In particular, CLK_REC_I_GAIN_FAST and CLK_REC_P_GAIN_FAST are used before the SYNC while CLK_REC_I_GAIN_SLOW and CLK_REC_P_GAIN_SLOW are used after the SYNC detection.

4.4.5.4 RX channel filter bandwidth

The bandwidth of the receiver channel filter is programmable from 1 kHz to 800 kHz. The setting goes through the register CHFLT according to the following table.

Table 37. Channel filter words

	E=0	E=1	E=2	E=3	E=4	E=5	E=6	E=7	E=8	E=9
M=0	800.1	450.9	224.7	112.3	56.1	28.0	14.0	7.0	3.5	1.8
M=1	795.1	425.9	212.4	106.2	53.0	26.5	13.3	6.6	3.3	1.7
M=2	768.4	403.2	201.1	100.5	50.2	25.1	12.6	6.3	3.1	1.6
M=3	736.8	380.8	190.0	95.0	47.4	23.7	11.9	5.9	3.0	1.5
M=4	705.1	362.1	180.7	90.3	45.1	22.6	11.3	5.6	2.8	1.4
M=5	670.9	341.7	170.6	85.3	42.6	21.3	10.6	5.3	2.7	1.3
M=6	642.3	325.4	162.4	81.2	40.6	20.3	10.1	5.1	2.5	1.3
M=7	586.7	294.5	147.1	73.5	36.7	18.4	9.2	4.6	2.3	1.2
M=8	541.4	270.3	135.0	67.5	33.7	16.9	8.4	4.2	2.1	1.1

The actual filter bandwidth for any digital clock frequency can be obtained by multiplying the values in the table above by the factor $\frac{f_{dig}}{26000000}$. The bandwidth values are intended as double-sided.

4.4.5.5 Intermediate frequency setting

The intermediate frequency (IF) can be tuned and be controlled by the registers IF_OFFSET_ANA and IF_OFFSET_DIG and can be set as follows:

Intermediate frequency

$$f_{IF} = \frac{f_{xo}}{12} \cdot \frac{(IF\_OFFSET\_ANA + 100)}{2^{11}} = \frac{fdig}{12} \cdot \frac{(IF\_OFFSET\_DIG + 100)}{2^{11}} \quad (14)$$

where f_{XO} is the XTAL oscillator frequency and f_{dig} is the digital clock frequency. The recommended IF value is about 300 kHz.

4.4.5.6 *RX timer management*

The programmable RX timer used can be configured using quality indicator to avoid unwanted interruption during a valid packet due to RX timer expiration. The quality indicators used to stop the RX timer are SQI, CS and PQI. More specifically, AND or OR Boolean relationships among any of them can be configured, to suit user application. In particular, it is required to include always SQI valid check, to avoid to stay in RX state for unlimited time, if timeout is stopped but no valid SQI is detected (in such cases, the RX state can be left using a SABORT command).

On timer expiration, reception aborts and the packet is discarded.

Table 38. RX timer stop condition configuration

RX_TIMEOUT_AND_OR_SELECT	CS_TIMEOUT_MASK	SQI_TIMEOUT_MASK	PQI_TIMEOUT_MASK	Description
0	0	0	0	The RX timeout never expires and the reception ends at the reception of the packet
1	0	0	0	The RX timeout cannot be stopped. It starts at the RX state and at the end expires
X	1	0	0	RSSI above threshold
X	0	1	0	SQI above threshold (default)
X	0	0	1	PQI above threshold
0	1	1	0	Both RSSI AND SQI above threshold
0	1	0	1	Both RSSI AND PQI above threshold
0	0	1	1	Both SQI AND PQI above threshold
0	1	1	1	ALL above threshold
1	1	1	0	RSSI OR SQI above threshold
1	1	0	1	RSSI OR PQI above threshold
1	0	1	1	SQI OR PQI above threshold
1	1	1	1	ANY above threshold

4.4.5.7 *Receiver data modes*

Direct modes are primarily intended to completely bypass the automatic packet handler, in order to give the user maximum flexibility in the choice of frame formats. Specifically:

- **Direct through FIFO mode**: the packet bytes are continuously received and written in the RX FIFO without any processing. It is the responsibility of the microcontroller to avoid any overflow conditions on the RX FIFO.
- **Direct through GPIO mode**: the packet bits are continuously written to one of the GPIO pins without any processing. To allow the synchronization of an external data sink, a data clock signal is also provided on one of the GPIO pins. Data are updated by the device on the falling edge of such clock signal so the MCU must read it during falling edge of CLK.

4.4.5.8 *Receiver quality indicators*

4.4.5.8.1 RSSI

The received signal strength indicator (RSSI) is a measurement of the received signal power at the antenna measured in the channel filter bandwidth. The measured RSSI is in steps of 1 dB, from 0 to 255 (1 byte value) and it is offset in such a way that the number 0 corresponds to -146 dBm, so the register value can be converted in dBm by subtracting 146. Laboratory calibration may be needed for accurate absolute power measurements. The RSSI value can be read through two registers: RSSI_LEVEL_CAPTURE and RSSI_LEVEL_RUN. In particular RSSI_LEVEL_CAPTURE reports the RSSI value captured at the end of the SYNC word detection, exit from RX state by SABORT command or RX timeout expiration, while RSSI_LEVEL_RUN is the continuous output of the RSSI filter. The last mode supports the continuous fast SPI reading that means if the CSn signal, of the SPI interface, is kept low, after the first 16 bits (S2-LP status register), then a new RSSI value will be available every 8 SPI clock cycles (this mode is the same of the SPI burst mode, but no automatic address increment).

4.4.5.8.2 Carrier sense

The carrier sense functionality can be used to detect if any RF signal is being received, the detection is based on the measured RSSI value. There are two operational modes for carrier sensing: static and dynamic carrier sensing.

When static carrier sensing is used (CS_MODE = 0), the carrier sense signal is asserted when the measured RSSI is above the value specified in the RSSI_TH register and is de-asserted when the RSSI falls 3 dB below the same threshold.

When dynamic carrier sense is used (CS_MODE = 1, 2, 3), the carrier sense signal is asserted if the signal is above the threshold and a fast power increase of 6, 12 or 18 dB is detected; it is de-asserted if a power fall of the same amplitude is detected.

The carrier sense signal is also used internally to the demodulator to start the automatic frequency compensation and timing recovery algorithms.

The carrier sense function is controlled by the following parameters:

- RSSI threshold: this parameter sets the minimum signal power above which the carrier sense signal is asserted (RSSI_TH register).
- CS mode: this parameter controls the carrier sense operational modes.

Table 39. CS mode description

CS_MODE	Description
0	Static carrier sensing
1	Dynamic carrier sensing with 6 dB dynamic threshold
2	Dynamic carrier sensing with 12 dB dynamic threshold
3	Dynamic carrier sensing with 18 dB dynamic threshold

4.4.5.8.3 PQI

The preamble quality indicator (PQI) is intended to provide a measurement of the reliability of the preamble detected. The PQI is increased by 1 every time a bit inversion occurs, while it is decreased by 4 every time a bit repetition occurs. The running peak PQI is compared to a threshold value and the preamble valid IRQ is asserted as soon as the threshold is passed. The preamble quality indicator threshold is 4 x PQI_TH (with PQI_TH = 0, 1, …15).

4.4.5.8.4 SQI

The synchronization quality indicator (SQI) is a measurement of the best correlation between the received SYNC word and the expected one. This indicator is calculated as the peak cross-correlation between the received data stream and the expected SYNC word. If the SQI_EN = 1b, the running peak SQI is compared to a threshold value and the SYNC valid IRQ is asserted as soon as the threshold is passed. The SYNC quality threshold is equal to SYNC_LEN – 2 x SQI_TH (with SQI_TH = 0, 1, …7). When SQI_TH = 0b, perfect match is required. It is recommended the SQI check always enabled. The peak SQI value can be read from the register SQI[5:0] and represents the peak value from 0 to 32, while the bit SQI[6], when equal to ‘1’ indicates that the SQI peak value refers to the secondary SYNC word.

4.4.5.9 CS blanking

The CS blanking feature prevents data to be received if the RSSI level on the air is below the RSSI threshold (set by the RSSI_TH field). The feature can be enabled through the CS_BLANKING bit in the ANT_SELECT_CONF register.

4.4.5.10 Antenna switching

The device implements a switching based antenna diversity algorithm. The antenna switching function allows controlling an external switch in order to select the antenna providing the highest measured RSSI. The switching decision is based on a comparison between the received power level on antenna 1 and antenna 2 during the preamble reception controlling through GPIO an external RF switch in order to select the antenna providing the highest measured RSSI.

When antenna switching is enabled, the two antennas are repeatedly switched during the reception of the preamble of each packet, until the carrier sense threshold is reached (static CS mode must be used). From this point on, the antenna with highest power is selected and switching is frozen. The switch control signal is available on GPIO and in the MC_STATE[1] register.

The algorithm is controlled by the following parameters:

- AS_MEAS_TIME: this register/parameter controls the time interval for RSSI measurement. The actual measurement time is done with the following formula.

Antenna switching measurement time

$$T_{meas} = \frac{24 \cdot 2^{CHFLT\_E} \cdot 2^{AS\_MEAS\_TIME}}{f_{dig}} \quad (15)$$

In case of FSK modulation, the whole T_{meas} is used to let the signal level settle after the antenna switch and one single measurement is taken at the end of such period.

In case of OOK modulation, after one first interval equal to T_{meas} again used to let the signal level settle after the antenna switch, one second interval still equal to T_{meas}, is used to perform a peak power measurement and select the best antenna.

- AS_ENABLE: this parameter enables the antenna switching function.

4.4.6 Transmitter

The S2-LPS contains an integrated PA capable of transmitting at output levels programmable between -30 dBm to +14 dBm (+16 dBm in boost mode), at step of 0.5 dB.

The PA is single-ended and has a dedicated pin (TXOUT). The PA output is ramped up and down to prevent unwanted spectral splatter. In TX mode the PA drives the signal generated by the frequency synthesizer out to the antenna terminal. Delivered power, as well as harmonic content, depends on the external impedance seen by the PA. It is possible to program TX to send an unmodulated carrier.

The output stage is supplied from the SMPS through an external choke and is loaded with a LC-type network which has the function of transforming the impedance of the antenna and filter out the harmonics. The TX and RX pins are tied directly to share the antenna. During TX, the LNA inputs are internally shorted to ground to allow for the external network resonance, so minimizing the power loss due to the RX.

4.4.6.1 PA configuration

The PA output power level is programmable in 0.5 dB steps. The user can store up to eight output levels to provide flexible PA power ramp-up and ramp-down at the start and end of a frequency modulation transmission as well as ASK modulation shaping.

With the digital power-ramping enabled (PA_RAMP_EN = 1 in the PA_POWER0 register) the ramp starts from the minimum output power programmed and stops at the programmed maximum value, thus a maximum of 8 steps can be set up as shown in Figure 10. Output power ramping configuration. The interpolation factor ranges from 64 down to 1 depending on the actual data rate. The assumption is that output power monotonically decrease. Each step is held for a programmable time interval expressed in terms of bit period units ($T_b/8$), maximum value is 3 (which means $4 \times T_b/8 = T_b/2$). Therefore, the PA ramp may last up to 4 T_b (about 3.3 ms if the bit rate is 1.2 kbit/s).

$$T_{ramp} = \frac{(PA\_RAMP\_STEP\_LEN + 1) \times (PA\_LEVEL\_MAX\_IDX + 1)}{8 \times DataRate} \quad (16)$$

where *DataRate* is the transmission data rate expressed in symbols/s.

The set of eight levels is used to shape the ASK signal. In this case, the modulator works as a counter that counts when transmitting a one and down when transmitting a zero. The counter counts at a rate equal to 8 times the symbol rate (in this case, the step width is fixed by symbol rate).

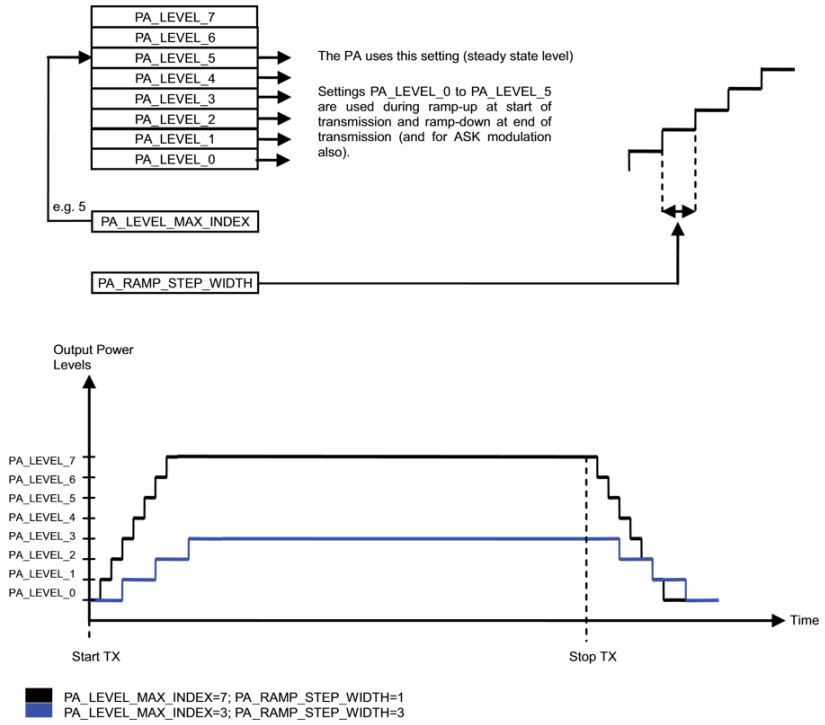
For OOK modulation, the signal is abruptly switched between two levels only: no power and maximum. This mode is obtained setting the PA_RAMP_EN=0.

With the digital power-ramping, the digital PA interpolation can be enabled through the PA_INTERP_EN field of the MOD1 register.

When this feature is enabled, the power values specified in the PA_POWER registers are linearly interpolated by the modulator before being applied to the PA.

The mathematical interpolation factor applied at each output sample is 64 for data rates corresponding to DATA_RATE_E < 5, it is then automatically scaled as $\frac{64}{2^{DATA\_RATE\_E-5}}$ and it is automatically disabled for DATA_RATE_E = 11.

Figure 10. Output power ramping configuration



4.4.6.2 *Transmitter data modes*

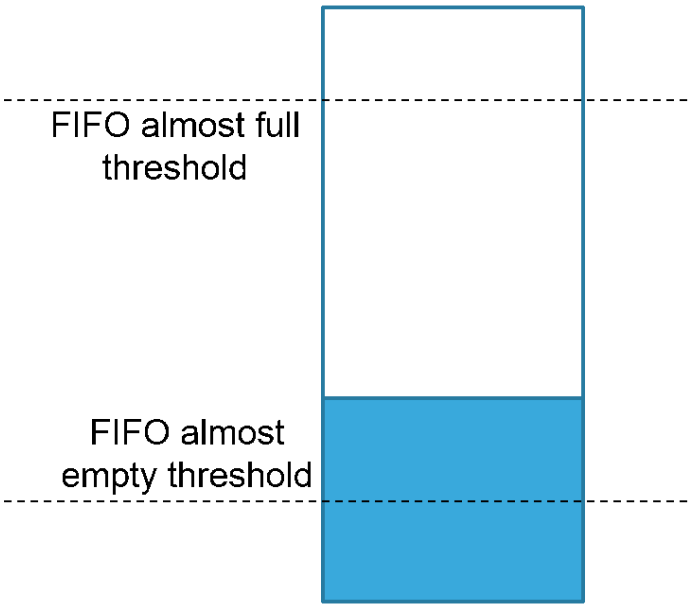
Direct modes are primarily intended to completely bypass the automatic packet handler, in order to give the user maximum flexibility in the choice of frame formats. In specific:

- **Direct through FIFO mode**: the packet is written in TX FIFO. The user build the packet according to his need including preamble, payload and soon on. The data are transmitted without any processing.
- **Direct through GPIO mode**: the packet bits are continuously read from one of the GPIO pins, properly configured, and transmitted without any processing. To allow the synchronization of an external data source, a data clock signal is also provided on one of the GPIO pins. Data are sampled by the device on the rising edge of such clock signal; it is the responsibility of the external data source to provide a stable input at this edge.
- **PN9 mode**: a pseudo-random binary sequence is generated internally. This mode is provided for test purposes only.

4.4.6.3 *Data FIFO*

In the S2-LPS there are two data FIFOs, a TX FIFO for data to be transmitted and an RX FIFO for the received data both of 128 bytes. The SPI interface is used to read from the RX FIFO and write to the TX FIFO starting from the address 0xFF.

Figure 11. Threshold in FIFO



The TX FIFO has two programmable thresholds (see figure above). An interrupt event occurs when the data in the TX FIFO reaches any of these thresholds. The first threshold is the “FIFO Almost Full” threshold, TX_AF_THR registers. The value in this field corresponds to the desired threshold value in number of bytes + 2. When empty locations (free) amount inside the TX FIFO reaches this threshold limit, an interrupt to the MCU is generated so it can send a TX command to transmit the contents of the TX FIFO. The second threshold for TX is the “FIFO Almost Empty” threshold, TX_AE_THR register. When the data being shifted out of the TX FIFO reaches the Almost Empty threshold, an interrupt will be generated also. The MCU could to switch out of TX mode or fill new data into the TX FIFO.

The RX FIFO has two programmable thresholds (see figure above). The first threshold is the “FIFO Almost Full” threshold, RX_AF_THR0 registers. The value in this register corresponds to the desired threshold value in number of bytes. When empty locations (free) amount inside the RX FIFO reaches this threshold limit, an interrupt will be generated to the MCU. The MCU should then start to read the data from the RX FIFO. The second threshold for RX is the “FIFO Almost Empty” threshold, RX_AE_THR register. When the data being shifted out of the RX FIFO reaches the Almost Empty threshold, an interrupt will be generated also. The MCU will need to switch on RX mode to fill with new data the RX FIFO or stop to read after the number of byte indicated by the RX_AE_THR register.

In order to enable the RX_FIFO thresholds interrupts, the bit FIFO_GPIO_OUT_MUX_SEL (PROTOCOL2 register) must be set to 1. To enable the TX_FIFO thresholds interrupts the FIFO_GPIO_OUT_MUX_SEL must be set to 0.

The FIFO controller detects overflow or underflow in the RX FIFO and overflow or underflow in the TX FIFO. It is the responsibility of the MCU to avoid TX FIFO overflow since the MCU only can decide to writing on the TX FIFO. A TX FIFO overflow results in an error in the TX FIFO content, while an underflow results in the continuous transmission of the last byte stored in the TX FIFO. Likewise, when reading the RX FIFO the MCU must avoid reading the RX FIFO after its empty condition is reached, since a RX FIFO underflow will result in an error in the data read out of the RX FIFO.

When an overflow or an underflow is detected, the MCU has to issue a SABORT and a FLUSHTXFIFO/ FLUSHRXFIFO command before resuming the normal transceiver activity. For each FIFO, when one of these errors is detected an interrupt is generated to the MCU.

The TX FIFO may be flushed by issuing a FLUSHTXFIFO command (see Table 42. Commands). Similarly, a FLUSHRXFIFO command flushes the RX FIFO.

The full / empty status of the TX / RX FIFO is readable on the bits [9:8] of the MC_STATE registers, and at the same time, the related IRQs are generated.

In the SLEEP state, the FIFO content is retained only if the SLEEP_B mode is selected (bit SLEEP_MODE_SEL=1 in the register 0x79).

4.4.7 Integrated RCO

The S2-LPS contains an ultra-low power RC oscillator with accuracy better than 1%. The RC oscillator frequency is calibrated using as a reference the XO frequency. It depends on two values: raw (4 bits) and fine (5 bits). The raw value is obtained by a linear search algorithm in which for each value a counting of half clock reference inside the period of RCO is done. When the correction is near to the final value, a dichotomy search algorithm starts.

The RCO calibration starts as soon as the RCO_CALIBRATION bit is set to 1. When it finishes, the RC_CAL_OK bit is set and the ERROR_LOCK bit is reset.

Moreover, after a sleep or standby state, if the RCO_CALIBRATION bit is kept to 1, when the device returns to the ready state, an RCO calibration automatically runs to compensate some drift.

It is possible to perform an offline calibration of the RCO using the following procedure:

1. Enable the RCO CALIB setting the bit to 1
2. Wait until the RC_CAL_OK becomes 1
3. Copy the RWT_OUT and RFB_OUT (registers 0x94 and 0x95) out values in the RWT_IN and RFB_IN fields (registers 0x6E and 0x6F)
4. Disable the RCO CALIB setting the bit to 0

In this way, the RCO works with these values. It is advisable to repeat the RCO calibration to reject effects related to the variation of temperature. It is recommended to use this procedure if the following SLEEP time (i.e. when using LDC mode) is shorter or comparable to the calibration time.

By default, the calibration is disabled at reset to avoid using an out-of-range reference frequency, after the internal clock divider is correctly configured, the user can enable the RCO calibration by register.

Once calibrated, the RCO generates a clock frequency that depends on the XO frequency used:

Table 40. RCO Frequency

Ref. frequency [MHz]	RCO frequency [kHz]
24 or 48	32
25 or 50	33.33
26 or 52	34.66

4.4.8 Low battery indicator

The battery indicator can provide the user with an indication of the battery voltage level.

There are two blocks to detect battery level:

- Brownout with a fixed threshold
- Battery level detector with a programmable threshold

The MCU enables optionally these blocks to provide an early warning of impending power failure. It does not reset the system, but gives the MCU time to prepare for an orderly power-down and provides hardware protection of data stored in the program memory.

The low battery indicator function is available in any of the S2-LPS operation modes. As this function requires the internal bias circuit operation, the overall current consumption in STANDBY, SLEEP, and READY modes increase by 400 µA.

4.4.9 Voltage reference

This block provides the precise reference voltage needed by the internal circuit.

5 Operating modes

The S2-LPS is provided with a built-in main controller which controls the switching between the two main operating modes: transmitter (TX) and receiver (RX), driven by SPI commands.

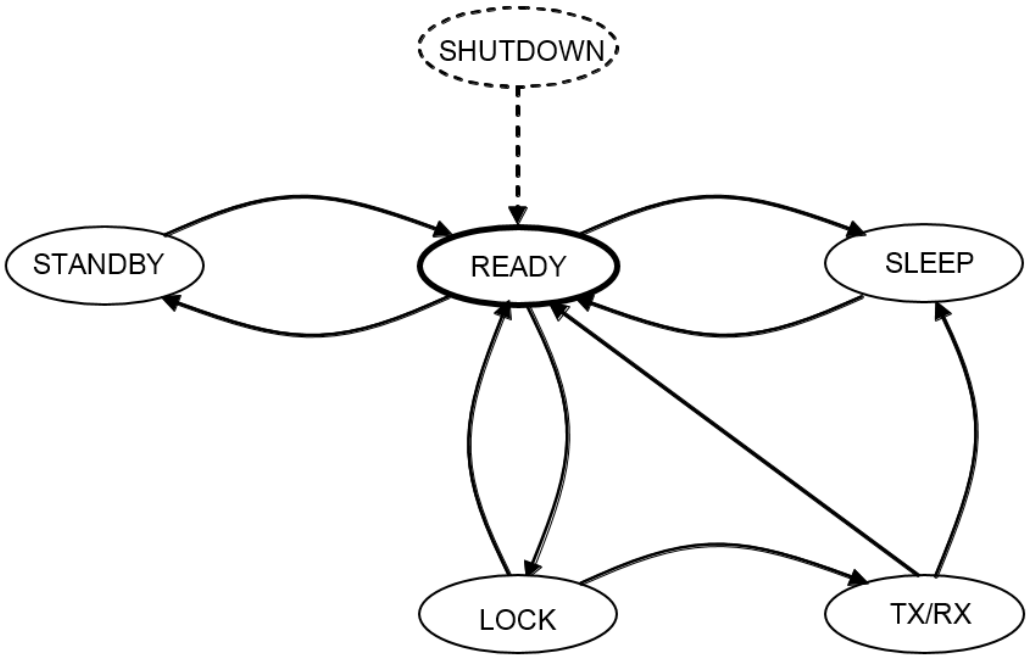
In shutdown condition (the S2-LPS can be switched on/off with the external pin SDN), no internal supply is generated, and all stored data and configurations are lost.

From shutdown, the S2-LPS can be switched on going to READY state, where the reference clock signal is available.

From READY state, the S2-LPS can be moved to LOCK state to generate the high precision LO signal and then in TX or RX modes. Switching from RX to TX and vice versa can happen only by passing through the LOCK state. This operation is managed by the main controller through a single user command (TX or RX). At the end of the operations, the S2-LPS can return to READY state or can go to SLEEP state, having a very low power consumption.

SLEEP state can be configured to retain the FIFOs content or not enabling very low power mode. If also no wake-up timer is required, the S2-LPS can be moved from READY to STANDBY state, which has the lowest possible current consumption.

Figure 12. State diagram



Three states: READY, STANDBY and LOCK may be defined as stable state.

All other states are transient, which means that, in a typical configuration, the controller remains in those states, at most for any timeout timer duration. Also the READY and LOCK states behave as transients when they are not directly accessed with the specific commands (for example, when LOCK is temporarily used before reaching the TX or RX states).

Table 41. States

State code(1)	State name	Digital LDO	SPI	XTAL	RF synth.	Wake-up timer
NA	SHUTDOWN	OFF	Off	Off	Off	Off
0x02	STANDBY	ON	On	Off	Off	Off

State code(1)	State name	Digital LDO	SPI	XTAL	RF synth.	Wake-up timer
0x01	SLEEP_A		On	Off	Off	On
0x03	SLEEP_B		On	Off	Off	On
0x00	READY		On	On	Off	Do not care
0x0C	LOCK		On	On	On	Do not care
0x30	RX		On	On	On	Do not care
0x5C	TX		On	On	On	Do not care
0x50	SYNTH_SETUP		On	On	On	Do not care

1. *Other codes are invalid and are an indication of an error condition due to bad register configuration and/or hardware issue in the application board hosting.*

Commands are used in the S2-LPS to change the operating mode and to use its functionality. A command is sent on the SPI interface and may be followed by any other SPI access without pulling CSn high. A command code is the second byte to be sent on the MOSI pin (the first byte must be 0x80). The commands are immediately valid after SPI transfer completion (no need for any CSn positive edge).

5.1 Command list

Table 42. Commands

Command code	Command name	State for execution	Description
0x60	TX	READY	Send the S2-LPS to TX state for transmission
0x61	RX	READY	Send the S2-LPS to RX state for reception
0x62	READY	STANDBY, SLEEP, LOCK	Go to READY state
0x63	STANDBY	READY	Go to STANDBY state
0x64	SLEEP	READY	Go to SLEEP state
0x65	LOCKRX	READY	Go to LOCK state by using the RX configuration of the synthesizer
0x66	LOCKTX	READY	Go to LOCK state by using the TX configuration of the synthesizer
0x67	SABORT	TX, RX	Exit from TX or RX states and go to READY state
0x68	LDC_RELOAD	ANY	Reload the LDC timer with a pre-programmed value stored in registers
0x70	SRES	ANY	Reset the S2-LPS state machine and registers values
0x71	FLUSHRXFIFO	All	Clean the RX FIFO
0x72	FLUSHTXFIFO	All	Clean the TX FIFO
0x73	SEQUENCE_UPDA TE	ANY	Reload the packet sequence counter with the value stored in register

5.2 State transaction response time

Table 43. Response time

Initial state	Final state	Response time [µs]
SHUTDOWN	READY	500

Initial state	Final state	Response time [µs]
READY	STANDBY/ SLEEP	3
READY	LOCK with no VCO calibration	70
READY	LOCK with VCO calibration	85
RX/TX	READY	1
STANDBY/SLEEP	READY	100
LOCK	RX/TX	26

Note: The transition time enables the S2-LPS for frequency hopping operation due to its reduced response time and very quick programming synthesizer. The response time depends on frequency of the clock in digital domain, from 24 MHz to 26 MHz.

Note: The first bit of preramble is sent after TX state is reached, if PA ramping is not enabled. If PA ramping is enabled, the first bit is sent after tramp (see Section 4.4.6.1 PA configuration).

5.3 Sleep states

S2-LPS provides 2 SLEEP states:

- SLEEP without FIFO retention (SLEEP_A): in this low power state, the device keeps all the register values but not the TX and RX FIFOs. This is the device default SLEEP state.
- SLEEP with FIFO retention (SLEEP_B): in this low power state, the device keeps the content of the registers and the two FIFOs.

The responsibility of the SLEEP type to be used is demanded to the user. To select the SLEEP mode, the bit SLEEP_MODE_SEL (register 0x79) can be used. If this bit is set to 0, SLEEP_A is used each time the device enters SLEEP (by SPI command, LDC flow in non-persistent mode). If it is 1, SLEEP_B is used instead.

6 Packet handler engine

The S2-LPS offers a highly flexible and fully programmable packet handler (framer and de-framer) that build the packet according to the user configuration settings. The packet types are available: BASIC format, and UART over the air packet format.

WMBUS format is supported but it can be obtained using the proper features combination.

The RX packet handler is in charge of treating the raw bits produced by the demodulator. The main functions of the RX packet handler are:

- Detect a valid preamble
- Detect a valid synchronization word and start-of-frame
- Extract all packet fields according to the selected packet format
- Calculate the local CRC and compare to the received one

The device supports 2 different packet formats. The current packet format is set by the PCK_FRMT field of the PCKTCTRL3 register.

In particular:

- 0: Basic packet format
- 2: UART over the air packet format

6.1 BASIC packet format

The packet format BASIC is selected by writing 0b in the register PCK_FRMT. The packet frame is as follows:

Table 44. BASIC packet format

Preamble	Sync	Length	Address	Payload	CRC	Postamble
0:2046 bits	0:32 bits	0:2 bytes	0:1 bytes	0:65535 bytes	0:4 bytes	0:510 bits

- **Preamble**: each preamble is a pair of ‘01’ or ‘10’ from 0 pair to 1023 pairs, programmed by the register PREAMBLE_LENGTH. The binary sequences transmitted in the various modulation modes are summarized in the following table (leftmost bit is transmitted first).

Table 45. Preamble field selection

PREAMBLE_SEL	2(G)FSK or OOK/ASK
0	0101
1	1010
2	1100
3	0011

- **Sync**: the pattern that identify the start of the frame can be configured in value with a programmable length from 0 to 32 bits, in steps of 1-bit length. The setting is done by the register SYNC_LENGTH. The S2LP supports dual synchronization with a either a primary or a secondary synchronization word. The binary content of the primary SYNC word is programmable through registers SYNCx (x= 0, 1, 2, 3). The binary content of the secondary SYNC word is programmable through registers SEC_SYNCx (x= 0, 1, 2, 3), note that such registers are in alternate use with address filtering registers. On the transmitter side either the primary or the secondary word is transmitted according to the value of the SECONDARY_SYNC_SEL register, in particular if SECONDARY_SYNC_SEL = 0 then the primary synchronization word is transmitted; if SECONDARY_SYNC_SEL = 1 then the secondary synchronization word is transmitted. On the receiver side, the primary synchronization word is always enabled. The search for the secondary synchronization word can be enabled setting SECONDARY_SYNC_SEL = 1b. In this case, both the binary patterns are searched for and both of them can trigger the start of payload demodulation. The SQI[5:0] value reported in the LINQ_QUALIF register is the maximum between the SQI of the primary and secondary words. The bit SQI[6] indicates which synchronization word has been detected: in particular, if the secondary synchronization word has been detected then the SQI[6] = 1b otherwise if the primary synchronization word has been detected then SQI[6] = 0b. The binary pattern programmed in SYNCx (or SEC_SYNCx) is transmitted on air starting with the most significant bit of x = 1, to the least significant bit of x = 4 according to the programmed synchronization word length.
- **Length**: The device supports both fixed and variable packet length transmission from 0 to 65535 bytes. On the transmitting device, the packet length is always set by using the two registers PCKTLENx (x= 1, 2) as: PCKTLEN1 × 256 + PCKTLEN0. On the receiving device, if FIX_VAR_LEN register is set to '1', the packet length is directly extracted from the field Length of the received packet itself. If the register FIX_VAR_LEN = 0b the Length field of the received packet is not used, because is already known from the registers PCKTLENx (x= 1, 2) as for the transmitter. For the basic and stack packet formats, the number of address bytes is also counted in the packet length value. CRC is excluded. Furthermore, when variable packet length is used (FIX_VAR_LEN=1b), the width of the binary field transmitted, must be configured through the LEN_WID register in the following way:
  - If the packet length is from 0 to 255 bytes (payload + address field), then LEN_WID = 0b (1 byte length field transmitted).
  - If the packet length is from 0 to 65535 bytes (payload + address field), then LEN_WID = 1b (2 bytes length field transmitted).
- **Destination address**: can be enabled or no by the register ADDRESS_LEN. If enabled, ADDRESS_LEN=1b, its size is 1 byte. The destination address field is read from the register RX_SOURCE_ADDR (TX only). The receiver uses this field to perform automatic filtering on its value programmed in TX_SOURCE_ADDR (RX only).
- **Payload**: the main data from transmitter with a max length up to 65535 supported by the embedded automatic packet handler.
- **CRC**: can optionally be calculated on the transmitted data (Length field, Address field and Payload) and appended at the end of the payload (see Section 6.5.1 CRC).
- **Postamble**: The packet postamble allows inserting a certain number of '01' bit pairs at the end of the data packet. The number of postamble bit pairs can be set through the MBUS_PSTMBL register.

6.2 UART over the air packet format

Table 46. UART over the air packet format

Preamble	Sync	Payload
0:2046 bits	0:32 bits	0:65535 bytes

When this format is selected, a start bit and a stop bit can be programmed to be added to each byte of the TX FIFO. Such start and stop bits are automatically removed from the received payload before written to the RX FIFO. Start and stop bits are not added to the SYNC word.

Also, the BYTE_SWAP bit can be set in order to send the FIFO bytes in LSbit first (default is indeed MSbit first).

The actual binary value of the start and stop bit can be set through the START_BIT and the STOP_BIT fields of the PCKTCTRL2 register.

6.3 Wireless MBUS packet (W-MBUS, EN13757-4)

The W-MBUS packet structure referred to EN13757 can be obtained through registers setting programming the basic packet to fit the specific sub-mode used.

Preamble	Sync	1st block	2nd block	Opt. blocks	Postamble

Preamble: the preamble is fully programmable to fit the W-MBUS protocol. The generic setting is a pair of '01' or '10' from 1 pair to 1024 pairs (max. 256 bytes).

Sync: the pattern that identify the start of the frame is fully programmable to fit the W-MBUS protocol. The generic setting is in value with a programmable length from 1 bit to 64 bytes, in steps of 1-bit length.

Data blocks: the data coding can be fully programmed in NRZ and Manchester.

Postamble: The packet postamble allows inserting a certain number of '01' bit pairs at the end of the data packet. The number of postamble bit pairs can be set through the MBUS_PSTMBL register depending on the chosen sub-mode according to the W-MBUS protocol.

6.4 Payload transmission order

The bit order of the data from TX FIFO and written into the RX FIFO is controlled by the BYTE_SWAP register. In particular, the transmission is MSB first if BYTE_SWAP = 0 and LSB first if BYTE_SWAP = 1.

6.5 Automatic packet filtering

The receiver uses the following filtering criteria to reject the received packet. The automatic filtering is supported in BASIC and STack packet format only.

- **CRC**: the received packet is discarded if CRC check fails. Both transmitter and receiver must be configured with same CRC polynomial.
- **Destination address vs my address**: the received packet is discarded if the destination address field received does not match the programmed my address of the receiver.
- **Destination address vs. broadcast address**: the received packet is discarded if the destination address field received does not match the programmed broadcast address of the receiver.
- **Destination address vs. multicast address**: the received packet is discarded if the destination address field received does not match the programmed multicast address of the receiver.
- **Source address**: the received packet is discarded if the source address received does not match the programmed source address reference (a bit mask can be included). Supported in STack packet format only.

The automatic filtering can be programmed to discard packet below certain threshold settings. These kind of filtering are general purpose and can be used with any packet format.

- **Carrier sense**: The carrier sense (CS) functionality detects if any signal is being received, the detection is based on the measured RSSI value. There are 2 operational modes for carrier sensing: static and dynamic. In static CS mode, the CS is high when the measured RSSI is above the RSSI threshold specified and is low when the RSSI is 3 dB below the threshold. In dynamic CS mode, the CS is high if the signal is above the threshold and a fast power increase of 6, 12, or 18 dB is detected. The CS is also used internally for the demodulator to start the AFC and timing recovery algorithms (static CS mode only).
- **PQI**: It is possible to set a PQI threshold in such a way that, if PQI is below the threshold, the packet demodulation is automatically aborted.
- **SQI**: It is possible to set a SQI threshold in such a way that, if SQI is below the threshold, the packet demodulation is automatically aborted. When the SQI threshold is set at 0, a perfect match is required. It is recommended to always enable the SQI check.

6.5.1 CRC

Error detection is implemented by means of cyclic redundancy check codes. The CRC is calculated over all fields excluding preamble and SYNC word. The length of the checksum is programmable to 8, 16, 24 or 32 bits. The following standard CRC polynomials can be selected:

- mode 1: 8 bits: the poly is (0x07) X^8+X^2+X+1

- mode 2: 16 bits: the poly is (0x8005) $X^{16}+X^{15}+X^{2}+1$
- mode 3: 16 bits: the poly is (0x1021) $X^{16}+X^{12}+X^{5}+1$
- mode 4: 24 bits: the poly is (0x864CFB) $X^{24}+X^{23}+X^{18}+X^{17}+X^{14}+X^{11}+X^{10}+X^{7}+X^{6}+X^{5}+X^{4}+X^{3}+X+1$
- mode 5: 32 bits the poly is (0x04C011BB7) $x^{32}+x^{26}+ x^{23}+ x^{22}+ x^{16}+ x^{12}+ x^{11}+ x^{10}+ x^{8}+ x^{7}+ x^{5}+ x^{4}+ x^{2}+x+1$. 802.15.4g compatible

The initial state of the CRC polynomial is state to all 1b in all cases.

6.5.2 Manchester coding

Manchester coding can be enabled for the Basic and STack packet formats only by setting to ‘1’ the MANCHESTER_EN register.

Use of Manchester coding is exclusive with FEC and Three-out-of-six coding.

When Manchester coding is enabled each bit ‘1’ is actually transmitted on air as a ‘10’ sequence while a bit ‘0’ is transmitted as a ‘01’ sequence. If enabled, Manchester encoding is applied to all bits following the SYNC word.

7 MCU interface

Communication with the MCU goes through a standard 4-wire SPI interface and 4 GPIOs (plus SHUTDOWN pin).

MCU can performs the following operations:

- Program the S2-LPS in different operating modes by sending commands
- Read data from the RX FIFO and write data into the TX FIFO
- Configure the S2-LPS through the registers
- Retrieve information from the S2-LPS
- Get interrupt requests and signals from the GPIO pins
- Apply external signals to the GPIO pins
- Put the S2-LPS in SHUTDOWN state or exit from SHUTDOWN state

7.1 Serial peripheral interface

The four-wire SPI interface consist of:

- **SCLK**: the SPI clock from MCU to the S2-LPS
- **MOSI**: data from MCU to the S2-LPS
- **MISO**: data from the S2-LPS to MCU
- **CSn**: chip select signal, active low.

As the MCU is the master, it always drives the CSn and SCLK. According to the active SCLK polarity and phase, the S2-LPS SPI can be classified as mode 0 (CPOL=0, CPHA=0), which means that the base value of SCLK is zero, data are read on the clock rising edge and data are changed on the clock falling edge. The MISO is in tri-state mode when CSn is high. All transfers are MSB first.

The interface allows the following operations:

- Write data (to registers or TX FIFO)
- Read data (from registers or RX FIFO)
- Send commands.

The SPI communication is supported in all the active states, and also during the low power state: STANDBY and SLEEP.

When accessing the SPI interface, the two status bytes of the MC_STATE (MC_STATE[1], MC_STATE[0]) registers are sent to the MISO pin.

Figure 13. SPI write sequence

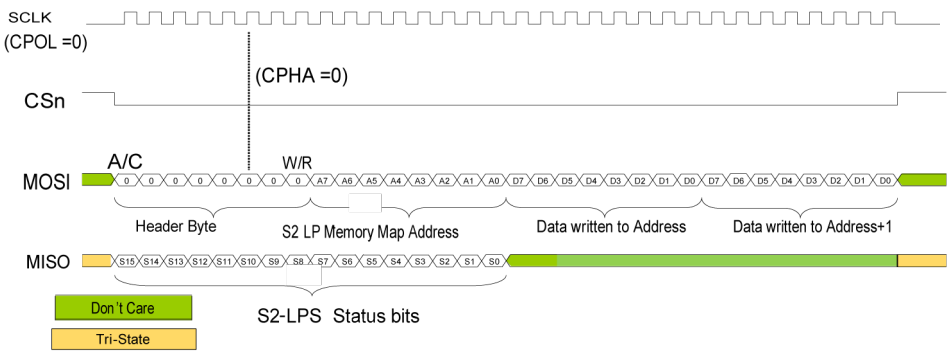


Figure 14. **SPI read sequence**

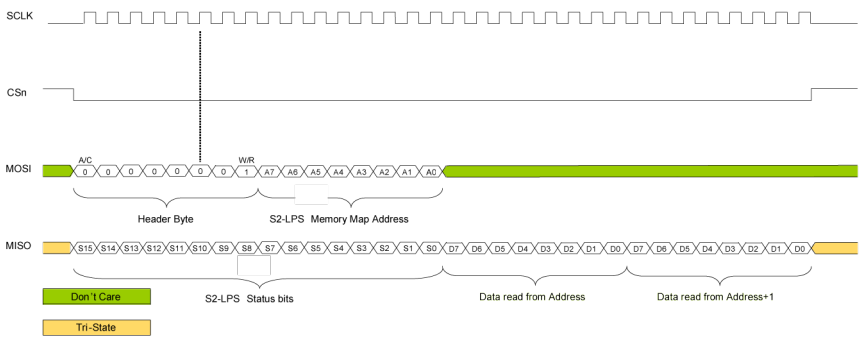
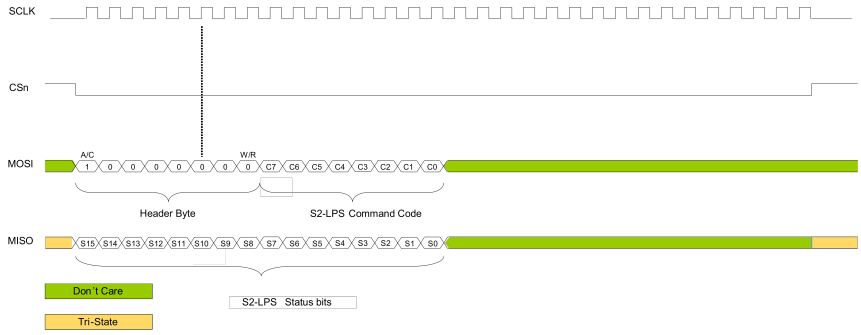


Figure 15. **SPI command sequence**



Concerning the first byte, the MSB is an A/C bit (address/commands: 0 indicates that the following byte is an address, 1 indicates that the following byte is a command code), while the LSB is a W/R bit (write/read: 1 indicates a read operation). All other bits must be zero.

Read and write operations are persistently executed while CSn is kept active (low), the address is automatically incremented (burst mode).

Accessing the FIFO is done as usual with the read and write commands, by putting, as address, the code 0xFF. Burst mode is available to access the sequence of bytes in the FIFO. Clearly, RX-FIFO is accessed with a read operation, TX-FIFO with a write operation.

7.2 Interrupts

In order to notify the MCU of a certain number of events an interrupt signal is generated on a selectable GPIO. The following events trigger an interrupt to the MCU:

Table 47. **Interrupts list**

Bit	Events group	Interrupt event
0	Packet oriented	RX data ready
1		RX data discarded (upon filtering)
2		TX data sent
3		Max. re-TX reached
4		CRC error
5		TX FIFO underflow/overflow error
6		RX FIFO underflow/overflow error

Bit	Events group	Interrupt event
7	Packet oriented	TX FIFO almost full
8		TX FIFO almost empty
9		RX FIFO almost full
10		RX FIFO almost empty
11		Max. number of back-off during CCA
12	Signal quality related	Valid preamble detected
13		Sync word detected
14		RSSI above threshold (CS)
15	Device status related	Wake-up timeout in LDCR mode (1)
16		READY (2)
17		STANDBY state switching in progress
18		Low battery level
19		Power-on reset
28	Timer related	RX timer timeout
29		Sniff timer timeout

1. *The interrupt flag n.15 is set (and consequently the interrupt request) only when the XO clock is available for the state machine. This time may be delayed compared to the actual timer expiration. However, the real time event can be sensed putting the end-of-counting signal on a GPIO output.*
2. *The interrupt flag n.16 is set each time the S2-LPS goes to READY state and the XO has completed its setting transient (XO ready condition detected).*

All interrupts are reported on a set of interrupt status registers and are individually maskable. The interrupt status register must be cleared upon a read event from the MCU.

The status of all the interrupts are reported in the IRQ_STATUS register: bits are high for the events that have generated any interrupts. The interrupts are individually maskable using the IRQ_MASK registers: if the mask bit related to a particular event is programmed at 0, that event does not generate any interrupt request.

7.3 GPIOs

The four GPIOs can be configured as follows:

Table 48. GPIO digital output functions

I/O selection	Output signal
0	nIRQ (interrupt request, active low)
1	POR inverted (active low)
2	Wake-up timer expiration: ‘1’ when WUT has expired
3	Low battery detection: ‘1’ when battery is below threshold setting
4	TX data internal clock output (TX data are sampled on the rising edge of it)
5	TX state outputs a command information coming from the RADIO_TX block
6	TX/RX FIFO almost empty flag
7	TX/RX FIFO almost full flag
8	RX data output
9	RX clock output (recovered from received data)
10	RX state indication: ‘1’ when the S2-LPS is transiting in the RX state

I/O selection	Output signal
11	Device in a state other than SLEEP or STANDBY: ‘0’ when in SLEEP/STANDBY
12	Device in STANDBY state
13	Antenna switch signal used for antenna diversity
14	Valid preamble detected flag
15	Sync word detected flag
16	RSSI above threshold (same indication of CS register)
17	Reserved
18	TX or RX mode indicator (to enable an external range extender)
19	VDD (to emulate an additional GPIO of the MCU, programmable by SPI)
20	GND (to emulate an additional GPIO of the MCU, programmable by SPI)
21	External SMPS enable signal (active high)
22	Device in SLEEP state
23	Device in READY state
24	Device in LOCK state
25	Device waiting for a high level of the lock-detector output signal
26	TX_DATA_OOK signal (internal control signal generated in the OOK analog smooth mode)
27	Device waiting for a high level of the READY2 signal from XO
28	Device waiting for timer expiration to allow PM block settling
29	Device waiting for end of VCO calibration
30	Device enables the full circuitry of the SYNTH block
31	Reserved

Table 49. GPIO digital input functions

I/O selection	Input signal
0	1 >> TX command
1	1 >> RX command
2	TX data input for direct modulation
3	Wake-up from external input (sensor output)
4	External clock @ 34.7 kHz (used for LDC modes timing)
From 5 to 31	Not used

8 Register contents

Table 50. **Register contents**

Name	Addr	Default	Bit	Field name	Description
GPIO0_CONF	00	0A	7:3	GPIO_SELECT	Specify the GPIO0 I/O signal, default setting POR (see Table 48. GPIO digital output functions).
			2	RESERVED	-
			1:0	GPIO_MODE	GPIO0 Mode: • 01b: Digital input • 10b: Digital output low power • 11b: Digital output high power
GPIO1_CONF	01	A2	7:3	GPIO_SELECT	Specify the GPIO1 I/O signal, default setting digital GND (see Table 48. GPIO digital output functions).
			2	RESERVED	-
			1:0	GPIO_MODE	GPIO1 Mode: • 01b: Digital input1 • 10b: Digital output low power • 11b: Digital Output High Power
GPIO2_CONF	02	A2	7:3	GPIO_SELECT	Specify the GPIO2 I/O signal, default setting digital GND (see Table 48. GPIO digital output functions).
			2	RESERVED	-
			1:0	GPIO_MODE	GPIO2 mMode: • 01b: Digital input • 10b: Digital output low power • 11b: Digital output high power
GPIO3_CONF	03	A2	7:3	GPIO_SELECT	Specify the GPIO3 I/O signal, default setting digital GND (see Table 48. GPIO digital output functions).
			2	RESERVED	-
			1:0	GPIO_MODE	GPIO3 Mode: • 00b: Analog

Name	Addr	Default	Bit	Field name	Description
GPIO3_CONF	03	A2			• 01b: Digital input • 10b: Digital output low power • 11b: Digital output high power
SYNT3	05	42	7:5	PLL_CP_ISEL	Set the charge pump current according to the XTAL frequency (see Table 30. Charge pump words).
			4	BS	Synthesizer band select. This parameter selects the out-of loop divide factor of the synthesizer: • 0: 4, band select factor for high band • 1: 8, band select factor for middle band.
			3:0	SYNT[27:24]	MSB bits of the PLL programmable divider.
SYNT2	06	16	7:0	SYNT[23:16]	Intermediate bits of the PLL programmable divider (see Section 4.3.1 RF channel frequency settings).
SYNT1	07	27	7:0	SYNT[15:8]	Intermediate bits of the PLL programmable divider (see Section 4.3.1 RF channel frequency settings).
SYNT0	08	62	7:0	SYNT[7:0]	LSB bits of the PLL programmable divider (see Section 4.3.1 RF channel frequency settings).
IF_OFFSET_ANA	09	2A	7:0	IF_OFFSET_ANA	Intermediate frequency setting for the analog RF synthesizer, default: 300 kHz, see Eq. (14).
IF_OFFSET_DIG	0A	B8	7:0	IF_OFFSET_DIG	Intermediate frequency setting for the digital shift-to-baseband circuits, default: 300 kHz, see Eq. (14).
CHSPACE	0C	3F	7:0	CH_SPACE	Channel spacing setting, see Eq. (15).

Name	Addr	Default	Bit	Field name	Description
CHNUM	0D	00	7:0	CH_NUM	Channel number. This value is multiplied by the channel spacing and added to the synthesizer base frequency to generate the actual RF carrier frequency, see Eq. (15).
MOD4	0E	83	7:0	DATARATE_M[15:8]	The MSB of the mantissa value of the data rate equation, see Eq. (13) .
MOD3	0F	2B	7:0	DATARATE_M[7:0]	The LSB of the mantissa value of the data rate equation, see Eq. (13).
MOD2	10	77	7:4	MOD_TYPE	Modulation type: • 0: 2-FSK • 1: 4-FSK • 2: 2-GFSK BT=1 • 3: 4-GFSK BT=1 • 5: ASK/OOK • 7: unmodulated • 10: 2-GFSK BT=0.5 • 11: 4-GFSK BT=0.5
			3:0	DATARATE_E	The exponent value of the data rate equation (see Eq. (13)).
MOD1	11	03	7	PA_INTERP_EN	1: enable the PA power interpolator (see Section 4.4.6.1 PA configuration).
			6	MOD_INTERP_EN	1: enable frequency interpolator for the GFSK shaping (see Section 4.4.1.1 Gaussian shaping).
			5:4	CONST_MAP	Select the constellation map for 4-(G)FSK or 2-(G)FSK modulations (see Table 34. Constellation mapping 2-(G)FSK and Table 35. Constellation mapping 4-(G)FSK).
			3:0	FDEV_E	The exponent value of the frequency deviation equation, see Eq. (9).
MOD0	12	93	7:0	FDEV_M	The mantissa value of the frequency deviation equation, see Eq. (9).

Name	Addr	Default	Bit	Field name	Description
CHFLT	13	23	7:4	CHFLT_M	The mantissa value of the receiver channel filter (see Table 37. Channel filter words).
			3:0	CHFLT_E	The exponent value of the receiver channel filter (see Table 37. Channel filter words).
AFC2	14	C8	7	AFC_FREEZE_ON_SYNC	1: enable the freeze AFC correction upon sync word detection.
			6	AFC_ENABLED	1: enable the AFC correction.
			5	AFC_MODE	Select AFC mode: 0: AFC loop closed on slicer 1: AFC loop closed on second conversion stage.
			4:0	RESERVED	-
AFC1	15	18	7:0	AFC_FAST_PERIOD	The length of the AFC fast period.
AFC0	16	25	7:4	AFC_FAST_GAIN	The AFC loop gain in fast mode (2's log).
			3:0	AFC_SLOW_GAIN	The AFC loop gain in slow mode (2's log).
RSSI_FLT	17	E3	7:4	RSSI_FLT	Gain of the RSSI filter.
			3:2	CS_MODE	Carrier sense mode: • 00b: Static CS • 01b: Dynamic CS with 6dB dynamic threshold • 10b: Dynamic CS with 12dB dynamic threshold • 11b: Dynamic CS with 18dB dynamic threshold. (see Section 4.4.5.8.2 Carrier sense)
			1:0	RESERVED	-
RSSI_TH	18	28	7:0	RSSI_TH	Signal detect threshold in 1 dB steps. The RSSI_TH can be converted in dBm using the formula RSSI_TH-146.
AGCCTRL4	1A	54	7:4	LOW_THRESHOLD_0	Low threshold 0 for the AGC

Name	Addr	Default	Bit	Field name	Description
AGCCTRL4	1A	54	3:0	LOW_THRESHOLD_1	Low threshold 1 for the AGC
AGCCTRL3	1B	10	7:0	LOW_THRESHOLD_SEL	Low threshold selection (defined in the AGCCTRL4). Bitmask for each attenuation step.
AGCCTRL2	1C	22	7:6	RESERVED	-
			5	FREEZE_ON_SYNC	Enable the AGC algorithm to be frozen on SYNC
			4	RESERVED	-
			3:0	MEAS_TIME	AGC measurement time
AGCCTRL1	1D	59	7:4	HIGH_THRESHOLD	High threshold for the AGC
			3:0	RESERVED	-
AGCCTRL0	1E	8C	7	AGC_ENABLE	0: disabled 1: enabled
			6	RESERVED	-
			5:0	HOLD_TIME	Hold time for after gain adjustment for the AGC.
ANT_SELECT_CONF	1F	45	7	RESERVED	-
			6:5	EQU_CTRL	ISI cancellation equalizer: • 00b: equalization disabled • 01b: single pass equalization • 10b: dual pass equalization. (see Section 4.4.1.2 ISI cancellation 4-(G)FSK)
			4	CS_BLANKING	Do not fill the RX FIFO with data if the CS is above threshold (see Section 4.4.5.9 CS blanking).
			3	AS_ENABLE	1: enable the antenna switching (see Section 4.4.5.10 Antenna switching).
			2:0	AS_MEAS_TIME	Set the measurement time.
CLOCKREC2	20	C0	7:5	CLK_REC_P_GAIN_SLOW	Clock recovery slow loop gain (log2).
			4	CLK_REC_ALGO_SEL	Select the symbol timing recovery algorithm: • 0: DLL

Name	Addr	Default	Bit	Field name	Description
					• 1: PLL.
CLOCKREC2	20	C0	3:0	CLK_REC_I_GAIN_SLOW	Set the integral slow gain for symbol timing recovery (PLL mode only).
CLOCKREC1	21	58	7:5	CLK_REC_P_GAIN_FAST	Clock recovery fast loop gain (log2).
			4	PSTFLT_LEN	Select the post filter length: • 0: 8 symbols • 1: 16 symbols.
			3:0	CLK_REC_I_GAIN_FAST	Set the integral fast gain for symbol timing recovery (PLL mode only).
PCKTCTRL6	2B	80	7:2	SYNC_LEN	The number of bits used for the SYNC field in the packet.
			1:0	PREAMBLE_LEN[9:8]	The MSB of the number of '01 or '10' of the preamble of the packet.
PCKTCTRL5	2C	10	7:0	PREAMBLE_LEN[7:0]	The LSB of the number of '01 or '10' of the preamble of the packet.
PCKTCTRL4	2D	00	7	LEN_WID	The number of bytes used for the length field: • 0: 1 byte • 1: 2 bytes.
			6:4	RESERVED	-
			3	ADDRESS_LEN	1: include the ADDRESS field in the packet.
			2:0	RESERVED	-
PCKTCTRL3	2E	20	7:6	PCKT_FRMT	Format of packet: • 0: Basic • 1: 802.15.4g • 2: UART OTA • 3: Stack (see Section 6 Packet handler engine)
			5:4	RX_MODE	RX mode: • 0: normal mode • 1: direct through FIFO • 2: direct through GPIO
			3	FSK4_SYM_SWAP	Reserved

Name	Addr	Default	Bit	Field name	Description
PCKTCTRL3	2E	20	2	BYTE_SWAP	Select the transmission order between MSB and LSB.
			1:0	PREAMBLE_SEL	Select the preamble pattern.
PCKTCTRL2	2F	00	7:6	RESERVED	-
			5	N/A	N/A
			4	RESERVED	N/A
			3	INT_EN_4G/ START_BIT	• If the 802.15.4 mode is enabled, 1: enable the interleaving of 802.15.4g packet. • If the UART packet is enabled, this is the value of the START_BIT
			2	MBUS_3OF6_EN	1: enable the 3-out-of-6 encoding/ decoding
			1	MANCHESTER_EN	1: enable the Manchester encoding/ decoding
			0	FIX_VAR_LEN	Packet length mode: • 0: fixed • 1: variable (in variable mode the field LEN_WID of PCKTCTRL3 register must be configured)
PCKTCTRL1	30	2C	7:5	CRC_MODE	CRC field: • 0: no CRC field • 1: CRC using poly 0x07 • 2: CRC using poly 0x8005 • 3: CRC using poly 0x1021 • 4: CRC using poly 0x864CBF • 5: CRC using poly 0x04C011BB7
			4	RESERVED	Reserved
			3:2	TXSOURCE	Tx source data: • 0: normal mode • 1: direct through FIFO • 2: direct through GPIO

Name	Addr	Default	Bit	Field name	Description
					• 3: PN9
PCKTCTRL1	30	2C	1	SECOND_SYNC_SEL	In TX mode: • 0 select the primary SYNC word • 1 select the secondary SYNC word. In RX mode, if 1 enable the dual SYNC word detection mode.
PCKTLEN1	31	00	7:0	PCKTLEN1	MSB of length of packet in bytes.
PCKTLEN0	32	14	7:0	PCKTLEN0	LSB of length of packet in bytes.
SYNC3	33	88	7:0	SYNC3	SYNC word byte 3.
SYNC2	34	88	7:0	SYNC2	SYNC word byte 2.
SYNC1	35	88	7:0	SYNC1	SYNC word byte 1.
SYNC0	36	88	7:0	SYNC0	SYNC word byte 0.
QI	37	01	7:5	SQI_TH	SQI threshold.
			4:1	PQI_TH	PQI threshold.
			0	SQI_EN	1: enable the SQI check.
PCKT_PSTMBL	38	00	7:0	PCKT_PSTMBL	Set the packet postamble length.
PROTOCOL2	39	40	7	CS_TIMEOUT_MASK	1: enable the CS value contributes to timeout disabling.
			6	SQI_TIMEOUT_MASK	1: enable the SQI value contributes to timeout disabling.
			5	PQI_TIMEOUT_MASK	1: enable the PQI value contributes to timeout disabling.
			4:3	TX_SEQ_NUM_RELOAD	TX sequence number to be used when counting reset is required using the related command.
			2	FIFO_GPIO_OUT_MUX_SEL	0: select the almost empty/full control for TX FIFO. 1: select the almost empty/full control for RX FIFO.
PROTOCOL1	3A	00			
PROTOCOL0	3B	08			

Name	Addr	Default	Bit	Field name	Description
PROTOCOL0	3B	08	1	PERS_RX	1: enable the persistent RX mode.
			0	RESERVED	-
FIFO_CONFIG3	3C	30	7	RESERVED	-
			6:0	RX_AFTHR	Set the RX FIFO almost full threshold.
FIFO_CONFIG2	3D	30	7	RESERVED	-
			6:0	RX_AETHR	Set the RX FIFO almost empty threshold.
FIFO_CONFIG1	3E	30	7	RESERVED	-
			6:0	TX_AFTHR	Set the TX FIFO almost full threshold.
FIFO_CONFIG0	3F	30	7	RESERVED	-
			6:0	TX_AETHR	Set the TX FIFO almost empty threshold.
PCKT_FLT_OPTIONS	40	40	7	RESERVED	-
			6	RX_TIMEOUT_AND_OR_SEL	Logical Boolean function applied to CS/SQI/PQI values: 1: OR, 0: AND.
			5	RESERVED	-
			4	SOURCE_ADDR_FLT	1: RX packet accepted if its source field matches with RX_SOURCE_ADDR register
			3	DEST_VS_BROADCAST_ADDR	1: RX packet accepted if its source field matches with BROADCAST_ADDR register.
			2	DEST_VS_MULTICAST_ADDR	1: RX packet accepted if its destination address matches with MULTICAST_ADDR register.
			1	DEST_VS_SOURCE_ADDR	1: RX packet accepted if its destination address matches with RX_SOURCE_ADDR register.
			0	CRC_FLT	1: packet discarded if CRC is not valid.
PCKT_FLT_GOALS4	41	00	7:0	RX_SOURCE_MASK	Mask register for source address filtering.
PCKT_FLT_GOALS3	42	00	7:0	RX_SOURCE_ADDR/ DUAL_SYNC3	If dual sync mode enabled: dual SYNC word byte 3, Otherwise RX packet source or TX packet destination field.

Name	Addr	Default	Bit	Field name	Description
PCKT_FLT_GOALS2	43	00	7:0	BROADCAST_ADDR/ DUAL_SYNC2	If dual sync mode enabled: dual SYNC word byte 2, Broadcast address.
PCKT_FLT_GOALS1	44	00	7:0	MULTICAST_ADDR/ DUAL_SYNC1	If dual sync mode enabled: dual SYNC word byte 1, Multicast address.
PCKT_FLT_GOALS0	45	00	7:0	TX_SOURCE_ADDR/ DUAL_SYNC0	If dual sync mode enabled: dual SYNC word byte 0, Tx packet source or RX packet destination field.
TIMERS5	46	01	7:0	RX_TIMER_CNTR	Counter for RX timer.
TIMERS4	47	00	7:0	RX_TIMER_PRESC	Prescaler for RX timer.
TIMERS3	48	01	7:0	LDC_TIMER_PRESC	Prescaler for wake up timer.
TIMERS2	49	00	7:0	LDC_TIMER_CNTR	Counter for wake up timer.
TIMERS1	4A	01	7:0	LDC_RELOAD_PRSC	Prescaler value for reload operation of wake up timer.
TIMERS0	4B	00	7:0	LDC_RELOAD_CNTR	Counter value for reload operation of wake up timer.
IRQ_MASK3	50	00	7:0	INT_MASK[31:24]	Enable the routing of the interrupt flag on the configured IRQ GPIO.
IRQ_MASK2	51	00	7:0	INT_MASK[23:16]	Enable the routing of the interrupt flag on the configured IRQ GPIO.
IRQ_MASK1	52	00	7:0	INT_MASK[15:8]	Enable the routing of the interrupt flag on the configured IRQ GPIO.
IRQ_MASK0	53	00	7:0	INT_MASK[7:0]	Enable the routing of the interrupt flag on the configured IRQ GPIO.
FAST_RX_TIMER	54	28	7:0	RSSI_SETTLING_LIMIT	Sniff timer configuration.
PA_POWER8	5A	01	7	RESERVED	-
			6:0	PA_LEVEL8	Output power level for 8th slot.
PA_POWER7	5B	0C	7	RESERVED	-
			6:0	PA_LEVEL_7	Output power level for 7th slot.
PA_POWER6	5C	18	7	RESERVED	-
			6:0	PA_LEVEL_6	Output power level for 6th slot.
PA_POWER5	5D	24	7	RESERVED	-

Name	Addr	Default	Bit	Field name	Description
PA_POWER5	5D	24	6:0	PA_LEVEL_5	Output power level for 5th slot.
PA_POWER4	5E	30	7	RESERVED	-
			6:0	PA_LEVEL_4	Output power level for 4th slot.
PA_POWER3	5F	48	7	RESERVED	-
			6:0	PA_LEVEL_3	Output power level for 3rd slot.
PA_POWER2	60	60	7	RESERVED	-
			6:0	PA_LEVEL_2	Output power level for 2nd slot.
PA_POWER1	61	00	7	RESERVED	-
			6:0	PA_LEVEL_1	Output power level for 1st slot.
PA_POWER0	62	47	7	DIG_SMOOTH_EN	1: enable the generation of the internal signal TX_DATA which is the input of the FIR. Needed when FIR_EN=1.
			6	PA_MAXDBM	1: configure the PA to send maximum output power. Power ramping is disable with this bit set to 1.
			5	PA_RAMP_EN	1: enable the power ramping.
			4:3	PA_RAMP_STEP_LEN	Set the step width (unit: 1/8 of bit period).
			2:0	PA_LEVEL_MAX_IDX	Final level for power ramping or selected output power index.
PA_CONFIG1	63	03	7:4	RESERVED	-
			3:2	FIR_CFG	FIR configuration: • 00b: filtering • 01b: ramping • 10b: switching (see Section 4.4.2.1 OOK smoothing)
			1	FIR_EN	1: enable FIR (see Section 4.4.2.1 OOK smoothing)
			0	RESERVED	-
PA_CONFIG0	64	8A	7:4	PA_DEGEN_TRIM	11xx ® code threshold: 485 10xx ® code threshold: 465 01xx ® code threshold: 439

Name	Addr	Default	Bit	Field name	Description
PA_CONFIG0	64	8A			00xx ® code threshold: 418 xx11 ® clamp voltage: 0.55 V xx10 ® clamp voltage: 0.50 V xx01 ® clamp voltage: 0.45 V xx00 ® clamp voltage: 0.40 V.
			3	PA_DEGEN_ON	Enables the 'degeneration' mode that introduces a pre-distortion to linearize the power control curve.
			2	SAFE_ASK_CAL	During a TX operation, enables and starts the digital ASK calibrator.
			1:0	PA_FC	PA Bessel filter bandwidth: • 00b: 12.5 kHz (data rate 16.2 kbps) • 01b: 25 kHz (data rate 32 kbps) • 10b: 50 kHz (data rate 62.5 kbps) • 11b: 100 kHz (data rate 125 kbps), (see Section 4.4.2.1 OOK smoothing) .
SYNTH_CONFIG2	65	D0	7:3	RESERVED	-
			2	PLL_PFD_SPLIT_EN	Enables increased DN current pulses to improve linearization of CP/PFD (see Table 30. Charge pump words).
			1:0	RESERVED	-
VCO_CONFIG	68	03	7:6	RESERVED	-
			5	VCO_CALAMP_EXT_SEL	1 → VCO amplitude calibration is skipped (external amplitude word forced on VCO).
			4	VCO_CALFREQ_EXT_SEL	1 → VCO frequency calibration is skipped (external amplitude word forced on VCO).
			3:0	RESERVED	-
VCO_CALIBR_IN2	69	88	7:0	RESERVED	-
VCO_CALIBR_IN1	6A	40	7:0	RESERVED	-

Name	Addr	Default	Bit	Field name	Description
VCO_CALIBR_IN0	6B	40	7:0	RESERVED	-
XO_RCO_CONF1	6C	45	7:5	RESERVED	-
			4	PD_CLKDIV	1: disable both dividers of digital clock (and reference clock for the SMPS) and IF-ADC clock.
			3:0	RESERVED	-
XO_RCO_CONF0	6D	30	7	EXT_REF	• 0: reference signal from XO circuit • 1: reference signal from XIN pin.
			6:4	GM_CONF	Set the driver gm of the XO at start up.
			3	REFDIV	1: enable the the reference clock divider.
			2	RESERVED	-
			1	EXT_RCO_OSC	1: the 34.7 kHz signal must be supplied from any GPIO.
			0	RCO_CALIBRATION	1: enable the automatic RCO calibration.
RCO_CALIBR_CONF3	6E	70	7:4	RWT_IN	RWT word value for the RCO.
			3:0	RFB_IN[4:1]	MSB part of RFB word value for RCO.
RCO_CALIBR_CONF2	6F	4D	7	RFB_IN[0]	LSB part of RFB word value for RCO.
			6:0	RESERVED	-
PM_CONF4	75	17	7:6	RESERVED	-
			5	EXT_SMPS	1: disable the internal SMPS.
			4:0	RESERVED	-
PM_CONF3	76	20	7	KRM_EN	• 0: divider by 4 enabled (SMPS' switching frequency is FSW=Fdig/4) • 1: rate multiplier enabled (SMPS' switching frequency is FSW=KRM*Fdig /(2^15).
			6:0	KRM[14:8]	Sets the divider ratio (MSB) of the rate multiplier (default: Fsw=Fdig/4)

Name	Addr	Default	Bit	Field name	Description
PM_CONF2	77	00	7:0	KRM[7:0]	Sets the divider ratio (LSB) of the rate multiplier (default: Fsw=Fdig/4)
PM_CONF1	78	39	7	RESERVED	-
			6	BATTERY_LVL_EN	1: enable battery level detector circuit.
			5:4	SET_BLD_TH	Set the BLD threshold: • 00b: 2.7 V • 01b: 2.5 V • 10b: 2.3 V • 11b: 2.1 V.
			3	SMPS_LVL_MODE	• 0: SMPS output level depends upon the value written in the PM_CONFIG0 register (SET_SMPS_LEVEL field) both in RX and TX state. • 1: SMPS output level depends upon the value in PM_CONFIG register just in TX state, while in RX state it is fixed to 1.4 V
			2	BYPASS_LDO	Set to 0 (default value)
			1:0	RESERVED	-
PM_CONF0	79	42	7	RESERVED	-
			6:4	SET_SMPS_LVL	SMPS output voltage: • 000b: not used • 001b: 1.2 V • 010b: 1.3 V • 011b: 1.4 V • 100b: 1.5 V • 101b: 1.6 V • 110b: 1.7 V • 111b: 1.8 V
			3:1	RESERVED	-
			0	SLEEP_MODE_SEL	• 0: SLEEP without FIFO retention (SLEEP A) • 1: SLEEP with FIFO retention (SLEEP B).
MC_STATE1	8D	52	7:5	RESERVED	-
			4	RCO_CAL_OK	RCO calibration successfully terminated.

Name	Addr	Default	Bit	Field name	Description
MC_STATE1	8D	52	3	ANT_SEL	Currently selected antenna.
			2	TX_FIFO_FULL	1: TX FIFO is full.
			1	RX_FIFO_EMPTY	1: RX FIFO is empty.
			0	ERROR_LOCK	1: RCO calibrator error.
MC_STATE0	8E	07	7:1	STATE	Current state.
			0	XO_ON	1: XO is operating.
TX_FIFO_STATUS	8F	00	7:0	NELEM_TXFIFO	Number of elements in TX FIFO.
RX_FIFO_STATUS	90	00	7:0	NELEM_RXFIFO	Number of elements in RX FIFO.
RCO_CALIBR_OUT4	94	70	7:4	RWT_OUT	RWT word from internal RCO calibrator.
			3:0	RFB_OUT[4:1]	RFB word (MSB) from internal RCO calibrator.
RCO_CALIBR_OUT3	95	00	7	RFB_OUT[0]	RF word (LSB) from internal RCO calibrator.
			6:0	RESERVED	-
VCO_CALIBR_OUT1	99	00	7:4	RESERVED	-
			3:0	VCO_CAL_AMP_OUT	VCO magnitude calibration output word (binary coding internally converted from thermometric coding).
VCO_CALIBROUT0	9A	00	7	RESERVED	-
			6:0	VCO_CAL_FREQ_OUT	VCO Cbank frequency calibration output word (binary coding internally converted from thermometric coding).
TX_PCKT_INFO	9C	00	7:6	RESERVED	-
			5:4	TX_SEQ_NUM	Current TX packet sequence number.
			3:0	N_RETX	Number of re-transmissions done for the last TX packet.
RX_PCKT_INFO	9D	00	7:3	RESERVED	-
			2	NACK_RX	NACK field of the received packet.
			1:0	RX_SEQ_NUM	Sequence number of the received packet.
AFC_CORR	9E	00	7:0	AFC_CORR	AFC corrected value.
LINK_QUALIF2	9F	00	7:0	PQI	PQI value of the received packet.

Name	Addr	Default	Bit	Field name	Description
LINK_QUALIF1	A0	00	7	CS	Carrier sense indication.
			6:0	SQI	SQI value of the received packet.
RSSI_LEVEL	A2	00	7:0	RSSI_LEVEL	RSSI level captured at the end of the SYNC word detection of the received packet.
RX_PCKT_LEN1	A4	00	7:0	RX_PCKT_LEN[14:8]	MSB value of the length of the packet received.
RX_PCKT_LEN0	A5	00	7:0	RX_PCKT_LEN[7:0]	LSB value of the length of the packet received.
CRC_FIELD3	A6	00	7:0	CRC_FIELD3	CRC field 3 of the received packet.
CRC_FIELD2	A7	00	7:0	CRC_FIELD2	CRC field 2 of the received packet.
CRC_FIELD1	A8	00	7:0	CRC_FIELD1	CRC field 1 of the received packet.
CRC_FIELD0	A9	00	7:0	CRC_FIELD0	CRC field 0 of the received packet.
RX_ADDRE_FIELD1	AA	00	7:0	RX_ADDRE_FIELD1	Source address field of the received packet.
RX_ADDRE_FIELD0	AB	00	7:0	RX_ADDRE_FIELD0	Destination address field of the received packet.
RSSI_LEVEL_RUN	EF	00	7:0	RSSI_LEVEL_RUN	RSSI level of the received packet, which supports continuous fast SPI reading.
DEVICE_INFO1	F0	03	7:0	PARTNUM	S2-LPS part number
DEVICE_INFO0	F1	C1	7:0	VERSION	S2-LPS version number
IRQ_STATUS3	FA	00	7:0	INT_LEVEL[31:24]	Interrupt status register 3
IRQ_STATUS2	FB	09	7:0	INT_LEVEL[23:16]	Interrupt status register 2
IRQ_STATUS1	FC	05	7:0	INT_LEVEL[15:8]	Interrupt status register 1
IRQ_STATUS0	FD	00	7:0	INT_LEVEL[7:0]	Interrupt status register 0

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN24L (4x4 mm) package information

Figure 16. QFN24L (4x4 mm) package outline

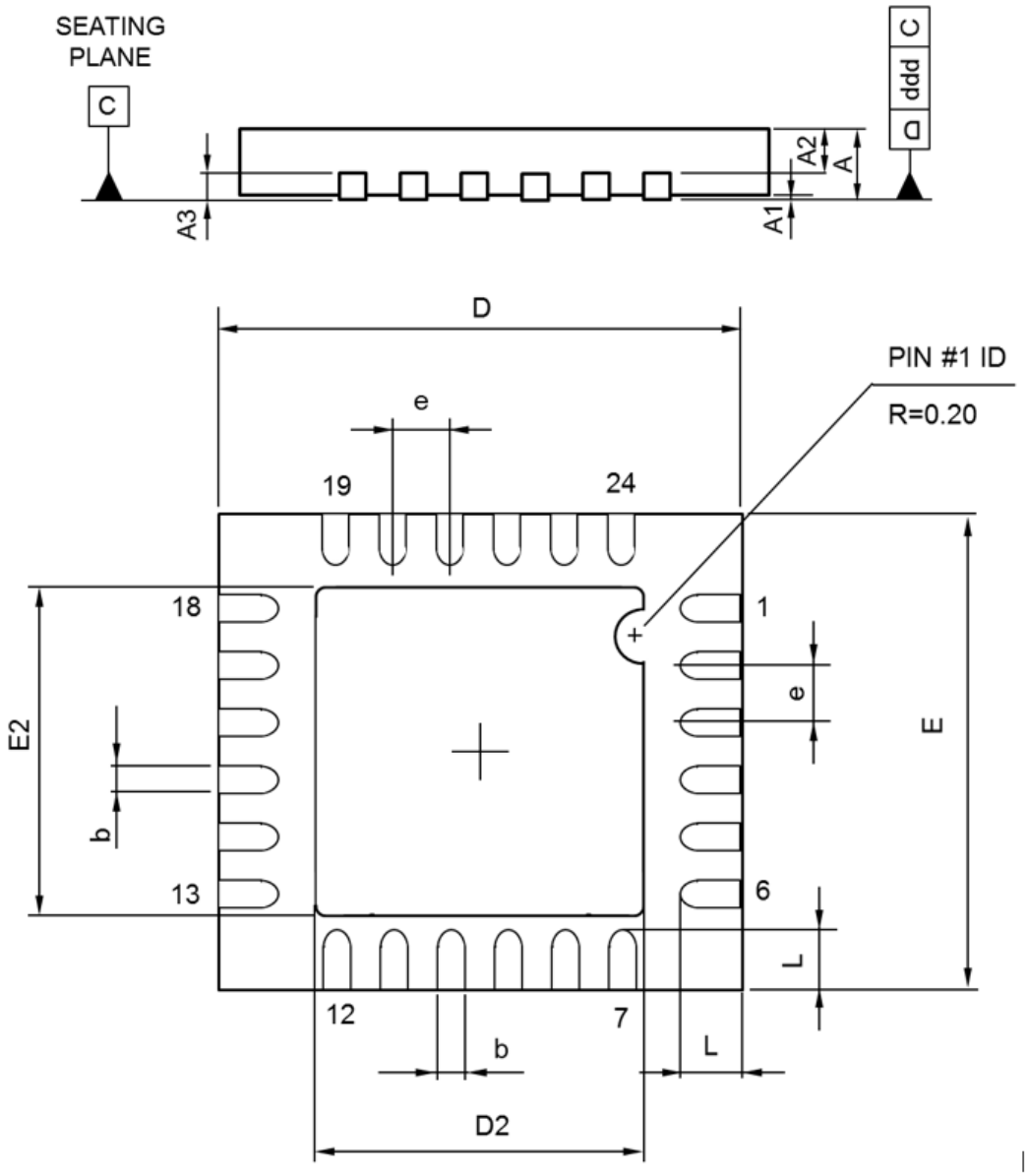


Table 51. **QFN24L (4x4 mm) package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
A1		0.02	0.05
A2		0.65	1.00
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.60	2.70	2.80
E	3.85	4.00	4.15
E2	2.60	2.70	2.80
e		0.50	
L	0.35	0.40	0.45
ddd			0.08

9.2 PCB pad pattern

In order to design a proper pad pattern, tolerance analysis is required on package and motherboard dimensions. The tolerance analysis requires consideration of component tolerances, PCB tolerances and the accuracy of the equipment used to place the component.

For the pad dimensioning three different minimum values have been considered:

- Minimum toe fillet = JTmin = 0.1 mm
- Minimum heel fillet = JHmin = 0.05 mm
- Minimum side fillet = JSmin = 0 mm

The PCB thermal pad should at least match the exposed die paddle size. The solder mask opening should be 120 to 150 microns larger than the pad size resulting in 60 to 75 microns clearance between the copper pas and solder mask.

Figure 17. **QFN24 4x4x1pitch 0.5 mm PCB pad pattern**

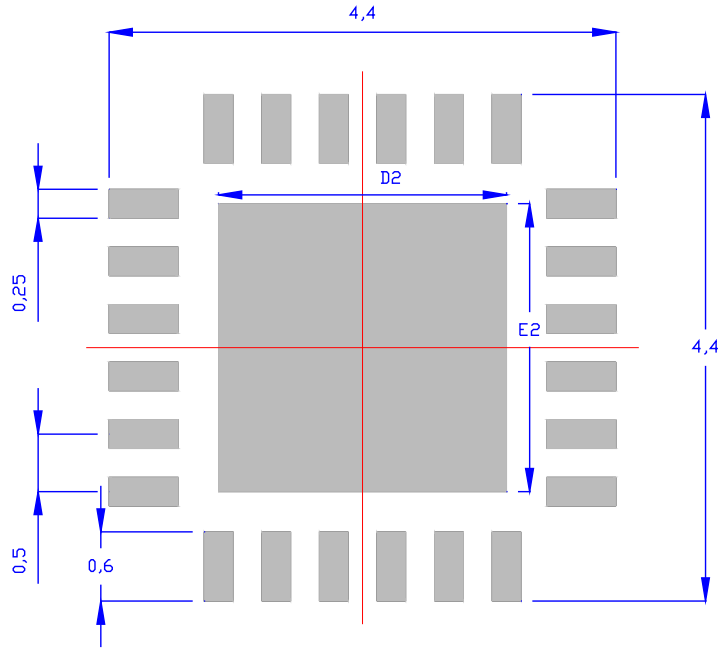


Table 52. **Exposed pad dimension**

D2 (mm)	E2 (mm)
2.70	2.70

9.3 QFN recommended profile parameters

The temperature profile is the most important control in the re-flow soldering and it must be fine tuned to establish a robust process. QFN recommended soldering profile for lead-free mounting is shown in the following table and picture.

Figure 18. **QFN recommended soldering profiles**

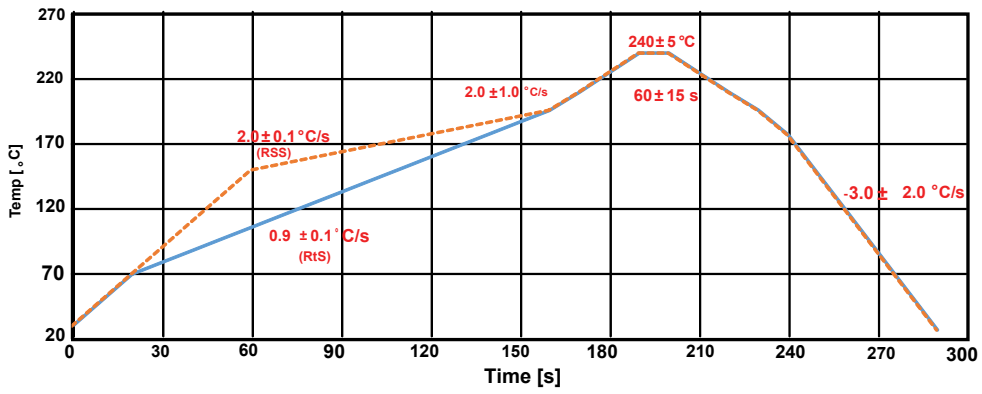


Table 53. Temperature profiles

Profile	Ramp-to-spike	Ramp-soak-spike
Temperature gradient in preheat	T from 70 °C to 150 °C 0.8 °C/s to 1.0 °C/s	T from 70 °C to 150 °C 1 °C/s to 3 °C/s
Soak/dwell (refer to solder paste supplier recommendation)	N/A or temp.: 150 °C to 200 °C, 40 to 80 s	Soak 150 °C to 200 °C, 40 to 100 s
Temperature gradient in preheat	Temp.: 200 °C to 225 °C, 1 °C/s to 3 °C/s	Temp.: 200 °C to 225 °C, 1 °C/s to 3 °C/s
Peak temperature	235 °C to 245 °C	
Duration above 220 °C	45 to 75 s	
Temperature gradient in cooling	-1 °C to -5 °C	
Time from 50 to 220 °C	150 to 230 s	

10 Ordering information

Table 54. **Ordering information**

Order code	Package	Packing
S2-LPSQTR	QFN24 4x4x1	Tape and reel
S2-LPSCBQTR	QFN24 4x4x1	Tape and reel

Revision history

Table 55. **Document revision history**

Date	Version	Changes
01-Feb-2022	1	Initial release.

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