

Quad 2-Input AND Gate

MM74HC08

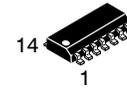
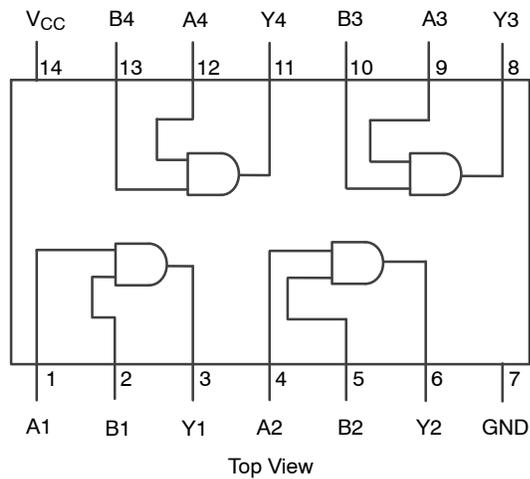
General Description

The MM74HC08 AND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

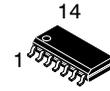
Features

- Typical Propagation Delay: 12 ns (t_{PHL}), 7 ns (t_{PLH})
- Fan-out of 10 LS-TTL Loads
- Quiescent Power Consumption: 2 μ A Maximum at Room Temperature
- Low Input Current: 1 μ A Maximum
- This Device is Pb-Free and Halide Free

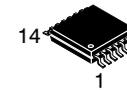
Connection Diagram



SOIC-14 NB
CASE 751A-03

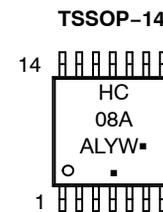
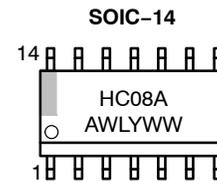


SOIC14
CASE 751EF



TSSOP-14 WB
CASE 948G-01

MARKING DIAGRAMS



HC08A = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot Number
Y = Year
WW, YW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

MM74HC08

ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Rating | Min | Max | Unit | |
|------------------|--|-------------------|----------------|------|----|
| V_{CC} | Supply Voltage | -0.5 | +7.0 | V | |
| V_{IN} | DC Input Voltage | -0.5 | $V_{CC} + 0.5$ | V | |
| V_{OUT} | DC Output Voltage | -0.5 | $V_{CC} + 0.5$ | V | |
| I_{IK}, I_{OK} | Clamp Diode Current | | ± 20 | mA | |
| I_{OUT} | DC Output Current, per pin | | ± 25 | mA | |
| I_{CC} | DC V_{CC} or GND Current, per pin | | ± 50 | mA | |
| T_{STG} | Storage Temperature Range | -65 | +150 | °C | |
| P_D | Power Dissipation | SOIC Package only | | 500 | mW |
| T_L | Lead Temperature (Soldering 10 second) | | 260 | °C | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|-------------------|-----------------------------|-------------------------|----------|------|----|
| V_{CC} | Supply Voltage | 2 | 6 | V | |
| V_{IN}, V_{OUT} | DC Input or Output Voltage | 0 | V_{CC} | V | |
| T_A | Operating Temperature Range | -55 | +125 | °C | |
| t_r, t_f | Input Rise or Fall Times | $V_{CC} = 2.0\text{ V}$ | - | 1000 | ns |
| | | $V_{CC} = 4.5\text{ V}$ | - | 500 | ns |
| | | $V_{CC} = 6.0\text{ V}$ | - | 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MM74HC08

DC ELECTRICAL CHARACTERISTICS (Note 2)

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | T _A = -40°C to 85°C | T _A = -55°C to 125°C | Unit |
|-----------------|-----------------------------------|---------------------|--|--|-------------------|-----------------------------------|------------------------------------|------|
| | | | | Typ | Guaranteed Limits | | | |
| V _{IH} | Minimum HIGH Level Input Voltage | 2.0 | | | 1.5 | 1.5 | 1.5 | V |
| | | 4.5 | | | 3.15 | 3.15 | 3.15 | |
| | | 6.0 | | | 4.2 | 4.2 | 4.2 | |
| V _{IL} | Maximum LOW Level Input Voltage | 2.0 | | | 0.5 | 0.5 | 0.5 | V |
| | | 4.5 | | | 1.35 | 1.35 | 1.35 | |
| | | 6.0 | | | 1.8 | 1.8 | 1.8 | |
| V _{OH} | Minimum HIGH Level Output Voltage | 2.0 | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | 4.5 | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | 6.0 | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | 4.5 | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA | 4.2 | 3.98 | 3.84 | 3.7 | |
| | | 6.0 | | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 5.2 mA | 5.7 | 5.48 | 5.34 | |
| V _{OL} | Maximum LOW Level Output Voltage | 2.0 | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA | | 0 | 0.1 | 0.1 | 0.1 |
| | | 4.5 | | 0 | 0.1 | 0.1 | 0.1 | |
| | | 6.0 | | 0 | 0.1 | 0.1 | 0.1 | |
| | | 4.5 | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA | 0.2 | 0.26 | 0.33 | 0.4 | |
| | | 6.0 | | V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 5.2 mA | 0.2 | 0.26 | 0.33 | 0.4 |
| I _{IN} | Maximum Input Current | 6.0 | V _{IN} = V _{CC} or GND | | | ±0.1 | ±1.0 | ±1.0 |
| I _{CC} | Maximum Quiescent Supply Current | 6.0 | V _{IN} = V _{CC} or GND, I _{OUT} = 0 μA | | 2.0 | 20 | 40 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- For a power supply of 5 V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

MM74HC08

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 15\text{ pF}$, $t_r = t_f = 6\text{ ns}$)

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Unit |
|-----------|---|------------|-----|------------------|------|
| t_{PHL} | Maximum Propagation Delay, Output HIGH-to-LOW | | 12 | 20 | ns |
| t_{PLH} | Maximum Propagation Delay, Output LOW-to-HIGH | | 7 | 15 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.0\text{ V to }6.0\text{ V}$, $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$, (unless otherwise specified))

| Symbol | Parameter | V_{CC} (V) | Conditions | $T_A = 25^\circ\text{C}$ | | $T_A = -40^\circ\text{C to }125^\circ\text{C}$ | | Unit |
|--------------------|---|--------------|------------|--------------------------|-------------------|--|----|------|
| | | | | Typ | Guaranteed Limits | | | |
| t_{PHL} | Maximum Propagation Delay, Output HIGH-to-LOW | 2.0 | | 77 | 121 | 175 | ns | |
| | | 4.5 | | 15 | 24 | 35 | | |
| | | 6.0 | | 13 | 20 | 30 | | |
| t_{PLH} | Maximum Propagation Delay, Output LOW-to-HIGH | 2.0 | | 30 | 90 | 134 | ns | |
| | | 4.5 | | 10 | 18 | 27 | | |
| | | 6.0 | | 8 | 15 | 23 | | |
| t_{TLH}, t_{THL} | Maximum Output Rise and Fall Time | 2.0 | | 30 | 75 | 110 | ns | |
| | | 4.5 | | 8 | 15 | 22 | | |
| | | 6.0 | | 7 | 13 | 19 | | |
| C_{PD} | Power Dissipation Capacitance (Note 3) | | (per gate) | 38 | | | pF | |
| C_{IN} | Maximum Input Capacitance | | | 4 | 10 | 10 | pF | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|--------------|---|--------------------------|
| MM74HC08M | SOIC-14 NB, Case 751A-03 (Pb-Free and Halide Free) | 55 Units / Tube |
| MM74HC08MX | SOIC 14, Case 751EF (Pb-Free and Halide Free) | 2500 Units / Tape & Reel |
| MM74HC08MTC | TSSOP-14 WB, Case 948G-01 (Pb-Free and Halide Free) | 96 Units / Tube |
| MM74HC08MTCX | | 2500 Units / Tape & Reel |

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

NOTE: All packages are lead free per JEDEC: J-STD-020B standard.

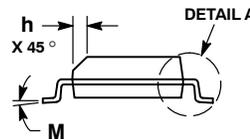
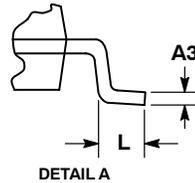
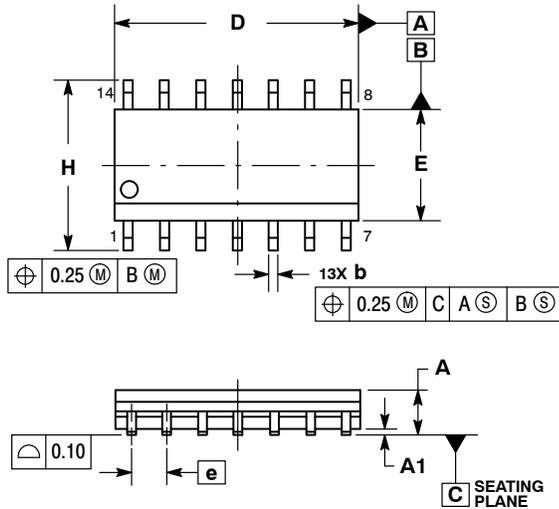
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

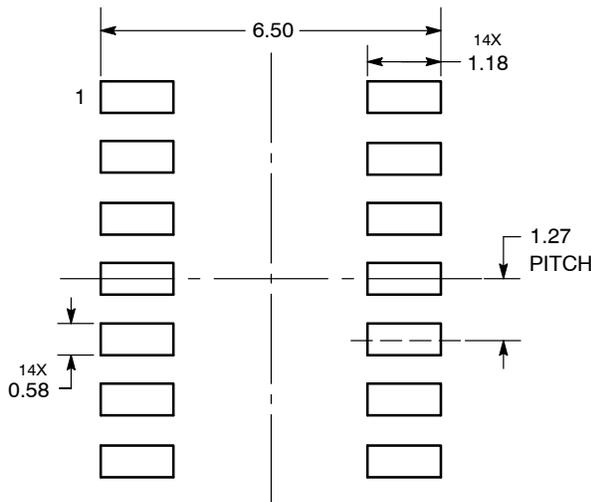
DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

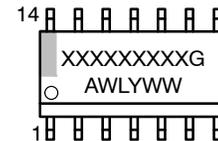
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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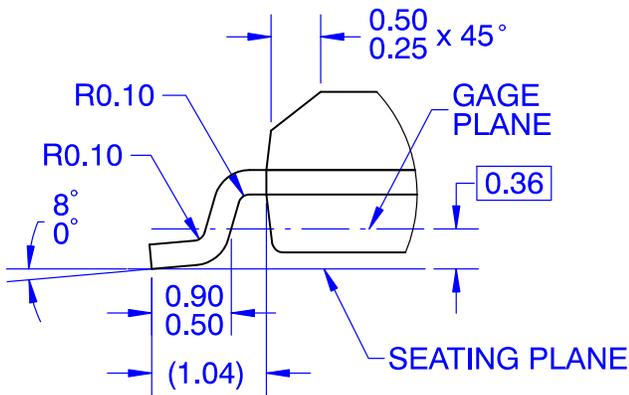
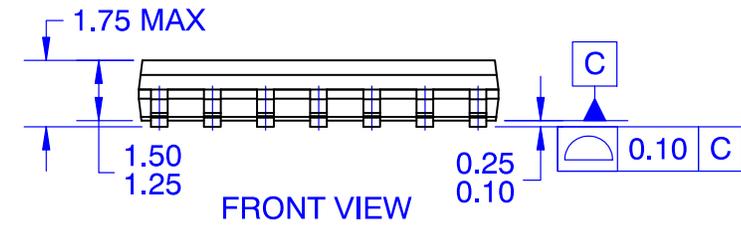
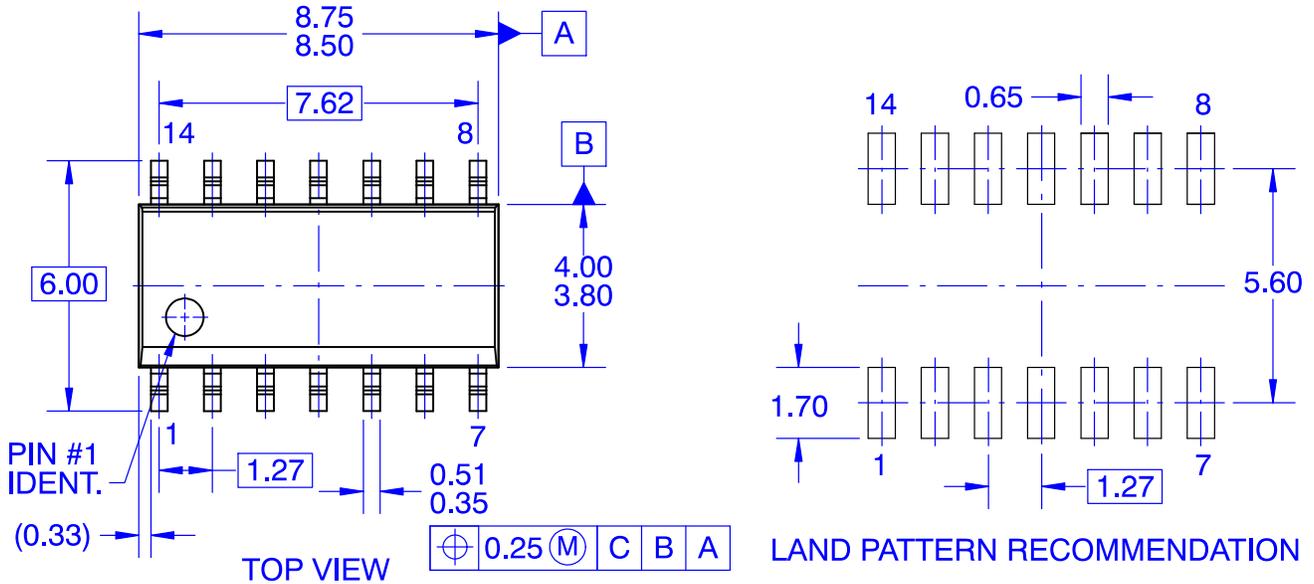
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



DETAIL A
SCALE 16 : 1

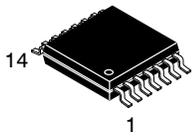
NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009

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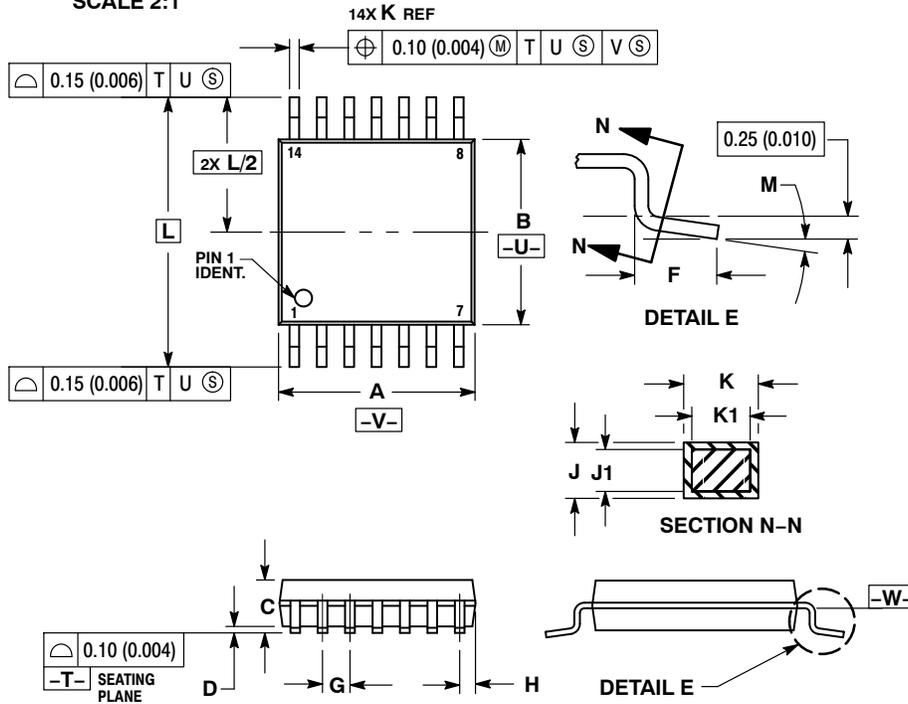
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

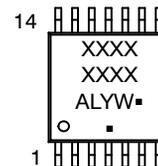


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

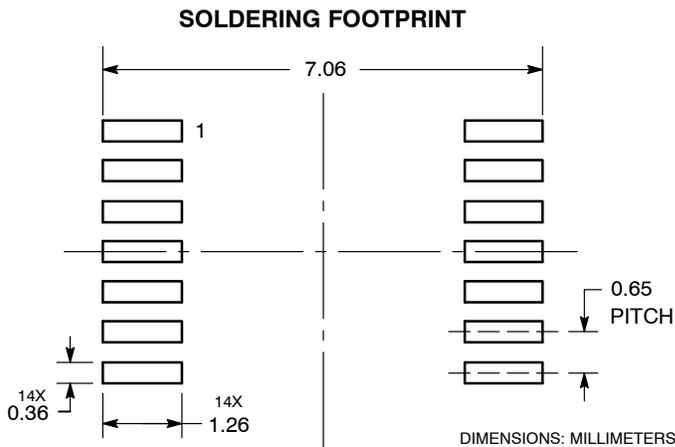
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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