

Audio Amplifier ISD8102 DataSheet

ISD8102 - Earphone Sense IN (Single-ended)

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1 GENERAL DESCRIPTION

ISD8102 is a general purpose analog audio amplifier, capable of driving a 4Ω load with up to $2W_{rms}$ output power. This device includes output current limiting, chip enable, low standby current and excellent pop-and-click suppression.

Also included is the ability to configure the input as single-ended. Internal resistors set the device to have default 20dB gain, and with external resistors any gain less than this can be achieved. The device is unity gain stable, including use with external feedback resistors and external capacitors as may be optionally used for implementing simple filtering functions.

ISD8102:

The ISD8102 output can be configured to drive either single ended or bridge tied loads (BTL). The Mode pin controls which configuration is active. This function is useful when using the ISD8102 to alternate between driving a speaker or a mono earpiece which is connected through a shorting phone jack. The Mode pin is connected to the normally closed pin of the shorting phone jack (see figure 3.1). When nothing is plugged into the jack, the external resistor holds the Mode pin low, enabling BTL mode. When a plug is inserted, the switch is opened and the mode pin goes to $1/2 V_{DD}$, as controlled by the resistor divider, putting the amplifier into single ended mode. Note that in this example, the speaker remains connected in both cases.

2 FEATURES

- Wide power supply range and excellent standby current
 - 2.0Vdc – 5.5Vdc operation
 - <1uA standby current
- High output power (cap-less BTL configuration)
 - Up to 2W output into 4Ω load (<10% distortion) with 5.5Vdc supply voltage
 - < 0.1% distortion at 600mW into 8-ohms with 5Vdc supply voltage
- Excellent pop-and-click performance
 - Low to inaudible pop/click using Chip Enable
- Single-Ended or Differential signal inputs
 - > 75dB common mode rejection in differential mode
 - > 70dB power supply noise rejection
- Very fast start-up time
 - Less than 1msec when using Chip Enable
- Current limiting for over-current conditions
- Package options:
DIE, SOP-8 (thermal pad)
- Less BOM cost / Easy PCB layout
- Temperature Range: -40°C ~ +85°C
- Package is Halogen-free, RoHS-compliant and TSCA-compliant

Applications:

- Toys
- Feature Phones
- Portable Game Consoles
- GPS
- Portable Speakers
- Boom Box
- White Goods

3 BLOCK DIAGRAM

3.1 ISD8102 WITH EARPIECE SENSE INPUT (PIN 3 = SE / BTL MODE)

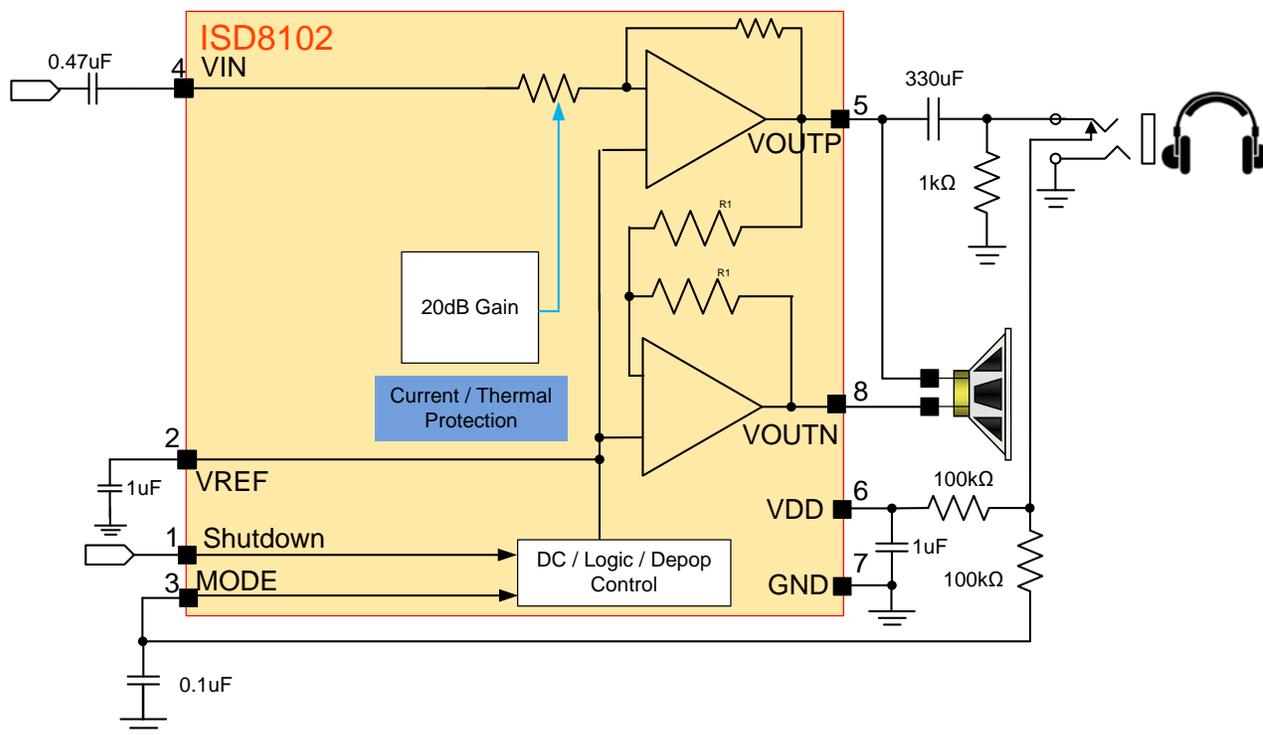


Figure 3-1 ISD8102 Earpiece Configuration Block Diagram

4 PINOUT CONFIGURATION: SOP- 8

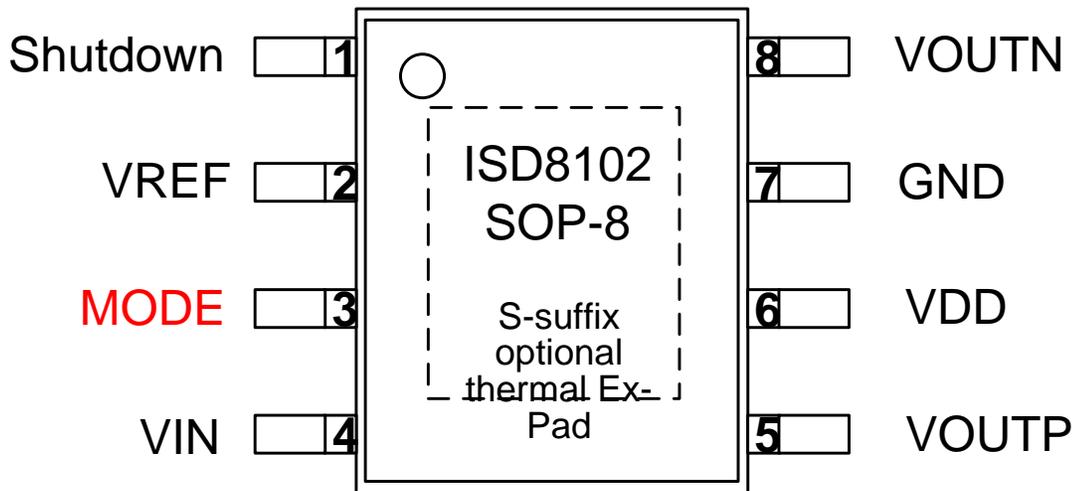


Figure 4-1 ISD8102 8-Lead SOP Pin Configuration

5 PIN DESCRIPTION

Pin Number	Pin Name	I/O	Function
1	Shutdown	I	Shutdown (Low = Chip Power Up / High = Chip Power Down)
2	VREF	O	Internal Reference Voltage (1/2 V _{DD})
3	MODE	I	Single-Ended / Differential Output Logic Control
4	VIN	I	Inverting Signal Input
5	VOUTP	O	Non-Inverting Speaker Output
6	VDD	I	Supply Voltage
7	GND	I	Ground
8	VOUTN	O	Inverting Speaker Output
9	Ex-Pad	I	Thermal Tab (must be connected to V _{SS} , SOP-8 package, only)

Table 5-1 ISD8102 8-Lead SOP Pin Description

6 ELECTRICAL CHARACTERISTICS

6.1 OPERATING CONDITIONS

OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Operating temperature range ¹	-40°C to +85°C
Supply voltage (V _{DD})	+2.0V to +5.5V
Ground voltage (V _{SS})	0V
Input voltage (V _{DD})	V _{SS} to V _{DD}
Voltage applied to any pins	(V _{SS} - 0.3V) to (V _{DD} + 0.3V)

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature) ¹	-40°C to +85°C
Supply voltage (V _{DD})	+2.0V to +5.5V
Ground voltage (V _{SS})	0V
Input voltage (V _{DD})	V _{SS} to V _{DD}
Voltage applied to any pins	(V _{SS} - 0.3V) to (V _{DD} + 0.3V)

Notes: ^[1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

6.2 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP ^[1]	MAX	UNITS	CONDITIONS
Supply Voltage	V _{DD}	2.0		5.5	V	
Operating Current	I _{DD}		2.6		mA	V _{DD} = 5V, no load
Standby Current	I _{SB}		0.1	1	μA	V _{DD} = 5V
CE input resistance			20k		Ω	Internal pull-down @ 0dB
CE input current			120		μA	CE=2.3V, V _{DD} = 5V
CE threshold enabled	V _{ENL}		0.9		V	All supply voltages
CE threshold standby	V _{ENH}		1.5		V	All supply voltages
VREF Reference Voltage			V _{DD} /2		V	

Notes: ^[1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

6.3 AC PARAMETERS

6.3.1 Analog Characteristics; $C_{ref} = 1\mu F / C_{V_{DD}} = 1\mu F$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Input Voltage Range			0.3 – 5.2		V	$V_{DD} = 5.5V_{dc}$
			0.3 – 3.4		V	$V_{DD} = 3.7V_{dc}$
			0.3 - 1.7		V	$V_{DD} = 2.0V_{dc}$
Inverting Input Impedance			2k Ω			Gain = 20dB
Non-Inverting Input Impedance			22k Ω			Gain = 20dB
Power Supply Rejection Ratio	PSRR		75		dB	$V_{DD} = 5V_{dc}$
Common Mode Rejection Ratio	CMRR		70		dB	Signal at INP = INV
Voltage Gain			20		dB	$R_{input} = 0 \Omega$
Enable Time from Standby			0.5		msec	Single-ended
Enable Time from Standby			0.5		msec	Differential
Pop-and-Click from Standby ¹			10		mV	Single Ended
Pop-and-Click from Standby ¹			10		mV	Differential
Thermal Resistance			60		$^{\circ}C/W$	SOP-8 (with Ex-Pad)
Thermal Resistance			150		$^{\circ}C/W$	SOP-8

Notes:^[1] Impulse voltage that is potentially audible. After impulse, there is a slow ramp from standby V_{ref} to operating V_{ref} , which is typically inaudible with $C_{ref} = 1\mu F$

6.3.2 Speaker Outputs

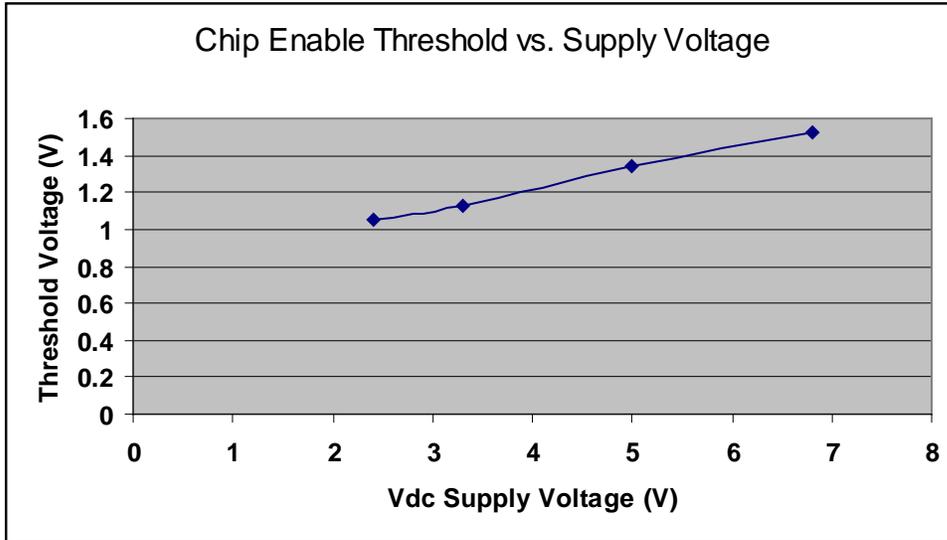
PARAMETER	SYMBOL	MIN	TYP ^[1]	MAX	UNITS	CONDITIONS
Signal-to-Noise Ratio	SNR		100		dB	0dB gain, 5Vdc
Load Impedance	R _{L(SPK)}		4		Ω	
Output Offset Voltage			8		mV	

PARAMETER	SYMBOL	MIN	TYP ^[1]	MAX	UNITS	CONDITIONS (THD+N)
Output Power (BTL mode) Load 4Ω V _{DD} =5 Vdc / 0dB gain	P _{BTL}		600		mW	<0.1% distortion
	P _{BTL}		1600		mW	<1% distortion
	P _{BTL}		2000		mW	<10% distortion

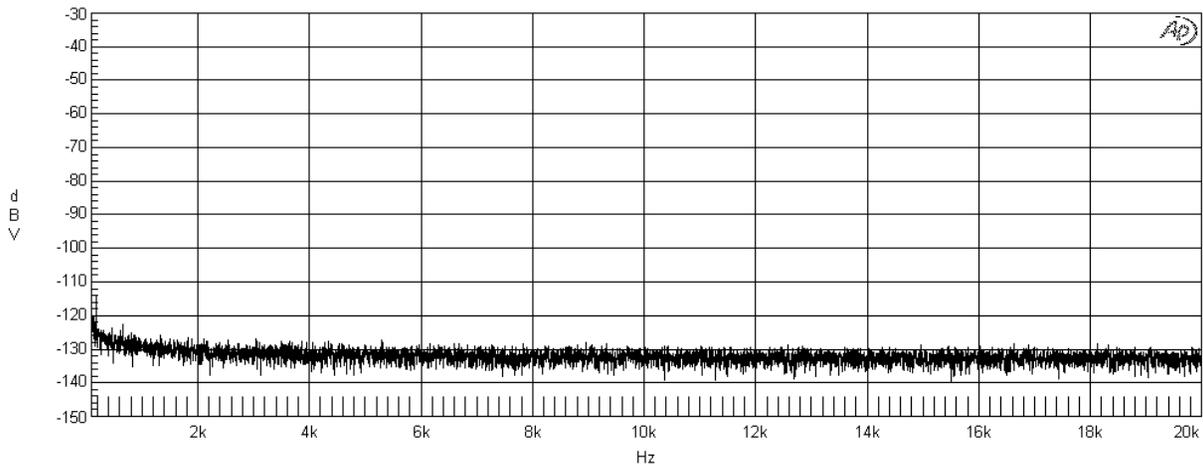
PARAMETER	SYMBOL	MIN	TYP ^[1]	MAX	Units	Conditions (THD+N)
Output Power (BTL mode) Load 8Ω V _{DD} =5 Vdc / 0dB gain	P _{BTL}		600		mW	<0.1% distortion
	P _{BTL}		1200		mW	<1% distortion
	P _{BTL}		1400		mW	<10% distortion

Notes: ^[1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by thermal design of the system.

6.3.3 Chip Enable Threshold Voltage

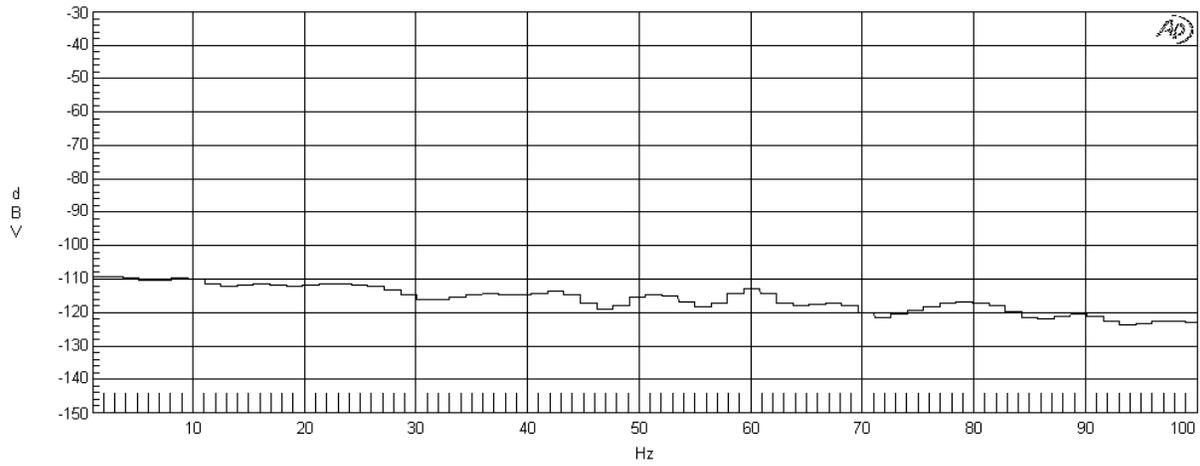


6.3.4 Output Noise Spectrum



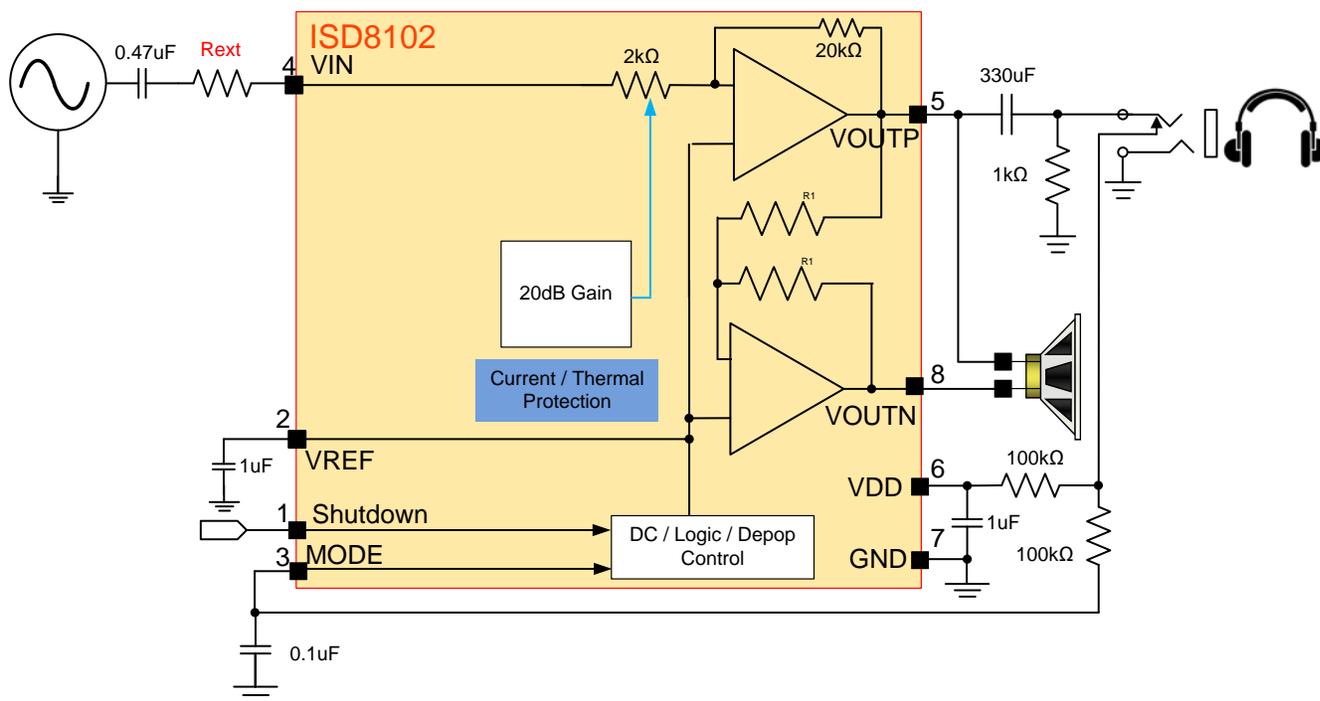
Noise spectrum at $V_{DD} = 5.0V_{dc}$, Gain = 0dB, BW<22kHz

Noise Spectrum at $V_{DD} = 5.0V_{dc}$, Gain = 20dB, BW<22kHz



7 APPLICATION

7.1 GAIN SETTING – ISD8102



Differential Output Gain (VOUTP – VOUTN) =

$$2 \times \frac{20\text{k}\Omega}{2\text{k}\Omega + R_{ext}}$$

By default: $R_{ext} = 0\Omega$,

ISD8102 Differential Output Gain = 20

ISD8102 Differential Output Gain (in dB) = $20 \times \log(20) = 26\text{dB}$

Example: $R_{ext} = 18\text{k}\Omega$

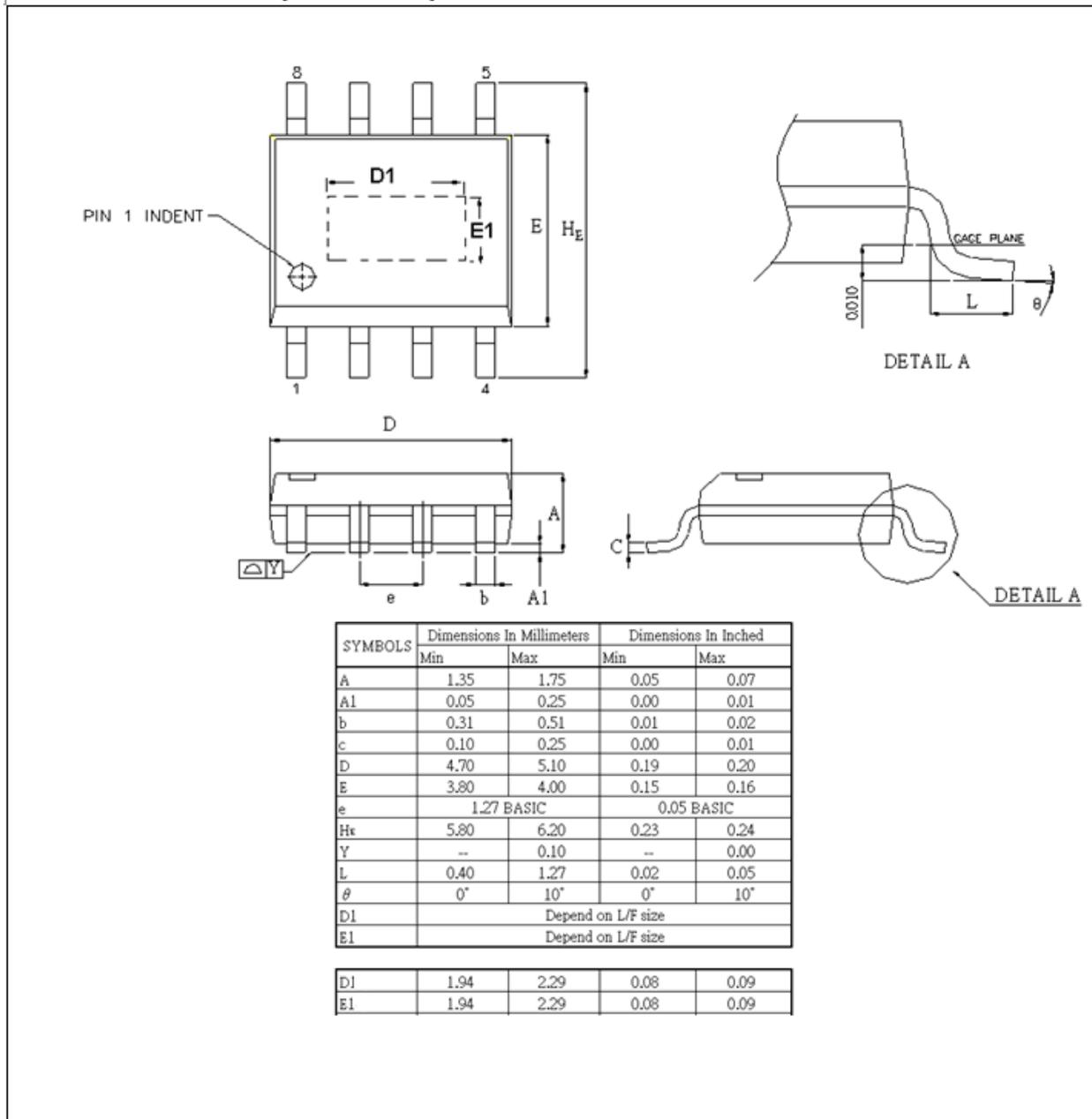
ISD8102 Differential Output Gain = 2

ISD8102 Differential Output Gain (in dB) = $20 \times \log(2) = 6\text{dB}$

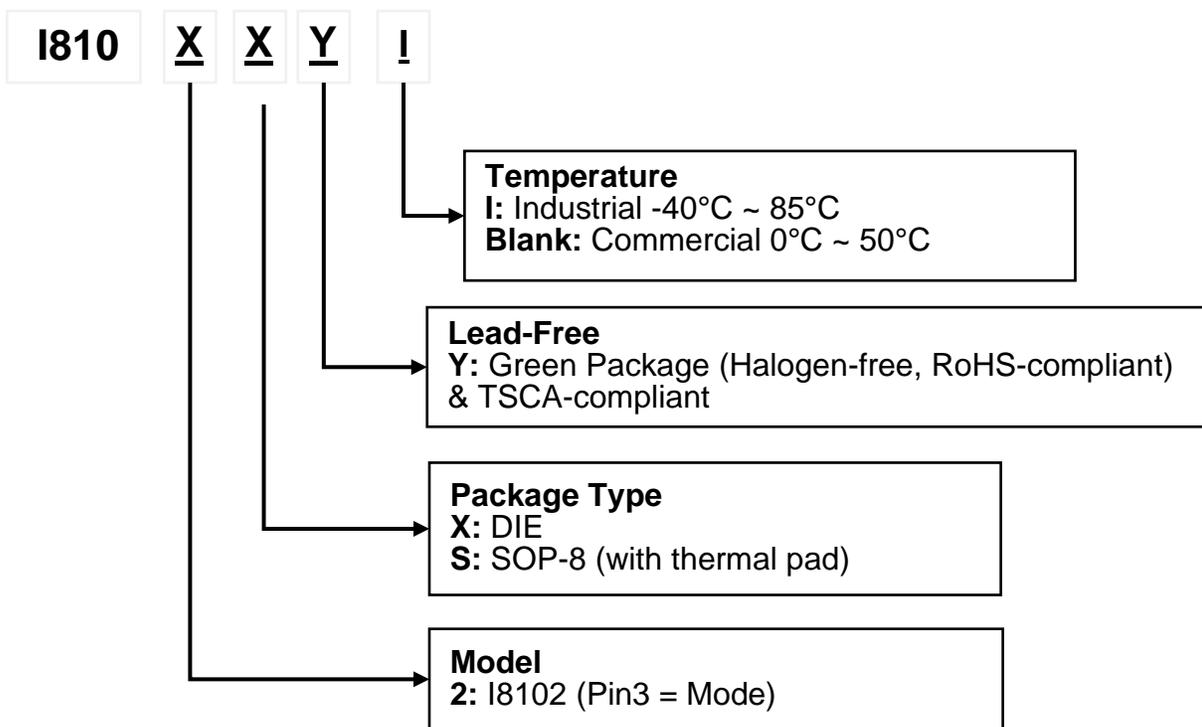
8 PACKAGE SPECIFICATION

8.1 SOP-8 (THERMAL EX-PAD)

8L SOP-150mil (EX-PAD)



9 ORDERING INFORMATION



Part Number	Package	Temperature	Notes
I8102X	DIE	0°C ~ 50°C	
I8102SYI	SOP-8 (Thermal Pad)	-40°C ~ 85°C	

10 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Apr 11, 2022	Initial Release
1.1	Feb 1, 2023	Update Halogen-free, RoHS-compliant and TSCA-compliant description
1.2	May 21, 2024	Update Operation Voltage

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