Analog Reinvented

ES9842 PRO

32-bit High-Performance 4-Channel ADC

Product Datasheet

The SABRE® ES9842 PRO is the world's highest performance 32-bit analog-to-digital (A/D) converter targeted for professional audio applications such as very high-quality recording systems, mixer consoles and digital audio workstations (DAW), test equipment, instruments, audio processors, digital turntables, and consumer applications.

The ES9842 PRO has 4 integrated ADCs which use the ESS proprietary Hyperstream® II Architecture, which delivers unprecedented SABRE HiFi® audio sound quality and specifications, including a True DNR of +128dB in mono mode and a True DNR +122dB THD+N of -116dB in 4 channel mode.

The SABRE® ADC supports synchronous S/PDIF, I²S master/slave, or native DSD output. For the most demanding audio enthusiast, the ES9842 PRO is capable of outputting RAW data, allowing the user to apply their own custom handling of the data. The ES9842 PRO comes in a small compact package and consumes less than 210mW.

The ES9842 can use preprogramed filter coefficients to match perfectly with the SABRE® PRO Series of DACs including the ES9038PRO. These complimentary filters allow for analog-digital-analog processing with the upmost audio fidelity and minimized time-domain smearing.

The Audio Signal Processor (ASP) integrated in the ADC allows for custom filtering such as RIAA presets to be implemented in the ADC, eliminating the need for re-processing later in the signal path.

The ES9842 PRO has an Ultra-Low Noise Floor Bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition, enabling higher resolution at higher sample rates.

FEATURE	DESCRIPTION
+122dB DNR 4 channel mode, +128dB DNR in mono mode -116dB THD+N 4 channel mode -118dB THD+N mono mode	Unprecedented dynamic range and ultra-low distortion
High Sample Rates	Up to PCM 768kHz, including 1.536MHz rate w/64FS Up to DSD512
Audio Signal Processors (ASP)	Available for custom FIR filters for any applications, including RIAA
Multiple Output formats available	PCM, TDM, DSD, S/PDIF, RAW
Customizable filter characteristics	8 presets and programmable filter coefficients for custom sound signature 2 audio signal processors for custom filter architectures and analog/digital mixing
I²C or SPI interface control	Configured by microcontroller or used as standalone
Integrated low noise ADC reference regulators	Reduced BOM cost, PCB area and improved DNR.
Low Power Consumption	Simplifies power supply design
Low Pin Count standardized Packaging	5mm x 5mm, 40 pin QFN
Ultra-Low Noise Floor Bandwidth	200kHz bandwidth enabling higher resolution at higher sample rates

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Functional Block Diagram

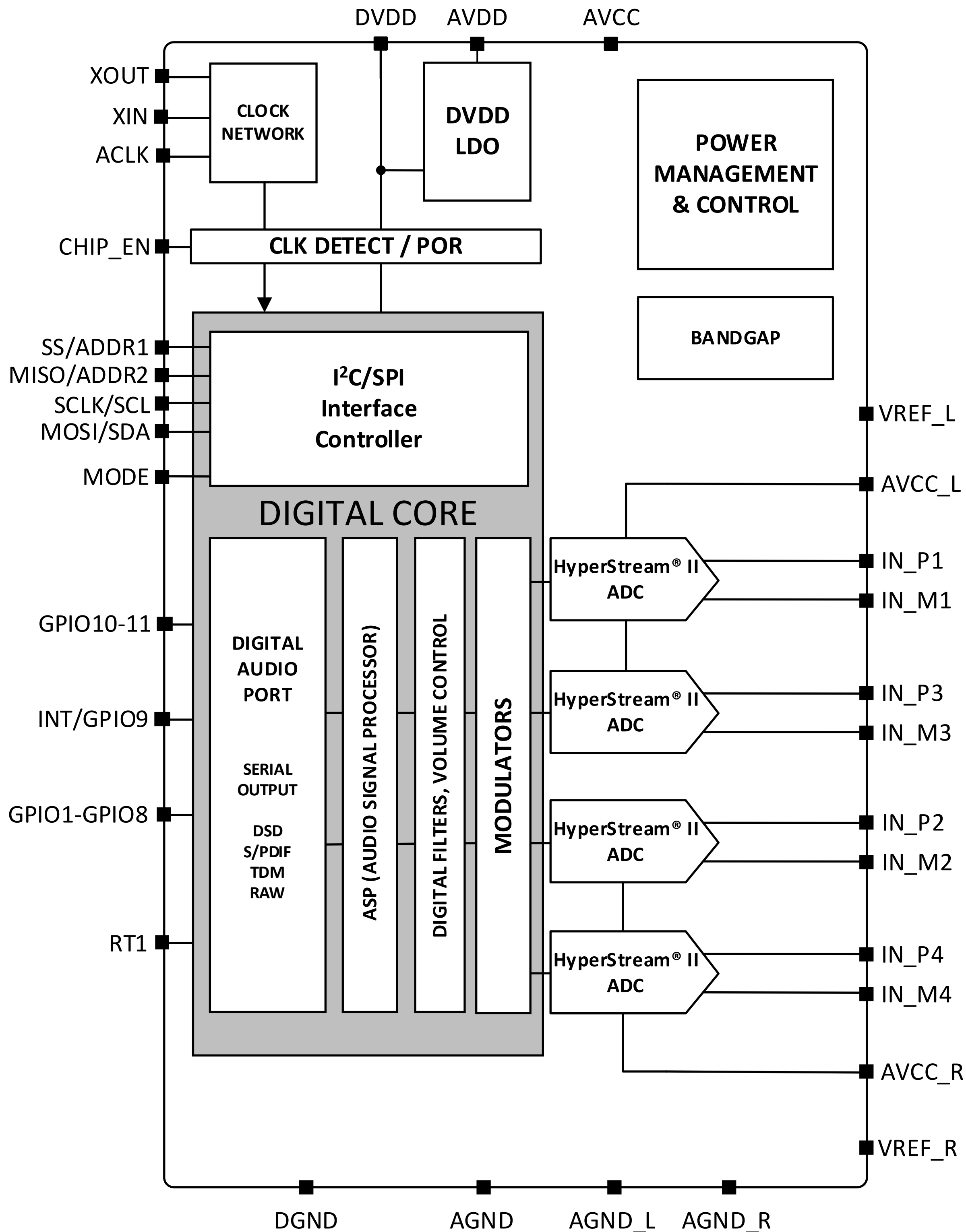


Figure 1 - ES9842 PRO Block Diagram

ES9842QPRO Package

40 QFN Pinout

(Pin 41 is QFN package pad, see package dimensions)

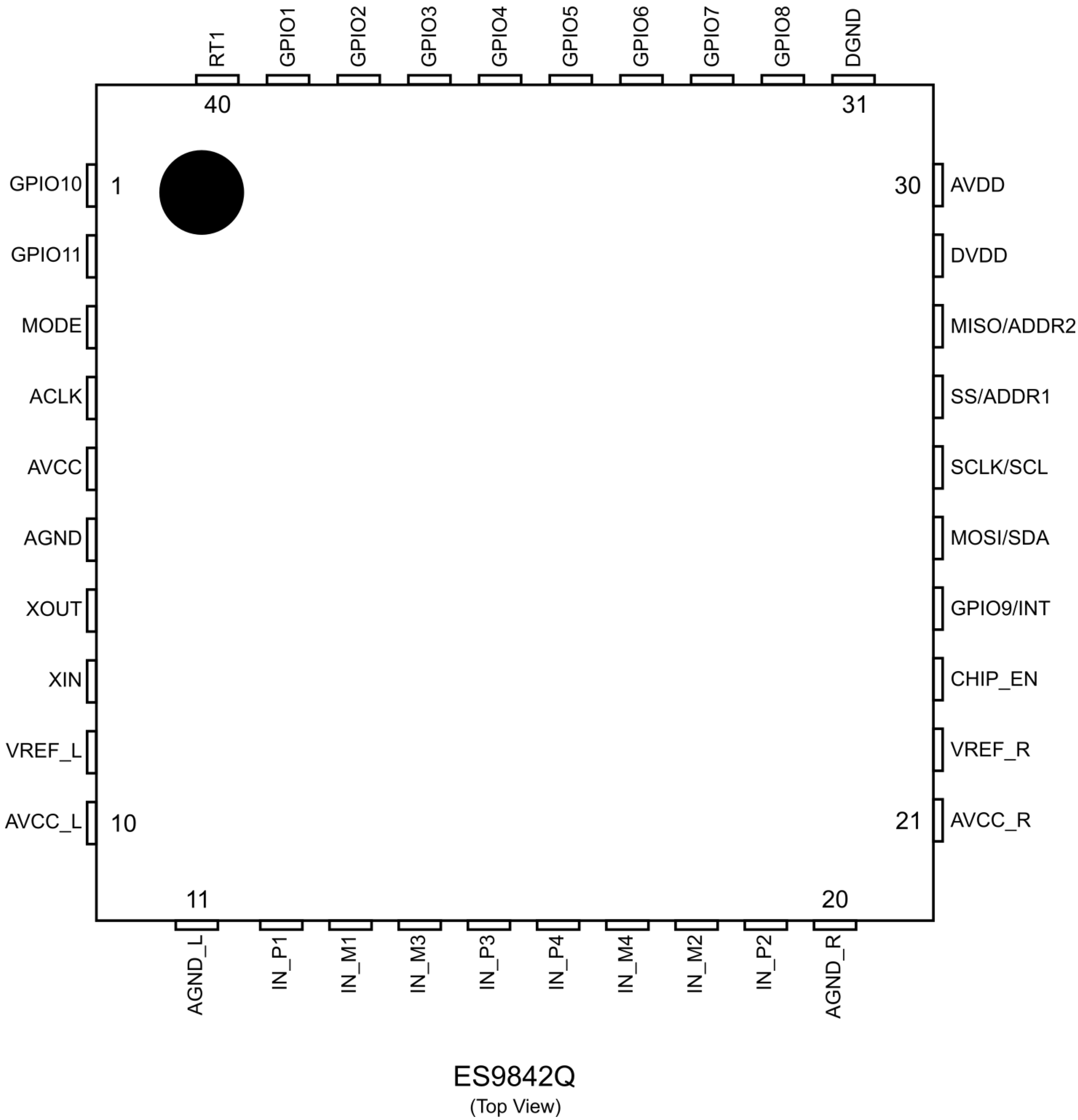


Figure 2 - 40 QFN Pinout

40 QFN Pin List

Pin	Name	Pin Type	Reset State	Pin Description
1	GPIO10	I/O	HiZ	General I/O w/extended functions
2	GPIO11	I/O	HiZ	General I/O w/extended functions
3	MODE	I/O	HiZ	I²C or SPI Control
4	ACLK[1]	AI	HiZ	Auxiliary Clock Input
5	AVCC	Power	Power	4.5V Supply
6	AGND	Ground	Ground	Analog Ground
7	XOUT	AO	HiZ	Crystal Output
8	XIN[1]	AI	HiZ	Crystal Input/Oscillator Input
9	VREF_L	Power	Power	Capacitor to ground (see reference schematic)
10	AVCC_L	Power	Power	ADC reference voltage 4.5V Supply
11	AGND_L	Ground	Ground	Analog Ground
12	IN_P1	AI	HiZ	ADC Channel 1 differential positive (+) input
13	IN_M1	AI	HiZ	ADC Channel 1 differential negative (-) input
14	IN_M3	AI	HiZ	ADC Channel 3 differential negative (-) input
15	IN_P3	AI	HiZ	ADC Channel 3 differential positive (+) input
16	IN_P4	AI	HiZ	ADC Channel 4 differential positive (+) input
17	IN_M4	AI	HiZ	ADC Channel 4 differential negative (-) input
18	IN_M2	AI	HiZ	ADC Channel 2 differential negative (-) input
19	IN_P2	AI	HiZ	ADC Channel 2 differential positive (+) input
20	AGND_R	Ground	Ground	Analog Ground
21	AVCC_R	Power	Power	ADC reference voltage 4.5V Supply
22	VREF_R	Power	Power	Capacitor to ground (see reference schematic)
23	CHIP_EN	I/O	HiZ	Active-high chip enable.
24	GPIO9	I/O	HiZ	General I/O w/extended functions, including INT (INTERRUPT)
25	MOSI	I/O	HiZ	SPI Main Out Sub In pin, controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
26	SCLK	I/O	HiZ	SPI Serial Clock pin, controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
27	SS	I/O	HiZ	SPI Slave Select pin, controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE
28	MISO	I/O	HiZ	SPI Main In Sub Out pin, controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
29	DVDD	Power	Power	Digital Core Supply. Internally Supplied
30	AVDD	Power	Power	3.3V, I/O Supply
31	DGND	Ground	Ground	Digital Core Ground
32	GPIO8	I/O	HiZ	General I/O w/extended functions, Serial Data 8
33	GPIO7	I/O	HiZ	General I/O w/extended functions, Serial Data 7
34	GPIO6	I/O	HiZ	General I/O w/extended functions, Serial Data 6
35	GPIO5	I/O	HiZ	General I/O w/extended functions, Serial Data 5
36	GPIO4	I/O	HiZ	General I/O w/extended functions, Serial Data 4

[1] MCLK can be connected to XIN or ACLK

37	GPIO3	I/O	HiZ	General I/O w/extended functions, Serial Data 3
38	GPIO2	I/O	HiZ	General I/O w/extended functions, Serial Data 2
39	GPIO1	I/O	HiZ	General I/O w/extended functions, Serial Data 1
40	RT1	I	HiZ	Reserved. Must be connected to DGND for normal operation.
41	Package Pad[1]	-	-	Not electrically connected, used for heat dissipation. Connect to DGND

Table 1 - 40 QFN Pin List

[1] Pin 41 is the package pad. See 40 QFN package dimensions for sizing. Connect to GND.

Interface Modes

The ES9842 PRO registers can be accessed either using an I²C or SPI interface.

The MODE pin (Pin 3) determines which interface will be used.

I²C Slave/Synchronous Slave Interface Commands

The I²C Slave/Synchronous Slave interface is used when the MODE pin (Pin 3) is pulled low.
The I²C interface can be accessed using Pin 25, 26, 27 and 28.

- Pin 25 SDA
- Pin 26 SCL
- Pin 27 ADDR1
- Pin 28 ADDR2

The ADDR1 (Pin 27) and ADDR2 (Pin 28) pins determine the I²C address.
The R/W bit determines the command type, Read (1) or Write (0).

- I²C Slave Address = [5'b01000, ADDR2, ADDR1, R/W]
- I²C Synchronous Slave Address = [5'b01001, ADDR2, ADDR1, R/W]

Note: The I²C Slave interface requires an MCLK present to function, the I²C Synchronous Slave interface does not.

I²C Slave Address	**I²C Synchronous Slave Address**	**ADDR2**	**ADDR1**
0x40	0x48	Tie Low	Tie Low
0x42	0x4A	Tie Low	Tie High
0x44	0x4C	Tie High	Tie Low
0x46	0x4E	Tie High	Tie High

Table 2 - I²C Slave/Synchronous Slave Addresses

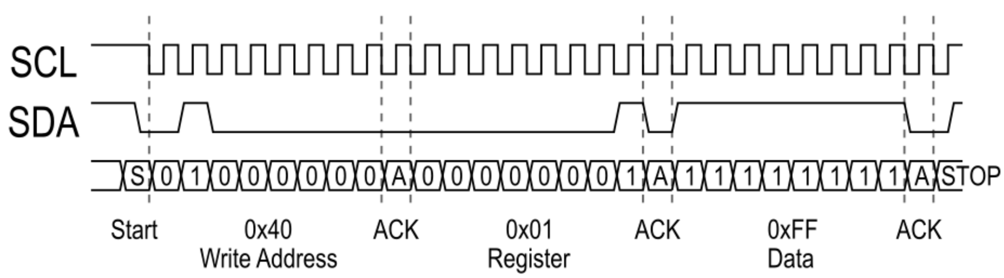


Figure 3 - I²C Write Example

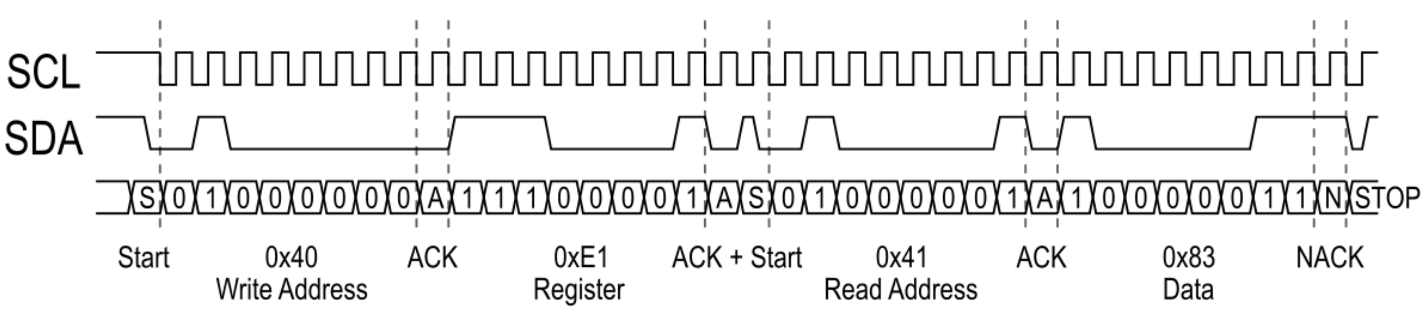


Figure 4 - I²C Read Example

SPI Slave Interface Commands

The SPI slave interface is used when the MODE pin (Pin 3) is pulled high.

The SPI Slave interface can be accessed using the Pins 25-28.

- Pin 25 MOSI
- Pin 26 SCLK
- Pin 27 SS
- Pin 28 MISO

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data

SPI commands:

- 0x01: Read
- 0x03: Write
- 0x07: Write-only Register Addresses 192-194 (0xC0 - 0xC2)

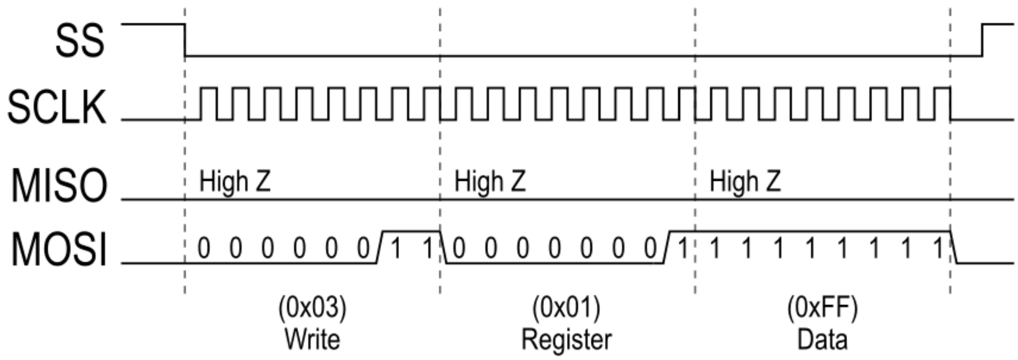


Figure 5 - SPI Single Byte Write

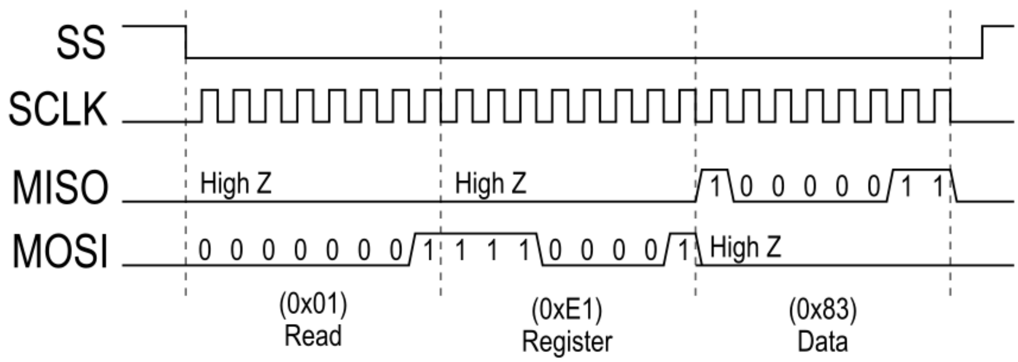


Figure 6 - SPI Single Byte Read

Digital Features

Audio Input/Output Formats

The ES9842 PRO supports multiple serial input/output formats. The output format is determined by Register 0[6:5] OUTPUT_SEL.

Pins are configured in Master (AUX Output) or Slave (Aux Input) mode through GPIO Configurations.

The formats include:

- PCM (Output)
  - Slave and Master mode in 16, 32 - bit widths
  - I²S, Left Justified (LJ)
  - Sample rates up to 768kHz (64fs mode)
  - Channel remapping
- PCM (Input)
  - Slave and Master mode in 16, 24 - bit widths
  - I²S
  - Sample rates up to 768kHz (64fs mode)
- TDM (Output)
  - 2 to 32 slots including daisy chain mode
  - Slave and Master mode in 16, 32 - bit widths
  - I²S, Left Justified (LJ)
  - Channel remapping
- DSD (Output)
  - Slave and master mode
  - Sample rates from DSD64 (2.8224Mbits/s, 64x44.1kHz) to DSD512
  - Channel mapping
- S/PDIF (Output)
- RAW (Output)

PCM/TDM Encoder

The ES9842 PRO integrates PCM/TDM Encoder whose output has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bits (default). The encoder allows for I²S, LJ, and TDM output streams.

The PCM/TDM Encoder can support up to 32 different slots and each channel of the ADC can be mapped to any of the 32 slots.

PCM/TDM Encoder Registers

- Register 10[7:3] TDM_BIT_DELAY
- Register 10[2] TDM_VALID_EDGE
- Register 10[1] TDM_LJ
- Register 10[0] ENABLE_TDM_CLK
- Register 11[7] TDM_GPIO456
- Register 11[6] TDM_CASCADE
- Register 11[5] TDM_LENGTH
- Register 11[4:0] TDM_CH_NUM

PCM/TDM Encoder Mapping Registers

- Register 12-15[6:5] TDM_LINE_SEL_CHx
- Register 12-15[4:0] TDM_SLOT_SEL_CHx

PCM/TDM Encoder Master Mode Registers

- Register 7[7:5] MASTER_WS_SCALE
- Register 8[7] MASTER_BCK_DIV1
- Register 8[6] MASTER_WS_IDLE
- Register 8[5:4] MASTER_FRAME_LENGTH
- Register 8[3] MASTER_WS_PULSE_MODE
- Register 8[2] MASTER_BCK_INVERT
- Register 8[1] MASTER_WS_INVERT
- Register 8[0] MASTER_MODE_ENABLE
- Register 9[7] SELECT_I²S_TDM_HALF
- Register 9[6:0] SELECT_I²S_TDM_NUM

I²S Decoder and Programmable Delay

The ES9842 PRO features a built in I²S decoder that can be mixed with the ASP. A programmable delay is also included to help with phase correction when mixing. Mixing is accomplished using the ASP. The I²S decoder input has a maximum word width of 32-bits (default) and a maximum bit depth of 24-bit (default). The Delay Line truncates the signal to 16-bit depth.

I²S Decoder Configuration Registers

- Registers 59-60: I²S DECODER CONFIG

Programmable Delay Registers

- Registers 62-61[9]: ENABLE_CLK_DL
- Registers 62-61[8:0]: PROG_DELAY_LINE

Configuration Pins for I²S Decoder

- GPIO 1: BCK
- GPIO 2: WS
- GPIO 5: DATA (would be configured as an AUX Input through the GPIO configuration)

Note: The I²S Decoder does not explicitly have a master mode enable bit and as a result will follow the same master mode setting as the PCM/TDM Encoder.

PCM (I²S, LJ) Format

See Bit-Clock (BCK) and Word-Select (WS) Timing for timing criteria.
Configure GPIO input/output through registers 74 - 76, 86 - 89. Must have Reg 11[7] TDM_GPIO456 Enabled.

Pin Name	Function	Description
GPIO1	PCM BCLK	PCM Clock (Master or Slave)
GPIO2	PCM WS	PCM WS (Master or Slave)
GPIO3	PCM DATA1	PCM DATA1 out (selectable for 2 channels)
GPIO4	PCM DATA2	PCM DATA2 out (selectable for 2 channels)

Table 3 - PCM Output Pin Connections

I²S Input Format

See Bit-Clock (BCK) and Word-Select (WS) Timing for timing criteria.
Configure GPIO input/output through registers 74 - 76, 86 - 89. Must have Reg 11[7] TDM_GPIO456 Enabled.

Pin Name	Function	Description
GPIO1	I²S BCLK	I²S Clock (Master or Slave)
GPIO2	I²S WS	I²S WS (Master or Slave)
GPIO5	I²S DATA	I²S DATA In

Table 4 - I²S Output Pin Connections

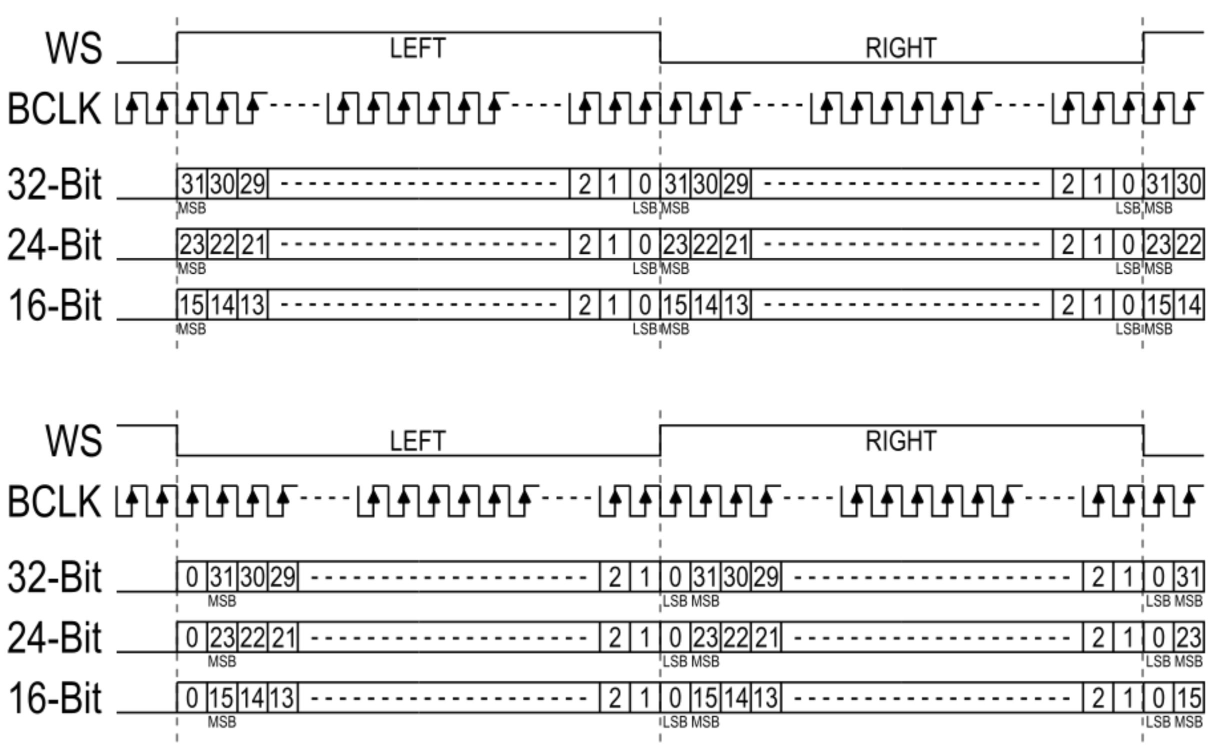


Figure 7 - LJ (top) & I²S (bottom) for 16, 24, and 32-bit Word Widths

TDM Format

See Bit-Clock (BCK) and Word-Select (WS) Timing for timing criteria.

See Registers 10-15 for configuration, can select GPIO 3-6 for the datapath.

Configure GPIO input/output through registers 74 - 76, 86 - 89. Must have Reg 11[7] TDM_GPIO456 Enabled.

Pin Name	Function	Description
GPIO1	TDM BCK	TDM clock (Master or Slave)
GPIO2	TDM WS	TDM WS (Master or Slave)
GPIO3	TDM DATA	TDM DATA out (default)

Table 5 - TDM Output Pin Connections

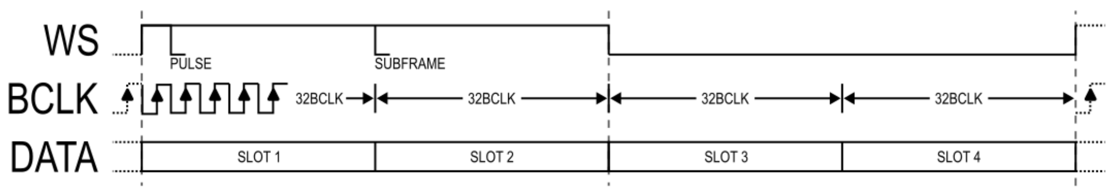


Figure 8 - TDM4 Mode

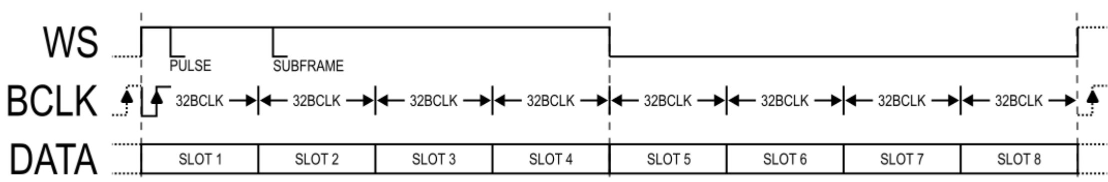


Figure 9 - TDM8 Mode

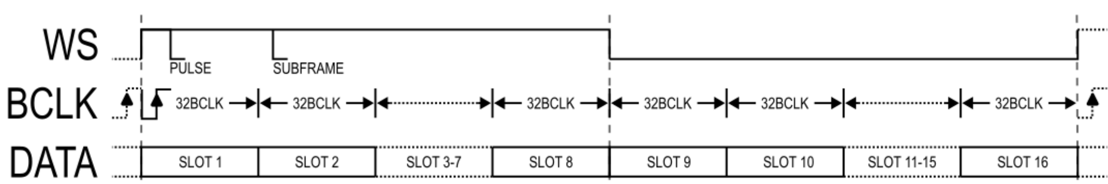


Figure 10 - TDM16 Mode

DSD Format

In DSD mode, there is a single DSD clock line, and each channel of data is an additional DSD data line. Each DSD source can be remapped to any output channel on a GPIO by using the below registers.

Configure GPIO input/output through registers 74 - 76, 86 - 89. Must have Reg 11[7] TDM_GPIO456 Enabled.

Pin Name	Function	Description
GPIO1	DSD Clock	DSD Bit Clock (Master or Slave)
GPIO3	DSD DATA out	DSD DATA1 (Channel 1 default)
GPIO4	DSD DATA out	DSD DATA2 (Channel 2 default)
GPIO5	DSD DATA out	DSD DATA3 (Channel 3 default)
GPIO6	DSD DATA out	DSD DATA4 (Channel 4 default)

Table 6 - DSD Output Pin Connections

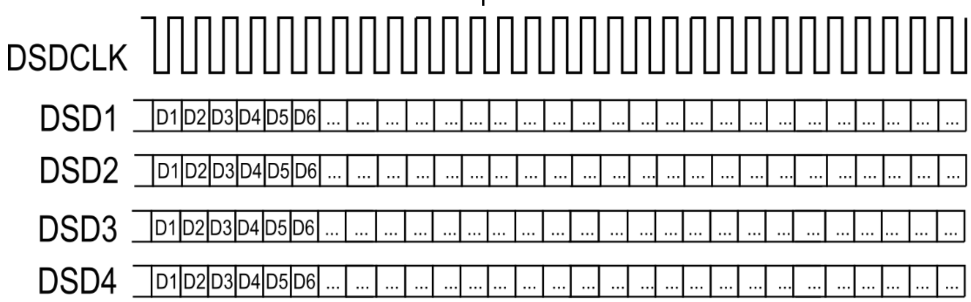


Figure 11 - 2CH DSD Format

DSD Config Registers:

- Register 6[5] DSD_DDR
- Register 6[4] DSD_MASTER_MODE
- Register 6[3] ENABLE_DSD_CLK_CH4
- Register 6[2] ENABLE_DSD_CLK_CH3
- Register 6[1] ENABLE_DSD_CLK_CH2
- Register 6[0] ENABLE_DSD_CLK_CH1
- Register 7[4] DSD_CLK_DIV2
- Register 7[3:0] SELECT_DSD_NUM

DSD Mapping Registers:

- Register 19[7:6] DSD_MAPPING_CH4
- Register 19[5:4] DSD_MAPPING_CH3
- Register 19[3:2] DSD_MAPPING_CH2
- Register 19[1:0] DSD_MAPPING_CH1

S/PDIF Format

S/PDIF output is stereo and uses Output Channel 1 and Output Channel 2. Channels can be remapped using Register 18[1:0] OUTPUT_MAPPING_CH1 and Register 18[3:2] OUTPUT_MAPPING_CH2.

Configure respective GPIOx_CFG through registers 74 - 76, 86 - 89. Must have Reg 11[7] TDM_GPIO456 enabled if using respective pins.

Note: Respective Register 74-76 GPIOx_CFG must be set to 4'd8 (S/PDIF Output)

Pin Name	Function	Description
GPIOx	S/PDIF OUT	S/PDIF OUT

Table 7 - S/PDIF Output Pin Connections

S/PDIF Config Registers:

- Register 5[2] ENABLE_SPDIF_CLK
- Register 28-32 SPDIF_CS

RAW Format

The ES9842 PRO can output the RAW data of the ADC onto GPIOs 1-8. The channel output from the RAW GPIOs is determined by the INPUT_DATA_MAPPING_CHx registers. The RAW data outputs are a single data rate (SDR) of the remapped CH1, and by setting RAW_DATA_DDR the RAW data outputs become double data rate (DDR), with the mapped CH1 on the falling edge, and the mapped CH2 on the rising edge of the RAW data clock on GPIO1.

The RAW clock rate on GPIO1 is required to be 22.5792 (512 x 44.1kHz) / 24.576MHz (512 x 48kHz) respectively by setting RAW_DATA_CLK_DIV2 when using a 45.1584/49.152MHz SYS_CLK.

Configure respective GPIOx_CFG through registers 74 - 77, 88 - 89.

Pin Name	Function	Description
GPIO1	RAW Data Clock Output	Clock output in RAW mode
GPIO2	RAW Data [0] Output	Raw data bit 0 (LSB)
GPIO3	RAW Data [1] Output	Raw data bit 1
GPIO4	RAW Data [2] Output	Raw data bit 2
GPIO5	RAW Data [3] Output	Raw data bit 3
GPIO6	RAW Data [4] Output	Raw data bit 4
GPIO7	RAW Data [5] Output	Raw data bit 5
GPIO8	RAW Data [6] Output	Raw data bit 6 (MSB)

Table 8 - RAW Output Pin Connections

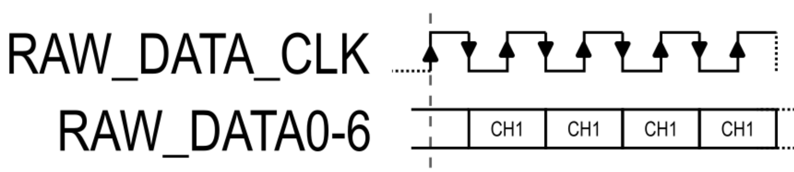


Figure 12 - 1CH RAW Single Data Rate Format

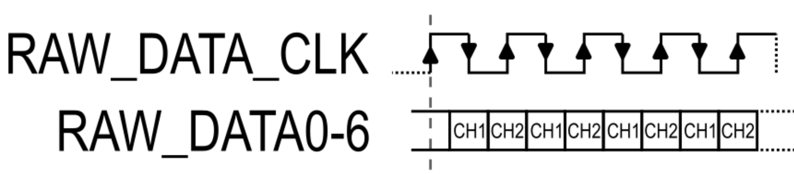


Figure 13 - 2CH RAW Double Data Rate Format

<u>RAW Config Registers:</u>

- Register 5[5] RAW_DATA_CLK_DIV2
- Register 5[4] RAW_DATA_DDR
- Register 5[3] ENABLE_RAW_DATA_CLK

<u>RAW Mapping Registers:</u>

- Register 17[3:2] INPUT_DATA_MAPPING_CH2
- Register 17[1:0] INPUT_DATA_MAPPING_CH1

GPIO

GPIO#_CONFIG	Function	I/O Direction
0	Analog Shutdown	Shutdown (default)
1	Aux Inputs	Inputs
2	Aux Outputs	Output
3	RAW Data Outputs	Output
4	Interrupt Ch1 Peak	Output
5	Interrupt Ch2 Peak	Output
6	Interrupt Ch3 Peak	Output
7	Interrupt Ch4 Peak	Output
8	SPDIF data output	Output
9	PWM1	Output
10	PWM2	Output
11	PWM3	Output
12	CLK IADC	Output
13	CLK ADC	Output
14	1'b0	Output
15	1'b1	Output

Table 9 - Standard GPIO Functions

For configuring pins as Inputs, Outputs, or Input/Outputs:

- Input Pin
  - Registers 87-86: GPIOxx_IE = 1'b1 (Input Enable),
  - Registers 89-88: GPIOxx_OE = 1b'0 (Output Enable),
- Output Pin
  - Registers 87-86: GPIOxx_IE = 1'b0
  - Registers 89-88: GPIOxx_OE = 1'b1
- In/Out Pin (Master Mode)
  - Registers 87-86: GPIOxx_IE = 1'b1
  - Registers 89-88: GPIOxx_OE = 1'b1

In Master mode GPIO1 & GPIO 2 should be configured as In/Out pins.

Data pins may be re-mapped to other GPIO via the System Registers. When utilizing GPIO pins 4-6, it is important to enable the TDM_GPIO456 bit.

GPIO 4-6 TDM Enable Register

- Register 11[7]: TDM_GPIO456

GPIO Configuration Registers

- Register 74: GPIO1/2 CONFIG
- Register 75: GPIO3/4 CONFIG
- Register 76: GPIO5/6 CONFIG
- Register 77: GPIO7/8 CONFIG
- Register 78: GPIO9/10 CONFIG
- Registers 80-91

GPIO Audio Data Configurations

The following table shows the configurations possible using GPIO#_config Aux Inputs, Aux Outputs, and RAW data outputs on the ES9842 PRO.

In certain modes, the data output pins may be re-mapped to GPIO pins 4-6. These scenarios are labeled "[optional]" in the table below. The channel order may also be changed in these modes. Although it is not denoted in the table, the data output in Slave Mode may also be re-mapped to the same pins.

<table>
<tr><th>GPIO #</th><th>4'b1
(AUX Inputs)
(Slave mode)</th><th colspan="4">4'd2
(AUX Outputs)
(Master mode)</th><th>4'd3
(Raw Data Output)</th><th>4'b8
(S/PDIF Output)</th></tr>
<tr><td>GPIO1</td><td>I^2S /TDM in BCK, DSD in clock</td><td>I^2S master BCK</td><td>TDM master BCK</td><td>DSD master clock out</td><td>PDM[1] clock</td><td>Raw Data Clock output</td><td rowspan="6">S/PDIF Data</td></tr>
<tr><td>GPIO2</td><td>I^2S /TDM in WS</td><td>I^2S master WS</td><td>TDM master WS</td><td>-</td><td>-</td><td>Raw Data[0] out</td></tr>
<tr><td>GPIO3</td><td>-</td><td>I^2S out DATA [optional][2] (default)</td><td>TDM out DATA [optional][2] (default)</td><td>DSD out DATA[3]</td><td>PDM[1] out DATA</td><td>Raw Data[1] out</td></tr>
<tr><td>GPIO4</td><td>TDM cascade data input Cascade mode for multiple devices</td><td>I^2S out DATA [optional][2]</td><td>TDM out DATA [optional][2]</td><td>DSD out DATA[3]</td><td>PDM[1] out DATA</td><td>Raw Data[2] out</td></tr>
<tr><td>GPIO5</td><td>I^2S decoder data input</td><td>I^2S out DATA [optional][2]</td><td>TDM out DATA [optional][2]</td><td>DSD out DATA[3]</td><td>-</td><td>Raw Data[3] out</td></tr>
<tr><td>GPIO6</td><td>-</td><td>I^2S out DATA [optional][2]</td><td>TDM out DATA [optional][2]</td><td>DSD out DATA[3]</td><td>-</td><td>Raw Data[4] out</td></tr>
<tr><td>GPIO7</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Raw Data[5] out</td><td>-</td></tr>
<tr><td>GPIO8</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Raw Data[6] out</td><td>-</td></tr>
<tr><td>GPIO9</td><td>-</td><td colspan="4">INTERRUPT (Triggered by any of the 4 channels)</td><td>INTERRUPT</td><td>-</td></tr>
<tr><td>GPIO10</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>GPIO11</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
</table>

Table 10 - GPIO Audio Data Configurations

1 To enable PDM mode, set Register 6[5] DSD_DDR

2 Using the TDM GPIO Re-mapping Registers, the data may be configured to output GPIO pins 4-6. In order to do this, Register 11[7]: TDM_GPIO456 must also be enabled.

3 The DSD channel order can be changed via Register 19: DSD_DATA_OUTPUT_MAPPING.

Digital Signal Path

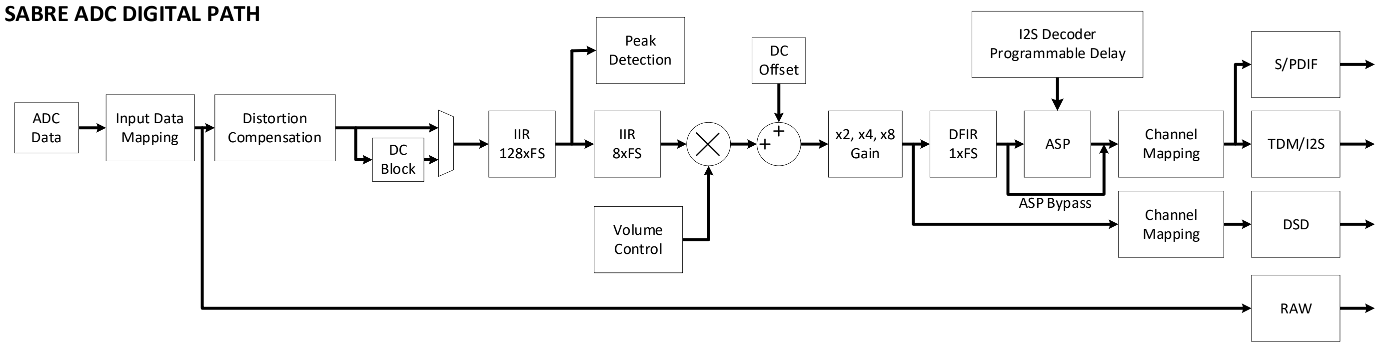


Figure 14 - Digital Signal Path

Input Data Mapping

Input ADC data can be mapped to any one of the four channels on the digital signal path.

Input Data Mapping Register

- Register 17[7:6]: INPUT_DATA_MAPPING_CH4
- Register 17[5:4]: INPUT_DATA_MAPPING_CH3
- Register 17[3:2]: INPUT_DATA_MAPPING_CH2
- Register 17[1:0]: INPUT_DATA_MAPPING_CH1

Distortion Compensation[1]

Distortion Compensation minimizes the non-linearities of the analog to digital data path. The ES9842 PRO can help compensate for system second and third harmonic distortion. For optimal results, compensation coefficients should be tuned for each device in-situ.

Distortion Compensation Enable Registers

- Register 102[0]: ADC1_ENABLE_THD_COMP
- Register 119[0]: ADC2_ENABLE_THD_COMP
- Register 136[0]: ADC3_ENABLE_THD_COMP
- Register 153[0]: ADC4_ENABLE_THD_COMP

DC Block

The integrated DC block exhibits a high cutoff frequency (-3dB @ 30Hz).

For customizable DC blocking filters with lower cutoff frequencies, use the integrated ASP. Ask your local FAE or Distributer for the DC Blocking Filter ASP Application Note.

DC Block Enable Registers

- Register 101[2]: ADC1_ENABLE_DC_BLOCKING
- Register 118[2]: ADC2_ENABLE_DC_BLOCKING
- Register 135[2]: ADC3_ENABLE_DC_BLOCKING
- Register 152[2]: ADC4_ENABLE_DC_BLOCKING

[1] For more information on using Distortion Compensation, please reference the Distortion Compensation Application Note. Available from your local FAE or Distributor upon request.

Peak Detection[1]

If the peak level of the ES9842 PRO input rises above the programmed ADCx_PEAK_LEVEL value, the corresponding peak flag will be set. The level will decay at a rate based off the value of ADCx_PEAK_DECAY_RATE. The peak detection can be toggled on or off using the ADCx_ENABLE_PEAK_DETECT registers. The peak flag will stay set until it is cleared with INTERRUPT_CLEAR_CHx_PEAK_DETECTION. GPIO pins can be configured to output the state of any peak flags if INTERRUPT_MASK_CHx_PEAK_ DETECTION is set for the corresponding channel.

Peak Level Registers

- Register 106: ADC CH1 PEAK DETECTOR LEVEL
- Register 123: ADC CH2 PEAK DETECTOR LEVEL
- Register 140: ADC CH3 PEAK DETECTOR LEVEL
- Register 157: ADC CH4 PEAK DETECTOR LEVEL

Peak Decay Rate Register

- Register 105[6:2]: ADC1_PEAK_DECAY_RATE
- Register 122[6:2]: ADC2_PEAK_DECAY_RATE
- Register 139[6:2]: ADC3_PEAK_DECAY_RATE
- Register 156[6:2]: ADC4_PEAK_DECAY_RATE

$$N(t) = N_0 exp\left(\frac{-FS * t}{2^{decay\_rate}}\right)$$

$$N(t) = N_0 - \frac{20 * FS * t}{ln(10) * 2^{decay\_rate}} [dB]$$

$$\frac{dN}{dt} = -\frac{N * FS}{2^{decay\_rate}} [1/s]$$

Peak Enable Register

- Register 105[0]: ADC1_ENABLE_PEAK_DETECT
- Register 122[0]: ADC2_ENABLE_PEAK_DETECT
- Register 139[0]: ADC3_ENABLE_PEAK_DETECT
- Register 156[0]: ADC4_ENABLE_PEAK_DETECT

Peak Interrupt Clear Registers

- Register 27[7:4]: INTERRUPT_CLEAR_CHx_PEAK_DETECTION

Peak Interrupt Mask Registers

- Register 27[3:0]: INTERRUPT_MASK_CHx_PEAK_DETECTION

The GPIO READBACK register values 4’d4 - 4’d7 output the peak interrupt state for CH1 to CH4, respectively. The corresponding channel bit in Register 27[3:0] INTERRUPT_CLEAR_CHx_PEAK_DETECTION needs to be set for the GPIO to output the flag value.

[1] For further information on using Peak Detection, please reference the Peak Detector Configuration Application Note. Available from your local FAE or Distributor upon request

Volume Control

This volume control is intended for use during audio playback. Each channel can be digitally attenuated from 0dB to -84dB in 0.5dB steps. The attenuation circuit automatically uses micro-stepping between 0.5dB register settings so that no switching noise occurs during the volume control transition. When a new volume level is set, the attenuation circuit will ramp softly to the new level. Each 0.5dB step takes up to 64 intermediate steps depending on the ADC CHx VOLUME RATE setting.

Volume Level Configuration Registers

- Register 109-110: ADC CH1 VOLUME
- Register 126-127: ADC CH2 VOLUME
- Register 143-144: ADC CH3 VOLUME
- Register 160-161: ADC CH4 VOLUME

Volume Rate Configuration Registers

- Register 111: ADC CH1 VOLUME RATE
- Register 128: ADC CH2 VOLUME RATE
- Register 145: ADC CH3 VOLUME RATE
- Register 162: ADC CH4 VOLUME RATE

DC Offset

The ES9842 PRO has a built in DC offset that can be used to add per channel DC offset. To achieve this, the 16-bit signed register must be set. To achieve a positive DC offset, the register must be within the range of 16’h0001(-120dB) to 16’h7FFF(-30dB). For a negative DC offset, the register must be within the range of 16’h8000(-30dB) to 16’hFFFF(-120dB).

The offset is set by using the following equation:

$$Offset[dB] = 20log_{10}\left(\frac{ADCx\_DC\_OFFSET}{(2^{15}-1)*2^{5}}\right)$$

DC Offset Registers

- Register 107-108: ADC1_DC_OFFSET
- Register 124-125: ADC2_DC_OFFSET
- Register 141-142: ADC3_DC_OFFSET
- Register 158-159: ADC4_DC_OFFSET

Digital Gain

The ES9842 PRO has an additional digital gain that can be added through registers. Settings for +6dB, +12dB or +18dB gain are available for each ADC channel.

Digital Gain Registers:

- Register 112[1:0]: ADC1_DATA_GAIN
- Register 129[1:0]: ADC2_DATA_GAIN
- Register 146[1:0]: ADC3_DATA_GAIN
- Register 163[1:0]: ADC4_DATA_GAIN

DFIR Filters

The ES9842 PRO has 8 preprogrammed digital filters. See Pre-Programmed Digital Filters section for more information.

Note: The DFIR Filters need to be resynced after sample rate changes. See Addendum for respective resync program.

Audio Signal Processor (ASP)[1]

The ES9842 PRO includes 2 stereo audio signal processors (ASP) which can be used to implement both custom filter coefficients as well as custom filter architectures. See Digital Signal Path diagram for location in the data path.

The ASP can be used to implement a DC blocking high pass, parametric equalizer (PEQ), and/or a RIAA filter.

ESS recommends using the ASP for DC Blocking function. See DC Blocking Filter Application note, available from your local FAE or Distributor upon request.

ASP Registers:

- Registers 35-58

Output Channel Mapping

TDM Channel Mapping Registers

- Register 12-15: TDM SLOT CONFIG CHx

PCM Channel Mapping Registers

- Register 18: PCM DATA OUTPUT MAPPING

DSD Channel Mapping Registers

- Register 19: DSD DATA OUTPUT MAPPING

SPDIF Mapping Registers

- Register 18[1:0] OUTPUT_MAPPING_CH1
- Register 18[3:2] OUTPUT_MAPPING_CH2

Note: SPDIF output only uses channels 1 and 2

[1] For help with designing with the ASP, please reference the ASP GUIDE Application Note. Available from your local FAE or Distributor upon request.

TDM Cascade Mode

The ES9842 PRO features TDM cascade mode. Cascade mode allows the digital output from one chip to be input (through GPIO4) to the next, and the last chip on the chain outputting the final data on serial data line. To enable TDM Cascade mode, set TDM_CASCADE to 1, and configure GPIO4 as input and GPIO3 as output. The figure below shows how several ES9842 PRO can be combined in TDM cascade mode.

Note: Cascade mode is for a minimum of an 8 channel TDM data line (TDM_CH_NUM ≥ 7).

Note: To ensure optimal performance, after setup of TDM Cascade Mode, the respective I²S or LJ Resync script must be written to all ES9842 PROs in Slave mode. See Addendum for the respective script.

Note: The TDM_IN (GPIO4) to the first ES9842 PRO must have no data on it. Ground for optimal performance.

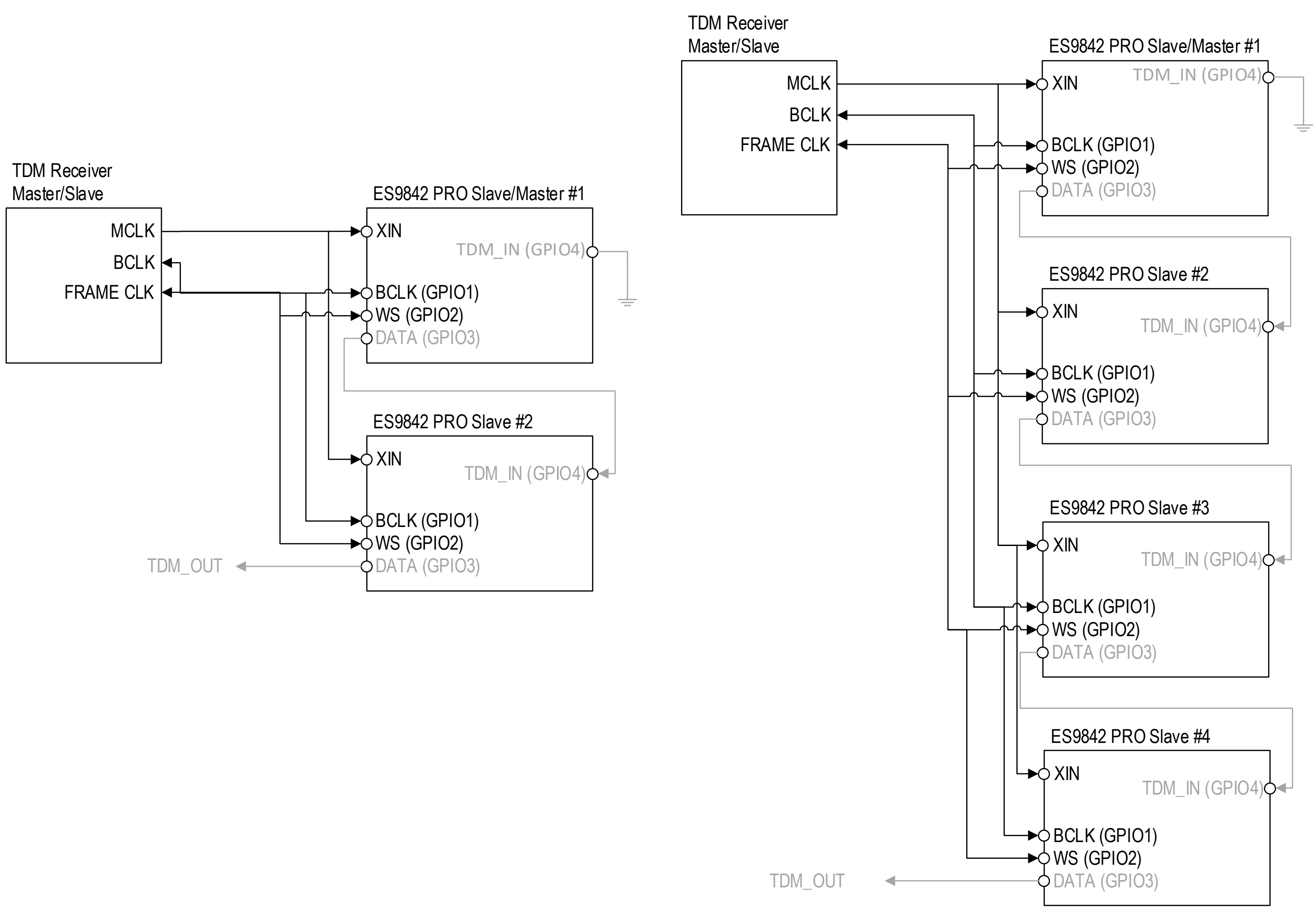
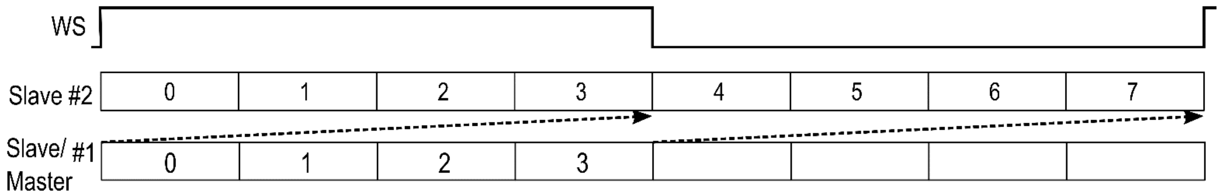


Figure 15 - Connection for TDM Cascade Mode

TDM Cascade Mode Registers:

- Register 11[6] TDM_CASCADE
- Register 11[4:0] TMD_CH_NUM

8 Channel TDM:



16 Channel TDM:

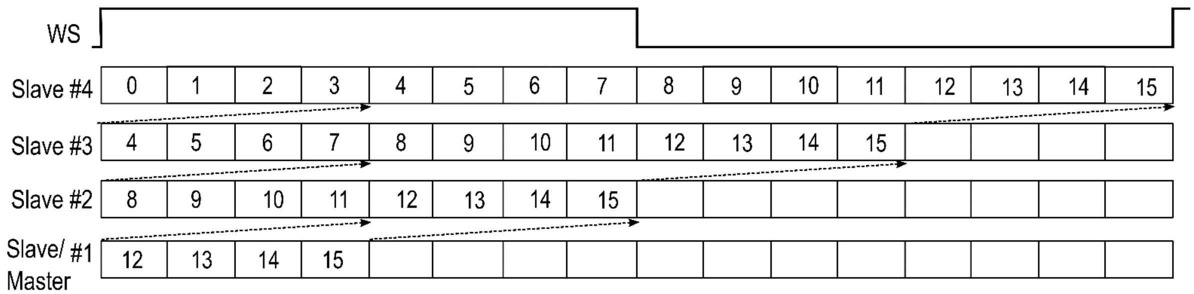


Figure 16 - Channel Cascading and Data Line Composition in TDM Cascade Mode

TDM / PCM Parallel Mode

The ES9842 PRO also supports TDM / PCM in parallel mode. In this case, the chips will simply connect the output data line together. Each chip will output data during the designated slots during a single frame of the TDM / PCM data line, then switch to high impedance so that the next chip may output its data onto the TDM data line. To set up TDM parallel mode, no specific registers are required.

Note: Parallel mode supports TDM and I²S (TDM_CH_NUM ≥ 1).

Note: To ensure optimal performance, after setup of TDM Parallel Mode, the respective I²S or LJ Resync script must be written to all ES9842 PROs in Slave mode. See Addendum for the respective script.

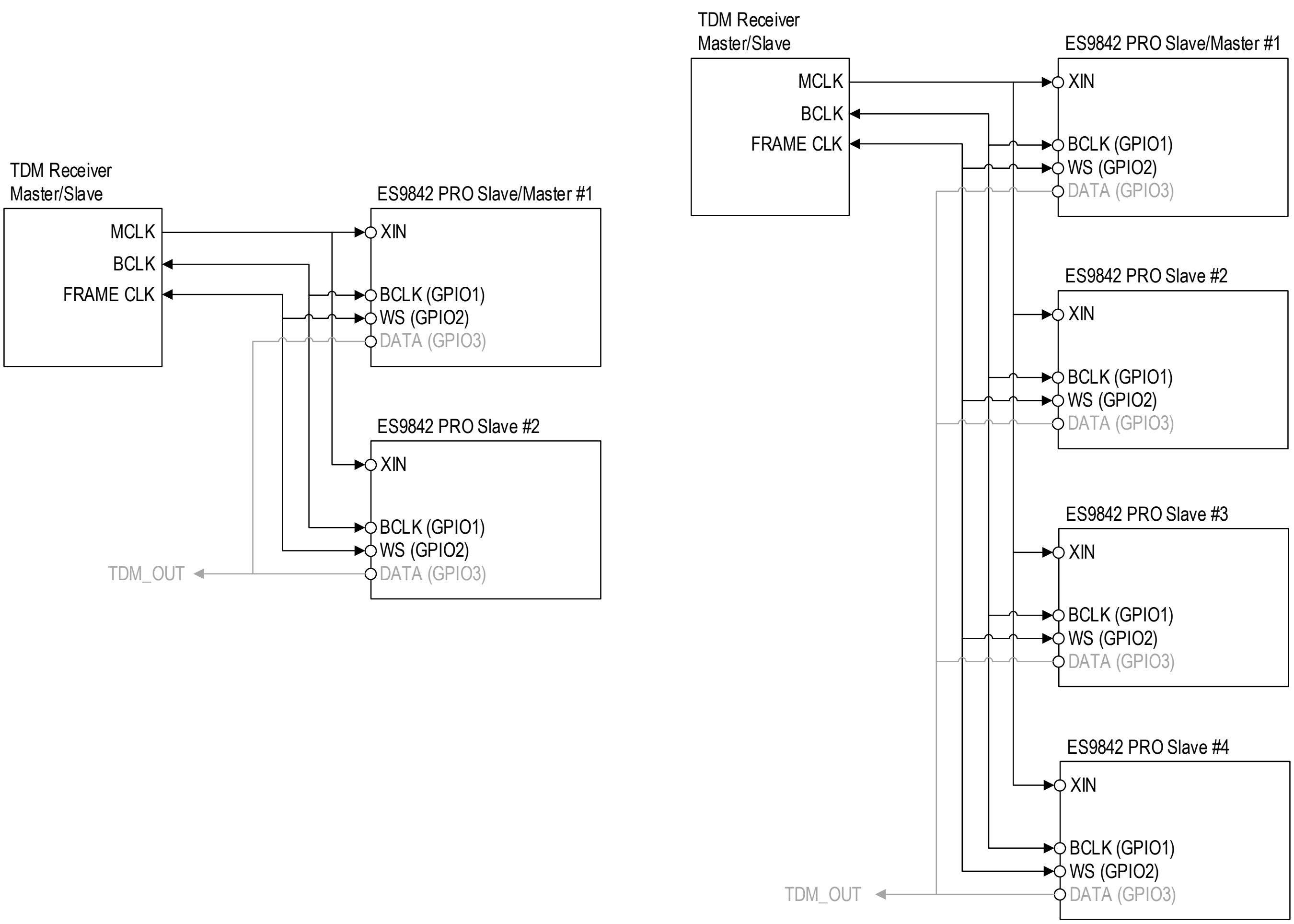
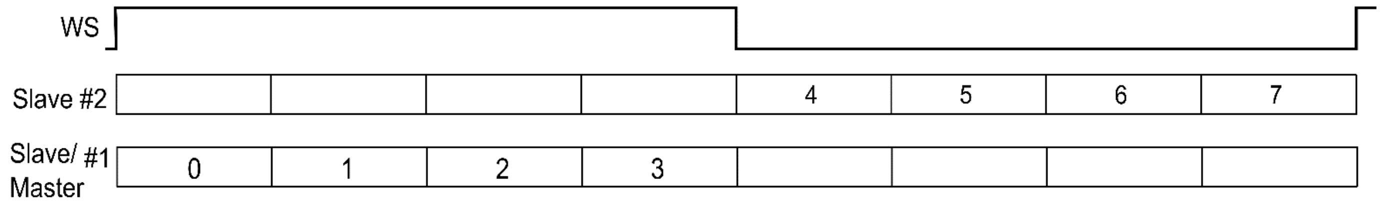


Figure 17 - Connection for Parallel TDM / PCM

8 Channel Mode:



16 Channel Mode:

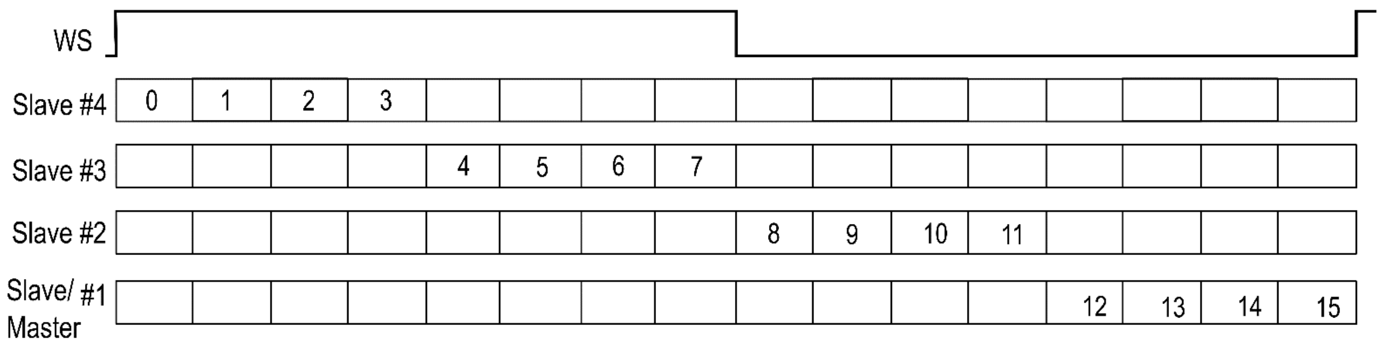


Figure 18 - Channel Mapping and Data Line Composition for TDM in Parallel Mode

Pre-Programmed Digital Filters

The ES9842 PRO has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 113[4:2] FILTER_SHAPE for configuration)

#	Filter	Description
1	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection
2	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55FS
4	Linear Phase Fast Roll-Off Low-Ripple	Sabre legacy filter, optimized for in-band ripple
5	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
6	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
7	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
8	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 11 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ FS = 44.1kHz
Minimum Phase (default)	142us
Linear Phase Apodizing Fast Roll-Off	805us
Linear Phase Fast Roll-Off	808us
Linear Phase Fast Roll-Off Low-Ripple	799us
Linear Phase Slow Roll-Off	184us
Minimum Phase Fast Roll-Off	128us
Minimum Phase Slow Roll-Off	105us
Minimum Phase Fast Roll-Off Low Dispersion	329us

Table 12 - PCM Filter Latency

PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3dB			0.48FS	Hz
Stop band	-103dB	0.55FS			Hz
Group Delay		3.43/FS		10.66/FS	s
Flatness (ripple)					dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41FS	Hz
Stop band	-109dB	0.50FS			Hz
Group Delay			33.25/FS		s
Flatness (ripple)	0.0022				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-115dB	0.55FS			Hz
Group Delay			33.38/FS		s
Flatness (ripple)	0.0025				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-82dB	0.55FS			Hz
Group Delay			33.00/FS		s
Flatness (ripple)	0.0009				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3dB			0.50FS	Hz
Stop band	-84dB	0.81FS			Hz
Group Delay			5.87/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3dB			0.48FS	Hz
Stop band	-96dB	0.54FS			Hz
Group Delay		2.91/FS		9.28/FS	s
Flatness (ripple)					dB

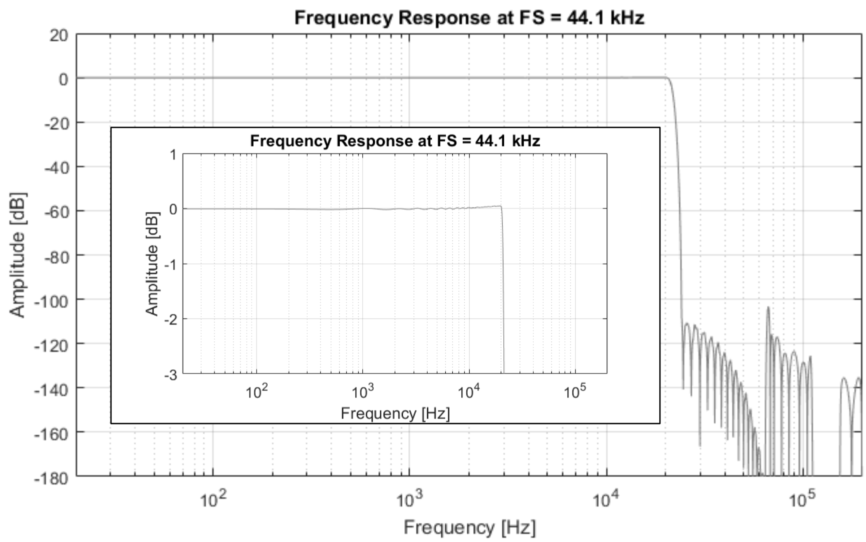
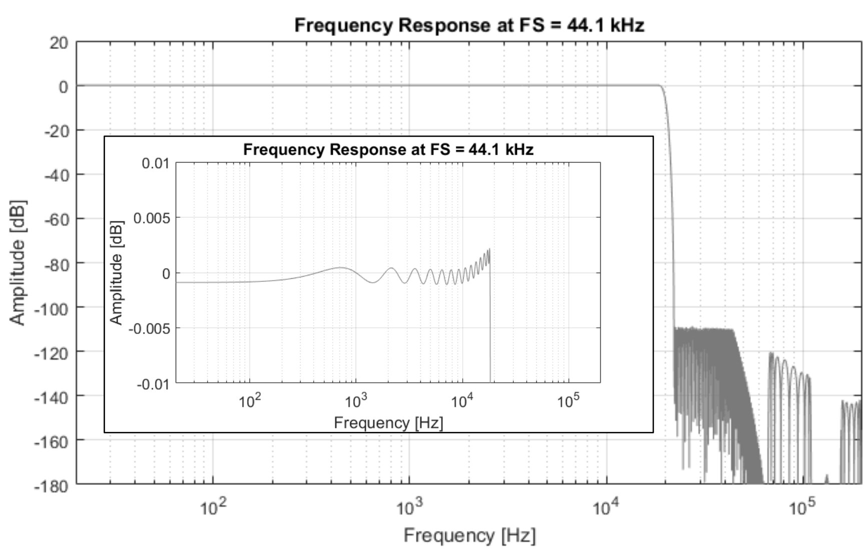
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3dB			0.43FS	Hz
Stop band	-90dB	0.79FS			Hz
Group Delay		2.03/FS		3.51/FS	s
Flatness (ripple)					dB

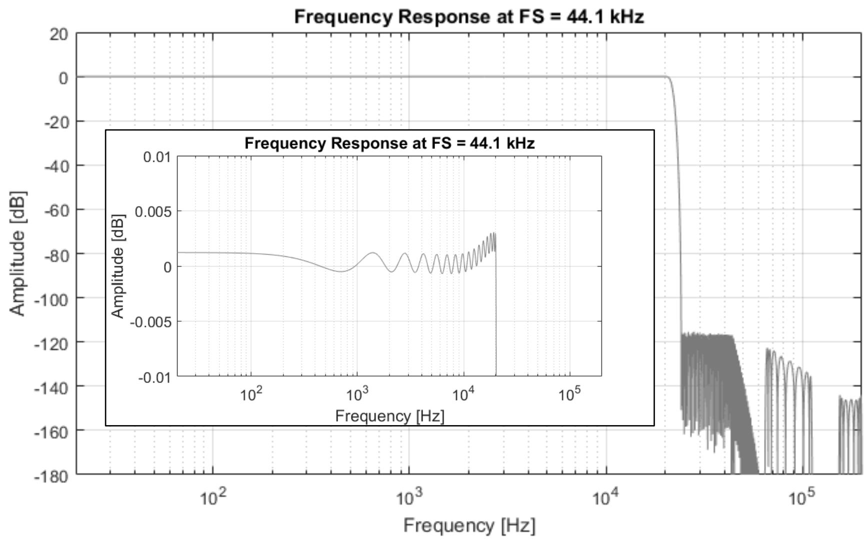
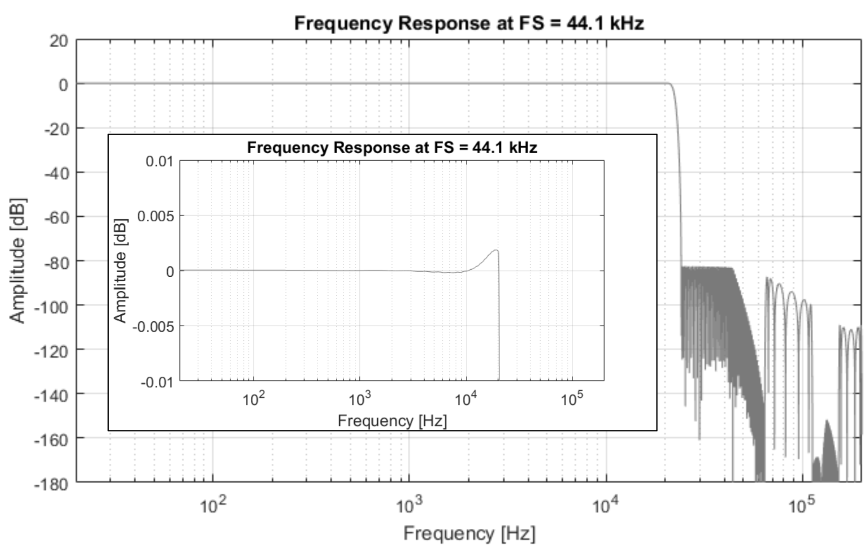
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3dB			0.43FS	Hz
Stop band	-90dB	0.80FS			Hz
Group Delay		12.13/FS		12.37/FS	s
Flatness (ripple)					dB

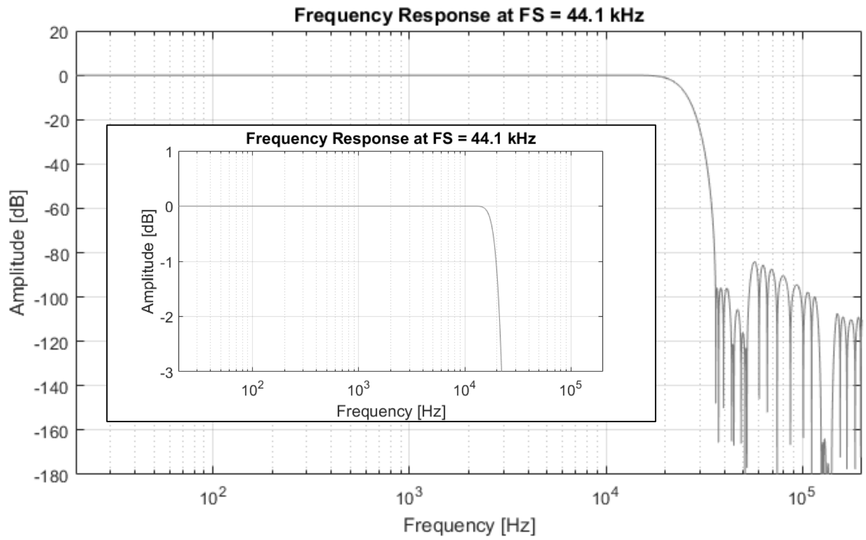
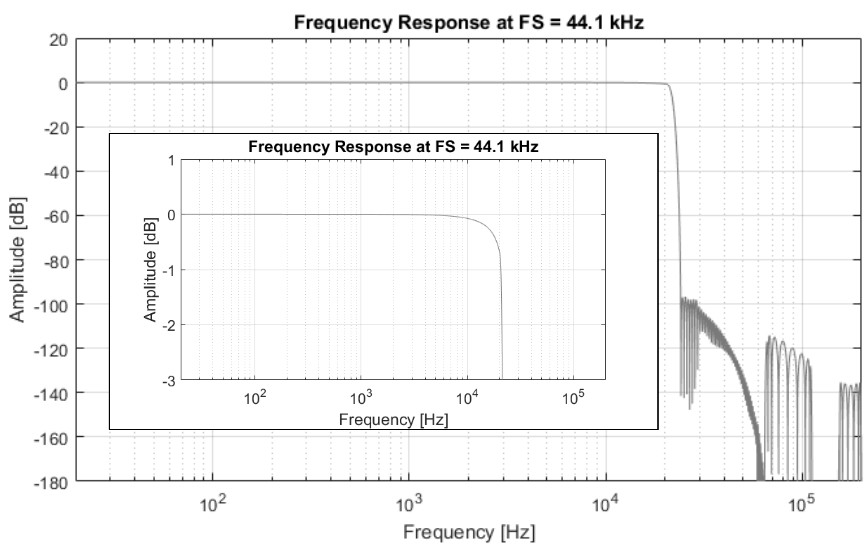
Table 13 - PCM Filter Properties

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

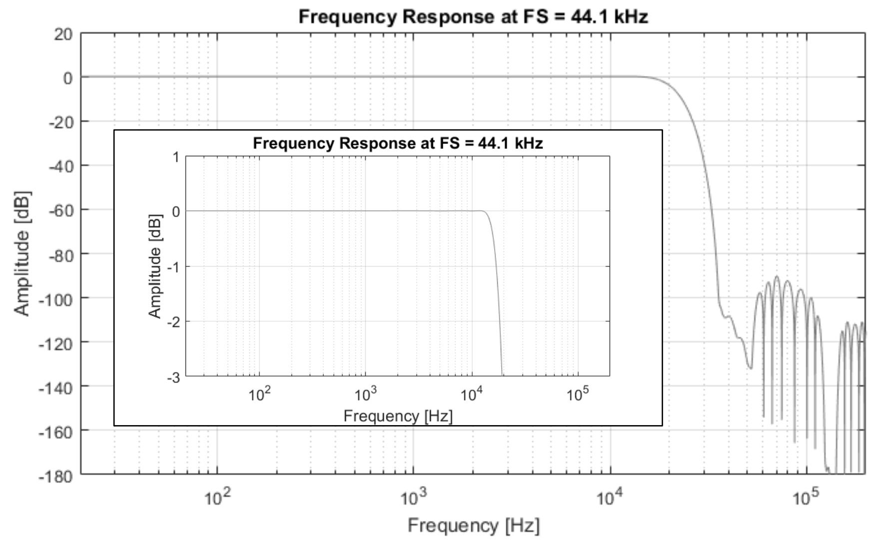
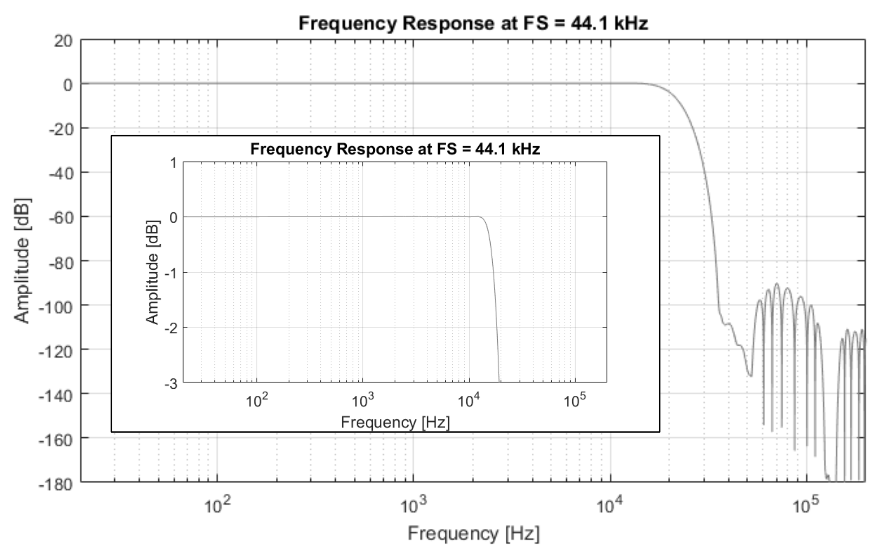
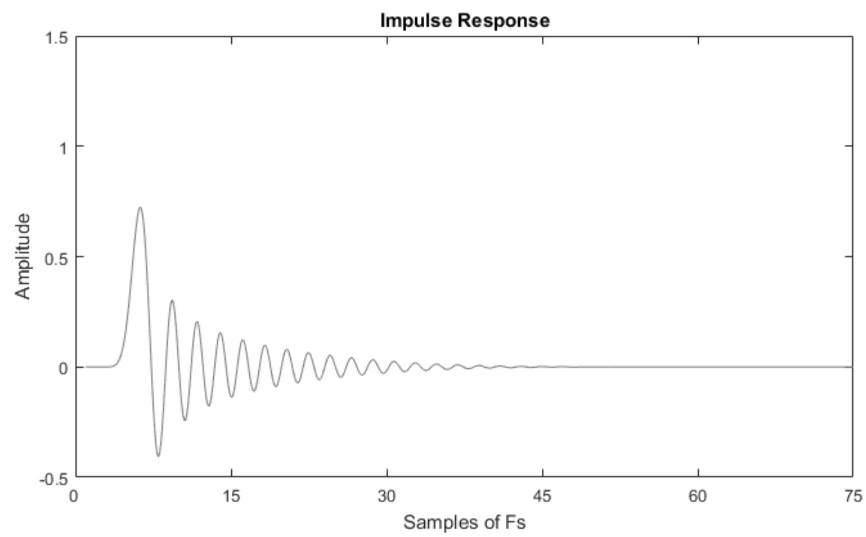
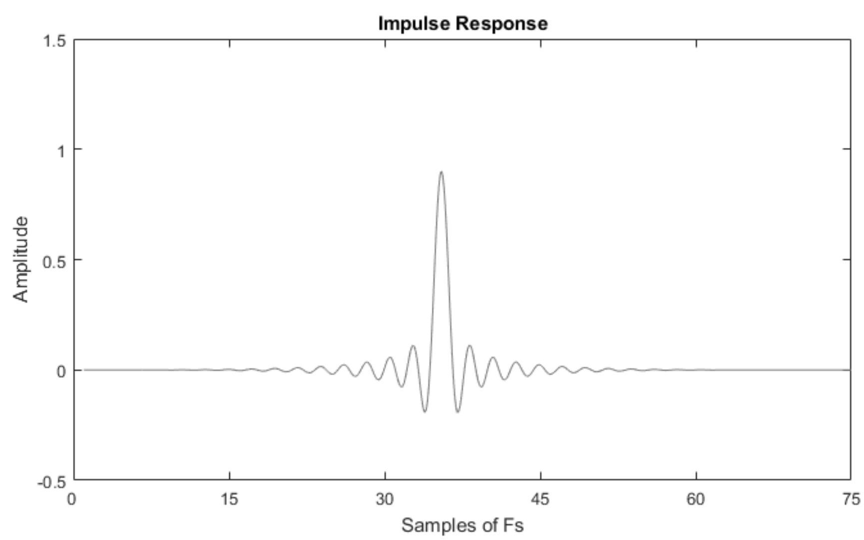
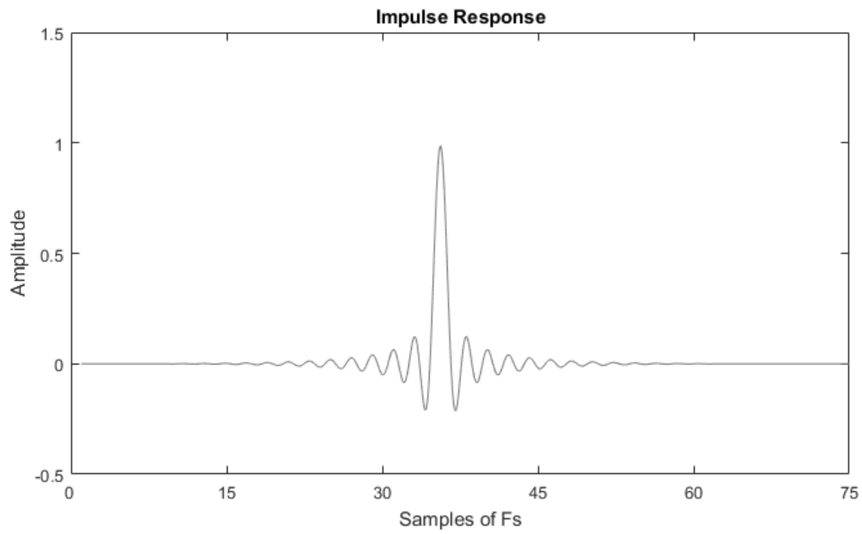
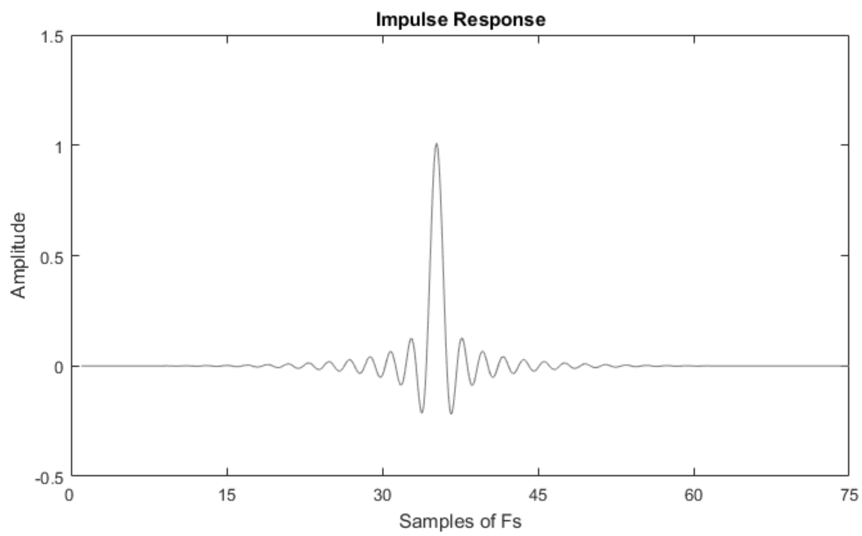
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

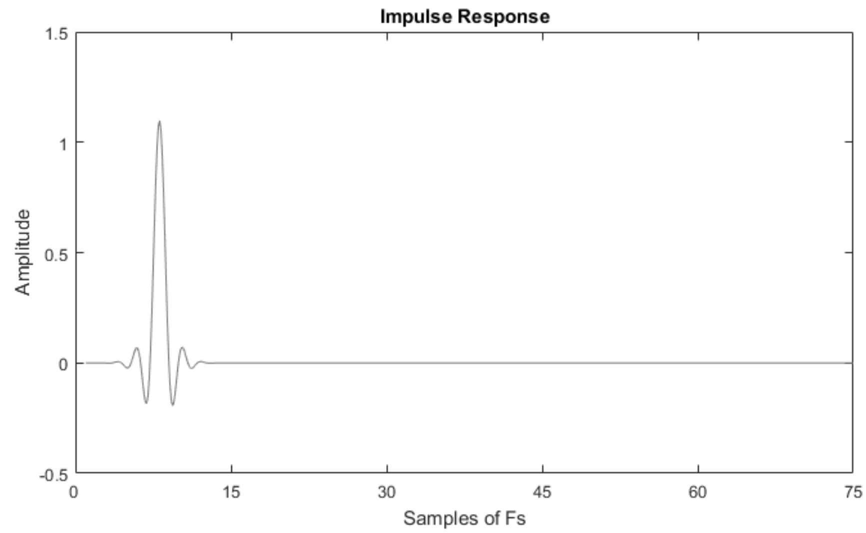
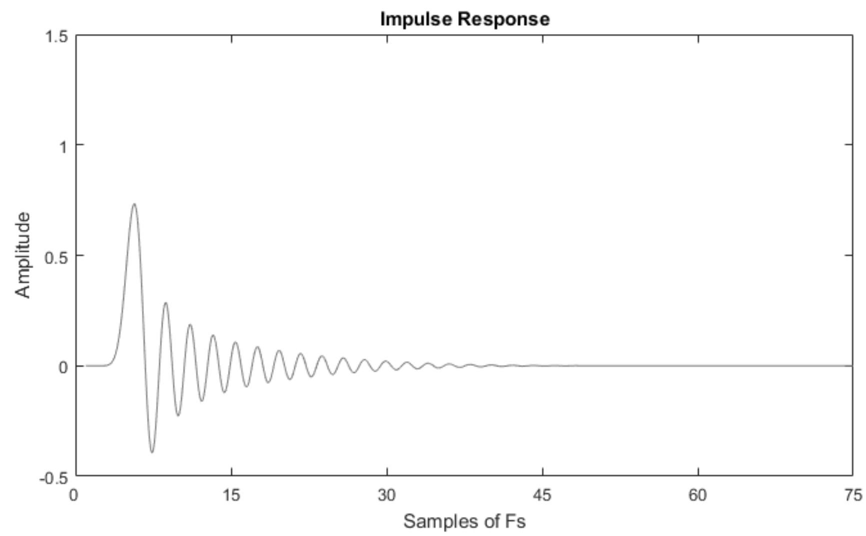
Table 14 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

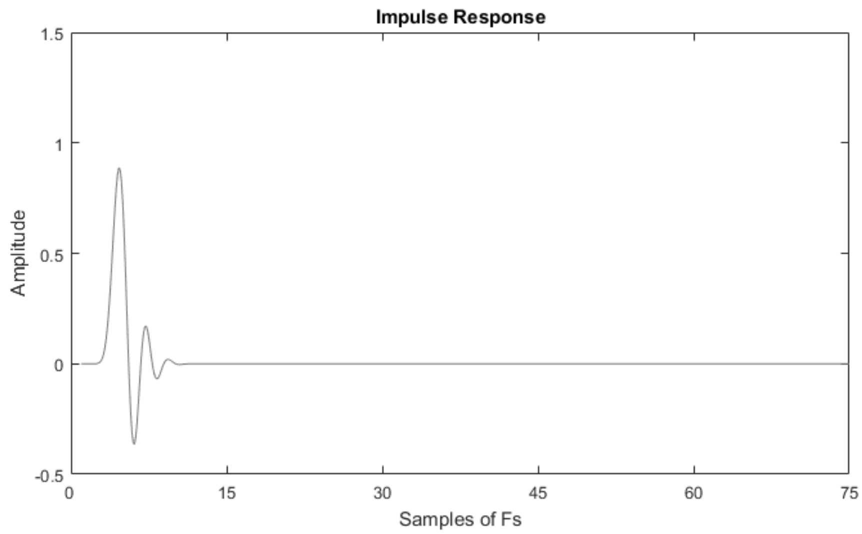
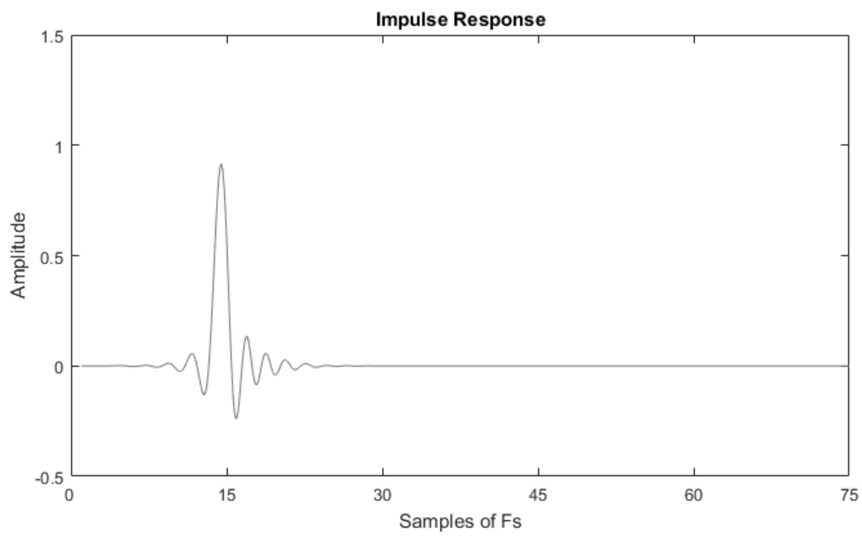
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 15 - PCM Filter Impulse Response

64FS Mode

When 64FS (MCLK/FS ratio) is required, it is necessary for the ES9842 PRO to be running in 64FS Mode. 64FS Mode can be manually entered by setting:

Software Register

- Register 0[3] ENABLE_64FS_MODE = 1’b1
  - Use for 64FS ratios, including 705.6/768kHz sample rates

This mode enables the Minimum Phase 64FS filter. See filter properties below.

Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ FS = 705.6 kHz
Minimum Phase 64FS	9.2us

Table 16 - Minimum Phase 64FS Latency

Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3dB			0.55FS	Hz
Stop band	-100dB	0.91FS			Hz
Group Delay		2.24/FS		4.03/FS	s
Flatness (ripple)					dB

Table 17 - Minimum Phase 64FS Properties

Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz.

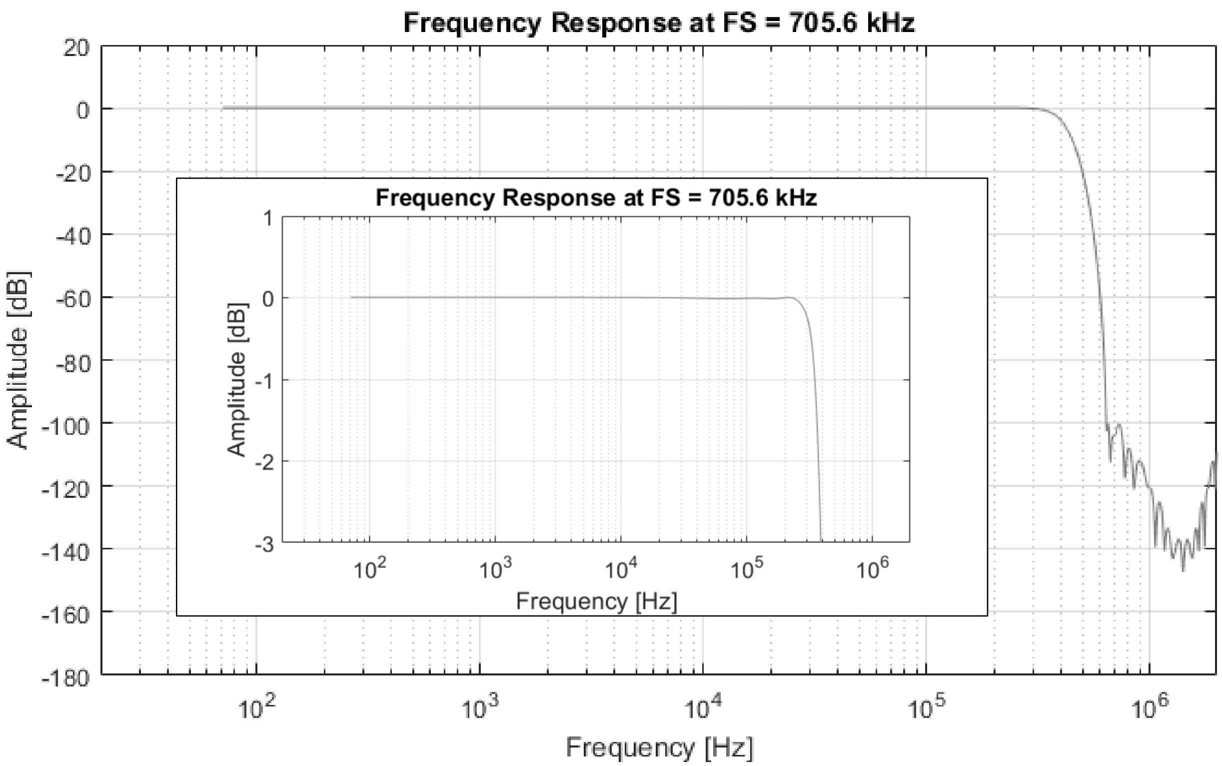


Figure 19 - Minimum Phase 64FS Frequency Response

Minimum Phase 64FS Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

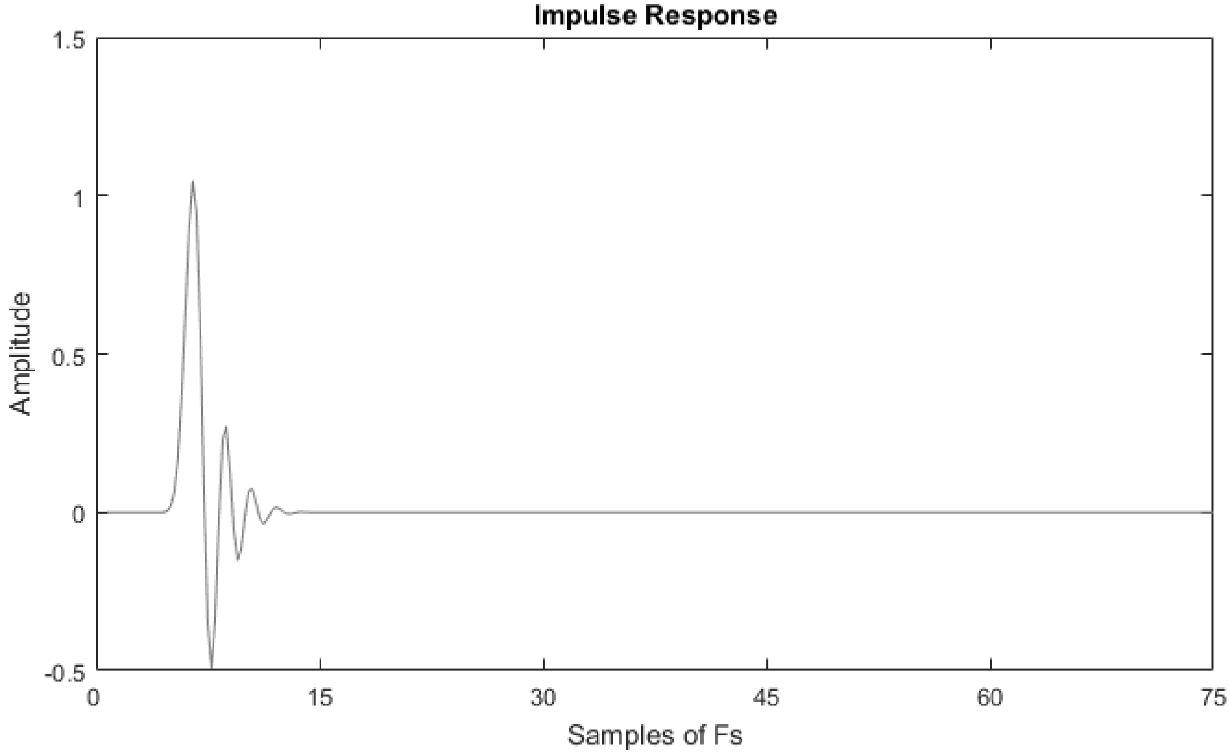


Figure 20 - Minimum Phase 64FS Impulse Response

Clock Distribution

The ES9842 PRO includes features for selecting and manipulating the input clock source.

The minimum MCLK frequency is 22.579MHz.

When using 24.576 MHz or 22.579 MHz, it is preferable to use GPIO4-6 as the data output.

- Register 74-91 (GPIOx/x_CONFIG) - Set desired GPIO as AUX output and enable output mode.
- Register 12-15[6:5] (TDM_LINE_SEL_CHx) - Change TDM Line Select to desired GPIO.
- Register 11[7] (TDM_GPIO456) - Enable TDM on GPIO456.

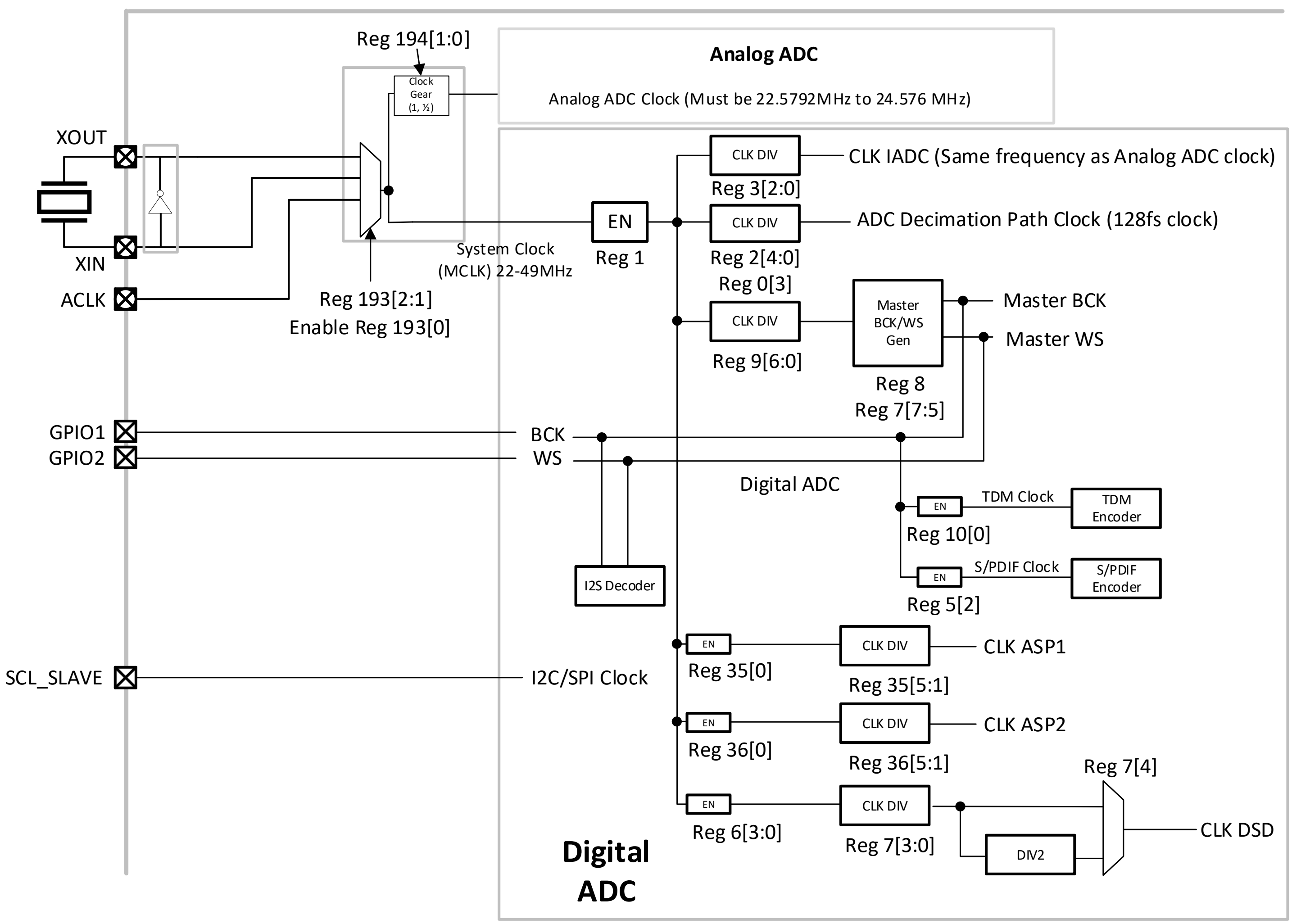


Figure 21 - ES9842 PRO Clock Distribution

The following list shows the various clocks of the ES9842 PRO and the associated registers for configuration.

Analog ADC Clock

ADC clock must be maintained to be between 22.5792MHz & 24.576MHz

- Register 194[1:0] (SEL_CLK_DIV)
- Register 193[2:1] (SEL_SYSCLK_IN)
- Register 193[0] (EN_ANA_CLKIN)

IADC Clock

Should be set to the same clock frequency as the analog ADC clock, sampling Analog ADC.

- Register 3[2:0] (SELECT_IADC_NUM)
    - Set this so it matches Analog ADC clock of 22.5792 or 24.576MHz.
- Register 1 (ADC CLOCK CONFIG1)
    - Dependent on channels required.
- Register 193[2:1] (SEL_SYSCLK_IN)
- Register 193[0] (EN_ANA_CLKIN)

ADC Decimation Path Clock

- Register 2[4:0] (SELECT_ADC_NUM)
- Register 1 (ADC CLOCK CONFIG1)
    - Dependent on channels required.
- Register 9[6:0] (SELECT_I²S_TDM_NUM)
- Register 193[2:1] (SEL_SYSCLK_IN)
- Register 193[0] (EN_ANA_CLKIN)

Master BCK & WS

- Register 8 (I²S/TDM MASTER MODE CONFIG)
- Register 7[7:5] MASTER_WS_SCALE
- Register 9[6:0] SELECT_I²S_TDM_NUM
- Register 193[2:1] (SEL_SYSCLK_IN)
- Register 193[0] (EN_ANA_CLKIN)

TDM Clock

- Register 10[0] (ENABLE_TDM_CLK)

S/PDIF Clock

- Register 5[2] (ENABLE_SPDIF_CLK)

ASP1 Clock

- Register 35[0] (ENABLE_ASP1_CLK)
- Register 35[5:1] (SELECT_ASP1_NUM)
- Register 1 (ADC CLOCK CONFIG1)
  - Dependent on channels required.
- Register 193[2:1] (SEL_SYSCLK_IN)
- Register 193[0] (EN_ANA_CLKIN)

ASP2 Clock

- Register 36[0] (ENABLE_ASP2_CLK)
- Register 36[5:1] (SELECT_ASP2_NUM)
- Register 1 (ADC CLOCK CONFIG1)
  - Dependent on channels required.
- Register 193[2:1] (SEL_SYSCLK_IN)
- Register 193[0] (EN_ANA_CLKIN)

I²S Decoder Clock

- Uses BCK / WS

I²S Master Clock Rate Configurations

WS can be scaled down further than shown via Register 7[7:5] MASTER_WS_SCALE.

MCLK Frequency	WS [kHz]	BCK [MHz]	Bits	Channels	Register 2 [4:0] SELECT_ADC_NUM		Register 9 [6:0] SELECT_I²S_TDM_NUM		Register 11 [5] TDM_LENGTH	
					Value	Divider	Value	Divider	Value	Length
22.579 MHz	44.1	2.822	32	2	5'd3	4	7'd3	4	1'b0	32
	88.2	5.645		2	5'd1	2	7'd1	2	1'b0	32
	176.4	11.290		2	5'd0	1	7'd0	1	1'b0	32
	44.1	1.411	16	2	5'd3	4	7'd3	4	1'b1	16
	88.2	2.822		2	5'd1	2	7'd1	2	1'b1	16
	176.4	5.645		2	5'd0	1	7'd0	1	1'b1	16
24.576 MHz	48	3.072	32	2	5'd3	4	7'd3	4	1'b0	32
	96	6.144		2	5'd1	2	7'd1	2	1'b0	32
	192	12.288		2	5'd0	1	7'd0	1	1'b0	32
	48	1.536	16	2	5'd3	4	7'd3	4	1'b1	16
	96	3.072		2	5'd1	2	7'd1	2	1'b1	16
	192	6.144		2	5'd0	1	7'd0	1	1'b1	16
45.158 MHz	44.1	2.822	32	2	5'd7	8	7'd7	8	1'b0	32
	88.2	5.645		2	5'd3	4	7'd3	4	1'b0	32
	176.4	11.290		2	5'd1	2	7'd1	2	1'b0	32
	352.8	22.579		2	5'd0	1	7'd0	1	1'b0	32
	44.1	1.411	16	2	5'd7	8	7'd7	8	1'b1	16
	88.2	2.822		2	5'd3	4	7'd3	4	1'b1	16
	176.4	5.645		2	5'd1	2	7'd1	2	1'b1	16
	352.8	11.290		2	5'd0	1	7'd0	1	1'b1	16
49.152 MHz	48	3.072	32	2	5'd7	8	7'd7	8	1'b0	32
	96	6.144		2	5'd3	4	7'd3	4	1'b0	32
	192	12.288		2	5'd1	2	7'd1	2	1'b0	32
	384	24.576		2	5'd0	1	7'd0	1	1'b0	32
	48	1.536	16	2	5'd7	8	7'd7	8	1'b1	16
	96	3.072		2	5'd3	4	7'd3	4	1'b1	16
	192	6.144		2	5'd1	2	7'd1	2	1'b1	16
	384	12.288		2	5'd0	1	7'd0	1	1'b1	16

Table 18 - I²S Master Clock Rate Configurations

I²S Slave Clock Rate Configurations

MCLK Frequency	WS [kHz]	BCK	Channels	Register 2 [4:0] SELECT_ADC_NUM		Register 0 [3] ENABLE_64FS_MODE	
				Value	Divider	Value	Multiplier
22.579 MHz	44.1	512FS	2	7’d3	4	1’b0	1x
	88.2	256FS	2	7’d1	2	1’b0	1x
	176.4	128FS	2	7’d0	1	1’b0	1x
	352.8	64FS	2	7’d0	1	1’b1	2x
24.576 MHz	48	512FS	2	7’d3	4	1’b0	1x
	96	256FS	2	7’d1	2	1’b0	1x
	192	128FS	2	7’d0	1	1’b0	1x
	384	64FS	2	7’d0	1	1’b1	2x
45.158 MHz	44.1	1024FS	2	7’d7	8	1’b0	1x
	88.2	512FS	2	7’d3	4	1’b0	1x
	176.4	256FS	2	7’d1	2	1’b0	1x
	352.8	128FS	2	7’d0	1	1’b0	1x
49.152 MHz	48	1024FS	2	7’d7	8	1’b0	1x
	96	512FS	2	7’d3	4	1’b0	1x
	192	256FS	2	7’d1	2	1’b0	1x
	384	128FS	2	7’d0	1	1’b0	1x

Table 19 - I²S Slave Clock Rate Configurations

TDM Master Clock Rate Configurations

All configurations are 32-bit.

When using left justified mode (Register 10[1] TDM_LJ = 1'b1) remember to enable Register 33[7] SYNC_POSEDGE_FRAME to correct for phase differences.

MCLK Frequency	WS [kHz]	BCK [MHz]	TDM Mode	Chan-nels	Register 2 [4:0] SELECT_ADC_NUM		Register 9 [6:0] SELECT_I²S_TDM_NUM		Register 7 [7:5] MASTER_WS_SCALE		Register 8 [7] MASTER_BCK_DIV1	
					Value	Divider	Value	Divider	Value	Divider	Value	Divider
22.579 MHz	44.1	5.645	TDM 128	4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	88.2	11.290		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	176.4	22.579		4	5'd0	1	7'd0	1	3'd0	1	1'b1	1
	44.1	11.290	TDM 256	8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	88.2	22.579		8	5'd1	2	7'd0	1	3'd1	2	1'b1	1
	44.1	22.579	TDM 512	16	5'd3	4	7'd0	1	3'd2	4	1'b1	1
24.576 MHz	48	6.144	TDM 128	4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	96	12.288		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	192	24.576		4	5'd0	1	7'd0	1	3'd0	1	1'b1	1
	48	12.288	TDM 256	8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	96	24.576		8	5'd1	2	7'd0	1	3'd1	2	1'b1	1
	48	24.576	TDM 512	16	5'd3	4	7'd0	1	3'd2	4	1'b1	1
45.158 MHz	44.1	5.645	TDM 128	4	5'd7	8	7'd3	4	3'd1	2	1'b0	2
	88.2	11.290		4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	176.4	22.579		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	44.1	11.290	TDM 256	8	5'd7	8	7'd1	2	3'd2	4	1'b0	2
	88.2	22.579		8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	44.1	22.579	TDM 512	16	5'd7	8	7'd0	1	3'd3	8	1'b0	2
49.152 MHz	48	6.144	TDM 128	4	5'd7	8	7'd3	4	3'd1	2	1'b0	2
	96	12.288		4	5'd3	4	7'd1	2	3'd1	2	1'b0	2
	192	24.576		4	5'd1	2	7'd0	1	3'd1	2	1'b0	2
	48	12.288	TDM 256	8	5'd7	8	7'd1	2	3'd2	4	1'b0	2
	96	24.576		8	5'd3	4	7'd0	1	3'd2	4	1'b0	2
	48	24.576	TDM 512	16	5'd7	8	7'd0	1	3'd3	8	1'b0	2

Table 20 - TDM Master Clock Rate Configurations

TDM Slave Clock Rate Configurations

All configurations are 32-bit.

When using left justified mode (Register 10[1] TDM_LJ = 1'b1) remember to enable Register 33[7] SYNC_POSEDGE_FRAME to correct for phase differences.

MCLK Frequency	WS [kHz]	BCK [MHz]	TDM Mode	Channels	Register 2 [4:0] SELECT_ADC_NUM	
					Value	Divider
22.579 MHz	44.1	5.645	TDM 128	4	5'd3	4
	88.2	11.290		4	5'd1	2
	176.4	22.579		4	5'd0	1
	44.1	11.290	TDM 256	8	5'd3	4
	88.2	22.579		8	5'd1	2
	44.1	22.579	TDM 512	16	5'd3	4
24.576 MHz	48	6.144	TDM 128	4	5'd3	4
	96	12.288		4	5'd1	2
	192	24.576		4	5'd0	1
	48	12.288	TDM 256	8	5'd3	4
	96	24.576		8	5'd1	2
	48	24.576	TDM 512	16	5'd3	4
45.158 MHz	44.1	5.645	TDM 128	4	5'd7	8
	88.2	11.290		4	5'd3	4
	176.4	22.579		4	5'd1	2
	44.1	11.290	TDM 256	8	5'd7	8
	88.2	22.579		8	5'd3	4
	44.1	22.579	TDM 512	16	5'd7	8
49.152 MHz	48	6.144	TDM 128	4	5'd7	8
	96	12.288		4	5'd3	4
	192	24.576		4	5'd1	2
	48	12.288	TDM 256	8	5'd7	8
	96	24.576		8	5'd3	4
	48	24.576	TDM 512	16	5'd7	8

Table 21 - TDM Slave Clock Rate Configurations

DSD Master Clock Rate Configurations

MCLK Frequency	BCK [MHz]	FS [kHz]	DSD Mode	Register 7 [3:0] SELECT_DSD_NUM		Register 7 [4] DSD_CLK_DIV2		Reg 2 [4:0] SELECT_ADC_NUM	
				Value	Divider	Value	Divider	Value	Divider
22.579 MHz	2.822	44.1	DSD 64	5’d3	4	1’b1	2	5’d7	8
	5.645	44.1	DSD 128	5’d1	2	1’b1	2	5’d7	8
	11.290	44.1	DSD 256	5’d0	1	1’b1	2	5’d7	8
45.158 MHz	2.822	44.1	DSD 64	5’d7	8	1’b1	2	5’d7	8
	5.645	44.1	DSD 128	5’d3	4	1’b1	2	5’d7	8
	11.290	44.1	DSD 256	5’d1	2	1’b1	2	5’d7	8
	22.579	44.1	DSD 512	5’d0	1	1’b1	2	5’d7	8

Table 22 - DSD Master Clock Rate Configurations

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_R/AVCC_L • AVCC • AVDD • DVDD Note: AVCC, AVCC_L/R and AVDD absolute negative max voltage is -0.3V	• +4.75V with respect to Ground • +4.75V with respect to Ground • +3.7V with respect to Ground • +1.4V with respect to Ground
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+125°C
Voltage Range for Digital Input Pins	-0.3V to AVDD (nom) + 0.3V
Maximum/Minimum Input Voltage on IN_P IN_M pins	-0.4V to AVCC (nom) + 0.7V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 23 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-Level Input Voltage	VIH	(AVDD / 2) + 0.4		V	
Low-Level Input Voltage	VIL		0.4	V	
High-Level Output Voltage	VOH	AVDD - 0.2		V	IOH = (AVDD / 2) + 1.4 [mA]
Low-Level Output Voltage	VOL		0.2	V	IOL = (AVDD / 2) + 1.7 [mA]

Table 24 - IO Electrical Characteristics

Switching Characteristics

Test Conditions (unless otherwise noted)

T_A = 25°C, AVCC = AVCCL = AVCCR = +4.5V, AVDD = +3.3V, fs = 48kHz, MCLK = 49.152MHz, I²S output

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
MCLK timing					
Frequency	f_{MCLK}	20	-	50	MHz
Analog ADC[1]	f_{ADC}	20	-	25	MHz
Duty Cycle	-	45	50	55	%
Bit Clock Frequency					
PCM (LJ/ I²S) Mode	f_{bCLK}	-	2 x fs x TDM_LENGTH	MCLK/2	MHz
PCM (LJ/ I²S) + Enable_64FS Mode	f_{bCLK}	-	-	MCLK	MHz
TDM4 (4ch data line)	f_{bCLK}	-	4 x fs x TDM_LENGTH	MCLK	MHz
TDM8 (8ch data line)	f_{bCLK}	-	8 x fs x TDM_LENGTH	MCLK	MHz
TDM16 (16ch data line)	f_{bCLK}	-	16 x fs x TDM_LENGTH	MCLK	MHz
Frame Clock Normal Frequency					
PCM (LJ/ I²S) Mode	WS	MCLK/4096	-	MCLK/128	kHz
PCM (LJ/ I²S) + Enable_64FS Mode	WS	-	-	MCLK/64	kHz
TDM4 (4ch data line)	WS	MCLK/4096	-	MCLK/128	kHz
TDM8 (8ch data line)	WS	MCLK/4096	-	MCLK/256	kHz
TDM16 (16ch data line)	WS	MCLK/4096	-	MCLK/512	kHz

Table 25 - Switching Characteristics

Note: The DFIR Filters need to be resynced after sample rate changes. See Addendum for respective resync program.

[1] Analog ADC (fADC) on the clock distribution diagram must be between 20-25MHz. MCLK used must be divided by 1 or 2 to create fADC.

Timing Characteristics

Bit-Clock (BCK) and Word-Select (WS) Timing

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
LJ/I²S Mode or TDM modes					
Slave Mode					
BCLK Period	tb	20	-	-	ns
BCLK High Duration	tbH	9	-	-	ns
BCLK Low Duration	tbL	9	-	-	ns
BCLK Fall to Frame Transition	tbsr	-6	0	6	ns
BCLK Fall to Serial Data Out	tbsdo	-	13.8	-	ns
Data in Setup Time	tsdisu	-	-	-	ns
Data in Hold Time	tsdihold	-	-	-	ns
Master Mode					
BCLK Period	tb	20	-	-	ns
BCLK High Duration	tbH	9	-	-	ns
BCLK Low Duration	tbL	9	-	-	ns
BCLK Fall to Frame Transition	tbsr	-	0	-	ns
BCLK Fall to Serial Data Out	tbsdo	-	13.2	-	ns
Data in Setup Time	tsdisu	-	-	-	-
Data in Hold Time	tsdihold	-	-	-	-

Table 26 - Audio Interface Timing Requirements

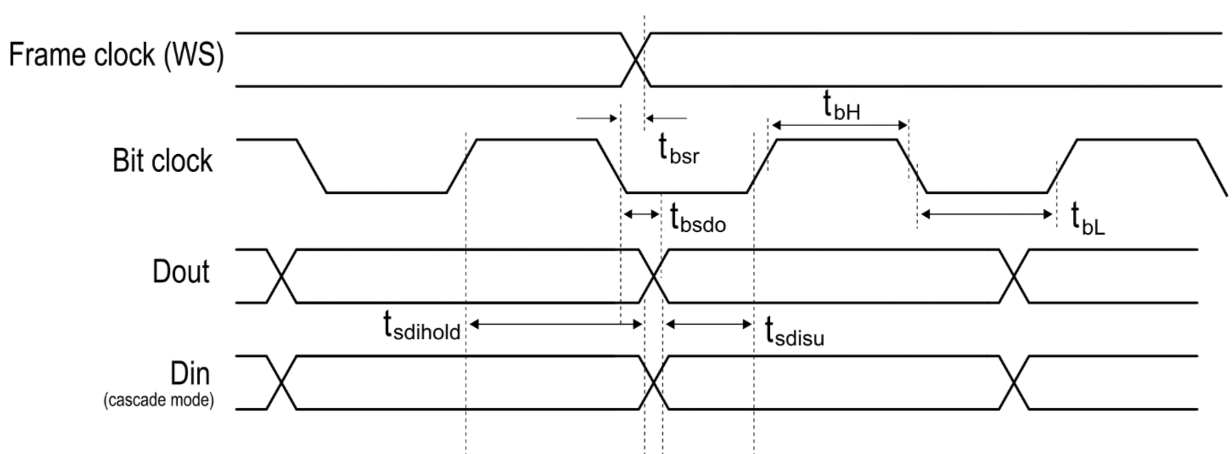


Figure 22 - Audio Interface Timing Requirements

Master Clock (MCLK) and Bit-Clock (BCK) Timing

The ES9842 PRO has a phase relationship requirement between MCLK (System Clock) and BCK (Bit Clock). The internal ADC_CLK (which must be 24.576/22.5792MHz) is derived from the provided MCLK. In slave mode, the ES9842PRO requires the BCK transition to be within a specific range of the MCLK period. This is due to the synchronization circuitry that aligns the output samples with the input clocks. The table below specifies the amount of time required between the bit clock transition and the MCLK falling edge. To achieve this, follow the MCLK to BCK timing outlined below.

45/49MHz MCLK

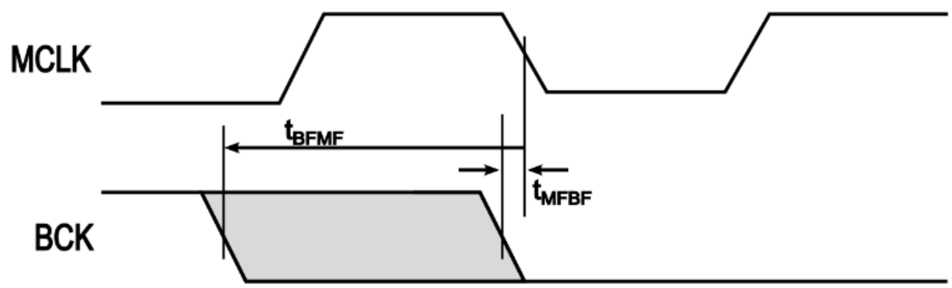


Figure 23 - 45/49MHz MCLK with BCK Phase Relationship

	Symbol	MCLK [MHz]	Minimum	Maximum	Unit
BCK "↓" to MCLK "↓"	t_{bfmf}	49.152 / 45.1584	-	10	ns
MCLK "↓" to BCK "↓"	t_{mfbf}		4	-	ns

Table 27 - Timing relationship for 45/49MHz MCLK & BCK

22/24MHz MCLK

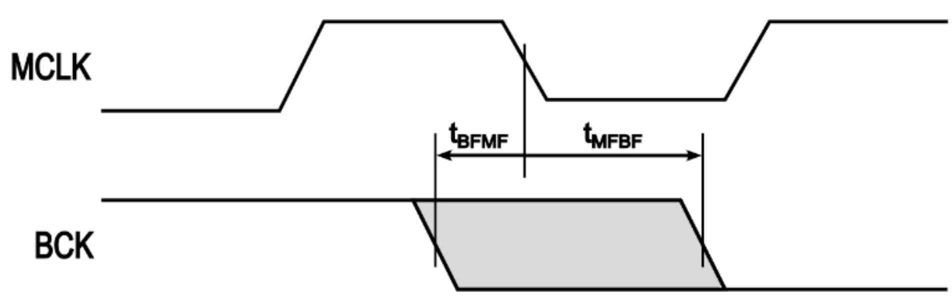


Figure 24 - 22/25MHz MCLK with BCK Phase Relationship

	Symbol	MCLK [MHz]	Minimum	Maximum	Unit
BCK "↓" to MCLK "↓"	t_{bfmf}	24.576 / 22.5792	-	5	ns
MCLK "↓" to BCK "↓"	t_{mfbf}		-	7	ns

Table 28 - Timing relationship for 22/24MHz MCLK & BCK

I²C Slave/Synchronous Slave Interface Timing

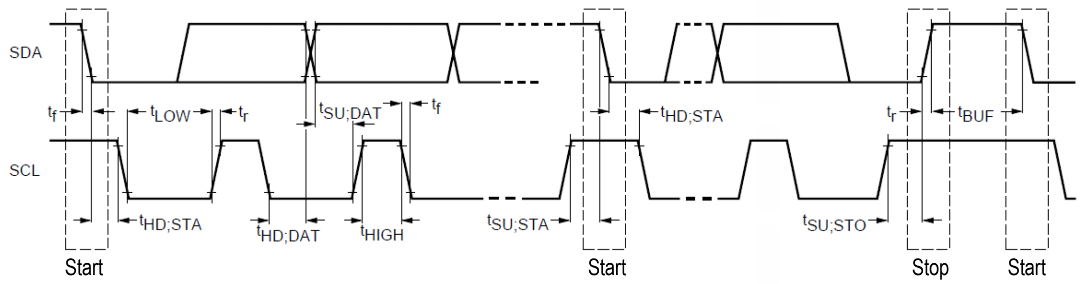


Figure 25 - I²C Slave Control Interface Timing Diagram

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000	-	300	ns
Fall time of SDA and SCL	t_f		-	300	-	300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 29 - I²C Slave Control Interface Timing Definitions

SPI Slave Interface Timing

The SPI slave interface is used when the MODE pin (Pin 3) is pulled high.

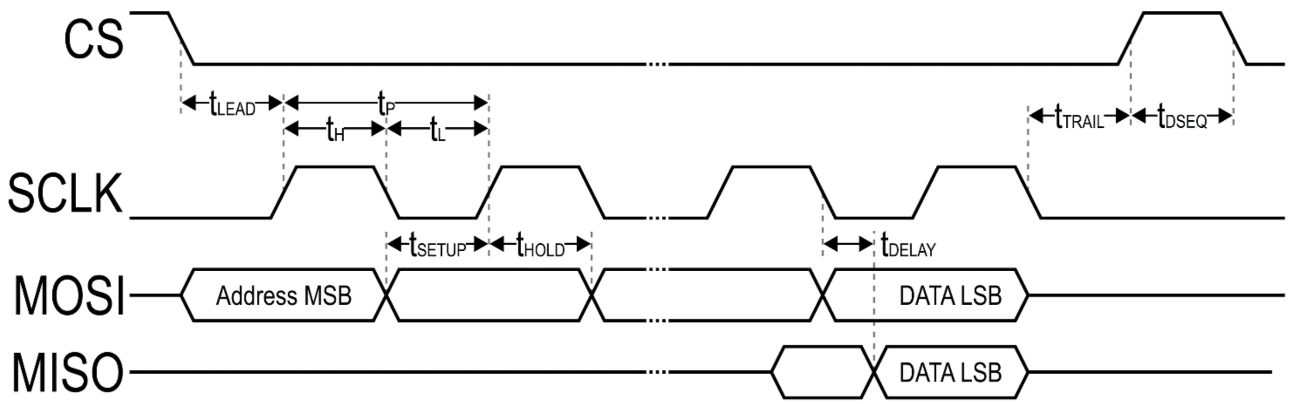


Figure 26 - SPI Slave Interface Timing

Parameter	Symbol	Min [ns]	Max [ns]
CS Lead Time (SCLK rising edge)	t_{LEAD}	10	-
CS Trail Time (SCLK falling edge)	t_{TRAIL}	10	-
MOSI Data Setup Time	t_{SETUP_MOSI}	-30	-
MOSI Data Hold Time	t_{HOLD_MOSI}	65	-
SCLK-MISO Delay Time	t_{DELAY_MISO}	-	65
SCLK Period	t_{P_SCLK}	170	-
SCLK High Pulse Duration	t_{H_SCLK}	60	-
SCLK Low Pulse Duration	t_{L_SCLK}	90	-
Sequential Transfer Delay	t_{DSEQ}	45	-

Table 30 - SPI Slave Interface Timing

Recommended Operating Conditions

These are the recommended operating conditions for the ES9842 PRO.

The minimum MCLK is 22MHz. Below this frequency, the device will not function.

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	-20°C to +85°C
AVCC		4.5V
AVDD		3.3V
AVCC_L		4.5V
AVCC_R		4.5V
VREF_L		Internal
VREF_R		Internal
DVDD		Internal 1.2V

Table 31 - Recommended Operating Conditions

Recommended Power Up/Down Sequences

The recommended power up/down sequences are shown in the following diagram. All supplies and MCLK should be stable before CHIP_EN is asserted.

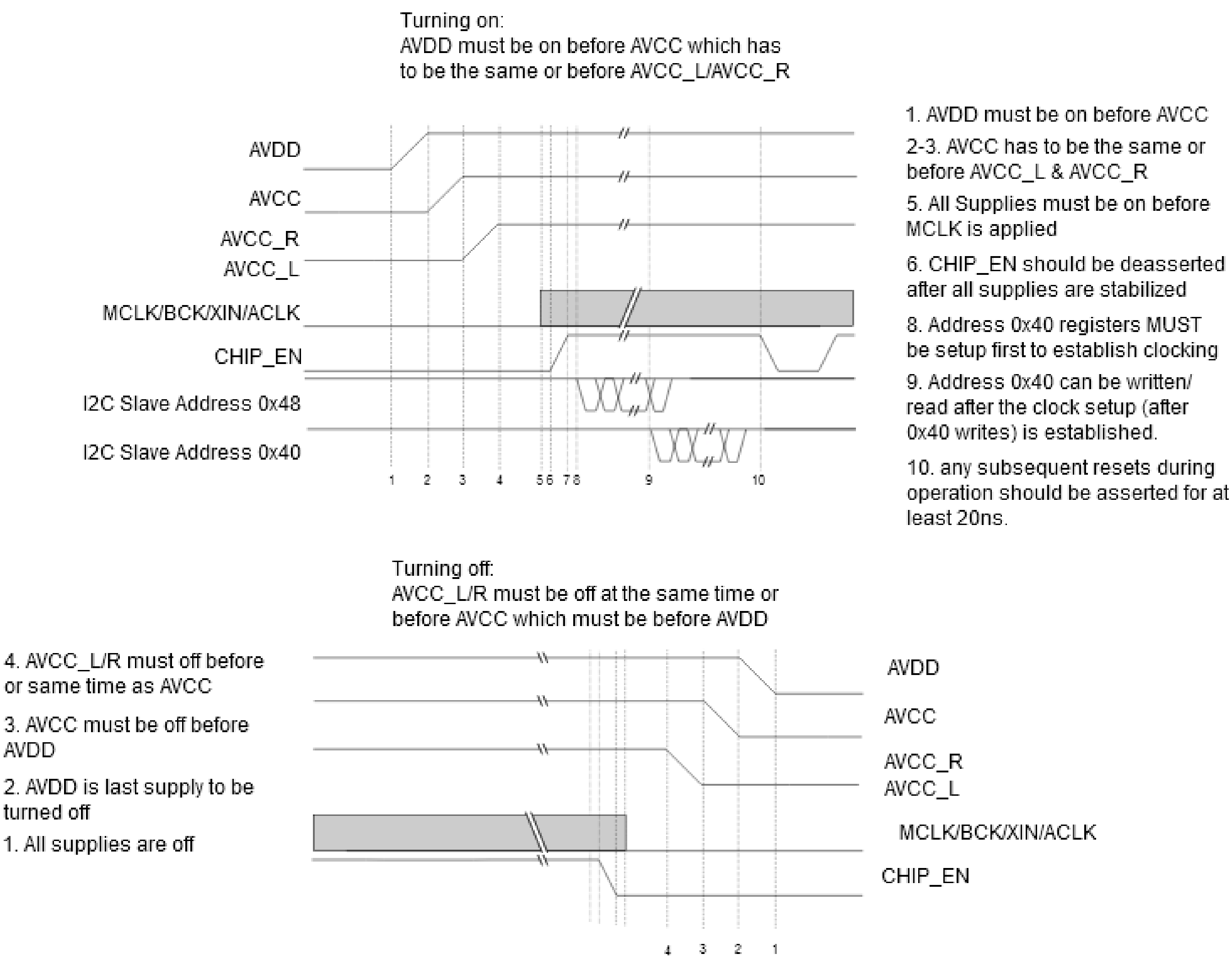


Figure 27 - Recommended Power Up/Down Sequences

Power Consumption

Test Conditions (unless otherwise noted)

T_A = 25°C, AVCC = AVCCL = AVCCR = +4.5V, AVDD = +3.3V, fs = 48kHz, I²S output, -1dBrG signal. AVDD supply includes DVDD current.

Parameter	**Min**	**Typ.**	**Max**	**Unit**
Standby				
AVCC, AVCC_L, AVCC_R		3		µA
AVDD		0.02		µA
MCLK = 49.152MHz				
Supply Current during 48kHz 4ch mode				
AVCC		10.2		mA
AVCC_L, AVCC_R		16.2		mA
AVDD		18.2		mA
Supply Current during 192kHz 4ch mode				
AVCC		10.2		mA
AVCC_L, AVCC_R		16.2		mA
AVDD		30.6		mA
MCLK = 24.576MHz				
Supply Current during 48kHz 4ch mode				
AVCC		10.1		mA
AVCC_L, AVCC_R		16.2		mA
AVDD		16.1		mA
Supply current during 192kHz 4ch mode				
AVCC		10.1		mA
AVCC_L, AVCC_R		16.2		mA
AVDD		28.7		mA

Table 32 - Power Consumption

Performance

Test Conditions (unless otherwise noted)

T_A = 25°C, AVCC = AVCCL = AVCCR = +4.5V, AVDD = +3.3V, fs = 48kHz, MCLK = 49.152MHz, I²S output

Parameter			Min	Typ	Max	Unit
Resolution				32		Bit
0dBFS Input Voltage				3.2		Vrms
THD+N Ratio @ fs=48kHz, BW=20Hz-20kHz	4 ch mode	-1dBFS		-116	-114	dB
	2 ch mode			-117		dB
	1 ch mode			-118		dB
THD+N Ratio @ fs=96kHz, BW=20Hz-40kHz	4 ch mode	-1dBFS		-113		dB
	2 ch mode			-115		dB
	1 ch mode			-118		dB
THD+N Ratio @ fs=192kHz, BW=20Hz-80kHz	4 ch mode	-1dBFS		-111		dB
	2 ch mode			-113		dB
	1 ch mode			-116		dB
DNR A-weighted	4ch mode	-60dBFS	119	122		dB
	2ch mode		122	125		dB
	1ch mode		125	128		dB
Inter-channel Gain Mismatch				±0.05	±0.4	dB
Input DC Common Mode				AVCC_L/2 AVCC_R/2		V
Input Impedance				860±14%		Ω
C_{in} (Input Capacitance)				~10		pF

Table 33 - Performance

Register Overview

I²C Slave Interface (Device Address 0x40, 0x42, 0x44, 0x46)

This interface contains Read/Write and Read-only registers. A system clock must be enabled through the write-only registers to read/write these registers.

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

.

Read/Write Register Addresses

Registers 0-179 (0x00 - 0xB3) are read/write registers.

Read-only Register Addresses

Registers 224 - 253 (0xE0 - 0xFD) are read only registers.

I²C Synchronous Slave Interface (Device Address 0x48, 0x4A, 0x4C, 0x4E)

This interface contains Write-only registers. These registers can be written even when there is no system clock present. These registers must be written to enable read and write access to the rest of the registers.

When the device is inactive, all peripherals are automatically disabled, and all clocks are stopped. An interrupt or a reset can wake the ES9842 PRO.

Write-only Register Addresses

Registers 192 - 194 (0xC0 - 0xC2) are write only registers.

Multi-Byte Registers

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written.

MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	OUTPUT_SEL		RESERVED	ENABLE_64FS_MODE	TWO_CH_MODE	MONO_MODE	RESERVED
0x01	1	ADC CLOCK CONFIG1	ENABLE_DATA_IN_CH4	ENABLE_DATA_IN_CH3	ENABLE_DATA_IN_CH2	ENABLE_DATA_IN_CH1	ENABLE_ADC_CH4	ENABLE_ADC_CH3	ENABLE_ADC_CH2	ENABLE_ADC_CH1
0x02	2	ADC CLOCK CONFIG2	RESERVED		SELECT_ADC_HALF	SELECT_ADC_NUM				
0x03	3	ADC CLOCK CONFIG3	OUTPUT2_SEL		FORCE_OUTPUT2	INVERT_FIRST_CLK_SAMPLE2	SELECT_IADC_HALF	SELECT_IADC_NUM		
0x04	4	ADC CLOCK CONFIG4	FORCE_PHASE_CLK_IADC	PHASE_CLK_IADC			INVERT_SAMPLE_CLOCK_CH4	INVERT_SAMPLE_CLOCK_CH3	INVERT_SAMPLE_CLOCK_CH2	INVERT_SAMPLE_CLOCK_CH1
0x05	5	RAW DATA AND SPDIF CONFIG	SELECT_RAW_DATA_NUM		RAW_DATA_CLK_DIV2	RAW_DATA_DDR	ENABLE_RAW_DATA_CLK	ENABLE_SPDIF_CLK	RESERVED	
0x06	6	DSD CONFIG	RESERVED		DSD_DDR	DSD_MASTER_MODE	ENABLE_DSD_CLK_CH4	ENABLE_DSD_CLK_CH3	ENABLE_DSD_CLK_CH2	ENABLE_DSD_CLK_CH1
0x07	7	DSD AND I²S/TDM MASTER CLK CONFIG	MASTER_WS_SCALE			DSD_CLK_DIV2	SELECT_DSD_NUM			
0x08	8	I²S/TDM MASTER MODE CONFIG	MASTER_BCK_DIV1	MASTER_WS_IDLE	MASTER_FRAME_LENGTH		MASTER_WS_PULSE_MODE	MASTER_BCK_INVERT	MASTER_WS_INVERT	MASTER_MODE_ENABLE
0x09	9	I²S/TDM MASTER CLK CONFIG	SELECT_I²S_TDM_HALF	SELECT_I²S_TDM_NUM						
0x0A	10	TDM CONFIG1	TDM_BIT_DELAY					TDM_VALID_EDGE	TDM_LJ	ENABLE_TDM_CLK
0x0B	11	TDM CONFIG2	TDM_GPIO456	TDM_CASCADE	TDM_LENGTH	TDM_CH_NUM				
0x0C	12	TDM SLOT CONFIG CH1	RESERVED	TDM_LINE_SEL_CH1		TDM_SLOT_SEL_CH1				
0x0D	13	TDM SLOT CONFIG CH2	RESERVED	TDM_LINE_SEL_CH2		TDM_SLOT_SEL_CH2				
0x0E	14	TDM SLOT CONFIG CH3	RESERVED	TDM_LINE_SEL_CH3		TDM_SLOT_SEL_CH3				
0x0F	15	TDM SLOT CONFIG CH4	RESERVED	TDM_LINE_SEL_CH4		TDM_SLOT_SEL_CH4				
0x10	16	RAW DATA OUTPUT CONFIG	RESERVED		RAW_DATA_MIX_DIV2_CH2_4	RAW_DATA_MIX_DIV2_CH1_3	ENABLE_RAW_DATA_MIX_CH2_4	ENABLE_RAW_DATA_MIX_CH1_3	NEG_RAW_DATA_SUB_CH2	NEG_RAW_DATA_SUB_CH1
0x11	17	INPUT DATA MAPPING	INPUT_DATA_MAPPING_CH4		INPUT_DATA_MAPPING_CH3		INPUT_DATA_MAPPING_CH2		INPUT_DATA_MAPPING_CH1	
0x12	18	PCM DATA OUTPUT MAPPING	OUTPUT_MAPPING_CH4		OUTPUT_MAPPING_CH3		OUTPUT_MAPPING_CH2		OUTPUT_MAPPING_CH1	
0x13	19	DSD DATA OUTPUT MAPPING	DSD_MAPPING_CH4		DSD_MAPPING_CH3		DSD_MAPPING_CH2		DSD_MAPPING_CH1	
0x14	20	TPDF DITHER LEVEL	RESERVED				DITHER_SCALE			
0x15	21	DITHER MASK	DITHER_MASK							
0x16	22		DITHER_MASK							
0x17	23	FS GEN PHASE CONTROL	DSD_SYNC_TO_1FS	FS_PHASE						
0x18-0x1A	24-26	RESERVED	RESERVED							
0x1B	27	INTERRUPT	INTERRUPT_CLEAR_CH4_PEAK_DETECT	INTERRUPT_CLEAR_CH3_PEAK_DETECT	INTERRUPT_CLEAR_CH2_PEAK_DETECT	INTERRUPT_CLEAR_CH1_PEAK_DETECT	INTERRUPT_MASK_CH4_PEAK_DETECT	INTERRUPT_MASK_CH3_PEAK_DETECT	INTERRUPT_MASK_CH2_PEAK_DETECT	INTERRUPT_MASK_CH1_PEAK_DETECT
0x1C	28	SPDIF SUBCODE CONFIG	SPDIF_CS							
0x1D	29		SPDIF_CS							
0x1E	30		SPDIF_CS							
0x1F	31		SPDIF_CS							
0x20	32		SPDIF_CS							
0x21	33	DSD DITHER SCALE & SYNC CONTROL	SYNC_POSEDGE_FRAME	DISABLE_SYNC_REF	FORCE_FIR_SYNC	DSD_DITHER_SCALE				
0x22	34	SYNC CONTROL	AUTO_ADC_CLKDIV_SYNC	AUTO_CLK_IADC_PHASE_SYNC	AUTO_DSD_PHASE_SYNC	AUTO_WS_PHASE_SYNC	AUTO_ICG_EN_SYNC	AUTO_ICG_SYNC	AUTO_FIR_SYNC	AUTO_FS_SYNC
0x23	35	ASP1 CONFIG	RESERVED		SELECT_ASP1_NUM					ENABLE_ASP1_CLK
0x24	36	ASP2 CONFIG	RESERVED		SELECT_ASP2_NUM					ENABLE_ASP2_CLK
0x25	37	ASP ENABLE & PROGRAM CONTROL	ASP2_COEFF_WE	ASP1_COEFF_WE	ASP2_PROGRAM_WE	ASP1_PROGRAM_WE	ASP2_PROGRAM_EN	ASP1_PROGRAM_EN	ENABLE_ASP2	ENABLE_ASP1
0x26	38	ASP PROGRAM ADDR	ASP_PROGRAM_ADDR							
0x27	39		RESERVED							ASP_PROGRAM_ADDR
0x28	40	ASP PROGRAM	ASP_PROGRAM_IN							
0x29	41		RESERVED		ASP_PROGRAM_IN					
0x2A	42	ASP COEFF ADDR	RESERVED		ASP_COEFF_ADDR					
0x2B	43	ASP COEFF	ASP_COEFF_LSB							
0x2C	44		ASP_COEFF_LSB							
0x2D	45		ASP_COEFF_LSB							
0x2E	46		ASP_COEFF_LSB							
0x2F	47		ASP_COEFF_MSB							
0x30	48		ASP_COEFF_MSB							
0x31	49		ASP_COEFF_MSB							
0x32	50		ASP_COEFF_MSB							
0x33	51	ASP1 CH1 STEP SIZE	ASP1_CH1_STEP_SIZE							
0x34	52	ASP1 CH2 STEP SIZE	ASP1_CH2_STEP_SIZE							
0x35	53	ASP2 CH1 STEP SIZE	ASP2_CH1_STEP_SIZE							
0x36	54	ASP2 CH2 STEP SIZE	ASP2_CH2_STEP_SIZE							
0x37	55	ASP1 CUSTOM ADDR	RESERVED		ASP1_CUSTOM_ADDR					

0x38	56	ASP1 CUSTOM ADDR2	RESERVED		ASP1_CUSTOM_ADDR2					
0x39	57	ASP2 CUSTOM ADDR	RESERVED		ASP2_CUSTOM_ADDR					
0x3A	58	ASP2 CUSTOM ADDR2	RESERVED		ASP2_CUSTOM_ADDR2					
0x3B	59	I²S DECODER CONFIG	I²S_DECODER_BIT_START							
0x3C	60	I²S DECODER CONFIG	I²S_DECODER_WORD_WIDTH		I²S_DECODER_BIT_DEPTH		I²S_DECODER_POSEDGE_FRAME	ENABLE_I²S_DECODER	I²S_DECODER_BIT_START	
0x3D	61	DELAY LINE CONFIG	PROG_DELAY_LINE							
0x3E	62		RESERVED						ENABLE_CLK_DL	PROG_DELAY_LINE
0x3F	63	ADC CH1 CONFIG 1	ADC_INT2_SEL_CH1		ADC_INT1_SEL_CH1		ADC_EN_FB_CH1	RESERVED	ADC_EN_INT_CH1	ADC_EN_CH1
0x40	64	ADC CH1 CONFIG 2	ADC_COMP_SEL_CH1			ADC_SUM_SEL_CH1		ADC_USE_DITHER_EXT_CH1	ADC_USE_DITHER_CH1	ADC_USE_STATE_CH1
0x41	65	ADC CH2 CONFIG 1	ADC_INT2_SEL_CH2		ADC_INT1_SEL_CH2		ADC_EN_FB_CH2	RESERVED	ADC_EN_INT_CH2	ADC_EN_CH2
0x42	66	ADC CH2 CONFIG 2	ADC_COMP_SEL_CH2			ADC_SUM_SEL_CH2		ADC_USE_DITHER_EXT_CH2	ADC_USE_DITHER_CH2	ADC_USE_STATE_CH2
0x43	67	ADC CH3 CONFIG 1	ADC_INT2_SEL_CH3		ADC_INT1_SEL_CH3		ADC_EN_FB_CH3	RESERVED	ADC_EN_INT_CH3	ADC_EN_CH3
0x44	68	ADC CH3 CONFIG 2	ADC_COMP_SEL_CH3			ADC_SUM_SEL_CH3		ADC_USE_DITHER_EXT_CH3	ADC_USE_DITHER_CH3	ADC_USE_STATE_CH3
0x45	69	ADC CH4 CONFIG 1	ADC_INT2_SEL_CH4		ADC_INT1_SEL_CH4		ADC_EN_FB_CH4	RESERVED	ADC_EN_INT_CH4	ADC_EN_CH4
0x46	70	ADC CH4 CONFIG 2	ADC_COMP_SEL_CH4			ADC_SUM_SEL_CH4		ADC_USE_DITHER_EXT_CH4	ADC_USE_DITHER_CH4	ADC_USE_STATE_CH4
0x47	71	ADC COMMON MODE CONFIG	ADC_CM_AMP_SEL_CH4	ADC_CM_INT_SEL_CH4	ADC_CM_AMP_SEL_CH3	ADC_CM_INT_SEL_CH3	ADC_CM_AMP_SEL_CH2	ADC_CM_INT_SEL_CH2	ADC_CM_AMP_SEL_CH1	ADC_CM_INT_SEL_CH1
0x48-0x49	72-73	RESERVED	RESERVED							
0x4A	74	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x4B	75	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x4C	76	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x4D	77	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG			
0x4E	78	GPIO9/10 CONFIG	GPIO10_CFG				GPIO9_CFG			
0x4F	79	GPIO11 CONFIG	RESERVED				GPIO11_CFG			
0x50-0x51	80-81	RESERVED	RESERVED							
0x52	82	INVERT GPIO	INVERT_GPIO8	INVERT_GPIO7	INVERT_GPIO6	INVERT_GPIO5	INVERT_GPIO4	INVERT_GPIO3	INVERT_GPIO2	INVERT_GPIO1
0x53	83		RESERVED					INVERT_GPIO11	INVERT_GPIO10	INVERT_GPIO9
0x54	84	GPIO WEAK ENABLE	GPIO8_WK_EN	GPIO7_WK_EN	GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x55	85		RESERVED					GPIO11_WK_EN	GPIO10_WK_EN	GPIO9_WK_EN
0x56	86	GPIO IE	GPIO8_IE	GPIO7_IE	GPIO6_IE	GPIO5_IE	GPIO4_IE	GPIO3_IE	GPIO2_IE	GPIO1_IE
0x57	87		RESERVED					GPIO11_IE	GPIO10_IE	GPIO9_IE
0x58	88	GPIO OE	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x59	89		RESERVED					GPIO11_OE	GPIO10_OE	GPIO9_OE
0x5A	90	GPIO READ	GPIO8_READ	GPIO7_READ	GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x5B	91		RESERVED					GPIO11_READ	GPIO10_READ	GPIO9_READ
0x5C	92	PWM1 COUNT	PWM1_COUNT							
0x5D	93	PWM1 FREQUENCY	PWM1_FREQ							
0x5E	94		PWM1_FREQ							
0x5F	95	PWM2 COUNT	PWM2_COUNT							
0x60	96	PWM2 FREQUENCY	PWM2_FREQ							
0x61	97		PWM2_FREQ							
0x62	98	PWM3 COUNT	PWM3_COUNT							
0x63	99	PWM3 FREQUENCY	PWM3_FREQ							
0x64	100		PWM3_FREQ							
0x65	101	ADC CH1 DATAPATH CONTROL	ADC1_BYPASS_FIR2X	ADC1_BYPASS_FIR4X	RESERVED			ADC1_ENABLE_DC_BLOCKING	RESERVED	ADC1_NEG_SEL
0x66	102	ADC CH1 THD COMP CONFIG	ADC1_CORRECTION_ADDR						ADC1_CORRECTION_WE	ADC1_ENABLE_THD_COMP
0x67	103	ADC CH1 THD COMP DATA	ADC1_CORRECTION_DATA							
0x68	104		ADC1_CORRECTION_DATA							
0x69	105	ADC CH1 PEAK DETECTOR CONFIG	ADC1_LOCK_PEAK	ADC1_PEAK_DECAY_RATE					RESERVED	ADC1_ENABLE_PEAK_DETECT
0x6A	106	ADC CH1 PEAK DETECTOR LEVEL	ADC1_PEAK_THRESH							
0x6B	107	ADC CH1 DC OFFSET	ADC1_DC_OFFSET							
0x6C	108		ADC1_DC_OFFSET							
0x6D	109	ADC CH1 VOLUME	ADC1_VOLUME							
0x6E	110		ADC1_VOLUME							
0x6F	111	ADC CH1 VOLUME RATE	ADC1_VOLUME_RATE							
0x70	112	ADC CH1 GAIN	RESERVED						ADC1_DATA_GAIN	
0x71	113	ADC CH1 PROG FILTER	RESERVED			ADC1_FILTER_SHAPE			ADC1_PROG_COEFF_WRITE_EN	ADC1_PROG_COEFF_EN
0x72	114	ADC CH1 PROG FILTER COEFF ADDR	ADC1_PROG_COEFF_STAGE	ADC1_PROG_COEFF_ADDR						
0x73	115	ADC CH1 PROG FILTER COEFF	ADC1_PROG_COEFF_IN							
0x74	116		ADC1_PROG_COEFF_IN							
0x75	117		ADC1_PROG_COEFF_IN							
0x76	118	ADC CH2 DATAPATH CONTROL	ADC2_BYPASS_FIR2X	ADC2_BYPASS_FIR4X	RESERVED			ADC2_ENABLE_DC_BLOCKING	RESERVED	ADC2_NEG_SEL

0x77	119	ADC CH2 THD COMP CONFIG	ADC2_CORRECTION_ADDR						ADC2_CORRECTION_WE	ADC2_ENABLE_THD_COMP
0x78	120	ADC CH2 THD COMP DATA	ADC2_CORRECTION_DATA							
0x79	121		ADC2_CORRECTION_DATA							
0x7A	122	ADC CH2 PEAK DETECTOR CONFIG	ADC2_LOCK_PEAK	ADC2_PEAK_DECAY_RATE					RESERVED	ADC2_ENABLE_PEAK_DETECT
0x7B	123	ADC CH2 PEAK DETECTOR THRESHOLD	ADC2_PEAK_THRESH							
0x7C	124	ADC CH2 DC OFFSET	ADC2_DC_OFFSET							
0x7D	125		ADC2_DC_OFFSET							
0x7E	126	ADC CH2 VOLUME	ADC2_VOLUME							
0x7F	127		ADC2_VOLUME							
0x80	128	ADC CH2 VOLUME RATE	ADC2_VOLUME_RATE							
0x81	129	ADC CH2 GAIN	RESERVED						ADC2_DATA_GAIN	
0x82	130	ADC CH2 PROG FILTER	RESERVED			ADC2_FILTER_SHAPE			ADC2_PROG_COEFF_WRITE_EN	ADC2_PROG_COEFF_EN
0x83	131	ADC CH2 PROG FILTER COEFF ADDR	ADC2_PROG_COEFF_STAGE	ADC2_PROG_COEFF_ADDR						
0x84	132	ADC CH2 PROG FILTER COEFF	ADC2_PROG_COEFF_IN							
0x85	133		ADC2_PROG_COEFF_IN							
0x86	134		ADC2_PROG_COEFF_IN							
0x87	135	ADC CH3 DATAPATH CONTROL	ADC3_BYPASS_FIR2X	ADC3_BYPASS_FIR4X	RESERVED			ADC3_ENABLE_DC_BLOCKING	RESERVED	ADC3_NEG_SEL
0x88	136	ADC CH3 THD COMP CONFIG	ADC3_CORRECTION_ADDR						ADC3_CORRECTION_WE	ADC3_ENABLE_THD_COMP
0x89	137	ADC CH3 THD COMP DATA	ADC3_CORRECTION_DATA							
0x8A	138		ADC3_CORRECTION_DATA							
0x8B	139	ADC CH3 PEAK DETECTOR CONFIG	ADC3_LOCK_PEAK	ADC3_PEAK_DECAY_RATE					RESERVED	ADC3_ENABLE_PEAK_DETECT
0x8C	140	ADC CH3 PEAK DETECTOR THRESHOLD	ADC3_PEAK_THRESH							
0x8D	141	ADC CH3 DC OFFSET	ADC3_DC_OFFSET							
0x8E	142		ADC3_DC_OFFSET							
0x8F	143	ADC CH3 VOLUME	ADC3_VOLUME							
0x90	144		ADC3_VOLUME							
0x91	145	ADC CH3 VOLUME RATE	ADC3_VOLUME_RATE							
0x92	146	ADC CH3 GAIN	RESERVED						ADC3_DATA_GAIN	
0x93	147	ADC CH3 PROG FILTER	RESERVED			ADC3_FILTER_SHAPE			ADC3_PROG_COEFF_WRITE_EN	ADC3_PROG_COEFF_EN
0x94	148	ADC CH3 PROG FILTER COEFF ADDR	ADC3_PROG_COEFF_STAGE	ADC3_PROG_COEFF_ADDR						
0x95	149	ADC CH3 PROG FILTER COEFF	ADC3_PROG_COEFF_IN							
0x96	150		ADC3_PROG_COEFF_IN							
0x97	151		ADC3_PROG_COEFF_IN							
0x98	152	ADC CH4 DATAPATH CONTROL	ADC4_BYPASS_FIR2X	ADC4_BYPASS_FIR4X	RESERVED			ADC4_ENABLE_DC_BLOCKING	RESERVED	ADC4_NEG_SEL
0x99	153	ADC CH4 THD COMP CONFIG	ADC4_CORRECTION_ADDR						ADC4_CORRECTION_WE	ADC4_ENABLE_THD_COMP
0x9A	154	ADC CH4 THD COMP DATA	ADC4_CORRECTION_DATA							
0x9B	155		ADC4_CORRECTION_DATA							
0x9C	156	ADC CH4 PEAK DETECTOR CONFIG	ADC4_LOCK_PEAK	ADC4_PEAK_DECAY_RATE					RESERVED	ADC4_ENABLE_PEAK_DETECT
0x9D	157	ADC CH4 PEAK DETECTOR THRESHOLD	ADC4_PEAK_THRESH							
0x9E	158	ADC CH4 DC OFFSET	ADC4_DC_OFFSET							
0x9F	159		ADC4_DC_OFFSET							
0xA0	160	ADC CH4 VOLUME	ADC4_VOLUME							
0xA1	161		ADC4_VOLUME							
0xA2	162	ADC CH4 VOLUME RATE	ADC4_VOLUME_RATE							
0xA3	163	ADC CH4 GAIN	RESERVED						ADC4_DATA_GAIN	
0xA4	164	ADC CH4 PROG FILTER	RESERVED			ADC4_FILTER_SHAPE			ADC4_PROG_COEFF_WRITE_EN	ADC4_PROG_COEFF_EN
0xA5	165	ADC CH4 PROG FILTER COEFF ADDR	ADC4_PROG_COEFF_STAGE	ADC4_PROG_COEFF_ADDR						
0xA6	166	ADC CH4 PROG FILTER COEFF	ADC4_PROG_COEFF_IN							
0xA7	167		ADC4_PROG_COEFF_IN							
0xA8	168		ADC4_PROG_COEFF_IN							
0xC0	192	SOFT RESET	AO_SOFT_RESET	RESERVED						
0xC1	193	CLK SELECT	RESERVED					SEL_SYSCLK_IN		EN_ANA_CLKIN
0xC2	194	ADC CLOCK DIVIDE	RESERVED						SEL_CLK_DIV	
0xC3-0xCB	195-203	RESERVED	RESERVED							
0xE0	224	READ SYSTEM REGISTER 0	RESERVED				MODE	ADDR2	ADDR1	RESERVED
0xE1	225	CHIP ID	CHIP_ID							
0xE2-0xE4	226-227	RESERVED	RESERVED							
0xE5	229	PEAK FLAG	RESERVED				PEAK_FLAG_CH4	PEAK_FLAG_CH3	PEAK_FLAG_CH2	PEAK_FLAG_CH1
0xE6	230	READ SYSTEM REGISTER 4	RESERVED							

0xE7	231	READ SYSTEM REGISTER 5	ASP2_INIT_DONE	ASP1_INIT_DONE	RESERVED	TDM_VALID	RESERVED			
0xE8	232	GPIO READBACK REGISTERS	GPIO8_READBACK	GPIO7_READBACK	GPIO6_READBACK	GPIO5_READBACK	GPIO4_READBACK	GPIO3_READBACK	GPIO2_READBACK	GPIO1_READBACK
0xE9	233		RESERVED					GPIO11_READBACK	GPIO10_READBACK	GPIO9_READBACK
0xEA	234	ADC CH1 PROG COEFF OUT	ADC1_PROG_COEFF_OUT							
0xEB	235		ADC1_PROG_COEFF_OUT							
0xEC	236		ADC1_PROG_COEFF_OUT							
0xED	237	ADC CH1 PEAK	ADC1_PEAK							
0xEE	238		ADC1_PEAK							
0xEF	239	ADC CH2 PROG COEFF OUT	ADC2_PROG_COEFF_OUT							
0xF0	240		ADC2_PROG_COEFF_OUT							
0xF1	241		ADC2_PROG_COEFF_OUT							
0xF2	242	ADC CH2 PEAK	ADC2_PEAK							
0xF3	243		ADC2_PEAK							
0xF4	244	ADC CH3 PROG COEFF OUT	ADC3_PROG_COEFF_OUT							
0xF5	245		ADC3_PROG_COEFF_OUT							
0xF6	246		ADC3_PROG_COEFF_OUT							
0xF7	247	ADC CH3 PEAK	ADC3_PEAK							
0xF8	248		ADC3_PEAK							
0xF9	249	ADC CH4 PROG COEFF OUT	ADC4_PROG_COEFF_OUT							
0xFA	250		ADC4_PROG_COEFF_OUT							
0xFB	251		ADC4_PROG_COEFF_OUT							
0xFC	252	ADC CH4 PEAK	ADC4_PEAK							
0xFD	253		ADC4_PEAK							

Table 34 - Register Map

Register Listing

System Registers

Register 0: SYS CONFIG

Bits	[7]	[6:5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to the digital core • 1'b0: Normal operation • 1'b1: Reset digital core
[6:5]	OUTPUT_SEL	Selects output data format. • 2'd0: I²S output (default) • 2'd1: S/PDIF output • 2'd2: TDM output • 2'd3: DSD output
[4]	RESERVED	N/A
[3]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: 64FS mode disabled (default) • 1'b1: 64FS mode enabled
[2]	TWO_CH_MODE	Enables ADC two channel mode. ADC Channel 3 is mixed into ADC Channel 1. ADC Channel 4 is mixed into Channel 2. • 1'b0: Two channel mode disabled (default) • 1'b1: Two channel mode enabled
[1]	MONO_MODE	Enables mono mode. All 4-channel data is mixed into Ch1. For Ch1, mono mode has higher priority than two channel mode. Note: All Channels require an input for Mono mode to function • 1'b0: Mono mode disabled (default) • 1'b1: Mono mode enabled
[0]	RESERVED	N/A

Register 1: ADC CLOCK CONFIG1

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ENABLE_DATA_IN_CH4	Enables Ch4 data input clock (before decimation path) for data mixing. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[6]	ENABLE_DATA_IN_CH3	Enables Ch3 data input clock (before decimation path) for data mixing. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[5]	ENABLE_DATA_IN_CH2	Enables Ch2 data input clock (before decimation path) for data mixing. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[4]	ENABLE_DATA_IN_CH1	Enables Ch1 data input clock (before decimation path) for data mixing. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[3]	ENABLE_ADC_CH4	Enables ADC Ch4 decimation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[2]	ENABLE_ADC_CH3	Enables ADC Ch3 decimation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[1]	ENABLE_ADC_CH2	Enables ADC Ch2 decimation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled
[0]	ENABLE_ADC_CH1	Enables ADC Ch1 decimation path clock. • 1'b0: Clock disabled (default) • 1'b1: Clock enabled

Register 2: ADC CLOCK CONFIG2

Bits	[7:6]	[5]	[4:0]
Default	2'b00	1'b0	5'd3

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	SELECT_ADC_HALF	• 1'b0: Divide by SELECT_ADC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_ADC_NUM + 1 Note: Can only produce half of an odd number divide
[4:0]	SELECT_ADC_NUM	Whole number divide value + 1 for CLK_ADC (SYS_CLK/divide_value). • 5'd0: Whole number divide value + 1 = 1 • 5'd1: Whole number divide value + 1 = 2 • 5'd31: Whole number divide value + 1 = 32

Register 3: ADC CLOCK CONFIG3

Bits	[7:6]	[5]	[4]	[3]	[2:0]
Default	2'd0	1'b0	1'b0	1'b0	3'd0

Bits	Mnemonic	Description
[7:6]	OUTPUT2_SEL	Selects DATA2 output (GPIO4) when FORCE_OUTPUT2 is set. • 2'd0: I²S output (default) • 2'd1: S/PDIF output • 2'd2: TDM output • 2'd3: DSD output
[5]	FORCE_OUTPUT2	Forces DATA2 output (GPIO4) to output from a different source, controlled by OUTPUT2_SEL. • 1'b0: Use OUTPUT_SEL (default) • 1'b1: Use OUTPUT2_SEL
[4]	INVERT_FIRST_CLK_SAMPLE2	Firstly, use neg edge of CLK_SAMPLE2 to sample adc_data_r1. Only used when different CLK_SAMPLE1 edges are used for the 4ch to ensure phase alignment. • 1'b0: Use pos edge of CLK_SAMPLE2 to sample adc_data_r1 (default) • 1'b1: Use neg edge of CLK_SAMPLE2 to sample adc_data_r1
[3]	SELECT_IADC_HALF	• 1'b0: Divide by SELECT_IADC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_IADC_NUM + 1 Note: Can only produce half of an odd number divide
[2:0]	SELECT_IADC_NUM	Whole number divide value + 1 for CLK_IADC (SYS_CLK/divide_value). • 3'd0: Whole number divide value + 1 = 1 (default) • 3'd1: Whole number divide value + 1 = 2 • 3'd7: Whole number divide value + 1 = 8

Register 4: ADC CLOCK CONFIG4

Bits	[7]	[6:4]	[3]	[2]	[1]	[0]
Default	1'b0	3'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	FORCE_PHASE_CLK_IADC	Sets phase of CLK_IADC by PHASE_CLK_IADC. • 1'b0: Auto phase tuning if AUTO_CLK_IADC_PHASE_SYNC is set (default) • 1'b1: Sets phase by PHASE_CLK_IADC
[6:4]	PHASE_CLK_IADC	Sets phase of CLK_IADC relative to SYS_CLK when FORCE_PHASE_CLK_IADC is set. For 48M SYS_CLK and 24M CLK_IADC only. • 3'd0: Phase 0 (default) • 3'd1: Phase 1 • others: Reserved
[3]	INVERT_SAMPLE_CLOCK_CH4	Inverts ADC Ch4 data sampling clock. • 1'b0: Not inverted (default) • 1'b1: Inverted
[2]	INVERT_SAMPLE_CLOCK_CH3	Inverts ADC Ch3 data sampling clock. • 1'b0: Not inverted (default) • 1'b1: Inverted
[1]	INVERT_SAMPLE_CLOCK_CH2	Inverts ADC Ch2 data sampling clock. • 1'b0: Not inverted (default) • 1'b1: Inverted
[0]	INVERT_SAMPLE_CLOCK_CH1	Inverts ADC Ch1 data sampling clock. • 1'b0: Not inverted (default) • 1'b1: Inverted

Register 5: RAW DATA AND SPDIF CONFIG

Bits	**[7:6]**	**[5]**	**[4]**	**[3]**	**[2]**	**[1:0]**
Default	2'd0	1'b0	1'b0	1'b0	1'b0	2'd0

Bits	**Mnemonic**	**Description**
[7:6]	SELECT_RAW_DATA_NUM	Whole number divide value + 1 for raw data clock (SYS_CLK/divide_value). When SELECT_RAW_DATA_NUM is larger than 0, the divided clock is not a 50% duty cycle clock. • 2'd0: Whole number divide value + 1 = 1 (default) • 2'd1: Whole number divide value + 1 = 2 • 2'd2: Whole number divide value + 1 = 3 • 2'd3: Whole number divide value + 1 = 4
[5]	RAW_DATA_CLK_DIV2	Further divides the raw data clock by 2 (after divided by SELECT_RAW_DATA_NUM+1) to create a 50% duty cycle raw data clock. • 1'b0: No divide (default) • 1'b1: Further divides the raw data clock by 2
[4]	RAW_DATA_DDR	Enables raw data double-data-rate (DDR) output. In the DDR mode, raw data is valid on both pos/neg edges of raw data clock. Otherwise, raw data is valid only on positive edge of raw data clock. • 1'b0: Double-data-rate disabled (default) • 1'b1: Double-data-rate enabled
[3]	ENABLE_RAW_DATA_CLK	Enables raw data clock. • 1'b0: Raw data clock disabled (default) • 1'b1: Raw data clock enabled
[2]	ENABLE_SPDIF_CLK	Enables S/PDIF encoding clock. • 1'b0: S/PDIF clock disabled (default) • 1'b1: S/PDIF clock enabled
[1:0]	RESERVED	N/A

Register 6: DSD CONFIG

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'b00	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DSD_DDR	Enables DSD double-data-rate (DDR) output. In the DDR mode, DSD data is valid on both pos/neg edges of DSD clock. Otherwise, DSD data is valid only on positive edge of DSD clock.
[4]	DSD_MASTER_MODE	Enables DSD master mode and generates DSD clock. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	ENABLE_DSD_CLK_CH4	Enables Ch4 DSD encoding clock. • 1'b0: DSD clock disabled (default) • 1'b1: DSD clock enabled
[2]	ENABLE_DSD_CLK_CH3	Enables Ch3 DSD encoding clock. • 1'b0: DSD clock disabled (default) • 1'b1: DSD clock enabled
[1]	ENABLE_DSD_CLK_CH2	Enables Ch2 DSD encoding clock. • 1'b0: DSD clock disabled (default) • 1'b1: DSD clock enabled
[0]	ENABLE_DSD_CLK_CH1	Enables Ch1 DSD encoding clock. • 1'b0: DSD clock disabled (default) • 1'b1: DSD clock enabled

Register 7: DSD AND I²S/TDM MASTER CLK CONFIG

Bits	[7:5]	[4]	[3:0]
Default	3'd0	1'b0	4'd0

Bits	Mnemonic	Description
[7:5]	MASTER_WS_SCALE	In I²S/TDM master mode, tunes master BCK/WS ratio by scaling master WS. It allows more TDM slots in a fixed frame. • 3'd0: No scale (default) • 3'd1: Scale down WS by 2 • 3'd2: Scale down WS by 4 • 3'd3: Scale down WS by 8 • 3'd4: Scale down WS by 16 • others: Reserved
[4]	DSD_CLK_DIV2	Further divides the DSD clock by 2 (after divided by SELECT_DSD_NUM+1) to create a 50% duty cycle DSD clock. • 1'b0: No divide (default) • 1'b1: Further divides the DSD clock by 2
[3:0]	SELECT_DSD_NUM	Whole number divide value + 1 for DSD clock (SYS_CLK/divide_value). When SELECT_DSD_NUM is larger than 0, the divided clock is not a 50% duty cycle clock. • 4'd0: Whole number divide value + 1 = 1 (default) • 4'd1: Whole number divide value + 1 = 2 • 4'd15: Whole number divide value + 1 = 16

Register 8: I²S/TDM MASTER MODE CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	MASTER_BCK_DIV1	When enabled, master BCK is I²S/TDM master encoding clock. Otherwise, BCK is less than or equal to (I²S/TDM master encoding clock)/2 (unless ENABLE_64FS_MODE is set). • 1'b0: BCK is not I²S/TDM master encoding clock (default) • 1'b1: BCK is I²S/TDM master encoding clock
[6]	MASTER_WS_IDLE	Sets the value of master WS when WS is idle. • 1'b0: WS is 0 when idle (default) • 1'b1: WS is 1 when idle
[5:4]	MASTER_FRAME_LENGTH	Selects the bit length in each I²S/TDM channel in master mode. • 2'd0: 32 bit (default) • 2'd2: 16 bit • Others: Reserved
[3]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[2]	MASTER_BCK_INVERT	Inverts master BCK. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_MODE_ENABLE	Enables I²S/TDM master mode and generates master BCK and master WS. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 9: I²S/TDM MASTER CLK CONFIG

Bits	[7]	[6:0]
Default	1'b0	7'd3

Bits	Mnemonic	Description
[7]	SELECT_I²S_TDM_HALF	• 1'b0: Divide by SELECT_I²S_TDM_NUM + 1 (default) • 1'b1: Divide by half of SELECT_I²S_TDM_NUM + 1 Note: Can only produce half of an odd number divide
[6:0]	SELECT_I²S_TDM_NUM	Whole number divide value + 1 for I²S/TDM master encoding clock (SYS_CLK/divide_value). • 7'd0: Whole number divide value + 1 = 1 (default) • 7'd1: Whole number divide value + 1 = 2 • 7'd127: Whole number divide value + 1 = 128

Register 10: TDM CONFIG1

Bits	[7:3]	[2]	[1]	[0]
Default	5'd0	1'b1	1'b0	1'b1

Bits	Mnemonic	Description
[7:3]	TDM_BIT_DELAY	Indicates the MSB-2 position of the data from the frame start. Valid from 5'd0 to 5'd31.
[2]	TDM_VALID_EDGE	Sets on which WS edge the frame starts. • 1'b0: Frame starts on posedge of WS • 1'b1: Frame starts on negedge of WS (default)
[1]	TDM_LJ	Sets left-justified mode. • 1'b0: No left-justified (default) • 1'b1: Left-justified
[0]	ENABLE_TDM_CLK	Enables I²S/TDM encoding clock. • 1'b0: I²S/TDM clock disabled • 1'b1: I²S/TDM clock enabled (default)

Register 11: TDM CONFIG2

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd1

Bits	Mnemonic	Description
[7]	TDM_GPIO456	Allows GPIO 4,5,6 to output TDM ADC data. Allows GPIO 4,5,6 to output TDM ADC data. • 1'b0: Disabled (default), TDM data uses GPIO3 • 1'b1: Enabled, allows TDM data on GPIO3-6
[6]	TDM_CASCADE	Enables TDM cascade mode. In TDM cascade mode, GPIO4 is used as the cascade data input. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	TDM_LENGTH	Sets data length in each channel. • 1'b0: 32 bits (default) • 1'b1: 16 bits
[4:0]	TDM_CH_NUM	Sets number of channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 12: TDM SLOT CONFIG CH1

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH1	Selects ADC CH1 data is presented on which TDM data line. • 2'd0: TDM data line 1 - GPIO3 (default) • 2'd1: TDM data line 2 - GPIO4 • 2'd2: TDM data line 3 - GPIO5 • 2'd3: TDM data line 4 - GPIO6
[4:0]	TDM_SLOT_SEL_CH1	Selects which TDM channel slot is filled by ADC CH1 data. • 5'd0: Slot 1 (default) • 5'd1: Slot 2 • 5'd31: Slot 32

Register 13: TDM SLOT CONFIG CH2

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH2	Selects ADC CH2 data is presented on which TDM data line. • 2'd0: TDM data line 1 - GPIO3 (default) • 2'd1: TDM data line 2 - GPIO4 • 2'd2: TDM data line 3 - GPIO5 • 2'd3: TDM data line 4 - GPIO6
[4:0]	TDM_SLOT_SEL_CH2	Selects which TDM channel slot is filled by ADC CH2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 14: TDM SLOT CONFIG CH3

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd2

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH3	Selects ADC CH3 data is presented on which TDM data line. • 2'd0: TDM data line 1 - GPIO3 (default) • 2'd1: TDM data line 2 - GPIO4 • 2'd2: TDM data line 3 - GPIO5 • 2'd3: TDM data line 4 - GPIO6
[4:0]	TDM_SLOT_SEL_CH3	Selects which TDM channel slot is filled by ADC CH3 data. • 5'd0: Slot 1 • 5'd1: Slot 2 • 5'd2: Slot 3 (default) • 5'd31: Slot 32

Register 15: TDM SLOT CONFIG CH4

Bits	**[7]**	**[6:5]**	**[4:0]**
Default	1'b0	2'd0	5'd3

Bits	**Mnemonic**	**Description**
[7]	RESERVED	N/A
[6:5]	TDM_LINE_SEL_CH4	Selects ADC CH4 data is presented on which TDM data line. • 2'd0: TDM data line 1 - GPIO3 (default) • 2'd1: TDM data line 2 - GPIO4 • 2'd2: TDM data line 3 - GPIO5 • 2'd3: TDM data line 4 - GPIO6
[4:0]	TDM_SLOT_SEL_CH4	Selects which TDM channel slot is filled by ADC CH4 data. • 5'd0: Slot 1 • 5'd1: Slot 2 • 5'd3: Slot 4 (default) • 5'd31: Slot 32

Register 16: RAW DATA OUTPUT CONFIG

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	RAW_DATA_MIX_DIV2_CH2_4	Divides the mixed Ch4-Ch2 raw data by 2. • 1'b0: No divide (default) • 1'b1: Divides by 2
[4]	RAW_DATA_MIX_DIV2_CH1_3	Divides the mixed Ch3-Ch1 raw data by 2. • 1'b0: No divide (default) • 1'b1: Divides by 2
[3]	ENABLE_RAW_DATA_MIX_CH2_4	Enables Ch2 and Ch4 raw data mixing. Mixed data = Ch4-Ch2. • 1'b0: No mix (default) • 1'b1: Enables mixing
[2]	ENABLE_RAW_DATA_MIX_CH1_3	Enables Ch1 and Ch3 raw data mixing. Mixed data = Ch3-Ch1. • 1'b0: No mix (default) • 1'b1: Enables mixing
[1]	NEG_RAW_DATA_SUB_CH2	Inverts ADC Ch2 raw data for Ch4-Ch2 raw data mixing. • 1'b0: No inversion (default) • 1'b1: Inverts Ch2 raw data
[0]	NEG_RAW_DATA_SUB_CH1	Inverts ADC Ch1 raw data for Ch3-Ch1 raw data mixing. • 1'b0: No inversion (default) • 1'b1: Inverts Ch1 raw data

Register 17: INPUT DATA MAPPING

Bits	[7:6]	[5:4]	[3:2]	[1:0]
Default	2'd3	2'd2	2'd1	2'd0

Bits	Mnemonic	Description
[7:6]	INPUT_DATA_MAPPING_CH4	Re-maps Ch4 data from 1 of the 4 analog ADC data inputs. • 2'd0: Ch4 data is from analog ADC Ch1 • 2'd1: Ch4 data is from analog ADC Ch2 • 2'd2: Ch4 data is from analog ADC Ch3 • 2'd3: Ch4 data is from analog ADC Ch4 (default)
[5:4]	INPUT_DATA_MAPPING_CH3	Re-maps Ch3 data from 1 of the 4 analog ADC data inputs. • 2'd0: Ch3 data is from analog ADC Ch1 • 2'd1: Ch3 data is from analog ADC Ch2 • 2'd2: Ch3 data is from analog ADC Ch3 (default) • 2'd3: Ch3 data is from analog ADC Ch4
[3:2]	INPUT_DATA_MAPPING_CH2	Re-maps Ch2 data from 1 of the 4 analog ADC data inputs. • 2'd0: Ch2 data is from analog ADC Ch1 • 2'd1: Ch2 data is from analog ADC Ch2 (default) • 2'd2: Ch2 data is from analog ADC Ch3 • 2'd3: Ch2 data is from analog ADC Ch4
[1:0]	INPUT_DATA_MAPPING_CH1	Re-maps Ch1 data from 1 of the 4 analog ADC data inputs. • 2'd0: Ch1 data is from analog ADC Ch1 (default) • 2'd1: Ch1 data is from analog ADC Ch2 • 2'd2: Ch1 data is from analog ADC Ch3 • 2'd3: Ch1 data is from analog ADC Ch4

Register 18: PCM DATA OUTPUT MAPPING

Bits	[7:6]	[5:4]	[3:2]	[1:0]
Default	2'd3	2'd2	2'd1	2'd0

Bits	Mnemonic	Description
[7:6]	OUTPUT_MAPPING_CH4	Re-maps Ch4 PCM data output from 1 of the 4 ADC decimation paths or ASP outputs (when ASP is enabled). • 2'd0: Ch4 PCM data output is from ADC decimation path Ch1 or ASP output Ch1 • 2'd1: Ch4 PCM data output is from ADC decimation path Ch2 or ASP output Ch2 • 2'd2: Ch4 PCM data output is from ADC decimation path Ch3 or ASP output Ch3 • 2'd3: Ch4 PCM data output is from ADC decimation path Ch4 or ASP output Ch4 (default)
[5:4]	OUTPUT_MAPPING_CH3	Re-maps Ch3 PCM data output from 1 of the 4 ADC decimation paths or ASP outputs (when ASP is enabled). • 2'd0: Ch3 PCM data output is from ADC decimation path Ch1 or ASP output Ch1 • 2'd1: Ch3 PCM data output is from ADC decimation path Ch2 or ASP output Ch2 • 2'd2: Ch3 PCM data output is from ADC decimation path Ch3 or ASP output Ch3 (default) • 2'd3: Ch3 PCM data output is from ADC decimation path Ch4 or ASP output Ch4
[3:2]	OUTPUT_MAPPING_CH2	Re-maps Ch2 PCM data output from 1 of the 4 ADC decimation paths or ASP outputs (when ASP is enabled). • 2'd0: Ch2 PCM data output is from ADC decimation path Ch1 or ASP output Ch1 • 2'd1: Ch2 PCM data output is from ADC decimation path Ch2 or ASP output Ch2 (default) • 2'd2: Ch2 PCM data output is from ADC decimation path Ch3 or ASP output Ch3 • 2'd3: Ch2 PCM data output is from ADC decimation path Ch4 or ASP output Ch4
[1:0]	OUTPUT_MAPPING_CH1	Re-maps Ch1 PCM data output from 1 of the 4 ADC decimation paths or ASP outputs (when ASP is enabled). • 2'd0: Ch1 PCM data output is from ADC decimation path Ch1 or ASP output Ch1 (default) • 2'd1: Ch1 PCM data output is from ADC decimation path Ch2 or ASP output Ch2 • 2'd2: Ch1 PCM data output is from ADC decimation path Ch3 or ASP output Ch3 • 2'd3: Ch1 PCM data output is from ADC decimation path Ch4 or ASP output Ch4

Register 19: DSD DATA OUTPUT MAPPING

Bits	[7:6]	[5:4]	[3:2]	[1:0]
Default	2'd3	2'd2	2'd1	2'd0

Bits	Mnemonic	Description
[7:6]	DSD_MAPPING_CH4	Re-maps Ch4 DSD data output from 1 of the 4 ADC decimation paths. • 2'd0: Ch4 DSD data output is from ADC decimation path Ch1 • 2'd1: Ch4 DSD data output is from ADC decimation path Ch2 • 2'd2: Ch4 DSD data output is from ADC decimation path Ch3 • 2'd3: Ch4 DSD data output is from ADC decimation path Ch4 (default)
[5:4]	DSD_MAPPING_CH3	Re-maps Ch3 DSD data output from 1 of the 4 ADC decimation paths. • 2'd0: Ch3 DSD data output is from ADC decimation path Ch1 • 2'd1: Ch3 DSD data output is from ADC decimation path Ch2 • 2'd2: Ch3 DSD data output is from ADC decimation path Ch3 (default) • 2'd3: Ch3 DSD data output is from ADC decimation path Ch4
[3:2]	DSD_MAPPING_CH2	Re-maps Ch2 DSD data output from 1 of the 4 ADC decimation paths. • 2'd0: Ch2 DSD data output is from ADC decimation path Ch1 • 2'd1: Ch2 DSD data output is from ADC decimation path Ch2 (default) • 2'd2: Ch2 DSD data output is from ADC decimation path Ch3 • 2'd3: Ch2 DSD data output is from ADC decimation path Ch4
[1:0]	DSD_MAPPING_CH1	Re-maps Ch1 DSD data output from 1 of the 4 ADC decimation paths. • 2'd0: Ch1 DSD data output is from ADC decimation path Ch1 (default) • 2'd1: Ch1 DSD data output is from ADC decimation path Ch2 • 2'd2: Ch1 DSD data output is from ADC decimation path Ch3 • 2'd3: Ch1 DSD data output is from ADC decimation path Ch4

Register 20: TPDF DITHER LEVEL

Bits	[7:5]	[4:0]
Default	3'd0	5'd16

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	DITHER_SCALE	TPDF dither level: • 5'd0: 16 bits • 5'd1: 17 bits • 5'd2: 18 bits • 5'd3: 19 bits • 5'd4: 20 bits • 5'd5: 21 bits • 5'd6: 22 bits • 5'd7: 23 bits • 5'd8: 24 bits • 5'd9: 25 bits • 5'd10: 26 bits • 5'd11: 27 bits • 5'd12: 28 bits • 5'd13: 29 bits • 5'd14: 30 bits • 5'd15: 31 bits • 5'd16: 32 bits (TPDF dither disabled) (default) • Others: Reserved

Register 22-21: DITHER MASK

Bits	[15:0]
Default	16'hFFFF

Bits	Mnemonic	Description
[15:0]	DITHER_MASK	Mask off the LSB's of PCM data output. • 16'h0000: Quantized to 16 bits • 16'h8000: Quantized to 17 bits • 16'hC000: Quantized to18 bits • 16'hE000: Quantized to 19 bits • 16'hF000: Quantized to 20 bits • 16'hF800: Quantized to 21 bits • 16'hFC00: Quantized to 22 bits • 16'hFE00: Quantized to 23 bits • 16'hFF00: Quantized to 24 bits • 16'hFF80: Quantized to 25 bits • 16'hFFC0: Quantized to 26 bits • 16'hFFE0: Quantized to 27 bits • 16'hFFF0: Quantized to 28 bits • 16'hFFF8: Quantized to 29 bits • 16'hFFFC: Quantized to 30 bits • 16'hFFFE: Quantized to 31 bits • 16'hFFFF: Quantized to 32 bits (default) • Others: Reserved

Register 23: FS GEN PHASE CONTROL

Bits	[7]	[6:0]
Default	1'b0	7'd4

Bits	Mnemonic	Description
[7]	DSD_SYNC_TO_1FS	In DSD mode, when enabled, DSD logic is sync to an 1FS signal input from GPIO2. When not enabled, DSD logic is sync to DSD clock input from GPIO1. • 1'b0: DSD logic is sync to DSD clock input from GPIO1 (default) • 1'b1: DSD logic is sync to 1FS signal input from GPIO2
[6:0]	FS_PHASE	Controls phase of the generated FS signals. • Valid from 7'd0 to 7'd127 Note: Should be set to 7'd10 for phase alignment of all sample rates and serial modes

Register 26-24: RESERVED

Register 27: INTERRUPT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	INTERRUPT_CLEAR_CH4_PEAK_DETECT	Clears the peak detector interrupt of ADC CH4. • 1'b0: Interrupt held if asserted and not masked (default) • 1'b1: Interrupt cleared
[6]	INTERRUPT_CLEAR_CH3_PEAK_DETECT	Clears the peak detector interrupt of ADC CH3. • 1'b0: Interrupt held if asserted and not masked (default) • 1'b1: Interrupt cleared
[5]	INTERRUPT_CLEAR_CH2_PEAK_DETECT	Clears the peak detector interrupt of ADC CH2. • 1'b0: Interrupt held if asserted and not masked (default) • 1'b1: Interrupt cleared
[4]	INTERRUPT_CLEAR_CH1_PEAK_DETECT	Clears the peak detector interrupt of ADC CH1. • 1'b0: Interrupt held if asserted and not masked (default) • 1'b1: Interrupt cleared
[3]	INTERRUPT_MASK_CH4_PEAK_DETECT	Masks the peak detector interrupt of ADC CH4. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt held if asserted
[2]	INTERRUPT_MASK_CH3_PEAK_DETECT	Masks the peak detector interrupt of ADC CH3. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt held if asserted
[1]	INTERRUPT_MASK_CH2_PEAK_DETECT	Masks the peak detector interrupt of ADC CH2. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt held if asserted
[0]	INTERRUPT_MASK_CH1_PEAK_DETECT	Masks the peak detector interrupt of ADC CH1. • 1'b0: Interrupt masked (default) • 1'b1: Interrupt held if asserted

Register 32-28: SPDIF SUBCODE CONFIG

Bits	[39:0]
Default	40'd0

Bits	Mnemonic	Description
[39:0]	SPDIF_CS	Configures SPDIF sub-code bits.

Register 33: DSD DITHER SCALE & SYNC CONTROL

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd21

Bits	Mnemonic	Description
[7]	SYNC_POSEDGE_FRAME	Selects the logic is sync to which edge of the sync reference signal. • 1'b0: Sync to negative edge of the sync reference (default) • 1'b1: Sync to positive edge of the sync reference
[6]	DISABLE_SYNC_REF	Disables the sync reference. • 1'b0: Sync reference enabled (default) • 1'b1: Sync reference disabled
[5]	FORCE_FIR_SYNC	Forces FIR to re-sync to the reference. • 1'b0: No force (default) • 1'b1: Forces FIR to re-sync
[4:0]	DSD_DITHER_SCALE	DSD noise shaped dither scale.

Register 34: SYNC CONTROL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	AUTO_ADC_CLKDIV_SYNC	When enabled, the analog ADC clock divider is only allowed to change synchronously to the reference. • 1'b0: Auto sync disabled (default) • 1'b1: Auto sync enabled
[6]	AUTO_CLK_IADC_PHASE_SYNC	Allows phase of CLK_IADC to be tuned automatically according to ADC input data. Only used when SYS_CLK is faster than CLK_IADC. • 1'b0: CLK_IADC phase tuning disabled (default) • 1'b1: Auto CLK_IADC phase tuning
[5]	AUTO_DSD_PHASE_SYNC	Uses DSD clock input from GPIO1 as the sync reference, unless DSD_SYNC_TO_1FS is set. • 1'b0: DSD clock is not the sync reference (default) • 1'b1: DSD clock is the sync reference, unless DSD_SYNC_TO_1FS is set
[4]	AUTO_WS_PHASE_SYNC	Uses WS input from GPIO2 as the sync reference, if AUTO_DSD_PHASE_SYNC is not set. • 1'b0: WS is not the sync reference • 1'b1: WS is the sync reference, if AUTO_DSD_PHASE_SYNC is not set (default)
[3]	AUTO_ICG_EN_SYNC	When enabled, the clock dividers and ADC enables are only allowed to change synchronously to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)
[2]	AUTO_ICG_SYNC	Allows programmable clock dividers to auto sync to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)
[1]	AUTO_FIR_SYNC	Allows FIR to auto sync to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)
[0]	AUTO_FS_SYNC	Allows FS signals to auto sync to the reference. • 1'b0: Auto sync disabled • 1'b1: Auto sync enabled (default)

ASP Registers

Register 35: ASP1 CONFIG

Bits	[7:6]	[5:1]	[0]
Default	2'b00	5'd0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:1]	SELECT_ASP1_NUM	Whole number divide value + 1 for ASP1 clock (SYS_CLK/divide_value). • 5'd0: Whole number divide value + 1 = 1 (default) • 5'd1: Whole number divide value + 1 = 2 • 5'd31: Whole number divide value + 1 = 32
[0]	ENABLE_ASP1_CLK	Enables ASP1 clock. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 36: ASP2 CONFIG

Bits	[7:6]	[5:1]	[0]
Default	2'b00	5'd0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:1]	SELECT_ASP2_NUM	Whole number divide value + 1 for ASP2 clock (SYS_CLK/divide_value). • 5'd0: Whole number divide value + 1 = 1 (default) • 5'd1: Whole number divide value + 1 = 2 • 5'd31: Whole number divide value + 1 = 32
[0]	ENABLE_ASP2_CLK	Enables ASP2 clock. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 37: ASP ENABLE & PROGRAM CONTROL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ASP2_COEFF_WE	Enables writing to the ASP2 coeff RAM. • 1'b0: Writing disabled (default) • 1'b1: Writing enabled
[6]	ASP1_COEFF_WE	Enables writing to the ASP1 coeff RAM. • 1'b0: Writing disabled (default) • 1'b1: Writing enabled
[5]	ASP2_PROGRAM_WE	Enables writing to the ASP2 program memory. • 1'b0: Writing disabled (default) • 1'b1: Writing enabled
[4]	ASP1_PROGRAM_WE	Enables writing to the ASP1 program memory. • 1'b0: Writing disabled (default) • 1'b1: Writing enabled
[3]	ASP2_PROGRAM_EN	Enables ASP2 program memory and coeff RAM programming before its output is enabled and used in the signal path. • 1'b0: Programming disabled (default) • 1'b1: Programming enabled
[2]	ASP1_PROGRAM_EN	Enables ASP1 program memory and coeff RAM programming before its output is enabled and used in the signal path. • 1'b0: Programming disabled (default) • 1'b1: Programming enabled
[1]	ENABLE_ASP2	Selects whether ASP2 is enabled and used in the signal path or disabled and bypassed. • 1'b0: ASP2 is disabled and bypassed (default) • 1'b1: ASP2 is enabled. Data is processed by ASP2 before output
[0]	ENABLE_ASP1	Selects whether ASP1 is enabled and used in the signal path or disabled and bypassed. • 1'b0: ASP1 is disabled and bypassed (default) • 1'b1: ASP1 is enabled. Data is processed by ASP1 before output

Register 39-38: ASP PROGRAM ADDR

Bits	[15:9]	[8:0]
Default	7'd0	9'd0

Bits	Mnemonic	Description
[15:9]	RESERVED	N/A
[8:0]	ASP_PROGRAM_ADDR	Selects the program address when writing custom program codes for either ASP.

Register 41-40: ASP PROGRAM

Bits	[15:14]	[13:0]
Default	2'd0	14'd0

Bits	Mnemonic	Description
[15:14]	RESERVED	N/A
[13:0]	ASP_PROGRAM_IN	A 14 bits program instruction that will be written to the address of either ASP defined by ASP_PROGRAM_ADDR.

Register 42: ASP COEFF ADDR

Bits	[7:6]	[5:0]
Default	2'd0	6'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:0]	ASP_COEFF_ADDR	Selects the coefficient address when writing custom coefficient for either ASP.

Register 50-43: ASP COEFF

Bits	[63:32]	[31:0]
Default	32'd0	32'd0

Bits	Mnemonic	Description
[63:32]	ASP_COEFF_MSB	A 32 bits coefficient that will be written to the address defined by ASP_COEFF_ADDR. These last 32 bits are typically used for the channel 2 data.
[31:0]	ASP_COEFF_LSB	A 32 bits coefficient that will be written to the address defined by ASP_COEFF_ADDR. These first 32 bits are typically used for the channel 1 data.

Register 51: ASP1 CH1 STEP SIZE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	ASP1_CH1_STEP_SIZE	Programmable value to be used in multiplications for Ch1 within ASP1.

Register 52: ASP1 CH2 STEP SIZE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	ASP1_CH2_STEP_SIZE	Programmable value to be used in multiplications for Ch2 within ASP1.

Register 53: ASP2 CH1 STEP SIZE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	ASP2_CH1_STEP_SIZE	Programmable value to be used in multiplications for Ch1 within ASP2.

Register 54: ASP2 CH2 STEP SIZE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	ASP2_CH2_STEP_SIZE	Programmable value to be used in multiplications for Ch2 within ASP2.

Register 55: ASP1 CUSTOM ADDR

Bits	[7:6]	[5:0]
Default	2'd0	6'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:0]	ASP1_CUSTOM_ADDR	Custom address that can be accessed through the MOV_RAM1_ADDR instruction in ASP1.

Register 56: ASP1 CUSTOM ADDR2

Bits	[7:6]	[5:0]
Default	2'd0	6'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:0]	ASP1_CUSTOM_ADDR2	Custom address that can be accessed through the MOV_RAM2_ADDR instruction in ASP1.

Register 57: ASP2 CUSTOM ADDR

Bits	[7:6]	[5:0]
Default	2'd0	6'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:0]	ASP2_CUSTOM_ADDR	Custom address that can be accessed through the MOV_RAM1_ADDR instruction in ASP2.

Register 58: ASP2 CUSTOM ADDR2

Bits	**[7:6]**	**[5:0]**
Default	2'd0	6'd0

Bits	**Mnemonic**	**Description**
[7:6]	RESERVED	N/A
[5:0]	ASP2_CUSTOM_ADDR2	Custom address that can be accessed through the MOV_RAM2_ADDR instruction in ASP2.

Delay Line Registers

Register 60-59: I²S DECODER CONFIG

Bits	**[15:14]**	**[13:12]**	**[11]**	**[10]**	**[9:0]**
Default	2'd0	2'd0	1'b0	1'b0	10'd0

Bits	**Mnemonic**	**Description**
[15:14]	I²S_DECODER_WORD_WIDTH	Sets the number of bits in a channel. • 2'd0: 32 bits (default) • 2'd1: 24 bits • 2'd2: 16 bits • 2'd3: Reserved
[13:12]	I²S_DECODER_BIT_DEPTH	Sets the number of bits of data. • 2'd0: 24 bits (default) • 2'd2: 16 bits • Others: Reserved
[11]	I²S_DECODER_POSEDGE_FRAME	Sets where the frame starts. • 1'b0: Indicates frame starts on negedge of WS (default) • 1'b1: Indicates frame starts on posedge of WS
[10]	ENABLE_I²S_DECODER	Enables I²S decoder. • 1'b0: Disabled (default) • 1'b1: Enabled
[9:0]	I²S_DECODER_BIT_START	Indicates the MSB-2 position of the data from the frame start. Valid from 10'h000 to 10'h3FF

Register 62-61: DELAY LINE CONFIG

Bits	**[15:10]**	**[9]**	**[8:0]**
Default	6'b101000	1'b0	9'd0

Bits	**Mnemonic**	**Description**
[15:10]	RESERVED	N/A
[9]	ENABLE_CLK_DL	Enables delay line clock and data output. • 1'b0: Disabled (default) • 1'b1: Enabled
[8:0]	PROG_DELAY_LINE	Sets the length of the delay line. • 9'd0: No delay (default) • 9'd1: Delay the I²S input data by 1 sample • 9'd2: Delay the I²S input data by 2 samples • 9'd511: Delay the I²S input data by 511 samples

Register 63: ADC CH1 CONFIG 1

Bits	**[7:6]**	**[5:4]**	**[3]**	**[2]**	**[1]**	**[0]**
Default	2'b00	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	**Mnemonic**	**Description**
[7:6]	ADC_INT2_SEL_CH1	ADC integrator control for Channel 1. • Program to 2'b10 for optimum performance
[5:4]	ADC_INT1_SEL_CH1	ADC integrator control for Channel 1. • Program to 2'b11 for optimum performance
[3]	ADC_EN_FB_CH1	Enable ADC1 feedback path. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	RESERVED	N/A
[1]	ADC_EN_INT_CH1	Enable for INT for Channel 1. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_EN_CH1	Enable for Comparator and Logic for Channel 1. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 64: ADC CH1 CONFIG 2

Bits	[7:5]	[4:3]	[2]	[1]	[0]
Default	3'b000	2'b00	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	ADC_COMP_SEL_CH1	Sets the gain of the comparator for Channel 1. • Program to 3'b001 for optimum performance
[4:3]	ADC_SUM_SEL_CH1	Sets the bandwidth of the summing amplifier for Channel 1. • Program to 2'b11 for optimum performance
[2]	ADC_USE_DITHER_EXT_CH1	Enable the external dither for Channel 1. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ADC_USE_DITHER_CH1	Enable the dither for Channel 1. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_USE_STATE_CH1	Use state as logic output for Channel 1. • Default value is 0.

Register 65: ADC CH2 CONFIG 1

Bits	[7:6]	[5:4]	[3]	[2]	[1]	[0]
Default	2'b00	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	ADC_INT2_SEL_CH2	ADC integrator control for Channel 2. • Program to 2'b10 for optimum performance
[5:4]	ADC_INT1_SEL_CH2	ADC integrator control for Channel 2. • Program to 2'b11 for optimum performance
[3]	ADC_EN_FB_CH2	Enable ADC2 feedback path. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	RESERVED	N/A
[1]	ADC_EN_INT_CH2	Enable for INT for Channel 2. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_EN_CH2	Enable for Comparator and Logic for Channel 2. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 66: ADC CH2 CONFIG 2

Bits	[7:5]	[4:3]	[2]	[1]	[0]
Default	3'b000	2'b00	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	ADC_COMP_SEL_CH2	Sets the gain of the comparator for Channel 2. • Program to 3'b001 for optimum performance
[4:3]	ADC_SUM_SEL_CH2	Sets the bandwidth of the summing amplifier for Channel 2. • Program to 2'b11 for optimum performance
[2]	ADC_USE_DITHER_EXT_CH2	Enable the external dither for Channel 2. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ADC_USE_DITHER_CH2	Enable the dither for Channel 2. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_USE_STATE_CH2	Use state as logic output for Channel 2. • Default value is 0.

Register 67: ADC CH3 CONFIG 1

Bits	[7:6]	[5:4]	[3]	[2]	[1]	[0]
Default	2'b00	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	ADC_INT2_SEL_CH3	ADC integrator control for Channel 3. • Program to 2'b10 for optimum performance
[5:4]	ADC_INT1_SEL_CH3	ADC integrator control for Channel 3. • Program to 2'b11 for optimum performance
[3]	ADC_EN_FB_CH3	Enable ADC3 feedback path. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	RESERVED	N/A
[1]	ADC_EN_INT_CH3	Enable for INT for Channel 3. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_EN_CH3	Enable for Comparator and Logic for Channel 3. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 68: ADC CH3 CONFIG 2

Bits	[7:5]	[4:3]	[2]	[1]	[0]
Default	3'b000	2'b00	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	ADC_COMP_SEL_CH3	Sets the gain of the comparator for Channel 3. • Program to 3'b001 for optimum performance
[4:3]	ADC_SUM_SEL_CH3	Sets the bandwidth of the summing amplifier for Channel 3. • Program to 2'b11 for optimum performance
[2]	ADC_USE_DITHER_EXT_CH3	Enable the external dither for Channel 3. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ADC_USE_DITHER_CH3	Enable the dither for Channel 3. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_USE_STATE_CH3	Use state as logic output for Channel 3. • Default value is 0.

Register 69: ADC CH4 CONFIG 1

Bits	[7:6]	[5:4]	[3]	[2]	[1]	[0]
Default	2'b00	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	ADC_INT2_SEL_CH4	ADC integrator control for Channel 4. • Program to 2'b10 for optimum performance
[5:4]	ADC_INT1_SEL_CH4	ADC integrator control for Channel 4. • Program to 2'b11 for optimum performance
[3]	ADC_EN_FB_CH4	Enable ADC4 feedback path. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	RESERVED	N/A
[1]	ADC_EN_INT_CH4	Enable for INT for Channel 4. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_EN_CH4	Enable for Comparator and Logic for Channel 4. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 70: ADC CH4 CONFIG 2

Bits	**[7:5]**	**[4:3]**	**[2]**	**[1]**	**[0]**
Default	3'b000	2'b00	1'b0	1'b0	1'b0

Bits	**Mnemonic**	**Description**
[7:5]	ADC_COMP_SEL_CH4	Sets the gain of the comparator for Channel 4. • Program to 3'b001 for optimum performance
[4:3]	ADC_SUM_SEL_CH4	Sets the bandwidth of the summing amplifier for Channel 4. • Program to 2'b11 for optimum performance
[2]	ADC_USE_DITHER_EXT_CH4	Enable the external dither for Channel 4. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ADC_USE_DITHER_CH4	Enable the dither for Channel 4. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ADC_USE_STATE_CH4	Use state as logic output for Channel 4. • Default value is 0.

Register 71: ADC COMMON MODE CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'd0	1'd0	1'd0	1'd0	1'd0	1'd0	1'd0

Bits	Mnemonic	Description
[7]	ADC_CM_AMP_SEL_CH4	Set the common mode voltage of the summing amplifiers for Channel 4. • Set to 1'b1 for optimal operation
[6]	ADC_CM_INT_SEL_CH4	Set the common mode voltages of the integrators for Channel 4. • Set to 1'b1 for optimal operation
[5]	ADC_CM_AMP_SEL_CH3	Set the common mode voltage of the summing amplifiers for Channel 3. • Set to 1'b1 for optimal operation
[4]	ADC_CM_INT_SEL_CH3	Set the common mode voltages of the integrators for Channel 3. • Set to 1'b1 for optimal operation
[3]	ADC_CM_AMP_SEL_CH2	Set the common mode voltage of the summing amplifiers for Channel 2. • Set to 1'b1 for optimal operation
[2]	ADC_CM_INT_SEL_CH2	Set the common mode voltages of the integrators for Channel 2. • Set to 1'b1 for optimal operation
[1]	ADC_CM_AMP_SEL_CH1	Set the common mode voltage of the summing amplifiers for Channel 1. • Set to 1'b1 for optimal operation
[0]	ADC_CM_INT_SEL_CH1	Set the common mode voltages of the integrators for Channel 1. • Set to 1'b1 for optimal operation

Register 73-72: RESERVED

GPIO Registers

Register 74: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configure GPIO2 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO1_CFG	Configure GPIO1 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 75: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO3_CFG	Configure GPIO3 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 76: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configure GPIO6 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO5_CFG	Configure GPIO5 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 77: GPIO7/8 CONFIG

Bits	**[7:4]**	**[3:0]**
Default	4'd0	4'd0

Bits	**Mnemonic**	**Description**
[7:4]	GPIO8_CFG	Configure GPIO8 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO7_CFG	Configure GPIO7 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 78: GPIO9/10 CONFIG

Bits	**[7:4]**	**[3:0]**
Default	4'd0	4'd0

Bits	**Mnemonic**	**Description**
[7:4]	GPIO10_CFG	Configure GPIO10 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output
[3:0]	GPIO9_CFG	Configure GPIO9 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 79: GPIO11 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3:0]	GPIO11_CFG	Configure GPIO11 • 4'd0: Analog outputs off - shutdown (default) • 4'd1: Aux inputs - input • 4'd2: Aux outputs - output • 4'd3: Raw data stream - output • 4'd4: Ch1 peak flag interrupt - output • 4'd5: Ch2 peak flag interrupt - output • 4'd6: Ch3 peak flag interrupt - output • 4'd7: Ch4 peak flag interrupt - output • 4'd8: S/PDIF stream - output • 4'd9: PWM1 signal - output • 4'd10: PWM2 signal - output • 4'd11: PWM3 signal - output • 4'd12: CLK_IADC - output • 4'd13: CLK_ADC - output • 4'd14: Output 0 - output • 4'd15: Output 1 - output

Register 81-80: RESERVED

Register 83-82: INVERT GPIO

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'b00000	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	INVERT_GPIO11	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO11 output
[9]	INVERT_GPIO10	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO10 output
[8]	INVERT_GPIO9	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO9 output
[7]	INVERT_GPIO8	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO8 output
[6]	INVERT_GPIO7	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO7 output
[5]	INVERT_GPIO6	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO6 output
[4]	INVERT_GPIO5	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO5 output
[3]	INVERT_GPIO4	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO4 output
[2]	INVERT_GPIO3	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO3 output
[1]	INVERT_GPIO2	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO2 output
[0]	INVERT_GPIO1	• 1'b0: Non-invert (default) • 1'b1: Invert GPIO1 output

Register 85-84: GPIO WEAK ENABLE

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'b00000	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_WK_EN	• 1'b0: GPIO11 weak keeper disabled (default) • 1'b1: GPIO11 weak keeper enabled
[9]	GPIO10_WK_EN	• 1'b0: GPIO10 weak keeper disabled (default) • 1'b1: GPIO10 weak keeper enabled
[8]	GPIO9_WK_EN	• 1'b0: GPIO9 weak keeper disabled (default) • 1'b1: GPIO9 weak keeper enabled
[7]	GPIO8_WK_EN	• 1'b0: GPIO8 weak keeper disabled (default) • 1'b1: GPIO8 weak keeper enabled
[6]	GPIO7_WK_EN	• 1'b0: GPIO7 weak keeper disabled (default) • 1'b1: GPIO7 weak keeper enabled
[5]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[4]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 87-86: GPIO IE

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'b00000	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_IE	• 1'b0: GPIO11 input disabled (default) • 1'b1: GPIO11 input enabled
[9]	GPIO10_IE	• 1'b0: GPIO10 input disabled (default) • 1'b1: GPIO10 input enabled
[8]	GPIO9_IE	• 1'b0: GPIO9 input disabled (default) • 1'b1: GPIO9 input enabled
[7]	GPIO8_IE	• 1'b0: GPIO8 input disabled (default) • 1'b1: GPIO8 input enabled
[6]	GPIO7_IE	• 1'b0: GPIO7 input disabled (default) • 1'b1: GPIO7 input enabled
[5]	GPIO6_IE	• 1'b0: GPIO6 input disabled (default) • 1'b1: GPIO6 input enabled
[4]	GPIO5_IE	• 1'b0: GPIO5 input disabled (default) • 1'b1: GPIO5 input enabled
[3]	GPIO4_IE	• 1'b0: GPIO4 input disabled (default) • 1'b1: GPIO4 input enabled
[2]	GPIO3_IE	• 1'b0: GPIO3 input disabled (default) • 1'b1: GPIO3 input enabled
[1]	GPIO2_IE	• 1'b0: GPIO2 input disabled (default) • 1'b1: GPIO2 input enabled
[0]	GPIO1_IE	• 1'b0: GPIO1 input disabled (default) • 1'b1: GPIO1 input enabled

Register 89-88: GPIO OE

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'b00000	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_OE	• 1'b0: Tristate GPIO11 output (default) • 1'b1: GPIO11 output enabled
[9]	GPIO10_OE	• 1'b0: Tristate GPIO10 output (default) • 1'b1: GPIO10 output enabled
[8]	GPIO9_OE	• 1'b0: Tristate GPIO9 output (default) • 1'b1: GPIO9 output enabled
[7]	GPIO8_OE	• 1'b0: Tristate GPIO8 output (default) • 1'b1: GPIO8 output enabled
[6]	GPIO7_OE	• 1'b0: Tristate GPIO7 output (default) • 1'b1: GPIO7 output enabled
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 output (default) • 1'b1: GPIO6 output enabled
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 output (default) • 1'b1: GPIO5 output enabled
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 output (default) • 1'b1: GPIO4 output enabled
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 output (default) • 1'b1: GPIO3 output enabled
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 output (default) • 1'b1: GPIO2 output enabled
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 output (default) • 1'b1: GPIO1 output enabled

Register 91-90: GPIO READ

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	5'b00000	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_READ	• 1'b0: GPIO11 readback disabled (default) • 1'b1: Allows readback of GPIO11 input
[9]	GPIO10_READ	• 1'b0: GPIO10 readback disabled (default) • 1'b1: Allows readback of GPIO10 input
[8]	GPIO9_READ	• 1'b0: GPIO9 readback disabled (default) • 1'b1: Allows readback of GPIO9 input
[7]	GPIO8_READ	• 1'b0: GPIO8 readback disabled (default) • 1'b1: Allows readback of GPIO8 input
[6]	GPIO7_READ	• 1'b0: GPIO7 readback disabled (default) • 1'b1: Allows readback of GPIO7 input
[5]	GPIO6_READ	• 1'b0: GPIO6 readback disabled (default) • 1'b1: Allows readback of GPIO6 input
[4]	GPIO5_READ	• 1'b0: GPIO5 readback disabled (default) • 1'b1: Allows readback of GPIO5 input
[3]	GPIO4_READ	• 1'b0: GPIO4 readback disabled (default) • 1'b1: Allows readback of GPIO4 input
[2]	GPIO3_READ	• 1'b0: GPIO3 readback disabled (default) • 1'b1: Allows readback of GPIO3 input
[1]	GPIO2_READ	• 1'b0: GPIO2 readback disabled (default) • 1'b1: Allows readback of GPIO2 input
[0]	GPIO1_READ	• 1'b0: GPIO1 readback disabled (default) • 1'b1: Allows readback of GPIO1 input

Register 92: PWM1 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 94-93: PWM1 FREQUENCY

Bits	**[15:0]**
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM1\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM1\_COUNT}}{\text{PWM1\_FREQ} + 1} \cdot 100$

Register 95: PWM2 COUNT

Bits	**[7:0]**
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 97-96: PWM2 FREQUENCY

Bits	**[15:0]**
Default	16'h0000

Bits	**Mnemonic**	**Description**
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM2\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM2\_COUNT}}{\text{PWM2\_FREQ} + 1} \cdot 100$

Register 98: PWM3 COUNT

Bits	**[7:0]**
Default	8'h00

Bits	**Mnemonic**	**Description**
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 100-99: PWM3 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM3\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM3\_COUNT}}{\text{PWM3\_FREQ} + 1} \cdot 100$

ADC CH1 Registers

Register 101: ADC CH1 DATAPATH CONTROL

Bits	[7]	[6]	[5:3]	[2]	[1]	[0]
Default	1'b0	1'b0	3'b000	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC1_BYPASS_FIR2X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_2x
[6]	ADC1_BYPASS_FIR4X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_4x
[5:3]	RESERVED	N/A
[2]	ADC1_ENABLE_DC_BLOCKING	Enables DC blocking path. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	RESERVED	N/A
[0]	ADC1_NEG_SEL	Inverts data input from analog ADC 1. • 1'b0: No inversion (default) • 1'b1: Inverts input data

Register 102: ADC CH1 THD COMP CONFIG

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	ADC1_CORRECTION_ADDR	Selects the address when writing the THD compensation RAM.
[1]	ADC1_CORRECTION_WE	Enables writing to the THD compensation RAM. • 1'b0: Writing disabled (default) • 1'b1: Writing enabled
[0]	ADC1_ENABLE_THD_COMP	Enables the THD compensation on ADC CH1. • 1'b0: Disabled and bypassed (default) • 1'b1: Enabled

Register 104-103: ADC CH1 THD COMP DATA

Bits	**[15:0]**
Default	16'h0000

Bits	**Mnemonic**	**Description**
[15:0]	ADC1_CORRECTION_DATA	A 16 bits THD corrected value that will be written to the address of the THD compensation RAM. Maximum -42dB (16'hFFFF).

Register 105: ADC CH1 PEAK DETECTOR CONFIG

Bits	**[7]**	**[6:2]**	**[1]**	**[0]**
Default	1'b0	5'd10	1'b0	1'b0

Bits	**Mnemonic**	**Description**
[7]	ADC1_LOCK_PEAK	Locks the stored value of the peak detector for reading back. • 1'b0: Stored value is allowed to update (default) • 1'b1: Stored value is locked
[6:2]	ADC1_PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved
[1]	RESERVED	N/A
[0]	ADC1_ENABLE_PEAK_DETECT	Enables the ADC signal peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 106: ADC CH1 PEAK DETECTOR LEVEL

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	ADC1_PEAK_THRESH	Threshold value to trigger the PEAK_FLAG in the CH1 peak detector. Triggers if the input signal > ADC1_PEAK_THRESH. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log 10 \frac{\text{ADC1\_PEAK\_THRESH}}{2^8 - 1}$

Register 108-107: ADC CH1 DC OFFSET

Bits	[15:0]
Default	16'd0

Bits	Mnemonic	Description
[15:0]	ADC1_DC_OFFSET	Signed ADC CH1 DC offset coefficient. Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-120dB). Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-120dB). 16'h0000 corresponds to zero offset. $\text{offset [dB]} = 20 \cdot \log 10 \frac{\text{ADC1\_DC\_OFFSET}}{(2^{15} - 1) \cdot 2^5}$

Register 110-109: ADC CH1 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	ADC1_VOLUME	Signed value for the next desired ADC CH1 volume coefficient. • 16'h0001: -90dB • 16'h7FFF: 0dB (default) • 16'h0000: Mute Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume. $\text{volume [dB]} = 20 \cdot \log 10 \frac{\text{ADC1\_VOLUME}}{2^{15} - 1}$

Register 111: ADC CH1 VOLUME RATE

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ADC1_VOLUME_RATE	Value by which the old coefficient value is incremented/decremented to reach the new coefficient. • 8'h00: Instant change (default) • 8'h01: Slowest change • 8'hFF: Fastest change

Register 112: ADC CH1 GAIN

Bits	[7:2]	[1:0]
Default	6'd36	2'd0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1:0]	ADC1_DATA_GAIN	ADC data gain. • 2'd0: +0dB • 2'd1: +6dB • 2'd2: +12dB • 2'd3: +18dB

Register 113: ADC CH1 PROG FILTER

Bits	[7:5]	[4:2]	[1]	[0]
Default	3'd4	3'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:2]	ADC1_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing fast roll-off • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[1]	ADC1_PROG_COEFF_WRITE_EN	Enables writing to the programmable coefficient RAM. • 1'b0: Disables write signal to the coefficient RAM (default) • 1'b1: Enables write signal to the coefficient RAM.
[0]	ADC1_PROG_COEFF_EN	Enables the custom decimation filter coefficients. • 1'b0: Uses a built-in filter selected by FILTER_SHAPE (default) • 1'b1: Uses the coefficients programmed via ADC1_PROG_COEFF_IN

Register 114: ADC CH1 PROG FILTER COEFF ADDR

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	ADC1_PROG_COEFF_STAGE	Selects which stage of the filter to write. • 1'b0: Selects stage 1 of the decimation filter DFir_4x (default) • 1'b1: Selects stage 2 of the decimation filter DFir_2x
[6:0]	ADC1_PROG_COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the decimation filter.

Register 117-115: ADC CH1 PROG FILTER COEFF

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	ADC1_PROG_COEFF_IN	A 24-bit signed filter coefficient that will be written to the address in ADC1_PROG_COEFF_ADDR.

ADC CH2 Registers

Register 118: ADC CH2 DATAPATH CONTROL

Bits	[7]	[6]	[5:3]	[2]	[1]	[0]
Default	1'b0	1'b0	3'b000	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC2_BYPASS_FIR2X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_2x
[6]	ADC2_BYPASS_FIR4X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_4x
[5:3]	RESERVED	N/A
[2]	ADC2_ENABLE_DC_BLOCKING	Enables DC blocking path. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	RESERVED	N/A
[0]	ADC2_NEG_SEL	Inverts data input from analog ADC 2. • 1'b0: No inversion (default) • 1'b1: Inverts input data

Register 119: ADC CH2 THD COMP CONFIG

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	ADC2_CORRECTION_ADDR	Selects the address when writing the THD compensation RAM.
[1]	ADC2_CORRECTION_WE	Enables writing to the THD compensation RAM. • 1'b0: Writing disabled (default) • 1'b1: Writing enabled
[0]	ADC2_ENABLE_THD_COMP	Enables the THD compensation on ADC CH2. • 1'b0: Disabled and bypassed (default) • 1'b1: Enabled

Register 121-120: ADC CH2 THD COMP DATA

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	ADC2_CORRECTION_DATA	A 16 bits THD corrected value that will be written to the address of the THD compensation RAM. Maximum -42dB (16'hFFFF).

Register 122: ADC CH2 PEAK DETECTOR CONFIG

Bits	[7]	[6:2]	[1]	[0]
Default	1'b0	5'd10	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC2_LOCK_PEAK	Locks the stored value of the peak detector for reading back. • 1'b0: Stored value is allowed to update (default) • 1'b1: Stored value is locked
[6:2]	ADC2_PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved
[1]	RESERVED	N/A
[0]	ADC2_ENABLE_PEAK_DETECT	Enables the ADC signal peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 123: ADC CH2 PEAK DETECTOR THRESHOLD

Bits	**[7:0]**
Default	8'hFF

Bits	**Mnemonic**	**Description**
[7:0]	ADC2_PEAK_THRESH	Threshold value to trigger the PEAK_FLAG in the CH2 peak detector. Triggers if the input signal > ADC2_PEAK_THRESH. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log 10 \frac{\text{ADC2\_PEAK\_THRESH}}{2^8 - 1}$

Register 125-124: ADC CH2 DC OFFSET

Bits	**[15:0]**
Default	16'd0

Bits	**Mnemonic**	**Description**
[15:0]	ADC2_DC_OFFSET	Signed ADC CH2 DC offset coefficient. Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-120dB). Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-120dB). 16'h0000 corresponds to zero offset. $\text{offset [dB]} = 20 \cdot \log 10 \frac{\text{ADC2\_DC\_OFFSET}}{(2^{15} - 1) \cdot 2^5}$

Register 127-126: ADC CH2 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	ADC2_VOLUME	Signed value for the next desired ADC CH2 volume coefficient. • 16'h0001: -90dB • 16'h7FFF: 0dB (default) • 16'h0000: Mute Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume. $\text{volume [dB]} = 20 \cdot \log10 \frac{\text{ADC2\_VOLUME}}{2^{15}-1}$

Register 128: ADC CH2 VOLUME RATE

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ADC2_VOLUME_RATE	Value by which the old coefficient value is incremented/decremented to reach the new coefficient. • 8'h00: Instant change (default) • 8'h01: Slowest change • 8'hFF: Fastest change

Register 129: ADC CH2 GAIN

Bits	[7:2]	[1:0]
Default	6'd36	2'd0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1:0]	ADC2_DATA_GAIN	ADC data gain. • 2'd0: +0dB • 2'd1: +6dB • 2'd2: +12dB • 2'd3: +18dB

Register 130: ADC CH2 PROG FILTER

Bits	[7:5]	[4:2]	[1]	[0]
Default	3'd4	3'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:2]	ADC2_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing fast roll-off • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[1]	ADC2_PROG_COEFF_WRITE_EN	Enables writing to the programmable coefficient RAM. • 1'b0: Disables write signal to the coefficient RAM (default) • 1'b1: Enables write signal to the coefficient RAM.
[0]	ADC2_PROG_COEFF_EN	Enables the custom decimation filter coefficients. • 1'b0: Uses a built-in filter selected by FILTER_SHAPE (default) • 1'b1: Uses the coefficients programmed via ADC2_PROG_COEFF_IN

Register 131: ADC CH2 PROG FILTER COEFF ADDR

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	ADC2_PROG_COEFF_STAGE	Selects which stage of the filter to write. • 1'b0: Selects stage 1 of the decimation filter DFir_4x (default) • 1'b1: Selects stage 2 of the decimation filter DFir_2x
[6:0]	ADC2_PROG_COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the decimation filter.

Register 134-132: ADC CH2 PROG FILTER COEFF

Bits	**[23:0]**
Default	24'd0

Bits	Mnemonic	Description
[23:0]	ADC2_PROG_COEFF_IN	A 24-bit signed filter coefficient that will be written to the address in ADC2_PROG_COEFF_ADDR.

ADC CH3 Registers

Register 135: ADC CH3 DATAPATH CONTROL

Bits	[7]	[6]	[5:3]	[2]	[1]	[0]
Default	1'b0	1'b0	3'b000	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC3_BYPASS_FIR2X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_2x
[6]	ADC3_BYPASS_FIR4X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_4x
[5:3]	RESERVED	N/A
[2]	ADC3_ENABLE_DC_BLOCKING	Enables DC blocking path. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	RESERVED	N/A
[0]	ADC3_NEG_SEL	Inverts data input from analog ADC 3. • 1'b0: No inversion (default) • 1'b1: Inverts input data

Register 136: ADC CH3 THD COMP CONFIG

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	ADC3_CORRECTION_ADDR	Selects the address when writing the THD compensation RAM.
[1]	ADC3_CORRECTION_WE	Enables writing to the THD compensation RAM. • 1'b0: Writing disabled (default) • 1'b1: Writing enabled
[0]	ADC3_ENABLE_THD_COMP	Enables the THD compensation on ADC CH3. • 1'b0: Disabled and bypassed (default) • 1'b1: Enabled

Register 138-137: ADC CH3 THD COMP DATA

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	ADC3_CORRECTION_DATA	A 16 bits THD corrected value that will be written to the address of the THD compensation RAM. Maximum -42dB (16'hFFFF).

Register 139: ADC CH3 PEAK DETECTOR CONFIG

Bits	[7]	[6:2]	[1]	[0]
Default	1'b0	5'd10	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC3_LOCK_PEAK	Locks the stored value of the peak detector for reading back. • 1'b0: Stored value is allowed to update (default) • 1'b1: Stored value is locked
[6:2]	ADC3_PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved
[1]	RESERVED	N/A
[0]	ADC3_ENABLE_PEAK_DETECT	Enables the ADC signal peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 140: ADC CH3 PEAK DETECTOR THRESHOLD

Bits	**[7:0]**
Default	8'hFF

Bits	**Mnemonic**	**Description**
[7:0]	ADC3_PEAK_THRESH	Threshold value to trigger the PEAK_FLAG in the CH3 peak detector. Triggers if the input signal > ADC3_PEAK_THRESH. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log 10 \frac{\text{ADC3\_PEAK\_THRESH}}{2^8 - 1}$

Register 142-141: ADC CH3 DC OFFSET

Bits	**[15:0]**
Default	16'h0000

Bits	**Mnemonic**	**Description**
[15:0]	ADC3_DC_OFFSET	Signed ADC CH3 DC offset coefficient. Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-120dB). Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-120dB). 16'h0000 corresponds to zero offset. $\text{offset [dB]} = 20 \cdot \log 10 \frac{\text{ADC3\_DC\_OFFSET}}{(2^{15} - 1) \cdot 2^5}$

Register 144-143: ADC CH3 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	ADC3_VOLUME	Signed value for the next desired ADC CH3 volume coefficient. • 16'h0001: -90dB • 16'h7FFF: 0dB (default) • 16'h0000: Mute Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume. $\text{volume [dB]} = 20 \cdot \log 10 \frac{\text{ADC3\_VOLUME}}{2^{15} - 1}$

Register 145: ADC CH3 VOLUME RATE

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ADC3_VOLUME_RATE	Value by which the old coefficient value is incremented/decremented to reach the new coefficient. • 8'h00: Instant change (default) • 8'h01: Slowest change • 8'hFF: Fastest change

Register 146: ADC CH3 GAIN

Bits	[7:2]	[1:0]
Default	6'd36	2'd0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1:0]	ADC3_DATA_GAIN	ADC data gain. • 2'd0: +0dB • 2'd1: +6dB • 2'd2: +12dB • 2'd3: +18dB

Register 147: ADC CH3 PROG FILTER

Bits	[7:5]	[4:2]	[1]	[0]
Default	3'd4	3'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:2]	ADC3_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing fast roll-off • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[1]	ADC3_PROG_COEFF_WRITE_EN	Enables writing to the programmable coefficient RAM. • 1'b0: Disables write signal to the coefficient RAM (default) • 1'b1: Enables write signal to the coefficient RAM.
[0]	ADC3_PROG_COEFF_EN	Enables the custom decimation filter coefficients. • 1'b0: Uses a built-in filter selected by FILTER_SHAPE (default) • 1'b1: Uses the coefficients programmed via ADC3_PROG_COEFF_IN

Register 148: ADC CH3 PROG FILTER COEFF ADDR

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	ADC3_PROG_COEFF_STAGE	Selects which stage of the filter to write. • 1'b0: Selects stage 1 of the decimation filter DFir_4x (default) • 1'b1: Selects stage 2 of the decimation filter DFir_2x
[6:0]	ADC3_PROG_COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the decimation filter.

Register 151-149: ADC CH3 PROG FILTER COEFF

Bits	**[23:0]**
Default	24'd0

Bits	**Mnemonic**	**Description**
[23:0]	ADC3_PROG_COEFF_IN	A 24-bit signed filter coefficient that will be written to the address in ADC3_PROG_COEFF_ADDR.

ADC CH4 Registers

Register 152: ADC CH4 DATAPATH CONTROL

Bits	[7]	[6]	[5:3]	[2]	[1]	[0]
Default	1'b0	1'b0	3'b000	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC4_BYPASS_FIR2X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_2x
[6]	ADC4_BYPASS_FIR4X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_4x
[5:3]	RESERVED	N/A
[2]	ADC4_ENABLE_DC_BLOCKING	Enables DC blocking path. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	RESERVED	N/A
[0]	ADC4_NEG_SEL	Inverts data input from analog ADC 4. • 1'b0: No inversion (default) • 1'b1: Inverts input data

Register 153: ADC CH4 THD COMP CONFIG

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	ADC4_CORRECTION_ADDR	Selects the address when writing the THD compensation RAM.
[1]	ADC4_CORRECTION_WE	Enables writing to the THD compensation RAM. • 1'b0: Writing disabled (default) • 1'b1: Writing enabled
[0]	ADC4_ENABLE_THD_COMP	Enables the THD compensation on ADC CH4. • 1'b0: Disabled and bypassed (default) • 1'b1: Enabled

Register 155-154: ADC CH4 THD COMP DATA

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	ADC4_CORRECTION_DATA	A 16 bits THD corrected value that will be written to the address of the THD compensation RAM. Maximum -42dB (16'hFFFF).

Register 156: ADC CH4 PEAK DETECTOR CONFIG

Bits	[7]	[6:2]	[1]	[0]
Default	1'b0	5'd10	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ADC4_LOCK_PEAK	Locks the stored value of the peak detector for reading back. • 1'b0: Stored value is allowed to update (default) • 1'b1: Stored value is locked
[6:2]	ADC4_PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved
[1]	RESERVED	N/A
[0]	ADC4_ENABLE_PEAK_DETECT	Enables the ADC CH4 signal peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 157: ADC CH4 PEAK DETECTOR THRESHOLD

Bits	**[7:0]**
Default	8'hFF

Bits	**Mnemonic**	**Description**
[7:0]	ADC4_PEAK_THRESH	Threshold value to trigger the PEAK_FLAG in the CH4 peak detector. Triggers if the input signal > ADC4_PEAK_THRESH. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log 10 \frac{\text{ADC4\_PEAK\_THRESH}}{2^8 - 1}$

Register 159-158: ADC CH4 DC OFFSET

Bits	**[15:0]**
Default	16'h0000

Bits	**Mnemonic**	**Description**
[15:0]	ADC4_DC_OFFSET	Signed ADC CH4 DC offset coefficient. Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-120dB). Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-120dB). 16'h0000 corresponds to zero offset. $\text{offset [dB]} = 20 \cdot \log 10 \frac{\text{ADC4\_DC\_OFFSET}}{(2^{15} - 1) \cdot 2^5}$

Register 161-160: ADC CH4 VOLUME

Bits	[15:0]
Default	16'h7FFF

Bits	Mnemonic	Description
[15:0]	ADC4_VOLUME	Signed value for the next desired ADC CH4 volume coefficient. • 16'h0001: -90dB • 16'h7FFF: 0dB (default) • 16'h0000: Mute Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume. $\text{volume [dB]} = 20 \cdot \log 10 \frac{\text{ADC4\_VOLUME}}{2^{15} - 1}$

Register 162: ADC CH4 VOLUME RATE

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	ADC4_VOLUME_RATE	Value by which the old coefficient value is incremented/decremented to reach the new coefficient. • 8'h00: Instant change (default) • 8'h01: Slowest change • 8'hFF: Fastest change

Register 163: ADC CH4 GAIN

Bits	[7:2]	[1:0]
Default	6'd36	2'd0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1:0]	ADC4_DATA_GAIN	ADC data gain. • 2'd0: +0dB • 2'd1: +6dB • 2'd2: +12dB • 2'd3: +18dB

Register 164: ADC CH4 PROG FILTER

Bits	[7:5]	[4:2]	[1]	[0]
Default	3'd4	3'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:2]	ADC4_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase apodizing fast roll-off • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[1]	ADC4_PROG_COEFF_WRITE_EN	Enables writing to the programmable coefficient RAM. • 1'b0: Disables write signal to the coefficient RAM (default) • 1'b1: Enables write signal to the coefficient RAM.
[0]	ADC4_PROG_COEFF_EN	Enables the custom decimation filter coefficients. • 1'b0: Uses a built-in filter selected by FILTER_SHAPE (default) • 1'b1: Uses the coefficients programmed via ADC4_PROG_COEFF_IN

Register 165: ADC CH4 PROG FILTER COEFF ADDR

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	ADC4_PROG_COEFF_STAGE	Selects which stage of the filter to write. • 1'b0: Selects stage 1 of the decimation filter DFir_4x (default) • 1'b1: Selects stage 2 of the decimation filter DFir_2x
[6:0]	ADC4_PROG_COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the decimation filter.

Register 168-166: ADC CH4 PROG FILTER COEFF

Bits	**[23:0]**
Default	24'd0

Bits	**Mnemonic**	**Description**
[23:0]	ADC4_PROG_COEFF_IN	A 24-bit signed filter coefficient that will be written to the address in ADC4_PROG_COEFF_ADDR.

Synchronous Slave Interface Registers

Register 192: SOFT RESET

Bits	[7]	[6:0]
Default	1'b0	7'b0000000

Bits	Mnemonic	Description
[7]	AO_SOFT_RESET	Performs soft reset to digital core except for the synchronous registers.
[6:0]	RESERVED	N/A

Register 193: CLK SELECT

Bits	[7:3]	[2:1]	[0]
Default	5'b00000	2'd0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2:1]	SEL_SYSCLK_IN	Selects digital core and ADC clock source when EN_ANA_CLKIN is set. • 2'd0: XTAL (default) • 2'd1: MCLK • 2'd2: ACLK • 2'd3: Reserved
[0]	EN_ANA_CLKIN	Enables clock outputs to the digital core and ADC. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 194: ADC CLOCK DIVIDE

Bits	[7:2]	[1:0]
Default	6'b000000	2'd0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1:0]	SEL_CLK_DIV	Sets ADC clock rate: • 2'd0: full-rate (Divide by 1) (default) • 2'd1: 1/2 rate (Divide by 2) • 2'd2: 1/4 rate (Divide by 4) • 2'd3: 1/8 rate (Divide by 8)

Register 203-195: RESERVED

Readback Registers

Register 224: READ SYSTEM REGISTER 0

Bits	[7:4]	[3]	[2]	[1]	[0]
Default		-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	MODE	Readback MODE pin.
[2]	ADDR2	Readback ADDR2 pin.
[1]	ADDR1	Readback ADDR1 pin.
[0]	RESERVED	N/A

Register 225: CHIP ID

Bits	[7:0]
Default	8'h83

Bits	Mnemonic	Description
[7:0]	CHIP_ID	• ES9842PRO: 0x83

Register 228-226: RESERVED

Register 229: PEAK FLAG

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PEAK_FLAG_CH4	ADC CH4 peak detector flag
[2]	PEAK_FLAG_CH3	ADC CH3 peak detector flag
[1]	PEAK_FLAG_CH2	ADC CH2 peak detector flag
[0]	PEAK_FLAG_CH1	ADC CH1 peak detector flag

Register 230: RESERVED

Register 231: READ SYSTEM REGISTER 5

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	-	-	-	-	-

Bits	Mnemonic	Description
[7]	ASP2_INIT_DONE	ASP2 initialize is done
[6]	ASP1_INIT_DONE	ASP1 initialize is done
[5]	RESERVED	N/A
[4]	TDM_VALID	TDM valid flag
[3:0]	RESERVED	N/A

Register 233-232: GPIO READBACK REGISTERS

Bits	[15:11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default		-	-	-	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[15:11]	RESERVED	N/A
[10]	GPIO11_READBACK	GPIO 11 Readback
[9]	GPIO10_READBACK	GPIO 10 Readback
[8]	GPIO9_READBACK	GPIO 9 Readback
[7]	GPIO8_READBACK	GPIO 8 Readback
[6]	GPIO7_READBACK	GPIO 7 Readback
[5]	GPIO6_READBACK	GPIO 6 Readback
[4]	GPIO5_READBACK	GPIO 5 Readback
[3]	GPIO4_READBACK	GPIO 4 Readback
[2]	GPIO3_READBACK	GPIO 3 Readback
[1]	GPIO2_READBACK	GPIO 2 Readback
[0]	GPIO1_READBACK	GPIO 1 Readback

Register 236-234: ADC CH1 PROG COEFF OUT

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	ADC1_PROG_COEFF_OUT	Programmable FIR coefficient readback.

Register 238-237: ADC CH1 PEAK

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	ADC1_PEAK	Detected peak value readback

Register 241-239: ADC CH2 PROG COEFF OUT

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	ADC2_PROG_COEFF_OUT	Programmable FIR coefficient readback.

Register 243-242: ADC CH2 PEAK

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	ADC2_PEAK	Detected peak value readback

Register 246-244: ADC CH3 PROG COEFF OUT

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	ADC3_PROG_COEFF_OUT	Programmable FIR coefficient readback.

Register 248-247: ADC CH3 PEAK

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	ADC3_PEAK	Detected peak value readback

Register 251-249: ADC CH4 PROG COEFF OUT

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	ADC4_PROG_COEFF_OUT	Programmable FIR coefficient readback.

Register 253-252: ADC CH4 PEAK

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	ADC4_PEAK	Detected peak value readback

ES9842 PRO Reference Schematic[1]

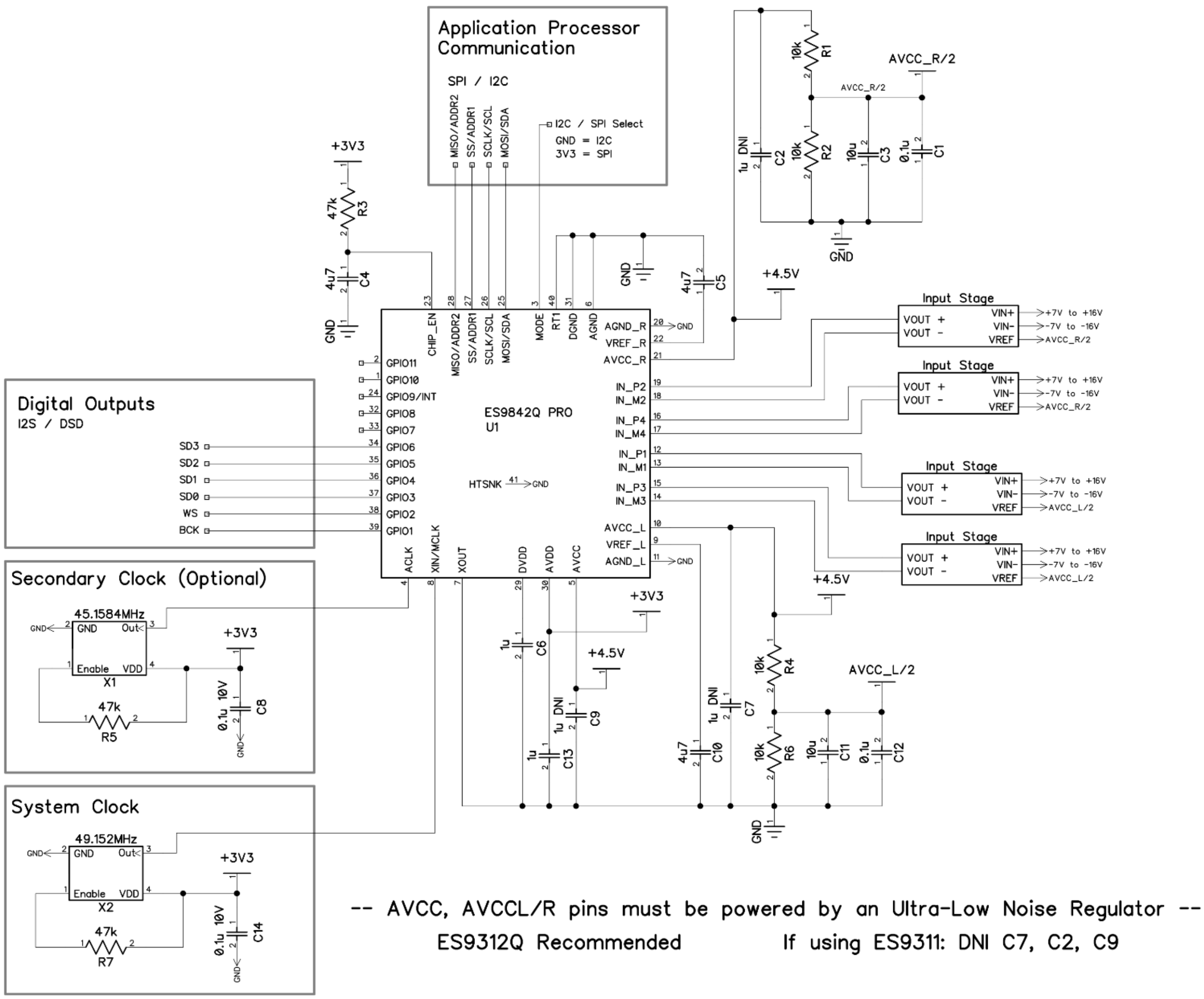


Figure 28 - ES9842PRO Reference Schematic for Normal Operation

Schematic subject to change

Note: An Ultra-Low Noise regulator is recommended for AVCC, AVCC_L and AVCC_R

[1] Pin 41 QFN Package Pad (EPAD) should be connected to DGND

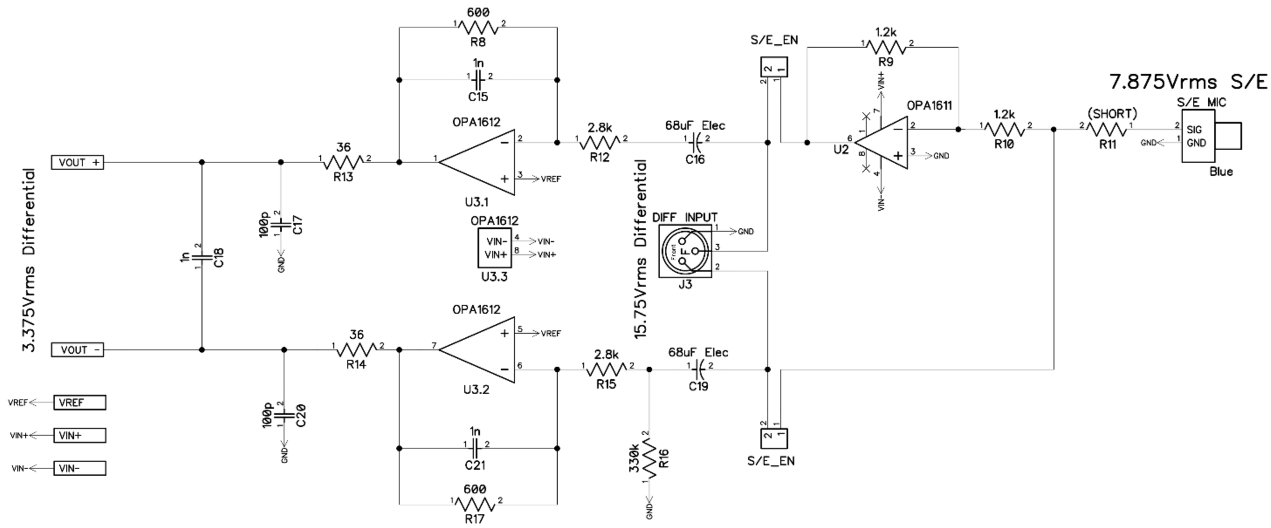


Figure 29 - Reference Schematic ADC Input Stage for Single Ended (S/E) and Differential Input

***Note: All resistors are thin-film, and all caps are COG/NPO unless otherwise specified.**

Note: OPA1612 can be replaced with an OPA1602 if required.

This diagram shows the configuration of the ES9312Q with an output of 3.3V and 4.5V respectively.

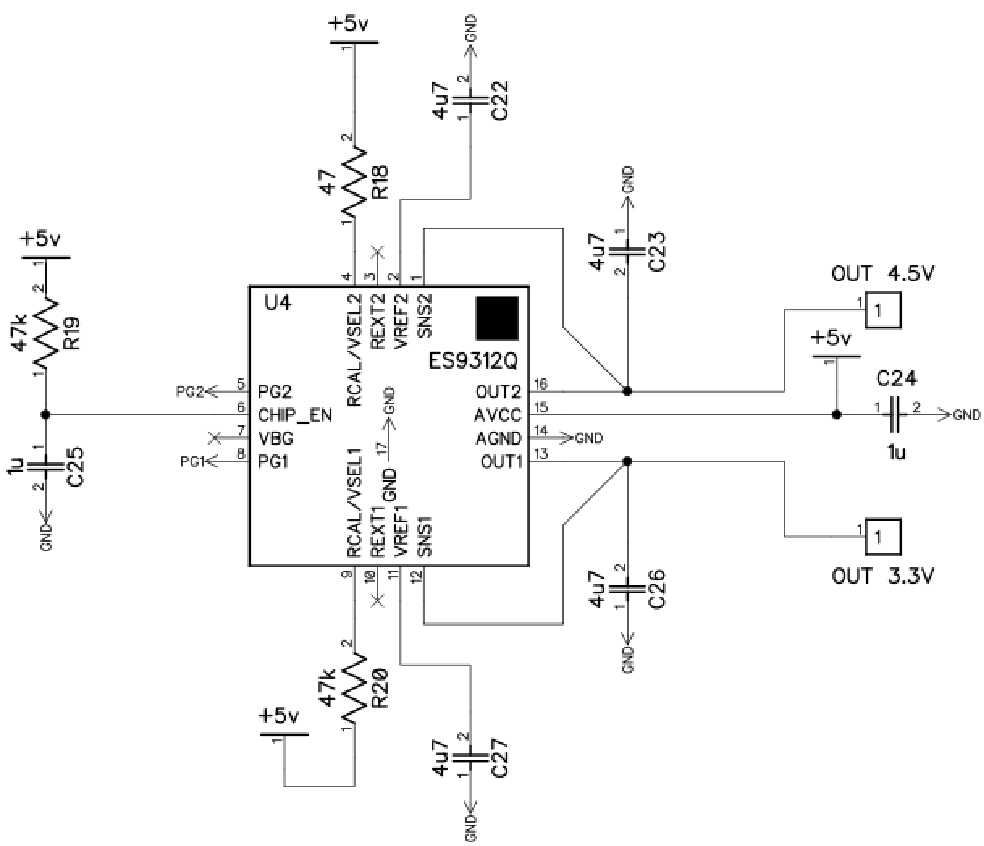
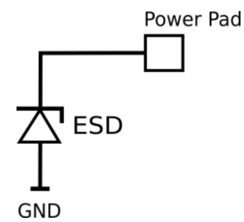
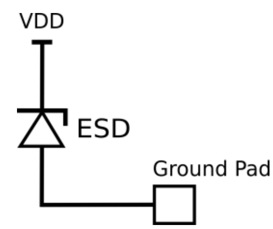
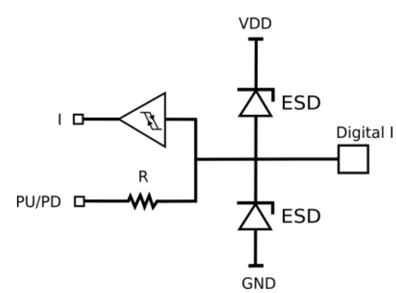


Figure 30 - ES9312Q Reference Voltage Regulator Schematic

Internal Pad Circuitry

Pin Name	Type	Pin	Equivalent Circuit
AVCC AVCC_L AVCC_R DVDD AVDD	Power (Positive)	5 10 21 29 30	
AGND AGND_L AGND_R DGND	Ground	6 11 20 31	
CHIP_EN	Reset	23	

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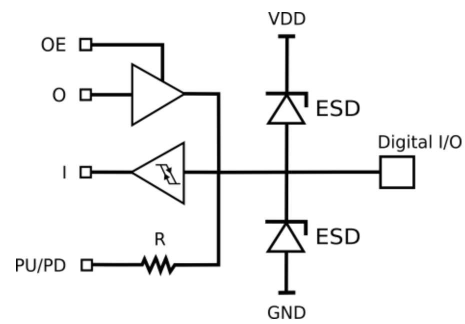
<tr><td>GPIO10</td><td rowspan="18">Digital I/O</td><td>1</td><td rowspan="18">
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<tr><td>MODE</td><td>3</td></tr>
<tr><td>ACLK</td><td>4</td></tr>
<tr><td>GPIO9/INT</td><td>24</td></tr>
<tr><td>MOSI/SDA</td><td>25</td></tr>
<tr><td>SCLK/SCL</td><td>26</td></tr>
<tr><td>SS/ADDR1</td><td>27</td></tr>
<tr><td>MISO/ADDR2</td><td>28</td></tr>
<tr><td>GPIO8</td><td>32</td></tr>
<tr><td>GPIO7</td><td>33</td></tr>
<tr><td>GPIO6</td><td>34</td></tr>
<tr><td>GPIO5</td><td>35</td></tr>
<tr><td>GPIO4</td><td>36</td></tr>
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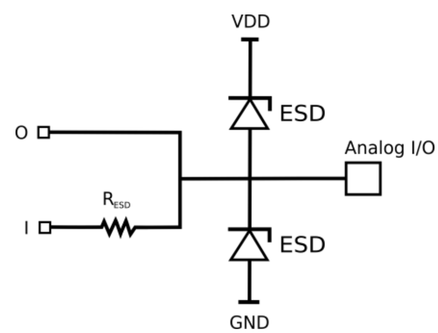
<tr><td>XOUT</td><td rowspan="12">Analog IO</td><td>7</td><td rowspan="12">
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<tr><td>IN_P2</td><td>19</td></tr>
<tr><td>VREF_R</td><td>22</td></tr>
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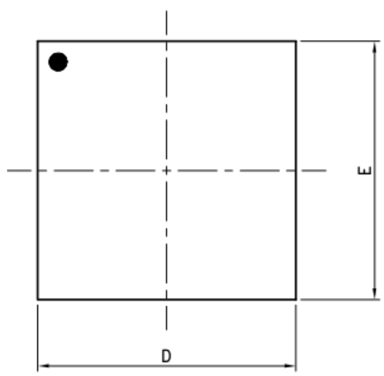
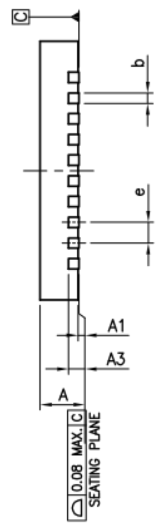
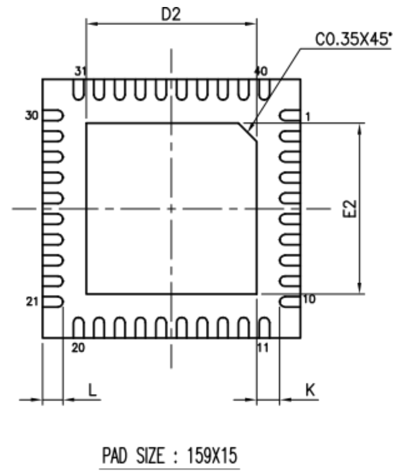
Table 35 - Internal Pad Circuitry

40 QFN Package Dimensions







PACKAGE TYPE

JEDEC OUTLINE	MO−220		
PKG CODΓ	WQFN(X540)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
K	0.20	—	—

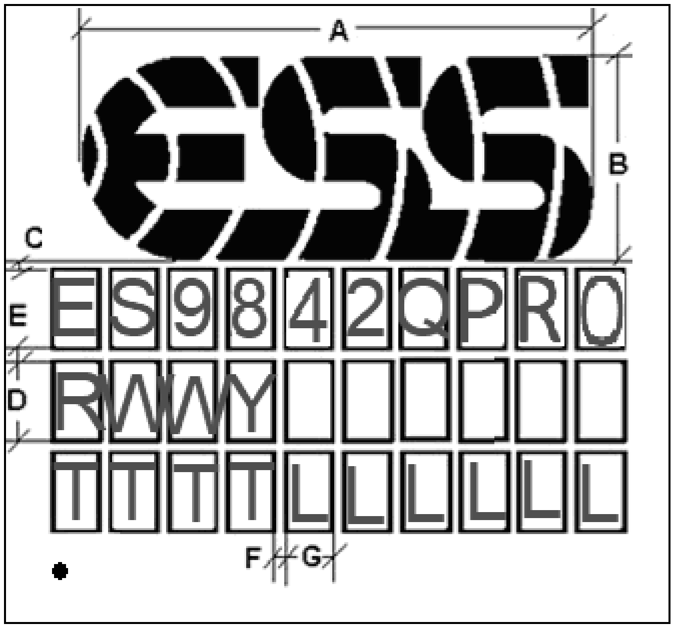
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
159X15* MIL	3.74	3.79	3.84	3.74	3.79	3.84	0.25	0.30	0.35

Figure 31 - 40 QFN Package Dimensions

40 QFN Top View Marking



	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 5mm x 5mm	4.0	1.6	0.2	0.4	0.2	0.1	0.3

T	Tracking number
W	Work week
Y	Last digit of year
L	Lot number
R	Silicon Revision

Marking is subject to change. This drawing is not to scale.

Figure 32 - ES9842 PRO QFN Marking

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

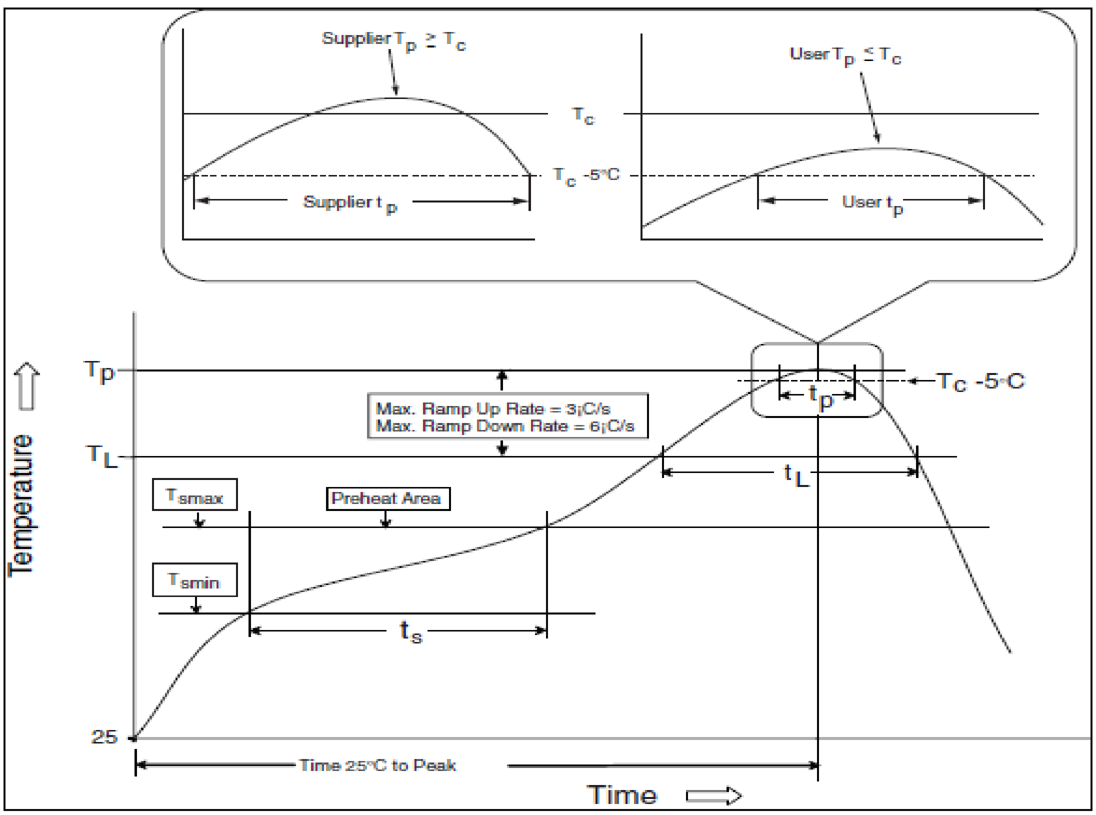


Figure 33 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	**Pb-Free Assembly**
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure 33	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 36 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 37 - RPC-2 Pb-Free Process

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9842QPRO	SABRE 32-bit 4 Channel ADC with Built in Programmable Filters, ASP, and Multiple Output Formats	5mm x 5mm 40 QFN

Table 38 - Ordering Information

Addendum

The following subsections outline the recommended configuration for Common I²S and TDM modes in s2m format.

I²S Master

FS=48kHz, 4 Channel, MCLK=49.152MHz

```
w 0x48 193 0x01;    //SEL_SYSCLK_IN = 00 (XTAL), EN_ANA_CLKIN = 1
//w 0x48 193 0x05;  //SEL_SYSCLK_IN = 10 (ACLK), EN_ANA_CLKIN = 1
w 0x48 194 0x01;    //SEL_CLK_DIV = 1/2 (for 49.152/45.1584MHz, this sets ADC clock rate, must be
22 or 24MHz)

w 0x40 0 0x00;      //OUTPUT_SEL = 00 (I²S)
w 0x40 1 0xFF;      //ENABLE_ADC_CH and ENABLE_DATA_IN_CH
w 0x40 2 0x07;      //SELECT_ADC_NUM = 7 for 48k/44.1k, 3 for 96k, 1 for 192k
w 0x40 3 0x01;      //SELECT_IADC_NUM = 1, should match SEL_CLK_DIV
w 0x40 8 0x07;      //MASTER_BCK_DIV1 = 0, MASTER_MODE_ENABLE = 1
w 0x40 9 0x07;      //SELECT_I²S_TDM_NUM = 7 for 48k/44.1k,3 for 96k,1 for 192k (must match Reg 2)
w 0x40 10 0x05;     //TDM_VALID_EDGE = 1, ENABLE_TDM_CLK = 1
w 0x40 11 0x01;     //TDM_CH_NUM = 1 (# of channels = 1 + TDM_CH_NUM)
w 0x40 12 0x00;     //TDM_LINE_SEL_CH1: 00 (GPIO3), TDM_SLOT_SEL_CH1: 0 (slot 0)
w 0x40 13 0x01;     //TDM_LINE_SEL_CH2: 00 (GPIO3), TDM_SLOT_SEL_CH2: 1 (slot 1)
w 0x40 14 0x20;     //TDM_LINE_SEL_CH3: 01 (GPIO4), TDM_SLOT_SEL_CH3: 0 (slot 0)
w 0x40 15 0x21;     //TDM_LINE_SEL_CH4: 01 (GPIO4), TDM_SLOT_SEL_CH4: 1 (slot 1)
w 0x40 23 0x0A;     //FS_PHASE = 10

//GPIO enabling
w 0x40 74 0x22;     //GPIO1_CFG and GPIO2_CFG set to AUX output (clocks out)
w 0x40 75 0x22;     //GPIO3_CFG set to AUX output (data out)
w 0x40 86 0x03;     //GPIO1_IE and GPIO2_IE input enabled
w 0x40 88 0x0F;     //GPIO1_OE and GPIO2_OE and GPIO3_OE and GPIO4_OE output enabled

//ADC CONFIG
w 0x40 63 0xBB;     //ADC Ch1 Config
w 0x40 64 0x38;
w 0x40 65 0xBB;     //ADC Ch2 Config
w 0x40 66 0x38;
w 0x40 67 0xBB;     //ADC Ch3 Config
w 0x40 68 0x38;
w 0x40 69 0xBB;     //ADC Ch4 Config
w 0x40 70 0x38;
w 0x40 71 0xFF;     //set common mode to 3

//ADC filter and datapath registers
w 0x40 113 0x98;    //ADC1_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 130 0x98;    //ADC2_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 147 0x98;    //ADC3_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 164 0x98;    //ADC4_FILTER_SHAPE = Minimum phase slow roll off
```

Note: If using ESS EVB 98x2 1v2v1, set Reg 118[0] = 1’b1 and 135[0] = 1’b1.

I²S Slave

FS=48kHz, 4 Channel from 2 data lines of I²S, MCLK=49.152MHz

```
w 0x48 193 0x01;    //SEL_SYSCLK_IN = 00 (XTAL), EN_ANA_CLKIN = 1
//w 0x48 193 0x05;  //SEL_SYSCLK_IN = 10 (ACLK), EN_ANA_CLKIN = 1
w 0x48 194 0x01;    //SEL_CLK_DIV = 1/2 (sets ADC CLK rate, must be 22 or 24MHz)

w 0x40 0 0x00;      //OUTPUT_SEL = 00 (I²S)
w 0x40 1 0xFF;      //ENABLE_ADC_CH and ENABLE_DATA_IN_CH
w 0x40 2 0x07;      //SELECT_ADC_NUM = 7 for 48k/44.1k, 3 for 96k, 1 for 192k
w 0x40 3 0x01;      //SELECT_IADC_NUM = 1, should match SEL_CLK_DIV
w 0x40 8 0x00;      //MASTER_BCK_DIV1 = 0, MASTER_MODE_ENABLE = 0
w 0x40 9 0x00;      //master mode is disabled
w 0x40 10 0x05;     //TDM_VALID_EDGE = 1, ENABLE_TDM_CLK = 1
w 0x40 11 0x01;     //TDM_CH_NUM = 1 (# of channels = 1 + TDM_CH_NUM)
w 0x40 12 0x00;     //TDM_LINE_SEL_CH1: 00 (GPIO3), TDM_SLOT_SEL_CH1: 0 (slot 0)
w 0x40 13 0x01;     //TDM_LINE_SEL_CH2: 00 (GPIO3), TDM_SLOT_SEL_CH2: 1 (slot 1)
w 0x40 14 0x20;     //TDM_LINE_SEL_CH3: 01 (GPIO4), TDM_SLOT_SEL_CH3: 0 (slot 0)
w 0x40 15 0x21;     //TDM_LINE_SEL_CH4: 01 (GPIO4), TDM_SLOT_SEL_CH4: 1 (slot 1)
w 0x40 23 0x0A;     //FS_PHASE = 10

//GPIO enabling
w 0x40 74 0x11;     //GPIO1 and GPIO2 set to AUX input (slave mode)
w 0x40 75 0x22;     //GPIO3 and GPIO4 set to AUX output
w 0x40 86 0x03;     //GPIO1 and GPIO2 input enabled
w 0x40 88 0x0C;     //GPIO3 and GPIO4 output enabled

//ADC CONFIG
w 0x40 63 0xBB;     //ADC Ch1 Config
w 0x40 64 0x38;
w 0x40 65 0xBB;     //ADC Ch2 Config
w 0x40 66 0x38;
w 0x40 67 0xBB;     //ADC Ch3 Config
w 0x40 68 0x38;
w 0x40 69 0xBB;     //ADC Ch4 Config
w 0x40 70 0x38;
w 0x40 71 0xFF;     //set common mode to 3

//ADC filter and datapath registers
w 0x40 113 0x98;    //ADC1_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 130 0x98;    //ADC2_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 147 0x98;    //ADC3_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 164 0x98;    //ADC4_FILTER_SHAPE = Minimum phase slow roll off
```

Note: If using ESS EVB 98x2 1v2v1, set Reg 118[0] = 1'b1 and 135[0] = 1'b1.

TDM Master

FS=48kHz, 4 Channel TDM (Left Justified), MCLK=49.152MHz

```
w 0x48 193 0x01;    //SEL_SYSCLK_IN = 00 (XTAL), EN_ANA_CLKIN = 1
//w 0x48 193 0x05;  //SEL_SYSCLK_IN = 10 (ACLK), EN_ANA_CLKIN = 1
w 0x48 194 0x01;    //SEL_CLK_DIV = 1/2 (sets ADC CLK rate, must be 22 or 24MHz)

w 0x40 0 0x40;      //OUTPUT_SEL = 10 (TDM)
w 0x40 1 0xFF;      //ENABLE_ADC_CH and ENABLE_DATA_IN_CH
w 0x40 2 0x07;      //SELECT_ADC_NUM = 7 for 48k/44.1k, 3 for 96k, 1 for 192k
w 0x40 3 0x01;      //SELECT_IADC_NUM = 1, should match SEL_CLK_DIV
w 0x40 7 0x20;      //MASTER_WS_SCALE = Scale WS by 2
w 0x40 8 0x07;      //MASTER_BCK_DIV1 = 0, MASTER_MODE_ENABLE = 1
w 0x40 9 0x03;      //SELECT_I²S_TDM_NUM = 3 (SELECT_I²S_TDM_NUM + 1)*(MASTER_WS_SCALE)
w 0x40 10 0x03;     //TDMLJ format: TDM_LJ = 1, TDM_VALID_EDGE = 0, ENABLE_TDM_CLK = 1
w 0x40 11 0x03;     //TDM_CH_NUM = 3 (# of channels = 1 + TDM_CH_NUM)
w 0x40 12 0x00;     //TDM_LINE_SEL_CH1: 00 (GPIO3),  TDM_SLOT_SEL_CH1: 0 (slot 0)
w 0x40 13 0x01;     //TDM_LINE_SEL_CH2: 00 (GPIO3),  TDM_SLOT_SEL_CH2: 1 (slot 1)
w 0x40 14 0x02;     //TDM_LINE_SEL_CH3: 00 (GPIO3),  TDM_SLOT_SEL_CH3: 2 (slot 2)
w 0x40 15 0x03;     //TDM_LINE_SEL_CH4: 00 (GPIO3),  TDM_SLOT_SEL_CH4: 3 (slot 3)
w 0x40 23 0x0A;     //FS_PHASE = 10
w 0x40 33 0x95;     //TDM format LJ requires SYNC_POSEDGE_FRAME = 1

//GPIO enabling
w 0x40 74 0x22;     //GPIO1_CFG and GPIO2_CFG set to AUX output (master mode)
w 0x40 75 0x02;     //GPIO3_CFG set to AUX output (data out)
w 0x40 86 0x03;     //GPIO1_IE and GPIO2_IE input enabled
w 0x40 88 0x0F;     //GPIO1_OE and GPIO2_OE and GPIO3_OE and GPIO4_OE output enabled

//ADC CONFIG
w 0x40 63 0xBB;     //ADC Ch1 Config
w 0x40 64 0x38;
w 0x40 65 0xBB;     //ADC Ch2 Config
w 0x40 66 0x38;
w 0x40 67 0xBB;     //ADC Ch3 Config
w 0x40 68 0x38;
w 0x40 69 0xBB;     //ADC Ch4 Config
w 0x40 70 0x38;
w 0x40 71 0xFF;     //set common mode to 3

//ADC filter and datapath registers
w 0x40 113 0x98;    //ADC1_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 130 0x98;    //ADC2_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 147 0x98;    //ADC3_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 164 0x98;    //ADC4_FILTER_SHAPE = Minimum phase slow roll off
```

Note: If using ESS EVB 98x2 1v2v1, set Reg 118[0] = 1’b1 and 135[0] = 1’b1.

TDM Slave

FS=48kHz, 4 Channel TDM (Left Justified), MCLK=49.152MHz

```
w 0x48 193 0x01;    //SEL_SYSCLK_IN = 00 (XTAL), EN_ANA_CLKIN = 1
//w 0x48 193 0x05;  //SEL_SYSCLK_IN = 10 (ACLK), EN_ANA_CLKIN = 1
w 0x48 194 0x01;    //SEL_CLK_DIV = 1/2 (sets ADC CLK rate, must be 22 or 24MHz)

w 0x40 0 0x40;      //OUTPUT_SEL = 10 (TDM)
w 0x40 1 0xFF;      //ENABLE_ADC_CH and ENABLE_DATA_IN_CH
w 0x40 2 0x07;      //SELECT_ADC_NUM = 7 for 48k/44.1k, 3 for 96k, 1 for 192k
w 0x40 3 0x01;      //SELECT_IADC_NUM = 1, should match SEL_CLK_DIV
w 0x40 8 0x00;      //MASTER_BCK_DIV1 = 0, MASTER_MODE_ENABLE = 0
w 0x40 9 0x00;      //master mode is disabled
w 0x40 10 0x03;     //TDMLJ format: TDM_LJ = 1, TDM_VALID_EDGE = 0, ENABLE_TDM_CLK = 1
w 0x40 11 0x03;     //TDM_CH_NUM = 3 (# of channels = 1 + TDM_CH_NUM)
w 0x40 12 0x00;     //TDM_LINE_SEL_CH1: 00 (GPIO3), TDM_SLOT_SEL_CH1: 0 (slot 0)
w 0x40 13 0x01;     //TDM_LINE_SEL_CH2: 00 (GPIO3), TDM_SLOT_SEL_CH2: 1 (slot 1)
w 0x40 14 0x02;     //TDM_LINE_SEL_CH3: 00 (GPIO3), TDM_SLOT_SEL_CH3: 2 (slot 2)
w 0x40 15 0x03;     //TDM_LINE_SEL_CH4: 00 (GPIO3), TDM_SLOT_SEL_CH4: 3 (slot 3)
w 0x40 23 0x0A;     //FS_PHASE = 10
w 0x40 33 0x95;     //TDM format LJ requires SYNC_POSEDGE_FRAME = 1

//GPIO enabling
w 0x40 74 0x11;     //GPIO1_CFG and GPIO2_CFG set to AUX input (clocks in)
w 0x40 75 0x02;     //GPIO3_CFG set to AUX output (data out)
w 0x40 86 0x03;     //GPIO1_IE and GPIO2_IE input enabled
w 0x40 88 0x0C;     //GPIO3_OE and GPIO4_OE output enabled

//ADC CONFIG
w 0x40 63 0xBB;     //ADC Ch1 Config
w 0x40 64 0x38;
w 0x40 65 0xBB;     //ADC Ch2 Config
w 0x40 66 0x38;
w 0x40 67 0xBB;     //ADC Ch3 Config
w 0x40 68 0x38;
w 0x40 69 0xBB;     //ADC Ch4 Config
w 0x40 70 0x38;
w 0x40 71 0xFF;     //set common mode to 3

//ADC filter and datapath registers
w 0x40 113 0x98;    //ADC1_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 130 0x98;    //ADC2_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 147 0x98;    //ADC3_FILTER_SHAPE = Minimum phase slow roll off
w 0x40 164 0x98;    //ADC4_FILTER_SHAPE = Minimum phase slow roll off
```

Note: If using ESS EVB 98x2 1v2v1, set Reg 118[0] = 1’b1 and 135[0] = 1’b1.

Resync

The respective s2m script is to be run on all slave mode ES9842 PROs in TDM Cascade or Parallel mode after clocks from the master have been initialized. This is to ensure all chips are properly synced with each other for optimal performance.

I²S Resync

```
w 34 0x1D; // Turn off AUTO_FIR_SYNC
w 33 0x35; // FORCE_FIR_SYNC = 1'b1
w 33 0x15; // FORCE_FIR_SYNC = 1'b0
w 34 0x1F; // Turn on AUTO_FIR_SYNC
```

LJ Resync

```
w 34 0x1D; // Turn off AUTO_FIR_SYNC
w 33 0x35; // FORCE_FIR_SYNC = 1'b1
w 33 0x95; // FORCE_FIR_SYNC = 1'b0
w 34 0x1F; // Turn on AUTO_FIR_SYNC
```

Revision History

Current Version 0.5.1

Rev.	Date	Notes
0.1.4	October 30, 2020	Initial release
0.5.1	October, 2025	• Updated formatting • Updated Digital Signal Path and Peak Detection • Added DC Offset, Gain, DFIR Filters, Input and Output Mapping • Updated TDM Cascade Mode and TDM/PCM Parallel Mode • Updated 64FS Mode Section • Updated Switching Characteristics • Updated MCLK Edge to BCK Edge wording and unit signs • Updated Functional Block Diagram • Updated I²S Decoder Section and Registers • Consolidated Digital Audio Input Port and Digital Audio Output Port into Audio Input/Output Formats • Updated S/PDIF Pin Connections and GPIO section • Added Resync Registers to Addendum • Added Interface Modes section • Updated Reference Schematic to use ES9312Q regulator • Renamed Reg 17, 112, 129, 146, 163 • Updated Descriptions in Registers 0[1], 63-71, 101[0], 118[0], 135[0], 152[0]