Analog Reinvented

ES9017
32-bit High-Performance 8-Channel DAC
Product Datasheet

The ESS SABRE® ES9017 is an 8 Channel synchronous 32-Bit digital-to-analog converter (DAC) that offers unsurpassed performance/cost solution for receivers, personal audio devices, professional audio applications such as recording systems, mixer consoles and digital audio workstations (DAW) audio processors applications.

The ES9017 has 8 integrated DACs which use ESS' new patented Hyperstream® IV DAC Architecture. The same technology that is used in the ESS SABRE PRO® lineup. It delivers incredible audio sound quality and specifications, including +120dB DNR and -110dB THD+N per channel.

The ES9017 SABRE® DAC improves on previous designs to include:

- TDM audio format & SPI serial communication support for more connectivity options.
- Lower power consumption than previous generations, including the Hyperstream® IV DAC modulator.
- Hardware mode support for ease-of-use.

TDM, DSD, DoP, and PCM (I²S, LJ) master/slave audio interfaces are supported both in hardware and software modes.

The ES9017 has 7 built-in pre-programmed digital filters which allows the most discerning user to tune the SABRE® sound to their own personal sound signature. In hardware mode, 2 of these filters are available through a GPIO setting.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream® IV Architecture DAC Technology	32-bit audio DAC with high dynamic range & ultra-low distortion
+120dB DNR per Channel -110dB THD+N per Channel	Excellent True dynamic range and low distortion
High Sample Rates	Up to PCM 768kHz & native DSD512
7 Built-In Filter Characteristics	Predefined digital filters optimized for latency or sound color
Multiple Input Formats and High Sample Rates	TDM, I²S, LJ, RJ, DSD, DoP. Up to PCM 768kHz and native DSD512.
I²C/SPI Software Interface Control or Hardware Interface	Configured by microcontroller or other I²C/SPI source, or pins through Hardware Mode
Lower Power Consumption than Previous Gen	Simplifies power supply design, <10mW/channel
Standardized Packaging	7mm x 7mm, 48 pin QFP/QFN for reduced PCB footprint

APPLICATIONS

- Digital Audio Workstations (DAW) Audio Playback
- A/V Receivers (AVR)
- Personal Audio Devices & Media Streamers
- Sound Bars
- Mixers
- High End Audio Equipment
- DAP (Digital Audio Players)
- DJ Equipment

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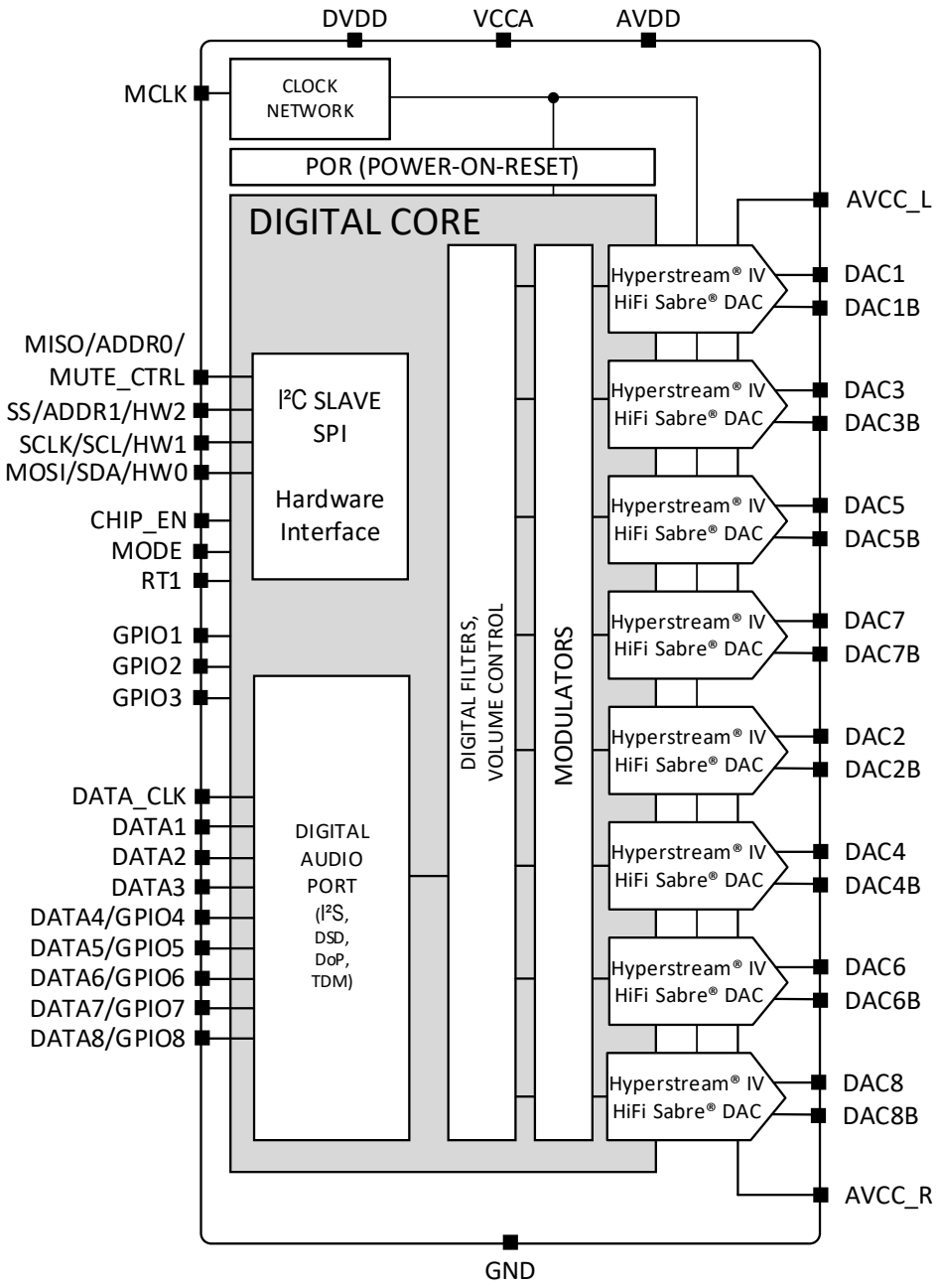


Figure 1 - Functional Block Diagram

ES9017 Package

48 QFN/QFP Pinout[1]

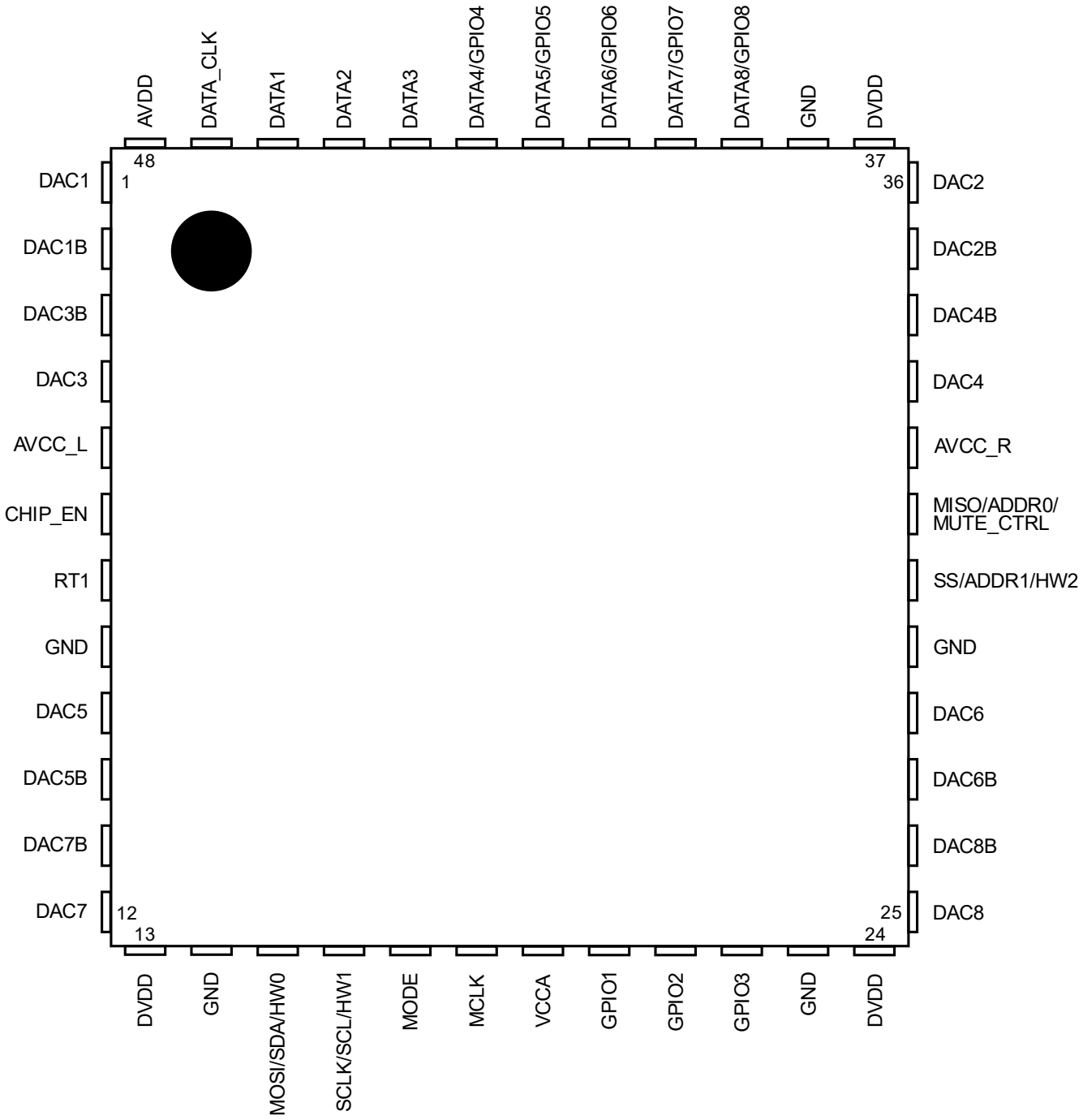


Figure 2 - 48 QFN/QFP Pinout

[1] ES9017Q has an exposed pad (Pin 49) that should be connected to ground, ES9017S does not have an exposed pad.

48 QFN/QFP Pin List

Pin	Name	Pin Type	Reset State	Pin Description
1	DAC1	AO	Ground	Differential Positive Output for Channel 1
2	DAC1B	AO	Ground	Differential Negative Output for Channel 1
3	DAC3B	AO	Ground	Differential Negative Output for Channel 3
4	DAC3	AO	Ground	Differential Positive Output for Channel 3
5	AVCC_L	Power	Power	3.3V DAC analog output stage reference supply for the Left side **Note: AVCC_L is required to be very low noise.**
6	CHIP_EN	I	HiZ	Active-high Chip Enable
7	RT1	I	HiZ	Reserved. Must be connected to GND for normal operation.
8	GND	Ground	Ground	Ground
9	DAC5	AO	Ground	Differential Positive Output for Channel 5
10	DAC5B	AO	Ground	Differential Negative Output for Channel 5
11	DAC7B	AO	Ground	Differential Negative Output for Channel 7
12	DAC7	AO	Ground	Differential Positive Output for Channel 7
13	DVDD	Power	Power	Digital Core Supply, 1.2V
14	GND	Ground	Ground	Ground
15	MOSI	I	HiZ	SPI Main Out Sub In pin, controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
16	SCLK	I	HiZ	SPI Serial Clock pin, controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
17	MODE	I	HiZ	I²C/SPI Control selection or HW mode
18	MCLK	I	HiZ	Oscillator input
19	VCCA	Power	Power	Analog Supply, 3.3V
20	GPIO1	I/O	HiZ	General I/O w/extended functions
21	GPIO2	I/O	HiZ	General I/O w/extended functions
22	GPIO3	I/O	HiZ	General I/O w/extended functions
23	GND	Ground	Ground	Ground
24	DVDD	Power	Power	Digital Supply, 1.2V
25	DAC8	AO	Ground	Differential Positive Output for Channel 8
26	DAC8B	AO	Ground	Differential Negative Output for Channel 8
27	DAC6B	AO	Ground	Differential Negative Output for Channel 6
28	DAC6	AO	Ground	Differential Positive Output for Channel 6
29	GND	Ground	Ground	Ground
30	SS	I	HiZ	SPI Slave Select pin, controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
31	MISO	I	HiZ	SPI Main In Sub Out pin, controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
	MUTE_CTRL			Hardware Mute Control pin, controlled by MODE

32	AVCC_R	Power	Power	3.3V DAC analog output stage reference supply for the Right side **Note: AVCC_R is required to be very low noise.**
33	DAC4	AO	Ground	Differential Positive Output for Channel 4
34	DAC4B	AO	Ground	Differential Negative Output for Channel 4
35	DAC2B	AO	Ground	Differential Negative Output for Channel 2
36	DAC2	AO	Ground	Differential Positive Output for Channel 2
37	DVDD	Power	Power	Digital Supply, 1.2V
38	GND	Ground	Ground	Ground
39	DATA8	I/O	HiZ	Serial DATA8
	GPIO8			General I/O 8
40	DATA7	I/O	HiZ	Serial DATA7
	GPIO7			General I/O 7
41	DATA6	I/O	HiZ	Serial DATA6
	GPIO6			General I/O 6
42	DATA5	I/O	HiZ	Serial DATA5
	GPIO5			General I/O 5
43	DATA4	I/O	HiZ	Serial DATA4
	GPIO4			General I/O 4
44	DATA3	I	HiZ	Serial DATA3 pin
45	DATA2	I	HiZ	Serial DATA2 pin
46	DATA1	I	HiZ	Serial DATA1 pin
47	DATA_CLK	I	HiZ	Serial Data Clock pin
48	AVDD	Power	Power	3.3V I/O Supply
49	Package Pad[1]	-	-	Only for ES9017Q, external pad, connect to GND

Table 1 - 48 QFN/QFP Pin List

*Note: AO = Analog Output, I = Digital Input, I/O = Digital Input/Output

*Note: Unused DAC Output pins must be left as a no connect and the respective DACs should be muted.

[1] Pin 49 is the package pad. See 48 QFN package dimensions for sizing. Connect to GND

Feature List

The ES9017 is a SABRE 32-bit 8 channel synchronous digital-to-analog converter (DAC) using the Hyperstream® IV DAC Architecture.

The ES9017 has improved analog performance over previous generations 8 channel DACs, such as the SABRE9006A. The ES9017 supports TDM, PCM, DSD, DoP audio interfaces, SPI (or I²C) control interface and supports software or hardware modes for ease-of-use.

In software mode, all registers can be accessed through I²C or SPI.

In hardware mode, the input format mode is selected through the hardware pins, limiting the flexibility of configuration.

Configuration Modes

The ES9017 supports 2 different software modes (SPI or I²C), and supports 2 different sets of hardware modes (PCM or TDM/DSD). These modes are controlled by the state of the MODE Pin (Pin 17).

MODE PIN	Configuration Mode	Description
1	Software	SPI interface
Pull 1	Hardware	TDM or DSD Modes
Pull 0	Hardware	PCM Slave or Master Modes
0	Software	I²C interface

Table 2 - Mode Pin Configuration Options

Design Information

Hardware pins can be configured in 4 different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. This also applies to MUTE_CTRL.

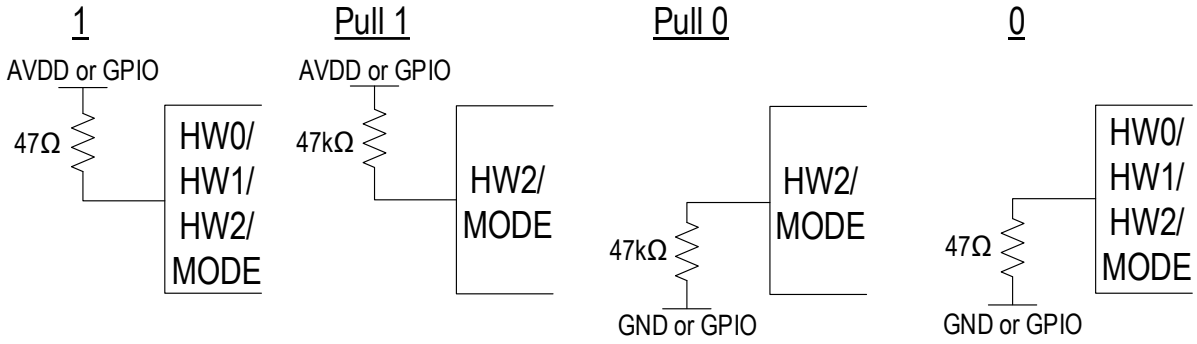


Figure 3 - Hardware Mode Pin Configurations

Note: Hardware mode pin states 0 and 1 can be directly connected to GND or AVDD.

Software Mode

The ES9017 supports I²C or SPI serial communication for configuring registers. The ES9017 has read/write registers and read-only registers. Software modes are set with the MODE pin (Pin 17).

Recommended Software Mode Setup Sequence

The software mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

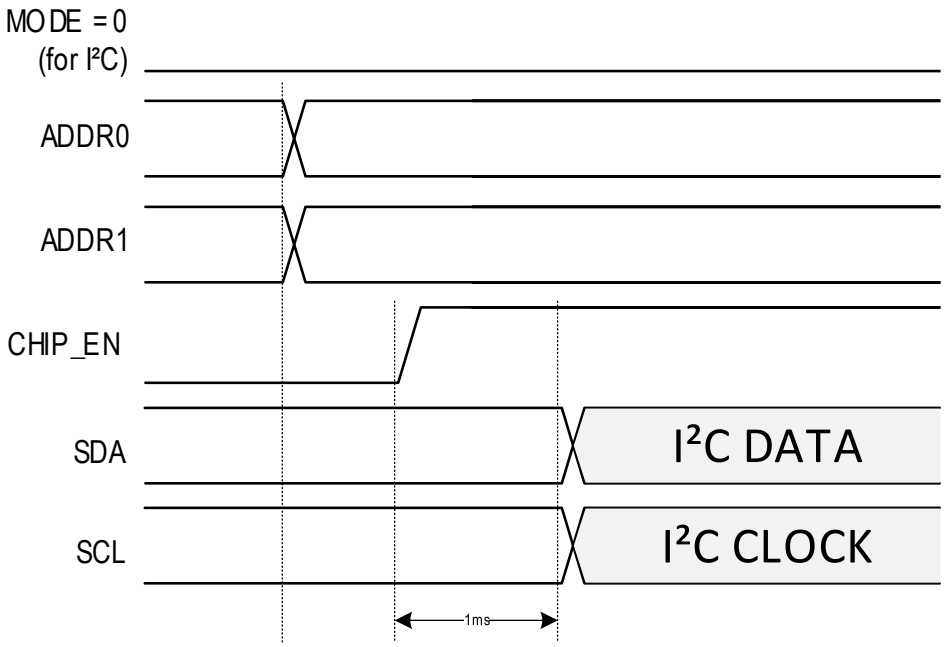


Figure 4 - I²C Software Mode Startup Sequence

I²C Slave Interface Commands

The I²C slave interface is enabled when the MODE pin (Pin 17) is tied low (MODE=0). In I²C mode, ADDR1 (Pin 30) and ADDR0 (Pin 31) determine the I²C address and the R/W bit controls reading or writing.

For I²C Timing information, see Timing Characteristics.

The I²C Slave Interface can be accessed by:

- Pin 15 SDA
- Pin 16 SCL
- Pin 30 ADDR1
- Pin 31 ADDR0

I²C Slave Address = [5'b10010, ADDR1, ADDR0, R/W]

I²C Slave Address	ADDR1	ADDR0
0x90	0	0
0x92	0	1
0x94	1	0
0x96	1	1

Table 3 - I²C Slave Addresses

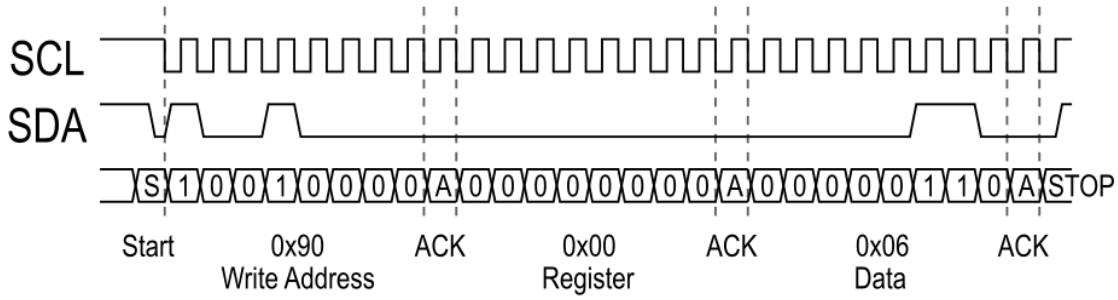


Figure 5 - I²C Write Example

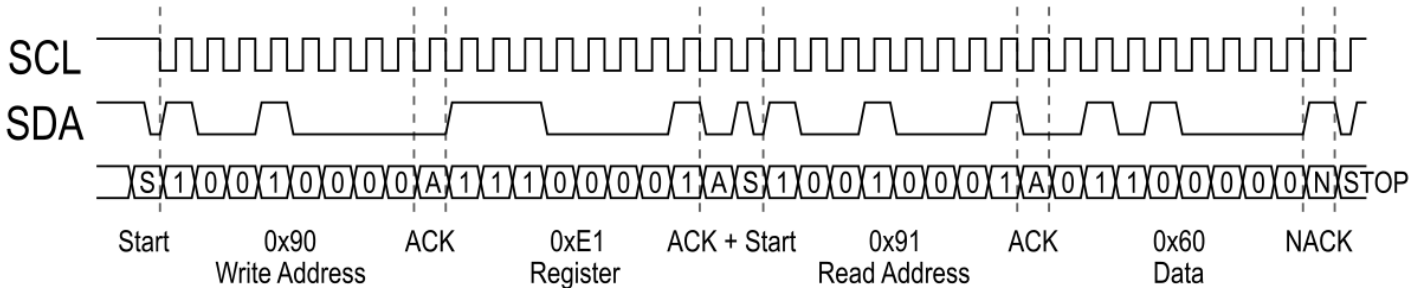


Figure 6 - I²C Read Example

SPI Slave Interface Commands

The Slave Serial Peripheral Interface (SPI) is used when the MODE pin (Pin 17) is tied high (MODE=1).

The slave SPI can be accessed by:

- Pin 15 MOSI
- Pin 16 SCLK
- Pin 30 SS
- Pin 31 MISO

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data.
SPI commands:

- 0x01: Read
- 0x03: Write

For SPI timing information, see Timing Characteristics.

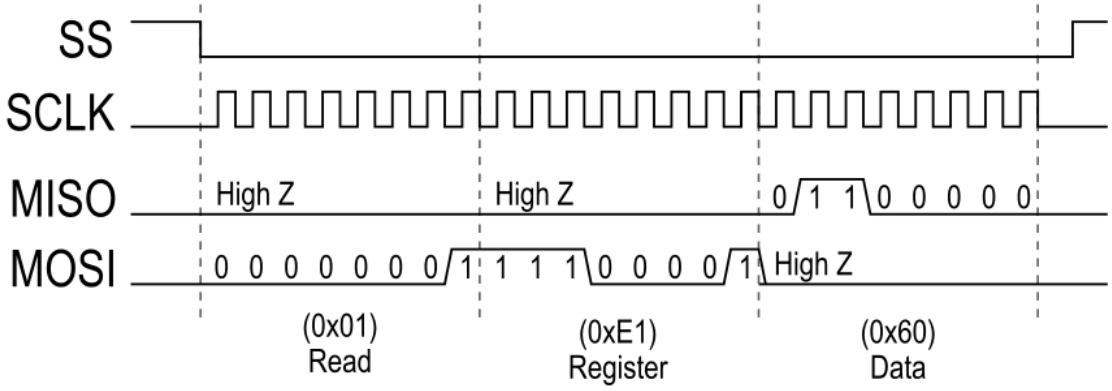


Figure 7 - SPI Single Byte Read

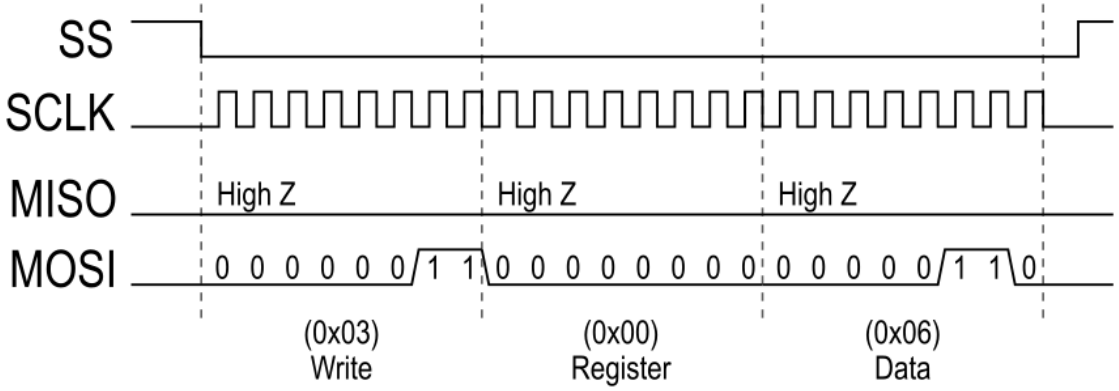


Figure 8 - SPI Single Byte Write

Hardware Mode

The ES9017 has 21 pre-configured modes that can be set with hardware pins. These modes configure the DAC for different audio input formats, master/slave, and sample rates. See Design Information on how to configure the hardware pins.

These modes are set with pins:

- MODE (Pin 17)
- HW0 (Pin 15)
- HW1 (Pin 16)
- HW2 (Pin 30)
- MUTE_CTRL (Pin 31)

Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below with all hardware pins being defined before CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is low until CHIP_EN is asserted, then asserted last to unmute the DAC.

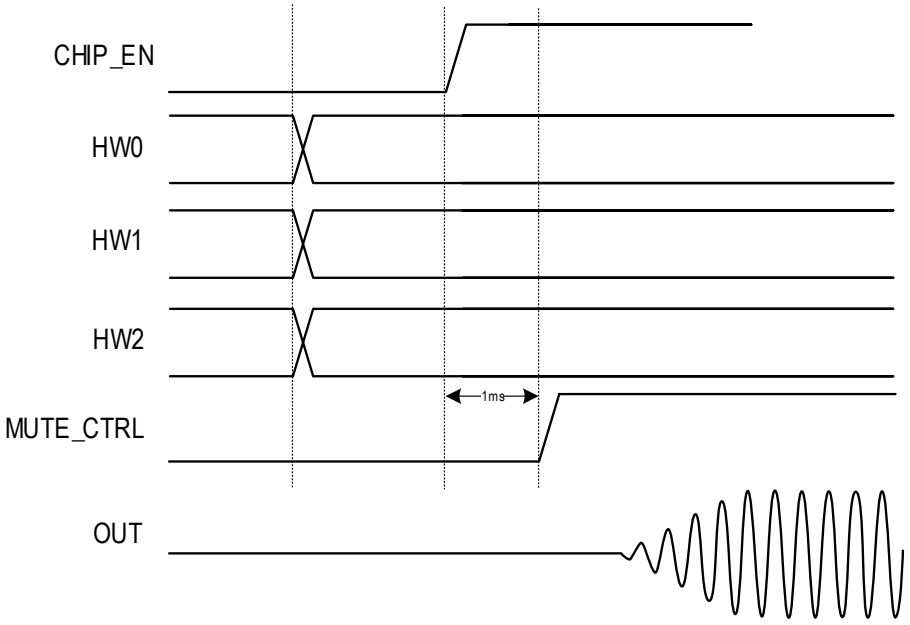


Figure 9 - Hardware Mode Startup Sequence

Hardware Mode Pin Configurations

All modes on ES9017 require synchronous MCLK/FS/BCK or MCLK/DSDCLK.

HW #	Description	FS [kHz]	BCK [MHz]	MCLK [MHz]	MODE	HW2	HW1	HW0
32-bit PCM Master Modes								
0	I²S Master	MCLK/128	64*FS	128*FS	Pull 0	0	0	0
1	I²S Master	MCLK/256	64*FS	256*FS	Pull 0	0	0	1
2	I²S Master	MCLK/512	64*FS	512*FS	Pull 0	0	1	0
3	I²S Master	MCLK/1024	64*FS	1024*FS	Pull 0	0	1	1
4	LJ Master Mode	MCLK/128	64*FS	128*FS	Pull 0	Pull 0	0	0
5	LJ Master Mode	MCLK/256	64*FS	256*FS	Pull 0	Pull 0	0	1
6	LJ Master Mode	MCLK/512	64*FS	512*FS	Pull 0	Pull 0	1	0
7	LJ Master Mode	MCLK/1024	64*FS	1024*FS	Pull 0	Pull 0	1	1
32-bit PCM Slave Modes								
8	I²S Slave, MCLK/1 (or DoP)[1]	8≤FS≤768	64*FS	64*FS≤1024*FS	Pull 0	Pull 1	0	0
9	I²S Slave, MCLK/2 (or DoP) [1]	8≤FS≤384	64*FS	128*FS≤1024*FS	Pull 0	Pull 1	0	1
10	I²S Slave, MCLK/4 (or DoP)[1]	8≤FS≤192	64*FS	256*FS≤1024*FS	Pull 0	Pull 1	1	0
11	I²S Slave, ACG[2] (or DoP)[1]	8≤FS≤768	64*FS	64*FS≤1024*FS	Pull 0	Pull 1	1	1
12	LJ Slave, MCLK/1	8≤FS≤768	64*FS	64*FS≤1024*FS	Pull 0	1	0	0
13	LJ Slave, MCLK/2	8≤FS≤384	64*FS	128*FS≤1024*FS	Pull 0	1	0	1
14	LJ Slave, MCLK/4	8≤FS≤192	64*FS	256*FS≤1024*FS	Pull 0	1	1	0
15	LJ Slave, ACG[2]	8≤FS≤768	64*FS	64*FS≤1024*FS	Pull 0	1	1	1
32-bit TDM LJ Slave Modes								
16	TDM LJ Slave[3] Autodetect CH num Slots 1-8	8≤FS≤192	Auto (256FS/ 512FS/1024FS)	256*FS≤49.152	Pull 1	1	0	0
17	TDM LJ Slave[3] Autodetect CH num Slots 9-16	8≤FS≤96	Auto (512FS/1024FS)	512*FS≤49.152	Pull 1	1	0	1
18	TDM LJ Slave[3] Autodetect CH num Slots 17-24	8≤FS≤48	Auto (1024FS)	1024*FS≤49.152	Pull 1	1	1	0
19	TDM LJ Slave[3] Autodetect CH num Slots 25-32	8≤FS≤48	Auto (1024FS)	1024*FS≤49.152	Pull 1	1	1	1
DSD Slave Modes								
20	DSD Slave, MCLK/1	DSD64-512	64*44.1kHz- 512*44.1kHz	2*DSDCLK≤45.1584MHz	Pull 1	Pull 1	0	0
21	DSD Slave, ACG[2]	DSD64-512	64*44.1kHz- 512*44.1kHz	2*DSDCLK≤45.1584MHz	Pull 1	Pull 1	0	1

Table 4 - Hardware Mode Pin Configurations Table

[1] To enable DoP in HW mode, DATA8/GPIO8 pin must be high.

[2] ACG (Auto Clock Gearing) will gear MCLK down to 128*FS, unless 64*FS is required, or 2*DSDCLK in DSD modes.

[3] TDM uses auto channel detect to determine the amount of channels. 8 Channels of data on a single data line is required in hardware mode to map to all 8 DACs. In software mode, 4 channels on 2 data lines is also supported.

GPIO Functions in Hardware Mode

The following GPIO pins add functionality in Hardware Modes. Unused GPIOs should be terminated to ground.

Warning: GPIO3 MUST be grounded in hardware modes.

Pin	Functionality	Settings
GPIO1	Outputs Automute Status	Output 0: Automute not engaged Output 1: Automute engaged
DATA6/GPIO6	Sets FILTER_SHAPE in Hardware Mode	1'b0: Minimum Phase 1'b1: Linear Phase Fast Roll-Off
DATA8/GPIO8	Enables the DoP decoder[1]	1'b0: DoP Disabled 1'b1: DoP Enabled

Table 5 - GPIO Functions in Hardware Mode

Mute Control

MUTE_CTRL (Pin 31) is used to control the mute configuration of the DAC in hardware mode. It allows for simply muting and unmuting, and to enable automute function to allow the DAC to mute itself as a function of input level.

- 1 Output Unmuted, No Automute
- Pull 1 Output Unmuted, Automute Enabled
- Pull 0 Output Muted, Automute Enabled
- 0 Output Muted, No Automute

[1] DoP is only supported in HW modes 8-11

Digital Features

Digital Signal Path

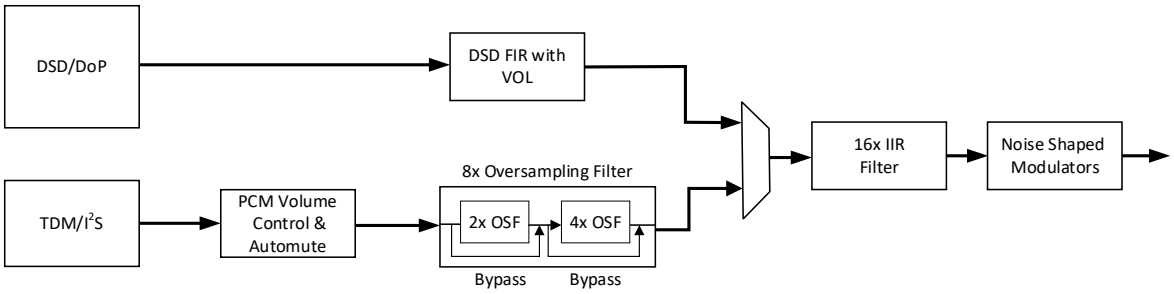


Figure 10 - Digital Signal Path

GPIO Configuration

GPIO CONFIG	Function	I/O Direction
0	Analog Shutdown*	N/A
1	1'b0	Output
2	1'b1	Output
3	CLK_IDAC output	Output
4	Reserved	N/A
5	Mute All Channel	Input
6	System Mode Control	Input
7	Reserved	Output
8	CLKEN_1FS	Output
9	TDM_VALID	Output
10	DOP_VALID	Output
11	BCK_WS_FAIL	Output
12	Volume Min	Output
13	Automute Status	Output
14	Soft Ramp Finished	Output
15	Reserved	N/A

Table 6 - GPIO Configuration Functions

GPIO Default states:

GPIO1: Automute Status
GPIO2-8: Analog Shutdown

Analog Shutdown

Analog Shutdown is input disabled, output is tri-stated.

Output 1'b0

Outputs a constant 1'b0.

Output 1'b1

Outputs a constant 1'b1.

CLK_IDAC Output

Outputs the CLK_IDAC clock. Requires DAC to be on.

Mute All Channels

Mute all DAC channels

System Mode Control

Change the system mode (enable/disable datapath) via GPIO. Register 23-24[15] GPIO_DAC_MODE changes whether a 1 on the GPIO will enable or disable the datapath.

When GPIOx input is 1'b0, the system mode will be determined by Register 0[1] DAC_MODE_REG.

Relevant Registers

- Register 23-24[15] GPIO_DAC_MODE
  - 1'b0: Disable datapath when GPIOx input is 1'b1
  - 1'b1: Enable datapath when GPIOx input is 1'b0
- Register 0[1] DAC_MODE_REG

CLKEN_1FS

Outputs the CLKEN_1FS clock, which is a clock with a pulse every 1FS.

TDM_VALID

Outputs HIGH when the TDM input is valid.

DOP_VALID

Outputs HIGH when the DoP input is valid.

Note: DOP_VALID is for Channel 1&2, as a channel pair

BCK_WS_FAIL

Outputs the status of the BCK and WS monitors. HIGH if either monitor detects an invalid signal.

BCK is considered invalid if the ratio MCLK/BCK > 1024.

WS is considered invalid if the ratio BCK/WS > 256.

Note: The minimum BCK frequency for the flag to stay valid is 176.4kHz/192kHz for 45.1584MHz/49.152MHz MCLKs respectfully.

Relevant Registers

- Register 30[5] ENABLE_WS_MONITOR
- Register 30[4] ENABLE_BCK_MONITOR

Volume Min

Outputs HIGH when the DAC is muted. This can occur from manually muting, automuting, and setting volume to 0xFF.

Relevant Registers

- Register 23-24[4] GPIO_OR_VOL_MIN sets the output to be the logical AND of both channels' vol min flags.
- Register 23-24[1] GPIO_AND_VOL_MIN sets the output to be the logical OR of both channels' vol min flags.
- Register 23-24[8:6] FLAG_CH_SEL selects which of the individual DAC channel flags to output.

Automute Status

Outputs HIGH when the DACs automute condition is met. The output can be any of the channels' flags or be the logical AND or OR of all the flags.

Relevant Registers

- Register 23-24[3] GPIO_OR_AUTOMUTE sets the output to be the logical OR of all channels' automute flags
- Register 23-24[0] GPIO_AND_AUTOMUTE sets the output to be the logical AND of all channels' automute flags
- Register 23-24[8:6] GPIO_SEL sets the output to be one of the individual channels' flags

Soft Ramp Finished

Outputs HIGH when the DAC is neither ramping up nor down. The output can be any of the channels' flags or be the logical AND or OR of all the flags.

Relevant Registers

- Register 23-24[5] GPIO_OR_SS_RAMP sets the output to be the logical OR of all channels' soft ramp flags
- Register 23-24[2] GPIO_AND_SS_RAMP sets the output to be the logical AND of all channels' soft ramp flags
- Register 23-24[8:6] GPIO_SEL sets the output to be one of the individual channels' flags

Clock Distribution

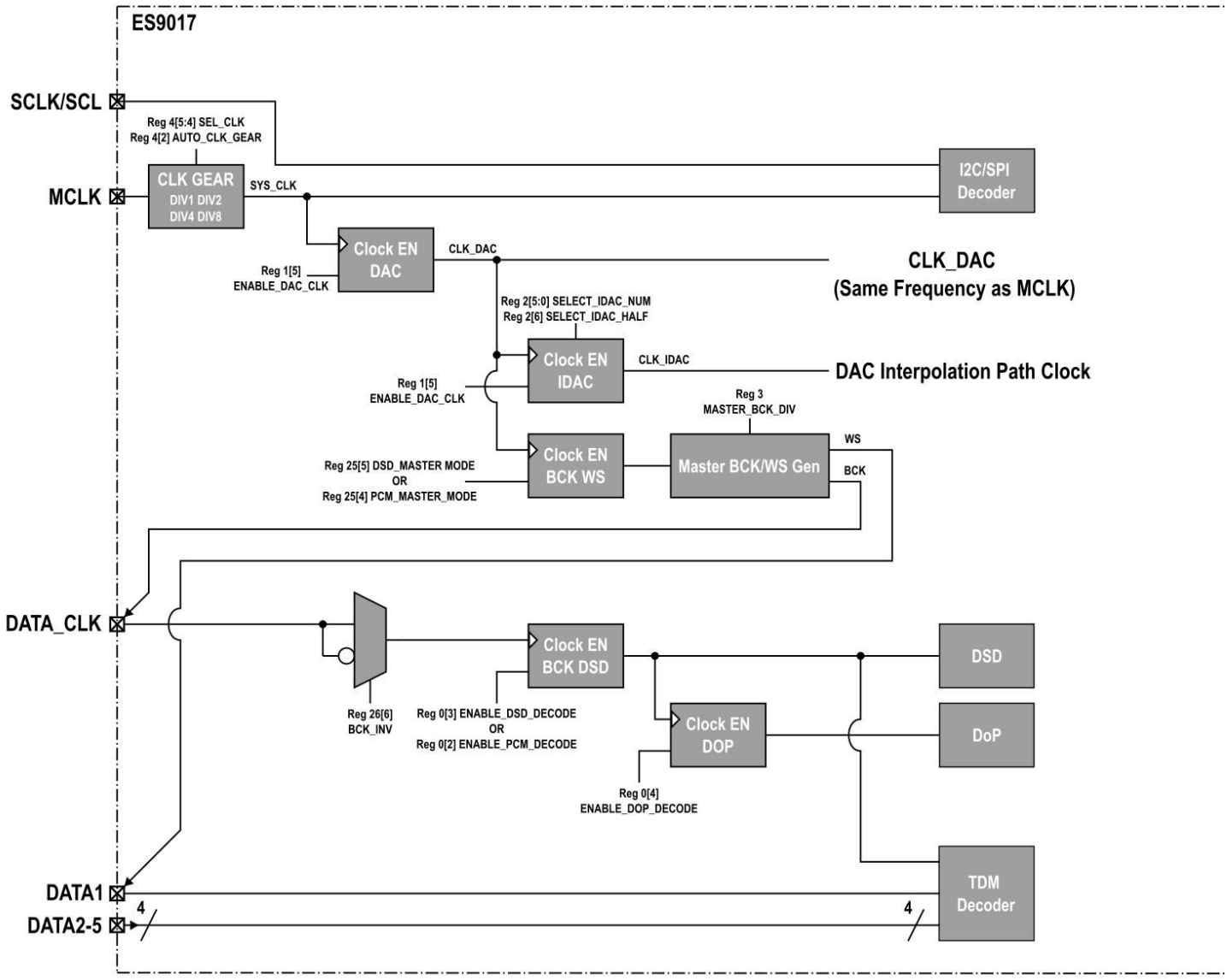


Figure 11 - Internal clock distribution diagram for ES9017

Audio Input Formats

The ES9017 supports PCM, TDM, DoP and Native DSD. ES9017 can detect the input format on DATA2 by default (Register 25[0] AUTO_INPUT_SEL=1). The input data format can also be manually set using Register 25[2:1] INPUT_SEL.

The formats include:

- PCM (I²S/LJ)
  - Slave and master mode in 16, 24, 32-bit widths.
  - I²S, Left Justified (LJ), and Right Justified (RJ).
  - Sample rates up to 768kHz (64fs mode).
  - Channel Remapping & Invert.
- TDM
  - Slave mode in hardware mode. Slave and master modes in software mode.
  - LJ format in hardware modes. I²S or LJ in software modes.
  - Channel Remapping & Invert.
- DoP (DSD Over PCM)
  - Slave and master mode.
  - Sample rates from DoP512 (24bit, 1.4112MHz PCM).
  - Channel Remapping & Invert.
- Native DSD
  - Slave and master mode.
  - Sample rates from DSD64 (2.8224Mbits/sec, 64 x 44.1kHz) to DSD512.
  - Channel Invert.

PCM (I²S/LJ)

Data is organized into 2 channels per data line. Any channel on any data line can be mapped to any DAC through the TDM_CHx_CONFIG channel mapping Registers 32-39. Data is latched on the positive edge of BCLK.

In hardware mode, PCM (I²S/LJ) data lines are fixed to the mapping shown in Table 8.

In software mode, PCM (I²S/LJ) data lines can be re-mapped to any DAC.

PCM Pin Connections:

Pin Name	Function	Description
DATA_CLK	PCM BCLK	PCM Clock (Bit Clock), Master or Slave
DATA1	PCM WS	PCM WS (Word Select/Frame Select), Master or Slave
DATA2	PCM DATA	PCM Data Channel 1 & 2
DATA3	PCM DATA	PCM Data Channel 3 & 4
DATA4	PCM DATA	PCM Data Channel 5 & 6
DATA5	PCM DATA	PCM Data Channel 7 & 8

Table 7 - PCM Pin Connections

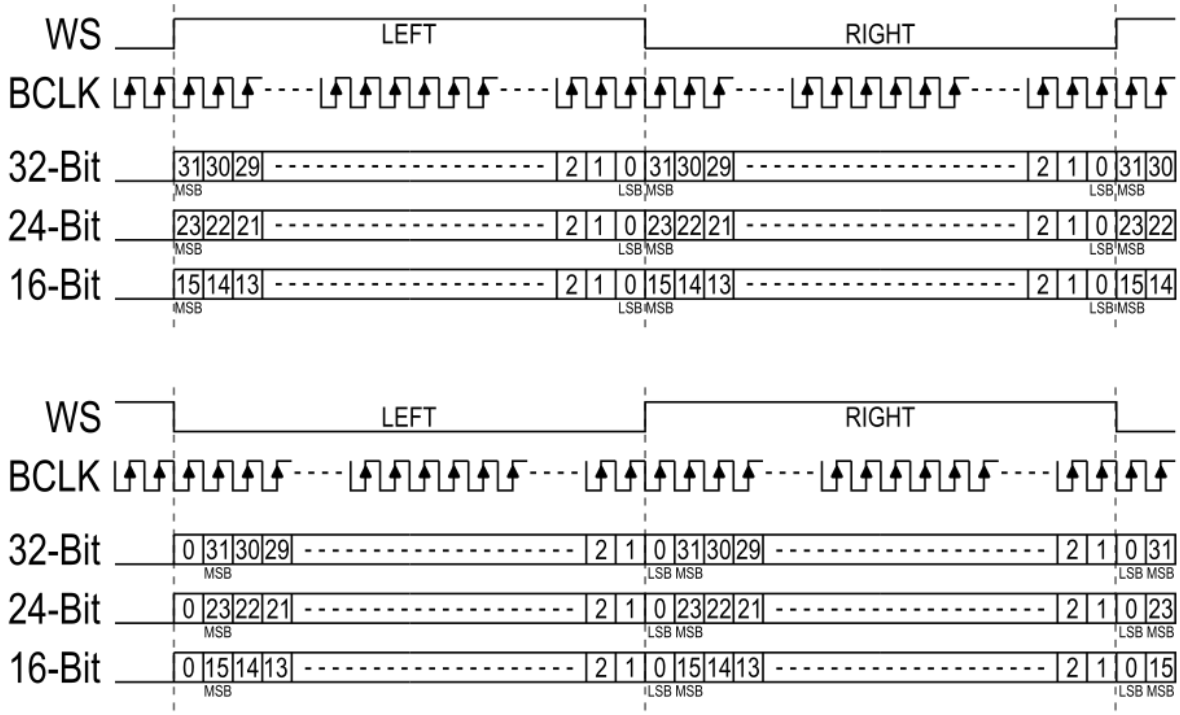


Figure 12 - LJ (top) & I²S (bottom) for 16, 24, and 32-bit Word Widths

Note: RJ is only supported in software mode

TDM (Time-Division Multiplexing)

The ES9017 supports TDM format, allowing for 4 channels, 8 channels, 16 channels or 32 channels on a single data line. Supported formats are TDM4 (4ch), TDM8 (8ch), TDM16 (16ch) and TDM32 (32ch). TDM is supported in both software and hardware modes. Data is latched on the positive edge of BCLK.

In hardware mode, TDM8 and above are supported. Hardware modes require TDM data line to be input through DATA2. In hardware mode, TDM8 will map slots 1 to 8 to DACs 1 to 8, respectively. In the case of TDM16, the hardware mode will be configured so that slots 1 to 8 will map to one device (HW mode #16), and slots 9-16 to the next device (HW mode #17).

In software mode, Register 32-39: TDM_CHx_CONFIG can be set to internally map any slot to each DAC. In this case TDM4, TDM8, TDM16 and TDM32 are all supported. Software mode allows the TDM Data to be input through any of the serial data lines (DATA2, DATA3, DATA4 or DATA5).

TDM Pin Connection:

Pin Name	Function	Description
DATA_CLK	TDM BCLK	TDM bit clock, Master or Slave
DATA1	TDM WS	TDM Word Select/Frame Clock, Master or Slave
DATA2	TDM DATA	TDM data line

Table 8 - TDM Pin Connections

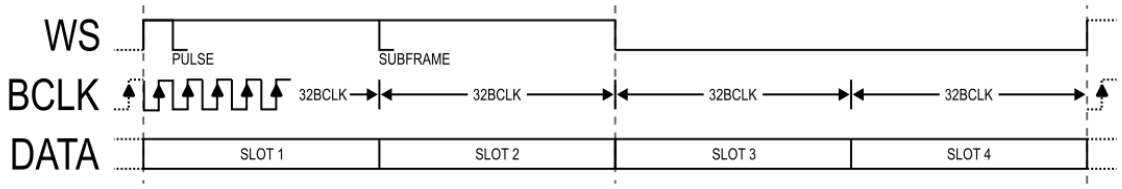


Figure 13 - TDM4 Mode

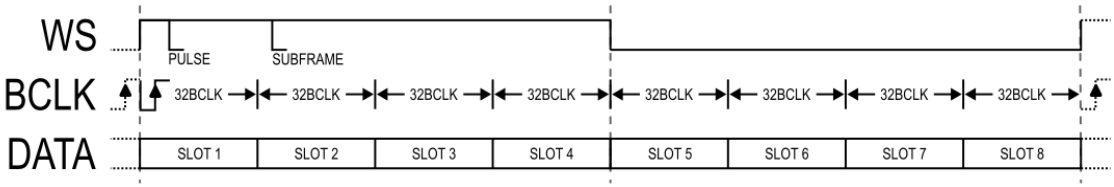


Figure 14 - TDM8 Mode

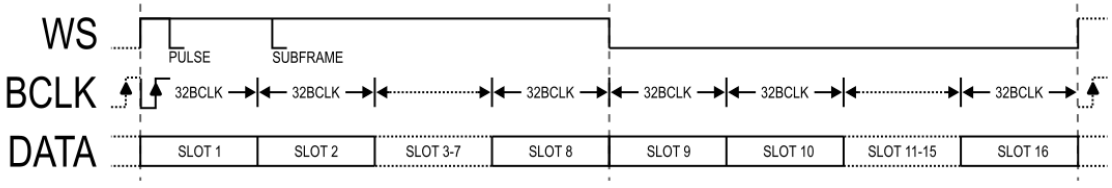


Figure 15 - TDM16 Mode

DSD[1]

In DSD mode, there is a single DSD clock line, and each channel of data is an additional DSD data line. There is no internal channel mapping for DSD input, DSD data input to DATA1 is sent to DAC1, DSD data input to DATA2 is set to DAC2, etc.

DSD Pin Connections:

Pin Name	Function	Description
DATA_CLK	DSD CLK	DSD Clock
DATA1	DSD CH1	DSD DATA Channel 1
DATA2	DSD CH2	DSD DATA Channel 2
DATA3	DSD CH3	DSD DATA Channel 3
DATA4	DSD CH4	DSD DATA Channel 4
DATA5	DSD CH5	DSD DATA Channel 5
DATA6	DSD CH6	DSD DATA Channel 6
DATA7	DSD CH7	DSD DATA Channel 7
DATA8	DSD CH8	DSD DATA Channel 8

Table 9 - DSD Pin Connections

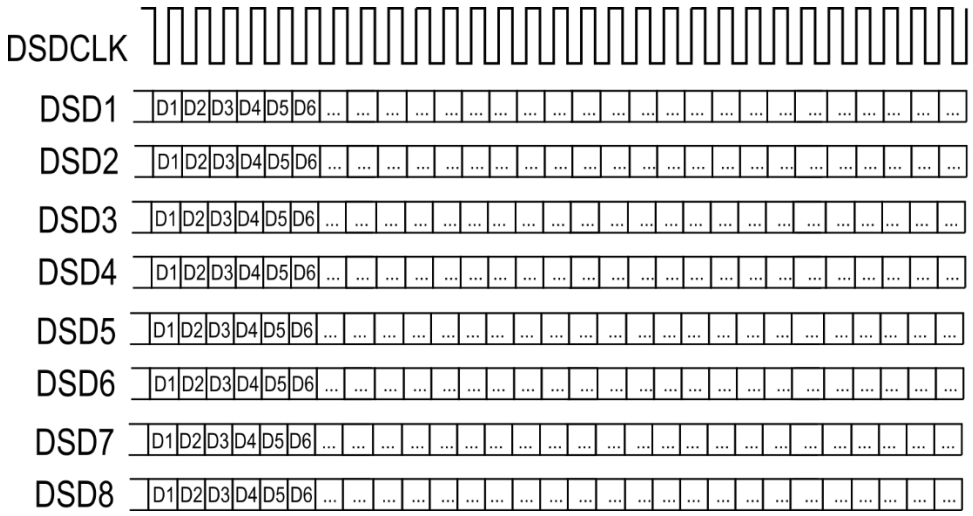


Figure 16 - DSD Format, 1-bit stream

[1] Automute feature is not available when using DSD mode.

Pre-Programmed Digital Filters

The ES9017 has 7 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 53[2:0] FILTER_SHAPE for configuration)

#	Filter	Description
0	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection
1	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
2	Linear Phase Fast Roll-Off	SABRE legacy filter, optimized for image rejection @ 0.55FS
4	Linear Phase Slow Roll-Off	SABRE legacy filter, optimized for lower latency, but symmetric impulse response
5	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
6	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
7	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 10 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ FS = 44.1kHz
Minimum Phase (default)	163us
Linear Phase Apodizing Fast Roll-Off	829us
Linear Phase Fast Roll-Off	843us
Linear Phase Slow Roll-Off	218us
Minimum Phase Fast Roll-Off	163us
Minimum Phase Slow Roll-Off	141us
Minimum Phase Fast Roll-Off Low Dispersion	299us

Table 11 - PCM Filter Latency

PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-97dB	0.55FS			Hz
Group Delay		2.90/FS		8.99/FS	s
Flatness (ripple)	0.0012				dB

Linear Phase Apodizing Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41FS	Hz
Stop band	-107dB	0.50FS			Hz
Group Delay			32.81/FS		s
Flatness (ripple)	0.0024				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45FS	Hz
Stop band	-117dB	0.55FS			Hz
Group Delay			33.43/FS		s
Flatness (ripple)	0.0030				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.44FS	Hz
Stop band	-91dB	0.75FS			Hz
Group Delay			5.87/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46FS	Hz
Stop band	-98dB	0.55FS			Hz
Group Delay		2.91/FS		9.14/FS	s
Flatness (ripple)	0.0023				dB

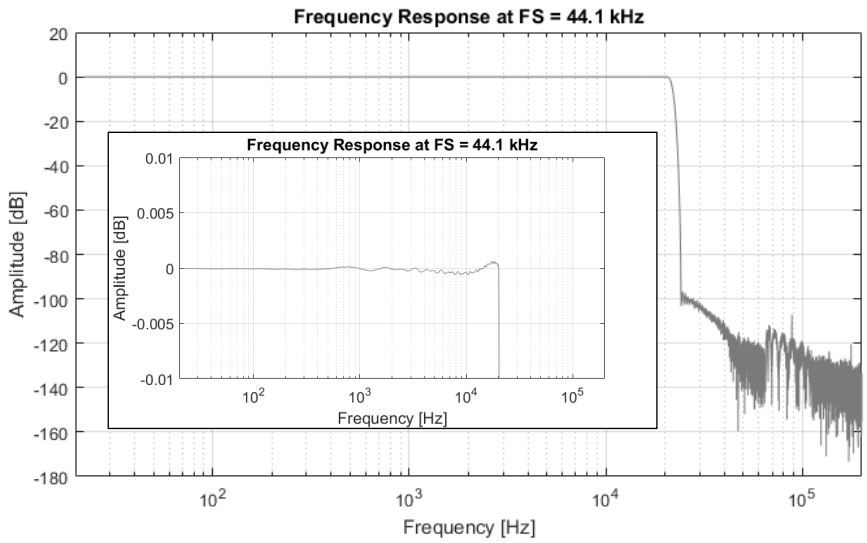
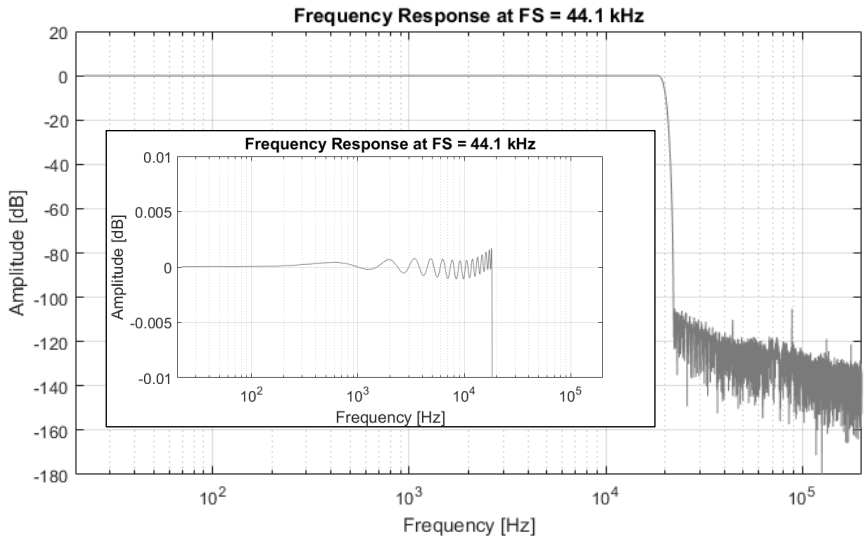
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.43FS	Hz
Stop band	-91dB	0.80FS			Hz
Group Delay		2.08/FS		3.56/FS	s
Flatness (ripple)					dB

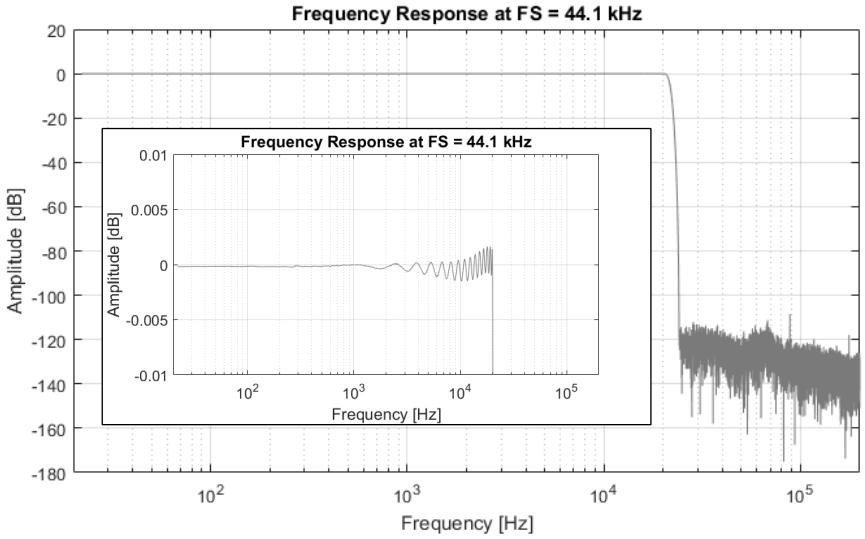
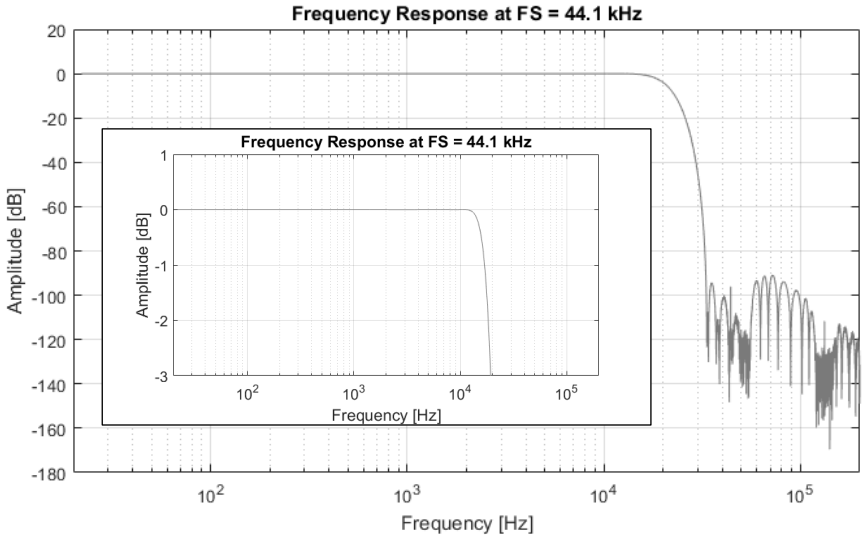
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.43FS	Hz
Stop band	-91dB	0.80FS			Hz
Group Delay		9.32/FS		9.93/FS	s
Flatness (ripple)					dB

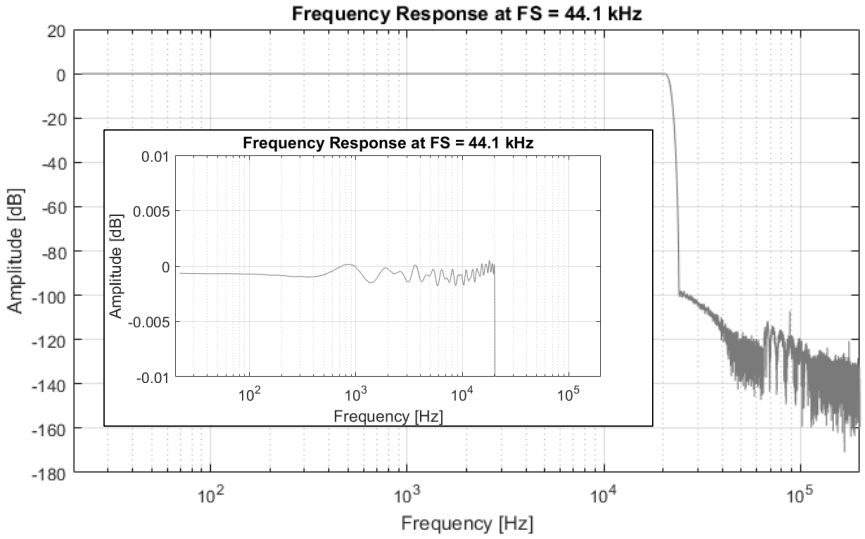
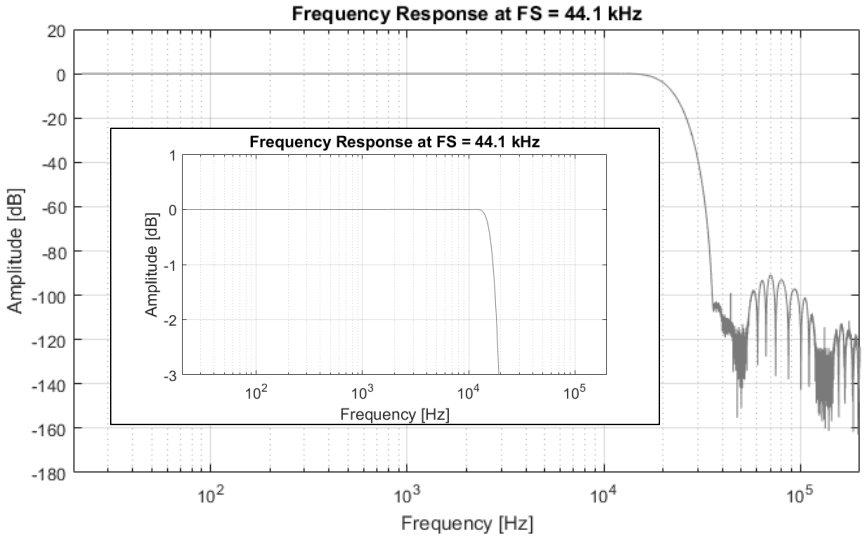
Table 12 - PCM Filter Properties

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing Fast Roll-Off	

Linear Phase Fast Roll-Off	
Linear Phase Slow Roll-Off	

Minimum Phase Fast Roll-Off	
Minimum Phase Slow Roll-Off	

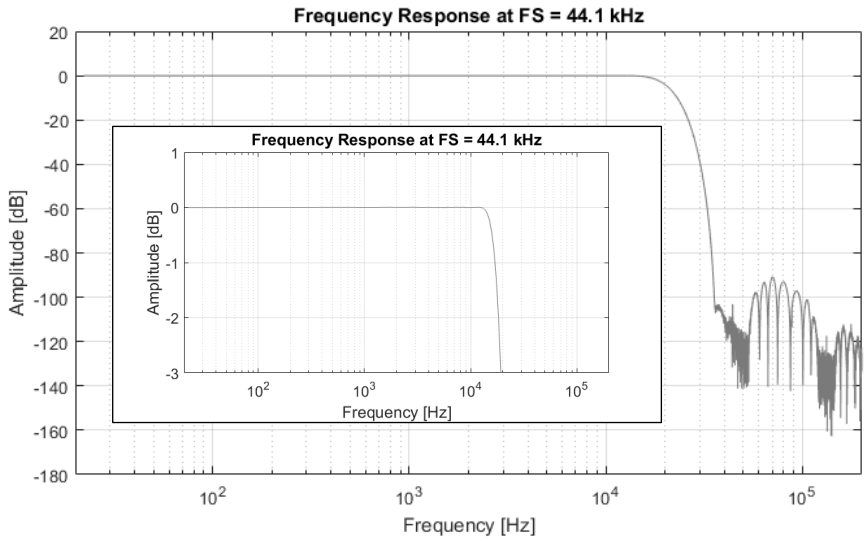
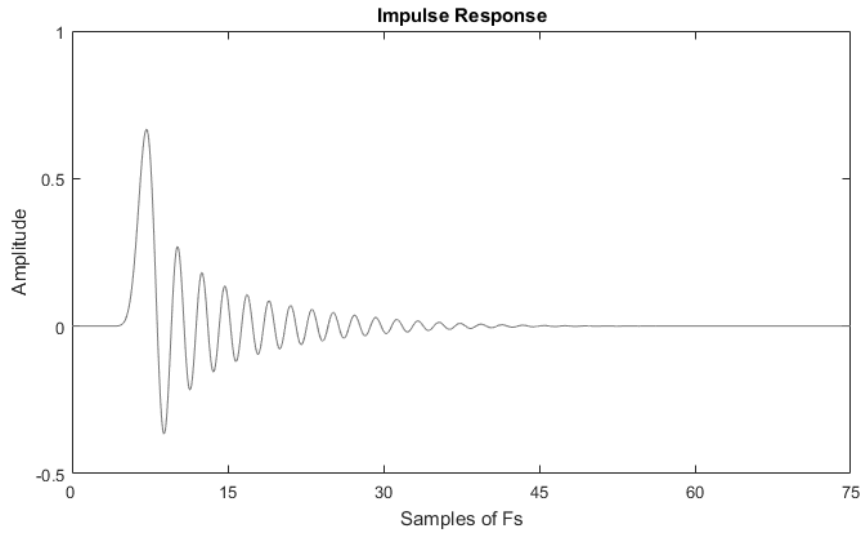
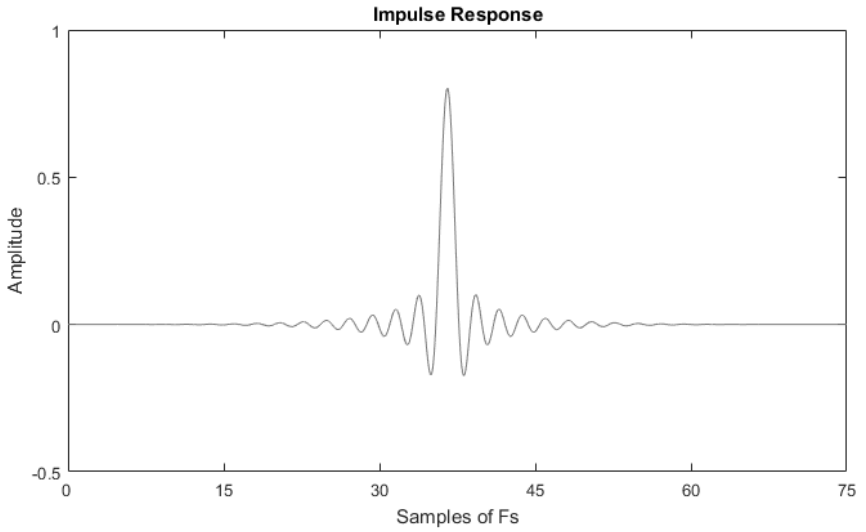
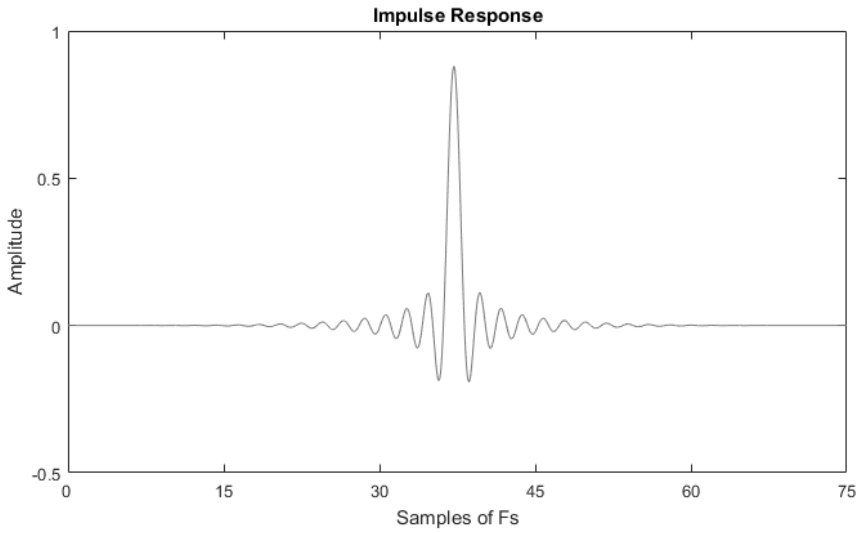
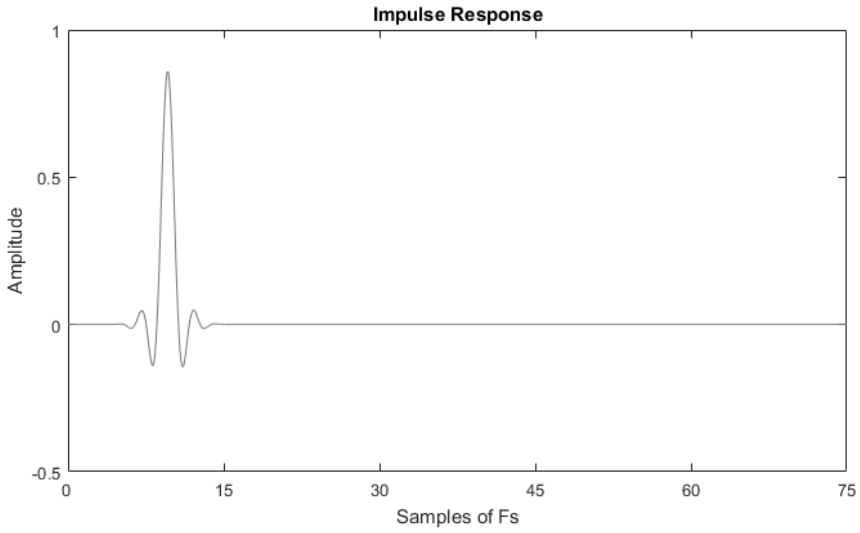
Minimum Phase Slow Roll-Off Low Dispersion	

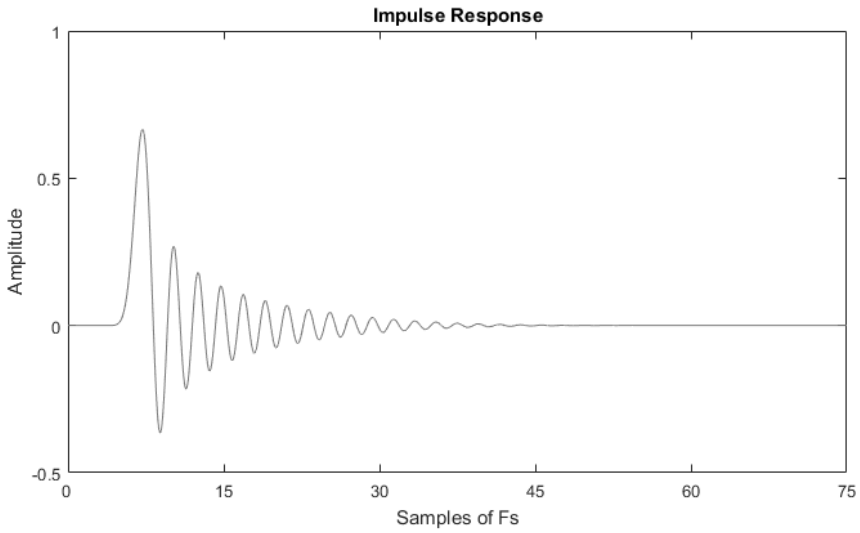
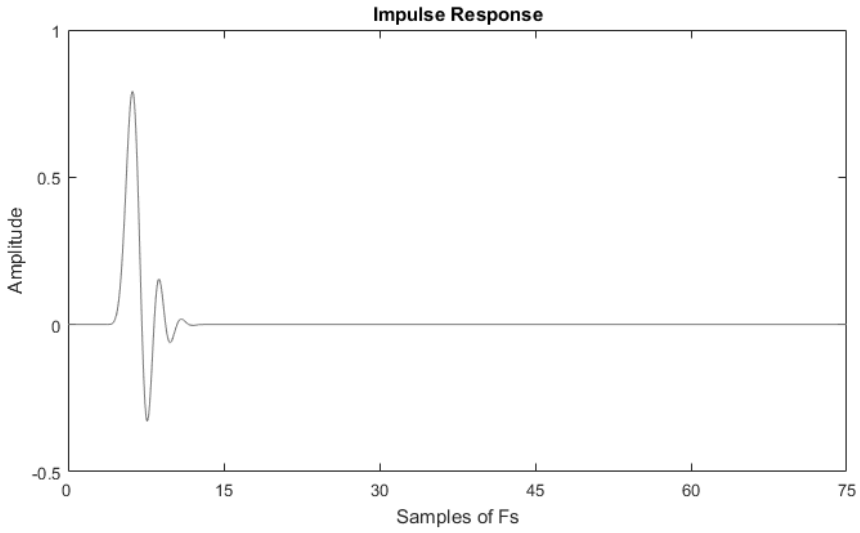
Table 13 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing Fast Roll-Off	

Linear Phase Fast Roll-Off	
Linear Phase Slow Roll-Off	

Minimum Phase Fast Roll-Off	
Minimum Phase Slow Roll-Off	

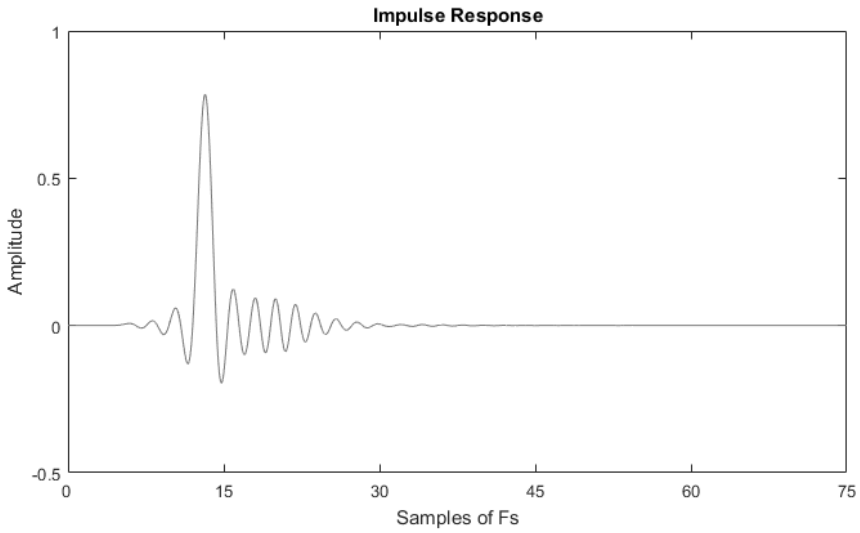
Minimum Phase Slow Roll-Off Low Dispersion	

Table 14 - PCM Filter Impulse Response

64FS Mode

64FS mode allows for PCM sample rates with an MCLK equal to 64*FS. This allows for support of 768kHz/705.6kHz sample rates with 49.152MHz/45.1584MHz MCLK, or 384kHz/352.8kHz sample rate with 24.576MHz/22.5792MHz MCLK.

64FS mode is supported in both software and hardware modes.

- AUTO_FS_DETECT will use 64FS mode if required.

Minimum Phase 64FS Latency

The following table shows the simulated latency at 705.6kHz sampling rate. The measurement was taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will scale with sample rate (FS).

Digital Filter	Delay(us) @ FS = 705.6 kHz
Minimum Phase Double Rate	8us

Table 15 - Minimum Phase 64FS Latency

Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.45FS	Hz
Stop band	-62dB	0.68FS			Hz
Group Delay		1.55/FS		2.35/FS	s
Flatness (ripple)					dB

Table 16 - Minimum Phase 64FS Properties

Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

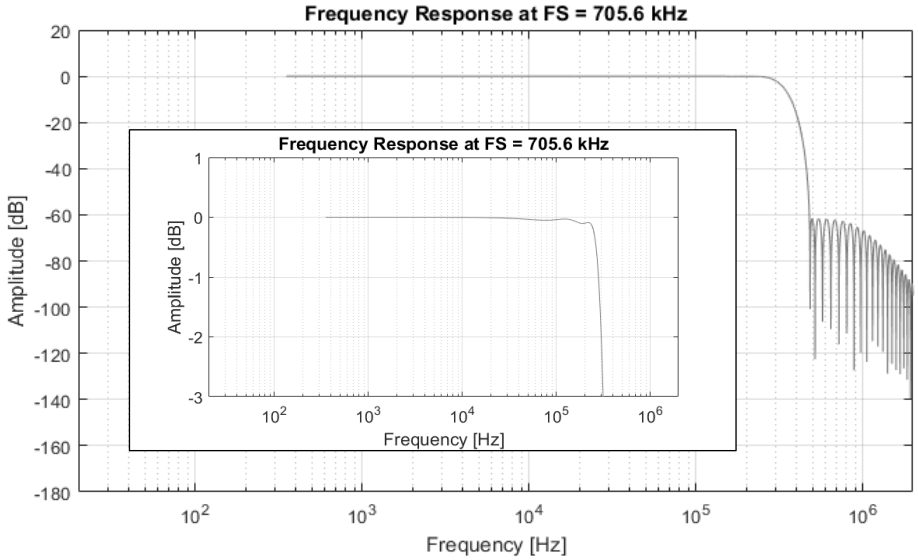


Figure 17 - Minimum Phase 64FS Frequency Response

Minimum Phase 64FS Impulse Response

The following impulse response was obtained from software simulations. It was measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream.

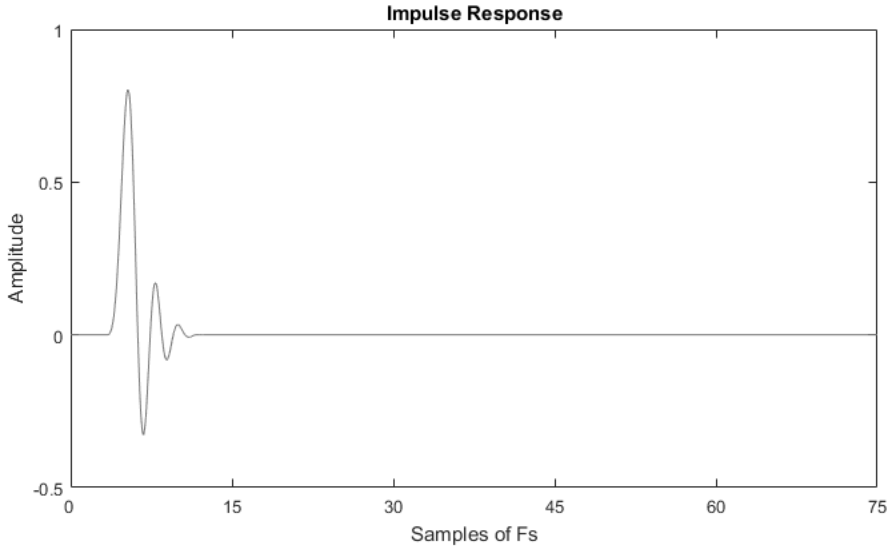


Figure 18 – Minimum Phase 64FS Impulse Response

Analog Features

Combining Channels

If 8 individual output channels are not required, ES9017 DACs can be combined to improve the performance per channel. For peak performance, it is recommended that channels are combined in an anti-phase approach as shown in Figure 19 - Example of Channel Combination for 4 Outputs.. In this way, DAC1 is connected to DAC3B, and DAC1B is connected to DAC3 to make one output channel. This method is extended to the other channels. Register 52: DAC_INVERT can be used to invert channels (3, 4, 7 and 8 in this example).

Combining channels in anti-phase allows for the effect of anti-phase summing, resulting in lower noise. Since register 52 must be set, it requires software mode. For combining channels in hardware mode, in-phase combination is recommended and will still improve performance per channel.

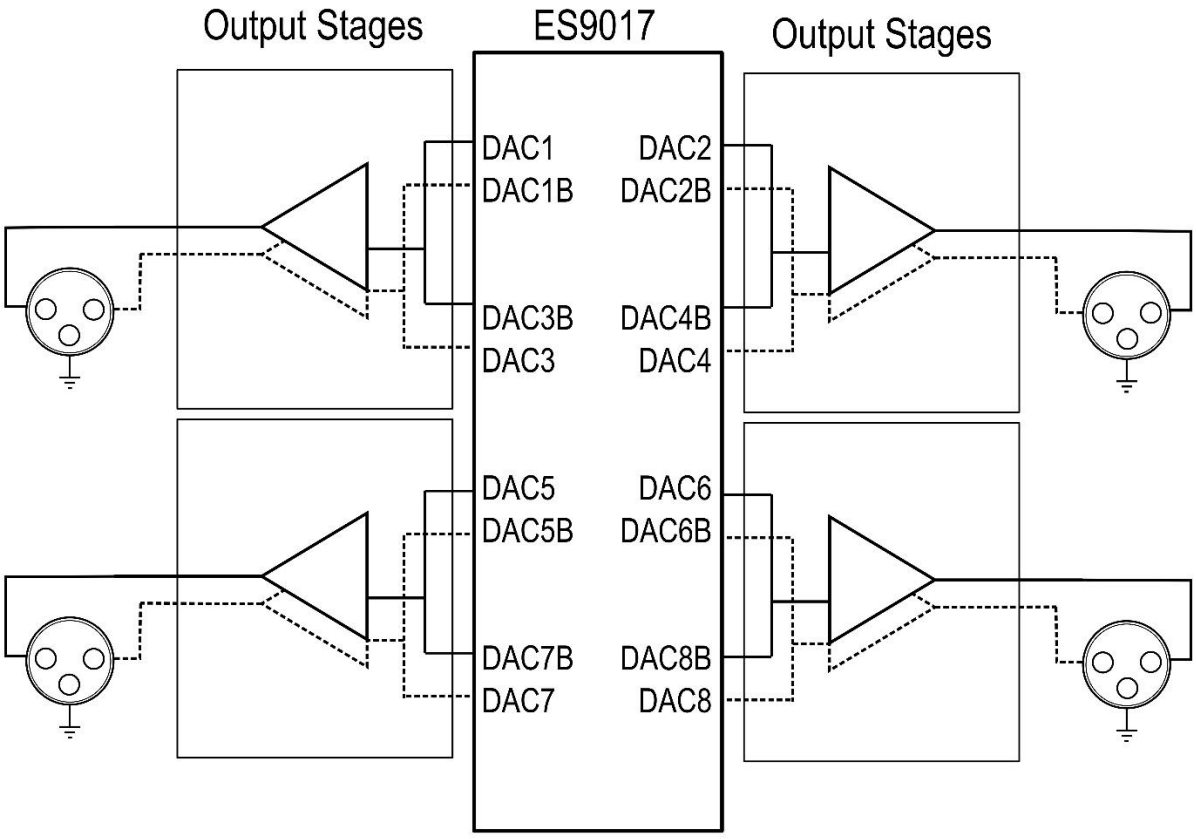


Figure 19 - Example of Channel Combination for 4 Outputs.

Calibration Resistor

ES9017 features a ~100kΩ calibration resistor accessible through GPIO3 (Pin 22) and terminated to ground as shown in Figure 18. **The calibration resistor is enabled by default but can be disabled with Register 13[6] CAL_RES_ENB =1.**

ESS's ES9312 features a calibration mode that can be paired with ES9017 to compensate AVCCL and AVCCR supplies. The ES9312 connects to the ES9017's integrated calibration resistor and adjusts the output supplies to maintain a tighter distribution on the output level in an application.

Note: The calibration resistor is only supported in software mode.

To access the calibration resistor through GPIO3, the following registers must be set upon initialization:

- Register 21[2] = 0 (default is 1)
- Register 63 = 0x03 (default is 0xC3)
- Register 65 = 0x14 (default is 0x95)

To use GPIO3 as a normal GPIO, disconnect the calibration resistor from GPIO3 by setting Register 13[6] CAL_RES_ENB =1 and set the GPIO CONFIG to desired setting. For using GPIO3 as a regular GPIO, the above registers still must be set.

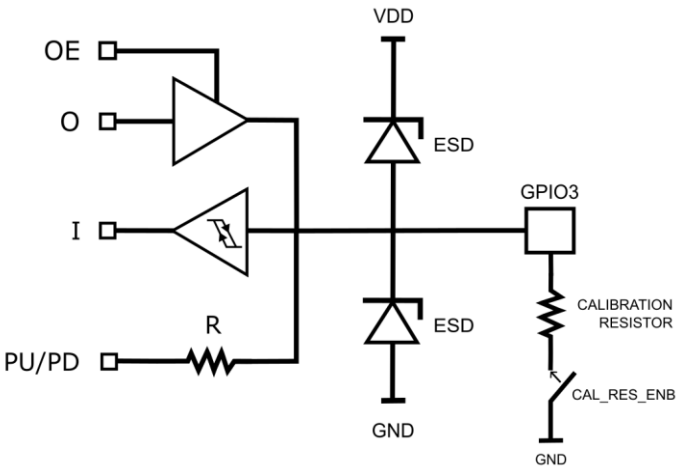


Figure 20 - GPIO3 Digital I/O with Calibration Resistor

Switching Characteristics

Parameter	Notes	Min.	Typ.	Max.	Unit
MCLK[1]					
Frequency		6.144	-	49.152	MHz
Duty Cycle		45	-	55	%
PCM Mode[2]					
WS Frequency (Word Select Clock)		8	-	MCLK/128	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	TDM_BIT_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
WS Frequency (Word Select Clock)	64FS Mode[3]	352.8	MCLK/64	768	kHz
BCLK Frequency (Bit Clock)		22.5792	MCLK	49.152	MHz
TDM Mode					
WS Frequency (Word Select Clock)	TDM4	8kHz	-	MCLK/128	kHz
	TDM8		-	MCLK/256	kHz
	TDM16		-	MCLK/512	kHz
	TDM32		-	MCLK/1024	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	(TDM_BIT_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
DSD Mode					
DSD Clock Frequency		2.8224	-	MCLK/2	MHz

Table 17 - Switching Characteristics

Notes:

1. MCLK must be synchronous to the digital serial audio clock.
2. In hardware mode, only 32bit word widths are supported for both PCM and TDM.
3. 64FS mode is for 705.6/768kHz with 45.1584/49.152MHz or 352.8/384kHz with 22.5792/24.576MHz.

Timing Characteristics

Bit-Clock (BCLK) and Word-Select (WS) Timing

Test Conditions 1 (unless otherwise noted)
TA = 25ºC, AVCC_R = AVCC_L = VCCA = AVDD = +3.3V, DVDD= +1.2V, fs = 48kHz, DAC enabled, 1kHz sine full scale.

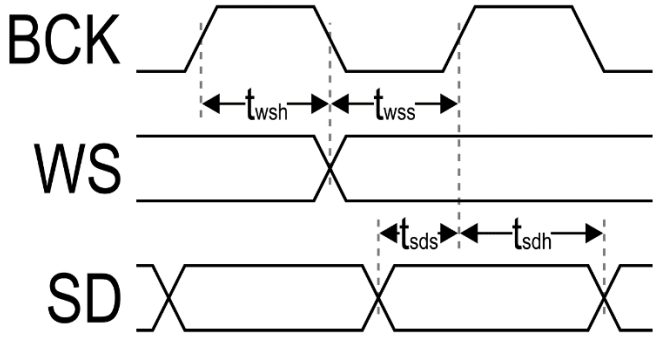


Figure 21 - Bit-Clock and Word-Select Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
WS hold time	t_{wsh}	0	-	-	ns
WS setup time	t_{wss}	2.6	-	-	ns
SD setup time	t_{sds}	2.8	-	-	ns
SD hold time	t_{sdh}	1.1	-	-	ns

Table 18 - Bit-Clock and Word-Select Timing Definitions

I²C Slave Interface Timing

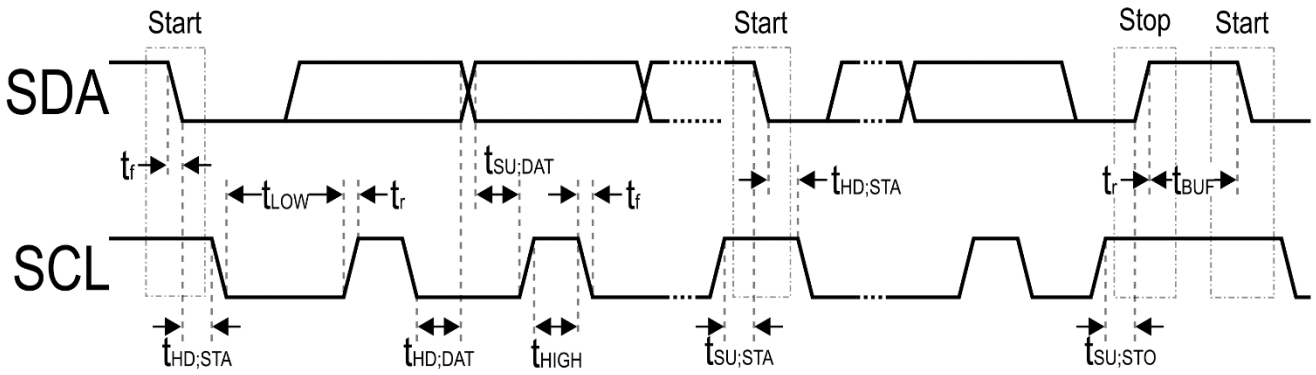


Figure 22 - I²C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000	-	300	ns
Fall time of SDA and SCL	t_f		-	300	-	300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 19 - I²C Slave/Synchronous Slave Interface Timing Definitions

SPI Slave Interface Timing

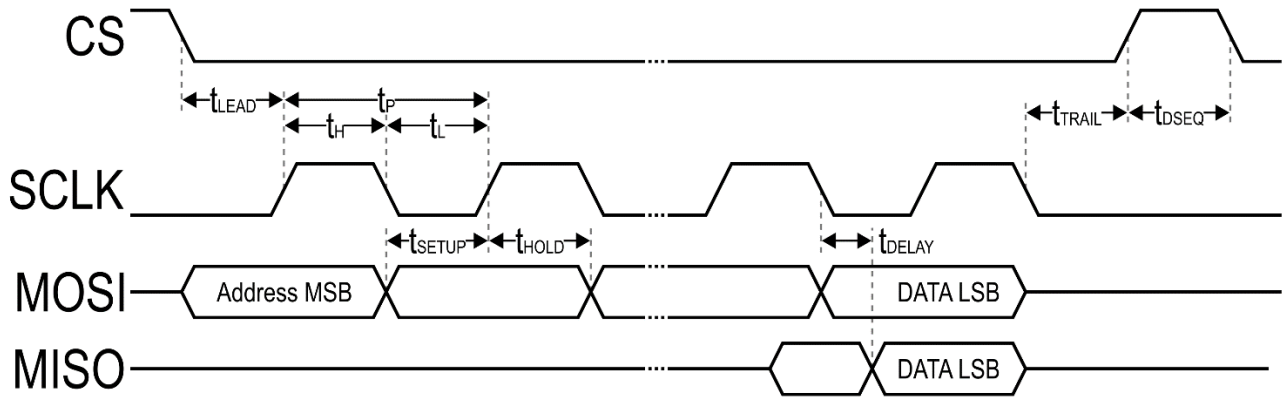


Figure 23 - SPI Slave Interface Timing

Parameter	Symbol	Min	Max	Unit
CS Lead Time (SCLK rising edge)	t_{LEAD}	4	-	ns
CS Trail Time (SCLK falling edge)	t_{TRAIL}	4	-	ns
MOSI Data Setup Time	t_{SETUP_MOSI}	-36	-	ns
MOSI Data Hold Time	t_{HOLD_MOSI}	60	-	ns
SCLK-MISO Delay Time	t_{DELAY_MISO}	-	74	ns
SCLK Period	t_{P_SCLK}	122	-	ns
SCLK High Pulse Duration	t_{H_SCLK}	94	-	ns
SCLK Low Pulse Duration	t_{L_SCLK}	60	-	ns
Sequential Transfer Delay	t_{DSEQ}	38	-	ns

Table 20 - SPI Slave Interface Timing Definitions

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_L • AVCC_R • AVDD • VCCA • DVDD	 • -0.3V to +3.8V with respect to ground • -0.3V to +3.8V with respect to ground • -0.3V to +3.7V with respect to ground • -0.3V to +3.7V with respect to ground • -0.3V to +1.4V with respect to ground
Storage Temperature	-65ºC to +150ºC
Operating Junction Temperature	+125ºC
Voltage Range for Digital Input Pins	-0.3V to AVDD (nom) + 0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2kV 500V

Table 21 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

I/O Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-level input voltage	VIH	(AVDD / 2) + 0.4		V
Low-level input voltage	VIL		0.4	V
High-level output voltage	VOH	AVDD – 0.2		V
Low-level output voltage	VOL		0.2	V

Table 22 - I/O Electrical Characteristics

Recommended Operating Conditions

AVCC_L and AVCC_R are the ES9017 voltage reference and supply, these are required to be low noise for the best performance. AVCC_L supplies the odd channels and AVCC_R supplies the even channels. AVDD is the digital I/O supply. VCCA is the analog power supply for the clock distribution and clock gearing. DVDD is a digital power supply for the digital core.

AVCC_L/AVCC_R are the references for the DACs and their voltage level will impact the DAC output voltage. To minimize the output voltage distribution, ESS recommends using the ES9312 in calibration mode with the ES9017.

Parameter	Symbol	Conditions
Operating temperature	T_A	–20°C to +85°C
AVCC_L[1]		3.3V ±15%
AVCC_R[1]		3.3V ±15%
AVDD		3.3V ±5%
VCCA		3.3V ±5%
DVDD		1.2V

Table 23 - Recommended Operating Conditions

Notes:

1. AVCC_L and AVCC_R can change up to ±15% when using the ES9312Q Voltage Regulator in Calibration Mode. The output voltage will change as the DAC's output impedance changes. See ES9312Q Datasheet for more information.

Power Consumption

Test Conditions 1 (unless otherwise noted)
TA = 25ºC, AVCC_R = AVCC_L = VCCA = AVDD = +3.3V, DVDD= +1.2V, fs = 48kHz, DAC enabled, 1kHz sine full scale.

Parameter	Min	Typ.	Max	Unit
Hardware Mode: 11 (Slave mode with ACG (128*FS), MCLK = 49.152MHz)				
AVCC_R		6.55		mA
AVCC_L		6.55		mA
VCCA		0.34		mA
AVDD		0.12		mA
DVDD		7.26		mA
Power Consumption		53.4		mW
Hardware Mode: 2 (Master mode with MCLK = 24.576MHz, FS=MCLK/512)				
AVCC_R		8.4		mA
AVCC_L		8.4		mA
VCCA		0.46		mA
AVDD		2.3		mA
DVDD		10.8		mA
Power Consumption		77.4		mW
Hardware Mode: 1 (Master mode with MCLK = 12.288MHz, FS=MCLK/256)				
AVCC_R		7.1		mA
AVCC_L		7.1		mA
VCCA		0.23		mA
AVDD		2.3		mA
DVDD		8.4		mA
Power Consumption		65.8		mW

Table 24 - Power Consumption with Test Condition 1

Test Conditions 2 (unless otherwise noted)
T_A = 25°C, AVCC_R = AVCC_L = VCCA = AVDD = +3.3V, DVDD= +1.2V, fs = 48kHz, DAC enabled, streaming zeros.

Parameter	Min	Typ.	Max	Unit
Hardware Mode: 11 (Slave mode with ACG (128*FS), MCLK = 49.152MHz)				
AVCC_R		0.6		mA
AVCC_L		0.6		mA
VCCA		0.4		mA
AVDD		0.2		mA
DVDD		2.6		mA
Power Consumption		9.1		mW
Hardware Mode: 2 (MCLK = 24.576MHz)				
AVCC_R		2.3		mA
AVCC_L		2.3		mA
VCCA		0.5		mA
AVDD		2.4		mA
DVDD		5.2		mA
Power Consumption		31.0		mW
Hardware Mode: 1 (MCLK = 12.288MHz)				
AVCC_R		1.1		mA
AVCC_L		1.1		mA
VCCA		0.3		mA
AVDD		2.4		mA
DVDD		3.5		mA
Power Consumption		20.4		mW

Table 25 - Power Consumption with Test Condition 2

Note: Automute is enabled. With automute disabled, power consumption is similar to Test Condition 1 with a full scale input.

Performance

Test Conditions 1 (unless otherwise noted)
T_A = 25°C, AVCC_R = AVCC_L = VCCA = AVDD = +3.3V, DVDD= +1.2V, fs = 48kHz, HW mode (I²S Master Mode)

Note: Performance numbers were measured using the ESS ES9017 1v1 evaluation board.

Parameter			Min	Typ.	Max	Unit
Resolution				32		Bit
Max MCLK frequency	Note: Synchronous clocks required				50	MHz
THD+N Ratio @ fs=48kHz (differential)	0dBFS BW=20Hz-20kHz			-110		dB
THD+N Ratio @ fs=96kHz (differential)	0dBFS BW=20Hz-40kHz			-108		dB
THD+N Ratio @ fs=192kHz (differential)	0dBFS BW=20Hz-80kHz			-106		dB
THD+N Ratio @ fs=384kHz (differential)	0dBFS BW=20Hz-160kHz			-104		dB
DNR (A-weighted) (8 ch mode – differential)	MCLK @ 49.152MHz	-60dBFS		120		dB
DNR (A-weighted) (Stereo mode – 4 ch sum diff)	MCLK @ 49.152MHz			124		dB
DNR (A-weighted) (Mono mode – 8 ch sum diff)	MCLK @ 49.152MHz			126		dB
Voltage output amplitude	Full-scale out			0.879 x AVCC		Vpp
Voltage output offset	Bipolar zero out			AVCC/2		V
Current output amplitude	Full-scale out			1000 x 0.879 x AVCC / Rdac		mApp
Current output offsets	Bipolar zero out			1000 x (AVCC/2 – Vg) / Rdac		mA
Output impedance (Per + or – pin of each differential DAC output pair)	R_{DAC}			1563 ± 15%		Ω

Table 26 - Performance Data

Power Up Sequence

During the power up sequence, the startup order of the ES9017 power supplies is not important as long as all power supply voltages and clock frequency (MCLK) are stable before CHIP_EN is set high.

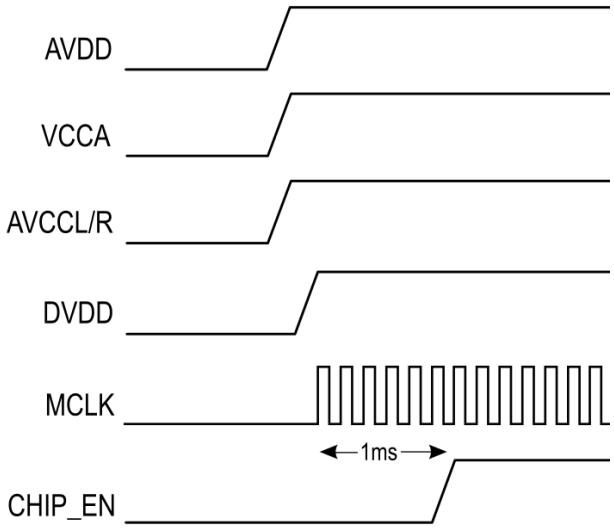


Figure 24 - Power up sequence

Power Down Sequence

During power down, CHIP_EN should be set low first. However, if power is lost before CHIP_EN is set low, no damage will occur.

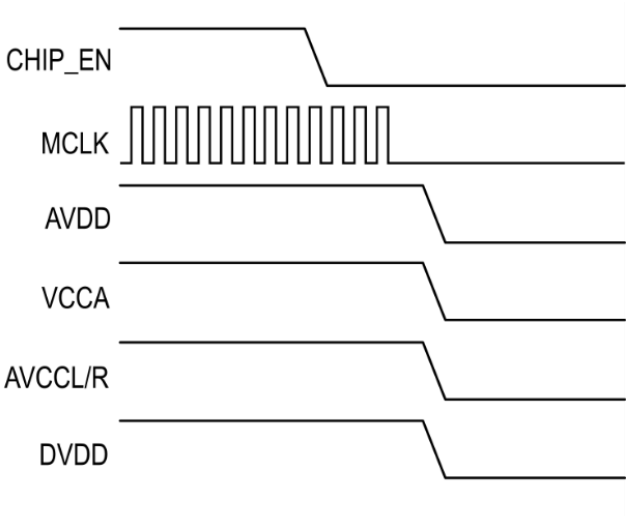


Figure 25 - Power down sequence

Register Overview

A system clock must be present to access registers.

Read/Write Register Addresses

Registers 0-65 (0x00 - 0x41) are read and write registers.

Read-Only Register Addresses

Register 224-251 (0xE0 - 0xE9) are read only registers.

Multi-Byte Registers

Multi-Byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-Byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYSTEM CONFIG	SOFT_RESET	ENABLE_64FS_MODE	RESERVED	ENABLE_DOP_DECODE	ENABLE_DSD_DECODE	ENABLE_TDM_DECODE	DAC_MODE_REG	RESERVED
0x01	1	SYS MODE CONFIG	RESERVED		ENABLE_DAC_CLK	ENABLE_NSMOD_CLK	RESERVED			
0x02	2	DAC CLOCK CONFIG	AUTO_FS_DETECT	SELECT_IDAC_HALF	SELECT_IDAC_NUM					
0x03	3	CLOCK CONFIG	MASTER_BCK_DIV							
0x04	4	CLK GEAR SELECT	RESERVED		SEL_CLK		RESERVED	AUTO_CLK_GEAR	RESERVED	
0x05-0x0C	5-12	RESERVED	RESERVED							
0x0D	13	DIGITAL AUTO CONTROL CONFIG	RESERVED	CAL_RES_ENB	RESERVED					
0x0E-0x0F	14-15	RESERVED	RESERVED							
0x10	16	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x11	17	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x12	18	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x13	19	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG			
0x14	20	GPIO OUTPUT ENABLE	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x15	21	GPIO INPUT	GPIO8_SDB	GPIO7_SDB	GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB
0x16	22	RESERVED	RESERVED							
0x17	23	GPIO OUTPUT LOGIC	GPIO_SEL		GPIO_OR_SS_RAMP	GPIO_OR_VOL_MIN	GPIO_OR_AUTOMUTE	GPIO_AND_SS_RAMP	GPIO_AND_VOL_MIN	GPIO_AND_AUTOMUTE
0x18	24		GPIO_DAC_MODE	RESERVED						GPIO_SEL
0x19	25	INPUT SELECTION	AUTO_CH_DETECT	ENABLE_DSD_FAULT_DETECT	DSD_MASTER_MODE	PCM_MASTER_MODE	RESERVED	INPUT_SEL		AUTO_INPUT_SEL
0x1A	26	SERIAL MASTER ENCODER CONFIG	TDM_RESYNC	BCK_INV	RESERVED	MASTER_FRAME_LENGTH		MASTER_WS_PULSE_MODE	MASTER_WS_INVERT	MASTER_BCK_INVERT
0x1B	27	TDM CONFIG	RESERVED		TDM_CH_NUM					
0x1C	28	TDM CONFIG1	TDM_LJ_MODE	TDM_VALID_EDGE	RESERVED					
0x1D	29	TDM CONFIG2	RESERVED	TDM_BIT_WIDTH	RESERVED					
0x1E	30	BCK/WS MONITOR CONFIG	DISABLE_DSD_DC	DISABLE_DSD_MUTE	ENABLE_WS_MONITOR	ENABLE_BCK_MONITOR	DISABLE_PCM_DC	RESERVED		
0x1F	31	RESERVED	RESERVED							
0x20	32	TDM CH1 CONFIG	RESERVED	TDM_CH1_LINE_SEL	TDM_CH1_SLOT_SEL					
0x21	33	TDM CH2 CONFIG	RESERVED	TDM_CH2_LINE_SEL	TDM_CH2_SLOT_SEL					
0x22	34	TDM CH3 CONFIG	RESERVED	TDM_CH3_LINE_SEL	TDM_CH3_SLOT_SEL					
0x23	35	TDM CH4 CONFIG	RESERVED	TDM_CH4_LINE_SEL	TDM_CH4_SLOT_SEL					
0x24	36	TDM CH5 CONFIG	RESERVED	TDM_CH5_LINE_SEL	TDM_CH5_SLOT_SEL					
0x25	37	TDM CH6 CONFIG	RESERVED	TDM_CH6_LINE_SEL	TDM_CH6_SLOT_SEL					
0x26	38	TDM CH7 CONFIG	RESERVED	TDM_CH7_LINE_SEL	TDM_CH7_SLOT_SEL					
0x27	39	TDM CH8 CONFIG	RESERVED	TDM_CH8_LINE_SEL	TDM_CH8_SLOT_SEL					
0x28	40	VOLUME1	VOLUME1							
0x29	41	VOLUME2	VOLUME2							
0x2A	42	VOLUME3	VOLUME3							
0x2B	43	VOLUME4	VOLUME4							
0x2C	44	VOLUME5	VOLUME5							
0x2D	45	VOLUME6	VOLUME6							
0x2E	46	VOLUME7	VOLUME7							
0x2F	47	VOLUME8	VOLUME8							
0x30	48	DAC VOL UP RATE	DAC_VOL_RATE_UP							
0x31	49	DAC VOL DOWN RATE	DAC_VOL_RATE_DOWN							
0x32	50	DAC VOL DOWN RATE FAST	DAC_VOL_RATE_FAST							
0x33	51	DAC MUTE	DAC_MUTE_CH8	DAC_MUTE_CH7	DAC_MUTE_CH6	DAC_MUTE_CH5	DAC_MUTE_CH4	DAC_MUTE_CH3	DAC_MUTE_CH2	DAC_MUTE_CH1
0x34	52	DAC INVERT	DAC_INVERT_CH8	DAC_INVERT_CH7	DAC_INVERT_CH6	DAC_INVERT_CH5	DAC_INVERT_CH4	DAC_INVERT_CH3	DAC_INVERT_CH2	DAC_INVERT_CH1
0x35	53	FILTER SHAPE	RESERVED					FILTER_SHAPE		
0x36	54	IIR BANDWIDTH	RESERVED				VOLUME_HOLD	IIR_BW		
0x37	55	DAC PATH CONFIG	RESERVED						BYPASS_FIR4X	BYPASS_FIR2X
0x38	56	AUTOMUTE ENABLE	AUTOMUTE_EN_CH8	AUTOMUTE_EN_CH7	AUTOMUTE_EN_CH6	AUTOMUTE_EN_CH5	AUTOMUTE_EN_CH4	AUTOMUTE_EN_CH3	AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x39	57	AUTOMUTE TIME	AUTOMUTE_TIME							
0x3A	58		RESERVED				AUTOMUTE_RAMP_TO_GROUND	AUTOMUTE_TIME		
0x3B	59	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x3C	60		AUTOMUTE_LEVEL							
0x3D	61	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x3E	62		AUTOMUTE_OFF_LEVEL							
0x3F	63	SOFT RAMP CONFIG	GPIO3_FUNC_OR	GPIO3_FUNC_SET1	RESERVED	SOFT_RAMP_TIME				
0x40	64	RESERVED	RESERVED							
0x41	65	GPIO3 FUNC and DITHER CONTROL	GPIO3_FUNC_SET2	RESERVED			DITHER_SETTING			
0xE0	224	SYS READ	RESERVED				MODES		ADDR1	ADDR0
0xE1	225	CHIP ID READ	CHIP_ID							

0xE2-0xE4	226-228	RESERVED	RESERVED			
0xE5	229	RATIO VALID READ	RATIO_VALID	RESERVED		
0xE6	230	INPUT READBACK	RESERVED	TDM_DATA_VALID	DOP_VALID	INPUT_SELECT_OVERRIDE
0xE7-0xE9	231-233	RESERVED	RESERVED			

Table 27 - Register Map

Register Listing

Some reserved registers values might be asserted in default mode. This is normal and does not need to be changed.

System Registers

Register 0: SYSTEM CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs a soft reset to the digital core • 1'b0: Normal operation • 1'b1: Reset digital core (all settings are set to default)
[6]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: 64FS mode disabled (default) • 1'b1: 64FS mode enabled Note: This mode is required for high sample rates (i.e., 705.6/768 kHz)
[5]	RESERVED	NA
[4]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	ENABLE_TDM_DECODE	Enables TDM decoding. • 1'b0: Disabled • 1'b1: Enabled (default)
[1]	DAC_MODE_REG	Enables DAC data path • 1'b0: DAC disabled (default) • 1'b1: DAC enabled
[0]	RESERVED	NA

Register 1: SYS MODE CONFIG

Bits	[7:6]	[5]	[4]	[3:0]
Default	2'b00	1'b1	1'b1	4'b1000

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5]	ENABLE_DAC_CLK	Enables DAC interpolation path clock. • 1'b0: Clock disabled • 1'b1: Clock enabled (default)
[4]	ENABLE_NSMOD_CLK	Enables clock to DAC
[3:0]	RESERVED	NA

Register 2: DAC CLOCK CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b1	1'b0	6'd0

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT	• 1'b0: Disabled • 1'b1: Auto tune MCLK/CLK_IDAC ratio according to detected FS (default)
[6]	SELECT_IDAC_HALF	• 1'b0: Divide by SELECT_IDAC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_IDAC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_IDAC_NUM	CLK_IDAC divider. Whole number divide value + 1 for CLK_IDAC (SYS_CLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd1: Whole number divide value + 1 = 2 • 6'd63: Whole number divide value + 1 = 64

Register 3: CLOCK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_BCK_DIV	Master mode clock divider. Whole number divide value + 1 for CLK_Master (SYS_CLK/divide_value).

Register 4: CLK GEAR SELECT

Bits	[7:6]	[5:4]	[3]	[2]	[1:0]
Default	2'b00	2'd0	1'b0	1'b0	2'b00

Bits	Mnemonic	Description
[7:6]	RESERVED	NA
[5:4]	SEL_CLK	Clock Gearing • 2'd0: SYS_CLK/1 • 2'd1: SYS_CLK/2 • 2'd2: SYS_CLK/4 • 2'd3: SYS_CLK/8
[3]	RESERVED	NA
[2]	AUTO_CLK_GEAR	• 1'b0: Disable automatic clock gearing. SEL_CLK = sel_clk_reg • 1'b1: Enable automatic clock gearing. SEL_CLK will increase up to sel_clk_reg
[1:0]	RESERVED	NA

Register 12-5: RESERVED

Register 13: DIGITAL AUTO CONTROL CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b1	1'b0	6'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	CAL_RES_ENB	Selects the calibration resistor connection on GPIO3 • 1'b0: DAC calibration resistor enabled (default) • 1'b1: DAC calibration resistor disabled
[5:0]	RESERVED	NA

Register 14-15: RESERVED

GPIO Registers

Register 16: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd13

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configures GPIO2 • 4'd0: Analog shutdown — shutdown (default) • 4'd1: Output 0 — output • 4'd2: Output 1 — output • 4'd3: CLK_IDAC — output • 4'd4: Reserved • 4'd5: Mute all channels — input • 4'd6: System mode control — input • 4'd7: Reserved • 4'd8: CLKEN_1FS — output • 4'd9: TDM_VALID — output • 4'd10: DOP_VALID — output • 4'd11: BCK_WS_FAIL — output • 4'd12: Minimum Volume — output • 4'd13: Automute Status — output • 4'd14: Soft Ramp Finished — output • 4'd15: Reserved
[3:0]	GPIO1_CFG	Configures GPIO1 • 4'd0: Analog shutdown — shutdown • 4'd1: Output 0 — output • 4'd2: Output 1 — output • 4'd3: CLK_IDAC — output • 4'd4: Reserved • 4'd5: Mute all channels — input • 4'd6: System mode control — input • 4'd7: Reserved • 4'd8: CLKEN_1FS — output • 4'd9: TDM_VALID — output • 4'd10: DOP_VALID — output • 4'd11: BCK_WS_FAIL — output • 4'd12: Minimum Volume — output • 4'd13: Automute Status — output (default) • 4'd14: Soft Ramp Finished — output • 4'd15: Reserved

Register 17: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configures GPIO4 • 4'd0: Analog shutdown — shutdown (default) • 4'd1: Output 0 — output • 4'd2: Output 1 — output • 4'd3: CLK_IDAC — output • 4'd4: Reserved • 4'd5: Mute all channels — input • 4'd6: System mode control — input • 4'd7: Reserved • 4'd8: CLKEN_1FS — output • 4'd9: TDM_VALID — output • 4'd10: DOP_VALID — output • 4'd11: BCK_WS_FAIL — output • 4'd12: Minimum Volume — output • 4'd13: Automute Status — output • 4'd14: Soft Ramp Finished — output • 4'd15: Reserved
[3:0]	GPIO3_CFG	Configures GPIO3 • 4'd0: Analog shutdown — shutdown (default) • 4'd1: Output 0 — output • 4'd2: Output 1 — output • 4'd3: CLK_IDAC — output • 4'd4: Reserved • 4'd5: Mute all channels — input • 4'd6: System mode control — input • 4'd7: Reserved • 4'd8: CLKEN_1FS — output • 4'd9: TDM_VALID — output • 4'd10: DOP_VALID — output • 4'd11: BCK_WS_FAIL — output • 4'd12: Minimum Volume — output • 4'd13: Automute Status — output • 4'd14: Soft Ramp Finished — output • 4'd15: Reserved

Register 18: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configures GPIO6 • 4'd0: Analog shutdown — shutdown (default) • 4'd1: Output 0 — output • 4'd2: Output 1 — output • 4'd3: CLK_IDAC — output • 4'd4: Reserved • 4'd5: Mute all channels — input • 4'd6: System mode control — input • 4'd7: Reserved • 4'd8: CLKEN_1FS — output • 4'd9: TDM_VALID — output • 4'd10: DOP_VALID — output • 4'd11: BCK_WS_FAIL — output • 4'd12: Minimum Volume — output • 4'd13: Automute Status — output • 4'd14: Soft Ramp Finished — output • 4'd15: Reserved
[3:0]	GPIO5_CFG	Configures GPIO5 • 4'd0: Analog shutdown — shutdown (default) • 4'd1: Output 0 — output • 4'd2: Output 1 — output • 4'd3: CLK_IDAC — output • 4'd4: Reserved • 4'd5: Mute all channels — input • 4'd6: System mode control — input • 4'd7: Reserved • 4'd8: CLKEN_1FS — output • 4'd9: TDM_VALID — output • 4'd10: DOP_VALID — output • 4'd11: BCK_WS_FAIL — output • 4'd12: Minimum Volume — output • 4'd13: Automute Status — output • 4'd14: Soft Ramp Finished — output • 4'd15: Reserved

Register 19: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO8_CFG	Configures GPIO8 • 4'd0: Analog shutdown — shutdown (default) • 4'd1: Output 0 — output • 4'd2: Output 1 — output • 4'd3: CLK_IDAC — output • 4'd4: Reserved • 4'd5: Mute all channels — input • 4'd6: System mode control — input • 4'd7: Reserved • 4'd8: CLKEN_1FS — output • 4'd9: TDM_VALID — output • 4'd10: DOP_VALID — output • 4'd11: BCK_WS_FAIL — output • 4'd12: Minimum Volume — output • 4'd13: Automute Status — output • 4'd14: Soft Ramp Finished — output • 4'd15: Reserved
[3:0]	GPIO7_CFG	Configures GPIO7 • 4'd0: Analog shutdown — shutdown (default) • 4'd1: Output 0 — output • 4'd2: Output 1 — output • 4'd3: CLK_IDAC — output • 4'd4: Reserved • 4'd5: Mute all channels — input • 4'd6: System mode control — input • 4'd7: Reserved • 4'd8: CLKEN_1FS — output • 4'd9: TDM_VALID — output • 4'd10: DOP_VALID — output • 4'd11: BCK_WS_FAIL — output • 4'd12: Minimum Volume — output • 4'd13: Automute Status — output • 4'd14: Soft Ramp Finished — output • 4'd15: Reserved

Register 20: GPIO OUTPUT ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	GPIO8_OE	GPIO8 output control. • 1'b0: Tristate GPIO8 (default) • 1'b1: GPIO8 Output Enable
[6]	GPIO7_OE	GPIO7 output control. • 1'b0: Tristate GPIO7 (default) • 1'b1: GPIO7 Output Enable
[5]	GPIO6_OE	GPIO6 output control. • 1'b0: Tristate GPIO6 (default) • 1'b1: GPIO6 Output Enable
[4]	GPIO5_OE	GPIO5 output control. • 1'b0: Tristate GPIO5 (default) • 1'b1: GPIO5 Output Enable
[3]	GPIO4_OE	GPIO4 output control. • 1'b0: Tristate GPIO4 (default) • 1'b1: GPIO4 Output Enable
[2]	GPIO3_OE	GPIO3 output control. • 1'b0: Tristate GPIO3 (default) • 1'b1: GPIO3 Output Enable
[1]	GPIO2_OE	GPIO2 output control. • 1'b0: Tristate GPIO2 (default) • 1'b1: GPIO2 Output Enable
[0]	GPIO1_OE	GPIO1 output control. • 1'b0: Tristate GPIO1 • 1'b1: GPIO1 Output Enable (default)

Register 21: GPIO INPUT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_SDB	GPIO8 input control. • 1'b0: Disables GPIO8 input (default) • 1'b1: Enables GPIO8 input
[6]	GPIO7_SDB	GPIO7 input control. • 1'b0: Disables GPIO7 input (default) • 1'b1: Enables GPIO7 input
[5]	GPIO6_SDB	GPIO6 input control. • 1'b0: Disables GPIO6 input (default) • 1'b1: Enables GPIO6 input
[4]	GPIO5_SDB	GPIO5 input control. • 1'b0: Disables GPIO5 input • 1'b1: Enables GPIO5 input (default)
[3]	GPIO4_SDB	GPIO4 input control. • 1'b0: Disables GPIO4 input • 1'b1: Enables GPIO4 input (default)
[2]	GPIO3_SDB	GPIO3 input control. • 1'b0: Disables GPIO3 input • 1'b1: Enables GPIO3 input (default)
[1]	GPIO2_SDB	GPIO2 input control. • 1'b0: Disables GPIO2 input (default) • 1'b1: Enables GPIO2 input
[0]	GPIO1_SDB	GPIO1 input control. • 1'b0: Disables GPIO1 input (default) • 1'b1: Enables GPIO1 input

Register 22: RESERVED

Register 24-23: GPIO OUTPUT LOGIC

Bits	[15]	[14:9]	[8:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	6'd0	3'd0	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[15]	GPIO_DAC_MODE	When any GPIOx_CFG = 6 (System mode control): • 1'b0: Power down when GPIO input is 1 • 1'b1: HIFI when GPIO input is 1 (when GPIO input is 0, system mode is determined by register DAC_MODE_REG (register 0, bit[1]))
[14:9]	RESERVED	NA
[8:6]	GPIO_SEL	When GPIOx_CFG = 12, 13 or 14, and the corresponding GPIO_AND and GPIO_OR are not set: • 3'd0: Outputs status/flag from ch1 • 3'd1: Outputs status/flag from ch2 • 3'd2: Outputs status/flag from ch3 • 3'd3: Outputs status/flag from ch4 • 3'd4: Outputs status/flag from ch5 • 3'd5: Outputs status/flag from ch6 • 3'd6: Outputs status/flag from ch7 • 3'd7: Outputs status/flag from ch8
[5]	GPIO_OR_SS_RAMP	When GPIOx_CFG = 14 (Soft Ramp Finished flag): • 1'b0: The Soft ramp Finished flag is determined by GPIO_AND_SS_RAMP and GPIO_SEL (default) • 1'b1: The Soft Ramp Finished flag is the "OR" of all 8ch Soft Ramp Finished flags
[4]	GPIO_OR_VOL_MIN	When GPIOx_CFG = 12 (Minimum Volume flag): • 1'b0: The Minimum Volume flag is determined by GPIO_AND_VOL_MIN and GPIO_SEL (default) • 1'b1: The Minimum Volume flag is the "OR" of all 8ch Minimum Volume flags
[3]	GPIO_OR_AUTOMUTE	When GPIOx_CFG = 13 (Automute Status): • 1'b0: The Automute Status is determined by GPIO_AND_AUTOMUTE and GPIO_SEL (default) • 1'b1: The Automute Status is the "OR" of all 8ch Automute Status
[2]	GPIO_AND_SS_RAMP	When GPIOx_CFG = 14 (Soft Ramp Finished flag) and GPIO_OR_SS_RAMP is not set: • 1'b0: The Soft Ramp Finished flag is from a single channel selected by GPIO_SEL • 1'b1: The Soft Ramp Finished flag is the "AND" of all 8ch Soft Ramp Finished flags (default)

[1]	GPIO_AND_VOL_MIN	When GPIOx_CFG = 12 (Minimum Volume flag) and GPIO_OR_VOL_MIN is not set: • 1'b0: The Minimum Volume flag is from a single channel selected by GPIO_SEL • 1'b1: The Minimum Volume flag is the "AND" of all 8ch Minimum Volume flags (default)
[0]	GPIO_AND_AUTOMUTE	When GPIOx_CFG = 13 (Automute Status) and GPIO_OR_AUTOMUTE is not set: • 1'b0: The Automute Status is from a single channel selected by GPIO_SEL • 1'b1: The Automute Status is the "AND" of all 8ch Automute Status (default)

DAC Registers

Register 25: INPUT SELECTION

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b0	1'b1	1'b0	1'b0	1'b0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Auto detect BCK/FRAME ratio to determine the number of TDM channels • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_DSD_FAULT_DETECT	• 1'b0: Disabled • 1'b1: Enabled (default)
[5]	DSD_MASTER_MODE	DSD master mode config. • 1'b0: DSD slave mode (default) • 1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK
[4]	PCM_MASTER_MODE	PCM master mode config. • 1'b0: PCM slave mode (default) • 1'b1: PCM master mode enabled. Master BCK and WS output from DATA_CLK and DATA1
[3]	RESERVED	NA
[2:1]	INPUT_SEL	Selects input data when AUTO_INPUT_SELECT is disabled. • 2'd0: TDM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: Reserved
[0]	AUTO_INPUT_SEL	Automatic input data selection config. • 1'b0: Disables auto input select. Input data format is set by INPUT_SEL (default) • 1'b1: Automatically determine the input data format.

Register 26: SERIAL MASTER ENCODER CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM decoder to resync. • 1'b0: Let decoder sync (default) • 1'b1: Force decoder not sync
[6]	BCK_INV	Invert the slave BCK • 1'b0: Normal operation • 1'b1: Invert slave BCK
[5]	RESERVED	NA
[4:3]	MASTER_FRAME_LENGTH	Selects the bit length in each TDM channel in master mode. • 2'd0: 32-bit (default) • 2'd1: 24-bit • 2'd2: 16-bit • 2'd3: Reserved
[2]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_BCK_INVERT	Inverts master BCK or DSD_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)

Register 27: TDM CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	NA
[4:0]	TDM_CH_NUM	Total number of TDM slots per frame = TDM_CH_NUM + 1.

Register 28: TDM CONFIG1

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'd0

Bits	Mnemonic	Description
[7]	TDM_LJ_MODE	TDM LJ mode. • 1'b0: Standard I²S (default) • 1'b1: LJ mode
[6]	TDM_VALID_EDGE	TDM WS valid edge. • 1'b0: negative edge (default) • 1'b1: positive edge
[5:0]	RESERVED	NA

Register 29: TDM CONFIG2

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'b00	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_BIT_WIDTH	Bit width of each TDM slot. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit • 2'b11: Reserved
[4:0]	RESERVED	NA

Register 30: BCK/WS MONITOR CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:0]
Default	1'b0	1'b0	1'b1	1'b1	1'b0	3'd0

Bits	Mnemonic	Description
[7]	DISABLE_DSD_DC	• 1'b0: DSD DC can trigger an automute if automute is enabled (default) • 1'b1: DSD DC is ignored.
[6]	DISABLE_DSD_MUTE	• 1'b0: DSD mute pattern can trigger an automute is automute is enabled (default) • 1'b1: DSD mute pattern is ignored.
[5]	ENABLE_WS_MONITOR	Enable WS monitor. • 1'b0: Disable • 1'b1: Enable (default)
[4]	ENABLE_BCK_MONITOR	Enable BCK monitor. • 1'b0: Disable • 1'b1: Enable (default)
[3]	DISABLE_PCM_DC	• 1'b0: PCM DC signal can trigger an automute if automute is enabled. • 1'b1: PCM DC is ignored.
[2:0]	RESERVED	NA

Register 31: RESERVED

Register 32: TDM CH1 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH1_LINE_SEL	CH1 data line selection, only valid for TDM, PCM and DoP. CH1 receives data from: • 2'd0: DATA2 (default) • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5
[4:0]	TDM_CH1_SLOT_SEL	CH1 data slot selection. CH1 receives data from the selected slot. Selected Slot = TDM_CH1_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 33: TDM CH2 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH2_LINE_SEL	CH2 data line selection, only valid for TDM, PCM and DoP. CH2 receives data from: • 2'd0: DATA2 (default) • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5
[4:0]	TDM_CH2_SLOT_SEL	CH2 data slot selection. CH2 receives data from the selected slot. Selected Slot = TDM_CH2_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 34: TDM CH3 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd1	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH3_LINE_SEL	CH3 data line selection, only valid for TDM, PCM and DoP. CH3 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 (default) • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5
[4:0]	TDM_CH3_SLOT_SEL	CH3 data slot selection. CH3 receives data from the selected slot. Selected Slot = TDM_CH3_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 35: TDM CH4 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd1	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH4_LINE_SEL	CH4 data line selection, only valid for TDM, PCM and DoP. CH4 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 (default) • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5
[4:0]	TDM_CH4_SLOT_SEL	CH4 data slot selection. CH4 receives data from the selected slot. Selected Slot = TDM_CH4_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 36: TDM CH5 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd2	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH5_LINE_SEL	CH5 data line selection, only valid for TDM, PCM and DoP. CH5 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 (default) • 2'd3: DATA5/GPIO5
[4:0]	TDM_CH5_SLOT_SEL	CH5 data slot selection. CH5 receives data from the selected slot. Selected Slot = TDM_CH5_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 37: TDM CH6 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd2	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH6_LINE_SEL	CH6 data line selection, only valid for TDM, PCM and DoP. CH6 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 (default) • 2'd3: DATA5/GPIO5
[4:0]	TDM_CH6_SLOT_SEL	CH6 data slot selection. CH6 receives data from the selected slot. Selected Slot = TDM_CH6_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 38: TDM CH7 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd3	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH7_LINE_SEL	CH7 data line selection, only valid for TDM, PCM and DoP. CH7 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5 (default)
[4:0]	TDM_CH7_SLOT_SEL	CH7 data slot selection. CH7 receives data from the selected slot. Selected Slot = TDM_CH7_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 39: TDM CH8 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd3	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6:5]	TDM_CH8_LINE_SEL	CH8 data line selection, only valid for TDM, PCM and DoP. CH8 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5 (default)
[4:0]	TDM_CH8_SLOT_SEL	CH8 data slot selection. CH8 receives data from the selected slot. Selected Slot = TDM_CH8_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 40: VOLUME1

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME1	DAC ch1 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 41: VOLUME2

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME2	DAC ch2 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 42: VOLUME3

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME3	DAC ch3 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 43: VOLUME4

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME4	DAC ch4 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 44: VOLUME5

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME5	DAC ch5 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 45: VOLUME6

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME6	DAC ch6 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 46: VOLUME7

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME7	DAC ch7 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 47: VOLUME8

Bits	[7:0]
Default	8'd0

Bits	Mnemonic	Description
[7:0]	VOLUME8	DAC ch8 volume. -0dB to -127.5dB 0.5dB steps. • 8'd0: 0dB • 8'd255: -127.5dB

Register 48: DAC VOL UP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_UP	Value by which the old VOLUME value is incremented to reach the new VOLUME value: $\text{ramp\_rate [dB/s]} = 20\log_{10}\left(\frac{\text{DAC\_VOL\_RATE\_UP} \cdot FS}{2^{12}}\right)$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 49: DAC VOL DOWN RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_DOWN	Value by which the old VOLUME value is incremented to reach the new VOLUME value $\text{ramp\_rate [dB/s]} = 20\log_{10}\left(\frac{\text{DAC\_VOL\_RATE\_DOWN} \cdot FS}{2^{12}}\right)$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default • 8'hFF: Fastest change

Register 50: DAC VOL DOWN RATE FAST

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_FAST	Value by which the old VOLUME value is incremented to reach the new VOLUME value Only used during abnormal mute (BCK_WS ratio failed) $\text{ramp\_rate [dB/s]} = 20\log_{10}\left(\frac{\text{DAC\_VOL\_RATE\_FAST} \cdot FS}{2^{12}}\right)$ • 8'h00: Instant change • 8'h01: Slowest change • 8'hFF: Fastest change (default)

Register 51: DAC MUTE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_MUTE_CH8	• 1'b0: Normal operation (default) • 1'b1: Mute ch8
[6]	DAC_MUTE_CH7	• 1'b0: Normal operation (default) • 1'b1: Mute ch7
[5]	DAC_MUTE_CH6	• 1'b0: Normal operation (default) • 1'b1: Mute ch6
[4]	DAC_MUTE_CH5	• 1'b0: Normal operation (default) • 1'b1: Mute ch5
[3]	DAC_MUTE_CH4	• 1'b0: Normal operation (default) • 1'b1: Mute ch4
[2]	DAC_MUTE_CH3	• 1'b0: Normal operation (default) • 1'b1: Mute ch3
[1]	DAC_MUTE_CH2	• 1'b0: Normal operation (default) • 1'b1: Mute ch2
[0]	DAC_MUTE_CH1	• 1'b0: Normal operation (default) • 1'b1: Mute ch1

Register 52: DAC INVERT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_INVERT_CH8	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch8, OUT/OUTB are phase inverted
[6]	DAC_INVERT_CH7	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch7, OUT/OUTB are phase inverted
[5]	DAC_INVERT_CH6	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch6, OUT/OUTB are phase inverted
[4]	DAC_INVERT_CH5	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch5, OUT/OUTB are phase inverted
[3]	DAC_INVERT_CH4	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch4, OUT/OUTB are phase inverted
[2]	DAC_INVERT_CH3	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch3, OUT/OUTB are phase inverted
[1]	DAC_INVERT_CH2	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch2, OUT/OUTB are phase inverted
[0]	DAC_INVERT_CH1	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch1, OUT/OUTB are phase inverted

Register 53: FILTER SHAPE

Bits	[7:3]	[2:0]
Default	5'd23	3'd0

Bits	Mnemonic	Description
[7:3]	RESERVED	NA
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 54: IIR BANDWIDTH

Bits	[7:4]	[3]	[2:0]
Default	4'd0	1'b0	3'd4

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3]	VOLUME_HOLD	Hold volume coefficients to allow for all channels to update at same time
[2:0]	IIR_BW	Controls the IIR bandwidth in the digital datapath. • 3'd0: Reserved • 3'd1: BW * 8 • 3'd2: BW * 4 • 3'd3: BW * 2 • 3'd4: BW (default) • 3'd5: BW / 2 • 3'd6: BW / 4 • 3'd7: BW / 8

Register 55: DAC PATH CONFIG

Bits	[7:2]	[1]	[0]
Default	6'b000000	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	NA
[1]	BYPASS_FIR4X	• 1'b0: Non-bypass IFir_4x (default) • 1'b1: Bypass IFir_4x
[0]	BYPASS_FIR2X	• 1'b0: Non-bypass IFir_2x (default) • 1'b1: Bypass IFir_2x

Register 56: AUTOMUTE ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	AUTOMUTE_EN_CH8	• 1'b0: Disables ch8 automute • 1'b1: Enables ch8 automute (default) Note: Automute is available for PCM only
[6]	AUTOMUTE_EN_CH7	• 1'b0: Disables ch7 automute • 1'b1: Enables ch7 automute (default) Note: Automute is available for PCM only
[5]	AUTOMUTE_EN_CH6	• 1'b0: Disables ch6 automute • 1'b1: Enables ch6 automute (default) Note: Automute is available for PCM only
[4]	AUTOMUTE_EN_CH5	• 1'b0: Disables ch5 automute • 1'b1: Enables ch5 automute (default) Note: Automute is available for PCM only
[3]	AUTOMUTE_EN_CH4	• 1'b0: Disables ch4 automute • 1'b1: Enables ch4 automute (default) Note: Automute is available for PCM only
[2]	AUTOMUTE_EN_CH3	• 1'b0: Disables ch3 automute • 1'b1: Enables ch3 automute (default) Note: Automute is available for PCM only
[1]	AUTOMUTE_EN_CH2	• 1'b0: Disables ch2 automute • 1'b1: Enables ch2 automute (default) Note: Automute is available for PCM only
[0]	AUTOMUTE_EN_CH1	• 1'b0: Disables ch1 automute • 1'b1: Enables ch1 automute (default) Note: Automute is available for PCM only

Register 58-57: AUTOMUTE TIME

Bits	[15:12]	[11]	[10:0]
Default	4'd0	1'b1	11'h00F

Bits	Mnemonic	Description
[15:12]	RESERVED	NA
[11]	AUTOMUTE_RAMP_TO_GROUND	• 1'b0: When ramped to min volume during normal mute, do not soft ramp to ground • 1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default) normal mute includes: automute, mute by register, mute by GPIO
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. • 11'h000: Disabled • 11'h001: Slowest • 11'h00F: Default • 11'h7FF: Fastest $Time(s) = 2^{18}/(AUTOMUTE\_TIME * FS)$

Register 60-59: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'h0008

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	The threshold which the audio must be below before an automute condition is flagged. • 16'h0001: -138dB • 16'h0008: -120dB (default) • 16'hFFFF: -42dB Note: this register works in tandem with AUTOMUTE_TIME to create the automute condition. $level[db] = 20 * log10\left(AUTOMUTE\_LEVEL/\left((2^{16}-1) * 2^{7}\right)\right)$

Register 62-61: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'h000A

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	The threshold which the audio must be above before the automute condition is immediately cleared. • 16'h0001: -138dB • 16'h000A: -118dB (default) • 16'hFFFF: -42dB $level[db] = 20 * log10\left(AUTOMUTE\_OFF\_LEVEL/\left((2^{16}-1)*2^{7}\right)\right)$

Register 63: SOFT RAMP CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'b1	1'b1	1'b0	5'd3

Bits	Mnemonic	Description
[7]	GPIO3_FUNC_OR	GPIO3 defaults as a non-customer special function which must be set to 0. In hardware mode, it is done by grounding GPIO3, in software mode the user must set GPIO3_FUNC_OR, GPIO3_FUNC_SET1 and GPIO3_FUNC_SET2 to 0. • 1'b0: Disable GPIO3 function. • 1'b1: GPIO3 function override (default).
[6]	GPIO3_FUNC_SET1	• 1'b0: Disable GPIO3 function setting option 1. • 1'b1: GPIO3 function setting option 1 (default).
[5]	RESERVED	NA
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 20 (inclusive). $Time[s] = 4096 * \left(2^{(SOFT\_RAMP\_TIME+1)}\right)/CLK\_IDAC[Hz]$

Register 64: RESERVED

Register 65: GPIO3 FUNC and DITHER CONTROL

Bits	[7]	[6:4]	[3:0]
Default	1'b1	3'b001	4'd5

Bits	Mnemonic	Description
[7]	GPIO3_FUNC_SET2	GPIO3 defaults as a special function which must be set to 0. In hardware mode it is done by grounding GPIO3, in software mode the user must set GPIO3_FUNC_OR, GPIO3_FUNC_SET1 and GPIO3_FUNC_SET2 to 0. • 1'b0: Disable GPIO3 function setting option 2. • 1'b1: GPIO3 function setting option 2 (default).
[6:4]	RESERVED	NA
[3:0]	DITHER_SETTING	Required to be set to 4'd4 only for using the calibration resistor (see section), otherwise leave at default value of 4'd5. All other values are reserved.

Readback Registers

Register 224: SYS READ

Bits	[7:4]	[3:2]	[1]	[0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	NA
[3:2]	MODES	Chip mode readback. Based on MODE Pin • 2'd0: I²C • 2'd3: SPI Note: All other values are invalid.
[1]	ADDR1	I²C address select bit 1.
[0]	ADDR0	I²C address select bit 0.

Register 225: CHIP ID READ

Bits	[7:0]
Default	8'h60

Bits	Mnemonic	Description
[7:0]	CHIP_ID	Chip ID. • ES9017: 0x60

Register 228-226: RESERVED

Register 229: RATIO VALID READ

Bits	[7]	[6:0]
Default	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	Indicates validity of the MCLK/CLK_IDAC ratio • 1'b0: Invalid • 1'b1: Valid
[6:0]	RESERVED	NA

Register 230: INPUT READBACK

Bits	[7]	[6]	[5:2]	[1:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	RESERVED	NA
[6]	TDM_DATA_VALID	TDM valid data flag
[5:2]	DOP_VALID	DoP valid flag
[1:0]	INPUT_SELECT_OVERRIDE	AUTO_INPUT_SEL value

Register 233-231: RESERVED

ES9017 Reference Schematics

Hardware (HW) Mode

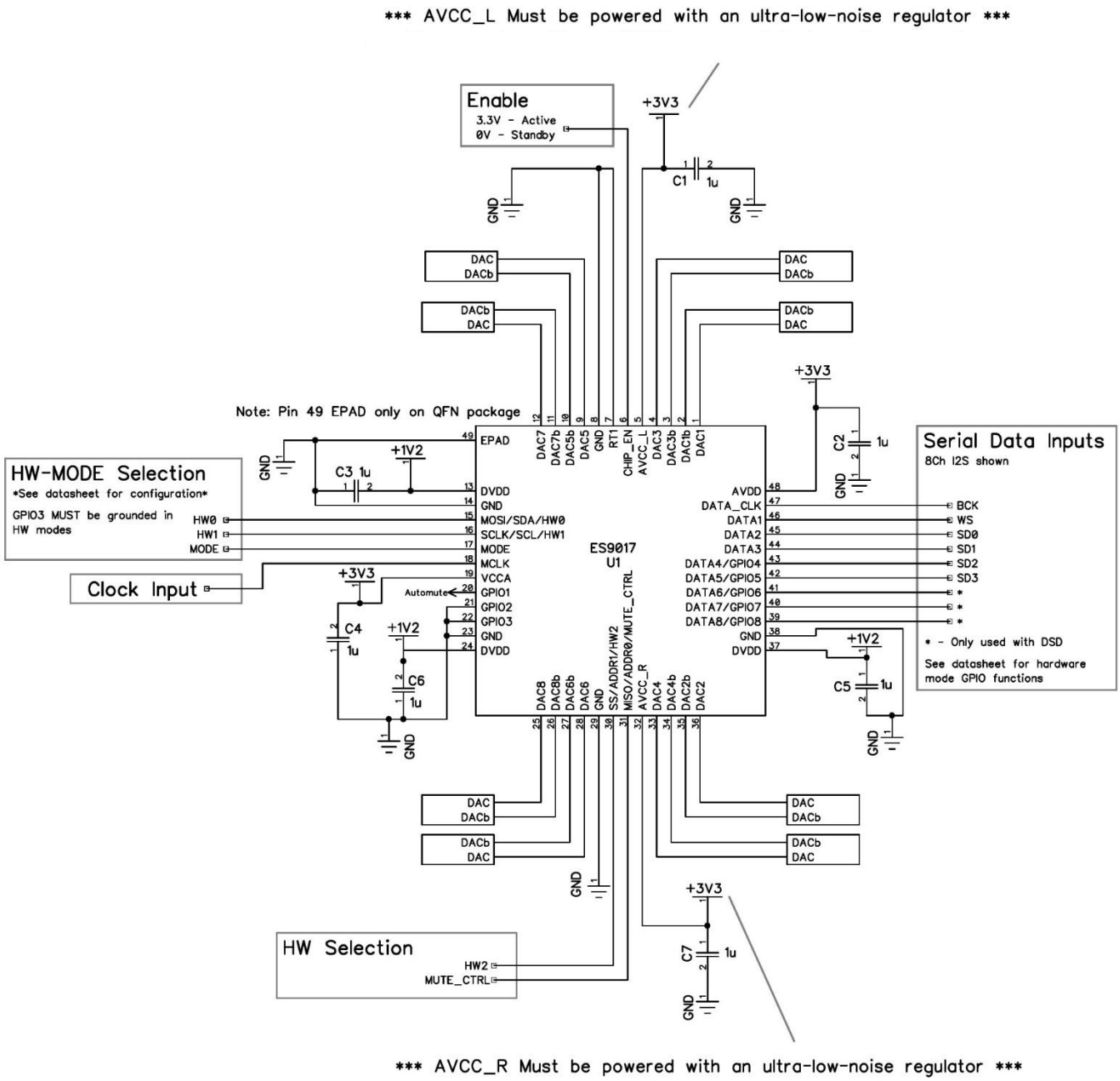


Figure 26 - ES9017Q Hardware Mode Reference Schematic

Note: ES9017Q has an exposed pad (EPAD, Pin 49) and should be grounded. ES9017S does not have an exposed pad.

Software (SW) Mode

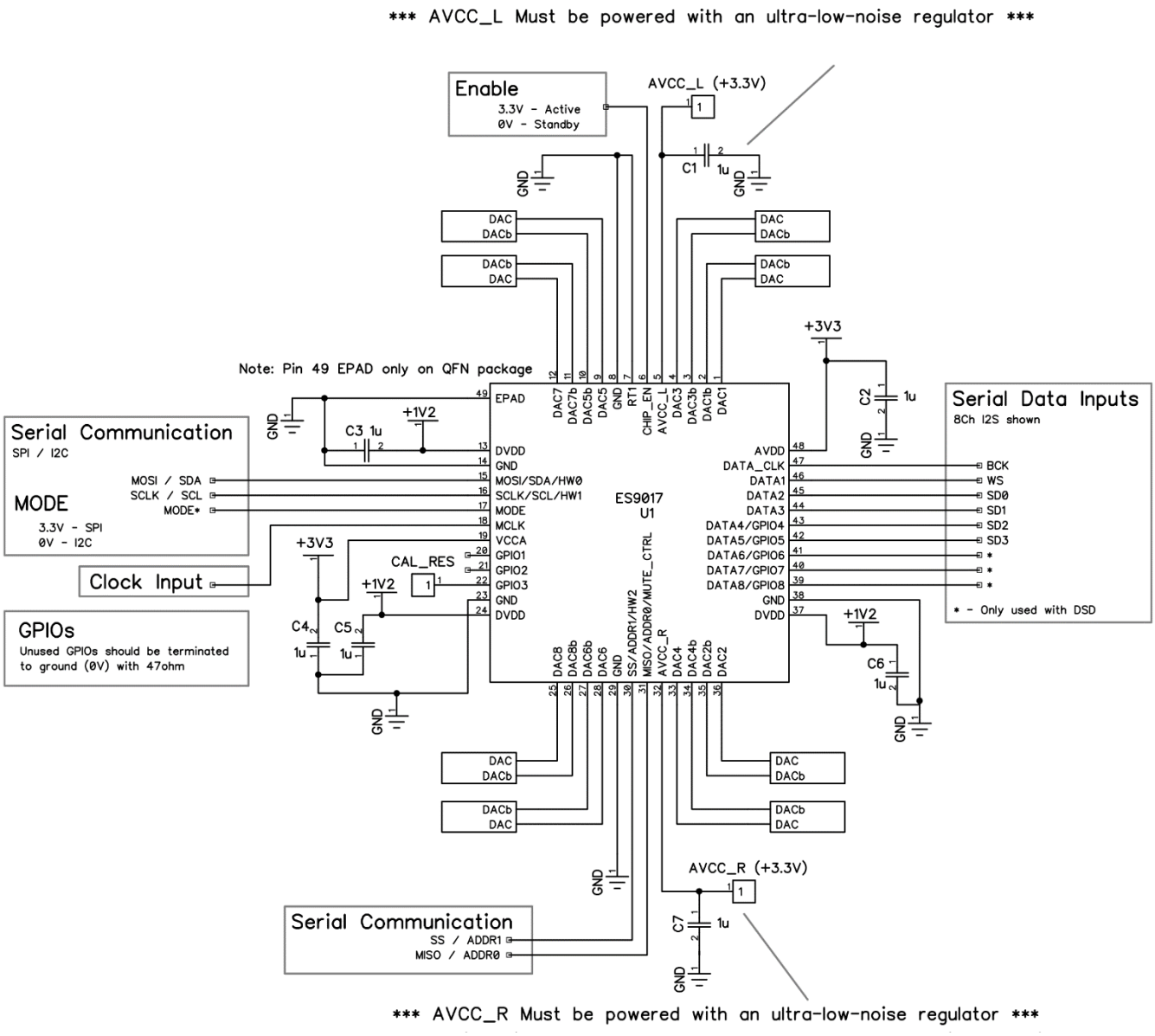


Figure 27 - ES9017Q Software Mode Reference Schematic

Note: ES9017Q has an exposed pad (EPAD, Pin 49) and should be grounded. ES9017S does not have an exposed pad.

Recommended Output Stage

The recommended output stage provides both a balanced output and a ground-centered single-ended output, optimized for low noise and low distortion. The gain of this output stage is determined by the value of the feedback resistor R94, R97, and the output impedance, R_{DAC}.

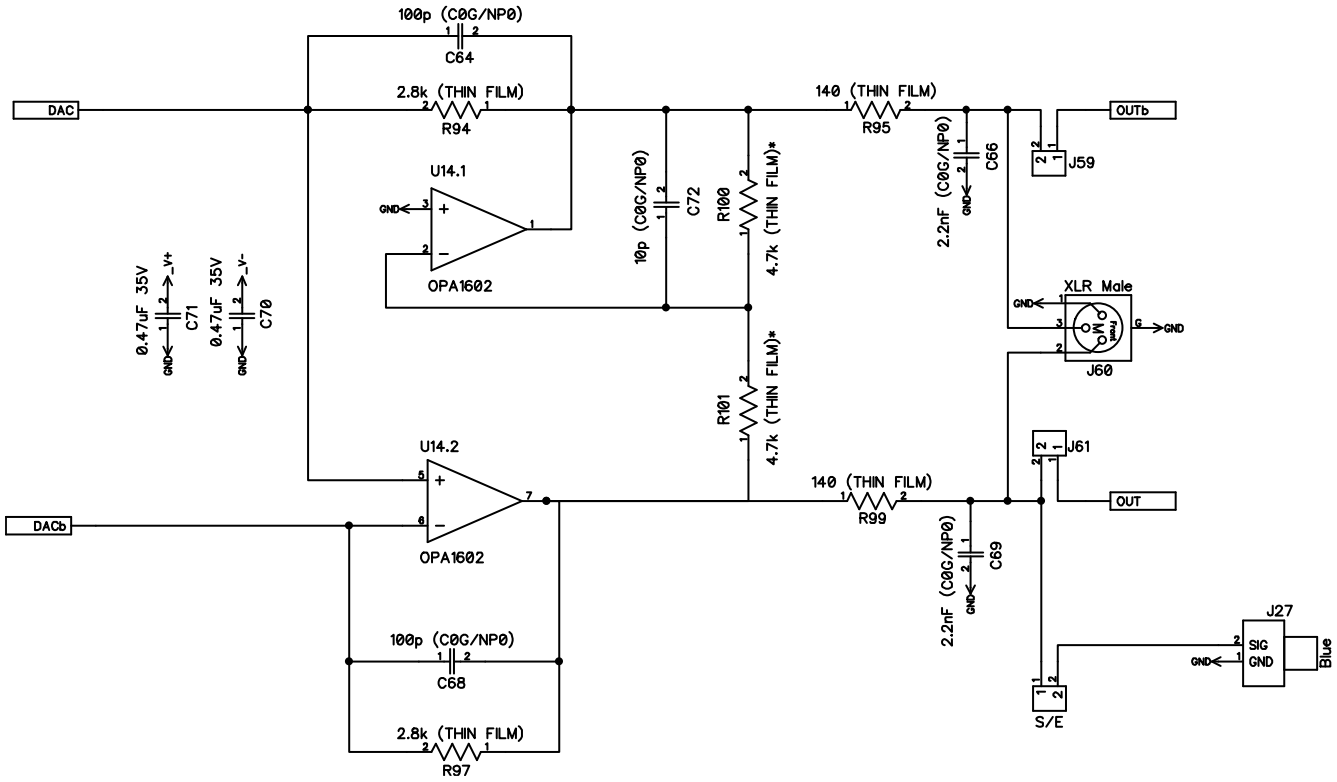


Figure 28 - ES9017 Output Stage Schematic

Note: Schematic is representative of ES9017 1v2 EVB. See EVB manual for more details.

Recommended Power Supply

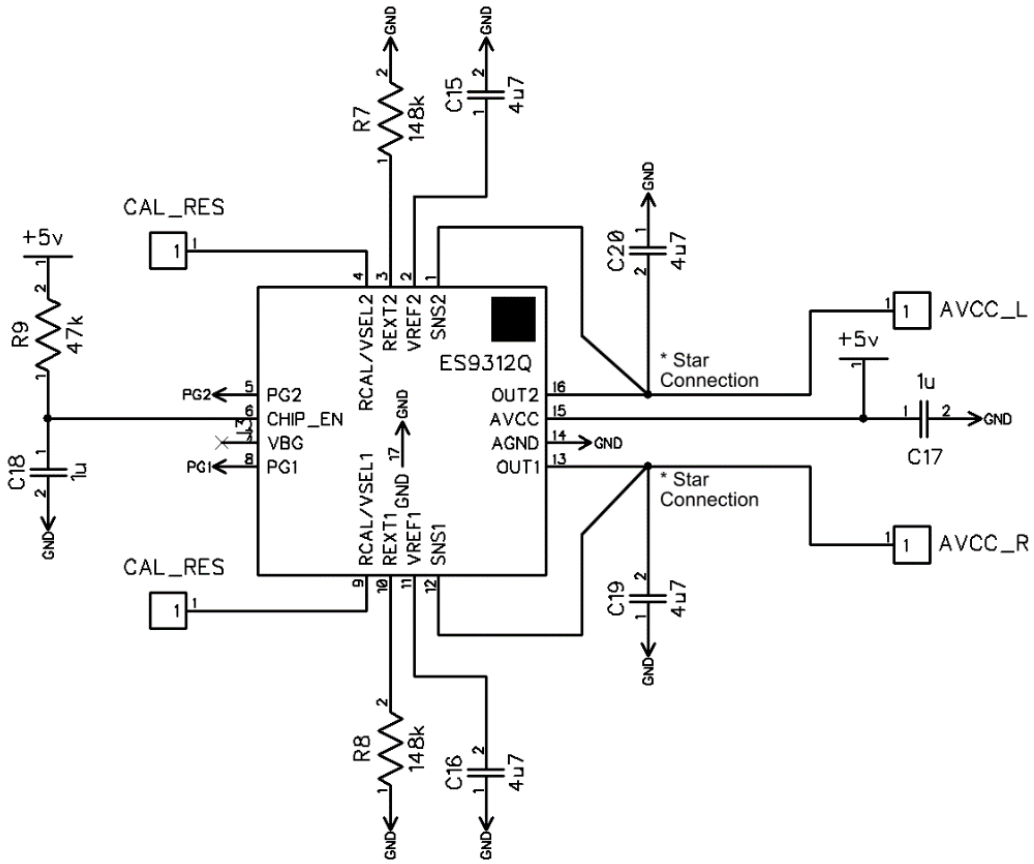


Figure 29 - ES9017 Power Supply Schematic

Note: In all configurations V_{BG} must remain floating. SNSx and OUTx pins need to be star connected to 4.7uF capacitors which are located close to ES9312.

Recommended PCB Layout Guidelines

To maximize performance of the ES9017 ESS Technology makes the following PCB Layout recommendations:

1. Use of a 4+ layer PCB with an uninterrupted ground plane immediately beneath the chip. Both analog and digital ground signal can be connected here.
2. All bypass capacitors to be placed as close to the chip as possible while keeping clear ground paths between them and the chip's ground pins.
3. The use of multiple vias for each supply near its bypass capacitor and chip ground pin.
4. Minimize the use of vias for high-speed data and clock lines and avoid routing them near or directly underneath the analog output signals.
5. Ensure the package pad is connected to ground plane on the back side of the PCB with multiple vias for heat dissipation.

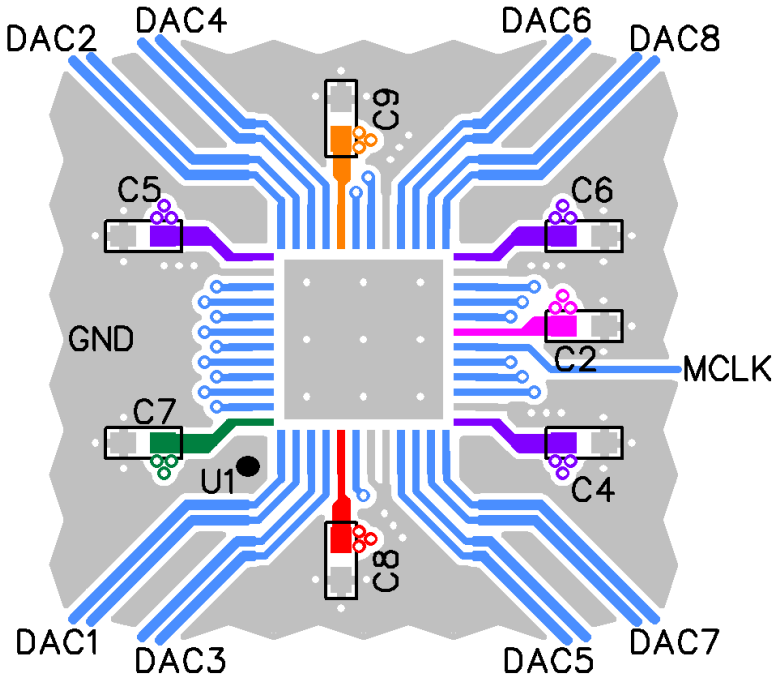
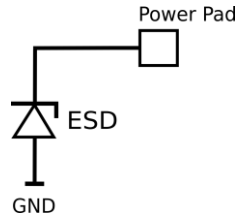
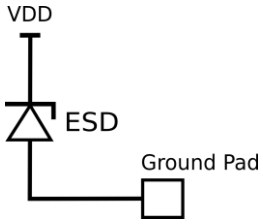
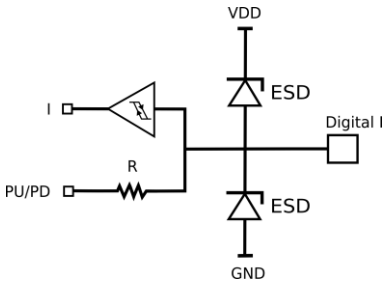
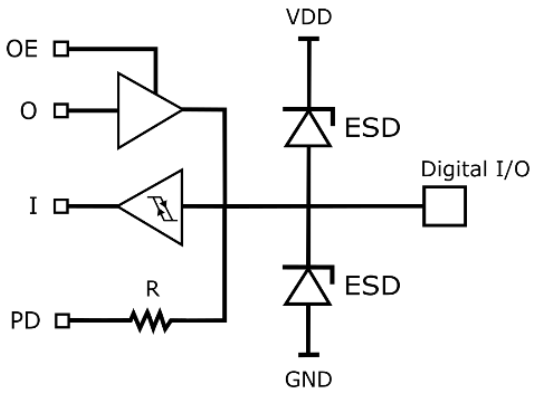


Figure 30 - ES9017 Recommended PCB Layout Guidelines

Internal Pad Circuitry

Pin Name	Pin	Type	Equivalent Circuit
AVCC_L VCAA AVCC_R AVDD	5 19 32 48	Power	
GND GND GND GND GND	8 14 23 29 38	Ground	
CHIP_EN	6	Reset	

RT1	7	Digital I/O	
MOSI/SDA/HW0	15		
SCLK/SCL/HW1	16		
MODE	17		
GPIO1	20		
GPIO2	21		
GPIO 3	22		
SS/ADDR1/HW1	30		
MISO/ADDR0/MUTE_CTRL	31		
DATA8/GPIO8	39		
DATA7/GPIO7	40		
DATA6/GPIO6	41		
DATA5/GPIO5	42		
DATA4/GPIO4	43		
DATA3	44		
DATA2	45		
DATA1	46		
DATA_CLK	47		

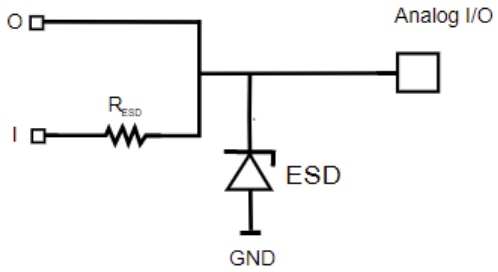
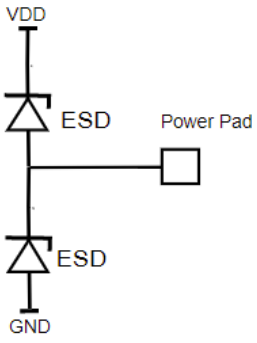
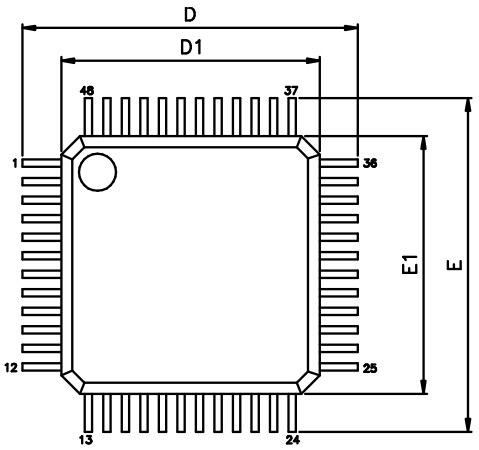
DAC1 DAC1B DAC3B DAC3 DAC5 DAC5B DAC7B DAC7 MCLK DAC8 DAC8B DAC6B DAC6 DAC4 DAC4B DAC2B DAC2	1 2 3 4 9 10 11 12 18 25 26 27 28 33 34 35 36	Analog IO DAC	
DVDD DVDD DVDD	13 24 37	IO Power	

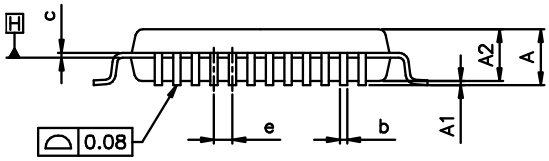
Table 28 - Internal Pad Circuitry

48 QFP Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



NOTES:
1. JEDEC OUTLINE : MS-026 BBC
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

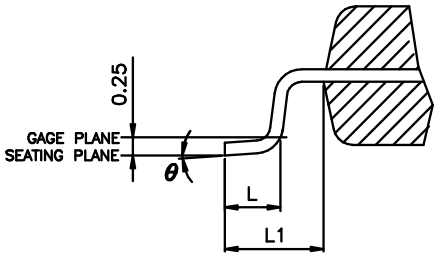
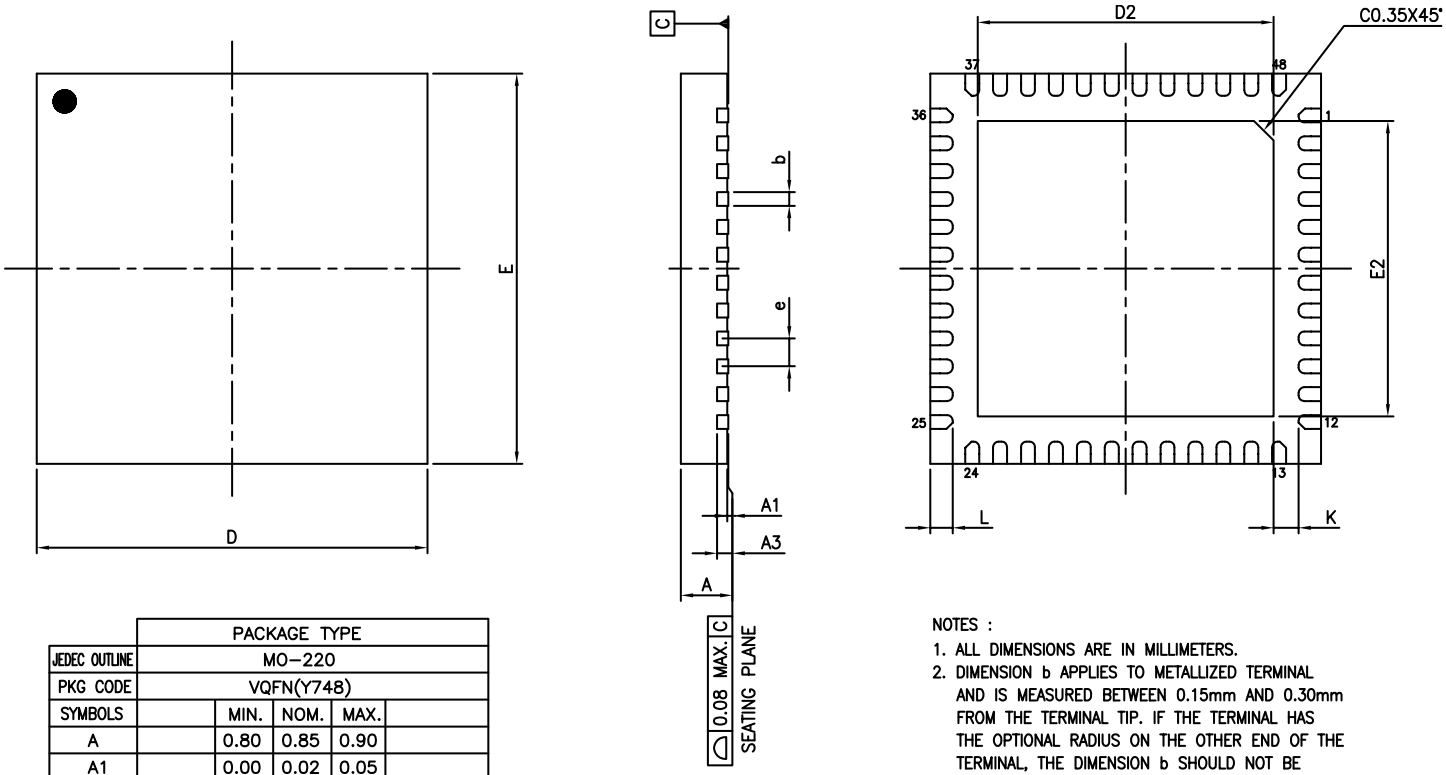


Figure 31 - ES9017S 48 QFP Package Dimensions

48 QFN Package Dimensions



	PACKAGE TYPE				
JEDEC OUTLINE	MO-220				
PKG CODE	VQFN(Y748)				
SYMBOLS		MIN.	NOM.	MAX.	
A		0.80	0.85	0.90	
A1		0.00	0.02	0.05	
A3		0.203 REF.			
b		0.20	0.25	0.30	
D		7.00 BSC			
E		7.00 BSC			
e		0.50 BSC			
L		0.35	0.40	0.45	
K		0.20	–	–	

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
224X224 MIL	5.25	5.30	5.35	5.25	5.30	5.35	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 32 - ES9017Q 48 QFN Package Dimensions

48 QFP Top View Marking

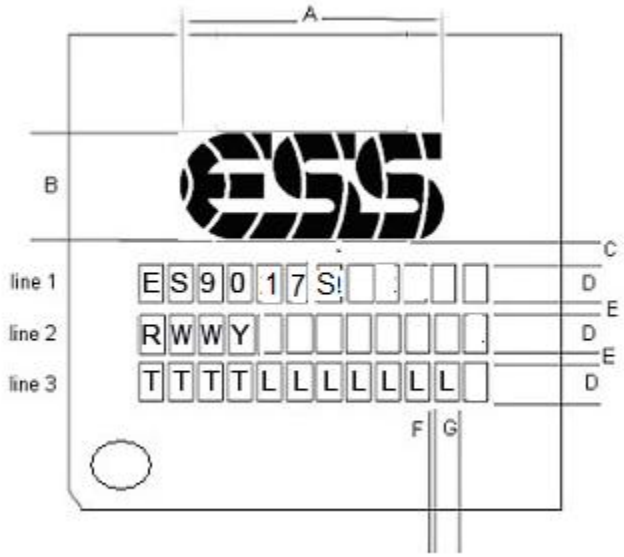


Figure 33 - ES9017S Marking

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
48 LQFP 7mm x 7mm	5.0	2.0	0.3	0.56	0.2	0.08	0.33

T	Tracking Number
W	Work Week
Y	Last Digit of Year
L	Lot Number
R	Silicon Revision

48 QFN Top View Marking

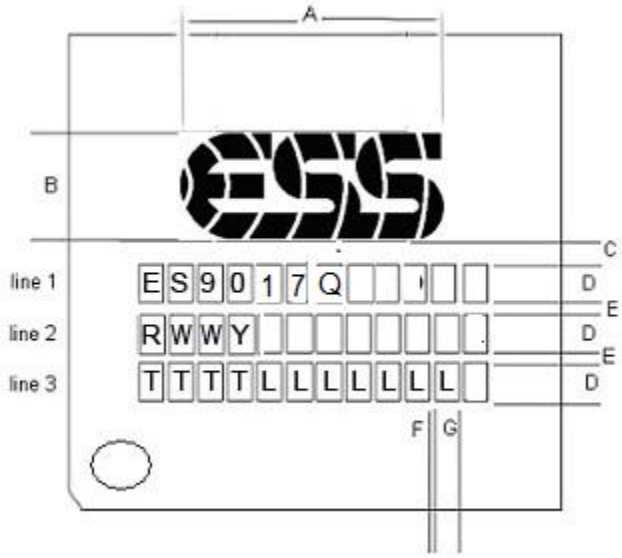


Figure 34 - ES9017Q Marking

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
48 QFN 7mm x 7mm	5.0	2.0	0.3	0.56	0.2	0.08	0.33

T	Tracking Number
W	Work Week
Y	Last Digit of Year
L	Lot Number
R	Silicon Revision

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures (Tc)) This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

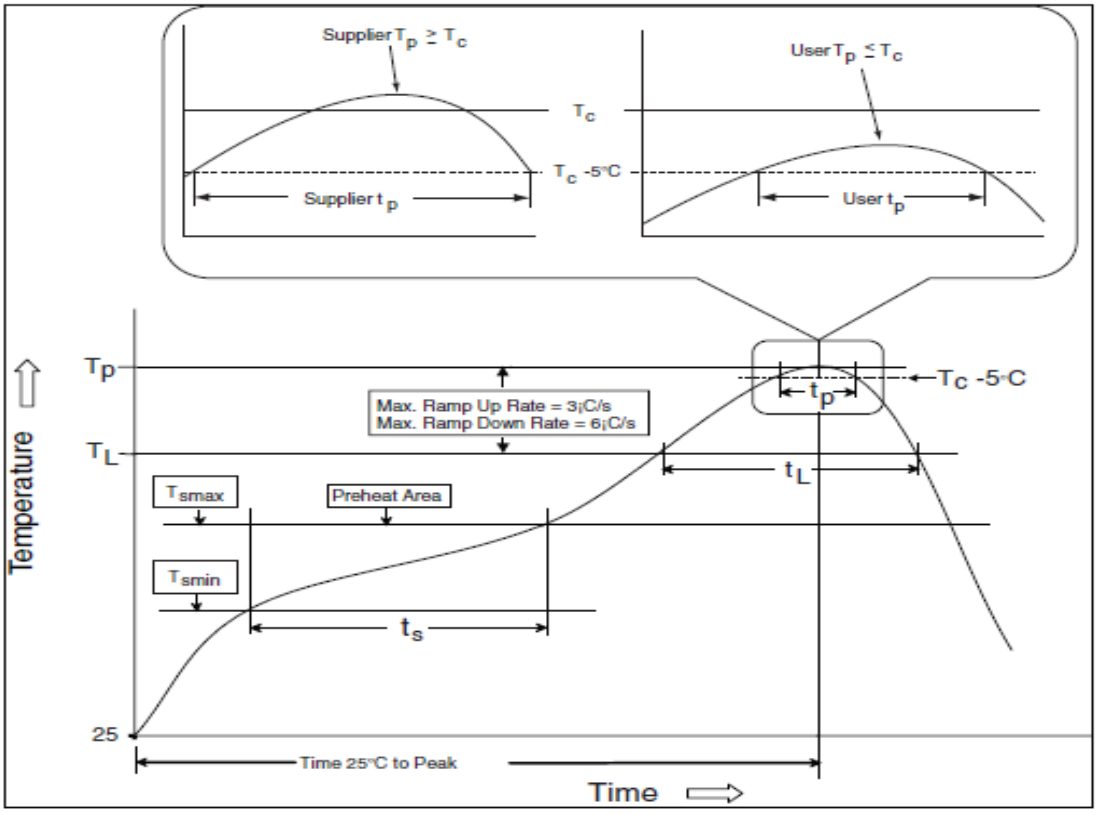


Figure 35 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 29 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2-Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 30 - RPC-2 Pb Free Classification Temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9017S	High Performance SABRE 32-bit 8 Channel DAC	7mm x 7mm 48 QFP
ES9017Q • Inquire for availability		7mm x 7mm 48 QFN

Table 31 - Ordering Information

Revision History

Current Version 0.4.3

Rev.	Date	Notes
0.1	June 24, 2022	Initial release
0.3	March, 2024	• Updated Reg 32-39 [6:5] [0:4], 52 descriptions • Added switching and timing characteristics • Unreserved Reg 13[6] CAL_RES_ENB, 63[7][6], 65[7][3:0] • Added Calibration resistor section
0.4.1	Jan, 2025	• Added power up and down sequences • Corrected Register 0 [4] default values • Clarified 64FS note • Added clock distribution diagram • Updated Block diagram for AVCC_L/R • Updated default state for Reg 30[4] • Added I²C Startup Sequence • Updated Register 65[3:0] description • Updated AVCC_L/R pin descriptions in pin list • Added description to recommended output stage • Fixed name for GPIO_CFG = 6 (System mode control) • Added absolute maximum negative supply voltage • Added supply description in Recommended Operating Conditions
0.4.3	Sept, 2025	• Updated AVCC_L/R Recommended Operating Conditions and Absolute Maximum Rating • Clarified Bit-Clock Word-Select Timing • Added note for unused DAC output pins under Pin List • Updated Reg 48-50 Volume equations • Fixed incorrect Hex Numbering in Register Map • Updated BCK-WS Timing • Added Recommended PCB Layout Guidelines