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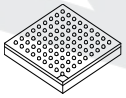
MIMX8ML8DVNLZAB **MIMX8ML6DVNLZAB**
MIMX8ML4DVNLZAB **MIMX8ML3DVNLZAB**

i.MX 8M Plus Applications Processor Datasheet for Consumer Products



Package Information
Bare die Package
FCBGA 15 x 15 mm, 0.5 mm pitch

Ordering Information
See Table 3 on page 7

1 i.MX 8M Plus introduction

The i.MX 8M Plus family focuses on neural processing unit (NPU) and vision system, advance multimedia, and industrial automation with high reliability.

The i.MX 8M Plus is a powerful quad Arm® Cortex®-A53 processor with speed up to 1.8 GHz integrated with a NPU of 2.3 TOPS that greatly accelerate machine learning inference. The vision engine is composed of two camera inputs and a HDR-capable Image Signal Processor (ISP) capable of 375 MPixels/s.
The advanced multimedia capabilities include 1080p60 video encode and decode H.265 and H.264. A 3D and 2D graphic acceleration supporting 1 GPixel/s, OpenVG 1.1, Open GL ES3.1, Vulkan, and Open CL 1.2 FP. Multiple audio and microphone interfaces for Immersive Audio and Voice systems.
For industrial applications, real time control is enabled by an integrated 800 MHz Arm® Cortex®-M7. Robust control networks are possible via CAN-FD interfaces. And a dual Gb Ethernet, one supporting Time Sensitive Networking (TSN), drive gateway applications with low latency. High industrial system reliability for safety is leveraged by DRAM Inline ECC as well as ECC support on internal software-accessible SRAMs.

The i.MX 8M Plus is very versatile presenting multiple displays and high-speed interfaces as well as multiple memory interfaces.
It is built to meet the needs for Smart Home, Building, City and Industry 4.0 applications.

Table 1. Features (Sheet 1 of 4)

Subsystem	Features
Cortex®-A53 MPCore platform	Quad Cortex®-A53 processors operation up to 1.8 GHz • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • Media Processing Engine (MPE) with Arm® NEON™ technology supporting the Advanced Single Instruction Multiple Data architecture • Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
	Support of 64-bit Arm® v8-A architecture
	512 KB unified L2 cache
Cortex®-M7 core platform	• Microcontroller available for customer application • Real-time processing • Cortex®-A53 complex off loading • Low power operation
	Cortex®-M7 CPU operating up to 800 MHz • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • 256 KB tightly coupled memory (TCM)
Image Sensor Processor (ISP)	375 Mpixel/s HDR ISP supporting configurations, such as 12MP@30fps, 4kp45, or 2x 1080p80
External memory interface	32-bit DRAM interfaces: • LPDDR4-4000 • DDR4-3200 • Inline ECC on the DDR bus
	8-bit NAND-Flash, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
	eMMC 5.1 Flash (2 interfaces: uSDHC1 and uSDHC3)
	SPI NOR Flash (3 interfaces)
	FlexSPI Flash with support for XIP (for Cortex®-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices. It also supports both Serial NOR and Serial NAND flash using the FlexSPI.
On-chip memory	Boot ROM (256 KB)
	On-chip RAM (868 KB): • OCRAM_A: 256 KB inside AUDIOMIX • OCRAM: 576 KB inside SUPERMIX • OCRAM_S: 36 KB inside SUPERMIX

Table 1. Features (continued) (Sheet 2 of 4)

Subsystem	Features
Graphic Processing Unit	• GC7000UL with OpenCL and Vulkan support • 2 shaders • 166 million triangles/sec • 1.0 giga pixel/sec • 16 GFLOPs 32-bit • Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL 1.2, Vulkan • Core clock frequency of 1000 MHz • Shader clock frequency of 1000 MHz • GC520L for 2D acceleration • Render target compatibility between 3D and 2D GPU (super tile status buffer)
Video Processing Unit	Video Decode • 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) • 1080p60 VP9 Profile 0, 2 • 1080p60 VP8 • 1080p60 AVC/H.264 Baseline, Main, High decoder Video Encode • 1080p60 AVC/H.264 encoder • 1080p60 HEVC/H.265 encoder
Neutral Processing Unit (NPU)	2.3 TOP/s Neural Network performance • Keyword detect, noise reduction, beamforming • Speech recognition (i.e. Deep Speech 2) • Image recognition (i.e. ResNet-50)
HDMI 2.0a Tx	HDMI 2.0a Tx supporting one display • Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30 • Pixel clock up to 297 MHz Audio support • 32-channel audio output support • 1 SPDIF audio eARC input support
LCDIF Display Controller	Support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously. • One LCDIF drives MIPI DSI, up to UWHD and WUXGA • One LCDIF drives LVDS Tx, up to 1920x1080p60 • One LCDIF drives HDMI Tx, up to 4kp30
Audio	• Cadence® Tensilica® HiFi 4 DSP, operating up to 800 MHz • SPDIF input and output, including a raw capture input mode • Six external synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, comprising one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and two SAI with 1 TX and 1RX lane. • All ports support 49.152 MHz BCLK. • ASRC supports processing 32 audio channels, 4 context groups, 8 kHz to 384 kHz sample rate, and 1/16 to 8x sample rate conversion ratio. • eARC/ARC • 8-channel PDM mic input

Table 1. Features (continued) (Sheet 3 of 4)

Subsystem	Features
MIPI Interface	Two instances of 4-lane MIPI CSI interface and HDR ISP • For single Camera, MIPI CSI 1 can support up to 400/500 MHz pixel clock in the Nominal/Overdrive mode. • For single Camera, MIPI CSI 2 can support up to 277 MHz pixel clock. • For dual Camera, both MIPI CSI can support up to 266 MHz pixel clock. • 2x ISP supporting 375 Mpixel/s aggregate performance and up to 3-exposure HDR processing. •When one camera is used, support up to 12MP@30fps or 4kp45 •When two cameras are used, each supports up to 1080p80 4-lane MIPI DSI interface • Maximum resolution limited to resolutions achievable with a 250 MHz pixel clock and active pixel rate of 200 Mpixel/s with 24-bit RGB. This includes resolutions such as: •1080 p60 •WUXGA (1920x1200) at 60 Hz •1920x1440 at 60 Hz •UWHD (2560x1080) at 60 Hz •MIPI DSI: WQHD (2560x1440) can be supported by reduced blanking mode
GPIO and pin multiplexing	General-purpose input/output (GPIO) modules with interrupt capability
	Input/output multiplexing controller (IOMUXC) to provide centralized pad control
Power management	Temperature sensor with programmable trip points
	Flexible power domain partitioning with internal power switches to support efficient power management
Connectivity	One PCIe Express (PCIe) Single Lane supporting PCIe Gen3 • Dual Mode operation to function as root complex or endpoint • Integrated PHY interface • Supports L1 low power sub-state
Security	Resource Domain Controller (RDC) • Supports 4 domains and up to 8 regions of DDR
	Arm® TrustZone® (TZ) architecture: • Cortex®-A53 MPCore TrustZone® support
	On-chip RAM (OCRAM) secure region protection using OCRAM controller
	High Assurance Boot (HAB)
	Cryptographic Acceleration and Assurance Module (CAAM) • Capable to support Widevine and PlayReady content protection • Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms • Real-time integrity checker (RTIC) • DRM support for RSA, AES, 3DES, DES • True random number generation (RNG) • Manufacturing protection support
	Secure Non-Volatile Storage (SNVS) • Secure real-time clock (RTC)
	Secure JTAG Controller (SJC)

Table 1. Features (continued) (Sheet 4 of 4)

Subsystem	Features
System debug	Arm® CoreSight™ debug and trace technology
	Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
	Unified trace capability for quad core Cortex®-A53 and Cortex®-M7 CPUs
	Cross Triggering Interface (CTI)
	Support for 5-pin (JTAG) debug interface

NOTE

The actual feature set depends on the part numbers as described in Table 3.

1.1 Block diagram

Figure 1 shows the functional modules in the i.MX 8M Plus processor system.

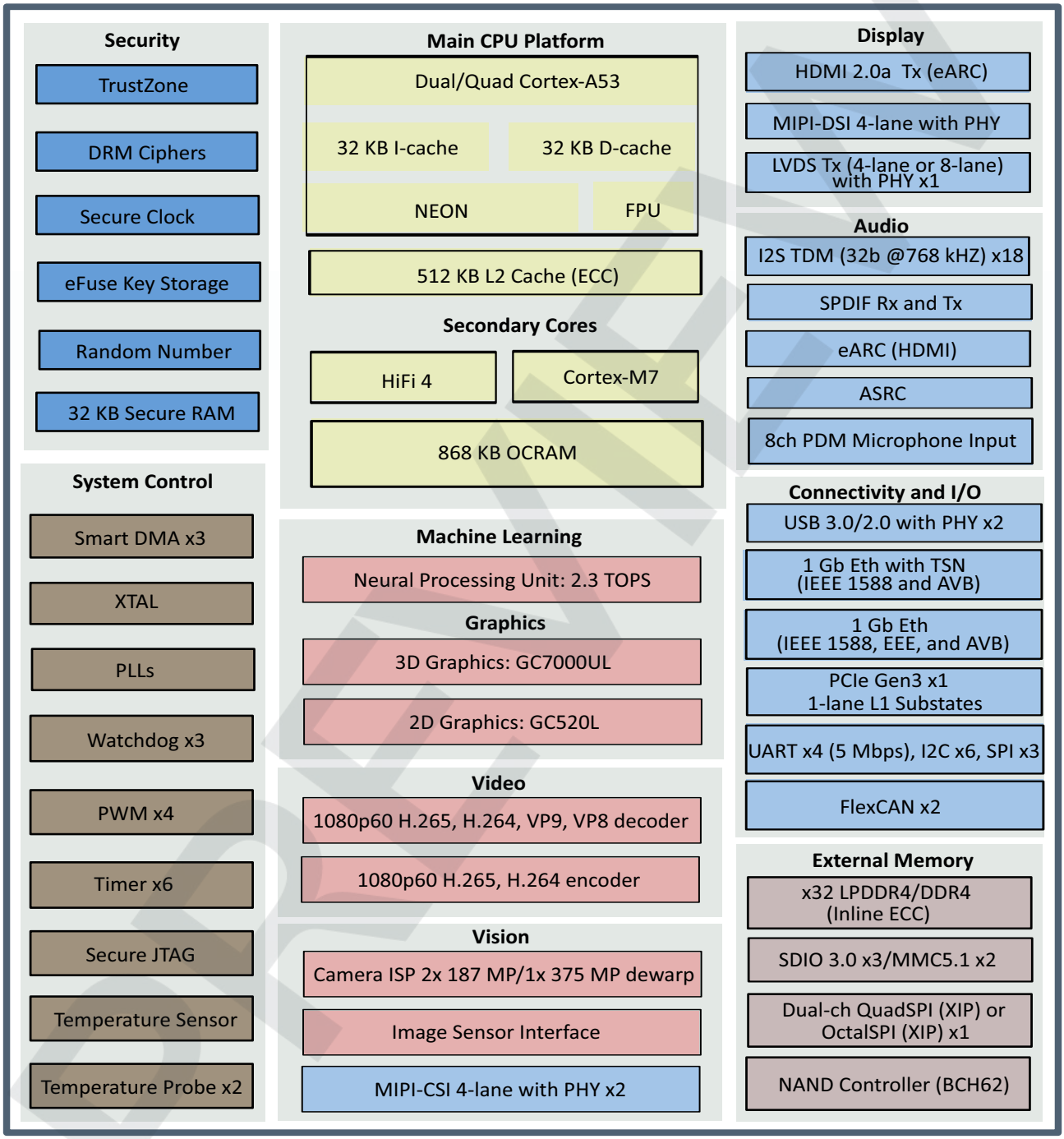


Figure 1. i.MX 8M Plus system block diagram

NOTE

Some modules shown in this block diagram are not offered on all derivatives. See Table 2 for exceptions.

Table 2. Modules supported

Key Modules	8CVN	6CVN	4CVN	3CVN	8DVN	6DVN	4DVN	3DVN
Cortex® A53	4x	4x	4x	2x	4x	4x	4x	2x
VPU	1x	1x	N/A	1x	1x	1x	N/A	1x
NPU	1x	N/A	N/A	1x	1x	N/A	N/A	1x
ISP	1x	1x	N/A	1x	1x	1x	N/A	1x
HiFi 4	1x	N/A	N/A	1x	1x	N/A	N/A	1x

1.2 Ordering information

Table 3 shows examples of orderable sample part numbers covered by this data sheet. This table does not include all possible orderable part numbers. If your desired part number is not listed in the table, or you have questions about available parts, contact your NXP representative.

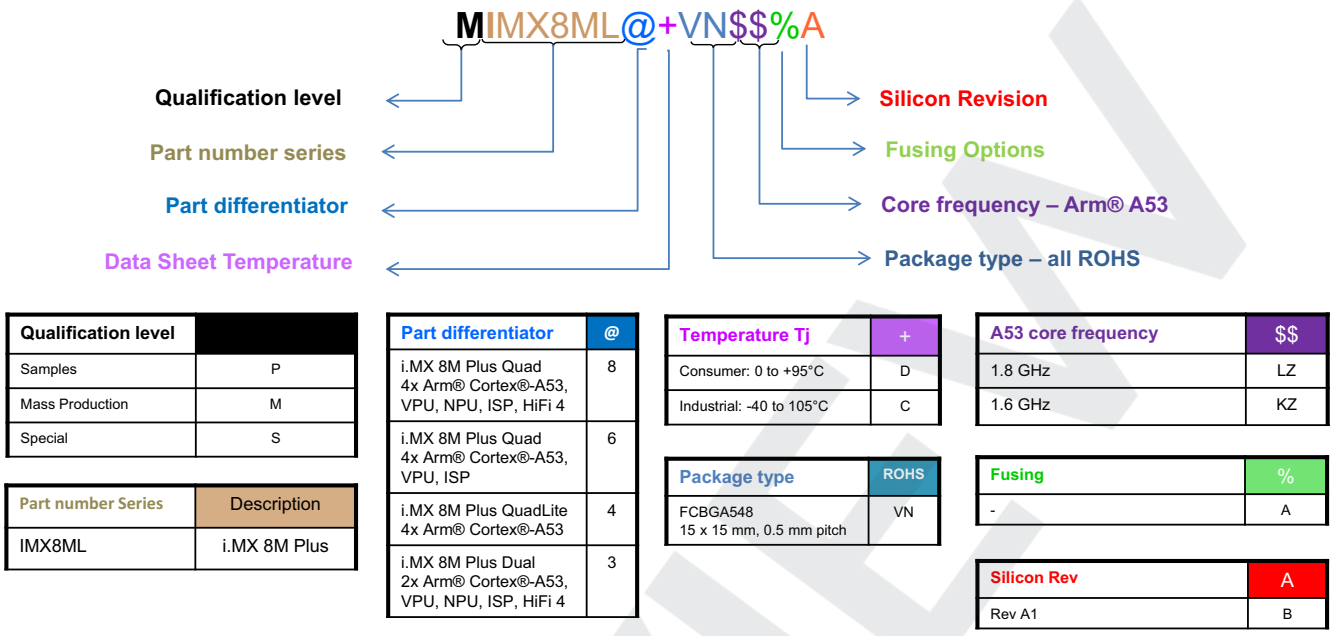
Table 3. Orderable part numbers

Part number	Device description	Part differentiator description	Number of A53 Cores	A53 speed	Qualification tier	Temperature T_j (°C)	Package description
MIMX8ML8DVNLZAB	i.MX 8M Plus Quad	NPU[1], ISP[2], VPU[3], HiFi 4, CAN	4	1.8 GHz	Consumer	0 to 95	15 x 15 mm, 0.5 pitch, FCBGA
MIMX8ML6DVNLZAB	i.MX 8M Plus Quad	ISP, VPU, CAN	4	1.8 GHz	Consumer	0 to 95	15 x 15 mm, 0.5 pitch, FCBGA
MIMX8ML4DVNLZAB	i.MX 8M Plus QuadLite	CAN	4	1.8 GHz	Consumer	0 to 95	15 x 15 mm, 0.5 pitch, FCBGA
MIMX8ML3DVNLZAB	i.MX 8M Plus Dual	NPU, ISP, VPU, HiFi 4, CAN	2	1.8 GHz	Consumer	0 to 95	15 x 15 mm, 0.5 pitch, FCBGA

1 Neural Processing Unit
2 Image Sensor Processor
3 Video Processing Unit

Figure 2 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.

Contact an NXP representative for additional details.



Qualification level	
Samples	P
Mass Production	M
Special	S

Part number Series	Description
IMX8ML	i.MX 8M Plus

Part differentiator	@
i.MX 8M Plus Quad 4x Arm® Cortex®-A53, VPU, NPU, ISP, HiFi 4	8
i.MX 8M Plus Quad 4x Arm® Cortex®-A53, VPU, ISP	6
i.MX 8M Plus QuadLite 4x Arm® Cortex®-A53	4
i.MX 8M Plus Dual 2x Arm® Cortex®-A53, VPU, NPU, ISP, HiFi 4	3

Temperature Tj	+
Consumer: 0 to +95°C	D
Industrial: -40 to 105°C	C

Package type	ROHS
FCBGA548 15 x 15 mm, 0.5 mm pitch	VN

A53 core frequency	$$
1.8 GHz	LZ
1.6 GHz	KZ

Fusing	%
-	A

Silicon Rev	A
Rev A1	B

Figure 2. Part number nomenclature—i.MX 8M Plus family of processors

2 Modules list

The i.MX 8M Plus family of processors contains a variety of digital and analog modules. Table 4 describes these modules in alphabetical order.

Table 4. i.MX 8M Plus modules list

Block mnemonic	Block name	Brief description
APBH-DMA	NAND Flash and BCH ECC DMA Controller	DMA controller used for GPMI2 operation.
Arm	Arm Platform	The Arm Core Platform includes a quad Cortex-A53 core and a Cortex-M7 core. The Cortex-A53 core includes associated sub-blocks, such as the Level 2 Cache Controller, Snoop Control Unit (SCU), General Interrupt Controller (GIC), private timers, watchdog, and CoreSight debug modules. The Cortex-M7 core is used as a customer microcontroller.
ASRC	Asynchronous Sample Rate Converter	The Asynchronous Sample Rate Converter (ASRC) can process 4 groups of audio channels with an independent time-base simultaneously. A group of channels with the same time-base (or resampling ration) is referred to as a context. Each context has independent processing pipelines. Contexts can be configured to start and stop at any time without affecting the processing of other contexts. The ASRC supports up to 32 audio channels, which can either be assigned to a single context or spread across multiple contexts.
BCH	Binary-BCH ECC Processor	The BCH module provides up to 62-bit ECC encoder/decoder for NAND Flash controller (GPMI).
CAAM	Cryptographic accelerator and assurance module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Plus processors, the secure memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 8M Plus platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interface	Cross Trigger Interface (CTI) allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A53 core platform.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to access: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.

Table 4. i.MX 8M Plus modules list (continued)

Block mnemonic	Block name	Brief description
DDRC	Double Data Rate Controller	The DDR Controller has the following features: • Supports 32-bit LPDDR4-4000 and DDR4-3200 • Supports up to 8 Gbyte DDR memory space
eCSPI1 eCSPI2 eCSPI3	Configurable SPI	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes.
eDMA	Enhanced Direct Memory Access	• There is one enhanced DMAs (eDMA). • The eDMA is a 32-channel DMA engine • It is provided specifically for copying between memory and memory (most likely such as between two of DRAM, OCRAM_A, and Audio DSPs TCM). • It separates the 32 channels into separate 64 KByte regions in the system memory map for virtualization and partitioning purpose. • There are no DMA requests connected to eDMA from any peripheral. It is generally controlled by the Audio DSP (or potentially the Cortex-A53 or Cortex_M7).
ENET	Ethernet Controller	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 8M Plus Applications Processor Reference Manual* (IMX8MPRM) for details.
ENET_QOS	Ethernet QoS Controller	The ENET_QOS is compliant with the IEEE 802.3–2015 specification and can be used in applications, such as AV bridges, AV nodes, switches, data center bridges and nodes, and network interface cards. It enables a host to transmit and receive data over Ethernet in compliance with the IEEE802.3–2015. A separate 1 Gbit Ethernet QoS with TSN supports the same features as ENET and also following features: • 802.1Qbv Enhancements to Scheduling Traffic • 802.1Qbu Frame preemption • Time Based Scheduling
FlexCAN1 FlexCAN2	Flexible Controller Area Network	Communication controller implementing the CAN with Flexible Data rate (CAN FD) protocol and the CAN protocol according to the CAN 2.0B protocol specification.
FlexSPI	FlexSPI	The FlexSPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi master access with priority and flexible and configurable buffer for each master
GIC	Generic Interrupt Controller	The GIC handles all interrupts from the various subsystems and is ready for virtualization.