

For automotive, $T_{opr}=125^{\circ}\text{C}$, Low noise, high PSRR, with ON/OFF control function, 300mA High-speed LDO regulator

☆AEC-Q100 Grade1

■ GENERAL DESCRIPTION

The XD6239 series is a high-speed LDO regulator that features high accuracy, low noise, high ripple rejection and low dropout. The series consists of a voltage reference, an error amplifier, a driver FET, a current limiter, a phase compensation circuit, a thermal shutdown circuit and an inrush current protection circuit.

The output voltage is selectable in 0.1V increments within the range of 1.2V to 3.4V.

The current limit circuit and the thermal shutdown circuit are built-in.

These protection circuits operate when the output current reaches the current limit level or when the junction temperature reaches the thermal limit.

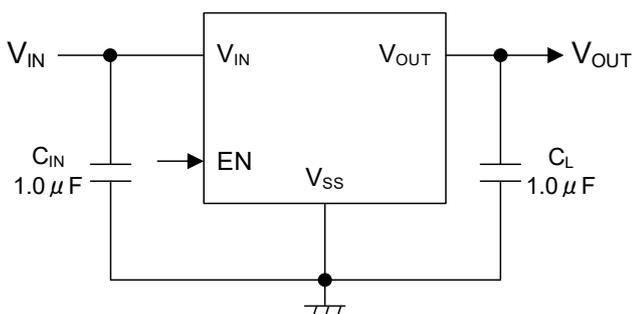
■ APPLICATIONS

- Automotive camera modules
- Automotive body control application systems
- Automotive Infotainment
 - Drive recorder
 - ETC
- Industrial Equipment

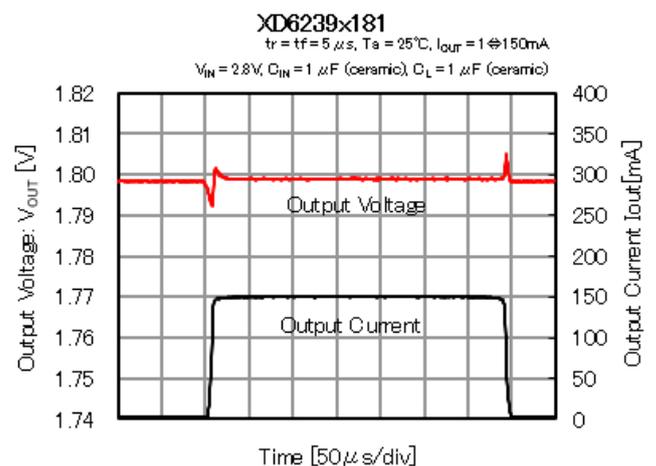
■ FEATURES

Input Voltage Range	: 2.0V ~ 6.0V
Output Voltages	: 1.2V ~ 3.4V (0.1V increments)
Maximum Output Current	: 300mA
Output Voltage Accuracy	: $\pm 1.0\%$ ($V_{OUT(T)} \geq 2.0\text{V}$) $\pm 20\text{mV}$ ($V_{OUT(T)} \leq 1.9\text{V}$)
Supply Current	: 100 μA
High Ripple Rejection Function	: 75dB@1kHz : EN function : C_L Discharge : Inrush Current Protection
Protection Function	: Current Limit : Thermal Shutdown
Low ESR Capacitors	: $C_{IN}=1\mu\text{F}$, $C_L=1\mu\text{F}$
Operating Ambient Temperature	: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
Packages	: DFN1010-4C (1.0x1.0x0.6mm) : SOT-25 (2.8x2.9x1.3mm) : SOT-89-5 (4.5x4.6x1.6mm)
Environmentally Friendly	: EU RoHS Compliant, Pb Free

■ TYPICAL APPLICATION CIRCUIT

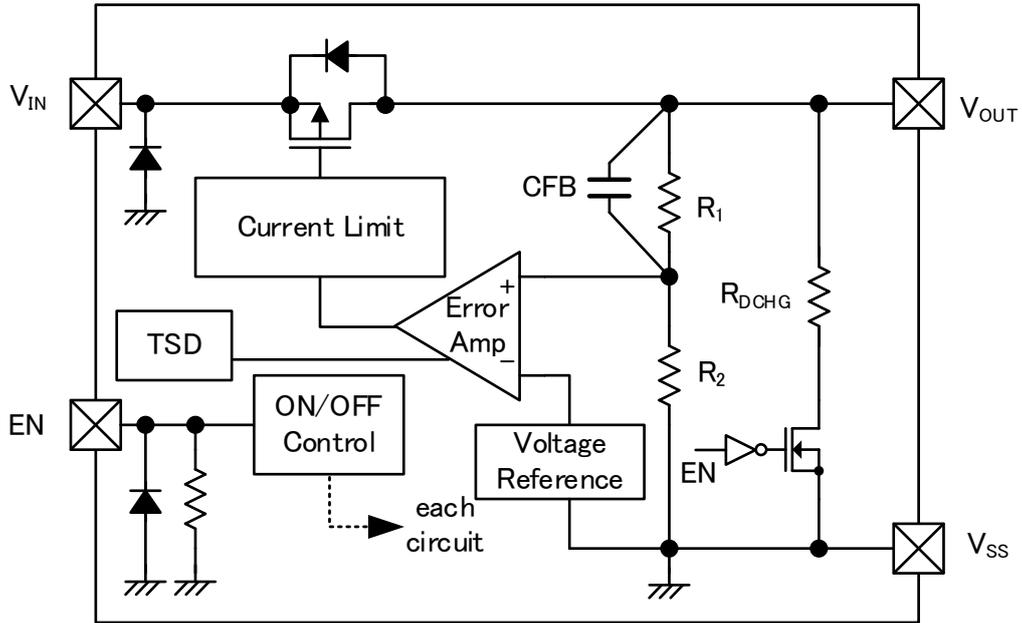


■ TYPICAL PERFORMANCE CHARACTERISTICS



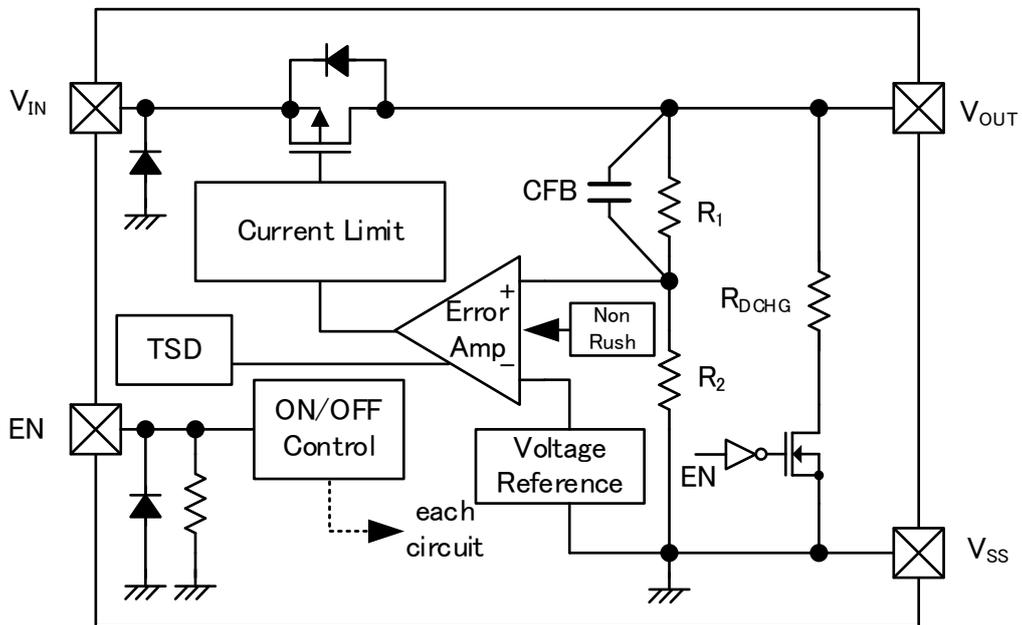
■ BLOCK DIAGRAMS

● D Type



* Diodes inside the circuits are ESD protection diodes and parasitic diodes

● H Type



* Diodes inside the circuits are ESD protection diodes and parasitic diodes

■ PRODUCT CLASSIFICATION

● Ordering Information

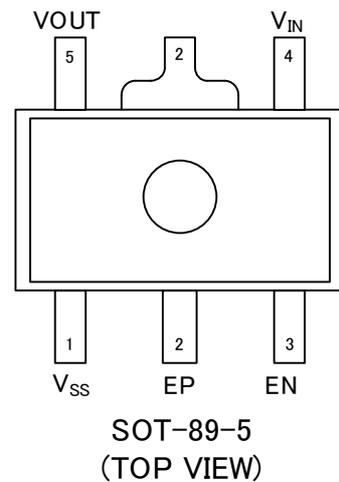
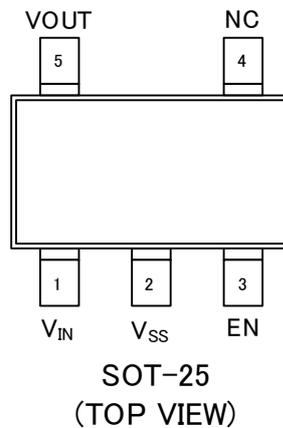
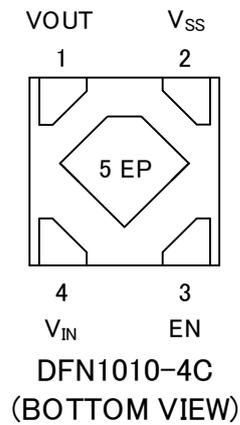
XD6239①②③④⑤⑥-⑦^(*1)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	TYPE	D	Without Inrush Current Protection
		H	With Inrush Current Protection
②③	Output Voltage	12 ~ 34	e.g. 2.5V → ②=2, ③=5
④	Output Accuracy	1	±1.0%
⑤⑥-⑦ ^(*1)	Packages (Order Unit)	6R-Q	DFN1010-4C (5,000pcs/Reel) ^(*2)
		MR-Q	SOT-25 (3,000pcs/Reel) ^(*2)
		PR-Q	SOT-89-5 (1,000pcs/Reel) ^(*2)

^(*1) The "-Q" suffix denotes "AEC-Q100" compliant.

^(*2) "Halogen and Antimony free" as well as being fully EU RoHS compliant.

PIN CONFIGURATION



PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTIONS
DFN1010-4C	SOT-25	SOT-89-5		
1	5	5	V _{OUT}	Output
2	2	1	V _{SS}	Ground
3	3	3	EN	ON/OFF Control
4	1	4	V _{IN}	Power Supply Input
5	-	2	EP	Exposed thermal pad. The exposed pad must be connected to V _{SS} pin.
-	4	-	NC	No Connection

FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN	L	Stand-by
	H	Active
	OPEN	Stand-by*

* The operation is OFF because an internal pull-down resistor maintains the EN pin voltage at a low level.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
V _{IN} Pin Voltage		V _{IN}	-0.3 ~ 7.0	V
V _{OUT} Pin Voltage		V _{OUT}	-0.3 ~ V _{IN} + 0.3 or 7.0 ^{(*)2}	V
V _{OUT} Pin Current		I _{OUT}	700	mA
Power Dissipation (T _a =25°C)	DFN1010-4C	P _d	830 (JESD51-7 Board) ^{(*)2}	mW
	SOT-25		950 (JESD51-7 Board) ^{(*)2}	
	SOT-89-5		2150 (JESD51-7 Board) ^{(*)2}	
Junction Temperature		T _j	-40 ~ 150	°C
Storage Temperature		T _{stg}	-55 ~ 150	°C

All voltages are specified with respect to V_{SS}.

^{(*)1} The maximum rating corresponds to the lower value of V_{IN} + 0.3V or 7.0V.

^{(*)2} The power dissipation figure shown is PCB mounted and is for reference only.

Please refer to PACKAGING INFORMATION for the mounting condition.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Voltage	V _{IN}	2.0	-	6.0	V
Output Current ^{(*)1}	I _{OUT}	0.0	-	300	mA
EN Pin Voltage	V _{EN/SS}	0.0	-	6.0	V
Operating Ambient Temperature	T _{opr}	-40	-	125	°C
Input Capacitor (Effective Value)	C _{IN} ^{(*)2,3}	0.9	-	Any	μF
Output Capacitor (Effective Value)	C _L ^{(*)2}	0.9	-	100	μF

All voltages are described based on the V_{SS} pin.

^{(*)1} Please use within the range where the junction temperature does not exceed the maximum junction temperature.

^{(*)2} Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

^{(*)3} If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase, and the IC may malfunction.

ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V _{IN}	-	2.0	-	6.0	V	①
Output Voltage	V _{OUT(E)} ^{(*)3}	V _{OUT(T)} ≥ 2.0V, I _{OUT} = 1mA	V _{OUT(T)} × 0.99	V _{OUT(T)}	V _{OUT(T)} × 1.01	V	①
		-40°C ≤ Ta ≤ 125°C ^{(*)1}	V _{OUT(T)} × 0.95		V _{OUT(T)} × 1.05		
		V _{OUT(T)} < 2.0V, I _{OUT} = 1mA	V _{OUT(T)} - 20mV	V _{OUT(T)}	V _{OUT(T)} + 20mV	V	
		-40°C ≤ Ta ≤ 125°C ^{(*)1}	V _{OUT(T)} - 50mV		V _{OUT(T)} + 50mV		
Maximum Output Current	I _{OUTMAX}	-40°C ≤ Ta ≤ 125°C ^{(*)2}	300	-	-	mA	①
Load Regulation	ΔV _{OUT}	V _{OUT@0.1mA} - V _{OUT@300mA}	-10	30	+45	mV	①
		SOT-25 -40°C ≤ Ta ≤ 125°C ^{(*)1}	-20		+65		
		V _{OUT@0.1mA} - V _{OUT@300mA}	-10	28	+45		
		SOT-89-5 -40°C ≤ Ta ≤ 125°C ^{(*)1}	-20		+65		
V _{OUT@0.1mA} - V _{OUT@300mA}	-10	25	+45				
DFN1010-4C -40°C ≤ Ta ≤ 125°C ^{(*)1}	-20		+65				
Dropout Voltage	V _{dif} ^{(*)5}	I _{OUT} = 300mA	(E-1)			mV	①
Supply Current	I _{SS}		40	100	270	μA	②
		-40°C ≤ Ta ≤ 125°C ^{(*)1}	20		355		
Stand-by Current	I _{STB}	V _{EN} = V _{SS}	-	0.01	0.98	μA	②
		-40°C ≤ Ta ≤ 125°C ^{(*)1}	-		9.0		
Line Regulation	ΔV _{OUT} / (ΔV _{IN} · V _{OUT})	V _{OUT(T)} + 0.5V ≤ V _{IN} ≤ 6.0V, I _{OUT} = 10mA	-0.1	0.0	0.1	% / V	①
		-40°C ≤ Ta ≤ 125°C ^{(*)1}	-0.2		0.2		
Power Supply Rejection Ratio	PSRR	V _{OUT(T)} < 2.5V, V _{IN} = 3.0V _{DC} + 0.5V _{p-p} AC V _{EN} = V _{OUT(T)} + 1.0V, I _{OUT} = 30mA, f = 1kHz	60	75	-	dB	③
		-40°C ≤ Ta ≤ 125°C ^{(*)2}	50		-		
		2.5V ≤ V _{OUT(T)} , V _{IN} = {V _{OUT(T)} + 1.0} V _{DC} + 0.5V _{p-p} AC V _{EN} = V _{OUT(T)} + 1.0V, I _{OUT} = 30mA, f = 1kHz	60		-		
		-40°C ≤ Ta ≤ 125°C ^{(*)2}	50		-		

V_{IN} = V_{OUT(T)} + 1.0V, V_{EN} = V_{IN}, C_{IN} = 1.0μF, C_L = 1.0μF unless otherwise specified.

(*)1 Design guarantee value.

(*)2 Design value.

(*)3 V_{OUT(E)} : Effective output voltage.

(i.e. the output voltage when "V_{OUT(T)}+1.0V" is provided at the V_{IN} pin while maintaining a certain I_{OUT} value.)

(*)4 V_{OUT(T)} : Set output voltage value.

(*)5 V_{dif} = {V_{IN1}^{(*)5} - V_{OUT1}^{(*)6}} (V_{IN1} ≥ 2.0V)

V_{IN1} : The input voltage when V_{OUT1} appears as input voltage is gradually decreased

V_{OUT1} : A voltage equal to 98% of the output voltage when a sufficiently stabilized input voltage of {V_{OUT(T)}+1.0V} is applied

■ ELECTRICAL CHARACTERISTICS(Continued)

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Current Limit	I _{LIM}	V _{OUT} =V _{OUT(T)} *0.95	310	600	650	mA	①
		-40°C ≤ Ta ≤ 125°C ^(*2)	306		700		
Short Current	I _{SHORT}	V _{OUT} =V _{SS}	50	100	200	mA	①
		-40°C ≤ Ta ≤ 125°C ^(*2)	30		290		
EN "H" Voltage	V _{ENH}	-40°C ≤ Ta ≤ 125°C ^(*1)	1.0	-	6.0	V	④
EN "L" Voltage	V _{ENL}	-40°C ≤ Ta ≤ 125°C ^(*1)	V _{SS}	-	0.3	V	④
EN "H" Current	I _{ENH}	V _{EN} =V _{IN} =6.0V	2.0	6.0	9.0	μA	④
		-40°C ≤ Ta ≤ 125°C ^(*1)	1.0		12.0		
EN "L" Current	I _{ENL}	V _{IN} =6.0V, V _{EN} =V _{SS}	-	0.0	0.1	μA	④
C _L Discharge Resistance	R _{DCHG}	V _{IN} =6.0V, V _{OUT} =2.0V, V _{EN} =V _{SS}	100	200	300	Ω	①
		-40°C ≤ Ta ≤ 125°C ^(*1)	80		320		
Inrush Current (Only H Type)	I _{rush}	V _{IN} =V _{EN} =6.0V	50	150	250	mA	⑤
		-40°C ≤ Ta ≤ 125°C ^(*2)	30		270		
Thermal Shutdown Detect Temperature	T _{TSD}	Junction Temperature	-	165	-	°C	①
Thermal Shutdown Release Temperature	T _{TSR}	Junction Temperature	-	135	-	°C	
Thermal Shutdown Hysteresis Width	T _{TSD} - T _{TSR}	Junction Temperature	-	30	-	°C	

V_{IN} = V_{OUT(T)} + 1.0V, V_{EN} = V_{IN}, C_{IN} = 1.0μF, C_L = 1.0μF unless otherwise specified.

^(*1) Design guarantee value.

^(*2) Design value.

■ ELECTRICAL CHARACTERISTICS(Continued)

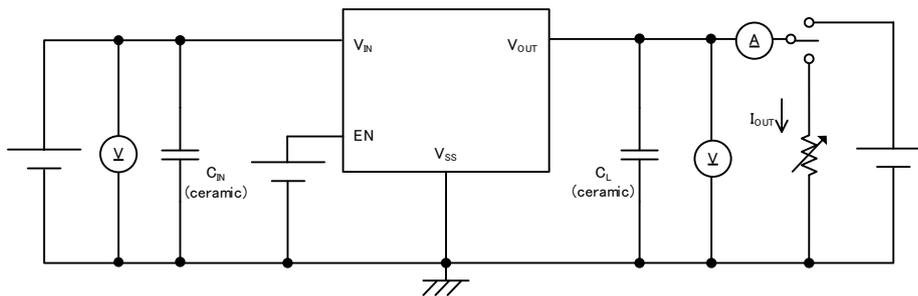
(E-1) Voltage Chart 1

NOMINAL OUTPUT VOLTAGE (V)	DROPOUT VOLTAGE : Vdif (mV)				
	Ta=25°C			-40°C ≤ Ta ≤ 125°C ^{(*)2}	
	V _{OUT(T)}	MIN.	TYP.	MAX.	MIN
1.20	330	480	820	300	870
1.30					
1.40					
1.50	240	420	520	190	650
1.60					
1.70					
1.80	190	300	410	120	490
1.90					
2.00					
2.10					
2.20					
2.30					
2.40					
2.50	130	240	350	70	430
2.60					
2.70					
2.80					
2.90					
3.00	95	200	305	50	390
3.10					
3.20					
3.30					
3.40					

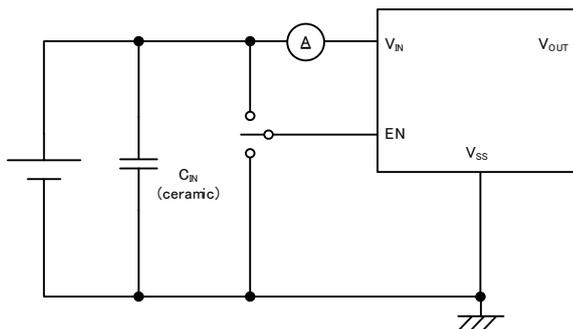
^{(*)2} Design value.

TEST CIRCUITS

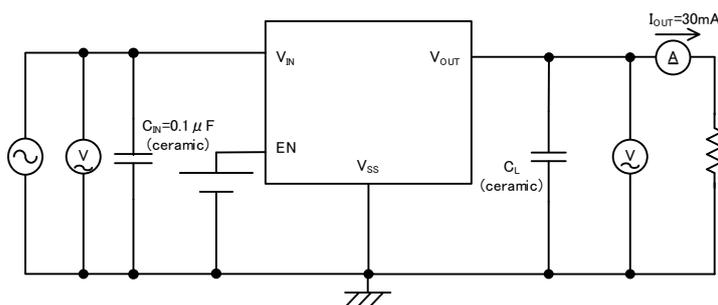
● Circuit 1



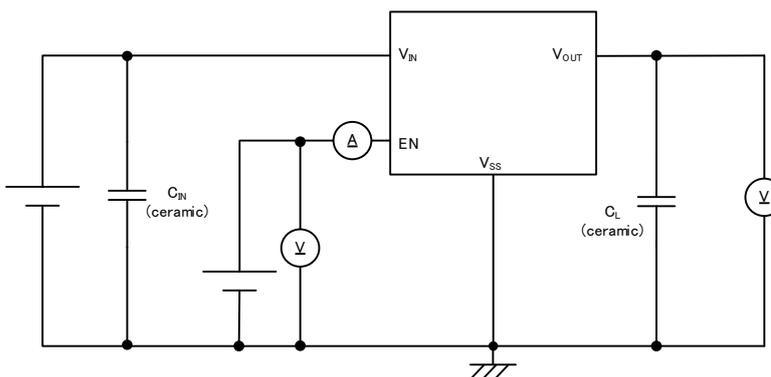
● Circuit 2



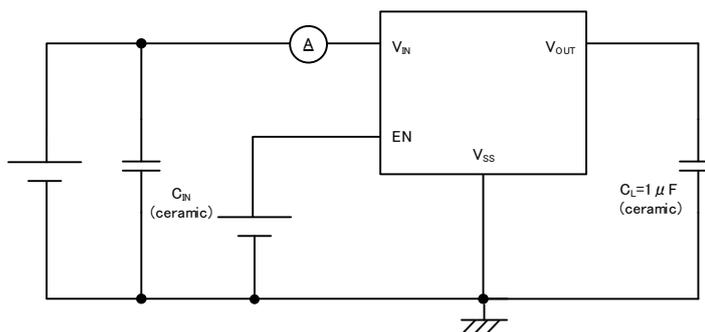
● Circuit 3



● Circuit 4



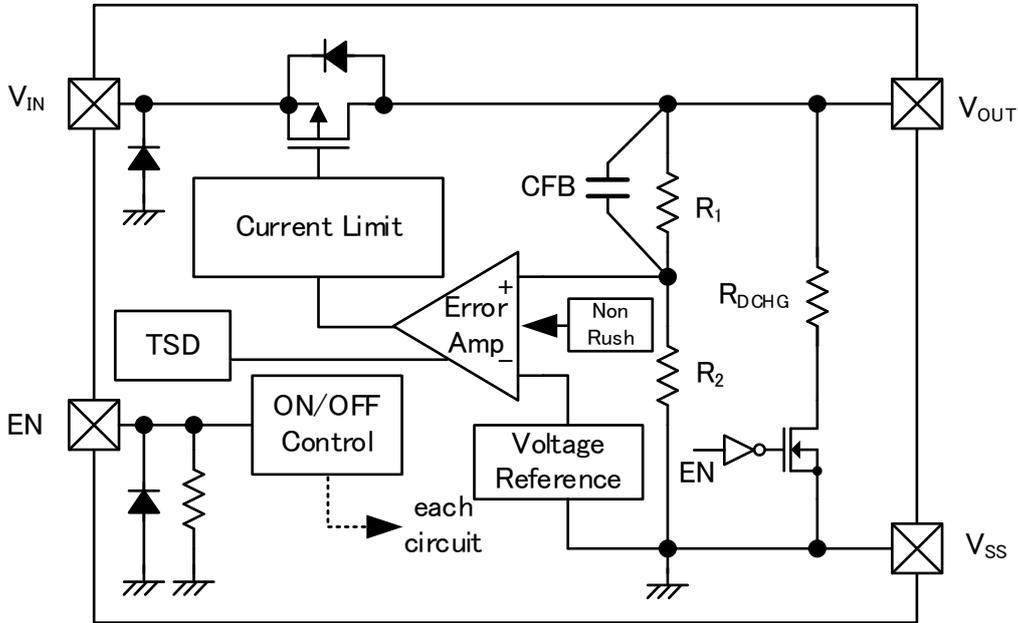
● Circuit 5



OPERATIONAL EXPLANATION

The voltage divided by resistors R_1 & R_2 is compared with the internal reference voltage by the error amplifier. The Pch MOSFET which is connected to the V_{OUT} pin is then driven by the subsequent control signal. The output voltage at the V_{OUT} pin is controlled and stabilized by a system of negative feedback.

The current limit circuit operates according to the output current level. Further, the IC's internal circuitry can be shutdown via the EN pin signal.



The XD6239 series needs an output capacitor C_L for phase compensation. In order to ensure the stable phase compensation, please place an output capacitor at the V_{OUT} pin and V_{SS} pin as close as possible. For a stable power input, please connect an input capacitor (C_{IN}) between the V_{IN} pin and the V_{SS} pin.

<EN function>

The XD6239 series can place the IC into standby mode using the EN function.

When the IC is in standby mode and power is supplied to the V_{IN} pin, the C_L discharge function enables the output capacitor to discharge quickly.

The EN pin has a pull-down resistor so that it allows current to flow into the EN pin when a voltage is supplied to the EN pin.

■ OPERATIONAL EXPLANATION(Continued)

<Inrush Current Protection>

The H types have a built-in inrush current prevention function.

When the output voltage is about 30% or less of the set voltage after the IC starts up, a short-circuit current flows and the output voltage rises. When the output voltage reaches about 30% of the set voltage, the inrush current prevention function operates for a period of about 120 μ s.

While the inrush current prevention function is operating, the inrush current flowing from the V_{IN} pin to the V_{OUT} pin is suppressed not to exceed the I_{rush} (150mA TYP.).

After the inrush current prevention function is released, the current flowing from the input pin to the output pin is limited by the current limit circuit.

<Current Limit >

The protection circuit operates as a combination of an output current limiter and fold-back short circuit protection. When load current reaches the current limit level, the output voltage drops. As a result, the load current starts to reduce with showing fold-back curve. When the output is short-circuited, the current drops to the Short Current I_{short} (100mA TYP.).

<Thermal Shutdown>

The XD6239 series has a built-in thermal shutdown circuit to protect against overheating. When the junction temperature reaches the detection temperature T_{TSD} (165°C TYP.), the driver FET is forcibly turned off.

When the junction temperature drops to the release temperature T_{TSR} (135°C TYP.) while the driver FET remains off, the driver FET turns on (automatic return) and starts regulation operation again.

< C_L Discharge Function>

The XD6239 series can quickly discharge the electric charge at the output capacitor (C_L), when a low signal (IC internal circuit stop signal) is applied to the EN pin by the Nch FET connected between V_{OUT} and V_{SS} in the block diagram. C_L discharge resistance is set to 200 Ω (TYP.) when V_{IN} is 6.0V (TYP.) and V_{OUT} is 2.0V (TYP.). Moreover, discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R_{DCHG}) and the output capacitance (C_L).

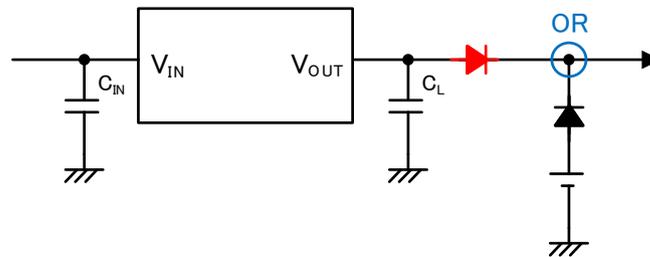
By setting time constant of a C_L discharge resistance (R_{DCHG}) and an output capacitance (C_L) as τ ($\tau = C_L \times R_{DCHG}$), the output voltage after discharge via the Nch FET is calculated by the following formula.

$$V = V_{OUT(E)} \times e^{-t/\tau} \text{ when expanding } t, t = \tau \ln (V_{OUT(E)} / V)$$

V	: Output voltage after discharge
$V_{OUT(E)}$: Output voltage
t	: Discharge time
τ	: $R_{DCHG} \times C_L$
C_L	: Output capacitance
R_{DCHG}	: C_L discharge resistance

NOTES ON USE

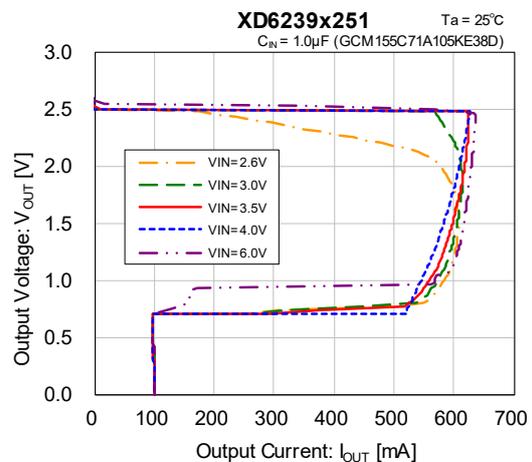
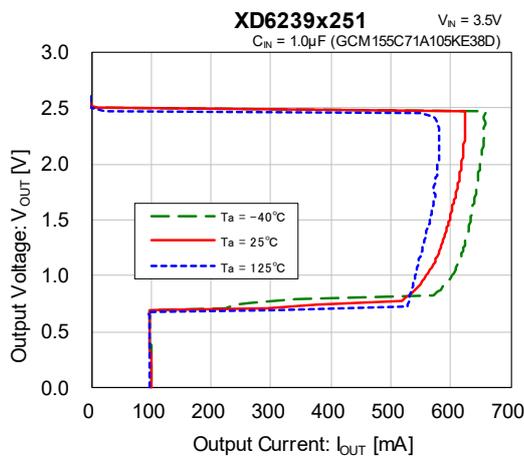
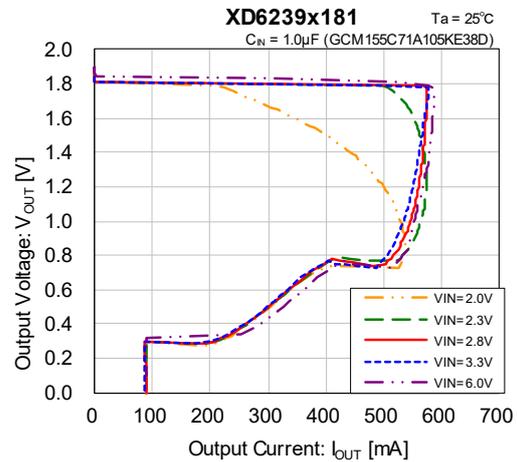
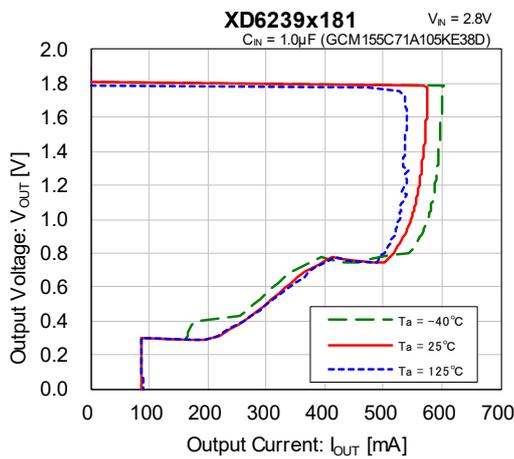
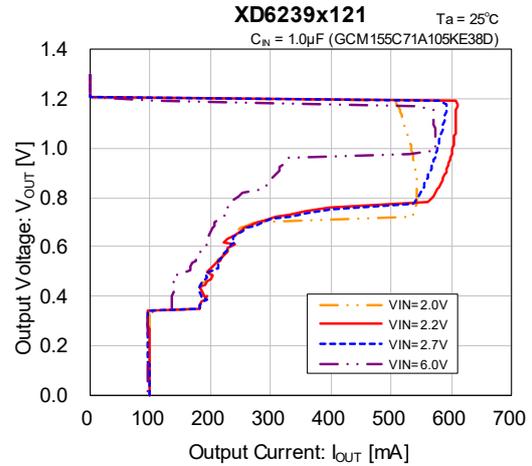
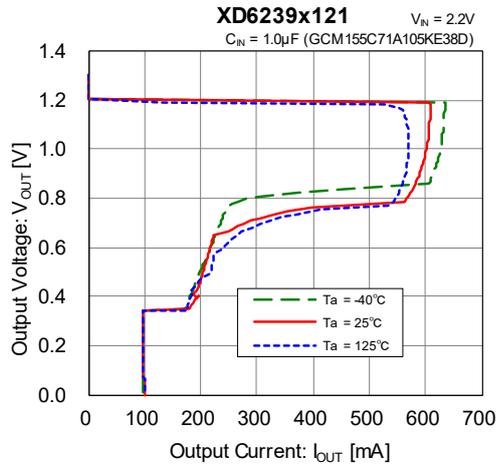
1. For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications. Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.
2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please strengthen V_{IN} and V_{OUT} wiring in particular.
3. The input capacitor C_{IN} and the output capacitor C_L should be placed as close as possible with short wiring.
4. The IC is controlled with constant current start-up. Start-up sequence control is requested to draw a load current after the output voltage has reached its nominal level.
5. Do not apply a voltage higher than the set output voltage to the V_{OUT} pin by an external power supply when $EN = "H"$. If a voltage higher than the output voltage is applied to the V_{OUT} pin when $EN = "H"$, make sure that no bias is applied to the V_{OUT} pin. Insert a diode or other means to prevent the bias from being applied to the V_{OUT} pin.



6. The EN pin current increases to tens of μA when a voltage higher than the V_{IN} pin voltage is applied to the EN pin. Therefore, if you want to suppress the EN pin current, design the device so that the V_{IN} pin voltage is higher than the EN pin voltage.
7. Torex places an importance on improving our products and their reliabilities. We request that users incorporate fail-safe designs and post-aging prevention treatment when using Torex products in their systems.

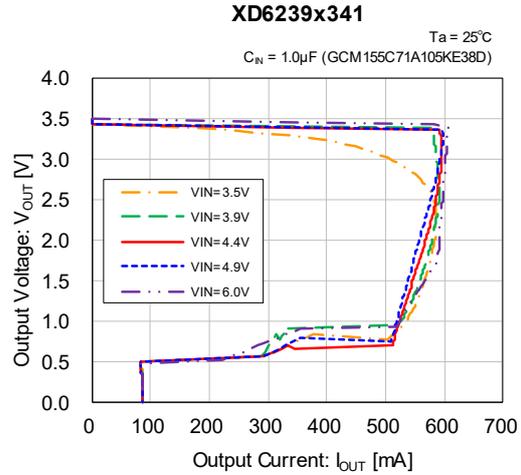
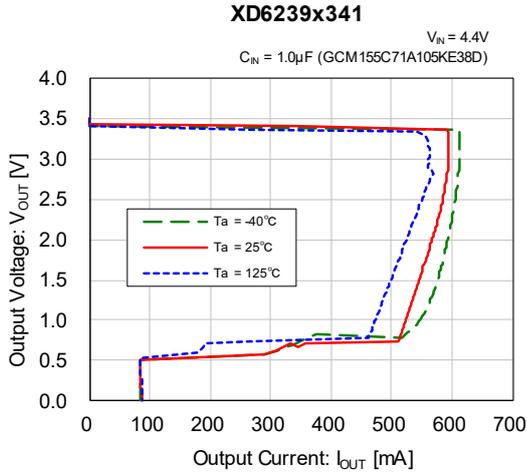
TYPICAL PERFORMANCE CHARACTERISTICS

(1) Output Voltage vs. Output Current (Current Limit)

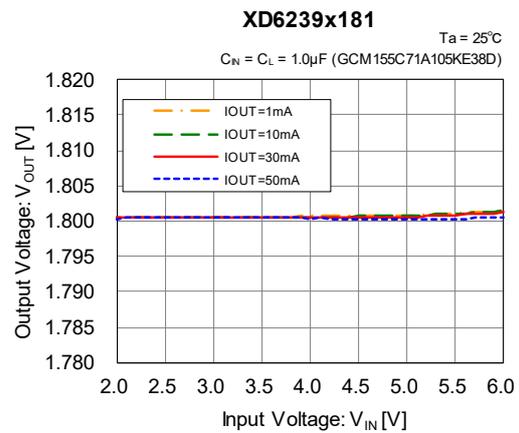
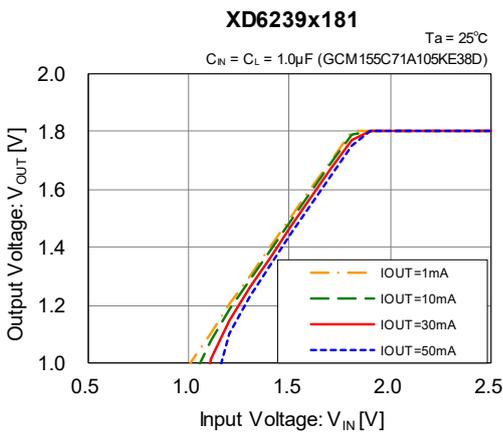
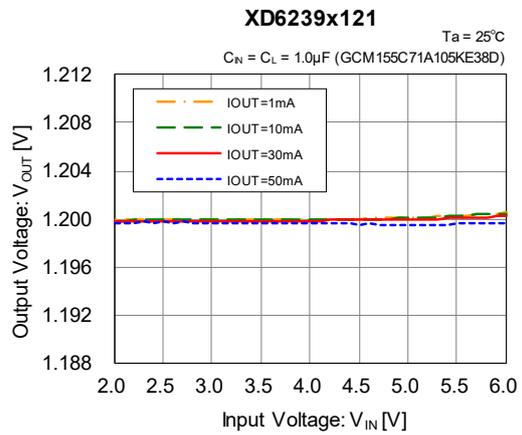
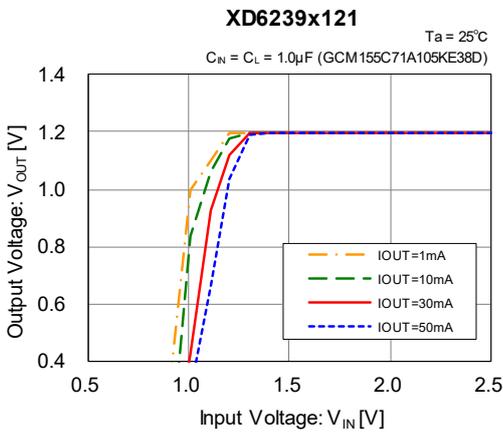


TYPICAL PERFORMANCE CHARACTERISTICS

(1) Output Voltage vs. Output Current (Current Limit)

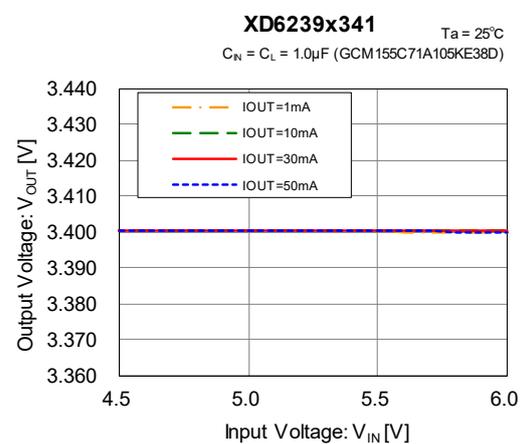
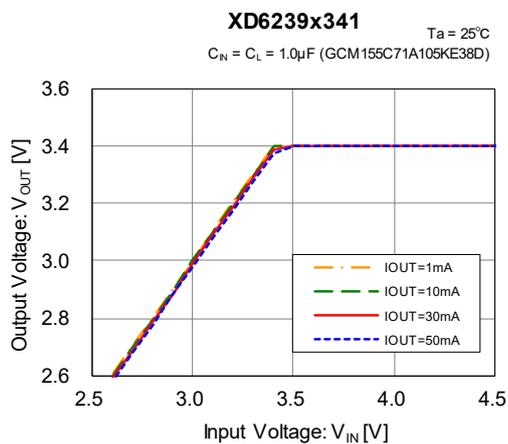
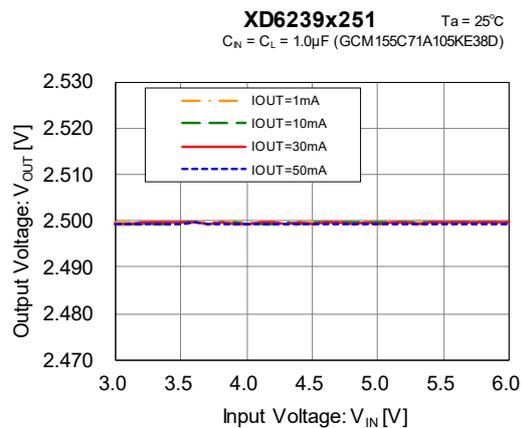
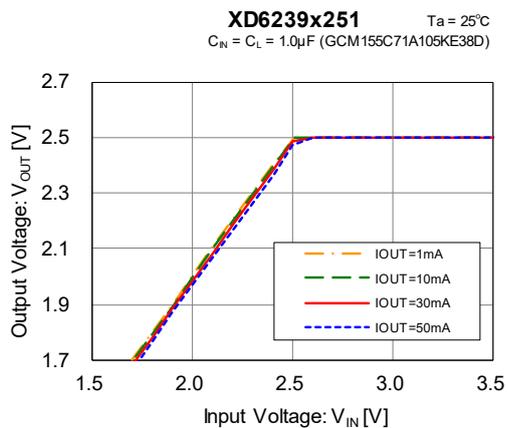


(2) Output Voltage vs. Input Voltage



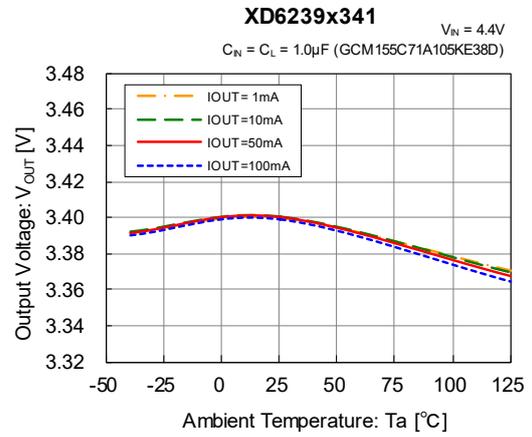
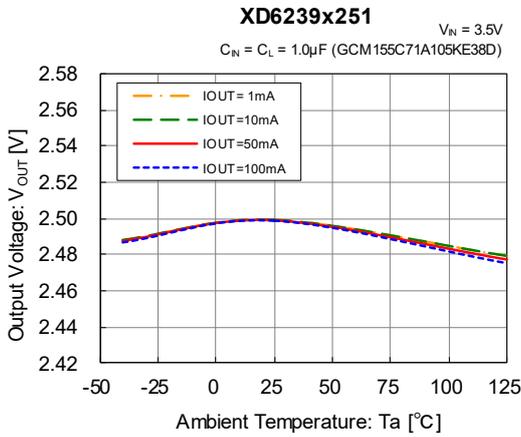
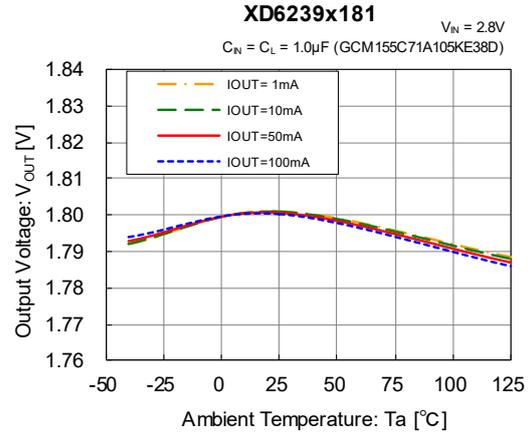
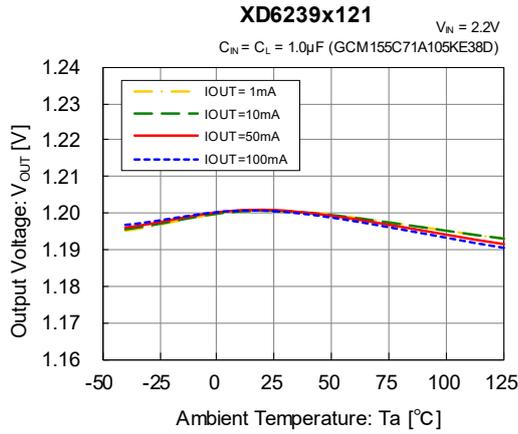
TYPICAL PERFORMANCE CHARACTERISTICS

(2) Output Voltage vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

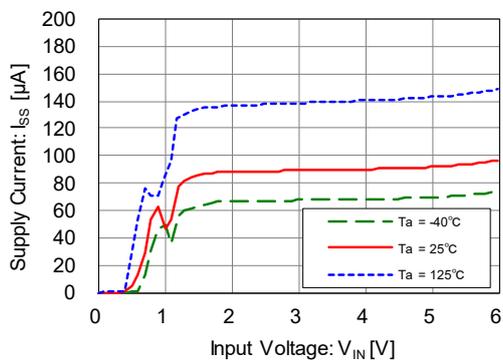
(3) Output Voltage vs. Ambient Temperature



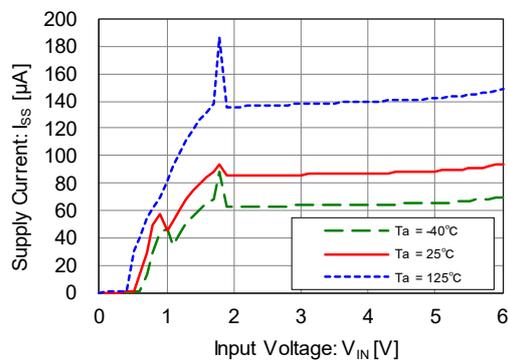
■ TYPICAL PERFORMANCE CHARACTERISTICS

(4) Quiescent Current vs. Input Voltage

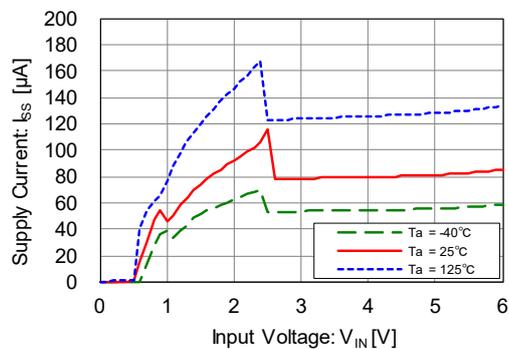
XD6239x121



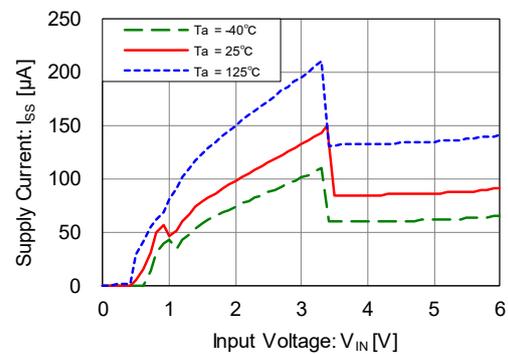
XD6239x181



XD6239x251

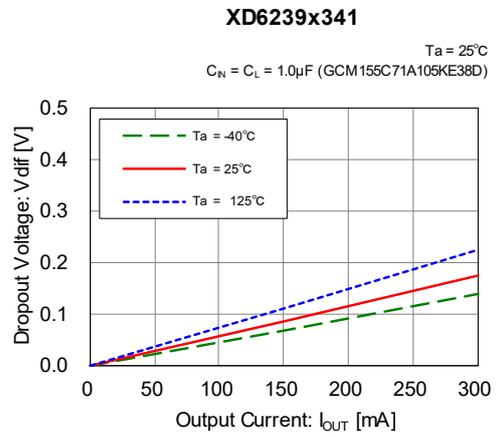
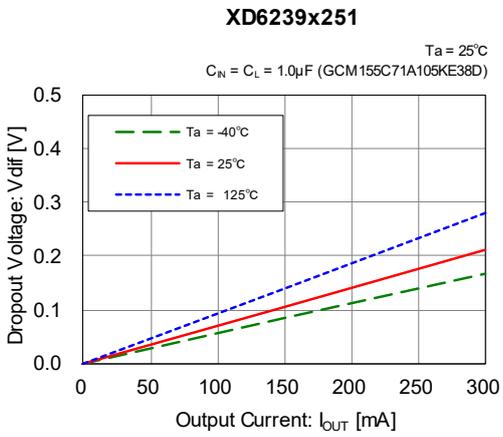
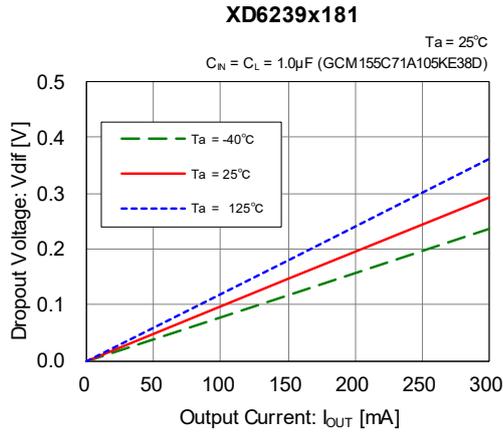


XD6239x341



TYPICAL PERFORMANCE CHARACTERISTICS

(5) Dropout Voltage vs. Output Current

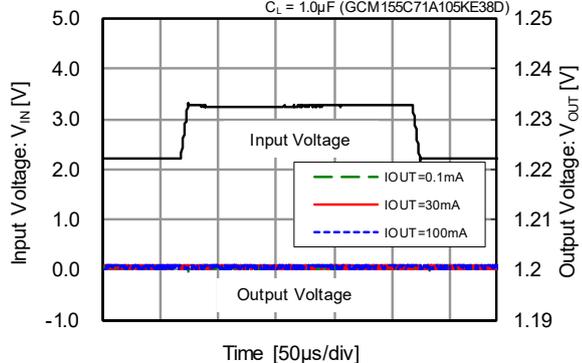


TYPICAL PERFORMANCE CHARACTERISTICS

(6) Input Voltage Transient Response

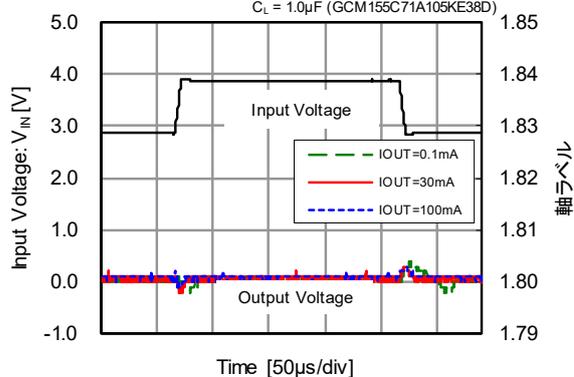
XD6239x121

$t_r = t_f = 5\mu s$, $T_a = 25^\circ C$, $V_{IN} = 2.2V \leftrightarrow 3.2V$
 $C_{IN} = 0.1\mu F$ (GCM155R71A104KA55D),
 $C_L = 1.0\mu F$ (GCM155C71A105KE38D)



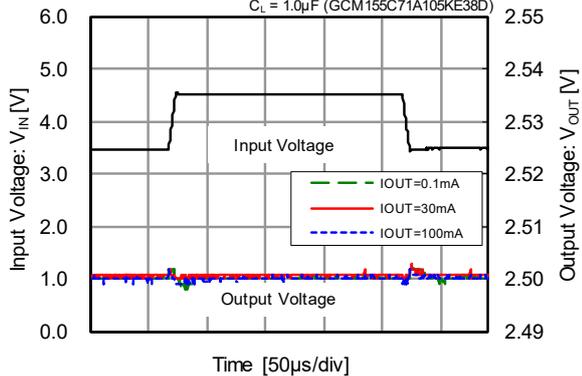
XD6239x181

$t_r = t_f = 5\mu s$, $T_a = 25^\circ C$, $V_{IN} = 2.8V \leftrightarrow 3.8V$
 $C_{IN} = 0.1\mu F$ (GCM155R71A104KA55D),
 $C_L = 1.0\mu F$ (GCM155C71A105KE38D)



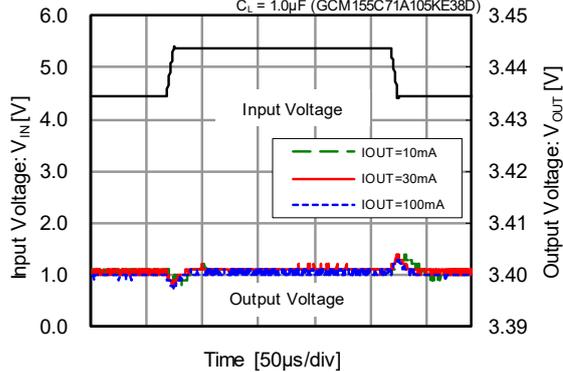
XD6239x251

$t_r = t_f = 5\mu s$, $T_a = 25^\circ C$, $V_{IN} = 3.5V \leftrightarrow 4.5V$
 $C_{IN} = 0.1\mu F$ (GCM155R71A104KA55D),
 $C_L = 1.0\mu F$ (GCM155C71A105KE38D)



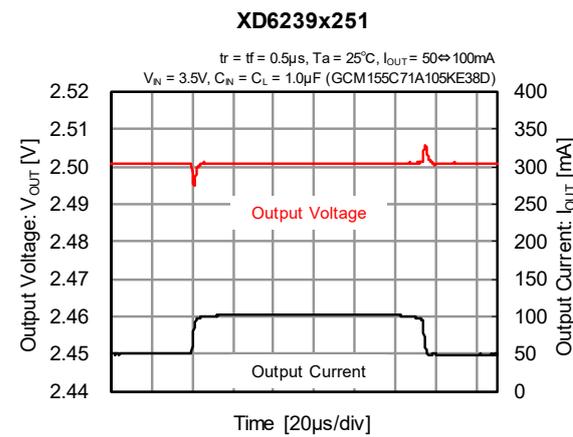
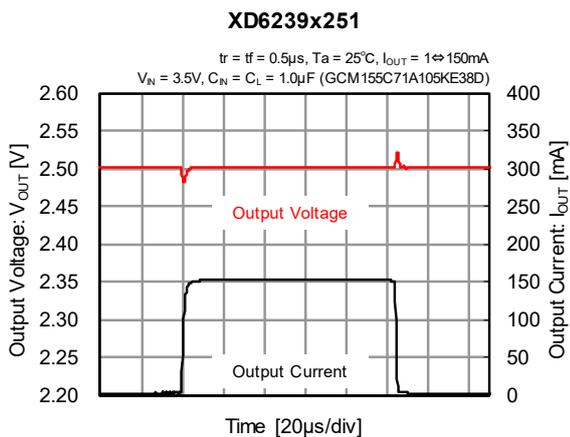
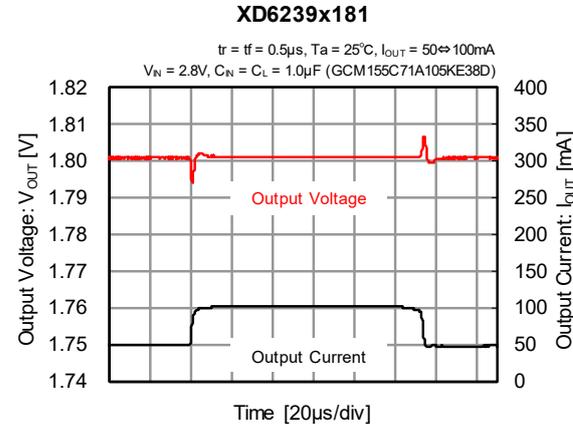
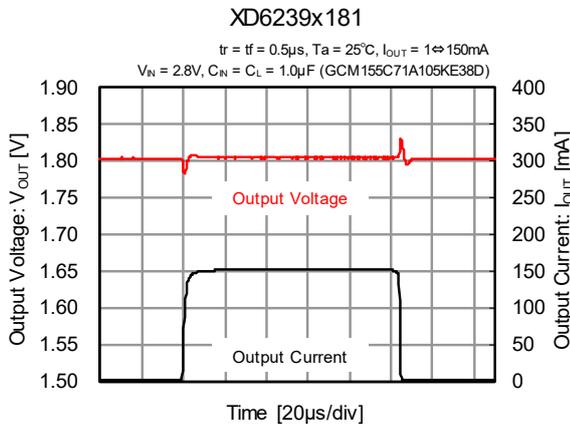
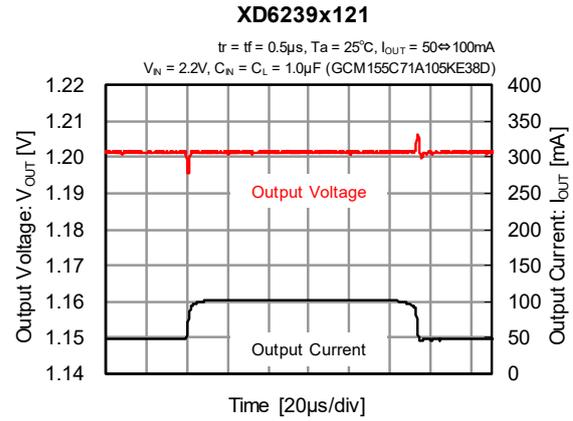
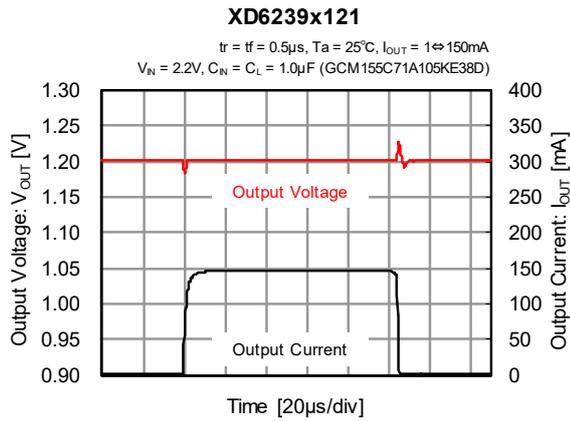
XD6239x341

$t_r = t_f = 5\mu s$, $T_a = 25^\circ C$, $V_{IN} = 4.4V \leftrightarrow 5.4V$
 $C_{IN} = 0.1\mu F$ (GCM155R71A104KA55D),
 $C_L = 1.0\mu F$ (GCM155C71A105KE38D)



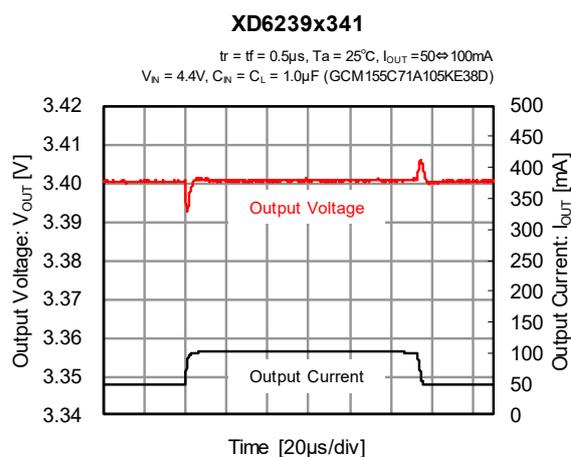
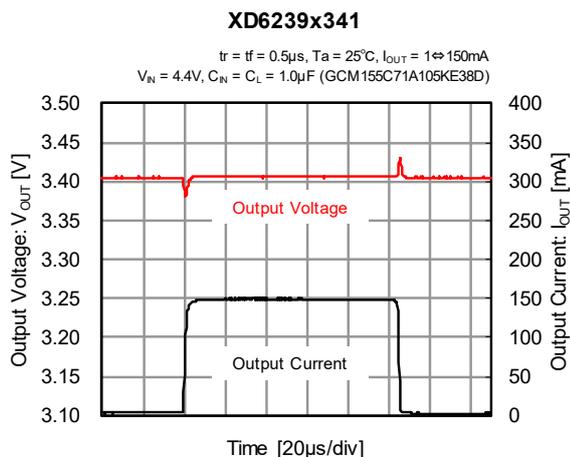
TYPICAL PERFORMANCE CHARACTERISTICS

(7-1) Load Transient Response ($t_r=t_f=0.5\mu s$)

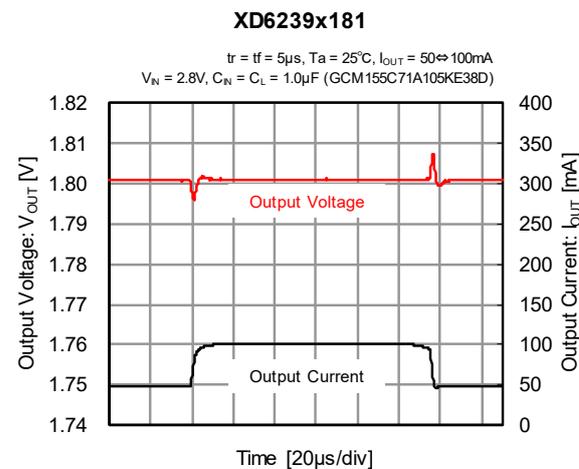
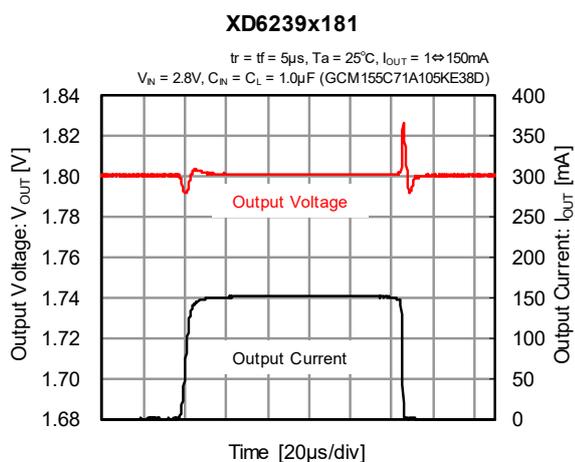
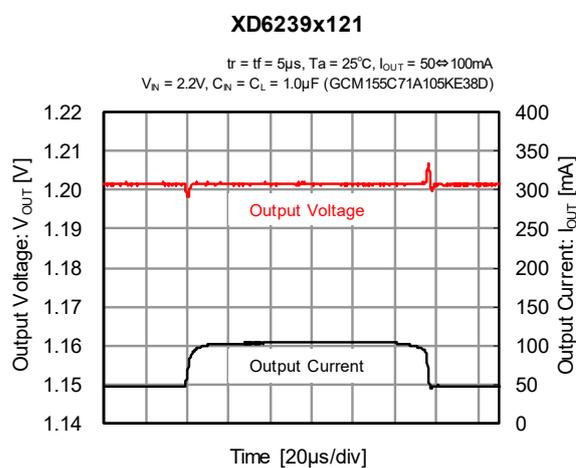
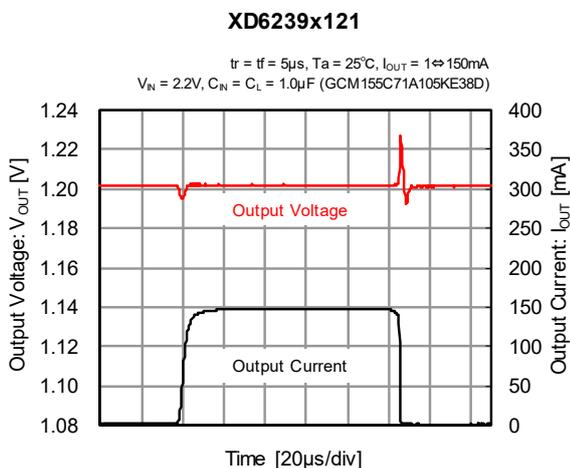


TYPICAL PERFORMANCE CHARACTERISTICS

(7-1) Load Transient Response ($t_r=t_f=0.5\mu s$)



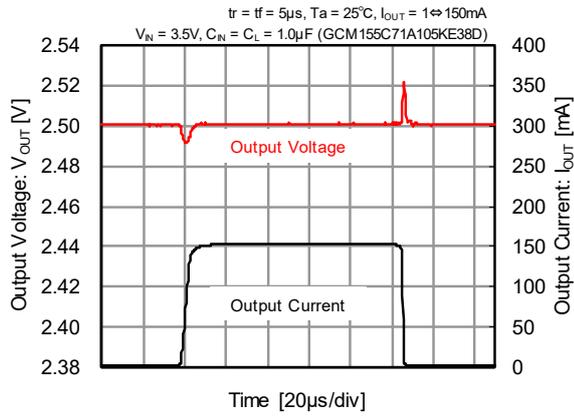
(7-2) Load Transient Response ($t_r=t_f=5\mu s$)



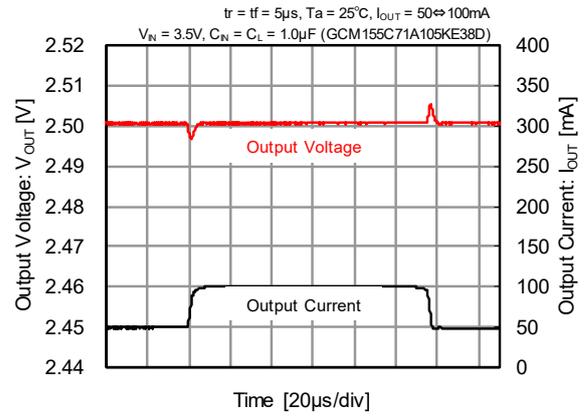
TYPICAL PERFORMANCE CHARACTERISTICS

(7-2) Load Transient Response ($t_r=t_f=5\mu\text{s}$)

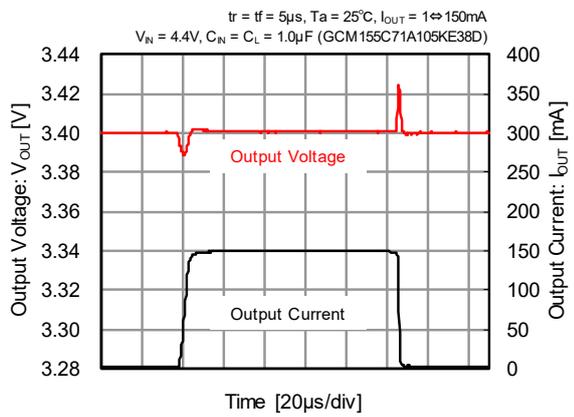
XD6239x251



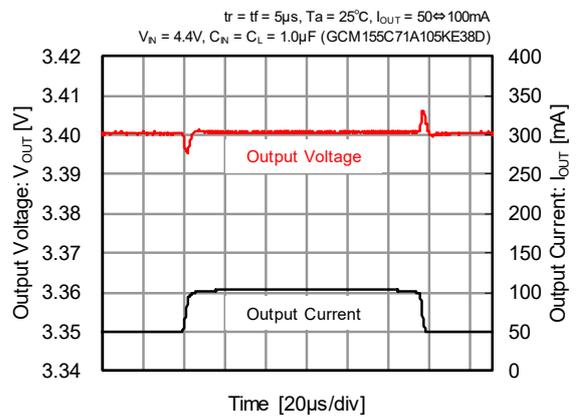
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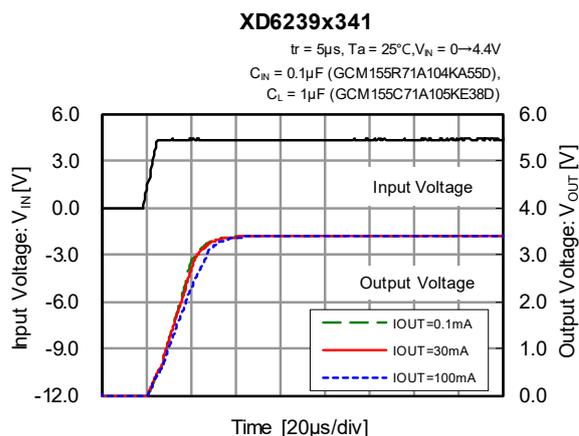
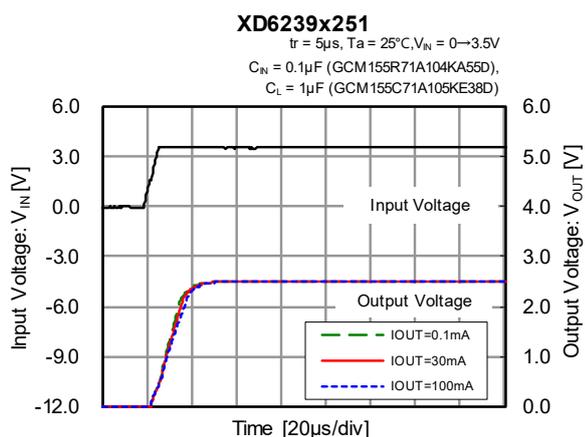


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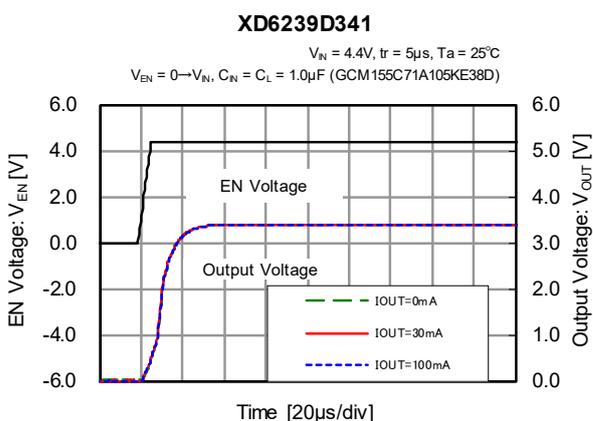
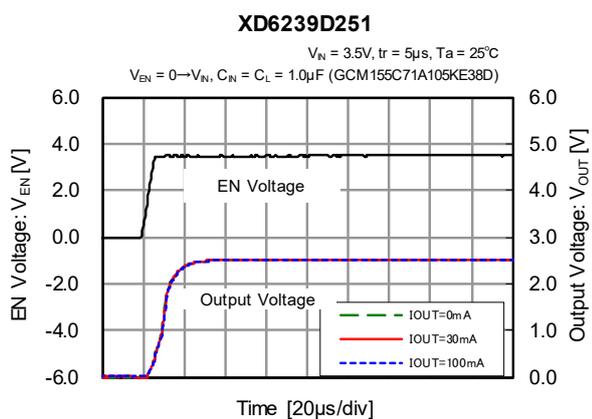
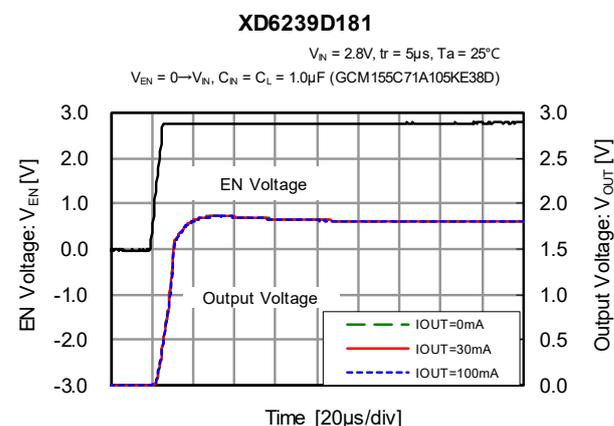
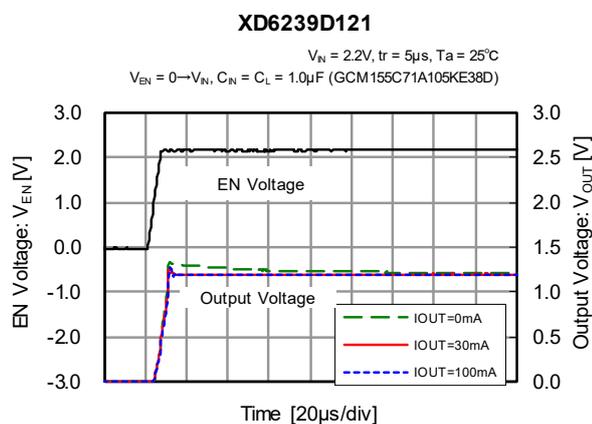


TYPICAL PERFORMANCE CHARACTERISTICS

(8) Input Voltage Rising Response



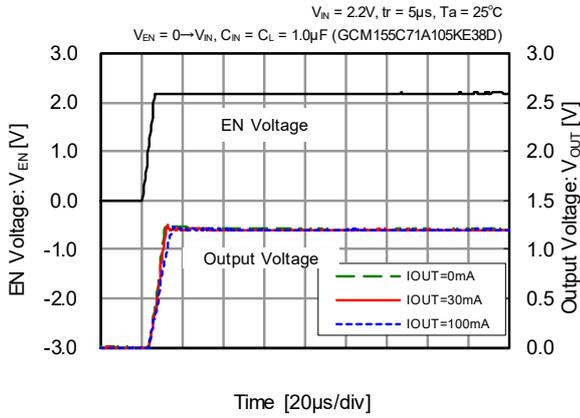
(9-1) EN Rising Response Time (D Type)



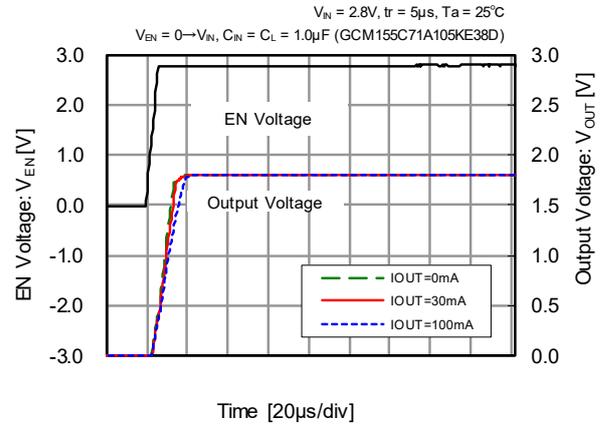
TYPICAL PERFORMANCE CHARACTERISTICS

(9-2) EN Rising Response Time (H Type)

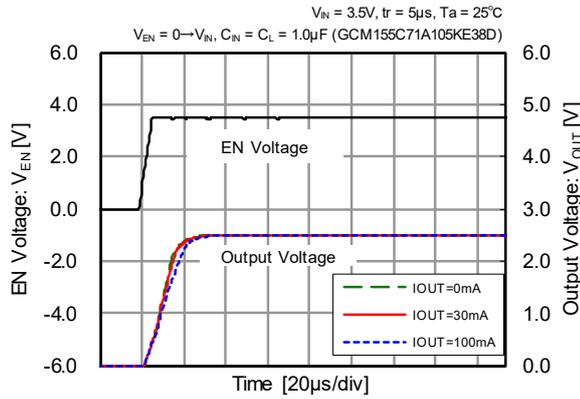
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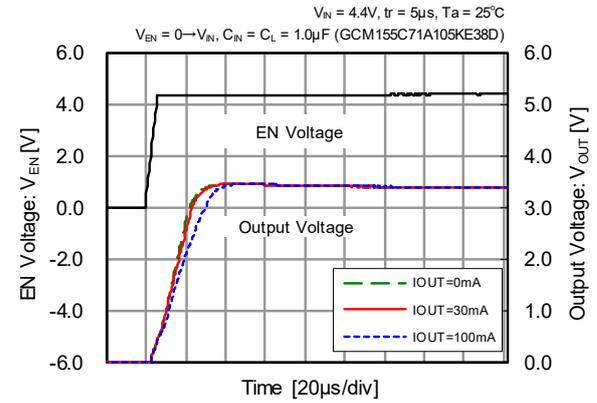
XD6239H181



XD6239H251



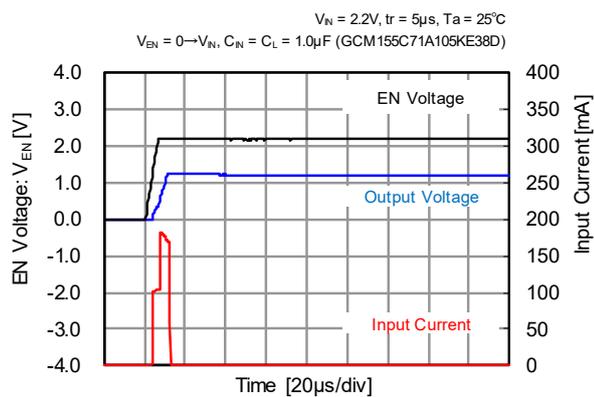
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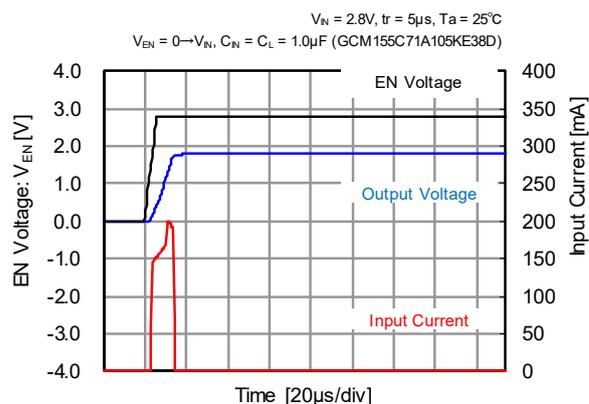
TYPICAL PERFORMANCE CHARACTERISTICS

(10) Inrush Current (H Type)

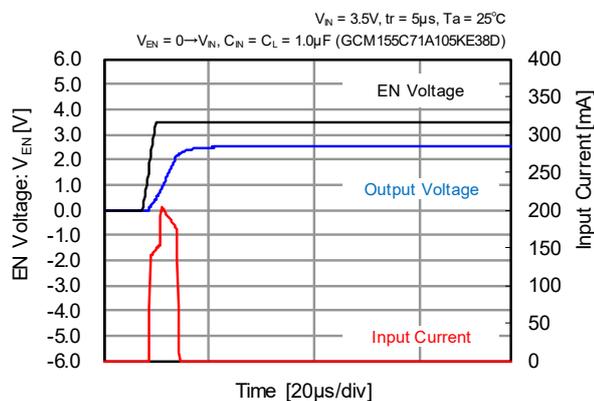
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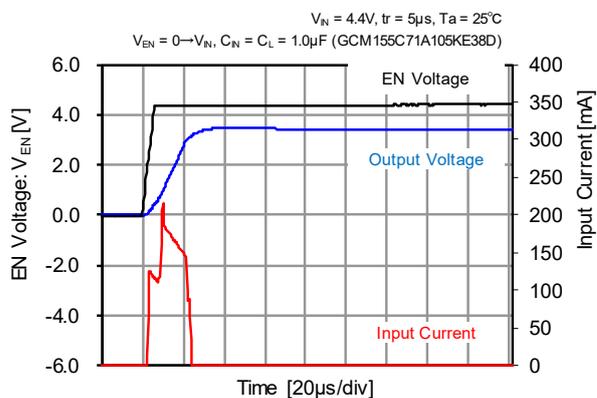
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XD6239H251



XD6239H341

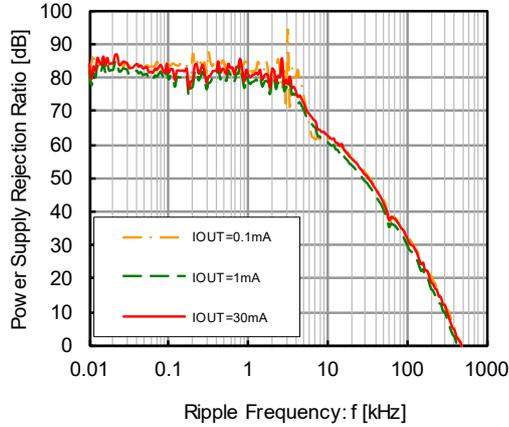


TYPICAL PERFORMANCE CHARACTERISTICS

(11) Power Supply Rejection Ratio

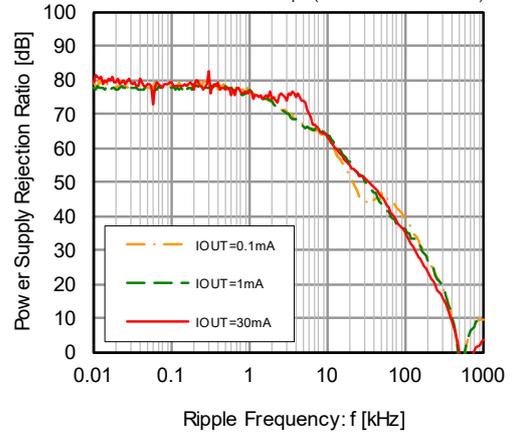
XD6239x121

$T_a = 25^\circ\text{C}$, $V_{IN} = 3.0V_{DC} + 0.5V_{p-pAC}$
 $C_{IN} = 0.1\mu\text{F}$ (GCM155R71A104KA55D),
 $CL = 1.0\mu\text{F}$ (GCM155C71A105KE38D)



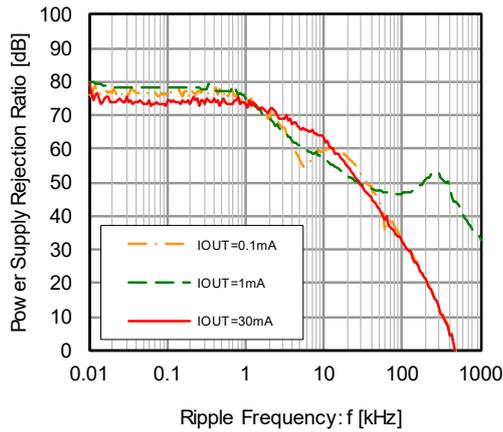
XD6239x181

$T_a = 25^\circ\text{C}$, $V_{IN} = 3.0V_{DC} + 0.5V_{p-pAC}$
 $C_{IN} = 0.1\mu\text{F}$ (GCM155R71A104KA55D),
 $CL = 1.0\mu\text{F}$ (GCM155C71A105KE38D)



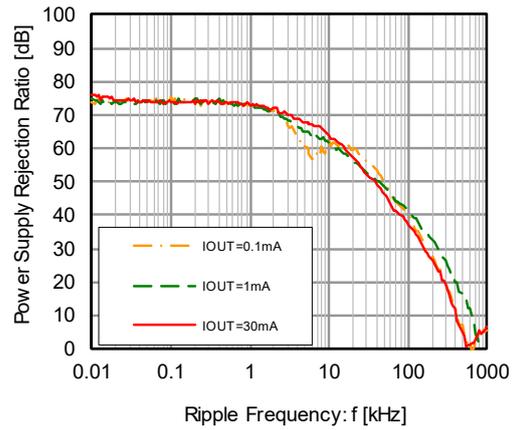
XD6239x251

$T_a = 25^\circ\text{C}$, $V_{IN} = 3.5V_{DC} + 0.5V_{p-pAC}$
 $C_{IN} = 0.1\mu\text{F}$ (GCM155R71A104KA55D),
 $CL = 1.0\mu\text{F}$ (GCM155C71A105KE38D)



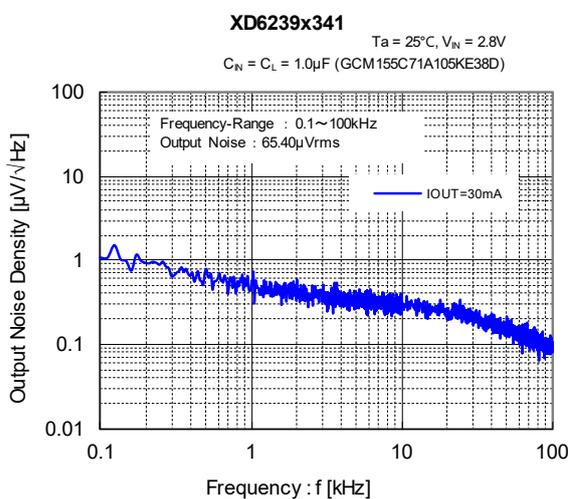
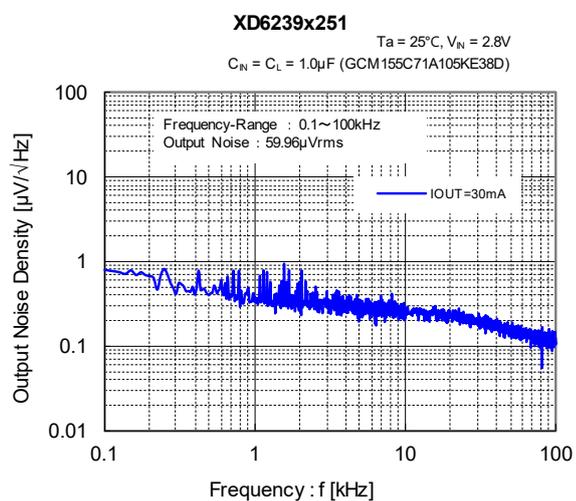
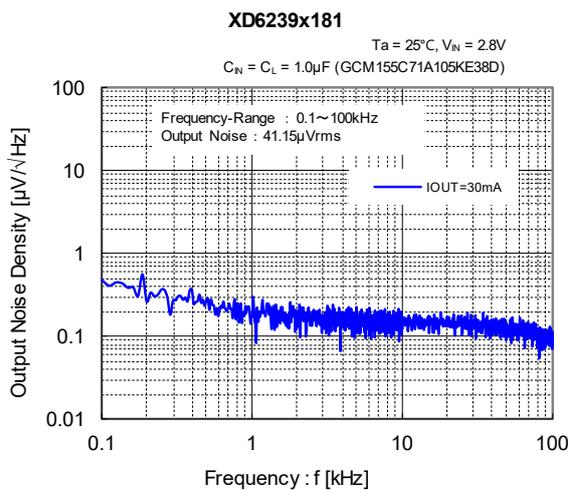
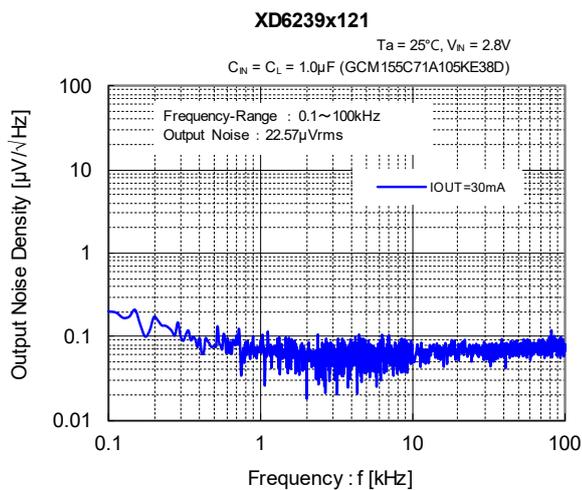
XD6239x341

$T_a = 25^\circ\text{C}$, $V_{IN} = 4.4V_{DC} + 0.5V_{p-pAC}$
 $C_{IN} = 0.1\mu\text{F}$ (GCM155R71A104KA55D),
 $CL = 1.0\mu\text{F}$ (GCM155C71A105KE38D)



TYPICAL PERFORMANCE CHARACTERISTICS

(12) Output Noise Density



■ PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
DFN1010-4C (DAF)	DFN1010-4C PKG	DFN1010-4C Power Dissipation
SOT-25	SOT-25 PKG	SOT-25 Power Dissipation
SOT-89-5	SOT-89-5 PKG	SOT-89-5 Power Dissipation

MARKING RULE

SOT-25/SOT-89-5

① represents products series

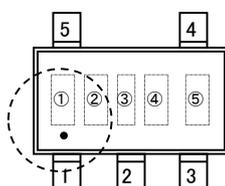
MARK	PRODUCT SERIES
0	XD6239*****-Q

SOT-25(Under dot)

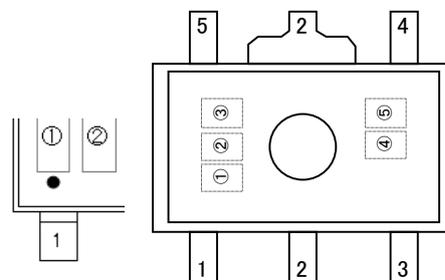
SOT-89-5

② represents products types

MARK	PRODUCT SERIES
R	XD6239D*****-Q
Y	XD6239H*****-Q



Expansion



③ represents output voltage

MARK	Vout (V)						
0	1.2	7	1.9	E	2.6	P	3.3
1	1.3	8	2.0	F	2.7	R	3.4
2	1.4	9	2.1	H	2.8		
3	1.5	A	2.2	K	2.9		
4	1.6	B	2.3	L	3.0		
5	1.7	C	2.4	M	3.1		
6	1.8	D	2.5	N	3.2		

④⑤ represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order. (G, I, J, O, Q, W excluded)

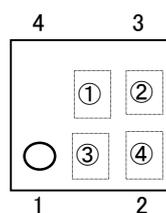
* No character inversion used.

DFN1010-4C

① represents products series

MARK	PRODUCT SERIES
0	XD6239D*****-Q
1	XD6239H*****-Q

DFN1010-4C



② represents output voltage

MARK	Vout (V)						
0	1.2	7	1.9	E	2.6	P	3.3
1	1.3	8	2.0	F	2.7	R	3.4
2	1.4	9	2.1	H	2.8		
3	1.5	A	2.2	K	2.9		
4	1.6	B	2.3	L	3.0		
5	1.7	C	2.4	M	3.1		
6	1.8	D	2.5	N	3.2		

③④ represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order. (G, I, J, O, Q, W excluded)

* No character inversion used.

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