EZ-PD™ CCG7D Automotive USB dual-port Type-C with PD and buck-boost controller

General description

EZ-PD™ CCG7D is a highly integrated dual-port USB Type-C Power Delivery (PD) solution with integrated buck-boost controllers. It complies with the latest USB Type-C and PD specifications, and is targeted for automotive applications such as infotainment head unit charger, rear seat chargers as well as rear seat entertainment. Integration offered by EZ-PD™ CCG7D not only reduces the bill-of-materials (BOM) but also provides a footprint optimized solution for automotive charging needs. It also includes hardware-controlled protection features on the VBUS. EZ-PD™ CCG7D supports a wide input voltage range (4 V–24 V with 40-V tolerance) and programmable switching frequency (150 kHz–600 kHz) in an integrated PD solution.

EZ-PD™ CCG7D is the most programmable USB PD solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128-KB flash, 16-KB RAM, and 32-KB ROM that leaves most flash available for user application use. It also includes various analog and digital peripherals such as ADC, PWMs, and timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, temperature monitoring, and fault logging.

Applications

- Head unit charger
- Rear seat charger (RSC)
- Rear seat entertainment (RSE)

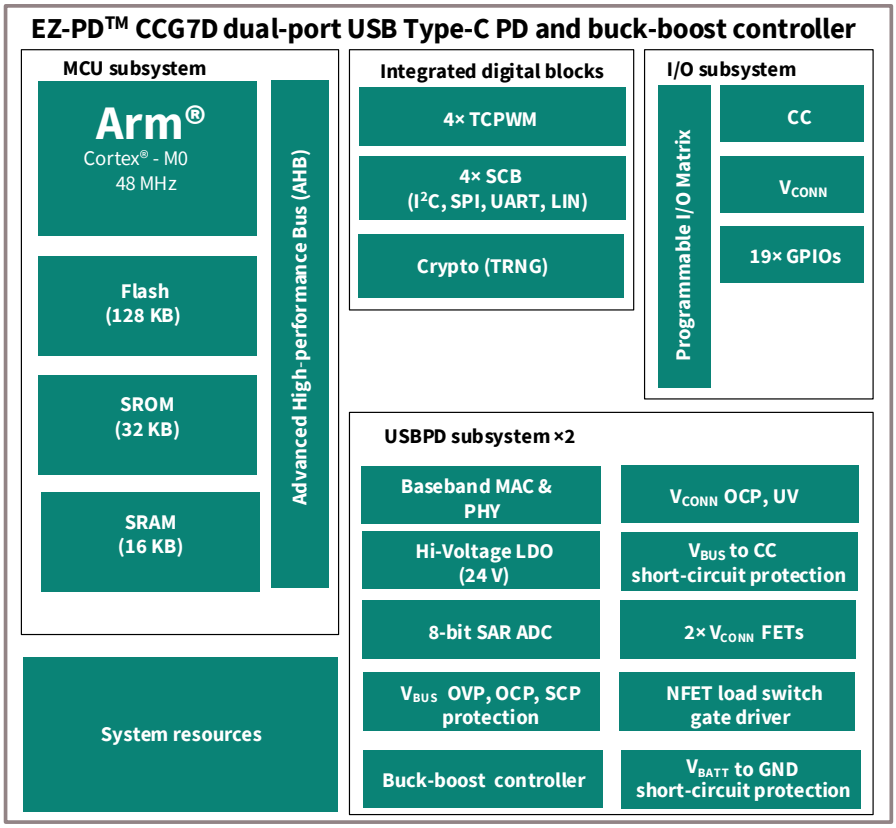
Features

- USB PD
  - Supports two USB PD ports
  - Supports USB PD Revision 3.2 including programmable power supply (PPS) mode
  - Extended data messaging
- Type-C
  - Configurable resistors RP and RD
  - VBUS provider NFET gate driver
  - Integrated 100-mW VCONN power supply and control
- 2× buck-boost controller
  - 150 to 600 kHz switching frequency
  - 5.5 to 24 V input, 40-V tolerant
  - 3.3 to 21.5 V output
  - 20-mV voltage and 50-mA current steps for PPS
  - Supports selectable pulse-skipping mode (PSM) and forced continuous current/conduction mode (FCCM)
  - Supports soft start
  - Programmable spread spectrum frequency modulation for low EMI
  - Programmable phase shift across two ports to further reduce the EMI
- 2× legacy/proprietary charging blocks
  - Supports QC 2.0/3.0/4.0/5.0, Apple charging 2.4A, Samsung adaptive fast charging (AFC), USB BC 1.2

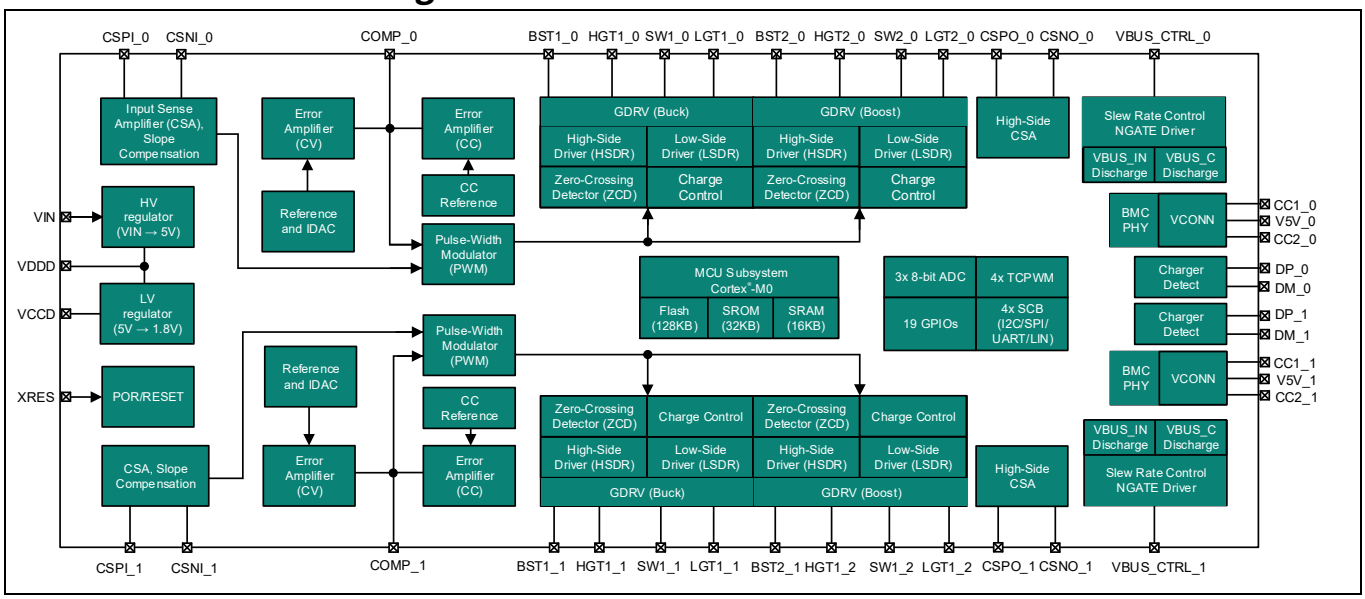
Features

- System-level fault protection
  - On-chip VBUS overvoltage protection (OVP), overcurrent protection (OCP), undervoltage protection (UVP)
  - VBUS to CC short protection
  - VBAT to GND protection FET gate driver
  - Undervoltage lockout (UVLO)
  - Supports overtemperature protection through integrated ADC circuit and internal temperature sensor
  - Supports connector and board temperature measurement using external thermistors
- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0 CPU
  - 128-KB flash
  - 16-KB SRAM
  - 32-KB ROM
- Peripherals and GPIOs
  - 19 GPIOs
  - Two overvoltage GPIOs
  - 3× 8-bit ADC
  - 4× 16-bit timer/counter/PWMs (TCPWM)
- Communication interfaces
  - 4× SCBs (I^2C/SPI/UART/LIN)
- Clocks and oscillators
  - Integrated oscillator eliminating the need for an external clock
- Power supply
  - 4 to 24 V input (40-V tolerant)
  - 3.3 to 21.5 V output
  - Integrated LDO capable of 5 V at 150 mA
- Packages
  - 68-pin QFN, wettable flank, AEC-Q100
  - Supports automotive ambient temperature range (–40°C to +105°C) with 125°C operating junction temperature

Logic block diagram



Functional block diagram



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1 Functional overview

1.1 MCU subsystem

1.1.1 CPU

The Cortex®-M0 in EZ-PD™ CCG7D devices is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. It also includes a hardware multiplier, which provides a 32-bit result in one cycle. It includes an interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode.

1.1.2 Flash ROM and SRAM

EZ-PD™ CCG7D devices have 128-KB flash and 32-KB ROM for non-volatile storage. ROM stores libraries for authentication and device drivers such as I^2C, SPI, and so on. That spares flash for user application. Flash provides the flexibility to store code for any customer feature and allows firmware upgrades to meet the latest USB PD specifications and application needs.

The 16-KB RAM is used under software control to store the temporary status of system variables and parameters. A supervisory ROM that contains boot and configuration routines is provided.

1.2 USBPD subsystem

This subsystem provides the interface to the Type-C USB port. This subsystem comprises:

- USB PD physical layer
- VCONN switches and 100 mW VCONN source
- UVP, OVP on VBUS
- Output high-side current sense amplifier (CSA) for VBUS
- VBUS discharge control
- Gate driver for VBUS provider NFET
- Charger detection block for legacy charging (for example: BC1.2, Apple charging, and so on)
- VBAT to ground short-circuit protection
- VBUS to CC short-circuit protection

1.2.1 USB PD physical layer

The USBPD subsystem contains the USB PD physical layer block and supporting circuits. The USB PD physical layer consists of a transmitter and receiver that communicate BMC encoded data over the CC channel per the PD 3.2 standard. All communication is half-duplex. The physical layer or PHY implements collision avoidance to minimize communication errors on the channel.

The USBPD block includes all termination resistors (Rp and Rd) and their switches as required by the USB Type-C specification. Rp and Rd resistors are required to implement connection detection, plug orientation detection and for the establishment of the USB source/sink roles. The Rp resistor is implemented as a current source.

EZ-PD™ CCG7D device family with accompanying firmware is fully complaint with Revisions 3.2 and 2.0 of the USB PD specification. The device supports PPS operation at all valid voltages from 3.3 to 21 V.

EZ-PD™ CCG7D devices support Rp under HW control in unconnected (standby) state to minimize standby power.

EZ-PD™ CCG7D devices support USB PD Extended Messages containing data of up to 260 bytes. The extended messages are larger than expected by USB PD 2.0 hardware. As per the USB PD protocol specification, devices compliant with USB PD Revision 3.0 and later implement a chunking mechanism; messages are limited to Revision 2.0 sizes unless both source and sink confirm and negotiate compatibility with longer message lengths.

1.2.2 VCONN switches

EZ-PD™ CCG7D's internal LDO voltage regulator is capable of powering a 100 mW VCONN supply for electronically marked cable assemblies (EMCA), VCONN-powered devices (VPD), and VCONN-powered accessories (VPA) as defined in the USB Type-C specification. All circuitry including VCONN switches and OCP is integrated in the device. In the event the VCONN current exceeds the VCONN OCP limit, EZ-PD™ CCG7D can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

1.2.3 VBUS UVP and OVP

VBUS undervoltage and overvoltage faults are monitored using internal resistor dividers. The fault thresholds and response times are user configurable. See **EZ-PD™ Configuration Utility** for more details. In the event of a UVP or OVP, EZ-PD™ CCG7D can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

1.2.4 VBUS OCP and SCP

VBUS overcurrent and short-circuit faults are monitored using internal current sense amplifiers. Similar to OVP and UVP, the OCP and SCP fault thresholds and response times are configurable as well. See **EZ-PD™ Configuration Utility** for more details. In the event of OCP or SCP, EZ-PD™ CCG7D can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

1.2.5 High-side CSA for VBUS

EZ-PD™ CCG7D device family supports VBUS current measurement and control using an external resistor (5 mΩ) in series with the VBUS path. The voltage drop across this resistor is used to measure the average output current. The same resistor is also used to sense and precisely control the output current in the PPS current foldback mode of operation.

1.2.6 VBUS discharge control

The chip supports high-voltage (21.5 V) VBUS discharge circuitry. Upon the detection of device disconnection, faults, or hard resets, the chip will discharge the output VBUS terminals to vSafe5V and/or vSafe0V within the time limits specified in the USB PD Specification.

1.2.7 Gate driver for VBUS provider NFET

EZ-PD™ CCG7D devices have an integrated high-voltage gate driver to drive the gate of an external high-side NFET on the VBUS provider path. The gate driver drives the load switch that controls the connection between VBUS_IN and VBUS_C. VBUS_CTRL is the output of this gate driver. To turn off the external NFET, the gate driver drives VBUS_IN low to 0 V. To turn on the external NFET, it drives the gate to VBUS_IN + 8 V. There is an optional slow turn-on feature which reduces the high-current spikes on the output. For a typical gate capacitance of 3 nF, a slow turn-on time of 2 ms to 10 ms is configurable using firmware.

1.2.8 Legacy charge detection and support

CG7D implements battery charger emulation and detection (source and sink) for USB BC.1.2, legacy Apple charging, Qualcomm Quick Charge 2.0/3.0, and Samsung AFC protocols.

1.2.9 VBAT to ground short protection

EZ-PD™ CCG7D devices can protect against high currents through the Type-C return (ground) path. A NFET and a current sense resistor are placed in series with the ground return path from the Type-C connector as shown in **Figure 1**. This resistor senses the current, and if it exceeds the firmware-configured threshold, the NFET is turned off to interrupt the current. This protects against overcurrent conditions caused by external faults (for example, if the Type-C connector ground is accidentally connected to the car's battery). The current sense can be implemented with either a single-ended connection (referenced to internal ground) or with a true differential connection (see CSN connection in **Figure 1**). The differential connection provides better current measurement accuracy but uses an extra pin that can otherwise be repurposed as a GPIO. In the event of VBAT to ground short protection, EZ-PD™ CCG7D can be configured to shut down the series FET between the Type-C receptacle ground and the system ground. The recovery and retry mechanism can be customized using application firmware.

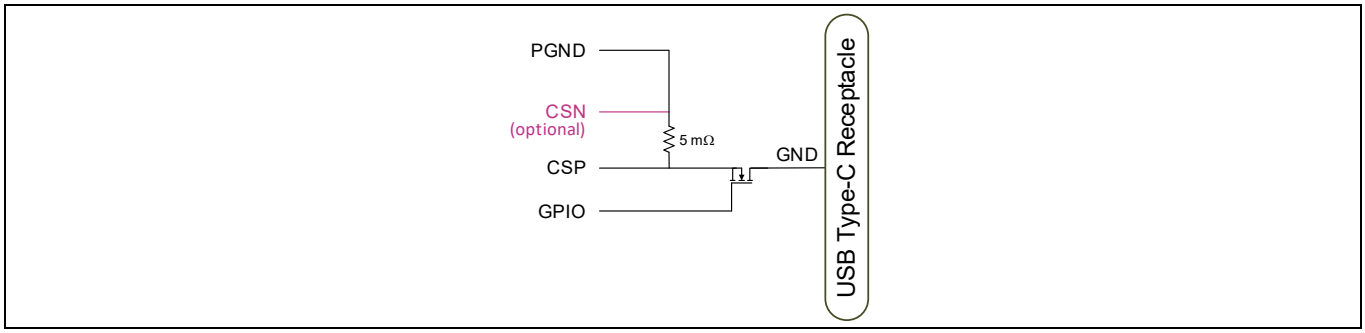


Figure 1 VBUS to ground short circuit protection

1.2.10 VBUS to CC short protection

EZ-PD™ CCG7D's CC pins have integrated protection from accidental shorts to high-voltage VBUS and VBAT. EZ-PD™ CCG7D devices can handle up to 24 V external voltage on its CC pins without damage. In the event an overvoltage is detected on the CC pin, EZ-PD™ CCG7D can be configured to shut down the Type-C port completely. The port will resume normal operation once the CC voltage detected is within normal range.

1.3 Buck-boost subsystem

The buck-boost subsystem in EZ-PD™ CCG7D devices can be configured to operate in buck-boost mode, buck-only mode or boost-only mode. While buck-boost mode requires four external switching FETs, buck-only and boost-only modes require only two FETs. Buck-only mode is useful when EZ-PD™ CCG7D device's port is used for USB Type-A only applications. **Figure 2** shows the buck-boost subsystem's main external components and connections.

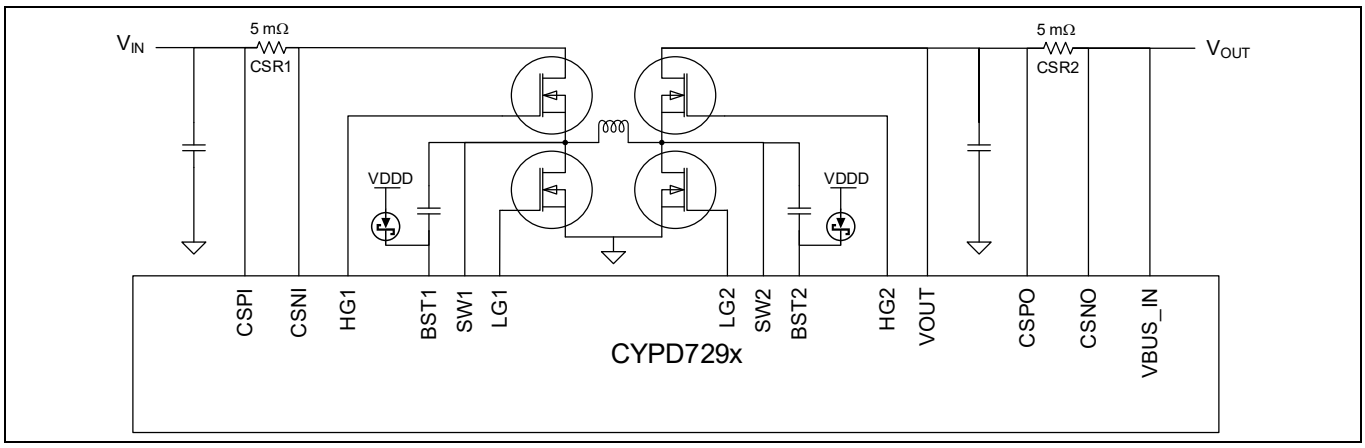


Figure 2 Buck-boost schematic showing external components

Buck-boost subsystem in EZ-PD™ CCG7D devices have the following key functional blocks:

- High-side (cycle-by-cycle) CSA
- High-side and low-side gate driver
- Pulse width modulator (PWM)
- Error amplifier (EA)

1.3.1 High-side (cycle-by-cycle) CSA

EZ-PD™ CCG7D device's buck-boost controller implements peak current control in both boost and buck modes. A high-side CSA is used for peak current sensing through an external resistor (5 mΩ; see CSR1 in **Figure 2**) placed in series with the buck control FET. This current sense amplifier has a high bandwidth and a very wide common mode range. This current sense resistor is connected to the CSA block through pins CSPI and CSNI as shown in **Figure 2**. This block implements slope compensation to avoid sub-harmonic oscillation for the internal current loop. In addition to peak current sensing, it provides a current limit comparator for shutting off the buck-boost converter if the current hits an upper threshold which is programmable.

1.3.2 High-side gate driver and low-side gate driver

EZ-PD™ CCG7D's buck-boost controller provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HG1 and HG2 pins, and two ground referenced low-side drivers at the LG1 and LG2 pin. The high-side gate drivers drive the high-side external FET with a nominal VGS of 5 V. The high-side gate driver has a programmable drive strength to drive external FET. An external capacitor and Schottky diode form a bootstrap network to collect and store the high voltage source (VIN + ~5 V for HG1 and VBUS + ~5 V for HG2) needed to drive the high-side FET.

The low-side gate driver drives the low-side external FET with a nominal VGS of 5 V using energy sourced from EZ-PD™ CCG7D's internal LDO regulator and stored in the capacitor between PVDD and PGND. Low-side gate driver has programmable drive strength to drive external FET.

In addition to drive strength, the high-side gate driver and the low-side gate driver have programmable options for deadtime control and zero-crossing levels. High-side gate driver and low-side gate driver blocks include zero-crossing detector (ZCD) to implement discontinuous-conduction mode (DCM) mode with diode emulation.

The gate drivers for the switching FETs function at their nominal drive voltage levels (5 V) provided the VIN voltage is between 5.5 V and 24 V.

1.3.3 Error amplifier (EA)

EZ-PD™ CCG7D's buck-boost controller contains two error amplifiers for output voltage and current regulation. The error amplifier is a trans-conductance type amplifier with single compensation pin (COMP) to ground for both the voltage and current loops. In voltage regulation, the output voltage is compared with the internal reference voltage and the output of EA is fed to the PWM block. In current regulation, the average current is sensed by VBUS high-side current sense amplifier through the external resistor. The output of the VBUS CSA is compared with an internal reference in error amplifier block and EA output is fed to the PWM block. EZ-PD™ CCG7D's firmware configures and controls the integrated programmable error amplifier circuit for achieving the required VBUS voltage output from the power section.

1.3.4 Pulse width modulator (PWM)

EZ-PD™ CCG7D device family's PWM block generates the control signals for the gate drivers driving the external FETs in peak current mode control. There are many programmable options for minimum/maximum pulse width, minimum/maximum period, frequency and pulse skip levels to optimize the system design.

EZ-PD™ CCG7D devices have two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: PSM and FCCM.

1.3.5 Pulse-skipping mode (PSM)

In pulse-skipping mode, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in "bursts" of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses at the cost of higher output voltage ripple. When in this mode, EZ-PD™ CCG7D devices monitor the voltage across the buck or boost sync FET to detect when the inductor current reaches zero; when this occurs, the EZ-PD™ CCG7D devices switch off the buck or boost sync FET to prevent reverse current flow from the output capacitors (that is, diode emulation mode). Several parameters of this mode are programmable through firmware, allowing the user to strike their own balance between light load efficiency and output ripple.

1.3.6 Forced-continuous-conduction mode (FCCM)

In FCCM, the nominal switching frequency is maintained at all times, with the inductor current going below zero (that is, "backwards" or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

1.4 Buck-boost controller operation regions

The input-side CSA's output is compared with the output of the error amplifier to determine the pulse width of the PWM. PWM block compares the Input voltage and output voltage to determine the buck, boost, and buck-boost regions. The switching time/period of the four gate drivers (HG1, LG1, HG2, LG2) depends upon the region in which the block is operating as well as the mode such as DCM or FCCM. The exact Vin vs Vout thresholds for transitions into and out of each region are adjustable in firmware including the hysteresis.

1.4.1 Buck region operation (VIN >> VBUS)

When the VIN voltage is significantly higher than the required VBUS voltage, EZ-PD™ CCG7D devices operate in the buck region. In this region, the boost side FETs are inactivated, with the boost control FET (connected to LG2) turned off and the boost sync FET (connected to HG2) turned on. The buck side FETs are controlled as a buck converter with synchronous rectification as shown in **Figure 3**.

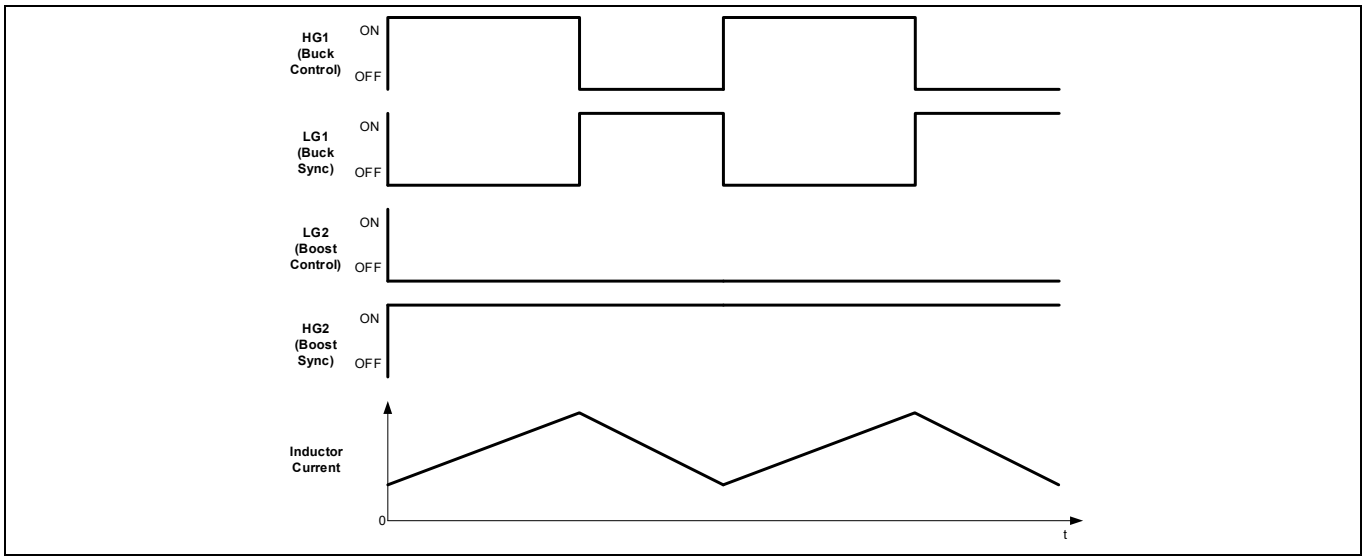


Figure 3 Buck operation waveforms

1.4.2 Boost region operation (VIN << VBUS)

When the VIN voltage is significantly lower than the required VBUS voltage, EZ-PD™ CCG7D devices operate in the boost region. In this region, the buck side FETs are inactivated, with the sync FET turned off and the buck control FET turned on. The boost side FETs are controlled as a boost converter with synchronous rectification as shown in **Figure 4**.

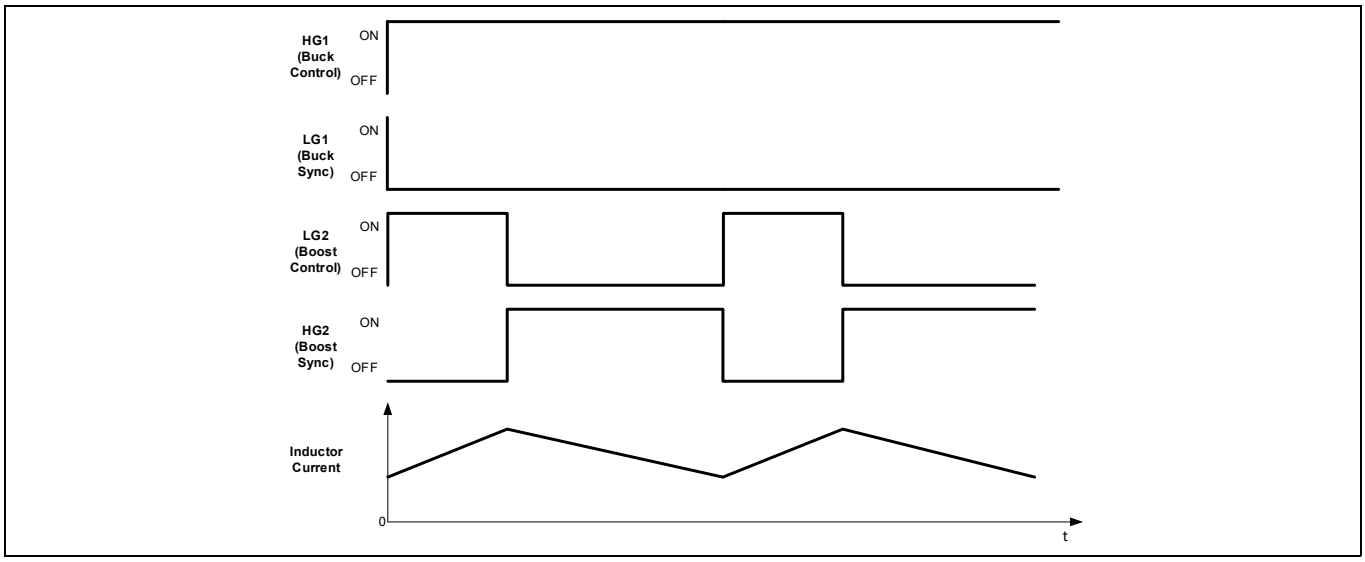


Figure 4 Boost operation waveforms

1.4.3 Buck-boost region 1 operation (VIN ~> VBUS)

When the VIN voltage is slightly higher than the required VBUS voltage, EZ-PD™ CCG7D devices operate in the buck-boost region 1. In this region, the boost side works at a fixed 20% duty cycle (programmable) while the buck side (LG1 / HG1) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 5**.

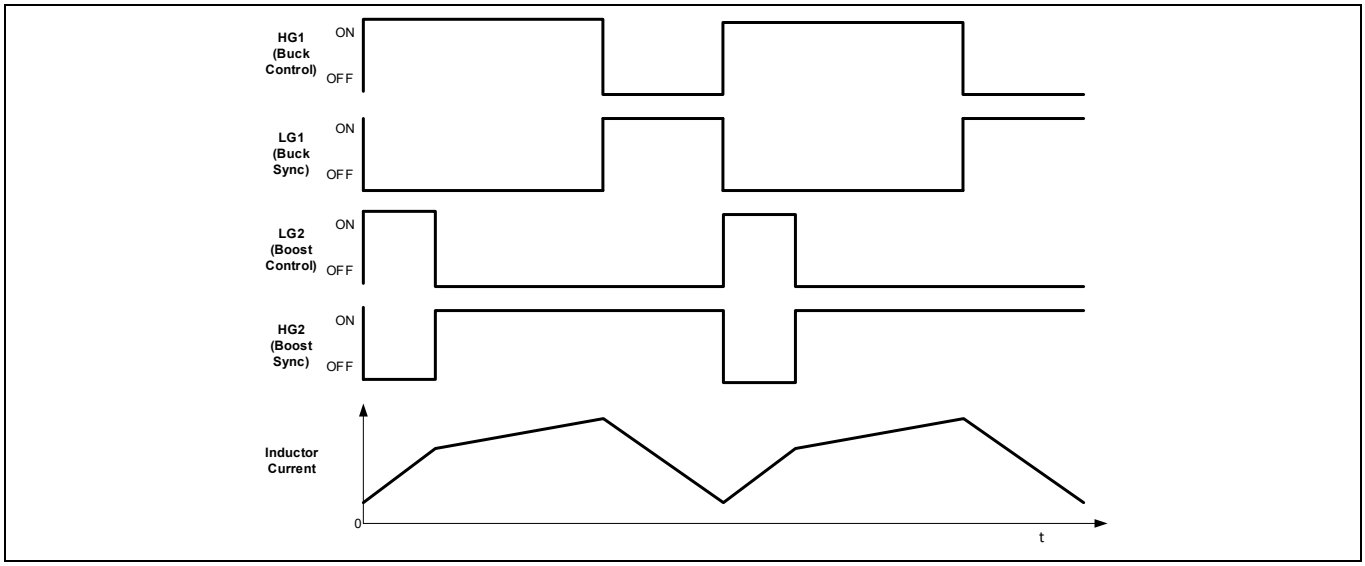


Figure 5 Buck-boost region 1 (VIN ~> VBUS) operation waveforms

1.4.4 Buck-boost region 2 operation (VIN ~< VBUS)

When the VIN voltage is slightly lower than the required VBUS voltage, EZ-PD™ CCG7D devices operate in the buck-boost region 2. In this region, the buck side works at a fixed 80% duty cycle (programmable) while the boost side (LG2) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 6**.

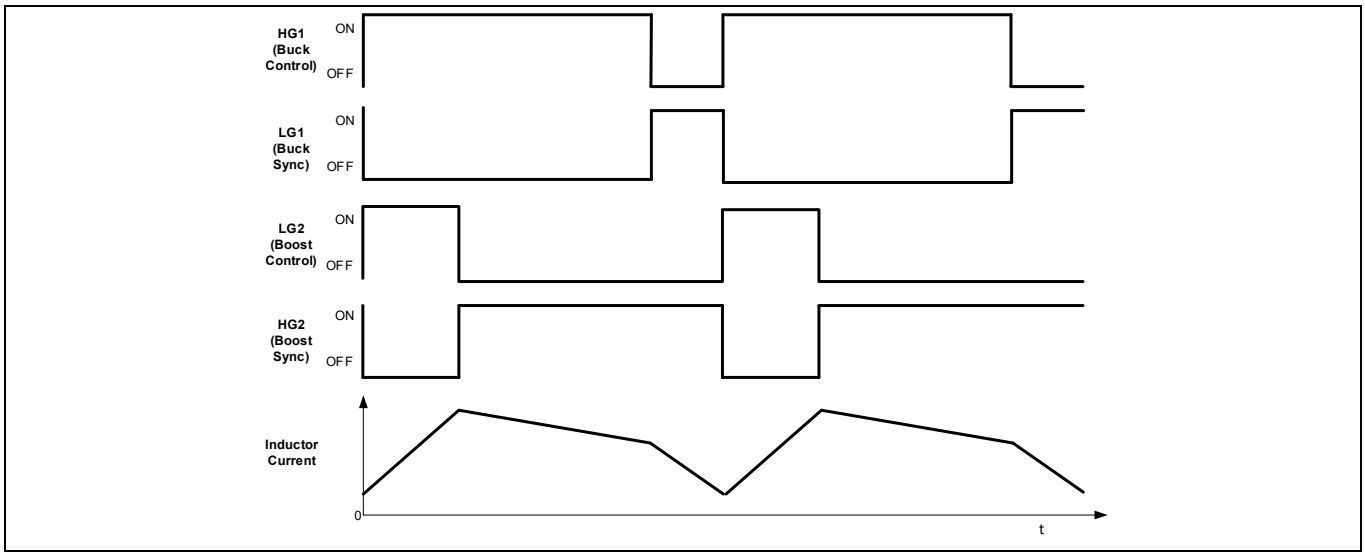


Figure 6 Buck-boost region 2 (VIN ~< VBUS) operation waveforms

1.4.5 Switching frequency and spread spectrum

EZ-PD™ CCG7D devices offer programmable switching frequency between 150 kHz and 600 kHz. The controller supports spread spectrum clocking within the operating frequency range in all operating modes. Spread spectrum is essential for charging applications to meet EMC/EMI requirements by spreading emissions caused by switching over a wide spectrum instead of a fixed frequency, thereby reducing the peak energy at any particular frequency. Both the switching frequency and the spread spectrum span are firmware programmable.

1.5 Analog blocks

1.5.1 ADC

EZ-PD™ CCG7D devices family has three 8-bit SAR ADCs available for general purpose analog-to-digital conversion applications in the chip. The ADCs can be accessed from the GPIOs through an on-chip analog mux. See **Table 30** for detailed specs on the ADCs.

1.6 Integrated digital blocks

1.6.1 Serial communication block (SCB)

EZ-PD™ CCG7D devices have four SCB blocks that can be configured for I^2C, SPI, UART or LIN. These blocks implement full multi-master and slave I^2C interfaces capable of multi-master arbitration. This I^2C implementation is compliant with the standard **NXP I2C Specification V3.0**. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for Receive and Transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The I^2C port I/Os for SCB0 are overvoltage tolerant (OVT). The I^2C ports for SCB1-3 are not OVT tolerant.

1.6.2 Timer, counter, pulse-width modulator (TCPWM)

The TCPWM block of EZ-PD™ CCG7D devices support four timers or counters or pulse-width modulators. These timers are available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

1.7 I/O subsystem

The EZ-PD™ CCG7D devices have 19 GPIOs including the I^2C and SWD pins which can also be used as GPIOs. The GPIO block implements the following:

- Eight output drive modes
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Disabled
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control
- OVT on one pair of GPIOs

During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals such as USB Type-C port are also fixed in order to reduce internal multiplexing complexity. Data output registers and pin state register store, respectively, the values to be driven on the pins and the states of the pins themselves. The configuration of the pins can be done by the programming of registers through software for each digital I/O port.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during Deep Sleep mode or remain ON. If the operation is restored using reset, then the pins shall go the High-Z state. If operation is restored by an interrupt event, then the pin drivers shall retain their state until firmware chooses to change it. The IOs (on data bus) do not draw current on power down.

1.8 System resources

1.8.1 Watchdog timer (WDT)

EZ-PD™ CCG7D devices have a watchdog timer running from the internal low-speed oscillator (ILO). This allows watchdog operation during Deep Sleep and generate a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

1.8.2 Reset

EZ-PD™ CCG7D devices can be reset from a variety of sources including a Software Reset. Reset events are asynchronous and guarantee reversion to a known state. The Reset cause is recorded in a Register, which is sticky through Reset and allows software to determine the cause of the reset. XRES pin is the dedicated pin for reset to apply hardware reset.

1.8.3 Clock system

EZ-PD™ CCG7D devices have a fully integrated clock with no external crystal required. EZ-PD™ CCG7D device's clock system is responsible for providing clocks to all sub-systems that require clocks (SCB and PD) and for switching between different clock sources, without glitches.

The HFCLK signal can be divided down as shown to generate synchronous clocks for the digital peripherals. The clock dividers have 8-bit, 16-bit and 16-bit fractional divide capability. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values. The clock dividers generate either enabled clocks (that is, 1 in N clocking where N is the divisor) or an approximately 50% duty cycle clock (exactly 50% for even divisors, one clock difference in the high and low values for odd divisors).

In **Figure 7**, PERXYZCLK represents the clocks for different peripherals.

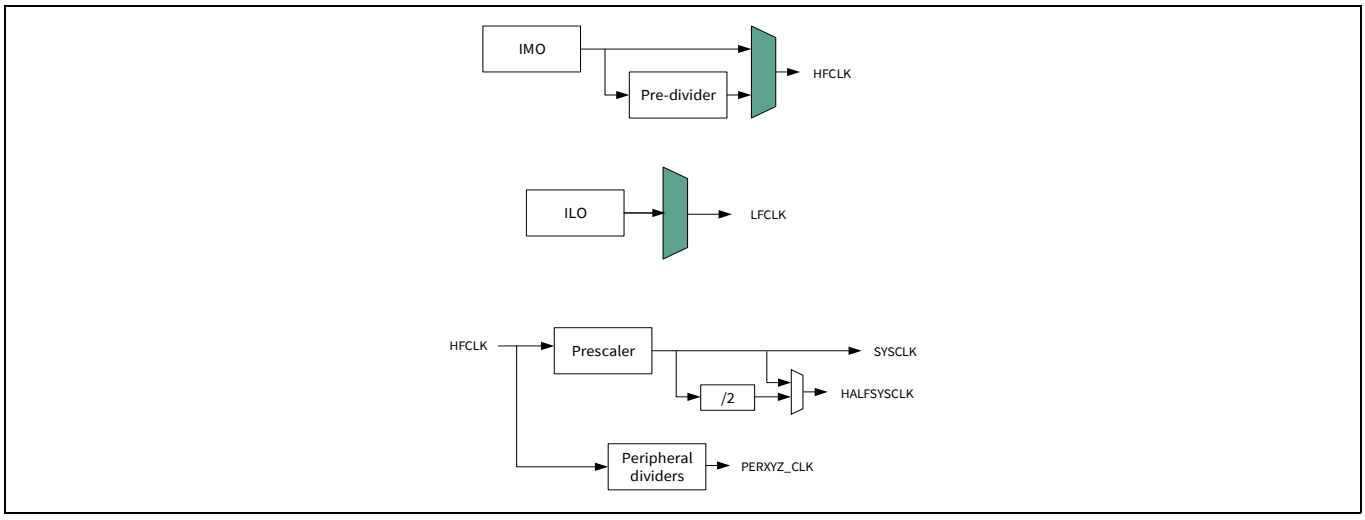


Figure 7 Clocking architecture of EZ-PD™ CCG7D devices

1.8.4 Internal main oscillator (IMO) clock source

The IMO is the primary source of internal clocking in EZ-PD™ CCG7D devices. IMO default frequency for EZ-PD™ CCG7D devices is 48 MHz ±2%.

1.8.5 ILO clock source

The internal low-speed oscillator is a very low power, relatively inaccurate, oscillator, which is primarily used to generate clocks for peripheral operation in USB suspend (Deep Sleep) mode.

2 Power subsystem

Figure 8 shows an overview of the power subsystem architecture for EZ-PD™ CCG7D devices. The power subsystem of EZ-PD™ CCG7D devices operate from VIN supply which can vary from 4 V to 24 V. The VDDD pin, the output of 5 V LDO gets input from VIN supply. The VDDD pin can also be used as a power supply for external loads up to 150 mA. EZ-PD™ CCG7D devices have two different power modes: Active and Deep Sleep, transitions between which are managed by the power system. The VCCD pin, the output of the core (1.8 V) regulator, is brought out for connecting a 0.1-µF capacitor for the regulator stability only. This pin is not supported as a power supply for external load.

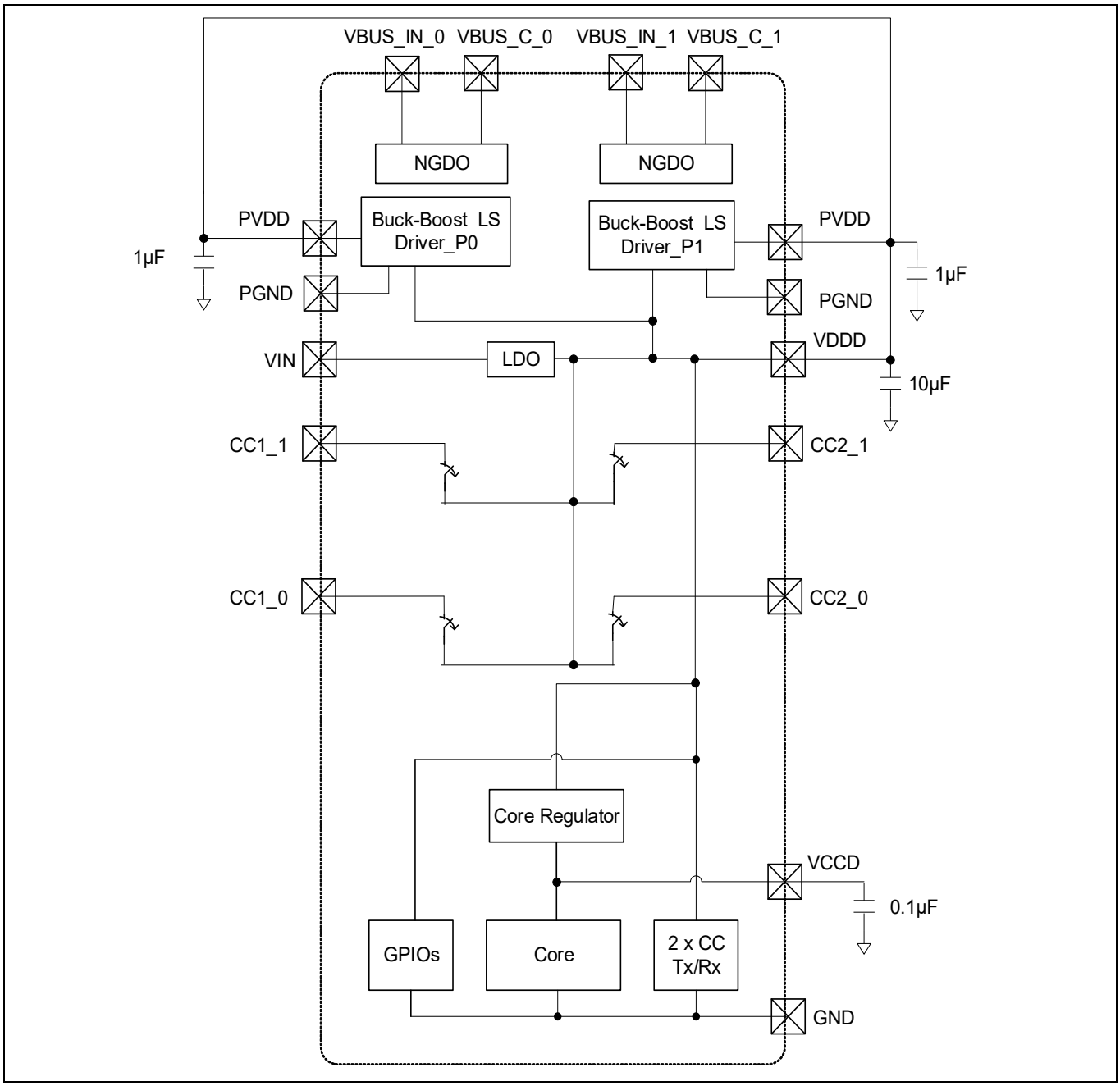


Figure 8 Power system requirement block diagram

2.1 VIN undervoltage lockout (UVLO)

EZ-PD™ CCG7D supports UVLO to allow the device to shut down when the input voltage is below the reliable level. It guarantees predictable behavior when the device is up and running.

2.2 Using external VDDD supply

By default, external VDDD is not supported for EZ-PD™ CCG7D devices. However, usage of external VDDD supply can be enabled using firmware. The pre-requisite for enabling external forcing of VDDD is to always maintain Vin higher than VDDD and the external load on VDDD pin of EZ-PD™ CCG7D devices should never be higher than prescribed load capability of internal VDDD LDO.

2.3 Power modes

Table 1 lists the power modes of the device accessible and observable by the user.

Table 1 Power modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or sleep controller is sequencing the system out of reset
ACTIVE	Power is valid and CPU is executing instructions
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available
XRES	Power is valid and XRES is asserted. Core is powered down

3 Pin list

Table 2 EZ-PD™ CCG7D pinout table

Pin#	Pin name	GPIO port assignment	Description
1	SW1_0	–	Negative power rail of port 0 buck high-side gate driver. This is also connected to one input terminal of zero current detection of buck low-side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
2	LG1_0		Buck low-side gate driver output of Port 0. Connect to the buck (input) side sync (low side) FET gate. Use a wide trace to minimize inductance of this connection.
3	PGND_0		Ground of low-side gate driver of Port 0. This is also connected to one input terminal of zero current detection (ZCD) of buck low-side gate driver. Connect directly to Port 0's board ground plane.
4	PVDD_0		Supply of low-side gate driver of Port 0. Connect to VDDD. Use 1 µF and 0.1 µF bypass capacitors as close to the EZ-PD™ CCG7D IC as possible.
5	LG2_0		Boost low-side gate driver output of Port 0. Connect to the boost (output) side control (low side) FET gate. Use a wide trace to minimize inductance of this connection.
6	VOUT_0		Output of the buck-boost converter of Port 0. This is also connected to one input terminal of reverse current protection (RCP) of Boost high-side gate driver. Connect to the boost sync (high side) FET's drain. Use a dedicated (Kelvin) trace for this connection.
7	SW2_0		Negative power rail of Port 0 boost high-side gate driver. This is also connected to one input terminal of RCP of boost high-side gate driver Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
8	HG2_0		Boost high-side gate driver output of Port 0. Connect to the boost (output) side sync (high side) FET gate. Use a wide trace to minimize inductance of this connection.
9	BST2_0		Boosted power supply of Port 0 boost high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST2_0. Also, connect a bootstrap capacitor from this pin to SW2_0.
10	COMP_0		EA output pin of Port 0. Connect a compensation network to GND. Contact Infineon for assistance in designing the compensation network.
11	CSPO_0		Positive input of output current sensing amplifier of Port 0. Connect to positive terminal of the output current sense resistor.
12	CSNO_0		Negative input of output current sensing amplifier of Port 0. Connect to negative terminal of the output current sense resistor.
13	VBUS_IN_0		Input of feedback voltage of error amplifier of Port 0. Connect to the VBUS node between the output current sense resistor and the VBUS provider NFET.
14	VBUS_C_0		Type-C connector VBUS voltage of Port 0. Connect to the Type-C connector's VBUS pin.
15	CC1_0		Type-C connector configuration channel 1 of Port 0. Connect directly to the CC1 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground.
16	CC2_0		Type-C connector configuration channel 2 of Port 0. Connect directly to the CC2 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground.
17	VBUS_CTRL_0		VBUS NFET gate driver output of Port 0. Connect to the provider NFET's gate.
18	CSN_0_GPIO0	P0.0	GPIO / negative input terminal of Port 0's VBAT – GND protection circuit. Connect to the negative terminal of the VBAT – GND short protection current sense resistor.
19	CSP_0_GPIO1	P0.1	GPIO/ positive input terminal of Port 0's VBAT – GND protection circuit. Connect to the positive terminal of the VBAT – GND short protection current sense resistor.

Table 2 EZ-PD™ CCG7D pinout table *(continued)*

Pin#	Pin name	GPIO port assignment	Description
20	GPIO2	P0.2	GPIO. This GPIO is pulled-down during reset/power-up, as it is used to disable the FET for the Vbat to GND short circuit protection for Port 0. Set the correct drive mode, if the Vbat to GND short circuit protection is not required in the design.
21	GPIO3	P0.3	GPIO
22	GPIO4	P0.4	
23	DP_0_GPIO5	P1.0	USB D+ of Port 0 / GPIO: D+ for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7D does not support USB data transmission on this pin.
24	DM_0_GPIO6	P1.1	USB D- of Port 0 / GPIO: D- for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7D does not support USB data transmission on this pin.
25	VDDD	–	5-V LDO output. Connect a 1-µF ceramic bypass capacitor to this pin. Also, connect this pin directly to pin 63.
26	DM_1_GPIO7	P1.2	USB D- of port 1/GPIO: D- for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7D does not support USB data transmission on this pin.
27	DP_1_GPIO8	P1.3	USB D+ of port 1/ GPIO: D+ for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7D does not support USB data transmission on this pin.
28	XRES	–	External reset – Active low. Contains a 3.5 KΩ to 8.5 KΩ internal pull-up.
29	GPIO9	P2.0	GPIO
30	GPIO10	P2.1	
31	GPIO11	P1.4	GPIO. This GPIO is pulled-down during reset/power-up, as it is used to disable the FET for the Vbat to GND short circuit protection for Port 1. Set the correct drive mode, if the Vbat to GND short circuit protection is not required in the design.
32	CSP_1_GPIO12	P1.5	GPIO / positive terminal of low-side current sense amplifier (LS CSA) of Port 1. Connect to the positive terminal of the VBAT – GND short protection current sense resistor.
33	CSN_1_GPIO13	P1.6	GPIO / negative terminal of low-side CSA of Port 1. Connect to the negative terminal of the VBAT – GND short protection current sense resistor.
34	GND	–	Chip ground. Connect directly to the exposed pad (EPAD) and to pin 64.
35	VBUS_CTRL_1		VBUS NFET gate driver output of Port 1. Connect to the provider NFET's gate.
36	CC2_1		Type-C connector configuration channel 2 of Port 1. Connect directly to the CC2 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground.
37	CC1_1		Type-C connector configuration channel 1 of Port 1. Connect directly to the CC1 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground.
38	VBUS_C_1		Type-C connector BUS voltage of Port 1. Connect to the Type-C connector's VBUS pin.
39	VBUS_IN_1		Input of feedback voltage of error amplifier of Port 1. Connect to the VBUS node between the output current sense resistor and the VBUS provider NFET.
40	CSNO_1		Negative input of output CSA of Port 1. Connect to negative terminal of the output current sense resistor.
41	CSPO_1		Positive input of output CSA of Port 1. Connect to positive terminal of the output current sense resistor.
42	COMP_1		EA output pin of Port 1. Connect a compensation network to GND. Contact Infineon for assistance in designing the compensation network.
43	BST2_1		Boosted power supply of Port 1 boost high-side gate driver. Connect Schottky diode from VDDD to BST2_1. Bootstrap capacitor node. Also, connect a bootstrap capacitor from this pin to SW2_1.
44	HG2_1		Boost high-side gate driver output of Port 1. Connect to the boost (output) side sync (high side) FET gate. Use a wide trace to minimize inductance of this connection.

Table 2 EZ-PD™ CCG7D pinout table *(continued)*

Pin#	Pin name	GPIO port assignment	Description
45	SW2_1	–	Negative power rail of Port 1 boost high-side gate driver. This is also connected to one input terminal of RCP of boost high-side gate driver. Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
46	VOUT_1		Output of the buck-boost converter of Port 1. This is also connected to one input terminal of RCP of boost high-side gate driver. Connect to the boost sync (high side) FET's drain. Use a dedicated (Kelvin) trace for this connection.
47	LG2_1		Boost low-side gate driver output of Port 1. Connect to the boost (output) side control (low side) FET gate. Use a wide trace to minimize inductance of this connection.
48	PVDD_1		Supply of low-side gate driver of Port 1. Connect to VDDD. Use a 1 µF and 0.1 µF bypass capacitors as close to the EZ-PD™ CCG7D device as possible.
49	PGND_1		Ground of low-side gate driver of port 1. This is also connected to one input terminal of zero current detection of buck low-side gate driver. Connect directly to Port 0's board ground plane.
50	LG1_1		Buck low-side gate driver output of Port 1. Connect to the buck (input) side sync (low side) FET gate. Use a wide trace to minimize inductance of this connection.
51	SW1_1		Negative power rail of Port 1 buck high-side gate driver. This is also connected to one input terminal of zero current detection of buck low-side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
52	HG1_1		Buck high-side gate driver output of Port 1. Connect to the buck (input) side control (high side) FET gate. Use a wide trace to minimize inductance of this connection.
53	BST1_1		Boosted power supply of Port 1 buck high-side gate driver. Connect Schottky diode from VDDD to BST1_1. Bootstrap capacitor node.
54	CSNI_1		Negative input of input CSA of Port 1. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
55	CSPI_1		Positive input of input CSA of Port 1. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
56	GPIO14/SWD_DAT	P3.0	GPIO/SWD programming and debug data signal
57	GPIO15/SWD_CLK	P3.1	GPIO/SWD programming and debug clock signal
58	GPIO16	P3.2	GPIO
59	GPIO17	P3.3	
60	GPIO18	P3.4	
61	VIN	–	4 V–24 V Input supply. Connect a ceramic bypass capacitor to GND close to this pin.
62	VCCD		1.8-V core LDO output. Connect a 0.1-µF bypass capacitor to ground. Do not connect anything else to this pin.
63	VDDD		5-V LDO output. Connect to pin 25. Also connect a 10-µF bypass capacitor to this pin.
64	GND		Chip ground. Connect to the EPAD and to pin 34.
65	CSPI_0		Positive input of input CSA of Port 0. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
66	CSNI_0		Negative input of input CSA of Port 0. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
67	BST1_0		Boosted power supply of Port 0 buck high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST1_0. Also, connect a bootstrap capacitor from this pin to SW1_0.
68	HG1_0		Buck high-side gate driver output of Port 0. Connect to the buck (input) side control (high side) FET gate. Use a wide trace to minimize inductance of this connection.
	EPAD		Exposed ground pad. Connect directly to pins 34 and 64.

Table 3 GPIO pins and functionality

68-QFN		SCB function				TCPWM		Fault protection
Pin	GPIO#	UART	SPI	I2C	Analog	ACT #0	ACT#1	
18	CSN_0_GPIO0	scb[1].uart_cts:0	scb[1].spi_select0:0	–	amuxbus_a/b	tcpwm.line[1]:0	tcpwm.tr_compare_match[1]:0	–
19	CSP_0_GPIO1	scb[2].uart_rts:0	scb[2].spi_miso:0	–	amuxbus_a/b	tcpwm.line[0]:0	tcpwm.tr_compare_match[0]:0	–
20	GPIO2	scb[2].uart_cts:0	scb[2].spi_mosi:0	–	amuxbus_a/b	-	–	usbpd[0].fault_gpio0
21	GPIO3	scb[2].uart_rx:0	scb[2].spi_clk:0	scb[2].i2c_scl:0	amuxbus_a/b	tcpwm.line[0]:2	–	–
22	GPIO4	scb[2].uart_tx:0	scb[2].spi_select0:0	scb[2].i2c_sda:0	amuxbus_a/b	tcpwm.line[1]:2	–	–
23	DP_0_GPIO5	scb[0].uart_cts:0	scb[0].spi_mosi:0	–	amuxbus_a/b	tcpwm.line[2]:2	–	–
24	DM_0_GPIO6	scb[0].uart_rts:0	scb[0].spi_select0:0	–	amuxbus_a/b	tcpwm.line[3]:2	–	–
26	DM_1_GPIO7	–	–	–	amuxbus_a/b	–	–	usbpd[1].fault_gpio1
27	DP_1_GPIO8	–	–	–	amuxbus_a/b	–	–	usbpd[0].fault_gpio1
29	GPIO9	scb[0].uart_tx:0	scb[0].spi_miso:0	scb[0].i2c_sda:0	amuxbus_a/b	–	–	–
30	GPIO10	scb[0].uart_rx:0	scb[0].spi_clk:0	scb[0].i2c_scl:0	amuxbus_a/b	–	–	–
31	GPIO11	scb[1].uart_tx:0	scb[1].spi_mosi:0	scb[1].i2c_sda:0	amuxbus_a/b	tcpwm.line[2]:0	–	usbpd[1].fault_gpio0
32	CSP_1_GPIO12	scb[1].uart_rx:0	scb[1].spi_clk:0	scb[1].i2c_scl:0	amuxbus_a/b	tcpwm.line[3]:0	tcpwm.tr_compare_match[3]:0	–
33	CSN_1_GPIO13	scb[1].uart_rts:0	scb[1].spi_miso:0	-	amuxbus_a/b	–	tcpwm.tr_compare_match[2]:0	–
56	GPIO14	scb[3].uart_tx:0	scb[3].spi_miso:0	scb[3].i2c_sda:0	amuxbus_a/b	tcpwm.line[0]:1	tcpwm.tr_compare_match[0]:1	–
57	GPIO15	scb[3].uart_rx:0	scb[3].spi_clk:0	scb[3].i2c_scl:0	amuxbus_a/b	tcpwm.line[1]:1	tcpwm.tr_compare_match[1]:1	–
58	GPIO16	scb[3].uart_cts:0	scb[3].spi_mosi:0	–	amuxbus_a/b	tcpwm.line[2]:1	tcpwm.tr_compare_match[2]:1	–
59	GPIO17	scb[3].uart_rts:0	scb[3].spi_select0:0	–	amuxbus_a/b	tcpwm.line[3]:1	tcpwm.tr_compare_match[3]:1	–
60	GPIO18	–	–	–	amuxbus_a/b	–	–	–

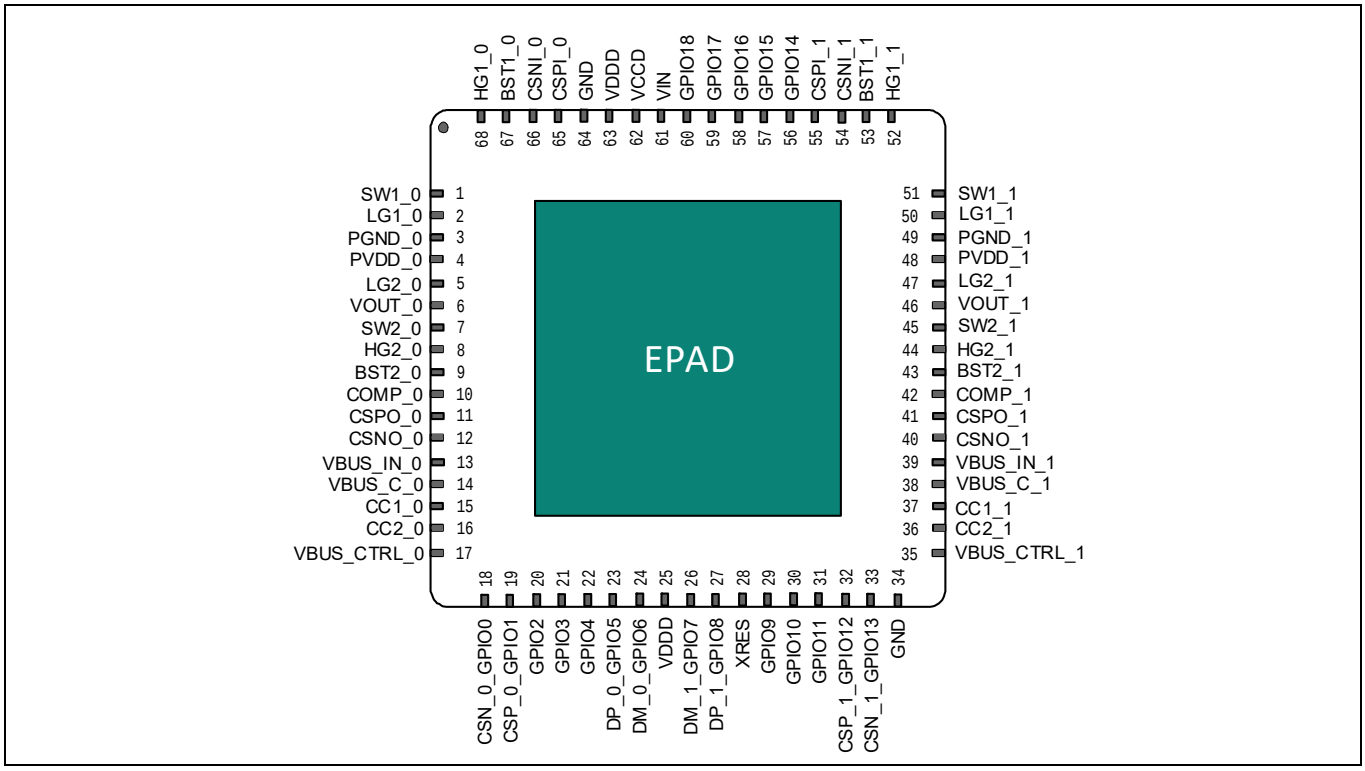


Figure 9 EZ-PD™ CCG7D 68-QFN pinout

4 EZ-PD™ CCG7D programming and bootloading

There are two ways to program application firmware into a CCG7D device:

1. Programming the device flash over SWD interface
2. Application firmware update over specific interfaces (CC, I2C)

Generally, the EZ-PD™ CCG7D devices are programmed over SWD interface only during development or during the manufacturing process of the end-product. Once the end-product is manufactured, the EZ-PD™ CCG7D device's application firmware can be updated via the appropriate bootloader interface. Infineon strongly recommends to use the **EZ-PD™ Configuration Utility** to turn off the application firmware update over CC or I2C interface in the firmware that is updated into EZ-PD™ CCG7D's flash before mass production. This prevents unauthorized firmware from being updated over CC interface in the field. If you desire to retain the application firmware update over CC/ I2C interfaces feature post-production for on-field firmware updates, contact **Infineon Sales** for further guidelines.

4.1 Programming the device flash over SWD interface

The EZ-PD™ CCG7D family of devices can be programmed using the SWD interface. Infineon provides programming kits (**CY8CKIT-002 MiniProg3 Kit**) called MiniProg3 and (**CY8CKIT-005 MiniProg4 Kit**) MiniProg4 which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in **PSOC™ Creator**. Click **here** for more information on how to use the MiniProg3 programmer. Click **here** for more information on how to use the MiniProg4 programmer. There are many third-party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in **Figure 10**, the SWD_DAT and SWD_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pins of EZ-PD™ CCG7D device. If the EZ-PD™ CCG7D device is powered using an on-board power supply, it can be programmed using the "Reset Programming" option. For more details, see **CYPDXXXX Programming Specifications**.

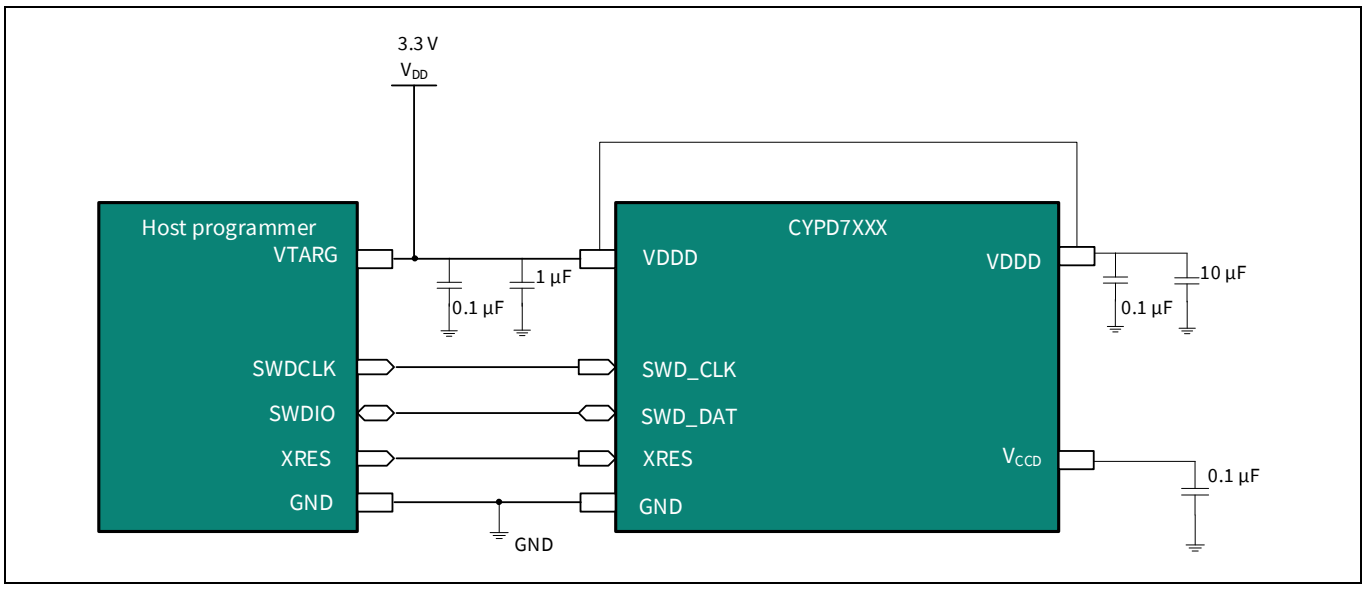


Figure 10 Connecting the programmer to CYPD7XXX device

4.2 Application firmware update using bootloader

There are two kinds of bootloader options available in EZ-PD™ CCG7D:

- CC and I2C bootloader – This bootloader has the GPIO 4, Pin 22 set to strong drive low to drive the FET for VBAT to GND short-circuit protection. VBUS_CTRL pin in the bootloader is configured to control the provider FET. The bootloader will work for designs with and without provider FET
- LIN bootloader – EZ-PD™ CCG7D parts will ship with the CC and I2C bootloader programmed at the factory

4.2.1 Application firmware update over CC interface

For bootloading EZ-PD™ CCG7D applications over the CC interface, the **CY4532 EVK** or **CCPROG PAT: USB-C Power Adapter Programmer and Tester** is used to send programming and configuration data as Infineon-specific vendor defined messages (VDMs) over the CC line. The CY4532 EVK's power board or PAT tester is connected to the system containing EZ-PD™ CCG7D device on one end and a Windows PC running the EZ-PD™ Configuration Utility as shown in **Figure 11** on the other end to boot load the EZ-PD™ CCG7D device.

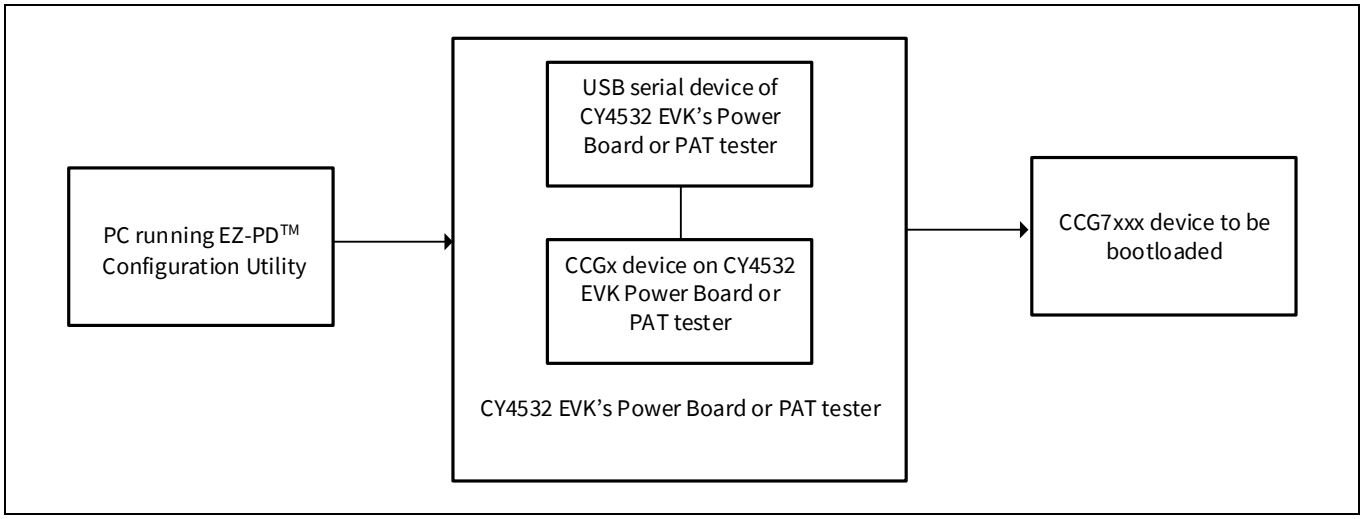


Figure 11 Application firmware update over CC interface

The application firmware (FW) update feature over CC interface is intended for use during development and manufacturing. Infineon strongly recommends customers to use the **EZ-PD™ Configuration Utility** to turn off the application FW update over CC interface in the firmware that is updated into EZ-PD™ CCG7D's flash before mass production. This prevents unauthorized firmware from being updated over CC-interface in the field. See the knowledge base article **KBA230192** on how to configure this in EZ-PD™ Configuration Utility. If you desire to retain the application firmware update over CC interface feature post-production for on-field firmware updates, contact **Infineon support** for further guidelines on how to use authenticated CC bootloader.

4.2.2 Application firmware update over I2C interface

The default bootloader supports both CC and I2C interface. For boot loading EZ-PD™ CCG7D applications over the I2C interface, any host processor can implement the legacy boot commands. Contact **Infineon support** for further details regarding the host processor implementation. The connections between the host processor and EZ-PD™ CCG7D for the bootloading via I2C interface is shown in **Figure 12**.

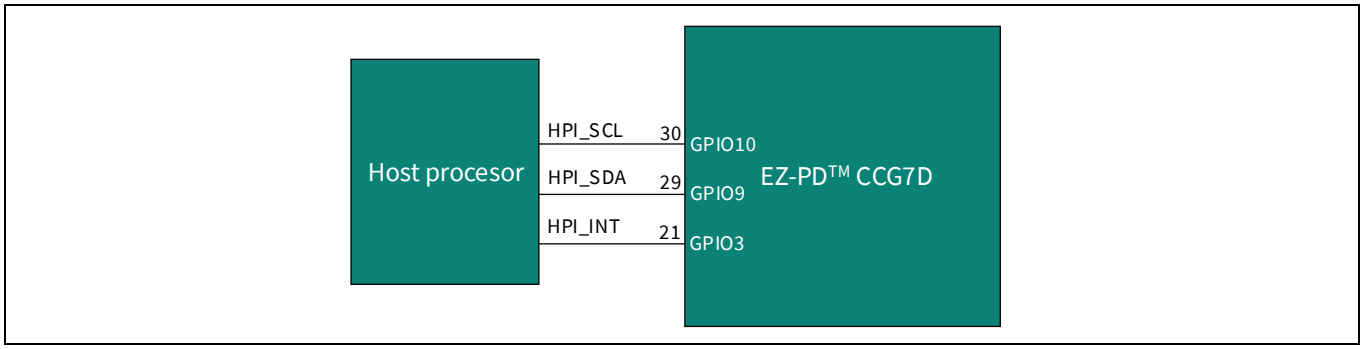


Figure 12 GPIO mapping for the application firmware update over I2C interface

4.2.3 Application firmware update over LIN interface

The LIN-based bootloader supports firmware and configuration updates over LIN interface using HPI. The Command sequence is same for all the bootloader interfaces irrespective of the underlying communication protocol (CC/I2C/LIN). The LIN bootloader will support standard diagnostic commands over UDS protocol thereby enabling easy integration with automotive LIN Network and helping in reduced design cycle time for customers. The default baud rate in the LIN bootloader is 19200. The connections between the LIN transceiver and EZ-PD™ CCG7D for the bootloading via LIN interface is shown in **Figure 13**.

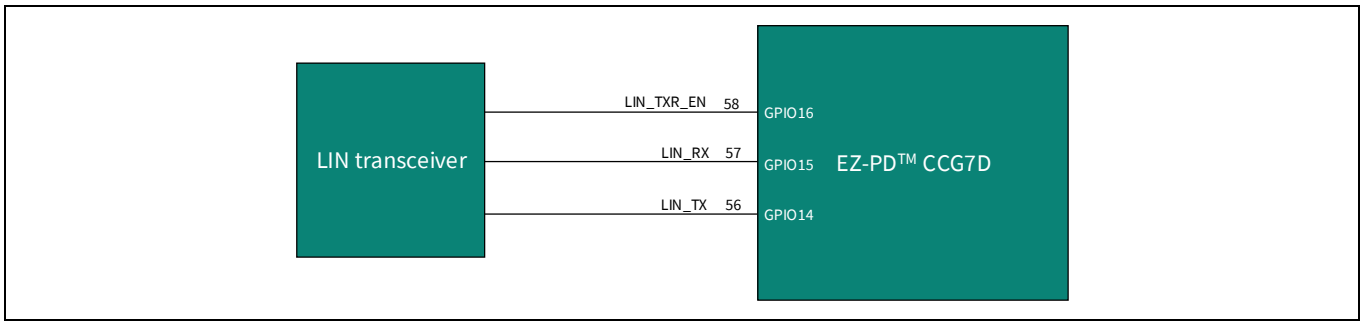


Figure 13 GPIO mapping for the application firmware update over LIN interface

5 Applications

Figure 14 shows a typical head unit charger application block diagram using EZ-PD™ CCG7D. A head unit charger (also known as center stack) is located prominently in the center of the dashboard or console. They are powered by the car battery and are used for charging the mobile/tablet and for media transfer using USB data communications. In this application, EZ-PD™ CCG7D will always be in DFP role supporting the charging of the device. It negotiates the power with the connected device and uses the integrated buck-boost controller to supply the required voltage and current.

The DP/DM lines of the Type-C receptacles are connected to the host processor/hub, for data connectivity to the head unit (HU). These pins are also connected to EZ-PD™ CCG7D to support legacy charging protocol BC v1.2 CDP. The I^2C interface is used to interface with the host processor/hub, to support host processor interface (HPI) commands, provide status to the Head Unit, and support FW updates. Note that per the Battery Charging Specification 1.2, other legacy charging protocols other than BC v1.2 CDP cannot be supported in conjunction with USB data communication.

EZ-PD™ CCG7D measures various temperatures using external NTC thermistors. EZ-PD™ CCG7D throttles the output power based on temperature and/or shuts off the power under critical conditions. It also monitors the battery voltage and lowers the output power if the battery voltage is lower than the user-configured threshold. When no load is connected to the USB Type-C port, EZ-PD™ CCG7D remains in standby mode without switching on the buck-boost controller.

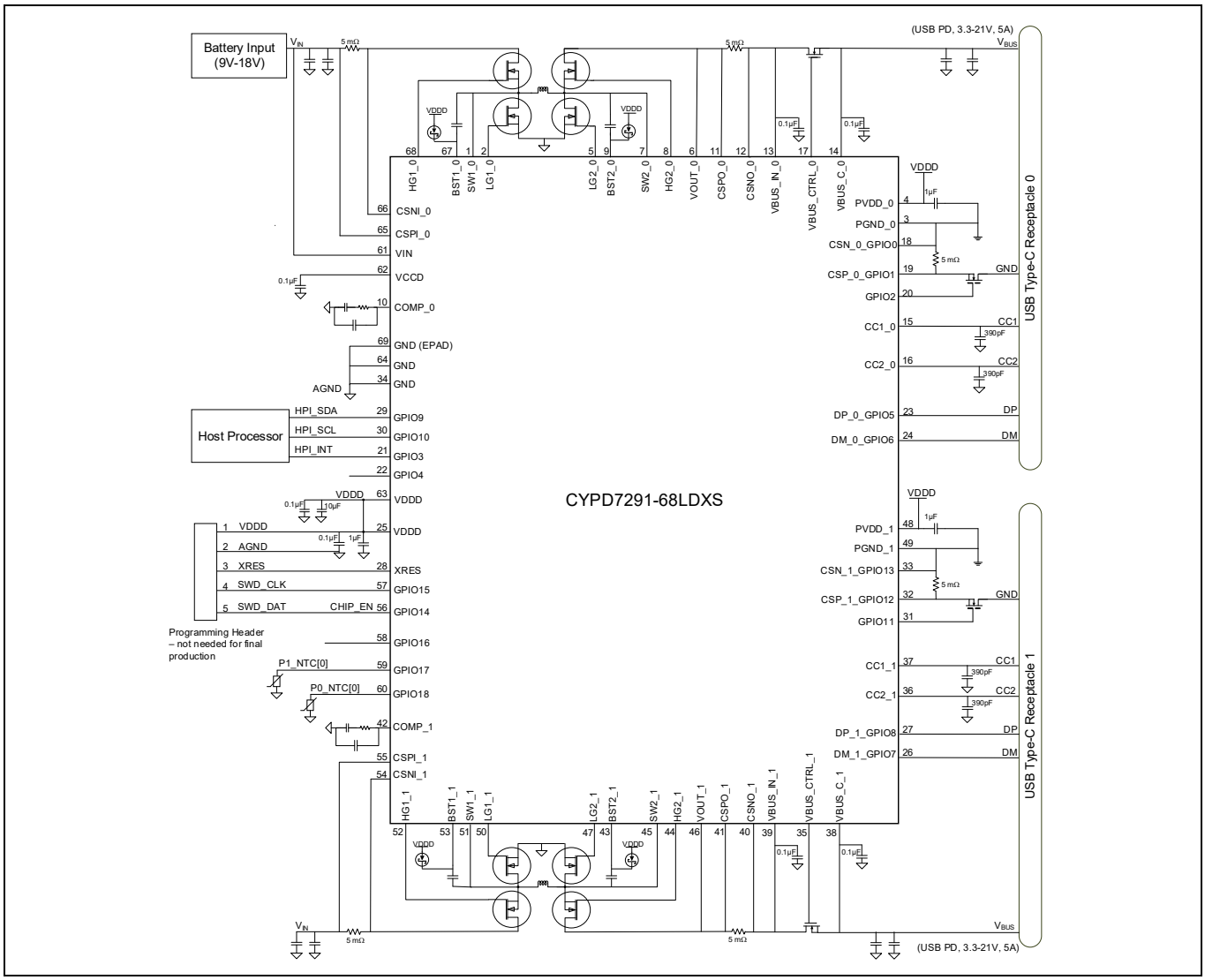


Figure 14 EZ-PD™ CCG7D head unit charger application diagram

Table 4 Head unit (HU) GPIO pin mapping for application diagram in Figure 14

Pin #	Pin name	Function	GPIO	HU
18	CSN_0_GPIO0	Port 0: CSN pin on ground side to implement VBAT to GND short circuit protection	P0.0	P0_VBAT_CSN
19	CSP_0_GPIO1	Port 0: CSP pin on ground side to implement VBAT to GND short circuit protection	P0.1	P0_VBAT_CSP
20	GPIO2	Port 0: GPIO to disable the FET for VBAT to GND short circuit protection	P0.2	P0_VBAT_FET
21	GPIO3	HPI Interrupt	P0.3	HPI_INT
22	GPIO4	GPIO, available for system level function	P0.4	GPIO
23	DP_0_GPIO5	Port 0: USB DP of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.0	P0_DP
24	DM_0_GPIO6	Port 0: USB DM of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.1	P0_DM
26	DM_1_GPIO7	Port 1: USB DM of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.2	P1_DM
27	DP_1_GPIO8	Port 1: USB DP of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.3	P1_DP
29	GPIO9	HPI data (SDA)	P2.0	HPI_SDA
30	GPIO10	HPI clock (SCL)	P2.1	HPI_SCL
31	GPIO11	Port 1: GPIO to disable the FET for VBAT to GND short circuit protection	P1.4	P1_VBAT_FET
32	CSP_1_GPIO12	Port 1: CSP pin on ground side to implement VBAT to GND short circuit protection	P1.5	P1_VBAT_CSP
33	CSN_1_GPIO13	Port 1: CSN pin on ground side to implement VBAT to GND short circuit protection	P1.6	P1_VBAT_CSN
56	GPIO14	Connect to the host programmer's SWDIO (data) for programming the EZ-PD™ CCG7D device	P3.0	GPIO
57	GPIO15	Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CCG7D Chip Enable pin	P3.1	CHIP_EN
58	GPIO16	GPIO, available for system level function	P3.2	GPIO
59	GPIO17	Port 1: Thermistor	P3.3	P1_NTC[0]
60	GPIO18	Port 0: Thermistor	P3.4	P0_NTC[0]

Figure 15 shows a typical rear seat charger application block diagram using EZ-PD™ CCG7D. This application is similar to the head unit charger application without the hub and data communications. There is no host processor/hub in this application. This application can be configured to support the legacy charging protocols – BC1.2 DCP, Qualcomm QC2.0/3.0, Apple charging, and Samsung AFC.

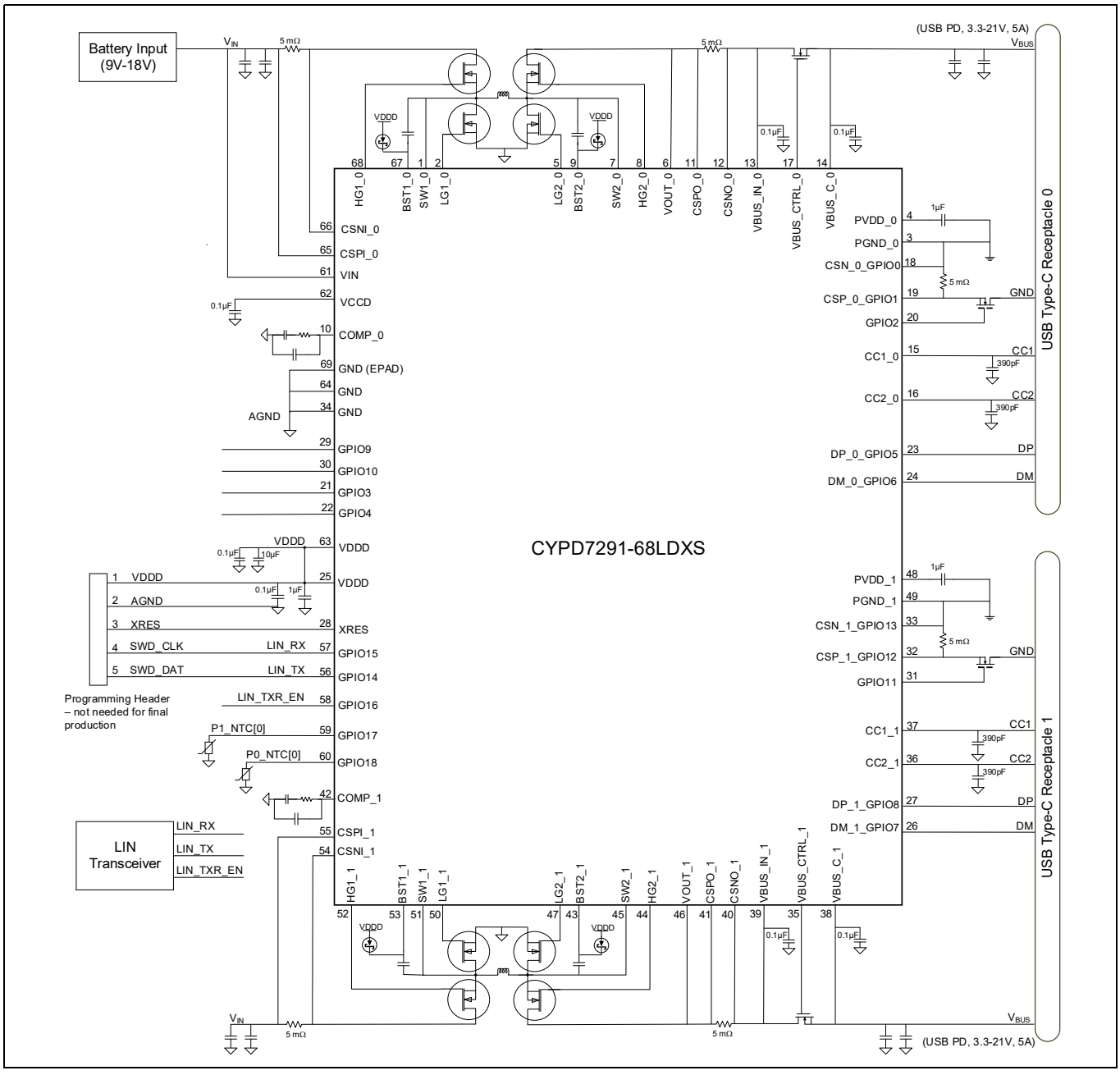


Figure 15 EZ-PD™ CCG7D RSC application diagram

Table 5 RSC GPIO pin mapping for application diagram in Figure 15

Pin #	Pin name	Function	GPIO	RSC
18	CSN_0_GPIO0	Port 0: CSN pin on ground side to implement VBAT to GND short circuit protection	P0.0	P0_VBAT_CSN
19	CSP_0_GPIO1	Port 0: CSP pin on ground side to implement VBAT to GND short circuit protection	P0.1	P0_VBAT_CSP
20	GPIO2	Port 0: GPIO to disable the FET for VBAT to GND short circuit protection	P0.2	P0_VBAT_FET
21	GPIO3	GPIO, available for system level function	P0.3	GPIO
22	GPIO4	GPIO, available for system level function	P0.4	GPIO
23	DP_0_GPIO5	Port 0: USB DP of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.0	P0_DP
24	DM_0_GPIO6	Port 0: USB DM of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.1	P0_DM
26	DM_1_GPIO7	Port 1: USB DM of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.2	P1_DM
27	DP_1_GPIO8	Port 1: USB DP of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.3	P1_DP
29	GPIO9	GPIO, available for system level function	P2.0	GPIO
30	GPIO10	GPIO, available for system level function	P2.1	GPIO
31	GPIO11	Port 1: GPIO to disable the FET for VBAT to GND short circuit protection	P1.4	P1_VBAT_FET
32	CSP_1_GPIO12	Port 1: CSP pin on ground side to implement VBAT to GND short circuit protection	P1.5	P1_VBAT_CSP
33	CSN_1_GPIO13	Port 1: CSN pin on ground side to implement VBAT to GND short circuit protection	P1.6	P1_VBAT_CSN
56	GPIO14	LIN TX pin Connect to the host programmer's SWDIO (data) for programming the EZ-PD™ CCG7D device	P3.0	LIN_TX
57	GPIO15	LIN RX pin Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CCG7D	P3.1	LIN_RX
58	GPIO16	LIN Transceiver enable	P3.2	LIN_TXR_EN
59	GPIO17	Port 1: Thermistor	P3.3	P1_NTC[0]
60	GPIO18	Port 0: Thermistor	P3.4	P0_NTC[0]

Figure 16 shows the rear seat entertainment (RSE) application block diagram using EZ-PD™ CCG7D. In the RSE application, one port is a dedicated charge-only port and the second port is used for charging and streaming video content to the rear-seat monitor, using a mobile phone, PC, or a tablet. The implementation of the charging-only port is identical to the RSC application. EZ-PD™ CCG7D supports display port alternate mode sink in the port that supports video streaming and controls the external display port multiplexer over I^2C. EZ-PD™ CCG7D also communicates with the system's SoC over I^2C.

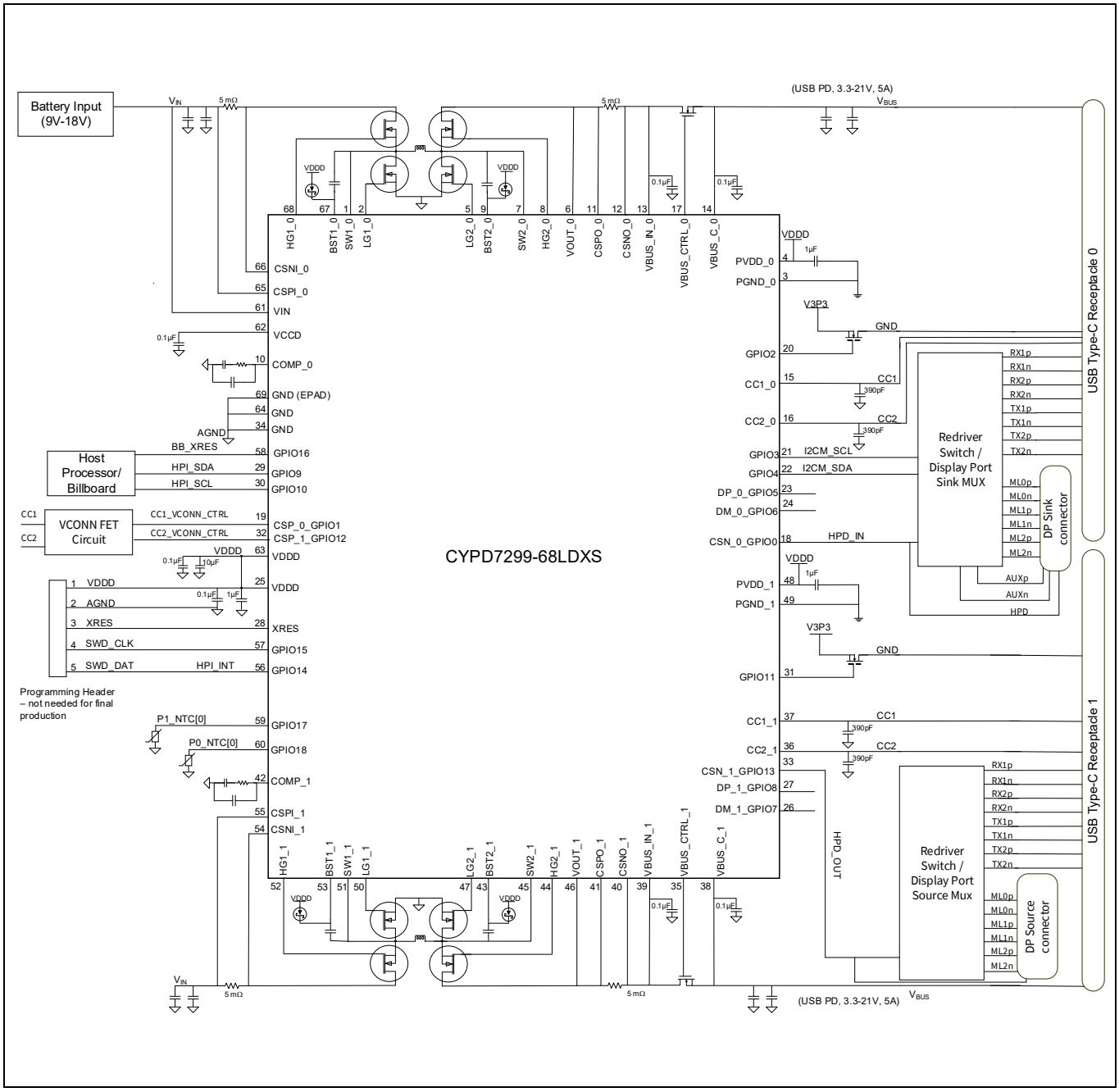


Figure 16 EZ-PD™ CCG7D RSE application diagram

Table 6 RSE GPIO pin mapping for application diagram in Figure 16

Port 0: Display and charger port

Port 1: Charge only port

Pin #	Pin name	Function	GPIO	RSE
18	CSN_0_GPIO0	Display port sink MUX Hot Plug Detect	P0.0	HPD_IN
19	CSP_0_GPIO1	CC1 Vconn control	P0.1	CC1_VCONN_CTRL
20	GPIO2	Port 0: GPIO to disable the FET for VBAT to GND short circuit protection	P0.2	P0_VBAT_FET
21	GPIO3	I^2C Master Clock (SCL) for controlling the Display port Mux	P0.3	I2CM_SCL
22	GPIO4	I^2C Master Data (SDA) for controlling the Display port Mux	P0.4	I2CM_SDA
23	DP_0_GPIO5	GPIO, available for system level function	P1.0	GPIO
24	DM_0_GPIO6	GPIO, available for system level function	P1.1	GPIO
26	DM_1_GPIO7	Port 1: USB DM of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.2	P1_DM
27	DP_1_GPIO8	Port 1: USB DP of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.3	P1_DP
29	GPIO9	HPI data (SDA)	P2.0	HPI_SDA [BILLBOARD]
30	GPIO10	HPI clock (SCL)	P2.1	HPI_SCL [BILLBOARD]
31	GPIO11	Port 1: GPIO to disable the FET for VBAT to GND short circuit protection	P1.4	P1_VBAT_FET
32	CSP_1_GPIO12	Port 1: CSP pin on ground side to implement VBAT to GND short circuit protection	P1.5	P1_VBAT_CSP
33	CSN_1_GPIO13	Display Port Source MUX HPI OUT	P1.6	HPI_OUT
56	GPIO14	HPI interrupt / SWD Data	P3.0	HPI_INT/SWD_DAT
57	GPIO15	SWD clock	P3.1	SWD_CLK
58	GPIO16	BillBoard XRES	P3.2	BB_XRES
59	GPIO17	Port 1: Thermistor	P3.3	P1_NTC[0]
60	GPIO18	Port 0: Thermistor	P3.4	P0_NTC[0]

Figure 17 shows a RSC buck application block diagram using EZ-PD™ CCG7D. This application uses the integrated buck controller to supply the required voltage and current to the connected device. This application is identical to the Rear Seat Charger application, except that this application uses only buck topology when compared to the buck-boost topology in the standard RSC application. In a buck application, the negotiated voltage should always be lower than the input voltage. If the input voltage drops lower than the output voltage, then the output voltage will not be maintained and the port will shut down. This application can also be configured to support the legacy charging protocols – BC1.2 DCP, Qualcomm QC2.0/3.0, Apple charging, and Samsung AFC.

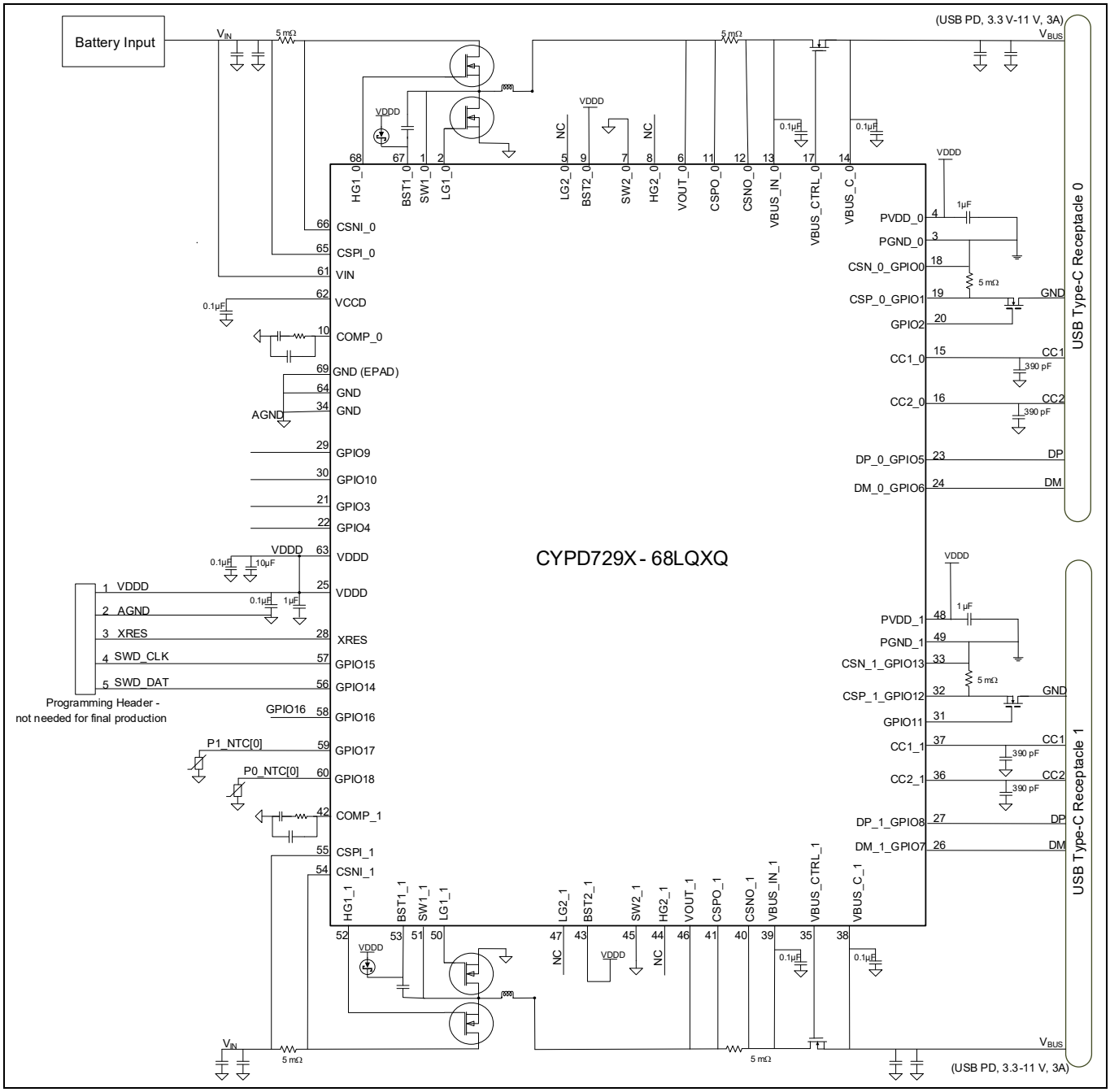


Figure 17 EZ-PD™ CCG7D RSC buck application diagram

Table 7 RSC buck GPIO pin mapping for application diagram in Figure 17

Pin #	Pin name	Function	GPIO	RSC
18	CSN_0_GPIO0	Port 0: CSN pin on ground side to implement VBAT to GND short circuit protection	P0.0	P0_VBAT_CSN
19	CSP_0_GPIO1	Port 0: CSP pin on ground side to implement VBAT to GND short circuit protection	P0.1	P0_VBAT_CSP
20	GPIO2	Port 0: GPIO to disable the FET for VBAT to GND short circuit protection	P0.2	P0_VBAT_FET
21	GPIO3	GPIO, available for system level function	P0.3	GPIO
22	GPIO4	GPIO, available for system level function	P0.4	GPIO
23	DP_0_GPIO5	Port 0: USB DP of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.0	P0_DP
24	DM_0_GPIO6	Port 0: USB DM of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.1	P0_DM
26	DM_1_GPIO7	Port 1: USB DM of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.2	P1_DM
27	DP_1_GPIO8	Port 1: USB DP of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC	P1.3	P1_DP
29	GPIO9	GPIO, available for system level function	P2.0	GPIO
30	GPIO10	GPIO, available for system level function	P2.1	GPIO
31	GPIO11	Port 1: GPIO to disable the FET for VBAT to GND short circuit protection	P1.4	P1_VBAT_FET
32	CSP_1_GPIO12	Port 1: CSP pin on ground side to implement VBAT to GND short circuit protection	P1.5	P1_VBAT_CSP
33	CSN_1_GPIO13	Port 1: CSN pin on ground side to implement VBAT to GND short circuit protection	P1.6	P1_VBAT_CSN
56	GPIO14	Connect to the host programmer's SWDIO (data) for programming the EZ-PD™ CCG7D device	P3.0	SWDIO
57	GPIO15	Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CCG7D	P3.1	SWDCLK
58	GPIO16	GPIO, available for system-level function	P3.2	GPIO
59	GPIO17	Port 1: Thermistor	P3.3	P1_NTC[0]
60	GPIO18	Port 0: Thermistor	P3.4	P0_NTC[0]

6 Electrical specifications

6.1 Absolute maximum ratings

Table 8 Absolute maximum ratings[1]

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_{IN_MAX}	Maximum input supply voltage	–	–	40	V	–
V_{DDD_MAX}	Maximum supply voltage relative to V_{SS}			6		
V_{5V_MAX}	Maximum supply voltage relative to V_{SS}					
$V_{BUS\_C\_MAX}$	Max V_{BUS_C} (P0/P1) voltage relative to Vss			24		
$V_{CC\_PIN\_ABS}$	Max voltage on CC1 and CC2 pins					
V_{GPIO_ABS}	Inputs to GPIO	–0.5		V_{DDD} + 0.5		
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage			6		
I_{GPIO_ABS}	Maximum current per GPIO	–25		25	mA	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5		0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2000		–	V	All pins.
ESD_CDM	Electrostatic discharge (ESD) charged device model	500				Charged device model ESD
LU	Pin current for latch-up	–100		100	mA	–
T_J	Junction temperature	–40		125	°C	

Note

1. Usage above the absolute maximum conditions listed in **Table 8** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 9 Pin based absolute maximum ratings

Pin #	Pin name	Absolute minimum (V)	Absolute maximum (V)
1	SW1_0	–0.7	35
2	LG1_0[2]	–0.5	PVDD + 0.5
3	PGND_0	–0.3	0.3
4	PVDD_0	–	VDDD
5	LG2_0[2]	–0.5	PVDD + 0.5
6	VOUT_0	–0.3	24
7	SW2_0		
8	HG2_0 (wrt SW2_0)[2]	–0.5	PVDD + 0.5
9	BST2_0 (wrt SW2_0)[2]	–	PVDD + 0.5
10	COMP_0[2]	–0.5	PVDD + 0.5
11	CSPO_0	–0.3	24
12	CSNO_0		
13	VBUS_IN_0		
14	VBUS_C_0		
15	CC1_0	–0.5	
16	CC2_0		
17	VBUS_CTRL_0		32
18	CSN_0_GPIO0[2]		PVDD + 0.5
19	CSP_0_GPIO1[2]		
20	GPIO2[2]		
21	GPIO3[2]		
22	GPIO4[2]		
23	DP_0_GPIO5[2]		
24	DM_0_GPIO6[2]		
25	VDDD	–	6
26	DM_1_GPIO7[2]	–0.5	PVDD + 0.5
27	DP_1_GPIO8[2]		
28	XRES[2]		
29	GPIO9[2]		
30	GPIO10[2]		
31	GPIO11[2]		
32	CSP_1_GPIO12[2]		
33	CSN_1_GPIO13[2]		
34	GND	–	–

Note
2. Max voltage cannot exceed 6 V.
3. Max absolute voltage w.r.t. GND must not exceed 40 V.

Table 9 Pin based absolute maximum ratings *(continued)*

Pin #	Pin name	Absolute minimum (V)	Absolute maximum (V)
35	VBUS_CTRL_1	–0.5	32
36	CC2_1		24
37	CC1_1		
38	VBUS_C_1	–0.3	
39	VBUS_IN_1		
40	CSNO_1		
41	CSPO_1	–0.3	24
42	COMP_1[1]	–0.5	PVDD + 0.5
43	BST2_1[1] (wrt SW2_1)	–	
44	HG2_1[1] (wrt SW2_1)	–0.5	
45	SW2_1	–0.3	24
46	VOUT_1		
47	LG2_1[1]	–0.5	PVDD + 0.5
48	PVDD_1	–	VDDD
49	PGND_1	–0.3	0.3
50	LG1_1[1]	–0.5	PVDD + 0.5
51	SW1_1	–0.7	35
52	HG1_1[1, 2](wrt SW1_1)	–0.5	PVDD + 0.5
53	BST1_1[1, 2] (wrt SW1_1)	–	
54	CSNI_1	–0.3	40
55	CSPI_1		
56	GPIO14/SWD_DAT[1]	–0.5	PVDD + 0.5
57	GPIO15/SWD_CLK[1]		
58	GPIO16[1]		
59	GPIO17[1]		
60	GPIO18[1]		
61	VIN	–0.3	40
62	VCCD	–	–
63	VDDD		6
64	GND		–
65	CSPI_0	–0.3	40
66	CSNI_0		
67	BST1_0[1, 2] (wrt SW1_0)	–	PVDD + 0.5
68	HG1_0[1, 2] (wrt SW1_0)	–0.5	
	EPAD	–	–

Note
2. Max voltage cannot exceed 6 V.
3. Max absolute voltage w.r.t. GND must not exceed 40 V.

6.2 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 125°C, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

6.2.1 DC specifications

Table 10 DC specifications (operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{IN}	Input supply voltage	4.0	–	24	V	–
SID.PWR#1A	V_{IN_BB}	Buck boost operating input supply voltage	5.5		24		
SID.PWR#2	V_{DDD_REG}	VDDD output with V_{IN} 5.5 to 24 V, Max load = 150 mA	4.6		5.5		
SID.PWR#3	V_{DDD_MIN}	VDDD output with V_{IN} 4 to 5.5 V, Max load = 20 mA	V_{IN} – 0.2		–		
SID.PWR#20	VBUS	VBUS_C_0/1 valid range	3.3		21.5		
SID.PWR#5	V_{CCD}	Regulated output voltage (for Core Logic)	–	1.8	–		
SID.PWR#16	C_{EFC_VCCD}	External regulator voltage bypass for VCCD	80	100	120	nF	X5R ceramic
SID.PWR#17	C_{EXC_VDDD}	Power supply decoupling capacitor for V_{DDD}	–	10	–	µF	
SID.PWR#18	C_{EXV}	Bootstrap supply capacitor (BST1_0, BST1_1, BST2_0, BST2_1)		0.1			
SID.PWR#24	I_{DD_ACT}	Supply current at 0.4 MHz switching frequency		85		mA	T_A = 25°C, V_{IN} = 12 V. CC IO IN Transmit or Receive, no I/O sourcing current, No VCONN load current, CPU at 24 MHz, two PD ports active. Buck-boost converter ON, 3-nF gate driver capacitance.
Deep Sleep mode							
SID_DS1	I_{DD_DS1}	V_{IN} = 12 V. CC wakeup on, Type-C not connected.	–	110	–	µA	Type-C not attached, CC enabled for wakeup. Rp connection should be enabled for both PD ports. T_A = 25°C. All faults disabled including VBAT-GND.
SID_DS2	I_{DD_DS2}	V_{IN} = 12 V	–	50	–	µA	USB PD disabled. Wake-up from GPIO. T_A = 25°C.
SID_DS3	IDD_DS3	V_{IN} = 12 V. CC wakeup on, Type-C not connected.		450			Type-C not attached, CC enabled for wakeup. Rp connection should be enabled for both PD ports. T_A = 25°C. All faults disabled except VBAT-GND.

6.2.2 CPU

Table 11 CPU specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	48	MHz	–40°C ≤ T_A ≤ +105°C, All V_{DDD}
SID.PWR#19	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode		35	–	µs	–
SYS.XRES#5	T_{XRES}	External reset pulse width	5	–			
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	

6.2.3 GPIO

Table 12 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#9	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#10	V_{IL_CMOS}	Input voltage LOW threshold	–		0.3 × V_{DDD}		
SID.GIO#7	V_{OH_3V}	Output voltage HIGH level	V_{DDD} – 0.6		–		I_{OH} = –4 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#8	V_{OL_3V}	Output voltage LOW level	–		0.6		I_{OL} = 10 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#2	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	–40°C ≤ T_A ≤ +105°C
SID.GIO#3	Rpd	Pull-down resistor when enabled					
SID.GIO#4	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GIO#5	C_{PIN_A}	Max pin capacitance			22	pF	–40°C ≤ T_A ≤ +105°C, Capacitance on DP, DM pins
SID.GIO#6	C_{PIN}	Max pin capacitance	–	3	7	pF	–40°C ≤ T_A ≤ +105°C, ALL V_{DDD}, All other I/Os
SID.GIO#11	V_{IHTTL}	LVTTL input	2	–	–	V	–40°C ≤ T_A ≤ +105°C
SID.GIO#12	V_{ILTTL}	LVTTL input	–		0.8		
SID.GIO#13	V_{HYSTTL}	Input hysteresis, LVTTL, V_{DDD} > 2.7 V	100		–	mV	V_{DDD} > 2.7 V
SID.GIO#14	$V_{HYSCMOS}$	Input hysteresis CMOS	0.1 × V_{DDD}				–

Table 13 GPIO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#16	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	C_{load} = 25 pF, –40°C ≤ T_A ≤ +105°C
SID.GIO#17	T_{FALLF}	Fall time in Fast Strong mode					
SID.GIO#18	T_{RISES}	Rise time in Slow Strong mode	10		60		
SID.GIO#19	T_{FALLS}	Fall time in Slow Strong mode					
SID.GIO#20	F_{GPIO_OUT1}	GPIO F_{OUT}; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Fast Strong mode.	–		16	MHz	
SID.GIO#21	F_{GPIO_OUT2}	GPIO F_{OUT}; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Slow Strong mode.			7		
SID.GIO#22	F_{GPIO_IN}	GPIO input operating frequency; 3.0 V ≤ V_{DDD} ≤ 5.5 V.			16		–40°C ≤ T_A ≤ +105°C

Table 14 GPIO OVT DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.GPIO_20VT_GIO #4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	–140	–	140	mA	Max / Min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT_GIO #5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	3.5		8.5	kΩ	–40°C ≤ T_A ≤ +105°C, All V_{DDD}
SID.GPIO_20VT_GIO #6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value					
SID.GPIO_20VT_GIO #16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	–		2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT_GIO #17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance			10	pF	–40°C ≤ T_A ≤ +105°C, All V_{DDD}
SID.GPIO_20VT_GIO #33	GPIO_20VT_Voh	GPIO_20VT output voltage high level.	VDDD – 0.6		–	V	I_{OH} = -4 mA
SID.GPIO_20VT_GIO #36	GPIO_20VT_Vol	GPIO_20VT output voltage low level.	–		0.6		I_{OL} = 8 mA
SID.GPIO_20VT_GIO #41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL input	2		–		–40°C ≤ T_A ≤ +105°C, All V_{DDD}
SID.GPIO_20VT_GIO #42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL input	–		0.8		
SID.GPIO_20VT_GIO #43	GPIO_20VT_Vhysttl	GPIO_20VT input hysteresis LVTTL	100	–	–	mV	–40°C ≤ T_A ≤ +105°C, All V_{DDD}
SID.GPIO_20VT_GIO #45	GPIO_20VT_ITOT_GPIO	GPIO_20VT maximum total sink pin current to ground	–	–	95	mA	V(GPIO_20VT Pin) > V_{DDD}

Table 15 GPIO OVT AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.GPIO_20VT_70	GPIO_20VT_TriseF	GPIO_20VT rise time in Fast Strong Mode	1	–	15	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT_71	GPIO_20VT_TfallF	GPIO_20VT fall time in Fast Strong Mode					
SID.GPIO_20VT_GIO#46	GPIO_20VT_TriseS	GPIO_20VT rise time in Slow Strong Mode	10		70		
SID.GPIO_20VT_GIO#47	GPIO_20VT_TfallS	GPIO_20VT fall time in Slow Strong Mode					
SID.GPIO_20VT_GIO#48	GPIO_20VT_FGPIO_OUT1	GPIO_20VT GPIO Fout; 3 V ≤ V_{DDD} ≤ 5.5 V. Fast Strong mode.	–		33	MHz	
SID.GPIO_20VT_GIO#50	GPIO_20VT_FGPIO_OUT3	GPIO_20VT GPIO Fout; 3 V≤V_{DDD}≤5.5V. Slow Strong mode.			7		
SID.GPIO_20VT_GIO#52	GPIO_20VT_FGPIO_IN	GPIO_20VT GPIO input operating frequency; 3 V ≤ V_{DDD} ≤ 5.5 V			8		All V_{DDD}

6.2.4 XRES

Table 16 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × V_{DDD}	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–		0.3 × V_{DDD}		
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin			7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin		0.05 × V_{DDD}	–	mV	

6.3 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

6.3.1 PWM for GPIO pins

Table 17 PWM AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS
SID.TCPWM.3	T_{PWMEXT}	Output trigger pulse width	2/Fc		–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs
SID.TCPWM.4	T_{CRES}	Resolution of counter	1/Fc				Minimum time between successive counts
SID.TCPWM.5	PWM_{RES}	PWM resolution					Minimum pulse width of PWM output

6.3.2 I^2C

Table 18 Fixed I^2C AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

6.3.3 UART

Table 19 Fixed UART AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

6.3.4 SPI

Table 20 Fixed SPI AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	F_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 21 Fixed SPI Master mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO valid before SClock capturing edge	20		–		Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0				Referred to slave capturing edge

Table 22 Fixed SPI Slave mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–		48 + (3 × T_{CPU})		$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext Clk mode			48		–
SID172	T_{HSO}	Previous MISO data hold time	0		–		
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK Valid edge	100				

6.3.5 Memory

Table 23 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.MEM#2	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–40°C ≤ T_A ≤ +85°C, All V_{DDD}
SID.MEM#1	FLASH_ERASE	Row erase time			15.5		
SID.MEM#5	FLASH_ROW_PGM	Row program time after erase			7		
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)			35		–
SID180	$T_{DEVPROG}$	Total device program time			7.5	s	
SID.MEM#6	FLASH_$_{ENPB}$	Flash write endurance	100k		–	cycles	25°C ≤ T_A ≤ 55°C, All V_{DDD}
SID182	F_{RET1}	Flash retention, T_A ≤ 55°C, 100K P/E cycles	20			years	–
SID182A	F_{RET2}	Flash retention, T_A ≤ 85°C, 10K P/E cycles	10				

6.4 System resources

6.4.1 Power-on-reset (POR) with brown out

Table 24 Imprecise power-on reset (IPOR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	Power-on reset (POR) rising trip voltage	0.80	–	1.50	V	–40°C ≤T_A ≤ +105°C, All V_{DDD}
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70		1.4		

Table 25 Precise POR

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in Active/Sleep modes	1.48	–	1.62	V	–40°C ≤ T_A ≤ +105°C, All V_{DDD}
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1		1.5		

6.4.2 SWD interface

Table 26 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	F_SWDCLK1	3.0 V ≤ V_{DDIO} ≤ 5.5 V	–	–	14	MHz	–
SID.SWD#2	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T		–	ns	
SID.SWD#3	T_SWDI_HOLD						
SID.SWD#4	T_SWDO_VALID		–		0.50 × T		
SID.SWD#5	T_SWDO_HOLD		1		–		

6.4.3 IMO

Table 27 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	3.0 V ≤ V_{DDD} < 5.5 V. –40°C ≤ T_A ≤ 105°C
SID226	$T_{STARTIMO}$	IMO start-up time			7	µs	–40°C ≤ T_A ≤ +105°C, All V_{DDD}
SID.CLK#1	F_{IMO}	IMO frequency	24		48	MHz	

6.4.4 Internal low-speed oscillator

Table 28 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO start-up time	–	–	2	ms	–40°C ≤ T_A ≤ +105°C, All V_{DDD}
SID238	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	
SID.CLK#5	F_{ILO}	ILO frequency	20	40	80	kHz	–

6.4.5 PD

Table 29 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.DC.cc_shvt.1	vSwing	Transmitter output High Voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter output Low Voltage	–		0.075		
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33		75	Ω	
SID.DC.cc_shvt.4	zBmcRx	Receiver input impedance	10		–	MΩ	
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64		96	µA	
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5 A at 5 V advertisement	166		194		
SID.DC.cc_shvt.7	Idac_3a	Source current for 3 A at 5 V advertisement	304		356		
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as upstream facing port (UFP)	4.59		5.61	kΩ	
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108		–		
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-standard USB	0.15		0.25	V	
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35		0.45		
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3 A	0.75		0.85		
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3 A	2.45		2.75		
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-Standard USB	0.61		0.7		
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16		1.31		
SID.DC.cc_shvt.17	Vattach_ds	Deep sleep attach threshold	0.3		0.6	%	
SID.DC.cc_shvt.18	Rattach_ds	Deep sleep pull-up resistor	10		50	kΩ	
SID.DC.cc_shvt.19	VTX_step	TX drive voltage step size	80		120	mV	

6.4.6 Analog-to-digital converter

Table 30 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	–2.5		2.5		Reference voltage generated from V_{DDD}
SID.ADC.4	Gain Error	Gain error	–1.5		1.5		Reference voltage generated from bandgap
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}		V_{DDDmax}	V	Reference voltage generated from V_{DDD}
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04		Reference voltage generated from deep sleep reference

6.4.7 High-side CSA

Table 31 High-side CSA DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.1	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active mode
SID.HSCSA.2	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10		10		
SID.HSCSA.3	Csa_Acc3	CSA accuracy 15 mV < Vsense < 25 mV	–5		5		
SID.HSCSA.4	Csa_Acc4	CSA accuracy 25 mV < Vsense	–3		3		
SID.HSCSA.7	Csa_SCP_Acc1	CSA SCP at 6 A with 5-mΩ sense resistor	–10		10		
SID.HSCSA.8	Csa_SCP_Acc2	CSA SCP at 10 A with 5-mΩ sense resistor	–10		10		
SID.HSCSA.9	Csa_OCP_1A	CSA OCP at 1 A with 5-mΩ sense resistor	104	130	156		
SID.HSCSA.10	Csa_OCP_5A	CSA OCP for 5 A with 5-mΩ sense resistor	123	130	137		

Table 32 High-side CSA AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.AC.1	T_{SCP_GATE}	Delay from SCP threshold trip to external NFET power gate turn off	–	3.5	–	µs	1 nF NFET gate
SID.HSCSA.AC.2	$T_{SCP\_GATE\_1}$	Delay from SCP threshold trip to external NFET power gate turn off		8			3 nF NFET gate

6.4.8 UV/OV

Table 33 UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.UVOV.1	VTHOV1	Overvoltage threshold Accuracy, 4 V to 11 V	–3	–	3	%	Active mode
SID.UVOV.2	VTHOV2	Overvoltage threshold Accuracy, 11 V to 21.5 V	–3.2		3.2		
SID.UVOV.3	VTHUV1	Undervoltage threshold Accuracy, 3 V to 3.3 V	–4		4		
SID.UVOV.4	VTHUV2	Undervoltage threshold Accuracy, 3.3 V to 4.0 V	–3.5		3.5		
SID.UVOV.5	VTHUV3	Undervoltage threshold Accuracy, 4.0 V to 21.5 V	–3		3		

6.4.9 VCONN switch

Table 34 VCONN switch DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.VCONN.1	VCONN_OUT	VCONN output voltage with 20 mA load current	4.5	–	5.5	V	–
DC.VCONN.2	I_{LEAK}	Connector side pin leakage current	–		10	µA	
DC.VCONN.3	I_{OCP}	VCONN Over-Current Protection Threshold	22.5	30	42.5	mA	

Table 35 VCONN switch AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
AC.VCONN.1	T_{ON}	VCONN switch turn-on time	–	–	600	µs	–
AC.VCONN.2	T_{OFF}	VCONN switch turn-off time			10		

6.4.10 V_{BUS}

Table 36 V_{BUS} discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.VBUS.DISC.1	R1	20-V NMOS ON resistance for DS = 1	500	–	2000	Ω	Measured at 0.5 V
SID.VBUS.DISC.2	R2	20-V NMOS ON resistance for DS = 2	250		1000		
SID.VBUS.DISC.3	R4	20-V NMOS ON resistance for DS = 4	125		500		
SID.VBUS.DISC.4	R8	20-V NMOS ON resistance for DS = 8	62.5		250		
SID.VBUS.DISC.5	R16	20-V NMOS ON resistance for DS = 16	31.25		125		
SID.VBUS.DISC.6	Vbus_stop_error	Error percentage of final VBUS value from setting	–		10	%	When VBUS is discharged to 5 V

6.4.11 Voltage regulation

Table 37 Voltage regulation DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.VR.1	VOUT	VBUS_IN output voltage range	3.3	–	21.5	V	–
SID.DC.VR.2	VR	VBUS_IN voltage regulation accuracy	–	±3	±5	%	
SID.DC.VR.3	VIN_UVLO	VIN Supply below which chip will get reset	1.7	–	3.0	V	

Table 38 Voltage regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VREG.1	T_{START}	Total startup time for the regulator supply outputs	–	–	200	µs	–

6.4.12 VBUS gate driver

Table 39 VBUS gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.1	GD_VGS	Gate to source overdrive during ON condition	4.5	5	10	V	NFET driver is ON.
SID.GD.2	GD_RPD	Resistance when pull-down enabled	–	–	2	kΩ	Applicable on VBUS_CTRL to turn off external NFET
SID.GD.5	GD_drv	Programmable typical gate current	0.3		9.75	µA	–

Table 40 VBUS gate driver AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.3	T_{ON}	VBUS_CTRL Low to High (1 V to VBUS + 1 V) with 3 nF external capacitance	2	5	10	ms	V_{BUS_IN} = 5 V
SID.GD.4	T_{OFF}	VBUS_CTRL High to Low (90% to 10%) with 3 nF external capacitance	–	7	–	µs	V_{BUS_IN} = 21.5 V

6.4.13 PWM controller

Table 41 Buck-boost PWM controller specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
PWM.1	F_{SW}	Switching frequency	150	–	600	kHz	–
PWM.2	FSS	Spread spectrum frequency dithering span	–	10	–	%	
PWM.3	Ratio_Buck_BB	Buck to buck boost ratio		1.16		–	
PWM.4	Ratio_Boost_BB	Boost to buck boost ratio		0.84			

6.4.14 NFET gate driver

Table 42 Buck-boost NFET gate driver specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DR.1	R_HS_PU	Top-side gate driver on-resistance - gate pull-up	–	2	–	Ω	–
DR.2	R_HS_PD	Top-side gate driver on-resistance - gate pull-down		1.5			
DR.3	R_LS_PU	Bottom-side gate driver on-resistance - gate pull-up		2			
DR.4	R_LS_PD	Bottom-side gate driver on-resistance - gate pull-down		1.5			
DR.5	Dead_HS	Dead time before high-side rising edge		30		ns	
DR.6	Dead_LS	Dead time before low-side rising edge		30			
DR.7	Tr_HS	Top-side gate driver rise time		25			
DR.8	Tf_HS	Top-side gate driver fall time		20			
DR.9	Tr_LS	Bottom-side gate driver rise time		25			
DR.10	Tf_LS	Bottom-side gate driver fall time		20			

6.4.15 LS-SCP

Table 43 LS-SCP DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.LSSCP.DC.1	SCP_6A	Short circuit current detect at 6A	5.4	6	6.6	A	Using differential inputs (CSN_1_GPIO12, CSP_1_GPIO13 or CSP_0_GPIO0, CSN_0_GPIO1)
SID.LSSCP.DC.1A	SCP_6A_SE	Short circuit current detect at 6A	4.5	6	7.5		Using single ended inputs (CSP_1_GPIO13 or CSP_0_GPIO0) and internal ground
SID.LSSCP.DC.2	SCP_10A	Short circuit current detect at 10A	9	10	11		Using differential inputs (CSN_1_GPIO12, CSP_1_GPIO13 or CSP_0_GPIO0, CSN_0_GPIO1)
SID.LSSCP.DC.2A	SCP_10A_SE	Short circuit current detect at 10A	7.5	10	12.5		Using single ended inputs (CSP_1_GPIO13 or CSP_0_GPIO0) and internal ground

6.4.16 Thermal

Table 44 Thermal specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.OTP.1	OTP	Thermal shutdown	120	125	130	°C	–

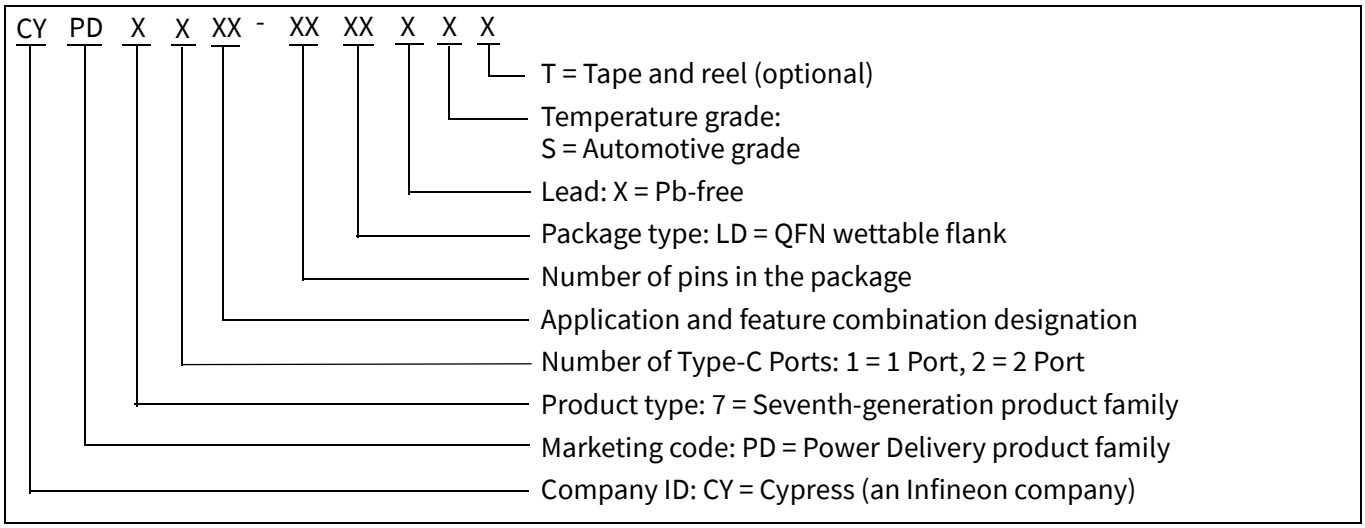
7 Ordering information

Table 45 lists the EZ-PD™ CCG7D part numbers and features.

Table 45 EZ-PD™ CCG7D ordering Information

Product	Application	Termination resistor	Role	Switching frequency	Package type
CYPD7291-68LDXS	Rear seat and head unit charger	R_P	DFP (power source only)	150 to 600 kHz	68-pin QFN
CYPD7291-68LDXST					
CYPD7299-68LDXS	Rear seat entertainment		DFP power, UFP data		
CYPD7299-68LDXST					

7.1 Ordering code definitions



8 Packaging

Table 46 Package characteristics

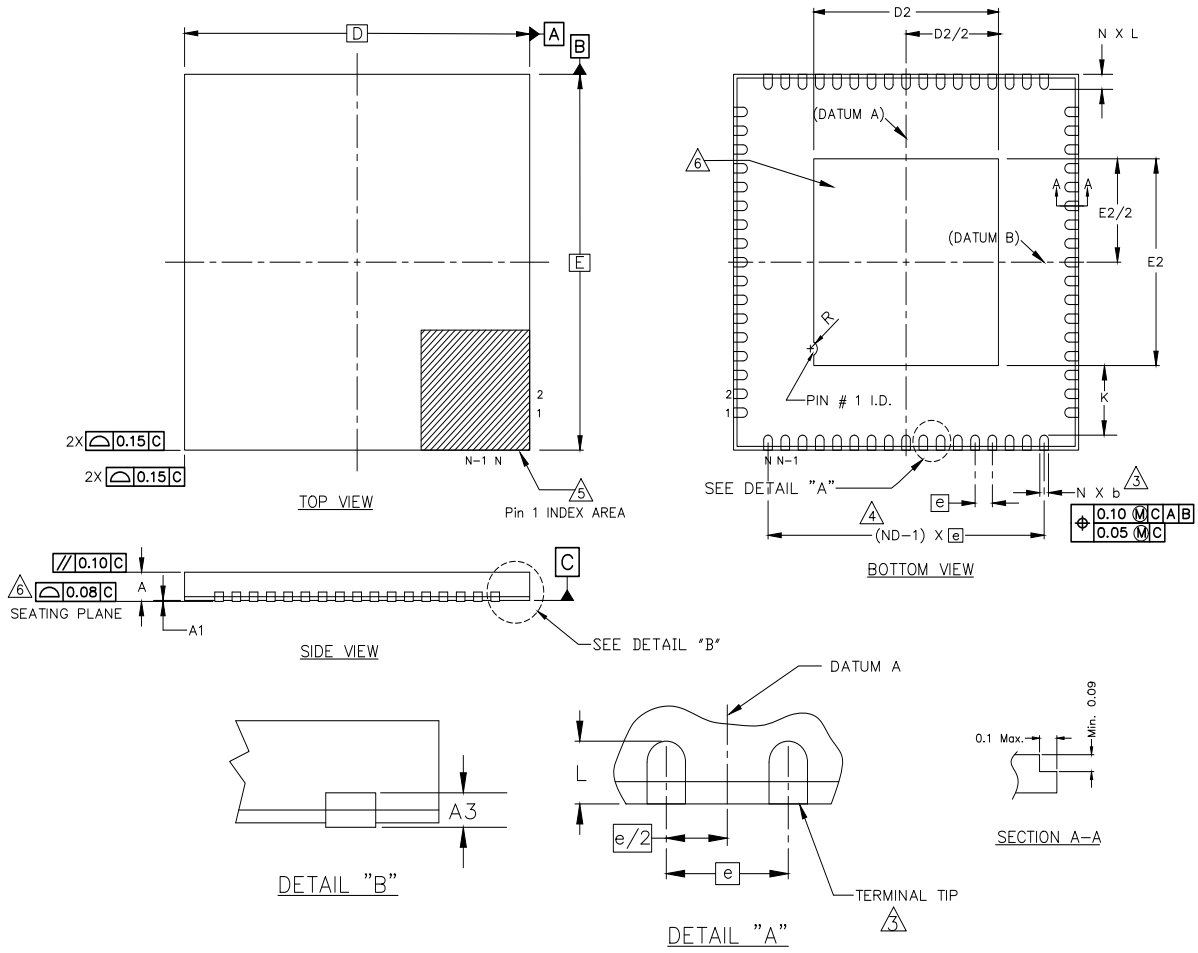
Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	–40	25	125	°C
T_{JA}	Package θ_{JA}		–	–	12.1	°C/W
T_{JC}	Package θ_{JC}				3.1	

Table 47 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
68-QFN	260°C	30 seconds

Table 48 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-QFN	MSL 3



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.50 BSC	
N		68	
ND		17	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
D2	5.25	5.35	5.45
E2	5.40	5.50	5.60
D		10.00 BSC	
E		10.00 BSC	
A	-	-	1.00
A1	0.00	-	0.05
A3		0.203 REF	
R		0.20 TYP	
K		0.35 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-29306 *A

Figure 18 68-lead QFN (10.0 10.0 1.0 mm), LV68A (5.35 5.50 mm) EPAD (SAWN) (wettable flank), (PG-VQFN-68)

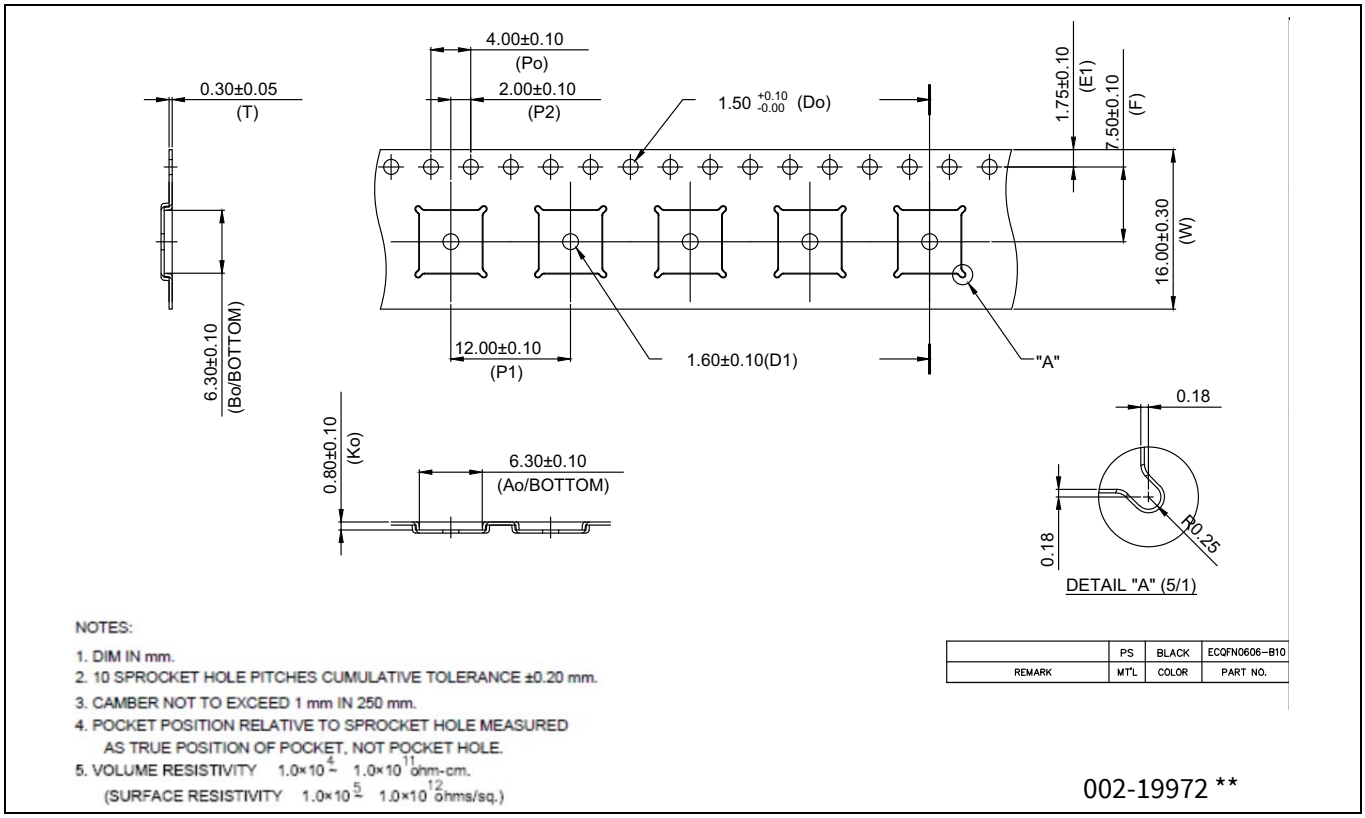


Figure 19 Carrier tape dimensions

9 Acronyms

Table 49 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AFC	Samsung Adaptive Fast Charging
Arm®	advanced RISC machine, a CPU architecture
BOD	brownout detect
BMC	biphase mark coding
CC	configuration channel
CDP	charging downstream port
CMOS	Complementary Metal Oxide Semiconductor
CPU	central processing unit
CSA	current sense amplifier
DAC	digital-to-analog converter
DCM	discontinuous-conduction mode
DFP	downstream facing port
EA	error amplifier
EMC	electromagnetic compatibility
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C
EMI	electromagnetic interference
EPAD	exposed pad
ESD	electrostatic discharge
FCCM	forced continuous current/conduction mode
GPIO	general-purpose input/output
HPI	host processor interface
HSDR	high-side driver
HSIOM	high-speed I/O matrix
HU	head unit
HUC	head unit charger
I^2C, or IIC	inter-integrated circuit, a communications protocol
IDAC	current DAC
I/O	input/output, see also GPIO
ILO	internal low-speed oscillator
IMO	internal main oscillator
IRQ	interrupt request
ISR	interrupt service routine
LSDR	low-side driver
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NTC	negative temperature coefficient (refers to a thermistor)

Table 49 Acronyms used in this document *(continued)*

Acronym	Description
OCP	overcurrent protection
OTP	overtemperature protection
OVP	overvoltage protection
PD	power delivery
POR	power-on reset
PPS	programmable power supply
PSOC™	Programmable System-on-Chip™
PSM	pulse-skipping mode
PWM	pulse-width modulator
RCP	reverse current protection
RAM	random-access memory
ROM	read-only memory
RSC	rear-seat charger
RSE	rear-seat entertainment
SCB	serial communications block
SPI	serial peripheral interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter/PWM
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UFP	upstream facing port
UVP	undervoltage protection
USB	Universal Serial Bus
UVLO	undervoltage lockout
VPA	VCONN-powered accessories
VPD	VCONN-powered devices
WDT	watchdog timer
WIC	wakeup interrupt controller
ZCD	zero-crossing detector

10 Document conventions

10.1 Units of measure

Table 50 Units of measure

Symbol	Unit of measure
°C	degree celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kiloohm
Mbps	megabits per second
MHz	megahertz
MΩ	megaohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second

Revision history

Document revision	Date	Description of changes
*N	2023-01-31	Removed “restricted” status from the datasheet. Post to external web.
*O	2025-01-31	Updated USB PD revision number to ‘3.2’ across the document. Added **Table 3**. Added **Application firmware update using bootloader** section. Updated **Figure 16** and its associated **Table 6**. Updated the maximum value of “DC.VCONN.3’ to ‘42.5 mA’ in **Table 34**. Added ordering part numbers “CYPD7291-68LDXST” and “CYPD7299-68LDXST” in **Table 45**. Updated document title.

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Email:
erratum@infineon.com

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