ATA5835

UHF ASK/FSK Transceiver Summary Data Sheet

Introduction

The ATA5835 is an ultra-low power, Ultra High Frequency (UHF) smart transceiver, based on an 8-bit AVR® microcontroller with System on Chip (SoC). It consists of an RF front end, a complex digital baseband, and a low-power 8-bit AVR microcontroller. This leads to a minimal Bill of Material (BOM) in customer applications and offers low power consumption, high sensitivity, blocking and image rejection.

The device integrates two receive paths that enable a simultaneous search for two telegrams with different modulations, data rates, wake-up conditions and so on. The ATA5835 offers additional flexibility as it enables up to eight different services with three channels each, which the user can configure independently and with up to 16 channel polling schemes.

The ATA5787 is a pure receiver with features identical to the ATA5835, but without the transmit function.

Features

- **Internal Microcontroller System**
  - 8-Bit AVR Microcontroller Core and Firmware Library in ROM
  - 20-Kbyte Flash Program Memory for Customer Applications and 2-Kbyte SRAM (1 Kbyte for Customer Applications)
  - 1-Kbyte EEPROM for Up to Four Service Configurations
- **Supported RF Ranges**
  - Low Band 310 MHz to 318 MHz, Low Band 418 MHz to 477 MHz, and High Band 836 MHz to 928 MHz
  - 315.00 MHz/433.92 MHz/868.30 MHz and 915 MHz with one 24.305 MHz Crystal
- **Current Consumption**
  - 5 nA in OFFMode
  - 40 µA in SleepMode
  - 6.5 mA in RXMode (434 MHz, VS = 5V, Internal DC-DC Converter Active)
  - 7.8 mA/10.8 mA in TXMode (434 MHz, P_{OUT} = 6 dBm/10 dBm, VS = 5V, Internal DC-DC Converter Active)
  - Three-Channel PollingMode
    - 450 µA with 50 ms Polling Cycle
    - 900 µA with 21 ms Polling Cycle
- **Receiver**
  - Demodulation
    - Amplitude Shift Keying (ASK) / On Off Keying (OOK)
    - Frequency Shift Keying (FSK) (Deviation ±0.375 kHz to ±93 kHz)
  - Decoding
    - Non-Return-to-Zero (NRZ) at 1 Kbit/s to 160 Kbits/s
    - Manchester at 500 bits/s to 80 Kbits/s
  - Sensitivity (Manchester Coded) at 433.92 MHz
    - ASK: -127 dBm at 0.5 Kbits/s, BWIF = 25 kHz
    - ASK: -112 dBm at 20 Kbits/s, BWIF = 80 kHz
    - FSK: -124 dBm at 0.75 Kbits/s, Δf = ±0.75 kHz, BWIF = 25 kHz

    - FSK: -113 dBm at 10 Kbits/s, Δf = ±10 kHz, BWIF = 165 kHz
    - FSK: -110 dBm at 20 Kbits/s, Δf = ±20 kHz, BWIF = 165 kHz
  - Image Rejection
    - 55 dB in 315 MHz/433 MHz Band and 25 dB in 868 MHz/915 MHz Band
  - Blocking
    - >64 dBc at 1 MHz Offset from Carrier
    - >48 dBc at 225 kHz Offset from Carrier in Low-Band
  - Channel Filter 25 kHz to 365 kHz (Approx. 10% Steps) and Digital RSSI with Relative Accuracy of ±1 dB
  - Fast Receiver Synchronization ≦ 8 Symbols and Autonomous Polling, Message and ID Validation
  - Pattern-Based Wake-up and Start-of-Frame Identification (SFID)
  - Flexible EEPROM and SRAM-Based Service Configuration Concept
  - Double Receive Path for Parallel Telegram Search on the Same Channel (For Example, ASK/FSK)
  - Buffered and Transparent Reception
  - Flexible Polling Configuration Concerning Timing, Order and Participating Channels
  - Configurable 4, 8, 16-Bit CRC Check
- **Transmitter**
  - Modulation
    - ASK (OOK)
    - FSK (Deviation ±0.375 kHz to ±93 kHz)
  - Coding
    - NRZ at 1 Kbit/s to 160 Kbits/s
    - Manchester at 500 bits/s to 80 Kbits/s
  - Programmable Output Power -12 dBm to +14.5 dBm in 0.4 dB Steps
  - Buffered and Transparent Transmission
  - Automatic Telegram Composition in Buffered mode
  - Configurable 4, 8, 16-Bit CRC Calculation
  - ASK and Gauss Shaping to Reduce Spectral Bandwidth of Modulated PA Output Signal
- **Interfaces**
  - SPI Interface with Up to 1 Mbit/s
  - LIN/UART Interface to Support LIN 2.2 Compliant Communication
  - Configurable Event Signal Towards Host Microcontroller and Programmable Clock Output Derived from Crystal Frequency
- **System Timings**
  - OFFMode to IDLEMode: 0.5 ms
  - OFFMode to RXMode: 1.5 ms
  - OFFMode to TXMode: 1.5 ms
  - RXMode to TXMode: 0.5 ms
  - TXMode to RXMode: 0.7 ms
- **Extended Features**
  - Integrated Temperature Sensor with ±1K Relative Accuracy (±3K Absolute)
  - Three Switchable Antenna Ports (Triplexer) and Antenna Diversity
  - RF Approach Wake-up with External Sleep Timer
- **Boundary Conditions**
  - Supply Voltage 2.0V to 5.5V and Temperature Range -40°C to +105°C
  - ESD Protection
    - ±4 kV HBM
    - ±750V FCDM
  - Package 5x5 mm 32-Lead QFN Wettable Flanks, 0.5 mm Pitch
  - Suitable for Applications Governed by EN 300 220 and FCC Part 15, Title 47

Table of Contents

1. Quick References

1.1 Reference Documentation

For further details, refer to the following:

- *ATA5835 UHF ASK/FSK Transceiver Data Sheet* (DS20005731)
- *ATA5835 UHF ASK/FSK Transceiver User's Guide* (DS50003152)

1.2 Acronym and Abbreviations

Table 1-1. Acronyms and Abbreviations

Acronyms and Abbreviations	Description
ADC	Analog-to-Digital Converter
BOM	Bill of Material
BWIF	Intermediate Frequency Bandwidth
CLK_OUT	Clock Output
CPU	Central Processing Unit
DC	Direct Current
DFIFO	Data FIFO
ESD	Electrostatic Discharge
FCDM	Field Induce Charge Device Model (ESD)
FRC	Fast Resistor Capacitor (Oscillator)
FSK	Frequency Shift Keying
GND	Ground
HBM	Human Body Model (ESD)
LDO	Low Dropout Voltage Regulator
LED	Light Emitting Diode
LIN	Local Interconnect Network
LNA	Low Noise Amplifier
MISO	Host In/Client Out (SPI)
MOSI	Host Out/Client In (SPI)
NRZ	Non-Return-to-Zero
NSS	Not Client Select (SPI)
OOK	On Off Keying
PEG	Passive Entry Go
PLL	Phase Locked Loop
ROM	Read Only Memory

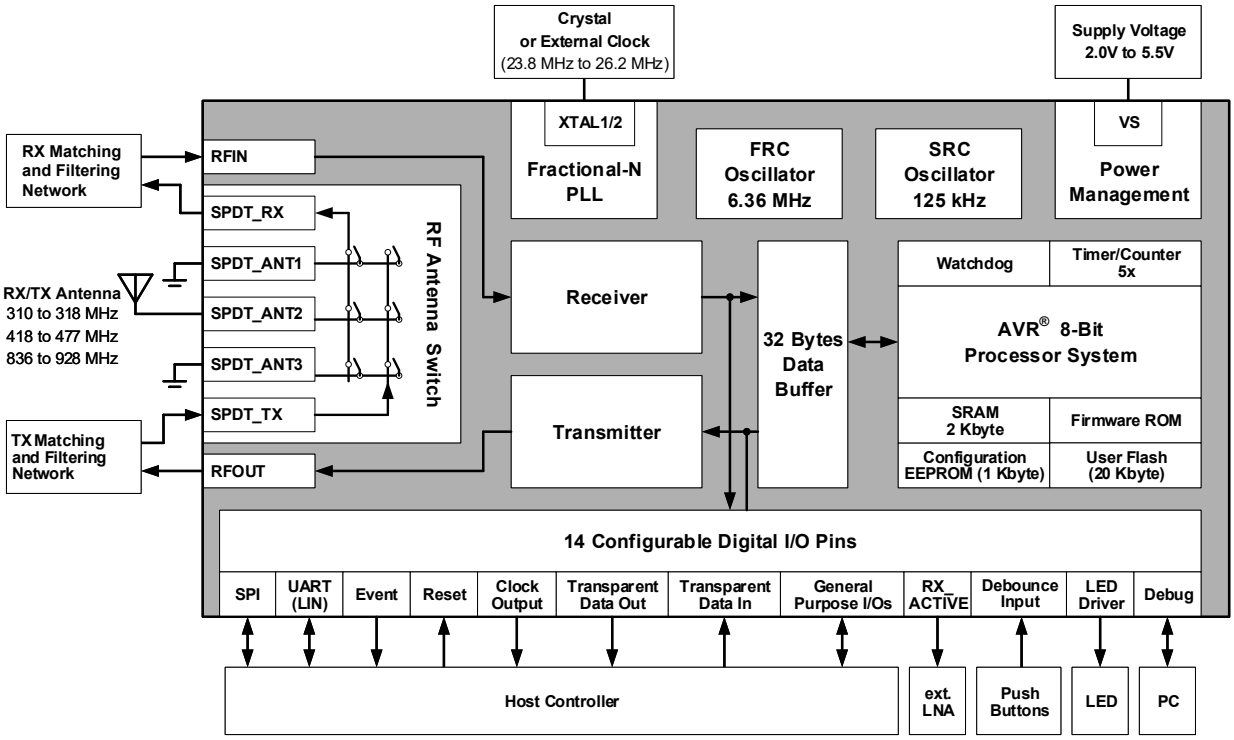
.....continued

Acronyms and Abbreviations	Description
RSSI	Received Signal Strength Indicator
RX	Receive
SCK	SPI Clock
SFIFO	Support FIFO
SPDT	Single Pole Double Throw
SPI	Serial Programming Interface
SRAM	Static Random Access Memory
SRC	Slow Resistor Capacitor (oscillator)
TMDO	Transparent Mode Data Output
TPM, TPMS	Tire Pressure Monitoring System
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
UHF	Ultra-High Frequency
VCO	Voltage Controlled Oscillator
VS	Voltage Supply
WDT	Watchdog Timer
WUP	Wake-Up Pattern
XTO	Crystal Oscillator

2. System Overview

The following block diagram illustrates an overview of the main functional blocks of the ATA5835.

Figure 2-1. System Functional Block Diagram



The ATA5835 consists of the following components:

- RF switch with three antenna ports
- Receiver unit
- Transmitter unit
- 32-byte data buffer
- 8-bit AVR microprocessor system

The internal RF switch enables various functions, such as RX/TX switching, antenna diversity or channel prefiltering with a minimized external component count.

The receiver is based on a low-IF architecture with FSK or ASK (OOK) demodulation and NRZ or Manchester decoding. Two digital receive paths, pattern-based wake-up detection and flexible telegram handling settings allow an application-specific adaptation of the receiver behavior. The user can either store the received telegram payload in the internal buffer or directly stream out on a transparent interface to a host microcontroller. In the RXMode (Buffered), the system provides automatic CRC-based verification of the received telegram.

The transmitter is compatible with the receiver concerning RF range, modulation and data coding to allow a transceiver link using two ATA5835 devices.

The transmitter has two modes: the Transparent and the Buffered mode.

- In the Transparent mode, the data are sent out as provided on the input pin.
- In the Buffered mode, the system provides an automatic telegram composition with cyclic preamble extension, stop sequence creation and CRC calculation.

The system contains various clock sources:

- A fractional-N PLL, which is based on a 23.8-MHz to 26.2-MHz crystal oscillator (XTO, default 24.305 MHz), clocks all RF activity.

- The AVR system runs on XTO/4 when the RF part is active or on a 6.36-MHz FRC oscillator when the front end is shut down for reduced power consumption.
- In deep Sleep modes, for example, Polling sleep phases, a low-power 125-kHz oscillator clocks the system.

The user can power-on the system using a single supply voltage (VS) between 2.0V and 5.5V, which leads to two different application scenarios:

- A 5V application – For this application, an embedded power management module generates all internal voltages. An integrated DC-DC converter allows additional significant reduction of current consumption on VS in the Receive and the Transmit modes.
- A 3V application – This application targets battery-powered applications with decreasing VS over its lifetime. In this mode, VS can directly power the power amplifier to avoid the voltage drop of the internal regulator and optimize the transmit output power.

All PWRON and NPWRON pins (PC1 to PC5, PB4, PB7) are active in the OFFMode. This means that even if the ATA5835 is in the OFFMode and the DVCC voltage is switched off, the internal power management circuitry biases these pins with VS to allow a wake-up of the system.

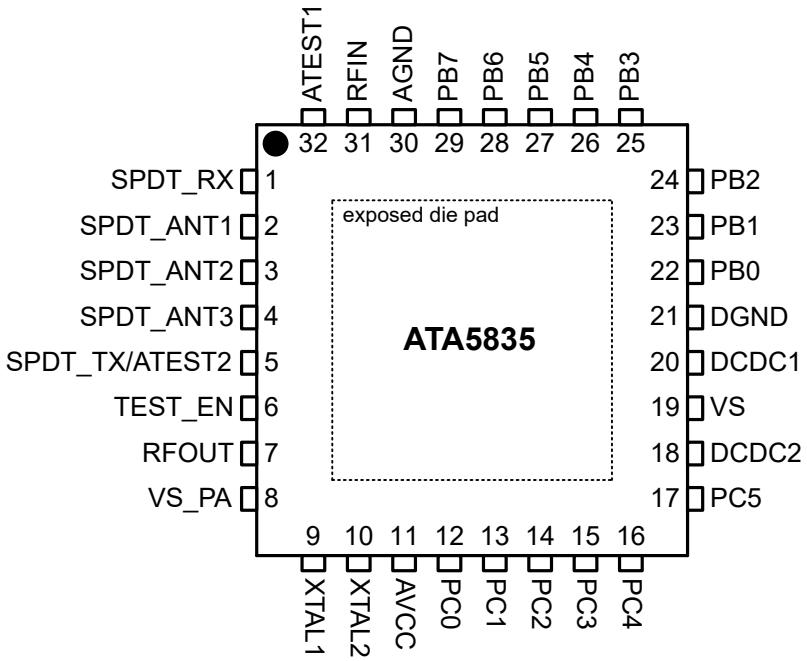
The EEPROM stores the configuration of the ATA5835 while the firmware located in the ROM defines the functionality and the AVR processes the firmware. The internal storage of configuration data has an advantage as it minimizes the external controller initialization tasks for decreased start-up time, response time and host controller burden. The SPI interface performs the external control of the system. An SPI command can trigger the AVR to configure the hardware according to settings that are stored in the EEPROM and start up a given system mode (example: RXMode, TXMode or PollingMode). Internal events such as “Start of Telegram” or “FIFO empty” are signaled to the external microcontroller on pin 28 (PB6/EVENT). Generally, the implemented firmware functions with the configuration range in the EEPROM are sufficient to design an advanced host-controlled radio link. However, the ATA5835 also provides 20-KByte of user Flash memory and an API to add highly-customized functions or run the system without a host controller.

The user can use the configurable digital I/O pins as button inputs, external LNA switch (RX_ACTIVE), LED drivers, EVENT pin, switching control for additional RF switches, general purpose digital inputs or wake-up inputs, clock output for an external host and so on.

Note: Some functionality of these ports is already implemented in the firmware and can be activated by adequate EEPROM configurations. Other functionality, such as a LIN/UART interface, is available only through custom software residing in the Flash program memory.

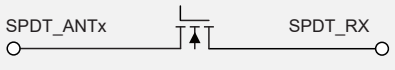
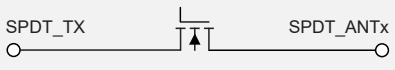
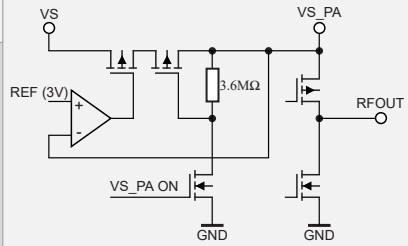
2.1 Pin Descriptions

Figure 2-2. Pin Diagram

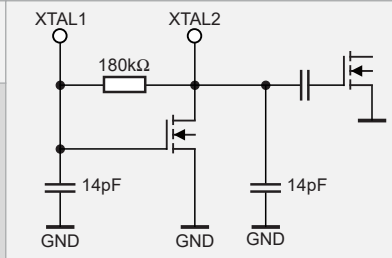
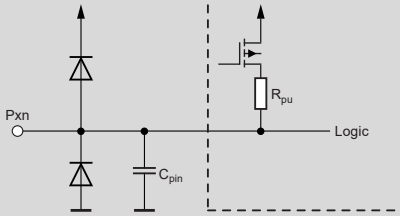
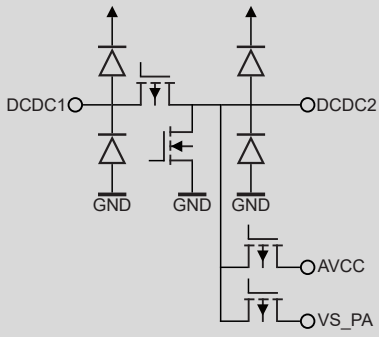


Note: The exposed die pad is connected to the internal die.

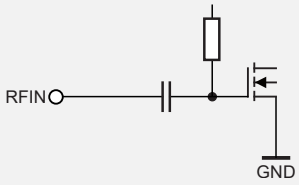
Table 2-1. Pin Description

Pin No.	Pin Name	Type	Equivalent Circuit	Description
1	SPDT_RX	Analog		RF switch RX output
2	SPDT_ANT1	Analog		RF switch antenna port 1
3	SPDT_ANT2	Analog		RF switch antenna port 2
4	SPDT_ANT3	Analog		RF switch antenna port 3
5	SPDT_TX/ ATEST2	Analog		RF switch TX input RF front-end test I/O2 (only in Test mode)
6	TEST_EN	Analog	—	Connect Test enable to GND within the application.
7	RFOUT	Analog		Power amplifier output
8	VS_PA	—		Power amplifier supply input (3V application) Power amplifier supply output (5V application)

.....continued

Pin No.	Pin Name	Type	Equivalent Circuit	Description
9	XTAL1	Analog		Crystal oscillator input External clock input
10	XTAL2	Analog		Crystal oscillator output
11	AVCC	—	ESD protection circuit	RF front-end supply regulator output
12	PC0	Digital		**Main:** AVR® Digital I/O Port C0 **Alternate:** PCINT8/NRESET/DebugWIRE
13	PC1	Digital	See pin PC0	**Main:** AVR® Digital I/O Port C1 **Alternate:** NPWRON1/PCINT9/EXT_CLK
14	PC2	Digital	See pin PC0	**Main:** AVR® Digital I/O Port C2 **Alternate:** NPWRON2/PCINT10/TRPA
15	PC3	Digital	See pin PC0	**Main:** AVR® Digital I/O Port C3 **Alternate:** NPWRON3/PCINT11/TxD/TMDO
16	PC4	Digital	See pin PC0	**Main:** AVR® Digital I/O Port C4 **Alternate:** NPWRON4/PCINT12/RxD/INT0/TMDI
17	PC5	Digital	See pin PC0	**Main:** AVR® Digital I/O Port C5 **Alternate:** NPWRON5/PCINT13/TRPB/ TMDO_CLK
18	DCDC2	Analog		DC-DC Converter pin 2
19	VS	Analog	ESD protection circuit	Main supply voltage input
20	DCDC1	Analog	See pin 18 (DCDC2)	DC-DC Converter pin 1
21	DGND	—	ESD protection circuit	Digital ground
22	PB0	Digital	See pin PC0	**Main:** AVR® Digital I/O Port B0 **Alternate:** PCINT0/CLK_OUT
23	PB1	Digital	See pin PC0	**Main:** AVR® Digital I/O Port B1 **Alternate:** PCINT1/SCK

.....continued

Pin No.	Pin Name	Type	Equivalent Circuit	Description
24	PB2	Digital	See pin PC0	**Main:** AVR® Digital I/O Port B2 **Alternate:** PCINT2/MOSI
25	PB3	Digital	See pin PC0	**Main:** AVR® Digital I/O Port B3 **Alternate:** PCINT3/MISO
26	PB4	Digital	See pin PC0	**Main**: AVR® Digital I/O Port B4 Alternate: PWRON/PCINT4/LED1
27	PB5	Digital	See pin PC0	**Main:** AVR® Digital I/O Port B5 **Alternate:** PCINT5/INT1/NSS
28	PB6	Digital	See pin PC0	**Main:** AVR® Digital I/O Port B6 **Alternate:** PCINT6/EVENT
29	PB7	Digital	See pin PC0	**Main:** AVR® Digital I/O Port B7 **Alternate:** NPWRON6/PCINT7/RX_ACTIVE/ LED0
30	AGND	—	ESD protection circuit	Analog ground
31	RFIN	Analog		LNA input
32	ATEST1	Analog	—	RF front-end test I/O1, connected to GND in application
	GND	—	—	Ground/backplane on exposed die pad

2.2 Typical Applications

The transceiver is designed to be used in the following application areas:

- Remote Keyless Entry (RKE) system
- Passive Entry Go (PEG) system
- Tire Pressure Monitoring (TPM, TPMS) system
- Remote Start (RS) system
- Remote control systems (example: garage door openers)
- Smart RF applications
- Telemetering systems

The subsequent sections give application examples to provide an impression of the application range and the Bill of Material using the ATA5835. The specific customer designs might vary concerning used features, components and wiring.

2.2.1 Typical 5V Antenna Diversity Application with External Microcontroller

Figure 2-3. Typical 5V Antenna Diversity Application

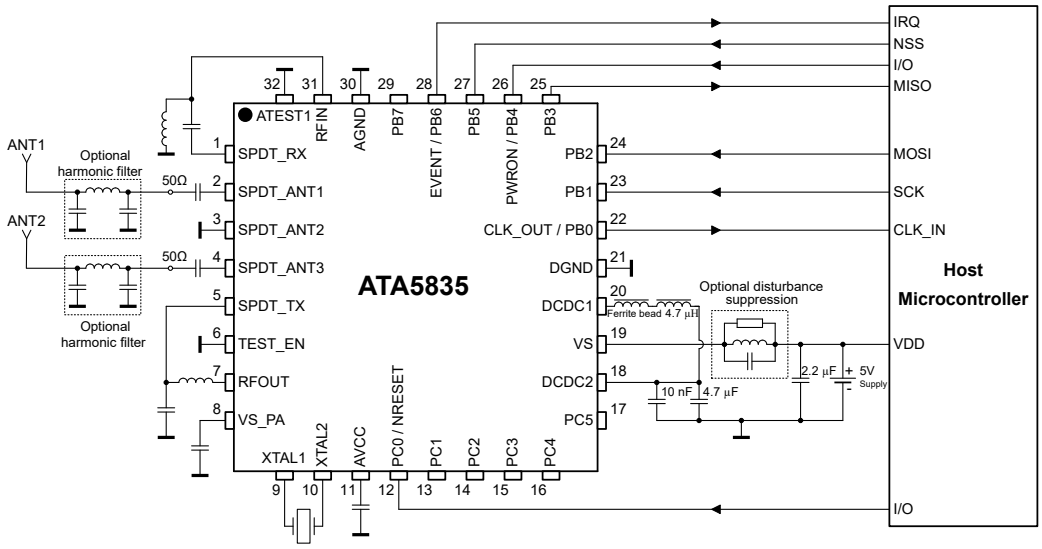


Figure 2-3 shows a typical vehicle side antenna diversity application circuit with an external host microcontroller running from a single 5V voltage regulator. The digital I/O pins are always part of the VS power domain, and therefore, set to 5V operation. All internal voltages are generated by the embedded power management circuitry. The DC-DC Converter is set up and activated to supply the analog front end and the power amplifier to substantially reduce the required power in the 5V domain.

The ATA5835 is powered on when the host sets the PWRON pin PB4 to ‘high’. After the internal start-up procedure, the ATA5835 enters the IDLEMode, which is signaled to the host by a system ready event on PB6. The system is now ready for SPI communication with the host. The ATA5835 can also be EEPROM-configured to directly switch to RXMode, PollingMode or TXMode after start-up.

The RF antenna switch is set up with two antennas at SPDT_ANT1 and SPDT_ANT3 for an antenna diversity application. The harmonic suppression can be improved by using an optional filter on the antenna side. If a SAW filter is used in the transmit path, the user has to ensure that the RF peak voltage on the pins, SPDT_ANTx and SPDT_TX, stays in the range between -0.3V and VS_PA + 0.3V. The antenna diversity algorithm itself is implemented in firmware and will automatically check the signal quality on both antennas whenever the RXMode is activated or a polling channel is checked. The better antenna is selected for telegram reception and stored for transmission of a successive Acknowledge message. This algorithm can significantly improve the service availability in scattered and disturbed environments when choosing an appropriate positioning and orientation of the antennas.

2.2.2 Typical 5V Triplexer Application with External Microcontroller

Figure 2-4. Typical 5V Triplexer Application

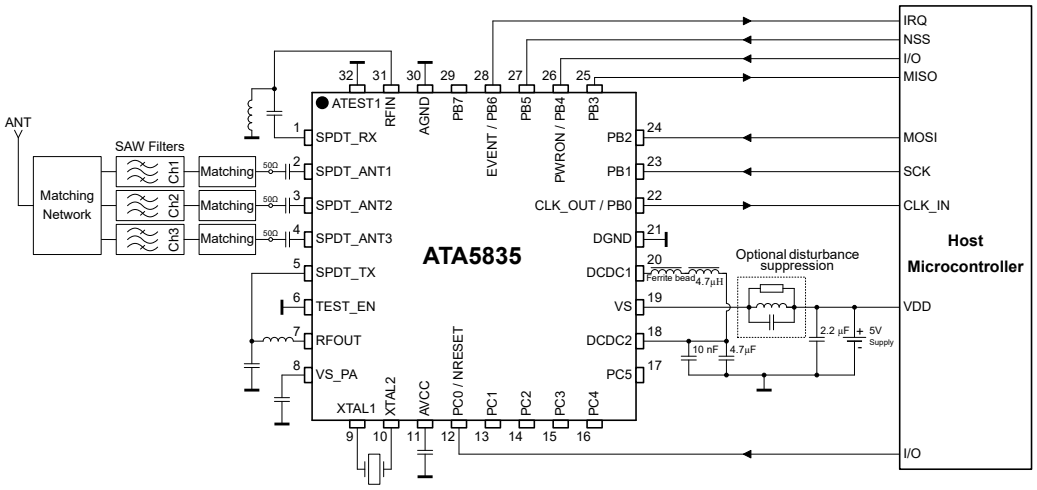


Figure 2-4 shows a typical vehicle side triplexer application circuit with an external host microcontroller running from a single 5V voltage regulator. The digital I/O pins are always part of the VS power domain, and therefore, set to 5V operation. All internal voltages are generated by the embedded power management circuitry. The DC-DC Converter is assembled and activated to supply the analog front end and the power amplifier to substantially reduce the required power in the 5V domain.

The ATA5835 is powered on when the host sets the PWRON pin PB4 to ‘high’. After the internal start-up procedure, the ATA5835 enters the IDLEMode, which is signaled to the host by a system ready event on PB6. The system is now ready for SPI communication with the host. The ATA5835 can also be EEPROM-configured to directly switch to RXMode, PollingMode or TXMode after start-up.

The RF antenna switch is assembled with three SAW filters for channel prefiltering in a high-end three-channel application. Together with the internal digital channel filter, this application provides excellent channel separation and robustness against interferences.

In a bidirectional application, the user has to ensure that the RF peak voltage on the pins, SPDT_ANTx and SPDT_TX, stays in the range between -0.3V and VS_PA + 0.3V.

2.2.3 Typical 5V Application Circuit with One-Wire Control

Figure 2-5. Typical 5V Application Circuit with One-Wire Control

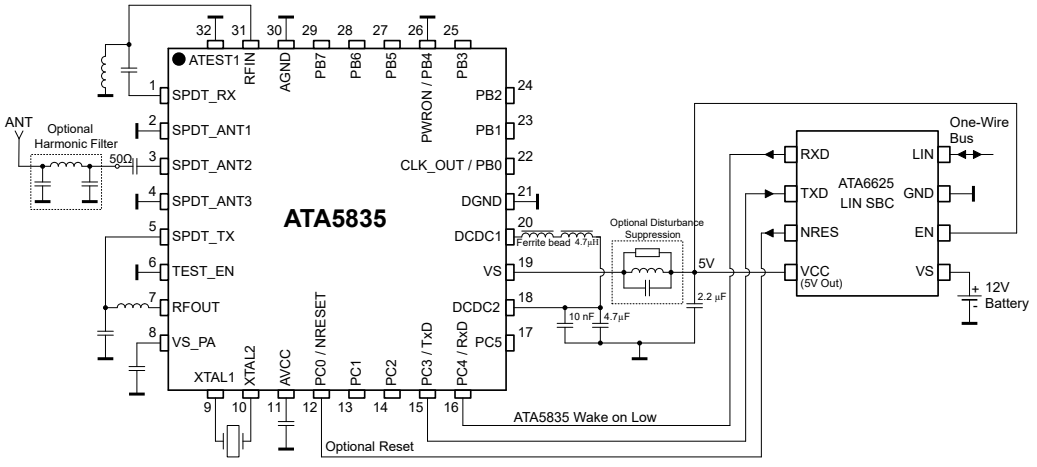


Figure 2-5 shows a typical vehicle side application circuit running from a 5V voltage regulator delivered from the LIN transceiver (for example, ATA6625) device. This application is especially suitable for remote antenna modules

located, for example, under the rooftop or next to window antennas. The ATA5835 can work autonomously and communicate to the external host microcontroller via a one-wire bus. The Flash inside the ATA5835 can be used to either integrate a LIN conformal software stack or a proprietary one-wire protocol. The integrated LIN-enabled UART IP can be used to reduce the processor and memory load for one-wire communication.

After connecting the ATA6625 to the 12V battery, the ATA5835 is permanently supplied with VS. A command on the one-wire bus wakes the ATA5835, which is then controlled by the customer application in Flash.

The unused digital ports can be left open when the internal 50 kΩ pull-up resistors are activated.

2.2.4 Typical 3V Stand-Alone Application

Figure 2-6. Typical 3V Stand-Alone Application

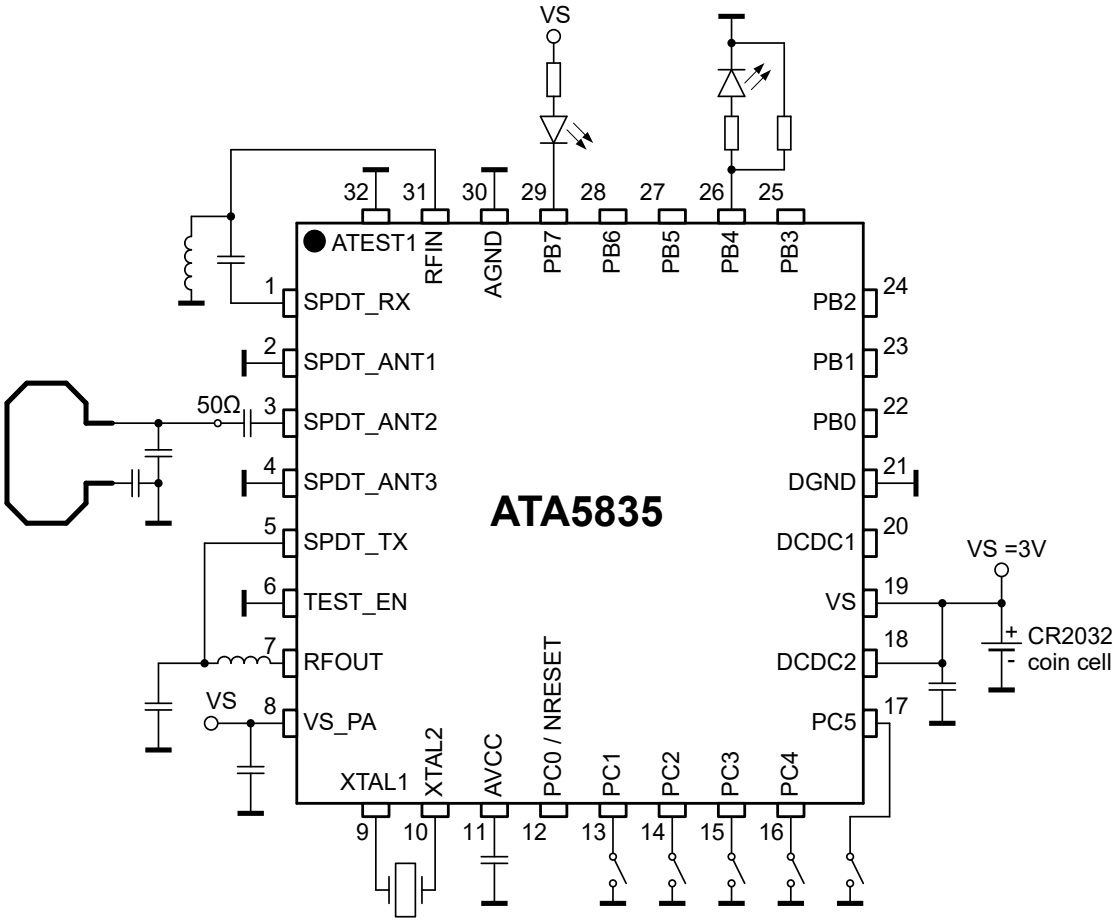


Figure 2-6 shows a stand-alone key fob application circuit running from a 3V lithium cell. The DC-DC Converter cannot be used in 3V mode, and, therefore, it must be short-circuited by connecting VS to DCDC2.

The ATA5835 stays in OFFMode until one of the NPWRON ports, PC1 to PC5, is pulled to ground level, waking up the circuit. The NPWRON ports, PC1 to PC5, have internal 50 kΩ pull-up resistors and can be left open if not used.

The user application software within the 20-Kbyte Flash is used to control the transceiver together with the ROM firmware.

In this application, LEDs can be connected to PB7 and PB4. At PB4, an additional pull-down resistor is recommended in parallel to prevent transverse currents in OFFMode.

3. System Functional Description

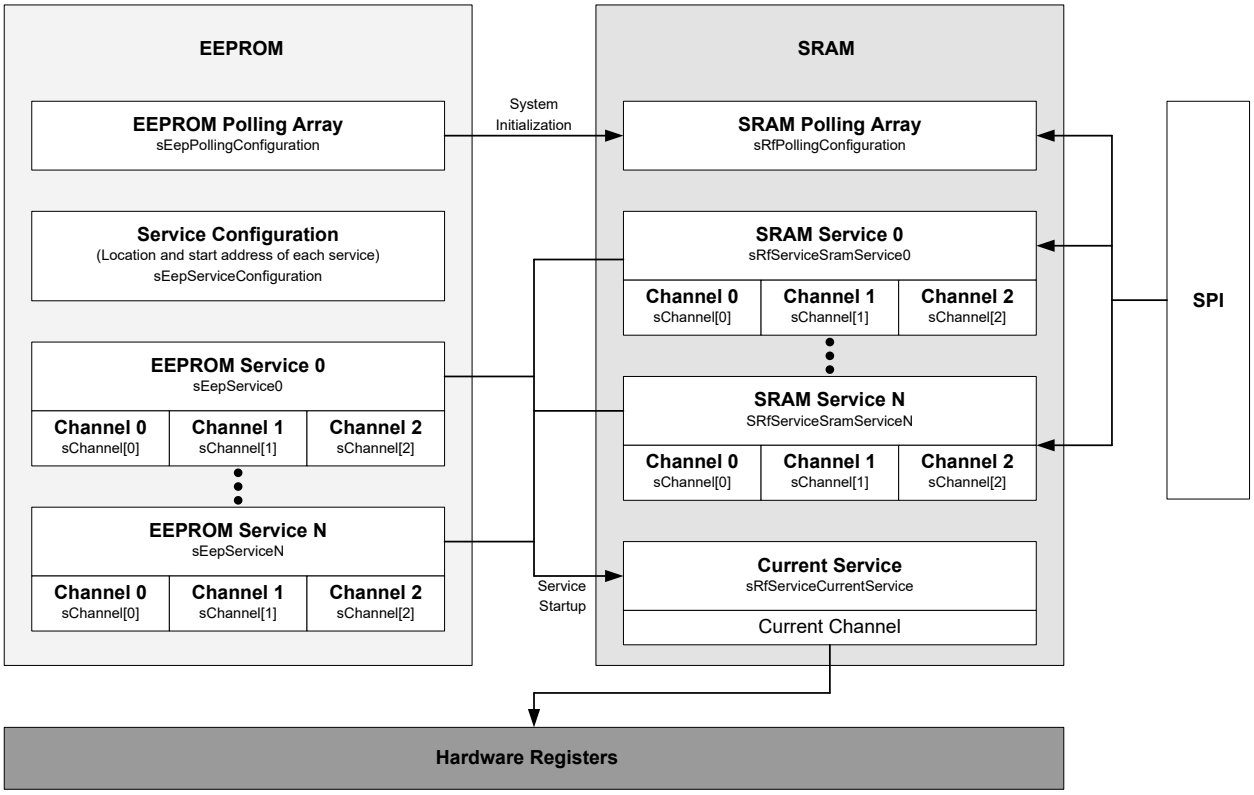
3.1 Functional Overview

3.1.1 Service-Based Concept

The ATA5835 is a highly configurable UHF transceiver. An internal 1024-byte EEPROM stores the configuration. The firmware controls the system. The system loads the general chip-wide settings from the EEPROM to hardware registers during system initialization. During start-up of the TXMode, RXMode or PollingMode, the system loads the service-specific settings from the EEPROM or SRAM to the current service in the SRAM, and from there to the corresponding hardware registers.

The following figure illustrates an overview on the service-based concept.

Figure 3-1. Service-Based Concept Overview



Service is a complete configuration set of the transceiver, which includes RF settings, demodulation settings and telegram handling information. Each service contains three channels that differ in the radio frequencies.

The ATA5835 supports up to eight services. The user can either store each service in the EEPROM (maximum four services) or SRAM (maximum seven services). The service configuration section in the EEPROM contains the information concerning which service is stored in which memory together with the corresponding start address. During run time, do not change the EEPROM-based services as these are fixed configurations that are programmed at the customer end of line. Write the SRAM services after start-up, either from an external host or as a copy of an EEPROM service. The user can modify the SRAM services by the Flash software application or SPI commands in the IDLEMode.

Each service consists of:

- One service-specific configuration part
- Three channel-specific configuration parts

Further configurations are available for the PollingMode and RSSI. In the IDLEMode, the user can modify the configurations via an SPI command and/or Flash user software.

3.1.2 Supported Telegrams

3.1.2.1 Telegram Structure

The system supports the transmission and reception of a wide variety of telegrams and protocols. Generally, the system can receive arbitrary telegrams. However, the chip contains designated hardware and software blocks that support the telegram structure illustrated in the following figure. Using this structure or parts of it will improve the sensitivity and the robustness of the broadcast.

Figure 3-2. Telegram Structure

<table>
<tr><td rowspan="2">Desync</td><td colspan="2">Preamble</td><td rowspan="2">Data Payload</td><td rowspan="2">Checksum</td><td rowspan="2">Stop Sequence</td></tr>
<tr><td>WUP</td><td>SFID</td></tr>
</table>

Desync
The de-synchronization is usually a coding violation with a length of several symbols that are supposed to provoke a defined restart of the receiver. The use of a de-synchronization leads to more deterministic receiver behavior, reducing the required preamble length. This can be favorable in timing-critical and energy-critical applications.

Preamble
The preamble is a pattern that is sent before the actual data payload to synchronize the receiver and provide the starting point of the payload. Microchip recommends a regular symbol pattern (example, 1-0-1-0...) for synchronization, Wake-Up Pattern (WUP), sometimes also called pre-burst, while a unique, well-defined pattern of up to 32 symbols is required to mark the start of the data payload (Start Frame Identifier (SFID) or Start bit). In polling scenarios, the WUP can be tens or hundreds of ms long.

Data Payload
The data payload contains the actual information content of the telegram. It can be NRZ or Manchester-coded. The length of the payload is application-dependent, typically 1 to 64 bytes.

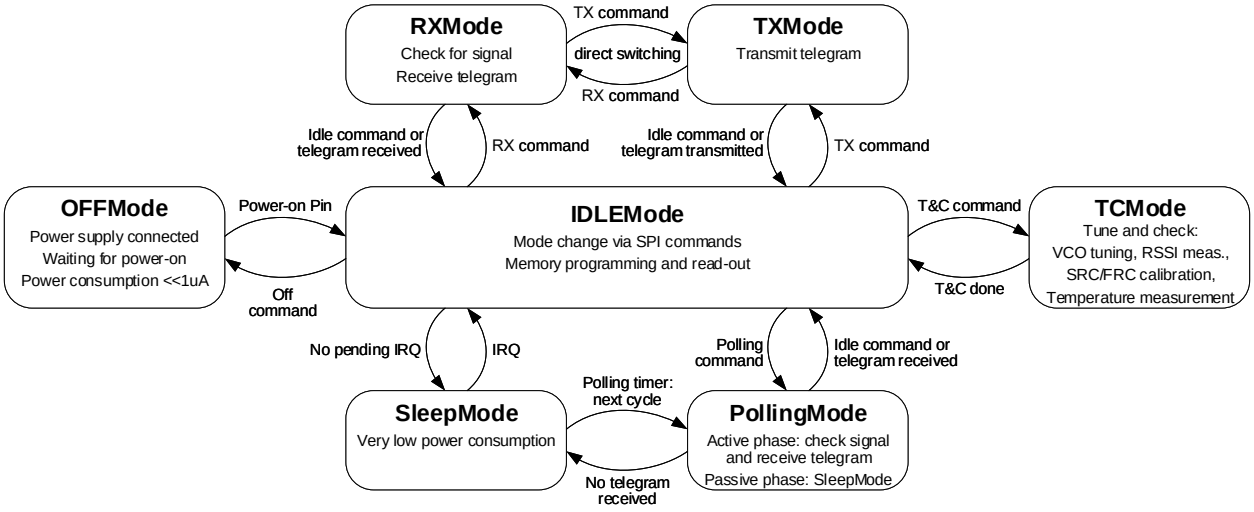
Checksum
The system calculates the checksum across the data payload to verify the received data. A typical example is an 8-bit CRC checksum.

Stop Sequence
The stop sequence is a short data pattern (typically, 2 to 6 symbols) to mark the end of the telegram. Use a coding violation to prevent additional (non-deterministic) data from being received.

3.2 Operating Modes Overview

The following figure illustrates an overview of the operating modes supported by the ATA5835:

Figure 3-3. Operating Modes Overview



After connecting the supply voltage to the VS pin, the ATA5835 always starts in OFFMode. All internal circuits are disconnected from the power supply; therefore, SPI communication is not supported. The ATA5835 can be woken up by activating the PWRON pin or one of the NPWRONx pins. This triggers the power-on sequence. After the initialization, the system reaches the IDLEMode.

The IDLEMode is the basic system mode supporting SPI communication and transitions to all other operating modes. There are two options of the IDLEMode requiring configuration in the EEPROM settings:

- IDLEMode(RC) with low-power consumption using the Fast RC (FRC) oscillator for processing
- IDLEMode(XTO) with active crystal oscillator for high-accuracy clock output or timing measurements

In the IDLEMode, the firmware cycles through the main loop. If there are no pending tasks during a main loop cycle, the processor system automatically switches into the configured SleepMode.

The TXMode enables data transmission using the selected service/channel configurations. It is usually enabled by the SPI command, “Set System Mode”, or directly after power-on when selected in the EEPROM setting. A system mode change can also be triggered by user Flash software.

The RXMode provides data reception on the selected service/channel configuration. The receiver continuously scans for a valid telegram and receives the data if all preconfigured checks are successful. The RXMode is usually enabled by the SPI command, “Set System Mode”, by user Flash software or directly after power-on when selected in the EEPROM setting.

In PollingMode, the receiver is activated for a short period of time to check for a valid telegram on the selected service/channel configurations. The receiver is deactivated if a valid telegram is not found. The SleepMode is entered until the polling cycle timer elapses. This process is repeated periodically in accordance with the polling configuration. The initial settings are stored in the EEPROM and copied during firmware initialization to the SRAM. This allows modification of the PollingMode timing and service/channel configuration during IDLEMode.

The TCMode offers calibration and self-checking functionality for the VCO and FRC oscillators, as well as for temperature measurement and polling cycle accuracy. This mode is activated via the SPI command, “Calibrate and Check”, or Flash software. When selected in the EEPROM settings, tune and check tasks are also used during system initialization after power-on. Furthermore, they can also be activated periodically during the PollingMode.

The following table shows the relation between the operating modes and their corresponding power supplies, clock sources and SleepMode settings.

Table 3-1. Operating Modes versus Power Supplies and Oscillators

Operation Mode	AVR® SleepMode	DVCC	AVCC	VS_PA	XTO	SRC	FRC
OFFMode	—	off	off	off	off	off	off

.....continued

Operation Mode	AVR® SleepMode	DVCC	AVCC	VS_PA	XTO	SRC	FRC
IDLEMode(RC)	Active mode Power-down(1)	on	off off	off off	off off	on on	on off
IDLEMode(XTO)	Active mode Power-down(1)	on	on on	off off	on on	on on	off off
TXMode	Active mode	on	on	on(2)	on	on	off
RXMode	Active mode	on	on	off	on	on	off
PollingMode(RC) - Active period - Sleep period	Active mode Power-down(1)	on	on off	off off	on off	on on	on off
PollingMode(XTO) - Active period - Sleep period	Active mode Power-down(1)	on	on on	off off	on on	on on	off off

Notes:

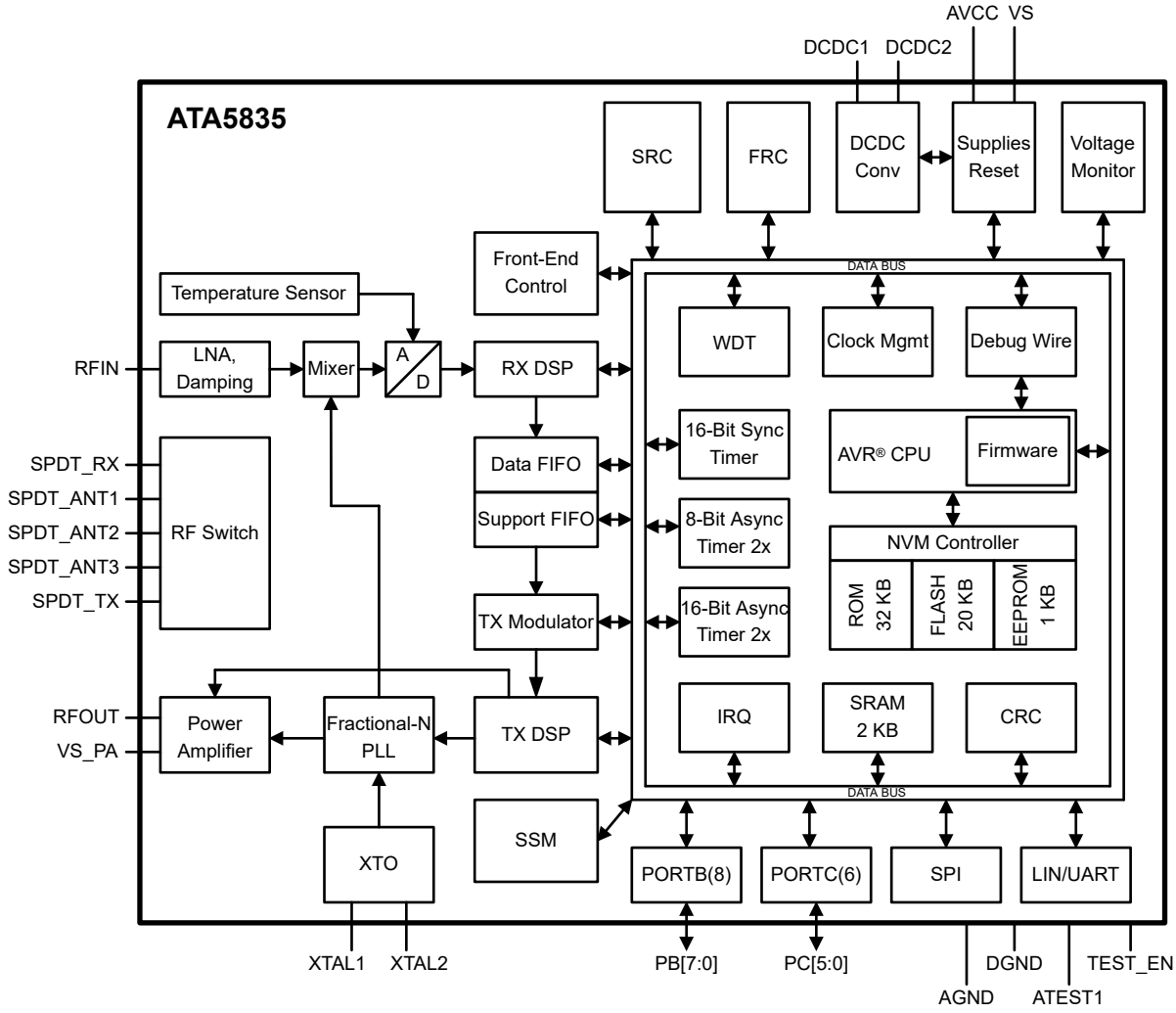
1. During the IDLEMode(RC) and the IDLEMode(XTO), the AVR microcontroller enters the SleepMode to reduce the current consumption. The SleepMode of the microcontroller section can be defined in the EEPROM. The power-down configuration is recommended for keeping the current consumption at a minimum.
2. Only activated at 5V applications. This is selectable in the EEPROM settings.

4. Hardware Description

4.1 Hardware Overview

The ATA5835 consists of an analog front end, Digital Signal Processing (DSP) blocks, an 8-bit AVR sub-system and supporting modules, such as oscillators and power regulators. The following figure illustrates the hardware block diagram of the device.

Figure 4-1. Hardware Block Diagram



The receiver system is based on a low-IF architecture. The fractional-N PLL, which is clocked by the crystal oscillator (XTO), generates the Local Oscillator (LO) signal for the mixer. The RF signal is input at the pin RFIN, amplified by a Low-Noise Amplifier (LNA) and down-converted by the mixer to the Intermediate Frequency (IF) of approximately 250 kHz using the LO signal. A 10-dB IF amplifier with low-pass filter characteristic is used to achieve enhanced system sensitivity without affecting blocking performance. After the mixer, the IF signal is sampled using a high-resolution Analog-to-Digital Converter (ADC). A damping stage in the LNA can be activated to increase the large-signal immunity of the system.

Within the RX Digital Signal Processing (RX DSP), the received signal from the ADC is filtered by a digital channel filter and successively demodulated. Two data receive paths, path A and path B, are included in the RX DSP after

the digital channel filter. In addition, the receive path can be configured to provide the digital output of an internal temperature sensor.

In the TXMode, the fractional-N PLL generates the TX frequency. The Power Amplifier (PA) generates a programmable RF output power signal at RFOUT. For more details on parameter number 10.00 output power of Electrical Characteristics, refer to the *ATA5835 UHF ASK/FSK Transceiver Data Sheet* (DS20005731). The FSK modulation is performed by changing the frequency setting of the fractional-N PLL dynamically by the TX Digital Signal Processing (TX DSP). Digital pre-emphasis and digital Gaussian shaping filter can be activated in the TX DSP to achieve higher data rates or reduce occupied bandwidth. The ASK modulation is performed by switching the power amplifier on and off. An ASK shaping filter is available to reduce the transmitted bandwidth of the modulated PA output signal. The shaping filter can also be used at the start and end of an FSK transmission.

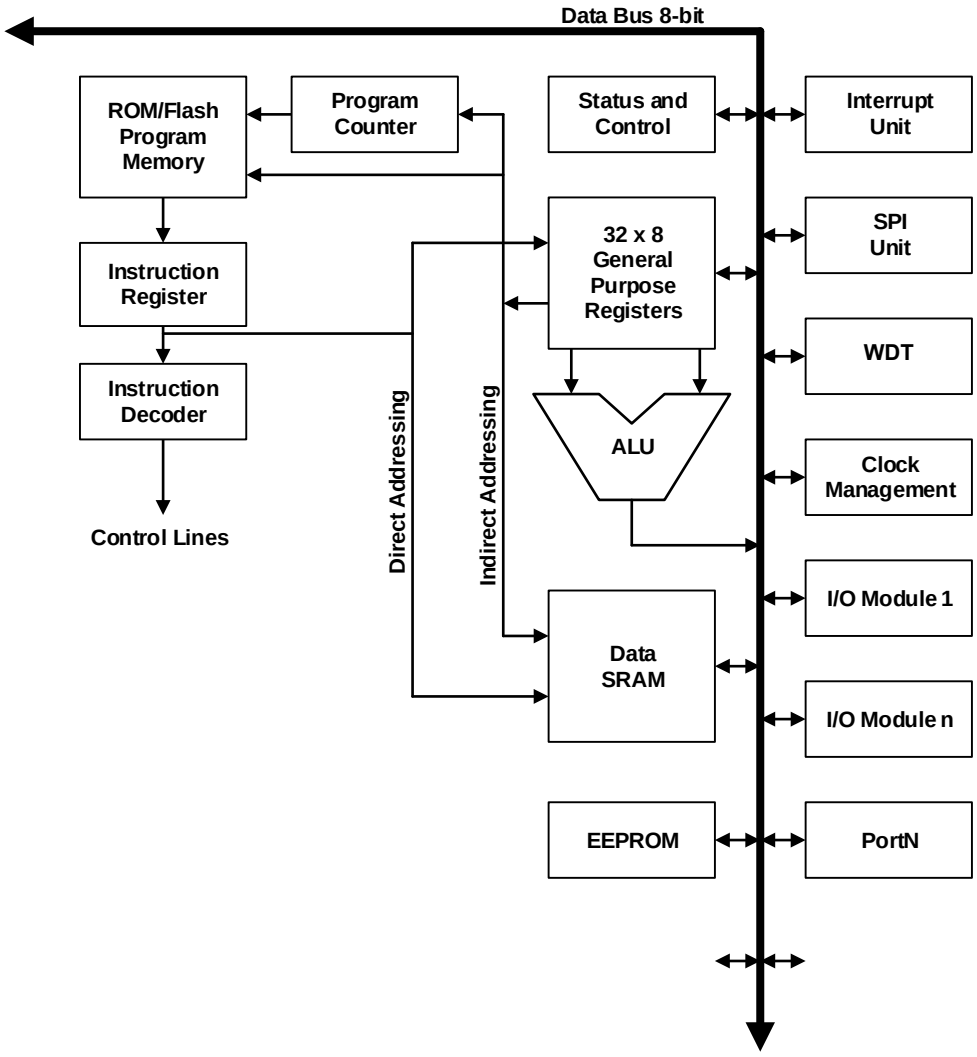
The internal RF switch has three antenna connection pins that allow antenna diversity applications or channel-dependent filtering of the RF signal. The RF switch can switch any antenna signal to the RX pin SPDT_RX or the TX pin SPDT_TX. These signals must be routed to the RFIN and RFOUT pins via external matching networks, respectively. In a single antenna RX application, the antenna can directly be connected to the RFIN pin without using the RF switch.

4.2 CPU Core

4.2.1 Architectural Overview

This section describes the AVR core architecture. The main function of the CPU core is to ensure correct program execution. Therefore, the CPU core can access memories, perform calculations, control peripherals and handle interrupts.

Figure 4-2. AVR Core Architecture - Overview



To maximize performance and parallelism, the AVR uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is prefetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system reprogrammable Flash memory and ROM.

The fast-access register file contains 32 × 8-bit general purpose working registers with a single clock cycle access time. This allows a single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the register file, the operation is executed and the result is stored in the register file, in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for Look-up Tables in the Flash program memory. Referred to as ‘X,’ ‘Y’ and ‘Z’ registers, these higher 16-bit function registers are described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The program flow is provided by conditional and unconditional jump and call instructions, which directly address the entire address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

The program memory space is divided in two sections, the boot program section and the application program section. Both sections have dedicated lock bits for write and read/write protection. The Store Program Memory (SPM) instruction that writes into the application Flash memory section must reside in the boot program section.

During interrupts and subroutine calls, the return address of the Program Counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM; the stack size is, thus, only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the Stack Pointer (SP) in the reset routine before subroutines or interrupts are executed. The SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

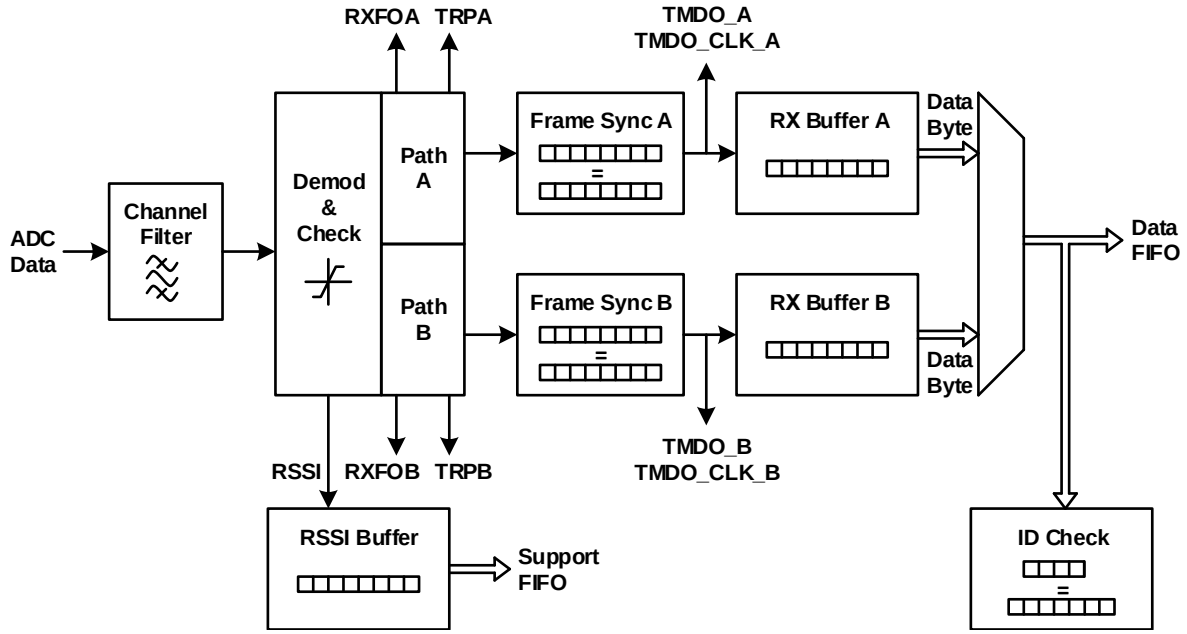
The I/O memory space contains 64 addresses for CPU peripheral functions as control registers, SPI and other I/O functions. The I/O memory can be accessed directly or as the data space locations following those of the register file, 0x20 to 0x5F. In addition, the circuit has extended I/O space from 0x60 to 0x1FF and SRAM, where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

4.3 RX Digital Signal Processing

The RX Digital Signal Processing (DSP) block performs the digital filtering, decoding, checking and byte-wise buffering of the RX samples that are derived from the ADC illustrated in the following figure. The RX DSP provides the following outputs:

- Raw demodulated data at the TRPA/B pins
- Decoded data at the TMDO and TMDO_CLK pins
- Buffered data bytes toward the data FIFO and ID check block
- Auxiliary information about the signal, such as the RSSI and the frequency offset of the received signal from the selected center frequency (RXFOA/B)

Figure 4-3. RX DSP Overview



The channel filter determines the receiver bandwidth. Its output is used for both receiving paths A and B, making it necessary to configure the filter to match both paths. The receiving paths A and B are identical and consist of an ASK and FSK demodulator with attached signal checks, a frame synchronizer that supports pattern-based searches for the telegram start and a 1-byte hardware buffer with integrated CRC checker for the received data.

Depending on the signal checks, one path is selected to write the received data to the data FIFO and optionally to the ID check block.

The RSSI values are determined by the demodulator and written via the RSSI buffer to the support FIFO where the latest 16 values are stored for further processing.

4.4 Transmit Path Overview

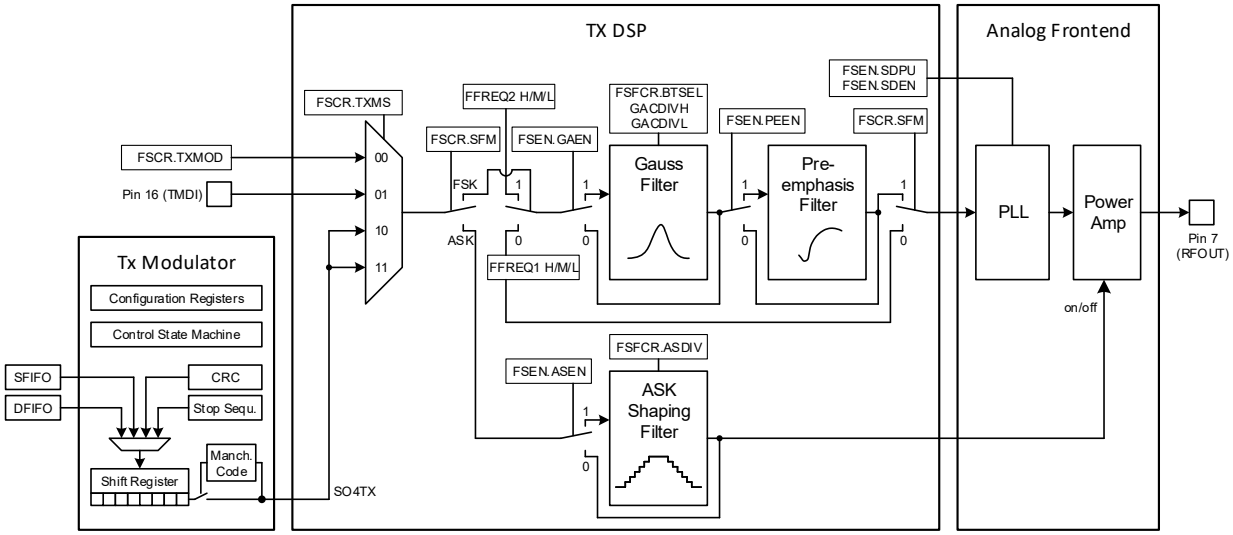
The ATA5835 integrates a transmitter that is capable of sending data with various options:

- Frequency bands 310 MHz to 318 MHz, 418 MHz to 477 MHz, 836 MHz to 928 MHz
- Data rates up to 80 kBits/s Manchester or 160 Ksym/s NRZ in buffered and transparent mode
- ASK or FSK modulation
- Transparent or buffered mode
- ASK shaping filter
- Gauss-shaping digital filter

This section describes the hardware blocks that are integrated to perform the transmit functionality. For detailed information on system and software flows, refer to the *ATA5835 UHF ASK/FSK Transceiver User's Guide* (DS50003152).

The following figure illustrates the transmit data path:

Figure 4-4. Transmit Data Path



The transmission data source can be selected either from a register bit, the transparent input pin 16 (TMDI), or the TX modulator that fetches the data from the DFIFO and SFIFO.

If ASK/OOK modulation is selected, the data stream is used to directly switch the power amplifier on and off. The transmitted carrier frequency is set by the PLL frequency synthesizer.

If FSK modulation is selected, the data stream is used to switch between two frequencies that are generated by the PLL frequency synthesizer. The power amplifier is constantly ON in this case. Power ramping (ASK shaping) can be used during on and off switching. To reduce the occupied bandwidth, a digital Gauss-shaping filter can be enabled. For data rates above 20 kHz Manchester or 40 kHz NRZ-coding, a digital preemphasis filter has to be enabled to compensate for the PLL loop filter.

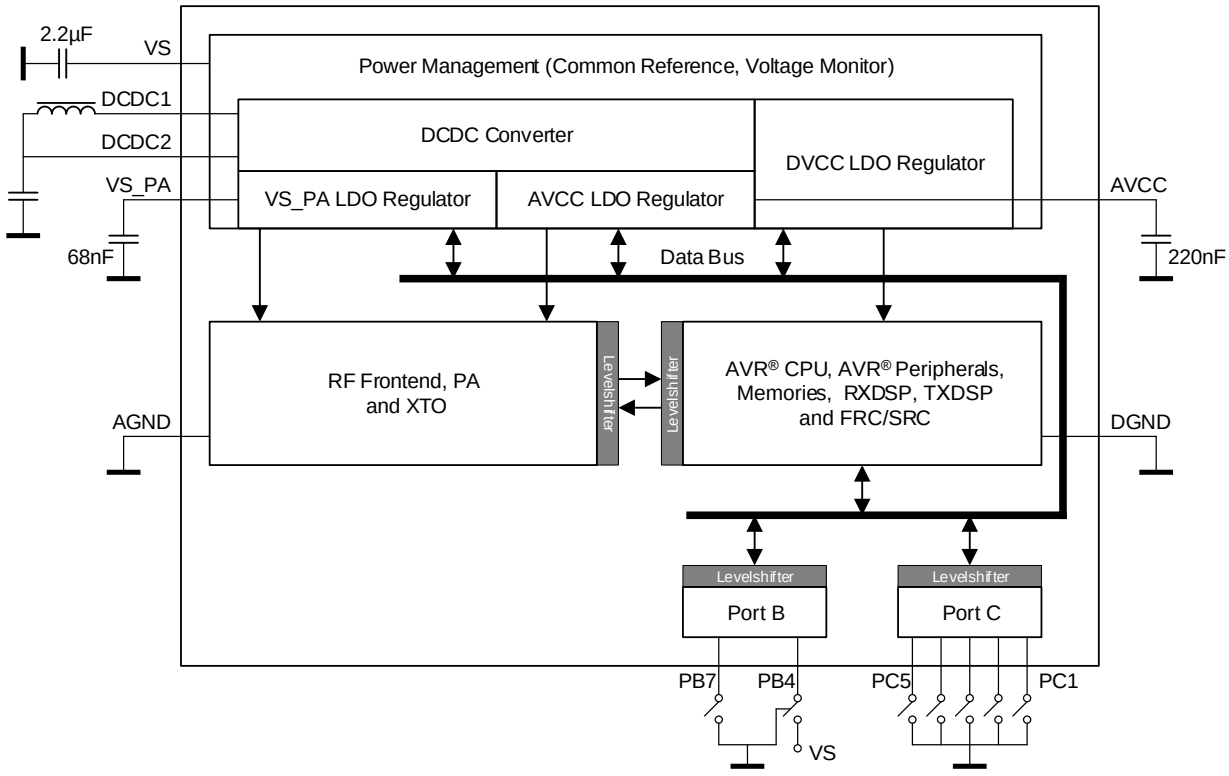
5. Power Management

The IC has four power domains:

1. VS – Unregulated battery voltage input
2. DVCC – Internally-regulated digital supply voltage. Typical value is 1.35V.
3. AVCC – Internally-regulated RF front end and XTO supply. Typical value is 1.85V.
4. VS_PA – Power amplifier supply: Depending on the battery voltage range (VS), the following application modes are available:
   - Connected externally to the battery in 3V applications (VS = VS_PA = 2.0V to 3.6V)
   - Generated by an internal 3V regulator in 3V/5V applications
     - VS = 3.2V to 5.5V; VS_PA = 3V
     - VS = 2.0V to 3.2V; VS_PA = VS – 200 mV
   - Generated by an internal 2.2V regulator in 3V/5V applications
     - VS = 2.4V to 5.5V; VS_PA = 2.2V
     - VS = 2.0V to 2.4V; VS_PA = VS – 200 mV

The device can be operated from VS = 2.0V to 3.6V (3V applications) and from VS = 2.4V to 5.5V (5V application). In the 5V application, an internal DC-DC converter can be activated to reduce the power consumption in the AVCC and VS_PA domain. In this case, the minimal VS voltage is 4.5V. The operating mode can be programmed in SUPCR.PVEN.

Figure 5-1. Power Supply Management



6. Ordering Information

Extended Type Number	Package	Remarks
ATA5835-GHQW-VAO	32-Lead QFN	5x5 mm, 6k tape and reel, PB-free, wettable flanks

7. Package Information

This section details the package marking information and package outline drawings.

7.1 Package Marking Information

The following figure illustrates the package marking information of the ATA5835.

Figure 7-1. 32-Lead QFN (5 mm x 5 mm x 0.5 mm)

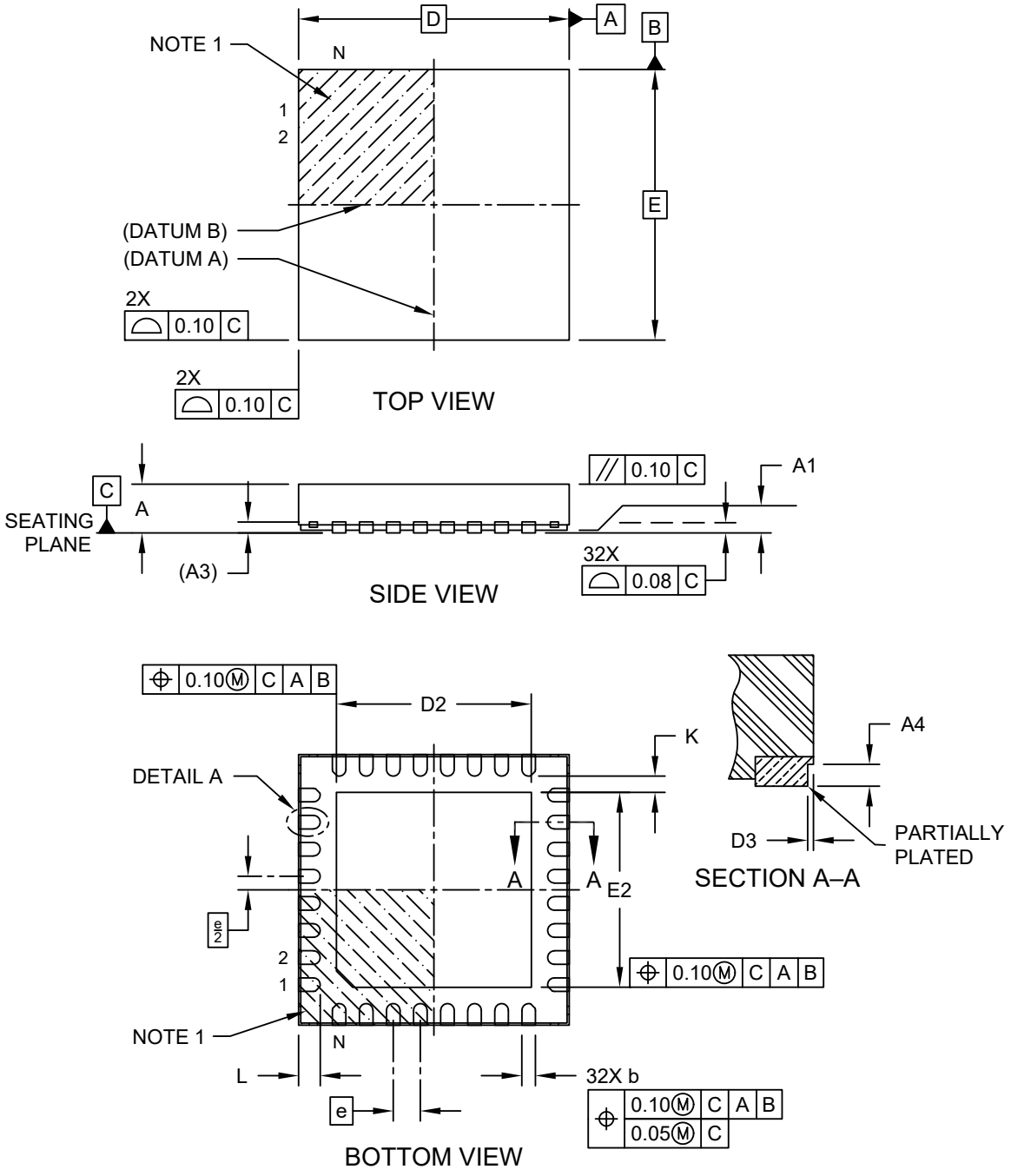
Table 7-1. Package Legend Description

Legend	Description
YY	Year code (last two digits of calendar year)
WW	Week code (for example, week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code

7.2 Package Outline Drawing

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZBS

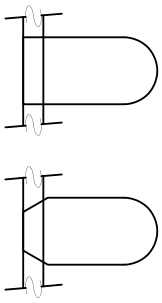
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



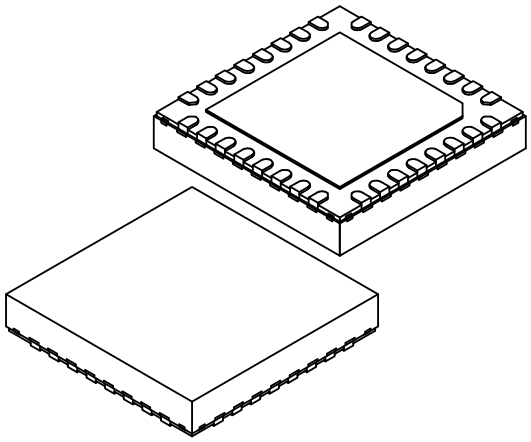
Microchip Technology Drawing C04-21391 Rev G Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZBS

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Width	D3	-	-	0.085
Wettable Flank Step Cut Depth	A4	0.10	-	0.19

Dimensions D3 and A4 above apply to all new products released after November 1, and all products shipped after January 1, 2019, and supersede dimensions D3 and A4 below.
No physical changes are being made to any package; this update is to align cosmetic and tolerance variations from existing suppliers.

Wettable Flank Step Length	D3	0.035	0.06	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

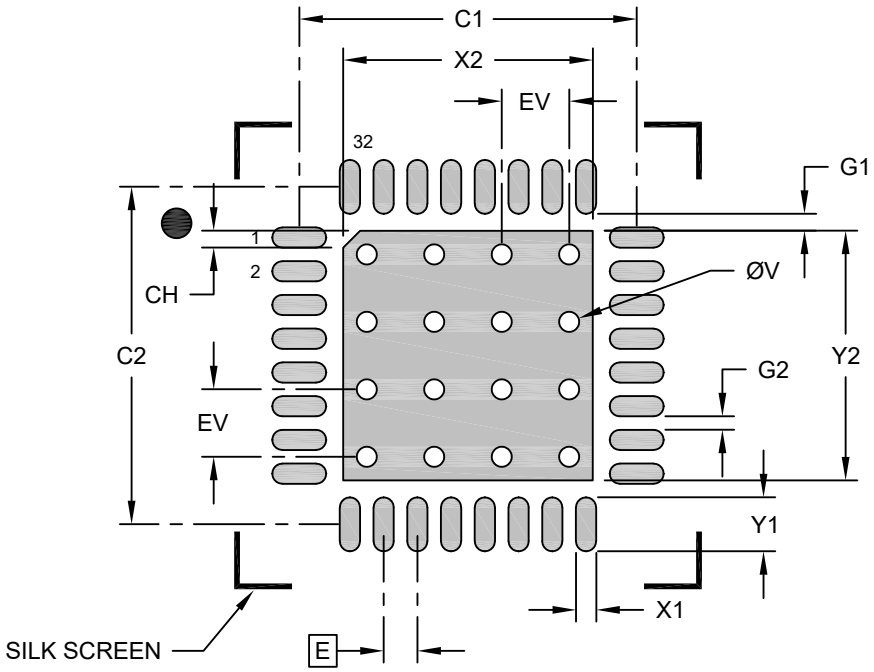
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21391 Rev G Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZBS

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Exposed Pad 45° Corner Chamfer	CH		0.25	
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.80
Contact Pad to Center Pad (X32)	G1	0.25		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23391 Rev G

8. Document Revision History

Revision	Date	Section	Description
A	03/2022	Document	Initial revision

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

Trademarks

ISBN: 978-1-5224-9973-2

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820