PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family

32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology

Operating Conditions
- -40ºC to +85ºC, -40ºC to +105ºC, DC to 200 MHz
  - VDDIO = 2.2V to 3.6V
  - VDDCORE = 1.7V to 1.9V

Core: 200 MHz/330 DMIPS MIPS32® microAptiv™
- 32 KB I-Cache, 32 KB D-Cache
- MMU for optimum embedded OS execution
- microMIPS™ mode for up to 35% smaller code size
- DSP-enhanced core:
  - Four 64-bit accumulators
  - Single-cycle MAC, saturating and fractional math
- Code-efficient (C and Assembly) architecture

Clock Management
- Programmable PLLs and oscillator clock sources
- Dedicated PLL for DDR2
- Fail-Safe Clock Monitor
- Independent Watchdog and Deadman Timers
- Fast wake-up and start-up

Power Management
- Various power management options for extreme power reduction (Sleep and Idle)
- Integrated POR and BOR
- Programmable High/Low-Voltage Detect (HLVD) on VDDIO and High-Voltage Detect (HVD) on VDDR1V8

Memory Interfaces
- Internal DDR2 SDRAM interface (up to DDR2-400)
- SD/SDIO/eMMC bus interface (up to 50 MHz)
- Serial Quad Interface (up to 76 MHz)
- External Bus Interface (up to 50 MHz)

Graphics Features
- 3-layer Graphics Controller with up to 24-bit color support
- High-performance 2D Graphics Processing Unit (GPU)

Audio Interfaces
- Audio data communication: I^2S, LJ, and RJ
- Audio control interfaces: SPI and I^2C
- Audio host clock: Fractional clock frequencies with USB synchronization

High-Speed Communication Interfaces (with Dedicated DMA)
- USB 2.0 High-Speed On-The-Go (OTG) controller
- 10/100 Mbps Ethernet MAC with MII and RMII interface

Security Features
- Crypto Engine with a RNG for data encryption/decryption and authentication (AES, 3DES, SHA, MD5, and HMAC)
- Advanced memory protection:
  - Peripheral and memory region access control

Direct Memory Access (DMA)
- Eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)

Advanced Analog Features
- 12-bit ADC modules:
  - 18 Msps with up to six ADC circuits (five dedicated and one shared)
  - Up to 45 analog input
  - Can operate during Sleep and Idle modes
  - Multiple trigger sources
  - Six Digital Comparators and six Digital Filters
- Two Comparators with 32 programmable voltage references
- Temperature sensor with ±2ºC accuracy
- Charge Time Measurement Unit (CTMU)

Communication Interfaces
- Two CAN modules (with dedicated DMA channels):
  - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (25 Mbps):
  - Supports up to LIN 2.1 and IrDA® protocols
- Six 4-wire SPI modules (up to 50 MHz)
- SQI configurable as additional SPI module (up to 80 MHz)
- Five I^2C modules (up to 1 Mbaud) with SMBus support
- Parallel Host Port (PMP)
- Peripheral Pin Select (PPS) to enable function remap

Timers/Output Compare/Input Capture
- Nine 16-bit and up to four 32-bit timers/counters
- Nine Output Compare (OC) modules
- Nine Input Capture (IC) modules
- Real-Time Clock and Calendar (RTCC) module

Input/Output
- 5V-tolerant pins with up to 32 mA source/sink
- Selectable open drain, pull-ups, and pull-downs
- Selectable slew rate control
- External interrupts on all I/O pins
- PPS to enable function remap

Qualification and Class B Support
- Class B Safety Library, IEC 60730
- Back-up internal oscillator
- AEC-Q100 Grade 1 (-40ºC to +105ºC)

Debugger Development Support
- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited software and 12 complex breakpoints
- IEEE® 1149.2-compatible (JTAG) boundary scan
- Non-intrusive hardware-based instruction trace

Integrated Software Libraries and Tools
- C/C++ compiler with native DSP/fractional support
- MPLAB® Harmony Integrated Software Framework
- TCP/IP, USB, Graphics, and mTouch™ middleware
- MFi, Android™, and Bluetooth® audio frameworks
- RTOS Kernels: Express Logic ThreadX, FreeRTOS™, OPEN-RTOS®, Micriμm® μC/OS™, and SEGGER embOS®

Packages

Type	LFBGA	LQFP
Pin Count	169	176
I/O Pins (up to)	120	120
Contact/Lead Pitch	0.8 mm	0.4 mm
Dimensions	11x11 mm	20x20 mm

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TABLE 1: PIC32MZ DAK/DAL/DAR/DAS FEATURES COMMON TO ALL DEVICES

Boot Flash Memory (KB)	Remappable Peripherals						12-bit ADC Channels	Analog Comparators	CTMU	USB 2.0 HS OTG	I^2C	GLCD	GPU	EBI	PMP	SQI	SDHC	RTCC	Ethernet	I/O Pins	JTAG	Trace
	Remappable Pins	Timers(1)/Capture/Compare	UART	SPI/I^2S	CAN 2.0B	External Interrupts(2)																
160	47	9/9/9	6	6	2	5	45	2	Y	Y	5	Y	Y	Y	Y	Y	Y	Y	Y	120	Y	Y

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.

TABLE 2: 169-PIN LFBGA PIC32MZ DAK/DAL/DAR/DAS FEATURES

Devices	Program Memory (KB)	Data Memory (KB)	DDR2 Controller Interface (Internal)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/Dedicated)	Package
PIC32MZ1025DAK169	1024	256	No	—	N	8/24	HF
PIC32MZ1025DAL169					Y	8/26	
PIC32MZ1064DAK169		640			N	8/24	
PIC32MZ1064DAL169					Y	8/26	
PIC32MZ2025DAK169	2048	256			N	8/24	
PIC32MZ2025DAL169					Y	8/26	
PIC32MZ2064DAK169		640			N	8/24	
PIC32MZ2064DAL169					Y	8/26	
PIC32MZ1025DAR169	1024	256	Yes	32	N	8/24	6J
PIC32MZ1025DAS169					Y	8/26	
PIC32MZ1064DAR169		640			N	8/24	
PIC32MZ1064DAS169					Y	8/26	
PIC32MZ2025DAR169	2048	256			N	8/24	
PIC32MZ2025DAS169					Y	8/26	
PIC32MZ2064DAR169		640			N	8/24	
PIC32MZ2064DAS169					Y	8/26	

TABLE 3: 176-PIN LQFP PIC32MZ DAK/DAL/DAR/DAS FEATURES

Devices	Program Memory (KB	Data Memory (KB	DDR2 Controller Interface (Internal)	DDR2 SDRAM Size (MB)	Crypto/RNG	DMA Channels (Programmable/Dedicated)	Package
PIC32MZ1025DAK176	1024	256	No	—	N	8/24	2J
PIC32MZ1025DAL176					Y	8/26	
PIC32MZ1064DAK176		640			N	8/24	
PIC32MZ1064DAL176					Y	8/26	
PIC32MZ2025DAK176	2048	256			N	8/24	
PIC32MZ2025DAL176					Y	8/26	
PIC32MZ2064DAK176		640			N	8/24	
PIC32MZ2064DAL176					Y	8/26	
PIC32MZ1025DAR176	1024	256	Yes	32	N	8/24	
PIC32MZ1025DAS176					Y	8/26	
PIC32MZ1064DAR176		640			N	8/24	
PIC32MZ1064DAS176					Y	8/26	
PIC32MZ2025DAR176	2048	256			N	8/24	
PIC32MZ2025DAS176					Y	8/26	
PIC32MZ2064DAR176		640			N	8/24	
PIC32MZ2064DAS176					Y	8/26	

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Device Pin Tables

TABLE 4: PIN NAMES FOR 169-PIN DEVICES

169-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAK169
PIC32MZ1025DAL169
PIC32MZ1064DAK169
PIC32MZ1064DAL169
PIC32MZ2025DAK169
PIC32MZ2025DAL169
PIC32MZ2064DAK169
PIC32MZ2064DAL169
PIC32MZ1025DAR169
PIC32MZ1025DAS169
PIC32MZ1064DAR169
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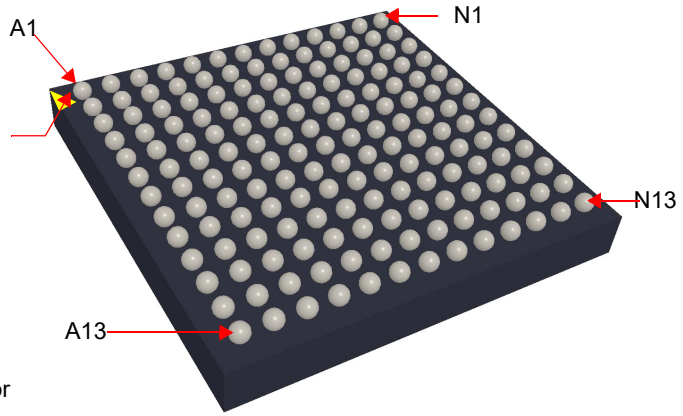
PIC32MZ2064DAS169



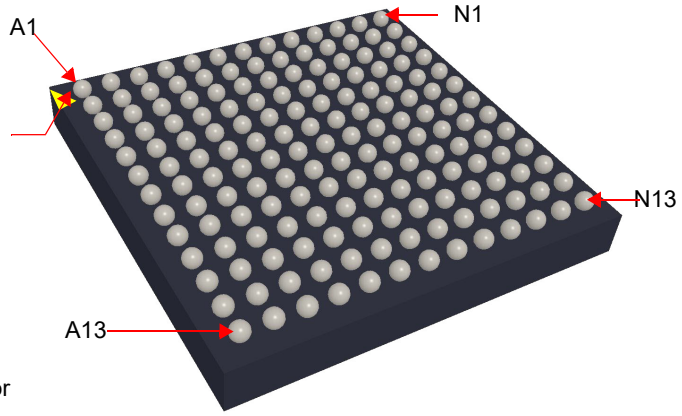
Ball/Pin Number	Full Pin Name	Ball/Pin Number	Full Pin Name
A1	No Connect	C5	EBIA2/AN23/C2INC/RPG9/PMA2/RG9
A2	VBUS	C6	TDO/AN31/RPF12/RF12
A3	RPF2/SDA3/RF2	C7	EBID7/AN15/PMD7/RE7
A4	EBID1/AN39/PMD1/RE1	C8	AVSS
A5	AN21/RG15	C9	VDDCORE
A6	TDI/AN17/SCK5/RF13	C10	VREF+/CVREF+/AN28/RA10
A7	$\overline{\text{EBIWE}}$/AN34/RPC3/PMWR/RC3	C11	CVREFOUT/AN5/RPB10/RB10
A8	EBID12/AN10/RPC2/PMD12/RC2	C12	PGED1/AN0/RPB0/CTED2/RB0
A9	EBID10/AN4/RPB8/PMD10/RB8	C13	SOSCI/RPC13(6)/RC13(6)
A10	AN8/RPB3/RB3	D1	TRD3/SDDATA3/SQID3/RA7
A11	EBIA5/AN7/PMA5/RA5	D2	TMS/$\overline{\text{SDCD}}$/RA0
A12	AN2/C1INB/RB4	D3	USBID
A13	AN1/C2INB/RPB2/RB2	D4	AN20/RH4
B1	D-	D5	AN13/C1INC/RPG7/SDA4/RG7
B2	VUSB3V3	D6	AN26/RPE9/RE9
B3	EBID4/AN18/PMD4/RE4	D7	PGEC2/RPB6/RB6
B4	VDDCORE	D8	AVSS
B5	AN30/C2IND/RPG8/SCL4/RG8	D9	AVDD
B6	VDDIO	D10	VBAT
B7	EBID5/AN12/RPC1/PMD5/RC1	D11	AN45/RPB5/RB5
B8	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	D12	PGED2/C1INA/AN46/RPB7/RB7
B9	PGEC1/AN9/RPB1/CTED1/RB1	D13	SOSCO/RPC14(6)/T1CK/RC14(6)
B10	AN3/C2INA/RPB15/OCFB/RB15	E1	TRD2/SDDATA2/SQID2/RG14
B11	VREF-/CVREF-/AN27/RA9	E2	TRD0/SDDATA0/SQID0/RG13
B12	EBIA7/AN47/HLVDIN/RPB9/PMA7/RB9	E3	TRD1/SDDATA1/SQID1/RG12
B13	AN6/RB12	E4	TRCLK/SDCK/SQICLK/RA6
C1	D+	E5	AN14/C1IND/SCK2/RG6
C2	VSS	E6	AN25/RPE8/RE8
C3	INT0/RH14	E7	AN49/RB11
C4	EBID0/PMD0/RE0	E8	GD20/EBIA22/RJ3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 2 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
5: This pin is a 'No Connect' in devices without DDR. Add 0.1uF and 0.01uF capacitors in parallel between DDRVREF pin and ground, when DDRVREF is used.
6: These pins are restricted to input functions only.

TABLE 4: PIN NAMES FOR 169-PIN DEVICES (CONTINUED)

169-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAK169
PIC32MZ1025DAL169
PIC32MZ1064DAK169
PIC32MZ1064DAL169
PIC32MZ2025DAK169
PIC32MZ2025DAL169
PIC32MZ2064DAK169
PIC32MZ2064DAL169
PIC32MZ1025DAR169
PIC32MZ1025DAS169
PIC32MZ1064DAR169
PIC32MZ1064DAS169
PIC32MZ2025DAR169
PIC32MZ2025DAS169
PIC32MZ2064DAR169
PIC32MZ2064DAS169



Ball/Pin Number	Full Pin Name	Ball/Pin Number	Full Pin Name
E9	AN22/RPD14/RD14	H2	SCK4/RD10
E10	AN29/SCK3/RB14	H3	RTCC/RPD0/RD0
E11	TCK/AN24/RA1	H4	VSS1V8
E12	OSC1/CLKI/RC12	H5	VDDR1V8(4)
E13	OSC2/CLKO/RC15	H6	VDDR1V8(4)
F1	SDCMD/SQICS0/RPD4/RD4	H7	VSS
F2	SQICS1/RPD5/RD5	H8	VSS
F3	EBIA6/RPE5/PMA6/RE5	H9	VDDIO
F4	DDRVREF(5)	H10	GD13/EBIA18/RK4
F5	VSS	H11	EBIA3/AN11/PMA3/RK2
F6	EBID6/AN16/PMD6/RE6	H12	$\overline{\text{SDWP}}$/EBIRP/RH2
F7	AN48/CTPLS/RB13	H13	EBIA0/PMA0/RJ15
F8	GD18/EBIBS1/RJ10	J1	GD7/EBIA12/RPD12/PMA12/RD12
F9	GD9/EBIBS0/RJ12	J2	GD22/EBIA13/PMA13/RD13
F10	EBIRDY3/AN32/RJ2	J3	RPF8/SCL3/RF8
F11	AN33/SCK6/RD15	J4	VSS1V8
F12	HSYNC/EBICS1/RJ5	J5	VDDR1V8(4)
F13	VSYNC/EBICS0/RJ4	J6	VDDR1V8(4)
G1	SCK1/RD1	J7	VSS
G2	GD10/EBIA14/RPD2/PMA14/PMCS1/RD2	J8	VSS
G3	GD11/EBIA15/RPD3/PMA15/PMCS2/RD3	J9	VDDIO
G4	VSS1V8	J10	GD14/EBIA19/RK5
G5	VSS	J11	EBIA1/AN38/PMA1/RK1
G6	VSS	J12	EBIA4/AN36/PMA4/RH7
G7	VSS	J13	AN35/RH3
G8	VSS	K1	$\overline{\text{MCLR}}$
G9	VDDIO	K2	GD16/EBID8/RPF5/SCL5/PMD8/RF5
G10	GD8/EBID11/PMD11/RJ14	K3	GD5/EBIA10/RPF1/PMA10/RF1
G11	GCLK/EBICS2/RJ6	K4	VSS1V8
G12	GD0/EBID13/PMD13/RJ13	K5	VDDR1V8(4)
G13	GEN/EBICS3/RJ7	K6	VDDR1V8(4)
H1	GD2/EBID15/RPD9/PMD15/RD9	K7	VSS

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 2 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
5: This pin is a 'No Connect' in devices without DDR. Add 0.1uF and 0.01uF capacitors in parallel between DDRVREF pin and ground, when DDRVREF is used.
6: These pins are restricted to input functions only.

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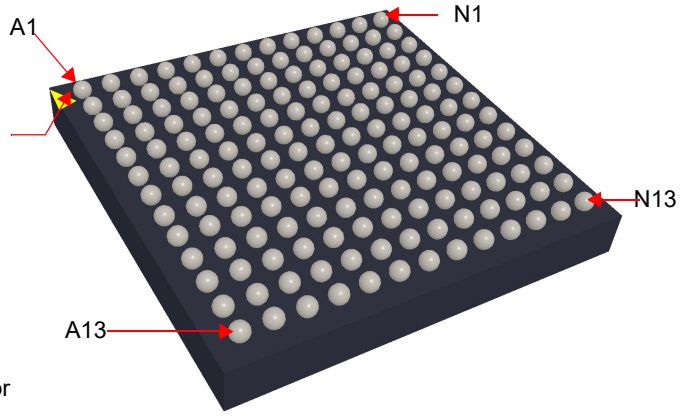
TABLE 4: PIN NAMES FOR 169-PIN DEVICES (CONTINUED)

169-PIN LFBGA (BOTTOM VIEW)

PIC32MZ1025DAK169
PIC32MZ1025DAL169
PIC32MZ1064DAK169
PIC32MZ1064DAL169
PIC32MZ2025DAK169
PIC32MZ2025DAL169
PIC32MZ2064DAK169
PIC32MZ2064DAL169
PIC32MZ1025DAR169
PIC32MZ1025DAS169
PIC32MZ1064DAR169
PIC32MZ1064DAS169
PIC32MZ2025DAR169
PIC32MZ2025DAS169
PIC32MZ2064DAR169
PIC32MZ2064DAS169



Ball/Pin Number	Full Pin Name
K8	VSS
K9	VDDIO
K10	EMDIO/RJ1
K11	ETXEN/RPD6/RD6
K12	GD23/EBIA16/RK0
K13	EBIRDY2/AN37/RH11
L1	GD6/EBIA11/RPF0/PMA11/RF0
L2	GD21/EBIA23/RH15
L3	GD17/EBID9/RPF4/SDA5/PMD9/RF4
L4	VSS1V8
L5	VSS1V8
L6	VDDIO
L7	VDDIO
L8	VDDCORE
L9	VDDIO
L10	ETXERR/RJ0
L11	GD1/EBID14/PMD14/RA4
L12	SCL2/RA2
L13	GD12/EBIA17/RK3
M1	ERXERR/RPF3/RF3
M2	GD4/EBIA9/RPG1/PMA9/RG1
M3	EBID3/RPE3/PMD3/RE3
M4	ERXD1/RH5

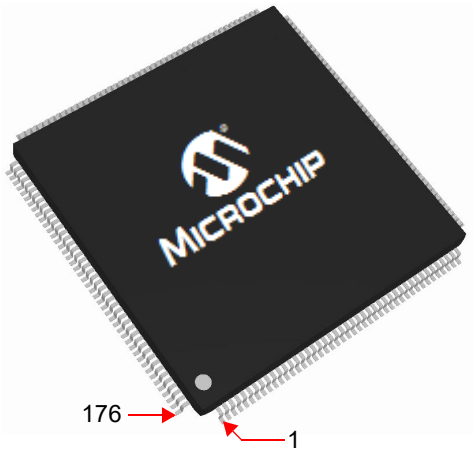
Ball/Pin Number	Full Pin Name
M5	ERXDV/ECRSDV/RH13
M6	ECOL/RH10
M7	ETXD3/RH1
M8	ETXD2/RH0
M9	ETXD1/RJ9
M10	ETXCLK/RPD7/RD7
M11	RPA14/SCL1/RA14
M12	GD19/EBIA21/RK7
M13	GD15/EBIA20/RK6
N1	VDDCORE
N2	GD3/EBIA8/RPG0/PMA8/RG0
N3	EBID2/PMD2/RE2
N4	ERXD2/RH6
N5	ECRS/RH12
N6	ERXD3/RH9
N7	ERXD0/RH8
N8	ERXCLK/EREFCLK/RJ11
N9	ETXD0/RJ8
N10	EMDC/RPD11/RD11
N11	RPA15/SDA1/RA15
N12	EBIRDY1/SDA2/RA3
N13	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 2 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
5: This pin is a 'No Connect' in devices without DDR. Add 0.1uF and 0.01uF capacitors in parallel between DDRVREF pin and ground, when DDRVREF is used.
6: These pins are restricted to input functions only.

TABLE 5: PIN NAMES FOR 176-PIN DEVICES

176-PIN LQFP (TOP VIEW)

PIC32MZ1025DAK176
PIC32MZ1025DAL176
PIC32MZ1064DAK176
PIC32MZ1064DAL176
PIC32MZ2025DAK176
PIC32MZ2025DAL176
PIC32MZ2064DAK176
PIC32MZ2064DAL176
PIC32MZ1025DAR176
PIC32MZ1025DAS176
PIC32MZ1064DAR176
PIC32MZ1064DAS176
PIC32MZ2025DAR176
PIC32MZ2025DAS176
PIC32MZ2064DAR176
PIC32MZ2064DAS176



Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	VREF-/CVREF-/AN27/RA9	37	VSS
2	VREF+/CVREF+/AN28/RA10	38	VDDIO
3	AVDD	39	VDDCORE
4	AVDD	40	EBID0/PMD0/RE0
5	AVSS	41	RPF2/SDA3/RF2
6	AVSS	42	INT0/RH14
7	AN3/C2INA/RPB15/OCFB/RB15	43	EBID4/AN18/PMD4/RE4
8	AN8/RPB3/RB3	44	No Connect
9	AN48/CTPLS/RB13	45	VBUS
10	EBID10/AN4/RPB8/PMD10/RB8	46	VUSB3V3
11	PGEC1/AN9/RPB1/CTED1/RB1	47	VUSB3V3
12	AN49/RB11	48	VSS
13	PGEC2/RPB6/RB6	49	VSS
14	EBID12/AN10/RPC2/PMD12/RC2	50	D-
15	$\overline{\text{EBIWE}}$/AN34/RPC3/PMWR/RC3	51	D+
16	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	52	USBID
17	EBID5/AN12/RPC1/PMD5/RC1	53	TMS/$\overline{\text{SDCD}}$/RA0
18	VDDCORE	54	TRCLK/SDCK/SQICLK/RA6
19	VDDIO	55	TRD3/SDDATA3/SQID3/RA7
20	No Connect	56	TRD1/SDDATA1/SQID1/RG12
21	VSS	57	VDDR1V8(5)
22	VSS	58	VDDR1V8(5)
23	EBID6/AN16/PMD6/RE6	59	VDDR1V8(5)
24	EBID7/AN15/PMD7/RE7	60	VDDR1V8(5)
25	AN25/RPE8/RE8	61	VDDR1V8(5)
26	AN26/RPE9/RE9	62	VDDR1V8(5)
27	TDO/AN31/RPF12/RF12	63	VDDR1V8(5)
28	TDI/AN17/SCK5/RF13	64	TRD0/SDDATA0/SQID0/RG13
29	VSS	65	TRD2/SDDATA2/SQID2/RG14
30	AN14/C1IND/SCK2/RG6	66	DDRVREF(6)
31	AN13/C1INC/RPG7/SDA4/RG7	67	VDDR1V8(5)
32	AN30/C2IND/RPG8/SCL4/RG8	68	VDDR1V8(5)
33	EBIA2/AN23/C2INC/RPG9/PMA2/RG9	69	EBIA6/RPE5/PMA6/RE5
34	AN21/RG15	70	SDCMD/SQICS0/RPD4/RD4
35	AN20/RH4	71	SQICS1/RPD5/RD5
36	EBID1/AN39/PMD1/RE1	72	VDDR1V8(5)

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is internally tied to VSS1V8 and should be connected to 1.8V ground externally.
5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
6: This pin is a 'No Connect' in devices without DDR.Add 0.1uF and 0.01uF capacitors in parallel between DDRVREF pin and ground, when DDRVREF is used.
7: These pins are restricted to input functions only.

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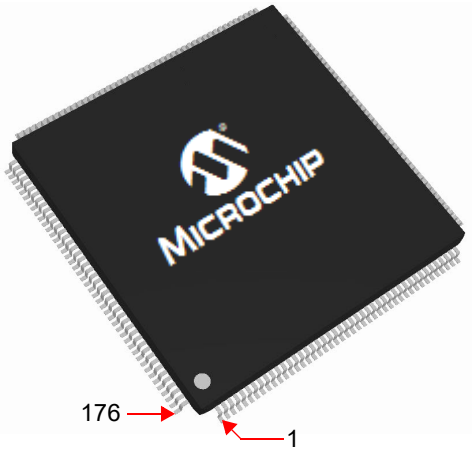
TABLE 5: PIN NAMES FOR 176-PIN DEVICES (CONTINUED)

176-PIN LQFP (TOP VIEW)

PIC32MZ1025DAK176
PIC32MZ1025DAL176
PIC32MZ1064DAK176
PIC32MZ1064DAL176
PIC32MZ2025DAK176
PIC32MZ2025DAL176
PIC32MZ2064DAK176
PIC32MZ2064DAL176
PIC32MZ1025DAR176
PIC32MZ1025DAS176
PIC32MZ1064DAR176
PIC32MZ1064DAS176
PIC32MZ2025DAR176
PIC32MZ2025DAS176
PIC32MZ2064DAR176
PIC32MZ2064DAS176



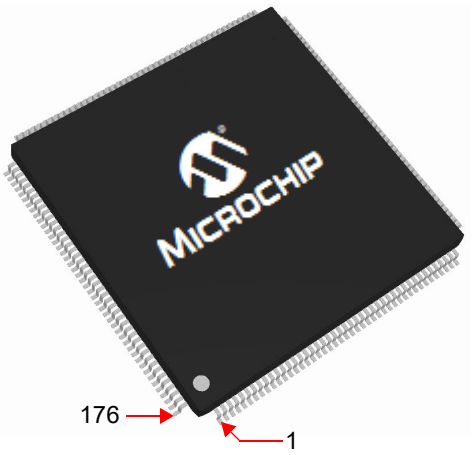
Pin Number	Full Pin Name	Pin Number	Full Pin Name
73	SCK1/RD1	109	ETXD3/RH1
74	GD10/EBIA14/RPD2/PMA14/PMCS1/RD2	110	ETXD2/RH0
75	GD11/EBIA15/RPD3/PMA15/PMCS2/RD3	111	ERXCLK/EREFCLK/RJ11
76	GD2/EBID15/RPD9/PMD15/RD9	112	ETXD1/RJ9
77	SCK4/RD10	113	ETXD0/RJ8
78	V_{DDR1V8}(5)	114	EMDIO/RJ1
79	RTCC/RPD0/RD0	115	V_{SS}
80	GD7/EBIA12/RPD12/PMA12/RD12	116	V_{DDCORE}
81	GD22/EBIA13/PMA13/RD13	117	V_{DDIO}
82	RPF8/SCL3/RF8	118	ETXERR/RJ0
83	V_{SS}	119	EMDC/RPD11/RD11
84	V_{DDCORE}	120	ETXCLK/RPD7/RD7
85	$\overline{MCLR}$	121	ETXEN/RPD6/RD6
86	V_{DDIO}	122	V_{SS}
87	V_{SS}	123	V_{SS}
88	No Connect	124	V_{DDIO}
89	GD16/EBID8/RPF5/SCL5/PMD8/RF5	125	RPA15/SDA1/RA15
90	GD5/EBIA10/RPF1/PMA10/RF1	126	RPA14/SCL1/RA14
91	GD6/EBIA11/RPF0/PMA11/RF0	127	GD1/EBID14/PMD14/RA4
92	GD21/EBIA23/RH15	128	EBIRDY1/SDA2/RA3
93	ERXERR/RPF3/RF3	129	SCL2/RA2
94	V_{SS}	130	GD19/EBIA21/RK7
95	GD4/EBIA9/RPG1/PMA9/RG1	131	GD15/EBIA20/RK6
96	GD3/EBIA8/RPG0/PMA8/RG0	132	GD14/EBIA19/RK5
97	GD17/EBID9/RPF4/SDA5/PMD9/RF4	133	GD13/EBIA18/RK4
98	EBID3/RPE3/PMD3/RE3	134	GD12/EBIA17/RK3
99	EBID2/PMD2/RE2	135	EBIA3/AN11/PMA3/RK2
100	ERXD1/RH5	136	EBIA1/AN38/PMA1/RK1
101	ERXD2/RH6	137	GD23/EBIA16/RK0
102	V_{DDIO}	138	EBIRDY2/AN37/RH11
103	V_{SS}	139	EBIA4/AN36/PMA4/RH7
104	ERXDV/ECRSDV/RH13	140	AN35/RH3
105	ECRS/RH12	141	$\overline{SDWP}$/EBIRP/RH2
106	ECOL/RH10	142	EBIA0/PMA0/RJ15
107	ERXD3/RH9	143	GD8/EBID11/PMD11/RJ14
108	ERXD0/RH8	144	GD0/EBID13/PMD13/RJ13

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is internally tied to V_{SS1V8} and should be connected to 1.8V ground externally.
5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
6: This pin is a 'No Connect' in devices without DDR.Add 0.1uF and 0.01uF capacitors in parallel between DDRVREF pin and ground, when DDRVREF is used.
7: These pins are restricted to input functions only.

TABLE 5: PIN NAMES FOR 176-PIN DEVICES (CONTINUED)

176-PIN LQFP (TOP VIEW)

PIC32MZ1025DAK176
PIC32MZ1025DAL176
PIC32MZ1064DAK176
PIC32MZ1064DAL176
PIC32MZ2025DAK176
PIC32MZ2025DAL176
PIC32MZ2064DAK176
PIC32MZ2064DAL176
PIC32MZ1025DAR176
PIC32MZ1025DAS176
PIC32MZ1064DAR176
PIC32MZ1064DAS176
PIC32MZ2025DAR176
PIC32MZ2025DAS176
PIC32MZ2064DAR176
PIC32MZ2064DAS176



Pin Number	Full Pin Name	Pin Number	Full Pin Name
145	GD9/EBIBS0/RJ12	161	SOSCO/RPC14(7)/T1CK/RC14(7)
146	GD18/EBIBS1/RJ10	162	SOSCI/RPC13(7)/RC13(7)
147	GEN/EBICS3/RJ7	163	OSC2/CLKO/RC15
148	GCLK/EBICS2/RJ6	164	OSC1/CLKI/RC12
149	HSYNC/EBICS1/RJ5	165	VDDIO
150	VSYNC/EBICS0/RJ4	166	VBAT
151	GD20/EBIA22/RJ3	167	AN45/RPB5/RB5
152	EBIRDY3/AN32/RJ2	168	AN5/RPB10/RB10
153	VSS	169	PGED1/AN0/RPB0/CTED2/RB0
154	VSS	170	PGED2/C1INA/AN46/RPB7/RB7
155	VDDIO	171	AN6/RB12
156	VDDIO	172	AN1/C2INB/RPB2/RB2
157	AN33/SCK6/RD15	173	EBIA7/AN47/HLVDIN/RPB9/PMA7/RB9
158	AN22/RPD14/RD14	174	EBIA5/AN7/PMA5/RA5
159	AN29/SCK3/RB14	175	AN2/C1INB/RB4
160	TCK/AN24/RA1	176	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 and Table 3 for the available peripherals and **12.4 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **12.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is internally tied to VSS1V8 and should be connected to 1.8V ground externally.
5: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.
6: This pin is a 'No Connect' in devices without DDR.Add 0.1uF and 0.01uF capacitors in parallel between DDRVREF pin and ground, when DDRVREF is used.
7: These pins are restricted to input functions only.

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 website: http://www.microchip.com/pic32.

- **Section 1. "Introduction"** (DS60001127)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 35. "Ethernet Controller"** (DS60001155)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)
- **Section 38. "High/Low Voltage Detect (HLVD)** (DS60001408)
- **Section 41. "Prefetch Module for Devices with L1 CPU Cache"** (DS60001183)
- **Section 42. "Oscillators with Enhanced PLL"** (DS60001250)
- **Section 46. "Serial Quad Interface (SQI)"** (DS60001244)
- **Section 47. "External Bus Interface (EBI)"** (DS60001245)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 51. "High-Speed USB with On-The-Go (OTG)"** (DS60001326)
- **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193)
- **Section 54. "Graphics LCD (GLCD) Controller"** (DS60001379)
- **Section 55. "DDR SDRAM Controller"** (DS60001321)
- **Section 57. "Secure Digital Host Controller (SDHC)"** (DS60001334)

NOTES:

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1.0 DEVICE OVERVIEW

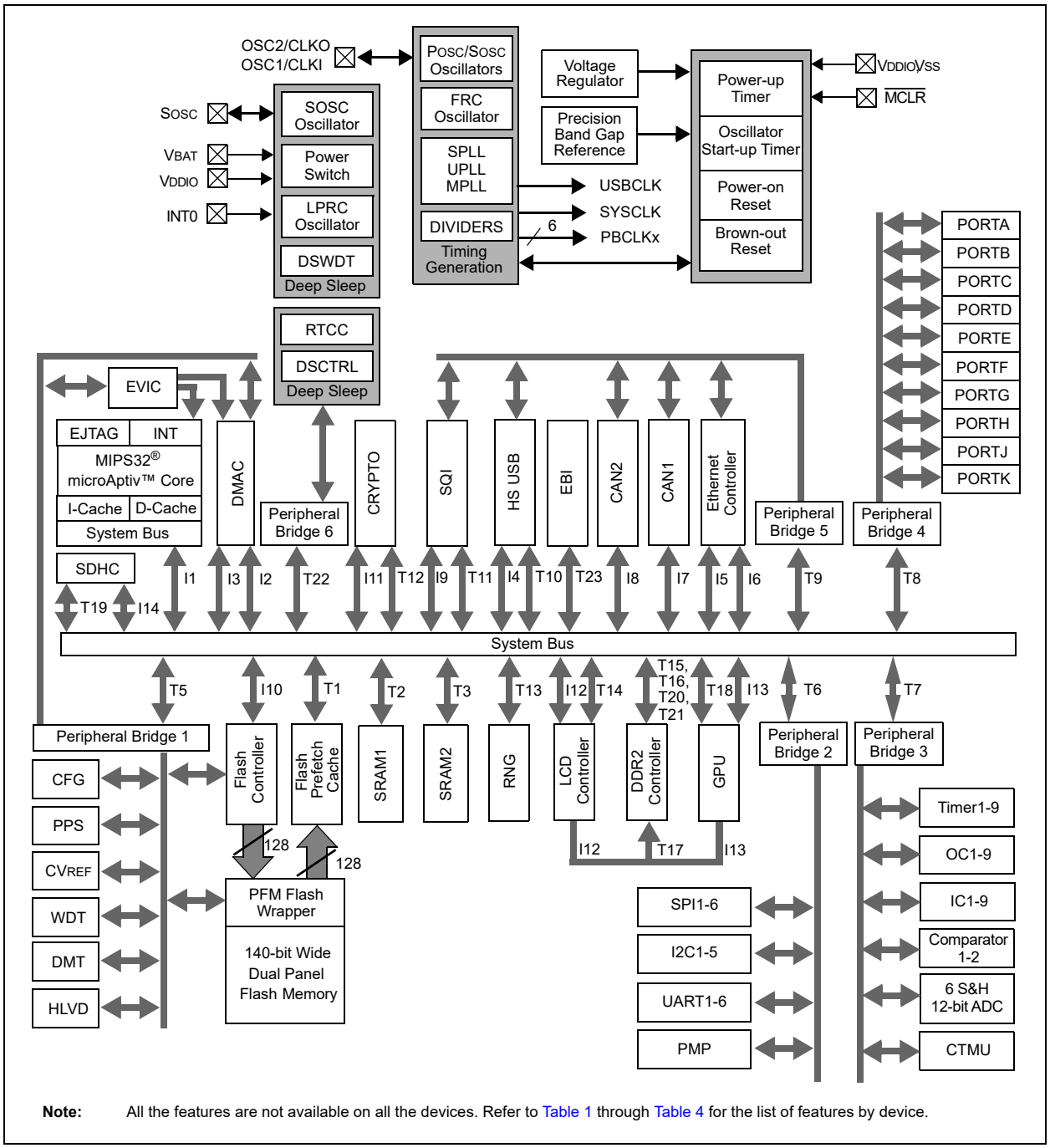
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

This data sheet contains device-specific information for the PIC32MZ DAK/DAL/DAR/DAS family of devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ DAK/DAL/DAR/DAS family of devices.

Table 1-1 through Table 1-23 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 4 through Table 7).

FIGURE 1-1: PIC32MZ DAK/DAL/DAR/DAS FAMILY BLOCK DIAGRAM



Note: All the features are not available on all the devices. Refer to Table 1 through Table 4 for the list of features by device.

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TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Analog-to-Digital Converter					
AN0	C12	169	I	Analog	Analog Input Channels
AN1	A13	172	I	Analog	
AN2	A12	175	I	Analog	
AN3	B10	7	I	Analog	
AN4	A9	10	I	Analog	
AN5	C11	168	I	Analog	
AN6	B13	171	I	Analog	
AN7	A11	174	I	Analog	
AN8	A10	8	I	Analog	
AN9	B9	11	I	Analog	
AN10	A8	14	I	Analog	
AN11	H11	135	I	Analog	
AN12	B7	17	I	Analog	
AN13	D5	31	I	Analog	
AN14	E5	30	I	Analog	
AN15	C7	24	I	Analog	
AN16	F6	23	I	Analog	
AN17	A6	28	I	Analog	
AN18	B3	43	I	Analog	
AN19	B8	16	I	Analog	
AN20	D4	35	I	Analog	
AN21	A5	34	I	Analog	
AN22	E9	158	I	Analog	
AN23	C5	33	I	Analog	
AN24	E11	160	I	Analog	
AN25	E6	25	I	Analog	
AN26	D6	26	I	Analog	
AN27	B11	1	I	Analog	
AN28	C10	2	I	Analog	
AN29	E10	159	I	Analog	
AN30	B5	32	I	Analog	
AN31	C6	27	I	Analog	
AN32	F10	152	I	Analog	
AN33	F11	157	I	Analog	
AN34	A7	15	I	Analog	
AN35	J13	140	I	Analog	
AN36	J12	139	I	Analog	
AN37	K13	138	I	Analog	
AN38	J11	136	I	Analog	
AN39	A4	36	I	Analog	
AN45	D11	167	I	Analog	
AN46	D12	170	I	Analog	
AN47	B12	173	I	Analog	
AN48	F7	9	I	Analog	
AN49	E7	12	I	Analog	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Oscillators					
CLKI	E12	164	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	E13	163	O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	E12	164	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	E13	163	O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	C13	162	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	D13	161	O	ST/CMOS	32.768 low-power oscillator crystal output. In external clock mode, SOSCO is the input. Secondary oscillator must be disabled in order to use the SOSCO as an input.
REFCLKI1	PPS	PPS	I	—	Reference Clock Generator Inputs 1-4
REFCLKI3	PPS	PPS	I	—	
REFCLKI4	PPS	PPS	I	—	
REFCLKO1	PPS	PPS	O	—	Reference Clock Generator Outputs 1-4
REFCLKO3	PPS	PPS	O	—	
REFCLKO4	PPS	PPS	O	—	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-3: IC1 THROUGH IC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Input Capture					
IC1	PPS	PPS	I	ST	Input Capture Inputs 1-9
IC2	PPS	PPS	I	ST	
IC3	PPS	PPS	I	ST	
IC4	PPS	PPS	I	ST	
IC5	PPS	PPS	I	ST	
IC6	PPS	PPS	I	ST	
IC7	PPS	PPS	I	ST	
IC8	PPS	PPS	I	ST	
IC9	PPS	PPS	I	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

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TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Output Compare					
OC1	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	O	—	
OC3	PPS	PPS	O	—	
OC4	PPS	PPS	O	—	
OC5	PPS	PPS	O	—	
OC6	PPS	PPS	O	—	
OC7	PPS	PPS	O	—	
OC8	PPS	PPS	O	—	
OC9	PPS	PPS	O	—	
OCFA	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
External Interrupts					
INT0	C3	42	I	ST	External Interrupt 0
INT1	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
PORTA					
RA0	D2	53	I/O	ST	PORTA is a bidirectional I/O port
RA1	E11	160	I/O	ST	
RA2	L12	129	I/O	ST	
RA3	N12	128	I/O	ST	
RA4	L11	127	I/O	ST	
RA5	A11	174	I/O	ST	
RA6	E4	54	I/O	ST	
RA7	D1	55	I/O	ST	
RA9	B11	1	I/O	ST	
RA10	C10	2	I/O	ST	
RA14	M11	126	I/O	ST	
RA15	N11	125	I/O	ST	
PORTB					
RB0	C12	169	I/O	ST	PORTB is a bidirectional I/O port
RB1	B9	11	I/O	ST	
RB2	A13	172	I/O	ST	
RB3	A10	8	I/O	ST	
RB4	A12	175	I/O	ST	
RB5	D11	167	I/O	ST	
RB6	D7	13	I/O	ST	
RB7	D12	170	I/O	ST	
RB8	A9	10	I/O	ST	
RB9	B12	173	I/O	ST	
RB10	C11	168	I/O	ST	
RB11	E7	12	I/O	ST	
RB12	B13	171	I/O	ST	
RB13	F7	9	I/O	ST	
RB14	E10	159	I/O	ST	
RB15	B10	7	I/O	ST	
PORTC					
RC1	B7	17	I/O	ST	PORTC is a bidirectional I/O port
RC2	A8	14	I/O	ST	
RC3	A7	15	I/O	ST	
RC4	B8	16	I/O	ST	
RC12	E12	164	I/O	ST	
RC13	C13	162	I	ST	
RC14	D13	161	I	ST	
RC15	E13	163	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

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TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
PORTD					
RD0	H3	79	I/O	ST	PORTD is a bidirectional I/O port
RD1	G1	73	I/O	ST	
RD2	G2	74	I/O	ST	
RD3	G3	75	I/O	ST	
RD4	F1	70	I/O	ST	
RD5	F2	71	I/O	ST	
RD6	K11	121	I/O	ST	
RD7	M10	120	I/O	ST	
RD9	H1	76	I/O	ST	
RD10	H2	77	I/O	ST	
RD11	N10	119	I/O	ST	
RD12	J1	80	I/O	ST	
RD13	J2	81	I/O	ST	
RD14	E9	158	I/O	ST	
RD15	F11	157	I/O	ST	
PORTE					
RE0	C4	40	I/O	ST	PORTE is a bidirectional I/O port
RE1	A4	36	I/O	ST	
RE2	N3	99	I/O	ST	
RE3	M3	98	I/O	ST	
RE4	B3	43	I/O	ST	
RE5	F3	69	I/O	ST	
RE6	F6	23	I/O	ST	
RE7	C7	24	I/O	ST	
RE8	E6	25	I/O	ST	
RE9	D6	26	I/O	ST	
PORTF					
RF0	L1	91	I/O	ST	PORTF is a bidirectional I/O port
RF1	K3	90	I/O	ST	
RF2	A3	41	I/O	ST	
RF3	M1	93	I/O	ST	
RF4	L3	97	I/O	ST	
RF5	K2	89	I/O	ST	
RF8	J3	82	I/O	ST	
RF12	C6	27	I/O	ST	
RF13	A6	28	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
PORTG					
RG0	N2	96	I/O	ST	PORTG is a bidirectional I/O port
RG1	M2	95	I/O	ST	
RG6	E5	30	I/O	ST	
RG7	D5	31	I/O	ST	
RG8	B5	32	I/O	ST	
RG9	C5	33	I/O	ST	
RG12	E3	56	I/O	ST	
RG13	E2	64	I/O	ST	
RG14	E1	65	I/O	ST	
RG15	A5	34	I/O	ST	
PORTH					
RH0	M8	110	I/O	ST	PORTH is a bidirectional I/O port
RH1	M7	109	I/O	ST	
RH2	H12	141	I/O	ST	
RH3	J13	140	I/O	ST	
RH4	D4	35	I/O	ST	
RH5	M4	100	I/O	ST	
RH6	N4	101	I/O	ST	
RH7	J12	139	I/O	ST	
RH8	N7	108	I/O	ST	
RH9	N6	107	I/O	ST	
RH10	M6	106	I/O	ST	
RH11	K13	138	I/O	ST	
RH12	N5	105	I/O	ST	
RH13	M5	104	I/O	ST	
RH14	C3	42	I/O	ST	
RH15	L2	92	I/O	ST	
PORTJ					
RJ0	L10	118	I/O	ST	PORTJ is a bidirectional I/O port
RJ1	K10	114	I/O	ST	
RJ2	F10	152	I/O	ST	
RJ3	E8	151	I/O	ST	
RJ4	F13	150	I/O	ST	
RJ5	F12	149	I/O	ST	
RJ6	G11	148	I/O	ST	
RJ7	G13	147	I/O	ST	
RJ8	N9	113	I/O	ST	
RJ9	M9	112	I/O	ST	
RJ10	F8	146	I/O	ST	
RJ11	N8	111	I/O	ST	
RJ12	F9	145	I/O	ST	
RJ13	G12	144	I/O	ST	
RJ14	G10	143	I/O	ST	
RJ15	H13	142	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

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TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
PORTK					
RK0	K12	137	I/O	ST	PORTK is a bidirectional I/O port
RK1	J11	136	I/O	ST	
RK2	H11	135	I/O	ST	
RK3	L13	134	I/O	ST	
RK4	H10	133	I/O	ST	
RK5	J10	132	I/O	ST	
RK6	M13	131	I/O	ST	
RK7	M12	130	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-7: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Timer1 through Timer9					
T1CK	D13	161	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar					
RTCC(1)	H3	79	O	—	Real-Time Clock Alarm/Seconds Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: The RTCC pin function in not available during VBAT operation.

TABLE 1-8: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Universal Asynchronous Receiver Transmitter 1					
U1RX	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	O	—	UART1 Transmit
$\overline{\text{U1CTS}}$	PPS	PPS	I	ST	UART1 Clear to Send
$\overline{\text{U1RTS}}$	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2					
U2RX	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	O	—	UART2 Transmit
$\overline{\text{U2CTS}}$	PPS	PPS	I	ST	UART2 Clear To Send
$\overline{\text{U2RTS}}$	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3					
U3RX	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	O	—	UART3 Transmit
$\overline{\text{U3CTS}}$	PPS	PPS	I	ST	UART3 Clear to Send
$\overline{\text{U3RTS}}$	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4					
U4RX	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	O	—	UART4 Transmit
$\overline{\text{U4CTS}}$	PPS	PPS	I	ST	UART4 Clear to Send
$\overline{\text{U4RTS}}$	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5					
U5RX	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	O	—	UART5 Transmit
$\overline{\text{U5CTS}}$	PPS	PPS	I	ST	UART5 Clear to Send
$\overline{\text{U5RTS}}$	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6					
U6RX	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	O	—	UART6 Transmit
$\overline{\text{U6CTS}}$	PPS	PPS	I	ST	UART6 Clear to Send
$\overline{\text{U6RTS}}$	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

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TABLE 1-9: SPI1 THROUGH SPI 6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Serial Peripheral Interface 1					
SCK1	G1	73	I/O	ST	SPI1 Synchronous Serial Clock Input/Output
SDI1	PPS	PPS	I	ST	SPI1 Data In
SDO1	PPS	PPS	O	—	SPI1 Data Out
$\overline{SS1}$	PPS	PPS	I/O	ST	SPI1 Select Or Frame Pulse I/O
Serial Peripheral Interface 2					
SCK2	E5	30	I/O	ST	SPI2 Synchronous Serial Clock Input/output
SDI2	PPS	PPS	I	ST	SPI2 Data In
SDO2	PPS	PPS	O	—	SPI2 Data Out
$\overline{SS2}$	PPS	PPS	I/O	ST	SPI2 Select Or Frame Pulse I/O
Serial Peripheral Interface 3					
SCK3	E10	159	I/O	ST	SPI3 Synchronous Serial Clock Input/Output
SDI3	PPS	PPS	I	ST	SPI3 Data In
SDO3	PPS	PPS	O	—	SPI3 Data Out
$\overline{SS3}$	PPS	PPS	I/O	ST	SPI3 Select Or Frame Pulse I/O
Serial Peripheral Interface 4					
SCK4	H2	77	I/O	ST	SPI4 Synchronous Serial Clock Input/Output
SDI4	PPS	PPS	I	ST	SPI4 Data In
SDO4	PPS	PPS	O	—	SPI4 Data Out
$\overline{SS4}$	PPS	PPS	I/O	ST	SPI4 Select Or Frame Pulse I/O
Serial Peripheral Interface 5					
SCK5	A6	28	I/O	ST	SPI5 Synchronous Serial Clock Input/Output
SDI5	PPS	PPS	I	ST	SPI5 Data In
SDO5	PPS	PPS	O	—	SPI5 Data Out
$\overline{SS5}$	PPS	PPS	I/O	ST	SPI5 Select Or Frame Pulse I/O
Serial Peripheral Interface 6					
SCK6	F11	157	I/O	ST	SPI6 Synchronous Serial Clock Input/Output
SDI6	PPS	PPS	I	ST	SPI6 Data In
SDO6	PPS	PPS	O	—	SPI6 Data Out
$\overline{SS6}$	PPS	PPS	I/O	ST	SPI6 Select Or Frame Pulse I/O

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-10: I2C1 THROUGH I2C5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Inter-Integrated Circuit 1					
SCL1	M11	126	I/O	ST	I2C1 Synchronous Serial Clock Input/Output
SDA1	N11	125	I/O	ST	I2C1 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 2					
SCL2	L12	129	I/O	ST	I2C2 Synchronous Serial Clock Input/Output
SDA2	N12	128	I/O	ST	I2C2 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 3					
SCL3	J3	82	I/O	ST	I2C3 Synchronous Serial Clock Input/Output
SDA3	A3	41	I/O	ST	I2C3 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 4					
SCL4	B5	32	I/O	ST	I2C4 Synchronous Serial Clock Input/Output
SDA4	D5	31	I/O	ST	I2C4 Synchronous Serial Data Input/Output
Inter-Integrated Circuit 5					
SCL5	K2	89	I/O	ST	I2C5 Synchronous Serial Clock Input/Output
SDA5	L3	97	I/O	ST	I2C5 Synchronous Serial Data Input/Output

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-11: COMPARATOR 1, COMPARATOR 2 AND CVREF PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Comparator Voltage Reference					
CVREF+	C10	2	I	Analog	Comparator Voltage Reference (High) Input
CVREF-	B11	1	I	Analog	Comparator Voltage Reference (Low) Input
CVREFOUT	C11	168	O	Analog	Comparator Voltage Reference Output
Comparator 1					
C1INA	D12	170	I	Analog	Comparator 1 Positive Input
C1INB	A12	176	I	Analog	Comparator 1 Selectable Negative Input
C1INC	D5	31	I	Analog	
C1IND	E5	30	I	Analog	
C1OUT	PPS	PPS	O	—	Comparator 1 Output
Comparator 2					
C2INA	B10	7	I	Analog	Comparator 2 Positive Input
C2INB	A13	172	I	Analog	Comparator 2 Selectable Negative Input
C2INC	C5	33	I	Analog	
C2IND	B5	32	I	Analog	
C2OUT	PPS	PPS	O	—	Comparator 2 Output

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

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TABLE 1-12: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
P M P					
PMA0	H13	142	I/O	TTL/ST	PMP Address bit 0 Input (Buffered Client modes) and Output (Host modes)
PMA1	J11	136	I/O	TTL/ST	PMP Address bit 1 Input (Buffered Client modes) and Output (Host modes)
PMA2	C5	33	O	—	PMP Address (Demultiplexed Host modes)
PMA3	H11	135	O	—	
PMA4	J12	139	O	—	
PMA5	A11	174	O	—	
PMA6	F3	69	O	—	
PMA7	B12	173	O	—	
PMA8	N2	96	O	—	
PMA9	M2	95	O	—	
PMA10	K3	90	O	—	
PMA11	L1	91	O	—	
PMA12	J1	80	O	—	
PMA13	J2	81	O	—	
PMA14	G2	74	O	—	
PMA15	G3	75	O	—	
PMCS1	G2	74	O	—	PMP Chip Select 1 Strobe
PMCS2	G3	75	O	—	PMP Chip Select 2 Strobe
PMD0	C4	40	I/O	TTL/ST	PMP Data (Demultiplexed Host mode) or Address/Data (Multiplexed Host modes)
PMD1	A4	36	I/O	TTL/ST	
PMD2	N3	99	I/O	TTL/ST	
PMD3	M3	98	I/O	TTL/ST	
PMD4	B3	43	I/O	TTL/ST	
PMD5	B7	17	I/O	TTL/ST	
PMD6	F6	23	I/O	TTL/ST	
PMD7	C7	24	I/O	TTL/ST	
PMD8	K2	89	I/O	TTL/ST	
PMD9	L3	97	I/O	TTL/ST	
PMD10	A9	10	I/O	TTL/ST	
PMD11	G10	143	I/O	TTL/ST	
PMD12	A8	14	I/O	TTL/ST	
PMD13	G12	144	I/O	TTL/ST	
PMD14	L11	127	I/O	TTL/ST	
PMD15	H1	76	I/O	TTL/ST	
PMALL	H13	142	O	—	PMP Address Latch Enable Low Byte (Multiplexed Host modes)
PMALH	J11	136	O	—	PMP Address Latch Enable High Byte (Multiplexed Host modes)
PMRD	B8	16	O	—	PMP Read Strobe
PMWR	A7	15	O	—	PMP Write Strobe

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

TABLE 1-13: EBI PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
External Bus Interface					
EBIA0	H13	142	O	—	External Bus Interface Address Bus
EBIA1	J11	136	O	—	
EBIA2	C5	33	O	—	
EBIA3	H11	135	O	—	
EBIA4	J12	139	O	—	
EBIA5	A11	174	O	—	
EBIA6	F3	69	O	—	
EBIA7	B12	173	O	—	
EBIA8	N2	96	O	—	
EBIA9	M2	95	O	—	
EBIA10	K3	90	O	—	
EBIA11	L1	91	O	—	
EBIA12	J1	80	O	—	
EBIA13	J2	81	O	—	
EBIA14	G2	74	O	—	
EBIA15	G3	75	O	—	
EBIA16	K12	137	O	—	
EBIA17	L13	134	O	—	
EBIA18	H10	133	O	—	
EBIA19	J10	132	O	—	
EBIA20	M13	131	O	—	
EBIA21	M12	130	O	—	
EBIA22	E8	151	O	—	
EBIA23	L2	92	O	—	
EBID0	C4	40	I/O	ST	External Bus Interface Data I/O Bus
EBID1	A4	36	I/O	ST	
EBID2	N3	99	I/O	ST	
EBID3	M3	98	I/O	ST	
EBID4	B3	43	I/O	ST	
EBID5	B7	17	I/O	ST	
EBID6	F6	23	I/O	ST	
EBID7	C7	24	I/O	ST	
EBID8	K2	89	I/O	ST	
EBID9	L3	97	I/O	ST	
EBID10	A9	10	I/O	ST	
EBID11	G10	143	I/O	ST	
EBID12	A8	14	I/O	ST	
EBID13	G12	144	I/O	ST	
EBID14	L11	127	I/O	ST	
EBID15	H1	76	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

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TABLE 1-13: EBI PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
$\overline{\text{EBIBS0}}$	J11	145	O	—	External Bus Interface Byte Select
$\overline{\text{EBIBS1}}$	J12	146	O	—	
$\overline{\text{EBICS0}}$	G10	150	O	—	External Bus Interface Chip Select
$\overline{\text{EBICS1}}$	H12	149	O	—	
$\overline{\text{EBICS2}}$	H11	148	O	—	
$\overline{\text{EBICS3}}$	H10	147	O	—	
$\overline{\text{EBIOE}}$	B8	16	O	—	External Bus Interface Output Enable
EBIRDY1	M10	128	I	ST	External Bus Interface Ready Input
EBIRDY2	C5	138	I	ST	
EBIRDY3	C4	152	I	ST	
$\overline{\text{EBIRP}}$	F1	141	O	—	External Bus Interface Flash Reset Pin
$\overline{\text{EBIWE}}$	A7	15	O	—	External Bus Interface Write Enable

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-14: USB PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Universal Serial Bus					
VBUS	A2	45	I	Analog	USB bus power monitor
VUSB3V3	B2	46, 47	P	—	USB internal transceiver supply. If the USB module is not used, this pin must be connected to VSS.
D+	C1	51	I/O	Analog	USB D+
D-	B1	50	I/O	Analog	USB D-
USBID	D3	52	I	ST	USB OTG ID detect

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-15: CAN1 AND CAN2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Controller Area Network					
C1TX	PPS	PPS	O	—	CAN1 Bus Transmit Pin
C1RX	PPS	PPS	I	ST	CAN1 Bus Receive Pin
C2TX	PPS	PPS	O	—	CAN2 Bus Transmit Pin
C2RX	PPS	PPS	I	ST	CAN2 Bus Receive Pin

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-16: ETHERNET MII I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Ethernet					
ERXD0	N7	108	I	ST	Ethernet Receive Data 0
ERXD1	M4	100	I	ST	Ethernet Receive Data 1
ERXD2	N4	101	I	ST	Ethernet Receive Data 2
ERXD3	N6	107	I	ST	Ethernet Receive Data 3
ERXERR	M1	93	I	ST	Ethernet Receive Error Input
ERXDV	M5	104	I	ST	Ethernet Receive Data Valid
ERXCLK	N8	111	I	ST	Ethernet Receive Clock
ETXD0	N9	113	O	—	Ethernet Transmit Data 0
ETXD1	M9	112	O	—	Ethernet Transmit Data 1
ETXD2	M8	110	O	—	Ethernet Transmit Data 2
ETXD3	M7	109	O	—	Ethernet Transmit Data 3
ETXERR	L10	118	O	—	Ethernet Transmit Error
ETXEN	K11	121	O	—	Ethernet Transmit Enable
ETXCLK	M10	120	I	ST	Ethernet Transmit Clock
ECOL	M6	106	I	ST	Ethernet Collision Detect
ECRS	N5	105	I	ST	Ethernet Carrier Sense
EMDC	N10	119	O	—	Ethernet Management Data Clock
EMDIO	K10	114	I/O	—	Ethernet Management Data

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-17: ETHERNET RMII PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Ethernet MII Interface					
ERXD0	N7	108	I	ST	Ethernet Receive Data 0
ERXD1	M4	100	I	ST	Ethernet Receive Data 1
ERXERR	M1	93	I	ST	Ethernet Receive Error Input
ETXD0	N9	113	O	—	Ethernet Transmit Data 0
ETXD1	M9	112	O	—	Ethernet Transmit Data 1
ETXEN	K11	121	O	—	Ethernet Transmit Enable
EMDC	N10	119	O	—	Ethernet Management Data Clock
EMDIO	K10	114	I/O	—	Ethernet Management Data
EREFCLK	N8	111	I	ST	Ethernet Reference Clock
ECRSDV	M5	104	I	ST	Ethernet Carrier Sense Data Valid

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

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TABLE 1-18: SQI1 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Serial Quad Interface					
SQICLK	E4	54	O	—	Serial Quad Interface Clock
$\overline{\text{SQICS0}}$	F1	70	O	—	Serial Quad Interface Chip Select 0
$\overline{\text{SQICS1}}$	F2	71	O	—	Serial Quad Interface Chip Select 1
SQID0	E2	64	I/O	ST	Serial Quad Interface Data 0
SQID1	E3	56	I/O	ST	Serial Quad Interface Data 1
SQID2	E1	65	I/O	ST	Serial Quad Interface Data 2
SQID3	D1	55	I/O	ST	Serial Quad Interface Data 3

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-19: SDHC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
SDHC					
SDCK	E4	54	O	—	SD Serial Clock
SDCMD	F1	70	O	—	SD Command/Response
SDDATA0	E2	64	I/O	ST	SD Serial Data 0
SDDATA1	E3	56	I/O	ST	SD Serial Data 1
SDDATA2	E1	65	I/O	ST	SD Serial Data 2
SDDATA3	D1	55	I/O	ST	SD Serial Data 3/Card Detect
$\overline{\text{SDCD}}$	D2	53	I	ST	SD Mechanical Card Detect
$\overline{\text{SDWP}}$	H12	141	I	ST	SD Write Protect

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-20: CTMU PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Charge Time Measurement Unit					
CTED1	B9	11	I	ST	CTMU External Edge Input 1
CTED2	C12	169	I	ST	CTMU External Edge Input 2
CTPLS	F7	9	O	—	CTMU Output Pulse

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-21: GRAPHICS LCD (GLCD) CONTROLLER PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
GLCD Controller					
GCLK	G11	148	O	—	Graphics Display Pixel Clock
HSYNC	F12	149	O	—	Graphics Display Horizontal Sync Pulse
VSYNC	F13	150	O	—	Graphics Display Vertical Sync Pulse
GEN	G13	147	O	—	Graphics Display Enable Output
GD0	G12	144	O	—	Graphics Controller Data Output
GD1	L11	127	O	—	
GD2	H1	76	O	—	
GD3	N2	96	O	—	
GD4	M2	95	O	—	
GD5	K3	90	O	—	
GD6	L1	91	O	—	
GD7	J1	80	O	—	
GD8	G10	143	O	—	
GD9	F9	145	O	—	
GD10	G2	74	O	—	
GD11	G3	75	O	—	
GD12	L13	134	O	—	
GD13	H10	133	O	—	
GD14	J10	132	O	—	
GD15	M13	131	O	—	
GD16	K2	89	O	—	
GD17	L3	97	O	—	
GD18	F8	146	O	—	
GD19	M12	130	O	—	
GD20	E8	151	O	—	
GD21	L2	92	O	—	
GD22	J2	81	O	—	
GD23	K12	137	O	—	

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

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TABLE 1-22: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
Power and Ground					
AVDD	D9	3, 4	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	C8, D8	5, 6	P	P	Ground reference for analog modules. This pin must be connected at all times.
VDDIO	B6, G9, H9, J9, K9, L6, L7, L9	19, 38, 86, 102, 117, 124, 155, 156, 165	P	—	Positive supply for peripheral logic and I/O pins. This pin must be connected at all times.
VDDCORE	B4, C9, L8, N1	18, 39, 84, 116	P	—	1.8V positive supply for core logic. This pin must be connected at all times.
VSS	C2, F5, G5, G6, G7, G8, H7, H8, J7, J8, K7, K8	21, 22, 29, 37, 48, 49, 83, 87, 94, 103, 115, 122, 123, 153, 154	P	—	Ground reference for logic, I/O pins, and USB. This pin must be connected at all times.
HLVDIN	B12	173	P	—	Low-voltage detect pin.
VBAT	D10	166	P	—	Positive supply for the battery backed section. It is recommended to connect this pin to VDDIO if VBAT mode is not used (i.e., not connected to the battery).
VDDR1V8	H5, H6, J5, J6, K5, K6 (**Note 2**)	57, 58, 59, 60, 61, 62, 63, 67, 68, 72, 78 (**Note 2**)	P	—	Positive supply for the DDR2 SDRAM memory.
VSS1V8	G4, H4, J4, K4, L4, L5	See **Note 1**	P	—	Ground reference for DDR2 SDRAM memory.
Voltage Reference					
DDRVREF	F4 (**Note 3**)	66 (**Note 3**)	P	—	Voltage Reference to DDR2 SDRAM memory.
VREF+	C10	2	I	Analog	Analog Voltage Reference (High) Input
VREF-	B11	1	I	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: The metal plane at the bottom of the device is internally tied to VSS1V8, and it must be connected to 1.8V ground externally.

2: This pin must be tied to Vss through a 20k Ω resistor in devices without DDR.

3: This pin is a 'No Connect' in devices without DDR. Add 0.1uF and 0.01uF capacitors in parallel between DDRVREF pin and ground, when DDRVREF is used. When external reference is selected, DDRVREF can be provided by dividing VDDR1V8 by 1K ohm +/-1% resistor divider.

TABLE 1-23: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	169-pin LFBGA	176-pin LQFP			
JTAG					
TCK	E11	160	I	ST	JTAG Test Clock Input Pin
TDI	A6	28	I	ST	JTAG Test Data Input Pin
TDO	C6	27	O	—	JTAG Test Data Output Pin
TMS	D2	53	I	ST	JTAG Test Mode Select Pin
Trace					
TRCLK	E4	54	O	—	Trace Clock
TRD0	E2	64	O	—	Trace Data bits 0-3
TRD1	E3	56	O	—	
TRD2	E1	65	O	—	
TRD3	D1	55	O	—	
Programming/Debugging					
PGED1	C12	169	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	B9	11	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	D12	170	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	D7	13	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
$\overline{\text{MCLR}}$	K1	85	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS-compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = Transistor-transistor Logic input buffer; Analog = Analog input; O = Output; PPS = Peripheral Pin Select; P = Power; I = Input

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2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Getting started with the PIC32MZ DAK/DAL/DAR/DAS family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDDIO, VDDCORE, and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- VBAT pin (see **2.2 "Decoupling Capacitors"**)
- All VDDR1V8 and VSS1V8 pins (see **2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **2.3 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.4 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **2.7 "External Oscillator Pins"**)

The following pins may be required:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

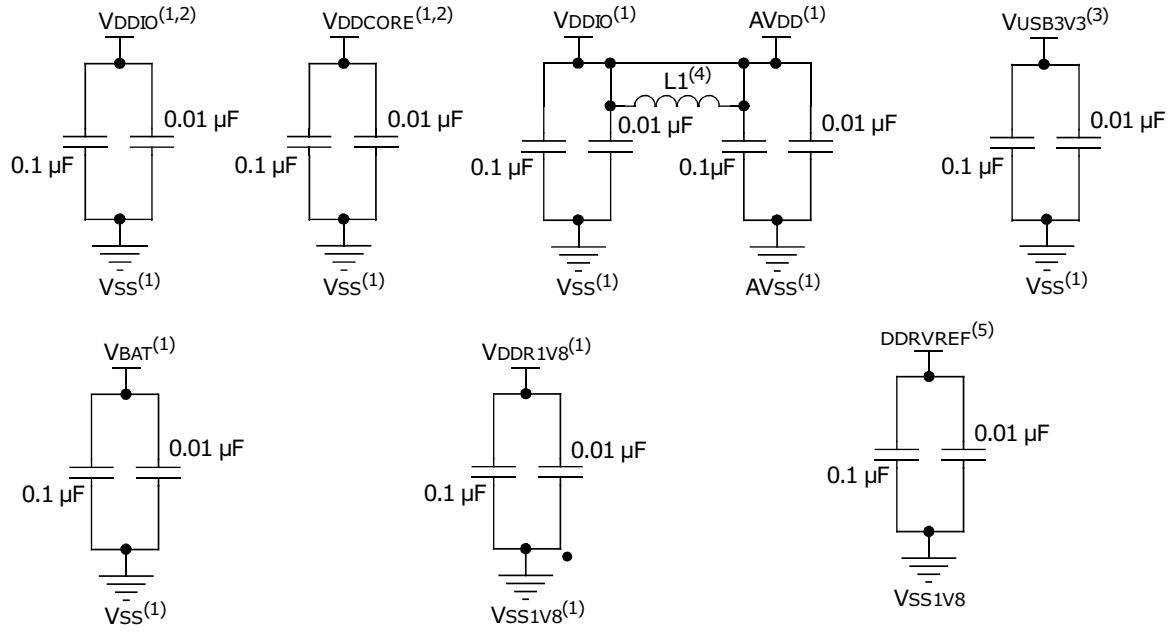
2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDDIO, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** It is recommended that two parallel capacitors with a value of 0.1 µF (100 nF, 10-20V) and a value of 0.01 µF be used. The 0.1 µF capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. Place both capacitors in close proximity and consider implementing the pair of capacitances as close to the power and ground pins as possible. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: There are multiple power and ground pairs and minimum connection rules which apply for each power pin (i.e., VDDIO, VDDCORE, AVDD, VUSB3V3, VBAT, VDDR1V8) and each ground pin (VSS, AVSS, VSS1V8).

2: Voltage on VDDIO must always be greater than or equal to VDDCORE during power-up.

3: If the USB module is not used, this pin must be connected to VSS.

4: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDDIO and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

5: This pin is a no connect in devices without DDR.

Where:

$$f = \frac{F_{CNV}}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 BULK CAPACITORS

The use of a bulk capacitor on VDDIO and VDDCORE is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

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2.3 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides for two specific device functions:

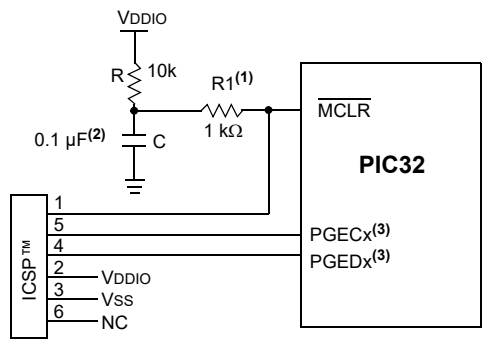
- Device Reset
- Device programming and debugging

Pulling The $\overline{\text{MCLR}}$ pin low generates a device Reset. Figure 2-2 illustrates a typical $\overline{\text{MCLR}}$ circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{\text{MCLR}}$ pin.

FIGURE 2-2: EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS



Note 1: 470W ≤ R1 ≤ 1KΩ will limit any current flowing into $\overline{\text{MCLR}}$ from the external capacitor C, in the event of $\overline{\text{MCLR}}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{\text{MCLR}}$ pin V_{IH} and V_{IL} specifications are met without interfering with the Debug/Programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

2.4 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For additional information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available for download from the Microchip web site, www.microchip.com:

- *“Using MPLAB® ICD 3”* (poster) (DS50001765)
- *“MPLAB® ICD 3 Design Advisory”* (DS50001764)
- *“MPLAB® REAL ICE™ In-Circuit Debugger User’s Guide”* (DS50001616)
- *“Using MPLAB® REAL ICE™ Emulator”* (poster) (DS50001749)

2.5 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer or debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

2.6 Trace

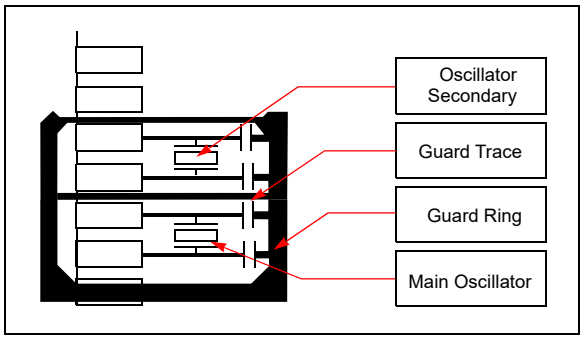
The trace pins can be connected to a hardware trace-enabled programmer to provide a compressed real-time instruction trace. When used for trace, the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for additional information).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.7.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_pin capacitance = 4 pF
- COUT = PIC32_OSC1_pin capacitance = 4 pF
- PCB stray capacitance (i.e., 12 mm length) = 2.5 pF
- C1 and C2 are the loading capacitors to use on your Crystal circuit design to guarantee that the effective capacitance as seen by the crystal in circuit meets the crystal manufacturer specification.

From the Crystal manufacturer CLOAD spec:

CLOAD = {([Cin + C1] * [COUT + C2]) / [Cin + C1 + C2 + COUT] } + oscillator PCB stray capacitance

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION

Crystal manufacturer data sheet spec example: CLOAD = 15 pF

Therefore:

MFG CLOAD = {([CIN + C1] * [COUT + C2]) / [CIN + C1 + C2 + COUT] }
+ estimated oscillator PCB stray capacitance

Assuming C1 = C2 and PIC32 Cin = Cout, the formula can be further simplified and restated to solve for C1 and C2 by:

C1 = C2 = ((2 * MFG Cload spec) - Cin - (2 * PCB capacitance))
= ((2 * 15) - 4 - (2 * 2.5 pF))
= (30 - 4 - 5)
= 21 pF

Therefore:

C1 = C2 = 21 pF is the correct loading capacitors to use on your crystal circuit design to guarantee that the effective capacitance as seen by the crystal in circuit in this example is 15 pF to meet the crystal.

Note: Do not add excessive gain such that the oscillator signal is clipped flat on top of the sine wave. If your oscillator signal is clipped, reduce the gain or add a series resistor (RS) as shown in the "Circuit A" of the Figure 2-4. Failure to do so will stress and reduce the lifetime of the crystal, which might result in a premature failure. When measuring the oscillator signal, the user must use an active-powered scope probe with ≤ 1 pF or the scope probe itself will unduly change the gain and Peak-to-Peak oscillator signal levels.

2.7.1.1 Additional Microchip References

- AN588 *"PICmicro® Microcontroller Oscillator Design Guide"*
- AN826 *"Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- AN849 *"Basic PICmicro® Oscillator Design"*

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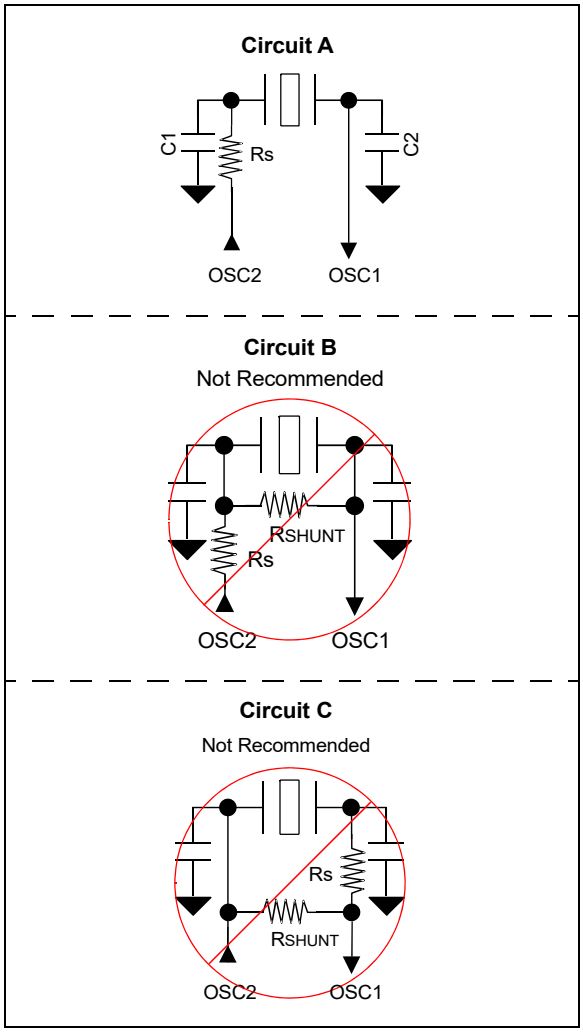
FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS



Note: For recommended resistor values versus crystal/frequency, Refer to the *"PIC32MK GP/MC Family Silicon Errata and Data Sheet Clarification"* (DS80000737) document, which is available for download from the Microchip website (www.microchip.com).

2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to VSS through a 1k to 10k resistor and configuring the pin as an input.

2.9 Considerations When Interfacing to Remotely Powered Circuits

2.9.1 NON-5V TOLERANT INPUT PINS

A quick review of the absolute maximum rating section in **44.0 "Electrical Characteristics"** indicates that the voltage on any non-5v tolerant pin should not exceed VDD + 0.3V, unless the input current is limited to meet the respective injection current specifications defined by the parameters DI60a, DI60b, and DI60c as shown in Table 44-12.

Figure 2-5 illustrates a remote circuit using an independent power source, which is powered while connected to a PIC32 non-5V tolerant circuit that is not powered.

Without a proper signal isolation on non-5V tolerant pins, the remote signal can power the PIC32 device through the high side ESD protection diodes. Besides violating the absolute maximum rating specification when VDD of the PIC32 device is restored and ramping up or ramping down, it can also negatively affect the internal Power-on Reset (POR) and Brown-out Reset (BOR) circuits, which can lead to improper initialization of internal PIC32 logic circuits. In these cases, it is recommended to implement digital or analog signal isolation as shown in Figure 2-6. This is indicative of all industry microcontrollers and not just Microchip products.

FIGURE 2-5: PIC32 NON-5V TOLERANT CIRCUIT EXAMPLE

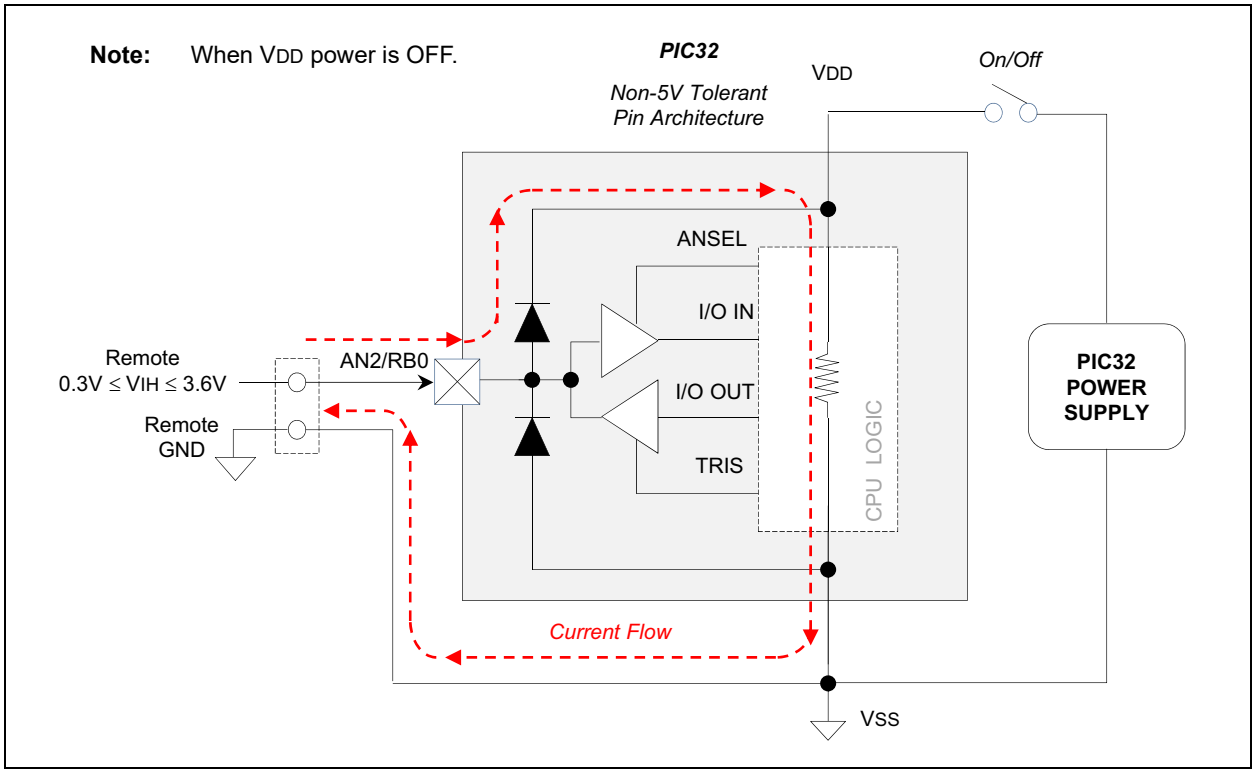


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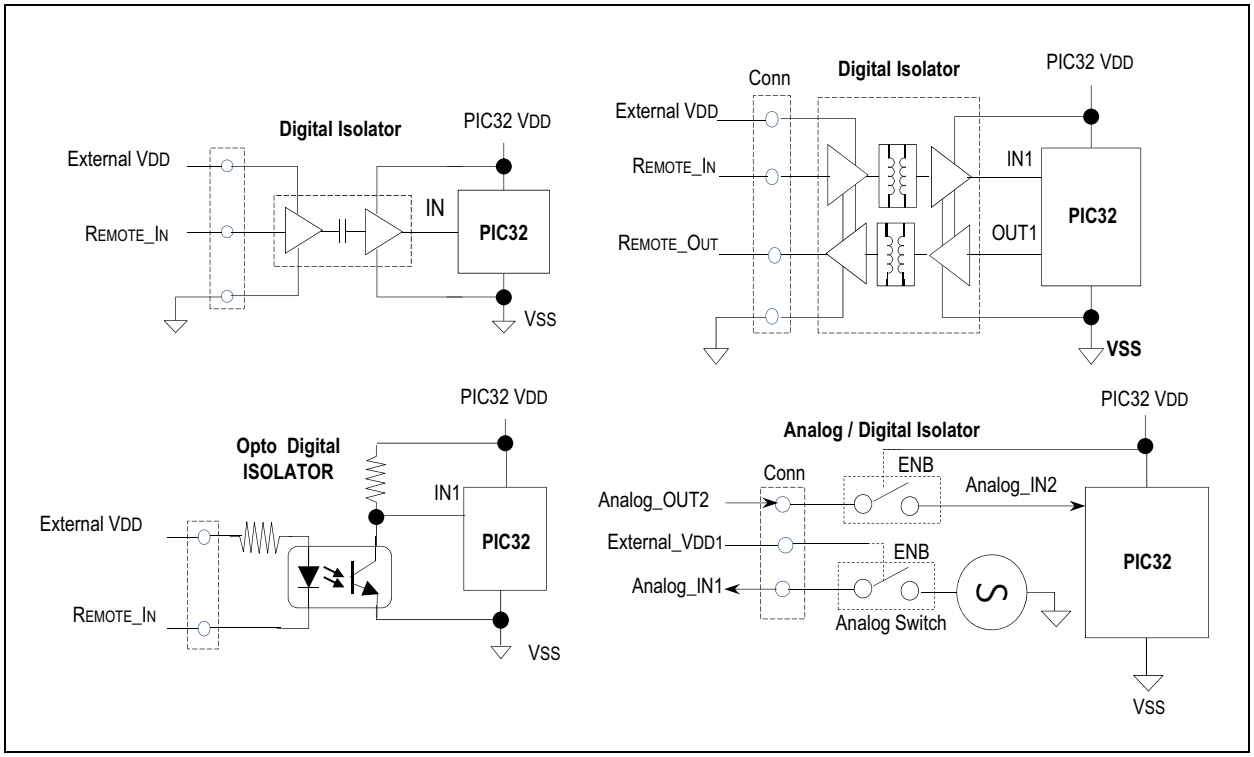
TABLE 2-1: EXAMPLES OF DIGITAL/ ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION

Example Digital/Analog Signal Isolation Circuits	Inductive Coupling	Capacitive Coupling	Opto Coupling	Analog/Digital Switch
ADuM7241 / 40 ARZ (1 Mbps)	X	—	—	—
ADuM7241 / 40 CRZ (25 Mbps)	X	—	—	—
ISO721	—	X	—	—
LTV-829S (2-Channel)	—	—	X	—
LTV-849S (4-Channel)	—	—	X	—
FSA266 / NC7WB66	—	—	—	X

FIGURE 2-6: EXAMPLE DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS

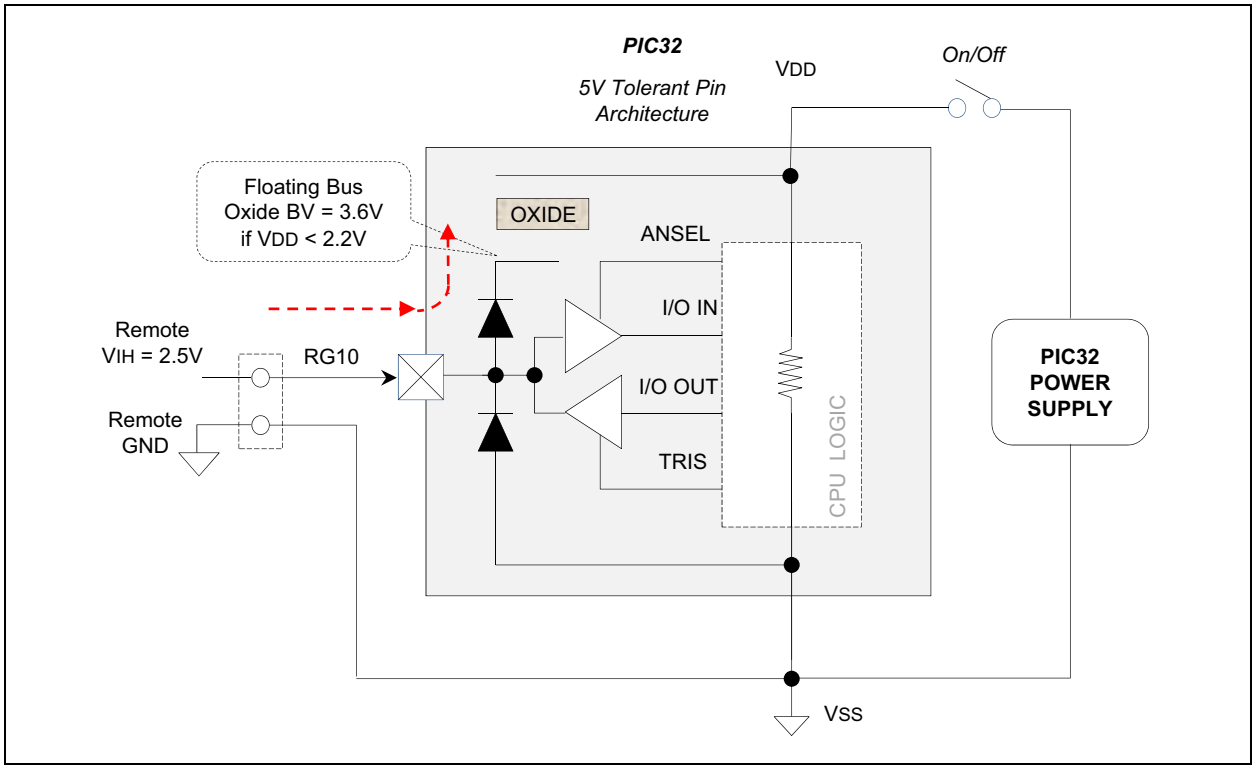


2.9.2 5V TOLERANT INPUT PINS

The internal high side diode on 5V tolerant pins are bussed to an internal floating node, rather than being connected to VDDIO, as shown in Figure 2-7. The voltage on these pins, if VDDIO < 2.2V (usually during power up/down), should not exceed 3.2V relative to VSS of the PIC32 device. The voltage of 3.6V or higher (when VDDIO < 2.2V) will violate the absolute maximum specification and will stress the oxide layer separating the high side floating node, which impacts device reliability.

If a remotely powered "digital-only" signal can be guaranteed to be ≤ 3.2V relative to Vss on the PIC32 device side, a 5V tolerant pin can be used without the need for a digital isolator. This is assuming there is no ground loop issue, that is, the logic ground of the two circuits are not at the same absolute level, and remote logic low input is not less than VSS - 0.3V. Once VDDIO is >2.2V, the pin can be operated up to 5.5V.

FIGURE 2-7: PIC32 5V TOLERANT PIN ARCHITECTURE EXAMPLE



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2.10 Designing for High-Speed Peripherals

The PIC32MZ DAK/DAL/DAR/DAS family devices have peripherals that operate at frequencies much higher than typical for an embedded environment. Table 2-2 lists the peripherals that produce high-speed signals on their external pins:

TABLE 2-2: PERIPHERALS THAT PRODUCE HS SIGNALS ON EXTERNAL PINS

Peripheral	High-Speed Signal Pins	Maximum Speed on Signal Pin
EBI	EBIAx, EBIDx	50 MHz
HS USB	D+, D-	480 MHz
SDHC	SDCK, DATAx	50 MHz
SQI	SQICLK, SQIDx	76 MHz

Due to these high-speed signals, it is important to consider several factors when designing a product that uses these peripherals, as well as the PCB on which these components will be placed. Adhering to these recommendations will help achieve the following goals:

- Minimize the effects of electromagnetic interference to the proper operation of the product
- Ensure signals arrive at their intended destination at the same time
- Minimize crosstalk
- Maintain signal integrity
- Reduce system noise
- Minimize ground bounce and power sag

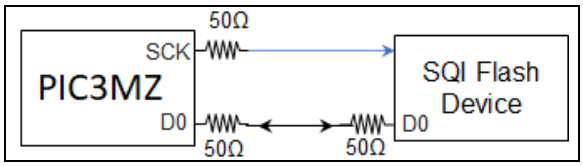
2.10.1 SYSTEM DESIGN

2.10.1.1 Impedance Matching

When selecting parts to place on high-speed buses, particularly the SQI bus, if the impedance of the peripheral device does not match the impedance of the pins on the PIC32MZ DAK/DAL/DAR/DAS device to which it is connected, signal reflections could result, thereby degrading the quality of the signal.

If it is not possible to select a product that matches impedance. For unidirectional signals place a series resistor at the output of the driver between 33-50 ohm generally, For Bi-directional signals place a series resistor at both ends of the trace next to any output driver on the bus. See Figure 2-8 for an example.

FIGURE 2-8: SERIES RESISTOR



2.10.1.2 PCB Layout Recommendations

The following list contains recommendations that will help ensure the PCB layout will promote the goals previously listed.

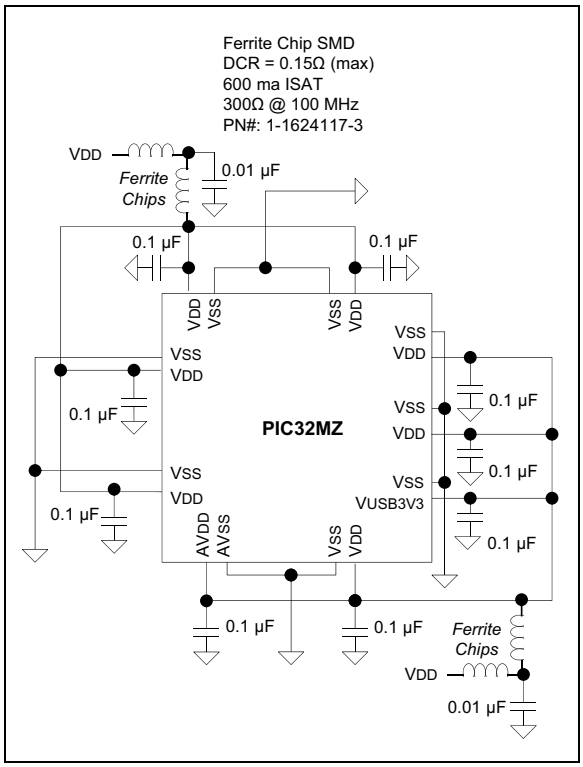
- **Component Placement**
  - Place bypass capacitors as close to their component power and ground pins as possible, and place them on the same side of the PCB
  - Devices on the same bus that have larger setup times should be placed closer to the PIC32MZ DAK/DAL/DAR/DAS device
- **Power and Ground**
  - Multi-layer PCBs will allow separate power and ground planes
  - Each ground pin should be connected to the ground plane individually
  - Place bypass capacitor vias as close to the pad as possible (preferably inside the pad)
  - If power and ground planes are not used, maximize width for power and ground traces
  - Use low-ESR, surface-mount bypass capacitors
- **Clocks and Oscillators**
  - Place crystals as close as possible to the PIC32MZ DAK/DAL/DAR/DAS device OSC/SOSC pins
  - Do not route high-speed signals near the clock or oscillator
  - Avoid via usage and branches in clock lines (SQICLK)
  - Place termination resistors at the end of clock lines
- **Traces**
  - Higher-priority signals should have the shortest traces
  - Match trace lengths for parallel buses (EBIAx, EBIDx, SQIDx)
  - Avoid long run lengths on parallel traces to reduce coupling
  - Make the clock traces as straight as possible
  - Use rounded turns rather than right-angle turns
  - Have traces on different layers intersect on right angles to minimize crosstalk
  - Maximize the distance between traces, preferably no less than three times the trace width
  - Power traces should be as short and as wide as possible
  - High-speed traces should be placed close to the ground plane

2.10.1.3 EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations

The use of LDO regulators is preferred to reduce overall system noise and provide a cleaner power source. However, when utilizing switching Buck/Boost regulators as the local power source for PIC32MZ DAK/DAL/DAR/DAS devices, as well as in electrically noisy environments or test conditions required for IEC 61000-4-4 and IEC 61000-4-2, users should evaluate the use of T-Filters (i.e., L-C-L) on the power pins, as shown in Figure 2-9. In addition to a more stable power source, using T-Filters can greatly reduce susceptibility to EMI sources and events.

> **Note:** The EMI/EMC/EFT Suppression Circuit represents only a few supply/ground pairs. However, the number of pairs on a given package may vary. The number of T-Filters in the system depends on the ferrite chip current limitation and the number of supply/ground pairs.

FIGURE 2-9: EMI/EMC/EFT SUPPRESSION CIRCUIT



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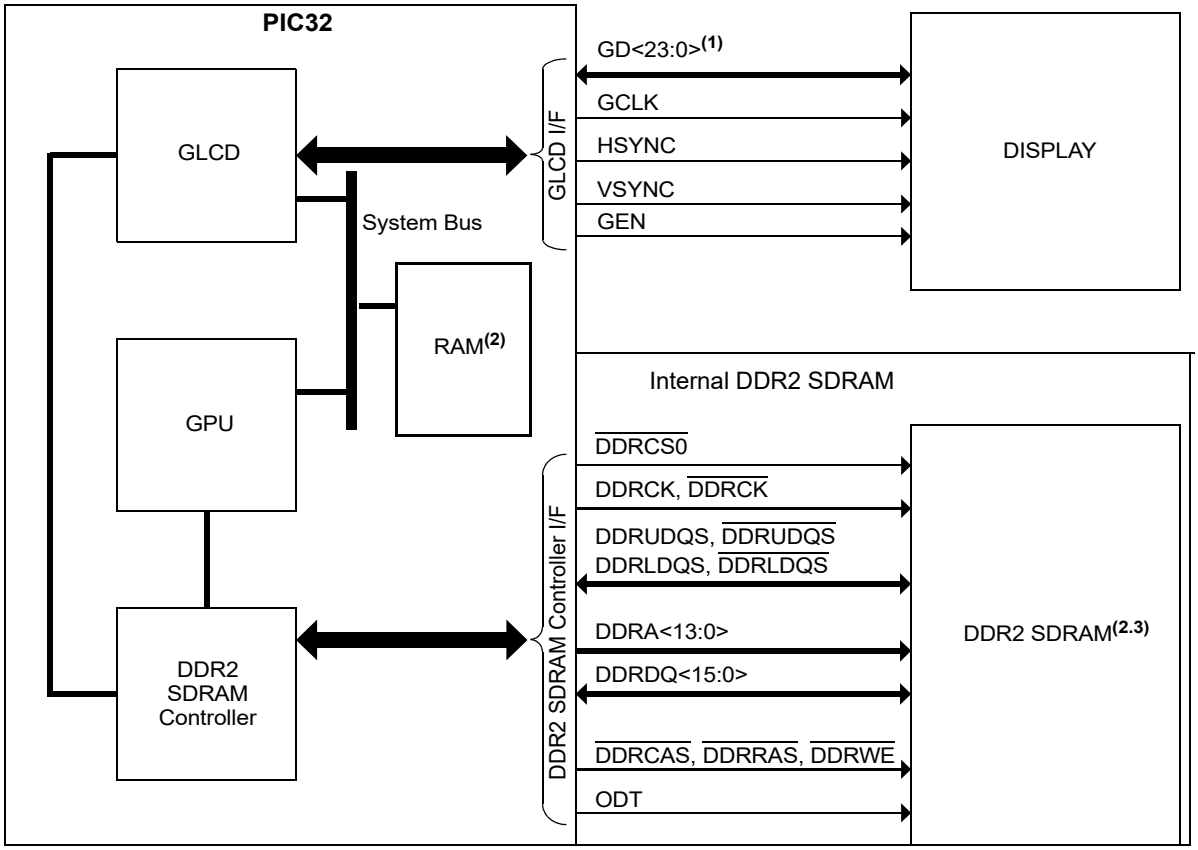
2.11 Typical Application Connection Example

An example of a typical application connection is shown in Figure 2-10.

FIGURE 2-10: GRAPHICS APPLICATION



Note 1: R<7:0> = GD<7:0>; G<7:0> = GD<15:8>; B<7:0> = GD<23:16>.

2: Frame buffers are either in system RAM or in the DDR2 SDRAM (maximum resolution supported depends on the memory size).

3: Supports 32 MB internal DDR2 SDRAM.

NOTES:

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3.0 CPU

Note 1: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

2: MIPS32® microAptiv™ Microprocessor Core resources are available at: http://www.imgtec.com.

The MIPS32 microAptiv Microprocessor Core is the heart of the PIC32MZ DAK/DAL/DAR/DAS family device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

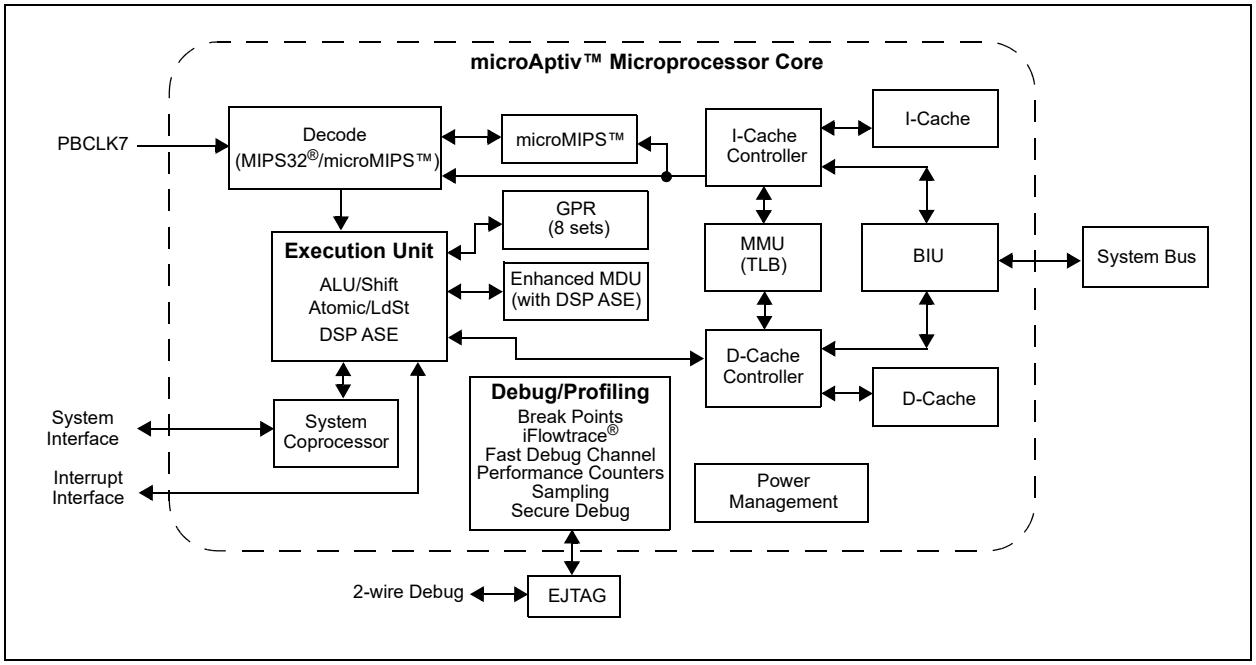
3.1 Features

The following are key features of the PIC32MZ DAK/DAL/DAR/DAS family processor core:

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2):
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions
  - Virtual memory support
- microMIPS compatible instruction set:
  - Improves code size density over MIPS32, while maintaining MIPS32 performance.
  - Supports all MIPS32 instructions (except branch-likely instructions)
  - Fifteen additional 32-bit instructions and 39 16-bit instructions corresponding to commonly-used MIPS32 instructions
  - Stack pointer implicit in instruction
  - MIPS32 assembly and ABI compatible
- MMU with Translation Lookaside Buffer (TLB) mechanism:
  - 32 dual-entry fully associative Joint TLB
  - 4-entry fully associative Instruction TLB
  - 4-entry fully associative Data TLB
  - 4 KB pages
- Separate L1 data and instruction caches:
  - 32 KB 4-way Instruction Cache (I-Cache)
  - 32 KB 4-way Data Cache (D-Cache)
- Autonomous Multiply/Divide Unit (MDU):
  - Maximum issue rate of one 32x32 multiply per clock
  - Early-in iterative divide. Minimum 12 and maximum 38 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control:
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace:
  - Support for single stepping
  - Virtual instruction and data address/value breakpoints
  - Hardware breakpoint supports both address match and address range triggering.
  - Eight instruction and four data complex breakpoints
- iFlowtrace® version 2.0 support:
  - Real-time instruction program counter
  - Special events trace capability
  - Two performance counters with 34 user-selectable countable events
  - Disabled if the processor enters Debug mode
- Four Watch registers:
  - Instruction, Data Read, Data Write options
  - Address match masking options
- DSP ASE Extension:
  - Native fractional format data type operations
  - Register Single Instruction Multiple Data (SIMD) operations (add, subtract, multiply, shift)
  - GPR-based shift
  - Bit manipulation
  - Compare-Pick
  - DSP Control Access
  - Indexed-Load
  - Branch
  - Multiplication of complex operands
  - Variable bit insertion and extraction
  - Virtual circular buffers
  - Arithmetic saturation and overflow handling
  - Zero-cycle overhead saturation and rounding operations

Figure 3-1 illustrates the block diagram of the PIC32MZ DAK/DAL/DAR/DAS family processor core.

FIGURE 3-1: PIC32MZ DAK/DAL/DAR/DAS FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



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3.2 Architecture Overview

The MIPS32 microAptiv Microprocessor core in PIC32MZ DAK/DAL/DAR/DAS family devices contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System control coprocessor (CP0)
- Memory Management Unit (MMU)
- Instruction/Data cache controllers
- Power Management
- Instructions and data caches
- microMIPS support
- Enhanced JTAG (EJTAG) controller

3.2.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. Seven additional register file shadow sets (containing thirty-two registers) are added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Trap condition comparator
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner
- DSP ALU and logic block for performing DSP instructions, such as arithmetic/shift/compare operations

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations, and DSP ASE multiply instructions. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x32 booth recoded multiplier, four pairs of result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown (‘32’ of 32x32) represents the *rs* operand. The second number (‘32’ of 32x32) represents the *rt* operand.

The MDU supports execution of one multiply or multiply-accumulate operation every clock cycle.

Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent `MDU` instruction while a divide is still active causes an IU pipeline stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the processor core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS32 microAptiv MICROPROCESSOR CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU, MADD/MADDU, MSUB/MSUBU` (HI/LO destination)	16 bits	5	1
	32 bits	5	1
`MUL` (GPR destination)	16 bits	5	1
	32 bits	5	1
`DIV/DIVU`	8 bits	12/14	12/14
	16 bits	20/22	20/22
	24 bits	28/30	28/30
	32 bits	36/38	36/38

The MIPS architecture defines that the result of a multiply or divide operation be placed in one of four pairs of HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

The MDU also implements various shift instructions operating on the HI/LO register and multiply instructions as defined in the DSP ASE. The MDU supports all of the data types required for this purpose and includes three extra HI/LO registers as defined by the ASE.

Table 3-2 lists the latencies and repeat rates for the DSP multiply and dot-product operations. The approximate latencies and repeat rates are listed in terms of pipeline clocks.

TABLE 3-2: DSP-RELATED LATENCIES AND REPEAT RATES

Op code	Latency	Repeat Rate
Multiply and dot-product without saturation after accumulation	5	1
Multiply and dot-product with saturation after accumulation	5	1
Multiply without accumulation	5	1

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation and cache protocols, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as cache size and set associativity, and the presence of options like microMIPS, is also available by accessing the CP0 registers, listed in Table 3-3.

TABLE 3-3: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0	Index	Index into the TLB array (microAptiv MPU only).
1	Random	Randomly generated index into the TLB array (microAptiv MPU only).
2	EntryLo0	Low-order portion of the TLB entry for even-numbered virtual pages (microAptiv MPU only).
3	EntryLo1	Low-order portion of the TLB entry for odd-numbered virtual pages (microAptiv MPU only).
4	Context/ UserLocal	Pointer to the page table entry in memory (microAptiv MPU only). User information that can be written by privileged software and read via the RDHWR instruction.
5	PageMask/ PageGrain	PageMask controls the variable page sizes in TLB entries. PageGrain enables support of 1 KB pages in the TLB (microAptiv MPU only).
6	Wired	Controls the number of fixed (i.e., wired) TLB entries (microAptiv MPU only).
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-privileged mode.
8	BadVAddr	Reports the address for the most recent address-related exception.
9	Count	Processor cycle count.
10	EntryHi	High-order portion of the TLB entry (microAptiv MPU only).
11	Compare	Core timer interrupt control.

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TABLE 3-3: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
12	Status	Processor status and control.
	IntCtl	Interrupt control of vector spacing.
	SRSCtl	Shadow register set control.
	SRSMap	Shadow register mapping control.
	View_IPL	Allows the Priority Level to be read/written without extracting or inserting that bit from/to the Status register.
	SRSMAP2	Contains two 4-bit fields that provide the mapping from a vector number to the shadow set number to use when servicing such an interrupt.
13	Cause	Describes the cause of the last exception.
	NestedExc	Contains the error and exception level status bit values that existed prior to the current exception.
	View_RIPL	Enables read access to the RIPL bit that is available in the Cause register.
14	EPC	Program counter at last exception.
	NestedEPC	Contains the exception program counter that existed prior to the current exception.
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	LLAddr	Load link address (microAptiv MPU only).
18	WatchLo	Low-order watchpoint address (microAptiv MPU only).
19	WatchHi	High-order watchpoint address (microAptiv MPU only).
20-22	Reserved	Reserved in the PIC32 core.
23	Debug	EJTAG debug register.
	TraceControl	EJTAG trace control.
	TraceControl2	EJTAG trace control 2.
	UserTraceData1	EJTAG user trace data 1 register.
	TraceBPC	EJTAG trace breakpoint register.
	Debug2	Debug control/exception status 1.
24	DEPC	Program counter at last debug exception.
	UserTraceData2	EJTAG user trace data 2 register.
25	PerfCtl0	Performance counter 0 control.
	PerfCnt0	Performance counter 0.
	PerfCtl1	Performance counter 1 control.
	PerfCnt1	Performance counter 1.
26	ErrCtl	Software test enable of way-select and data RAM arrays for I-Cache and D-Cache (microAptiv MPU only).
27	Reserved	Reserved in the PIC32 core.
28	TagLo/DataLo	Low-order portion of cache tag interface (microAptiv MPU only).

3.3 Power Management

The processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the `WAIT` instruction. For more information on power management, see **Section 40.0 "Power-Saving Features"**.

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MZ family makes extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 L1 Instruction and Data Caches

3.4.1 INSTRUCTION CACHE (I-CACHE)

The I-Cache is an on-core memory block of 32 Kbytes. Because the I-Cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access rather than having to wait for the physical address translation. The tag holds 23 bits of physical address, a valid bit, and a lock bit. The LRU replacement bits are stored in a separate array.

The I-Cache block also contains and manages the instruction line fill buffer. Besides accumulating data to be written to the cache, instruction fetches that reference data in the line fill buffer are serviced either by a bypass of that data, or data coming from the external interface. The I-Cache control logic controls the bypass function.

The processor core supports I-Cache locking. Cache locking allows critical code or data segments to be locked into the cache on a per-line basis, enabling the system programmer to maximize the efficiency of the system cache.

The cache locking function is always available on all I-Cache entries. Entries can then be marked as locked or unlocked on a per entry basis using the `CACHE` instruction.

3.4.2 DATA CACHE (D-CACHE)

The D-Cache is an on-core memory block of 32 Kbytes. This virtually indexed, physically tagged cache is protected. Because the D-Cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access. The tag holds 23 bits of physical address, a valid bit, and a lock bit. There is an additional array holding dirty bits and LRU replacement algorithm bits for each set of the cache.

In addition to I-Cache locking, the processor core also supports a D-Cache locking mechanism identical to the I-Cache. Critical data segments are locked into the cache on a per-line basis. The locked contents can be updated on a store hit, but cannot be selected for replacement on a cache miss.

The D-Cache locking function is always available on all D-Cache entries. Entries can then be marked as locked or unlocked on a per-entry basis using the `CACHE` instruction.

3.4.3 ATTRIBUTES

The processor core I-Cache and D-Cache attributes are listed in the Configuration registers (see Register 3-1 through Register 3-4).

3.5 EJTAG Debug Support

The processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the processor core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (`DERET`) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification specify which registers are selected and how they are used.

3.6 MIPS® DSP ASE Extension

The MIPS DSP Application-Specific Extension Revision 2 is an extension to the MIPS32 architecture. This extension comprises new integer instructions and states that include new HI/LO accumulator register pairs and a DSP control register. This extension is crucial in a wide range of DSP, multimedia, and DSP-like algorithms covering Audio and Video processing applications. The extension supports native fractional format data type operations, register Single Instruction Multiple Data (SIMD) operations, such as add, subtract, multiply, and shift. In addition, the extension includes the following features that are essential in making DSP algorithms computationally efficient:

- Support for multiplication of complex operands
- Variable bit insertion and extraction
- Implementation and use of virtual circular buffers
- Arithmetic saturation and overflow handling support
- Zero cycle overhead saturation and rounding operations

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3.7 microAptiv Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the microAptiv core, which is included on the PIC32MZ DAK/DAL/DAR/DAS family devices.

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	ISP
23:16	R-0	R-0	R-1	R-0	U-0	R-1	R-0	R-0
	DSP	UDI	SB	MDU	—	MM<1:0>		BM
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-0
	BE	AT<1:0>		AR<2:0>			MT<2:1>	
7:0	R-1	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0
	MT<0>	—	—	—	—	K0<2:0>		

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to ‘1’ to indicate the presence of the Config1 register.

bit 30-25 **Unimplemented:** Read as ‘0’

bit 24 **ISP:** Instruction Scratch Pad RAM bit
0 = Instruction Scratch Pad RAM is not implemented

bit 23 **DSP:** Data Scratch Pad RAM bit
0 = Data Scratch Pad RAM is not implemented

bit 22 **UDI:** User-defined bit
0 = CorExtend User-Defined Instructions are not implemented

bit 21 **SB:** SimpleBE bit
1 = Only simple byte enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit
0 = Fast, high-performance MDU

bit 19 **Unimplemented:** Read as ‘0’

bit 18-17 **MM<1:0>:** Merge Mode bits
10 = Merging is allowed

bit 16 **BM:** Burst Mode bit
0 = Burst order is sequential

bit 15 **BE:** Endian Mode bit
0 = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits
00 = MIPS32

bit 12-10 **AR<2:0>:** Architecture Revision Level bits
001 = MIPS32 Release 2

bit 9-7 **MT<2:0>:** MMU Type bits
001 = microAptiv MPU Microprocessor core uses a TLB-based MMU

bit 6-3 **Unimplemented:** Read as ‘0’

bit 2-0 **K0<2:0>:** Kseg0 Coherency Algorithm bits
010 = Uncached

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R-0	R-1	R-1	R-1	R-1	R-1	R-0
	—	MMU Size<5:0>						IS<2>
23:16	R-1	R-1	R-0	R-1	R-1	R-0	R-1	R-1
	IS<1:0>		IL<2:0>			IA<2:0>		
15:8	R-0	R-1	R-1	R-0	R-1	R-1	R-0	R-1
	DS<2:0>			DL<2:0>			DA<2:1>	
7:0	R-1	U-0	U-0	R-1	R-0	R-0	R-1	R-0
	DA<0>	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a ‘1’ to indicate the presence of the Config2 register.

bit 30-25 **MMU Size<5:0>:** Contains the number of TLB entries minus 1
011111 = 32 TLB entries

bit 24-22 **IS<2:0>:** Instruction Cache Sets bits
011 = Contains 512 instruction cache sets per way

bit 21-19 **IL<2:0>:** Instruction-Cache Line bits
011 = Contains instruction cache line size of 16 bytes

bit 18-16 **IA<2:0:** Instruction-Cache Associativity bits
011 = Contains 4-way instruction cache associativity

bit 15-13 **DS<2:0>:** Data-Cache Sets bits
011 = Contains 512 data cache sets per way

bit 12-10 **DL<2:0>:** Data-Cache Line bits
011 = Contains data cache line size of 16 bytes

bit 9-7 **DA<2:0>:** Data-Cache Associativity bits
011 = Contains the 4-way set associativity for the data cache

bit 6-5 **Unimplemented:** Read as ‘0’

bit 4 **PC:** Performance Counter bit
1 = The processor core contains Performance Counters

bit 3 **WR:** Watch Register Presence bit
1 = Four Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating Point Unit bit
0 = Floating Point Unit is not implemented

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REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R/W-y
	—	IPLW<1:0>		MMAR<2:0>			MCU	ISAONEXC(1)
15:8	R-y	R-y	R-1	R-1	R-1	R-1	U-0	R-1
	ISA<1:0>(1)		ULRI	RXI	DSP2P	DSPP	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-1
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired as ‘1’ to indicate the presence of the Config4 register

bit 30-23 **Unimplemented:** Read as ‘0’

bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8-bits in width

bit 20-18 **MMAR<2:0>:** microMIPS Architecture Revision Level bits
000 = Release 1

bit 17 **MCU:** MIPS MCU ASE Implemented bit
1 = MCU™ ASE is implemented

bit 16 **ISAONEXC:** ISA on Exception bit(1)
1 = microMIPS is used on entrance to an exception vector
0 = MIPS32 ISA is used on entrance to an exception vector

bit 15-14 **ISA<1:0>:** Instruction Set Availability bits(1)
11 = Both MIPS32 and microMIPS are implemented; microMIPS is used when coming out of reset
10 = Both MIPS32 and microMIPS are implemented; MIPS32 ISA used when coming out of reset

bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented

bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented

bit 11 **DSP2P:** MIPS DSP ASE Revision 2 Presence bit
1 = DSP Revision 2 is present

bit 10 **DSPP:** MIPS DSP ASE Presence bit
1 = DSP is present

bit 9 **Unimplemented:** Read as ‘0’

bit 8 **ITL:** Indicates that iFlowtrace hardware is present
1 = The iFlowtrace is implemented in the core

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented.

bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented

bit 4 **SP:** Small Page bit
0 = 4 KB page size

bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented

bit 2-1 **Unimplemented:** Read as ‘0’

bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented (this is old trace logic, which is replaced by iFlowtrace (ITL bit))

Note 1: These bits are set based on the value of the BOOTISA Configuration bit (DEVCFG0<6>).

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as ‘0’

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

REGISTER 3-5: CONFIG7: CONFIGURATION REGISTER 7; CP0 REGISTER 16, SELECT 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	WII	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **WII:** Wait IE Ignore bit

1 = Indicates that this processor will allow an interrupt to unblock a `WAIT` instruction

bit 30-0 **Unimplemented:** Read as ‘0’

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4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. For detailed information, refer to **Section 48. "Memory Organization and Permissions"** (DS60001214), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The PIC32MZ DAK/DAL/DAR/DAS microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, PIC32MZ DAK/DAL/DAR/DAS devices allow execution from data memory.

The key features of this module include:

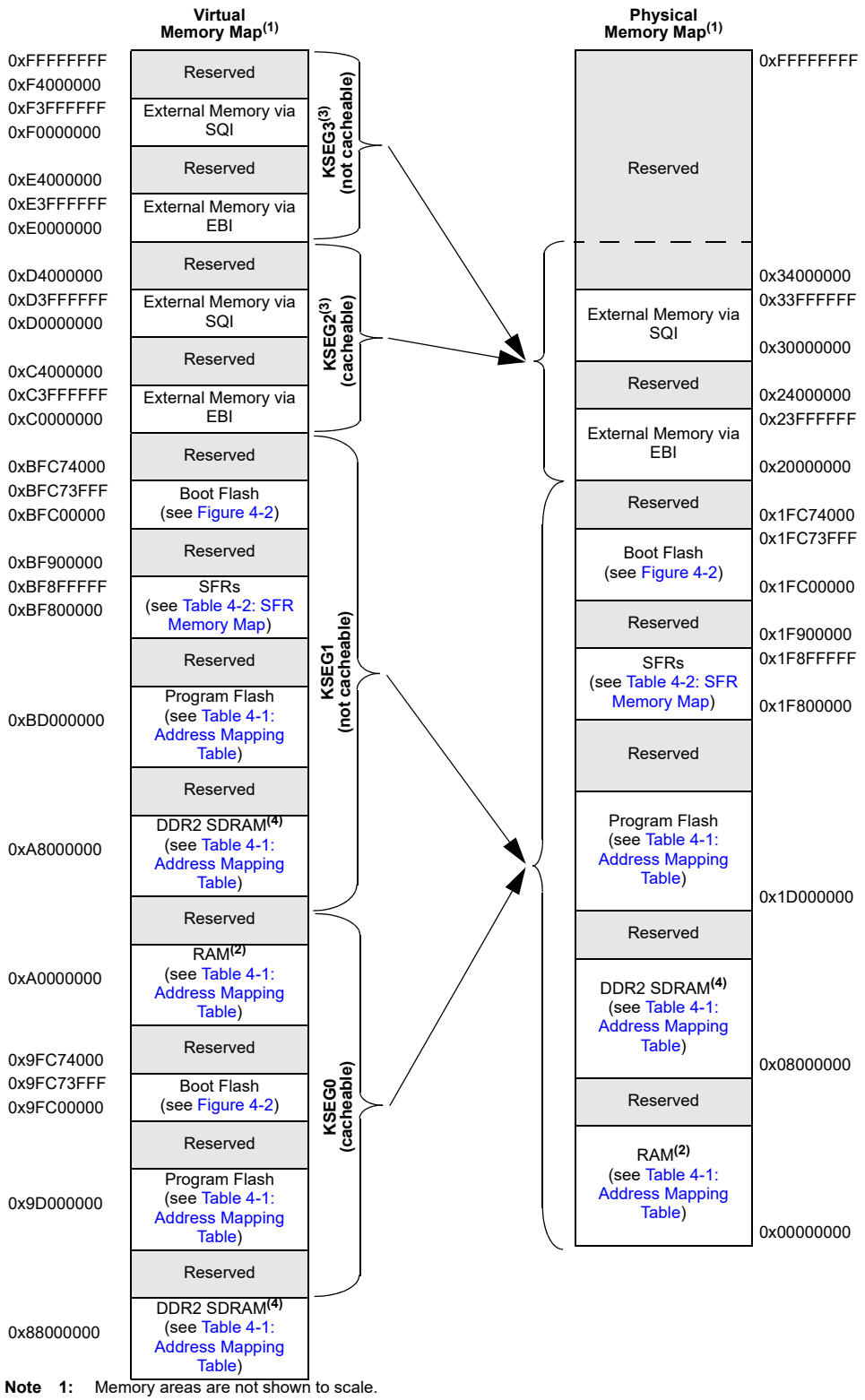
- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1/KSEG2/KSEG3) mode address space
- Separate Boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Cacheable (KSEG0/KSEG2) and non-cacheable (KSEG1/KSEG3) address regions
- Read-Write permission access to predefined memory regions

4.1 Memory Layout

PIC32MZ DAK/DAL/DAR/DAS microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus host peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The main memory maps for the PIC32MZ DAK/DAL/DAR/DAS devices are illustrated in Figure 4-1. Figure 4-2 provides memory map information for Boot Flash and boot alias. Table 4-1: Address Mapping Table provides memory map information for Program Flash, RAM, and DDR2 SDRAM. Table 4-2: SFR Memory Map provides memory map information for Special Function Registers (SFRs).

FIGURE 4-1: PIC32MZ DAK/DAL/DAR/DAS FAMILY MEMORY MAP



Note 1: Memory areas are not shown to scale.

2: RAM memory is divided into two banks. Refer to Table 4-1: Address Mapping Table for additional information.

3: The MMU must be enabled and the TLB must be set up to access this segment.

4: This region is Reserved in devices without the DDR2 option.

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TABLE 4-1: ADDRESS MAPPING TABLE

Memory	Size	Region End Address (KSEG1)	Region End Address (KSEG0)	Region End Address (Physical)
Program Flash	2 MB	0xBD1FFFFF	0x9D1FFFFF	0x1D1FFFFF
	1 MB	0xBD0FFFFF	0x9D0FFFFF	0x1D0FFFFF
DDR2 SDRAM	32 MB(4)	0xA9FFFFFF	0x89FFFFFF	0x09FFFFFF
	—(1)	Reserved	Reserved	Reserved
RAM	640 KB(2)	0xA009FFFF	0x8009FFFF	0x0009FFFF
	256 KB(3)	0xA003FFFF	0x8003FFFF	0x0003FFFF

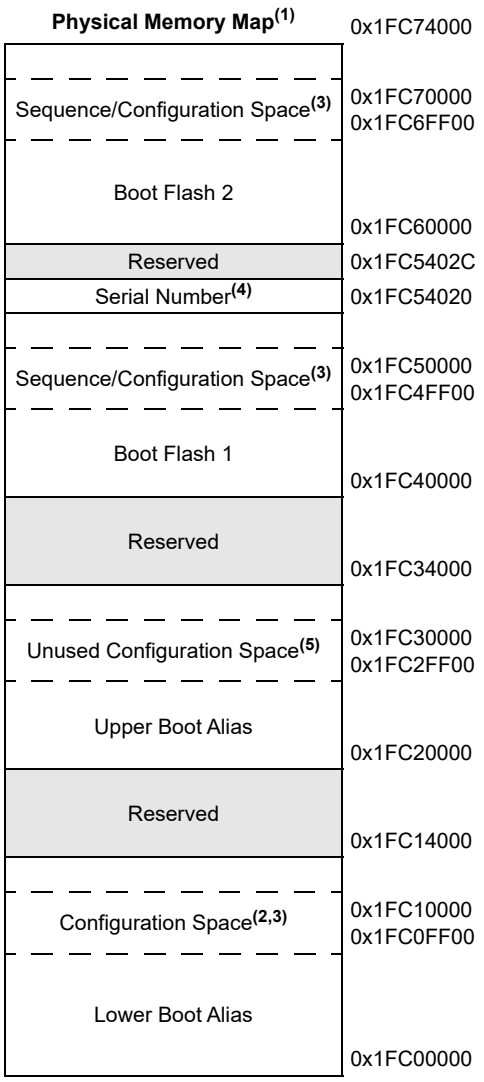
Note 1: Devices without the DDR2 option.

2: Devices with 640 KB RAM contain SRAM Bank 1 (256 KB) and SRAM Bank 2 (384 KB).

3: Devices with 256 KB RAM contain SRAM Bank 1 (128 KB) and SRAM Bank 2 (128 KB).

4: Refer to **4.2 "DDR2 SDRAM"** for DDR2 SDRAM features, which are applicable to devices with internal DDR2 SDRAM.

FIGURE 4-2: BOOT AND ALIAS MEMORY MAP



Note 1: Memory areas are not shown to scale.

2: Memory locations 0x1FC0FF40 through 0x1FC0FFFC are used to initialize Configuration registers (see **Section 41.0 "Special Features"**).

3: Refer to **Section 4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

4: Memory location 0x1FC54020 contains a 128-bit unique device serial number (see **Section 41.0 "Special Features"**).

5: This configuration space cannot be used for executing code in the upper boot alias.

TABLE 4-2: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
System Bus(1)	0xBF8F0000	0x0000
SDHC	0xBF8E0000	0xC000
GPU		0xB000
GLCD		0xA000
DDRPHY		0x9100
DDRC		0x8000
RNG		0x6000
Crypto		0x5000
USB		0x3000
SQI1		0x2000
EBI		0x1000
Prefetch		0x0000
DSCTRL	0xBF8C0000	0x0200
RTCC		0x0000
USBCR	0xBF880000	0x4000
Ethernet		0x2000
CAN1 and CAN2		0x0000
PORTA-PORTK	0xBF860000	0x0000
CTMU	0xBF840000	0xC200
Comparator 1, 2		0xC000
ADC		0xB000
OC1-OC9		0x4000
IC1-IC9		0x2000
Timer1-Timer9		0x0000
PMP	0xBF820000	0xE000
UART1-UART6		0x2000
SPI1-SPI6		0x1000
I2C1-I2C5		0x0000
DMA	0xBF810000	0x1000
Interrupt Controller		0x0000
HLVD	0xBF800000	0x1800
PPS		0x1400
Oscillator		0x1200
CVREF		0x0E00
Deadman Timer		0x0A00
Watchdog Timer		0x0800
Flash Controller		0x0600
Configuration		0x0000

Note 1: Refer to **4.4 "System Bus Arbitration"** for important legal information.

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4.1.1 BOOT FLASH SEQUENCE AND CONFIGURATION SPACES

Sequence space is used to identify which Boot Flash is aliased by aliased regions. If the value programmed into the TSEQ<15:0> bits of the BF1SEQ3 word is equal to or greater than the value programmed into the TSEQ<15:0> bits of the BF2SEQ3 word, Boot Flash 1 is aliased by the lower boot alias region, and Boot Flash 2 is aliased by the upper boot alias region. If the TSEQ<15:0> bits of the BF2SEQ3 word are greater than the TSEQ<15:0> bits of the BF1SEQ3 word, the opposite is true (see TABLE 4-3: Boot Flash 1 Sequence and Configuration Words Summary and TABLE 4-4: Boot Flash 2 Sequence and Configuration Words Summary for BFxSEQ3 word memory locations).

The CSEQ<15:0> bits must contain the complement value of the TSEQ<15:0> bits; otherwise, the value of the TSEQ<15:0> bits are considered invalid, and an alternate sequence is used, see **Section 4.1.2 "Alternate Sequence and Configuration Words"** for more information.

Once Boot Flash memories are aliased, configuration space located in the lower boot alias region is used as the basis for the Configuration words, DEVSIGN0, DEVCP0, and DEVCFGx (and the associated alternate configuration registers). This means that the Boot Flash region to be aliased by lower boot alias region memory must contain configuration values in the appropriate memory locations.

Note:	Do not use word program operation (NVMOP<3:0> = `0001`) when programming data into the sequence and configuration spaces.

4.1.2 ALTERNATE SEQUENCE AND CONFIGURATION WORDS

Every word in the configuration space and sequence space has an associated alternate word (designated by the letter A as the first letter in the name of the word). During device start-up, primary words are read and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and alternate words are used. If uncorrectable ECC errors are found in primary and alternate words, the BCFGFAIL (RCON<26>) flag is set and the default configuration is used.

TABLE 4-3: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
FF3C	ABF1DEVCFG4	31:0	**Note:** See TABLE 41-2: ADEVCFG: Alternate Device Configuration Word Summary for the bit descriptions.																xxxx
FF40	ABF1DEVCFG3	31:0																	xxxx
FF44	ABF1DEVCFG2	31:0																	xxxx
FF48	ABF1DEVCFG1	31:0																	xxxx
FF4C	ABF1DEVCFG0	31:0																	xxxx
FF50	ABF1DEVCP3	31:0																	xxxx
FF54	ABF1DEVCP2	31:0																	xxxx
FF58	ABF1DEVCP1	31:0																	xxxx
FF5C	ABF1DEVCP0	31:0																	xxxx
FF60	ABF1DEVSIGN3	31:0																	xxxx
FF64	ABF1DEVSIGN2	31:0																	xxxx
FF68	ABF1DEVSIGN1	31:0																	xxxx
FF6C	ABF1DEVSIGN0	31:0																	xxxx
FF70	ABF1SEQ3	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFF4	ABF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF78	ABF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF7C	ABF1SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFBC	BF1DEVCFG4	31:0	**Note:** See TABLE 41-1: DEVCFG: Device Configuration Word Summary for the bit descriptions.																xxxx
FFC0	BF1DEVCFG3	31:0																	xxxx
FFC4	BF1DEVCFG2	31:0																	xxxx
FFC8	BF1DEVCFG1	31:0																	xxxx
FFCC	BF1DEVCFG0	31:0																	xxxx
FFD0	BF1DEVCP3	31:0																	xxxx
FFD4	BF1DEVCP2	31:0																	xxxx
FFD8	BF1DEVCP1	31:0																	xxxx
FFDC	BF1DEVCP0	31:0																	xxxx
FFE0	BF1DEVSIGN3	31:0																	xxxx
FFE4	BF1DEVSIGN2	31:0																	xxxx
FFE8	BF1DEVSIGN1	31:0																	xxxx
FFEC	BF1DEVSIGN0	31:0																	xxxx
FFF0	BF1SEQ3	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFF4	BF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFF8	BF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFFC	BF1SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Read corresponding register bit detail for this information. Reset values are shown in hexadecimal.

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TABLE 4-4: BOOT FLASH 2 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC6_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FF3C	ABF2DEVCFG4	31:0	**Note:** See TABLE 41-2: ADEVCFG: Alternate Device Configuration Word Summary for the bit descriptions.																xxxx
FF40	ABF2DEVCFG3	31:0																	xxxx
FF44	ABF2DEVCFG2	31:0																	xxxx
FF48	ABF2DEVCFG1	31:0																	xxxx
FF4C	ABF2DEVCFG0	31:0																	xxxx
FF50	ABF2DEVCP3	31:0																	xxxx
FF54	ABF2DEVCP2	31:0																	xxxx
FF58	ABF2DEVCP1	31:0																	xxxx
FF5C	ABF2DEVCP0	31:0																	xxxx
FF60	ABF2DEVSIGN3	31:0																	xxxx
FF64	ABF2DEVSIGN2	31:0																	xxxx
FF68	ABF2DEVSIGN1	31:0																	xxxx
FF6C	ABF2DEVSIGN0	31:0																	xxxx
FF70	ABF2SEQ3	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFF4	ABF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF78	ABF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF7C	ABF2SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFBC	BF2DEVCFG4	31:0	**Note:** See TABLE 41-1: DEVCFG: Device Configuration Word Summary for the bit descriptions.																xxxx
FFC0	BF2DEVCFG3	31:0																	xxxx
FFC4	BF2DEVCFG2	31:0																	xxxx
FFC8	BF2DEVCFG1	31:0																	xxxx
FFCC	BF2DEVCFG0	31:0																	xxxx
FFD0	BF2DEVCP3	31:0																	xxxx
FFD4	BF2DEVCP2	31:0																	xxxx
FFD8	BF2DEVCP1	31:0																	xxxx
FFDC	BF2DEVCP0	31:0																	xxxx
FFE0	BF2DEVSIGN3	31:0																	xxxx
FFE4	BF2DEVSIGN2	31:0																	xxxx
FFE8	BF2DEVSIGN1	31:0																	xxxx
FFEC	BF2DEVSIGN0	31:0																	xxxx
FFF0	BF2SEQ3	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx
FFF4	BF2SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFF8	BF2SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFFC	BF2SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = Read corresponding register bit detail for this information. Reset values are shown in hexadecimal.

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REGISTER 4-1: BFxSEQ3/ABFxSEQ3: BOOT FLASH ‘x’ SEQUENCE WORD 0 REGISTER (‘x’ = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<7:0>							
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **CSEQ<15:0>:** Boot Flash Complement Sequence Number bits

bit 15-0 **TSEQ<15:0>:** Boot Flash True Sequence Number bits

Note: The registers BFxSEQ0 through BFxSEQ2 and ABFxSEQ0 through ABFxSEQ2 are used for Quad Word programming operation when programming the BFxSEQ3/ABFxSEQ3 registers, and do not contain any valid information.

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4.2 DDR2 SDRAM

Stacked DDR2 SDRAM memory devices support 32 MB of DDR2 SDRAM. Memory in these devices is organized as 4,194,304 x 4 banks x 16 bits. Refer to Figure 4-1 and Table 4-1: Address Mapping Table for the DDR2 SDRAM address ranges.

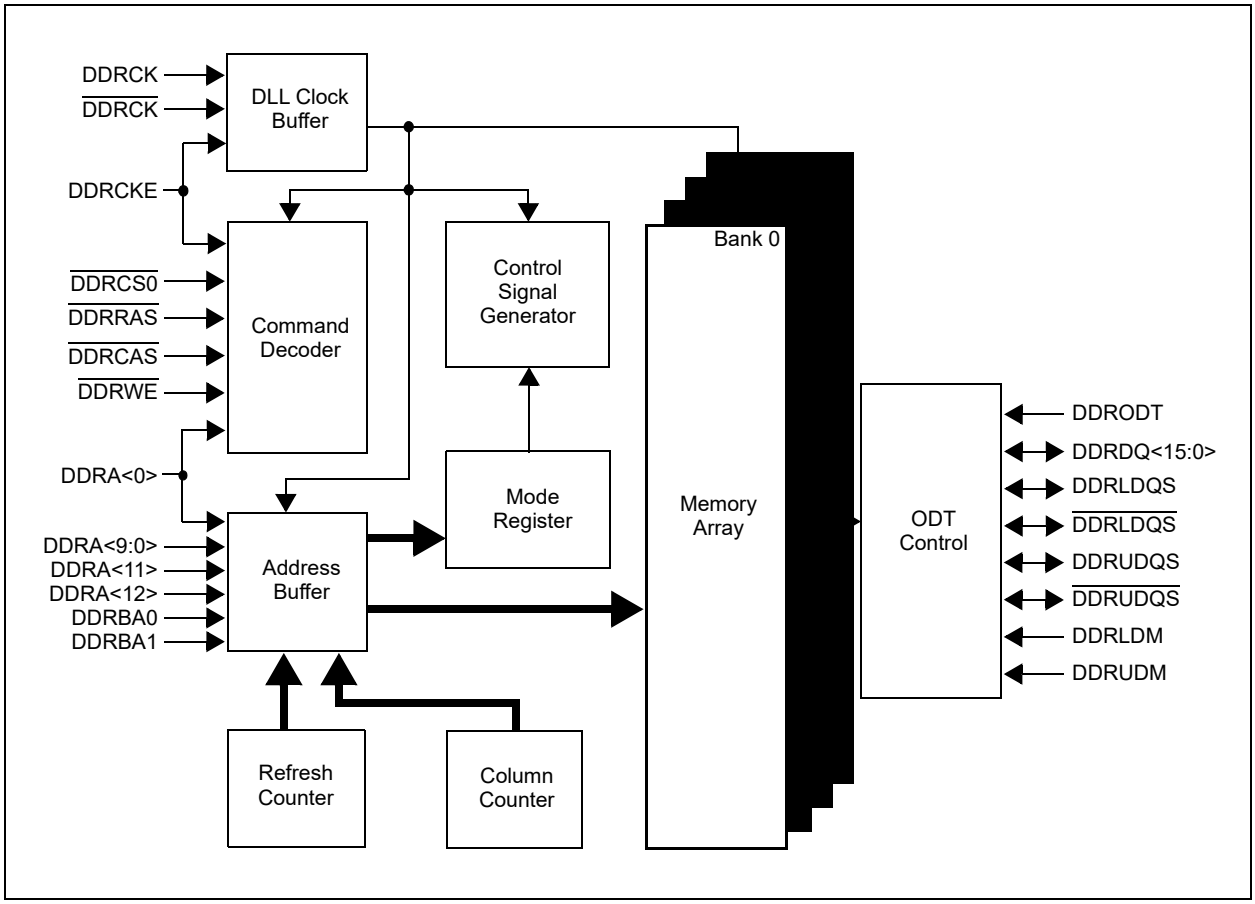
4.2.1 FEATURES

The DDR2 SDRAM includes the following features:

- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3, 4, and 5
- Burst Length: 8
- Bi-directional, differential data strobes (DDRUDQS, DDRLDQS and $\overline{\text{DDRUDQS}}$, $\overline{\text{DDRLDQS}}$) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns Data (DDRDQx) and Data Qualifier Strobe (DDRxDQS, $\overline{\text{DDRxDQS}}$) transitions with clock
- Differential clock inputs (DDRCK and /DDRCK)
- Data masks (DDRUDM, DDRLDM) for write data
- Commands entered on each positive DDRCK edge, data and data mask are referenced to both edges of DDRxDQS
- Posted CAS programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Latency = Read Latency - 1 (WL = RL - 1)

Figure 4-3 provides a block diagram of the DDR2 SDRAM.

FIGURE 4-3: DDR2 SDRAM BLOCK DIAGRAM



4.3 Timing Parameters

Table 44-55: DDR2 SDRAM Timing Specifications shows internal 32 MB DDR2 SDRAM timing parameters.

4.4 System Bus Arbitration

Note:	The System Bus interconnect implements many instantiations of the SonicsSX® interconnect from Sonics, Inc. This document contains materials that are (c) 2003-2015 Sonics, Inc., and that constitute proprietary information of Sonics, Inc. SonicsSX is a registered trademark of Sonics, Inc. All such materials and trademarks are used under license from Sonics, Inc.

As shown in the PIC32MZ DAK/DAL/DAR/DAS Family Block Diagram (see Figure 1-1), there are multiple initiator modules (I1 through I14) in the system that can access various target modules (T1 through T23). TABLE 4-5: Initiators to Targets Access Association illustrates which initiator can access which target. The System Bus supports simultaneous access to targets by initiators, so long as the initiators are accessing different targets. The System Bus will perform arbitration if multiple initiators attempt to access the same target.

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TABLE 4-5: INITIATORS TO TARGETS ACCESS ASSOCIATION

Target Number	Initiator ID	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Name	CPU	DMA Read	DMA Write	USB	Ethernet Read	Ethernet Write	CAN1	CAN2	SQI1	Flash Controller	Crypto	GLCD	GPU	SDHC
1	**Flash Memory:** Program Flash Boot Flash Prefetch Module	X	X		X	X		X	X			X			
2	RAM Bank 1 Memory	X	X	X	X	X	X	X	X	X	X	X	X	X	X
3	RAM Bank 2 Memory	X	X	X	X	X	X	X	X	X	X	X	X	X	X
5	**Peripheral Set 1:** System Control Flash Control DMT CVREF PPS Input PPS Output Interrupts DMA WDT	X													
6	**Peripheral Set 2:** SPI1-SPI6 I2C1-I2C5 UART1-UART6 PMP	X	X	X											
7	**Peripheral Set 3:** Timer1-Timer9 IC1-IC9 OC1-OC9 ADC Comparator 1 Comparator 2 CTMU	X	X	X											
8	**Peripheral Set 4:** PORTA-PORTK	X	X	X											
9	**Peripheral Set 5:** CAN1 CAN2 Ethernet Controller	X	X	X											
10	USB	X	X	X											
11	External Memory via SQI1 and SQI1 Module	X													
12	Crypto Engine	X													
13	RNG Module	X													
14	Graphics LCD Controller	X													
15	DDR2 SDRAM Memory via DDR2 and DDR2 Target 0	X													
16	DDR2 SDRAM Memory via DDR2 and DDR2 Targets 1 and 2		X	X	X	X	X	X	X	X	X	X			X

Note 1: The GLCD and GPU are directly connected to the DDR2 SDRAM Controller to use DDR2 SDRAM for frame buffers. Arbitration control is done through the DDR2 SDRAM Controller arbitration engine. Refer to **Section 55. "DDR2 SDRAM Controller"** (DS60001321) in the "PIC32 Family Reference Manual" for additional information.

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TABLE 4-5: INITIATORS TO TARGETS ACCESS ASSOCIATION (CONTINUED)

Target Number	Initiator ID	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Name	CPU	DMA Read	DMA Write	USB	Ethernet Read	Ethernet Write	CAN1	CAN2	SQI1	Flash Controller	Crypto	GLCD	GPU	SDHC
17	DDR2 SDRAM Memory via DDR2 and DDR2 Targets 3 and 4												X(1)	X(1)	
18	2D Graphics Processing Unit	X													
19	Secure Digital Host Controller	X													
20	DDR2 PHY Control Register Interface	X													
21	DDR2 Control Register Interface	X													
22	**Peripheral Set 6:** RTCC DSCTRL	X													
23	External Memory via EBI and EBI Module	X	X	X	X	X	X	X	X	X		X			X

Note 1: The GLCD and GPU are directly connected to the DDR2 SDRAM Controller to use DDR2 SDRAM for frame buffers. Arbitration control is done through the DDR2 SDRAM Controller arbitration engine. Refer to **Section 55. "DDR2 SDRAM Controller"** (DS60001321) in the "PIC32 Family Reference Manual" for additional information.

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The System Bus arbitration scheme implements a non-programmable, Least Recently Serviced (LRS).

The arbitration scheme for the available initiators is shown in Table 4-6: Initiator ID and Arbitration.

TABLE 4-6: INITIATOR ID AND ARBITRATION

ID	Name	Arbitration
1	CPU	LRS
2	DMA Read	LRS
3	DMA Write	LRS
4	USB	LRS
5	Ethernet Read	LRS
6	Ethernet Write	LRS
7	CAN1	LRS
8	CAN2	LRS
9	SQI1	LRS
10	Flash Controller	LRS
11	Crypto	LRS
12	GLCD(1)	LRS
13	GPU(1)	LRS
14	SDHC	LRS

Note 1: The GLCD and GPU are directly connected to the DDR2 SDRAM controller to use the DDR2 SDRAM for frame buffers. Arbitration control is done through the DDR2 SDRAM Controller arbitration engine.

4.5 Permission Access and System Bus Registers

The System Bus on the PIC32MZ DAK/DAL/DAR/DAS family of microcontrollers provides access control capabilities for the transaction initiators on the System Bus.

The System Bus divides the entire memory space into 17 regions and permits access to each target by initiators through permission groups. Four Permission Groups (0 through 3) can be assigned to each initiator. Each permission group is independent of the others and can have exclusive or shared access to a region.

Using the CFGPG register (see Register 41-12 in **Section 41.0 "Special Features"**), Boot firmware can assign a permission group to each initiator, which can make requests on the System Bus.

The available targets and their regions, as well as the associated control registers to assign protection, are described and listed in Table 4-7: System Bus Targets and Associated Protection Registers.

Register 4-2 through Register 4-13 are used for setting and controlling access permission groups and regions.

To change these registers, they must be unlocked in hardware. The register lock is controlled by the PGLOCK Configuration bit (CFGCON<11>). Setting the PGLOCK bit prevents writes to the control registers and clearing the PGLOCK bit allows writes.

To set or clear the PGLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

TABLE 4-7: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS

Target Protection Number	Target Description (see Note 5)	SBTxREGy Register (see Note 7)							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
0	System Bus	SBT0REG0	R	0x1F8F0000	R	64 KB	—	0	SBT0RD0	0,1,1,1	SBT0WR0	0,1,1,1
		SBT0REG1	R	0x1F8F8000	R	32 KB	—	3	SBT0RD1	0,0,0,1	SBT0WR1	0,0,0,1
1	Flash Memory(6): Program Flash Boot Flash Prefetch	SBT1REG0	R	0x1D000000	R(4)	R(4)	—	0	SBT1RD0	0,0,0,0	SBT1WR0	0,0,0,0
		SBT1REG2	R	0x1F8E0000	R	4 KB	1	2	SBT1RD2	R/W(1)	SBT1WR2	R/W(1)
		SBT1REG3	R/W	R/W	R/W	R/W	1	2	SBT1RD3	0,0,0,0	SBT1WR3	0,0,0,0
		SBT1REG4	R/W	R/W	R/W	R/W	1	2	SBT1RD4	0,0,0,0	SBT1WR4	0,0,0,0
		SBT1REG5	R/W	R/W	R/W	R/W	1	2	SBT1RD5	0,0,0,0	SBT1WR5	0,0,0,0
		SBT1REG6	R/W	R/W	R/W	R/W	1	2	SBT1RD6	0,0,0,0	SBT1WR6	0,0,0,0
		SBT1REG7	R/W	R/W	R/W	R/W	0	1	SBT1RD7	0,0,0,0	SBT1WR7	0,0,0,0
		SBT1REG8	R/W	R/W	R/W	R/W	0	1	SBT1RD8	0,0,0,0	SBT1WR8	0,0,0,0
2	RAM Bank 1 Memory	SBT2REG0	R	0	R(4)	R(4)	—	0	SBT2RD0	R/W(1)	SBT2WR0	R/W(1)
		SBT2REG1	R/W	R/W	R/W	R/W	—	3	SBT2RD1	R/W(1)	SBT2WR1	R/W(1)
		SBT2REG2	R/W	R/W	R/W	R/W	0	1	SBT2RD2	R/W(1)	SBT2WR2	R/W(1)
3	RAM Bank 2 Memory	SBT3REG0	R(4)	R(4)	R(4)	R(4)	—	0	SBT3RD0	R/W(1)	SBT3WR0	R/W(1)
		SBT3REG1	R/W	R/W	R/W	R/W	—	3	SBT3RD1	R/W(1)	SBT3WR1	R/W(1)
		SBT3REG2	R/W	R/W	R/W	R/W	0	1	SBT3RD2	R/W(1)	SBT3WR2	R/W(1)
4	DDR Memory via DDR2 and DDR2 Target 0	SBT4REG0	R	0x08000000	R	R(4)	—	0	SBT4RD0	R/W(1)	SBT4WR0	R/W(1)
		SBT4REG1	R/W	R/W	R/W	R/W	—	3	SBT4RD1	R/W(1)	SBT4WR1	R/W(1)
		SBT4REG2	R/W	R/W	R/W	R/W	1	2	SBT4RD2	R/W(1)	SBT4WR2	R/W(1)
		SBT4REG3	R/W	R/W	R/W	R/W	1	2	SBT4RD3	R/W(1)	SBT4WR3	R/W(1)
		SBT4REG4	R/W	R/W	R/W	R/W	1	2	SBT4RD4	R/W(1)	SBT4WR4	R/W(1)
5	DDR Memory via DDR2 and DDR2 Targets 1 and 2	SBT5REG0	R	0x08000000	R	R(4)	—	0	SBT5RD0	R/W(1)	SBT5WR0	R/W(1)
		SBT5REG1	R/W	R/W	R/W	R/W	—	3	SBT5RD1	R/W(1)	SBT5WR1	R/W(1)
		SBT5REG2	R/W	R/W	R/W	R/W	1	2	SBT5RD2	R/W(1)	SBT5WR2	R/W(1)
		SBT5REG3	R/W	R/W	R/W	R/W	1	2	SBT5RD3	R/W(1)	SBT5WR3	R/W(1)
		SBT5REG4	R/W	R/W	R/W	R/W	1	2	SBT5RD4	R/W(1)	SBT5WR4	R/W(1)

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

Note 1: Reset values for these bits are '0', '1', '1', '1', respectively.

2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

4: Refer to the Device Memory Map (Figure 4-1) for specific device memory sizes and start addresses.

5: See Table 4-2: SFR Memory Map for information on specific target memory size and start addresses.

6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

7: The 'x' in the SBTxREGy, SBTxRDy, and SBTxWRy registers represents the target protection number and not the actual target number (e.g., for SQI 'x' = 13 and not 11, whereas 11 is the actual target number).

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TABLE 4-7: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS (CONTINUED)

Target Protection Number	Target Description (see Note 5)	SBTxREGy Register (see Note 7)							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
6	External Memory via EBI and EBI Module(6)	SBT6REG0	R	0x20000000	R	64 MB	—	0	SBT6RD0	R/W(1)	SBT6WR0	R/W(1)
		SBT6REG2	R	0x1F8EC000	R	4 KB	0	1	SBT6RD2	R/W(1)	SBT6WR2	R/W(1)
7	System Controller	SBT7REG0	R	0x1F800000	R	—	—	0	SBT7RD0	R/W(1)	SBT7WR0	R/W(1)
	Flash Controller	SBT7REG1	R/W	R/W	R/W	R/W	—	3	SBT7RD1	R/W(1)	SBT7WR1	R/W(1)
	DMT/WDT CVREF PPS Input PPS Output Interrupts DMA	SBT7REG2	R/W	R/W	R/W	R/W	0	1	SBT7RD2	R/W(1)	SBT7WR2	R/W(1)
8	SPI1-SPI6	SBT8REG0	R	0x1F820000	R	64 KB	—	0	SBT8RD0	R/W(1)	SBT8WR0	R/W(1)
	I2C1-I2C5 UART1-UART6 PMP	SBT8REG1	R/W	R/W	R/W	R/W	—	3	SBT8RD1	R/W(1)	SBT8WR1	R/W(1)
9	Timer1-Timer9	SBT9REG0	R	0x1F840000	R	64 KB	—	0	SBT9RD0	R/W(1)	SBT9WR0	R/W(1)
	IC1-IC9 OC1-OC9 ADC Comparator 1 Comparator 2	SBT9REG1	R/W	R/W	R/W	R/W	—	3	SBT9RD1	R/W(1)	SBT9WR1	R/W(1)
10	PORTA-PORTK	SBT10REG0	R	0x1F860000	R	64 KB	—	0	SBT10RD0	R/W(1)	SBT10WR0	R/W(1)
		SBT10REG1	R/W	R/W	R/W	R/W	—	3	SBT10RD1	R/W(1)	SBT10WR1	R/W(1)
11	CAN1	SBT11REG0	R	0x1F880000	R	64 KB	—	0	SBT11RD0	R/W(1)	SBT11WR0	R/W(1)
	CAN2 Ethernet	SBT11REG1	R/W	R/W	R/W	R/W	—	3	SBT11RD1	R/W(1)	SBT11WR1	R/W(1)
12	GLCD	SBT12REG0	R	0x1F8EA000	R	4 KB	—	0	SBT12RD0	R/W(1)	SBT12WR0	R/W(1)
	GPU		R	0x1F8EB000	R	4 KB	—	0		R/W(1)		R/W(1)
	DDR2PHY		R	0x1F8E9000	R	4 KB	—	0		R/W(1)		R/W(1)
	DDR2SFR		R	0x1F8E8000	R	4 KB	—	0		R/W(1)		R/W(1)
13	External Memory via SQI1 and SQI1	SBT13REG0	R	0x30000000	R	64 MB	—	0	SBT13RD0	R/W(1)	SBT13WR0	R/W(1)
		SBT13REG1	R	0x1F8E2000	R	4 KB	—	3	SBT13RD1	R/W(1)	SBT13WR1	R/W(1)

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

Note 1: Reset values for these bits are '0', '1', '1', '1', respectively.

2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

4: Refer to the Device Memory Map (Figure 4-1) for specific device memory sizes and start addresses.

5: See Table 4-2: SFR Memory Map for information on specific target memory size and start addresses.

6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

7: The 'x' in the SBTxREGy, SBTxRDy, and SBTxWRy registers represents the target protection number and not the actual target number (e.g., for SQI 'x' = 13 and not 11, whereas 11 is the actual target number).

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TABLE 4-7: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS (CONTINUED)

Target Protection Number	Target Description (see Note 5)	SBTxREGy Register (see Note 7)							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
14	DSCTRL RTCC	SBT14REG0	R	0x1F8C0000	R	4 KB	—	0	SBT14RD0	R/W(1)	SBT14WR0	R/W(1)
		SBT14REG1	R/W	R/W	R/W	R/W	—	3	SBT14RD1	R/W(1)	SBT14WR1	R/W(1)
15	USB	SBT15REG0	R	0x1F8E0000	R	4 KB	—	0	SBT15RD0	R/W(1)	SBT15WR0	R/W(1)
	Crypto		R	0x1F8E5000	R	4 KB	—	0		R/W(1)		R/W(1)
	RNG		R	0x1F8E6000	R	4 KB	—	0		R/W(1)		R/W(1)
	SDHC		R	0x1F8EC000	R	4 KB	—	0		R/W(1)		R/W(1)
16	DDR2 SDRAM Memory via DDR2 and DDR2 Targets 3 and 4	SBT16REG0	R	0x08000000	R	R(4)	—	0	SBT16RD0	R/W(1)	SBT16WR0	R/W(1)
		SBT16REG1	R/W	R/W	R/W	R/W	—	3	SBT16RD1	R/W(1)	SBT16WR1	R/W(1)
		SBT16REG2	R/W	R/W	R/W	R/W	1	2	SBT16RD2	R/W(1)	SBT16WR2	R/W(1)
		SBT16REG3	R/W	R/W	R/W	R/W	1	2	SBT16RD3	R/W(1)	SBT16WR3	R/W(1)
		SBT16REG4	R/W	R/W	R/W	R/W	1	2	SBT16RD4	R/W(1)	SBT16WR4	R/W(1)

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

Note 1: Reset values for these bits are '0', '1', '1', '1', respectively.

2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

4: Refer to the Device Memory Map (Figure 4-1) for specific device memory sizes and start addresses.

5: See Table 4-2: SFR Memory Map for information on specific target memory size and start addresses.

6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

7: The 'x' in the SBTxREGy, SBTxRDy, and SBTxWRy registers represents the target protection number and not the actual target number (e.g., for SQI 'x' = 13 and not 11, whereas 11 is the actual target number).

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TABLE 4-8: SYSTEM BUS VIOLATION FLAG REGISTER MAP

Virtual Address (BFxx_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8F_0510	SBFLAG0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	T0PGV0	T3PGV	T6PGV	T2PGV	T5PGV	T4PGV	T1PGV	0000
90_0510	SBFLAG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	T0PGV1	T12PGV	T11PGV	T10PGV	T9PGV	T8PGV	T7PGV	0000
91_0510	SBFLAG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T0PGV2	T15PGV	T14PGV	T13PGV	0000
92_0510	SBFLAG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	T0PGV3	T16PGV	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-9: SYSTEM BUS TARGET PROTECTION GROUP 0 (T0PGV0 - T0PGV3) REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8020	SBT0ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8024	SBT0ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8028	SBT0ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8030	SBT0ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8038	SBT0ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8040	SBT0REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8050	SBT0RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8058	SBT0WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8060	SBT0REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8070	SBT0RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8078	SBT0WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-10: SYSTEM BUS TARGET PROTECTION GROUP 1 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8420	SBT1ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8424	SBT1ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8428	SBT1ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8430	SBT1ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8438	SBT1ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8440	SBT1REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8450	SBT1RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8458	SBT1WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8480	SBT1REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8490	SBT1RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8498	SBT1WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84A0	SBT1REG3	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84B0	SBT1RD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84B8	SBT1WR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84C0	SBT1REG4	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84D0	SBT1RD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84D8	SBT1WR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-10: SYSTEM BUS TARGET PROTECTION GROUP 1 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
84E0	SBT1REG5	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84F0	SBT1RD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84F8	SBT1WR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8500	SBT1REG6	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8510	SBT1RD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8518	SBT1WR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8520	SBT1REG7	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8530	SBT1RD7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8538	SBT1WR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8540	SBT1REG8	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8550	SBT1RD8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8558	SBT1WR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-11: SYSTEM BUS TARGET PROTECTION GROUP 2 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8820	SBT2ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8824	SBT2ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8828	SBT2ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT2ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT2ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT2REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8850	SBT2RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8858	SBT2WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8860	SBT2REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8870	SBT2RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8878	SBT2WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8880	SBT2REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8890	SBT2RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8898	SBT2WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-12: SYSTEM BUS TARGET PROTECTION GROUP 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-13: SYSTEM BUS TARGET PROTECTION GROUP 4 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
9020	SBT4ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9024	SBT4ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9028	SBT4ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9030	SBT4ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9038	SBT4ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9040	SBT4REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9050	SBT4RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9058	SBT4WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9060	SBT4REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9070	SBT4RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9078	SBT4WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9080	SBT4REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9090	SBT4RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9098	SBT4WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
90A0	SBT4REG3	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-13: SYSTEM BUS TARGET PROTECTION GROUP 4 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
90B0	SBT4RD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
90B8	SBT4WR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
90C0	SBT4REG4	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
90D0	SBT4RD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
90D8	SBT4WR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-14: SYSTEM BUS TARGET PROTECTION GROUP 5 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
9420	SBT5ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9424	SBT5ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9428	SBT5ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9430	SBT5ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9438	SBT5ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9440	SBT5REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9450	SBT5RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9458	SBT5WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9460	SBT5REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9470	SBT5RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9478	SBT5WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9480	SBT5REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9490	SBT5RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9498	SBT5WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-14: SYSTEM BUS TARGET PROTECTION GROUP 5 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
94A0	SBT5REG3	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
94B0	SBT5RD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
94B8	SBT5WR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
94C0	SBT5REG4	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
94D0	SBT5RD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
94D8	SBT5WR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-15: SYSTEM BUS TARGET PROTECTION GROUP 6 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
9820	SBT6ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9824	SBT6ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9828	SBT6ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9830	SBT6ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9838	SBT6ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9840	SBT6REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9850	SBT6RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9858	SBT6WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9860	SBT6REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9870	SBT6RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9878	SBT6WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-16: SYSTEM BUS TARGET PROTECTION GROUP 7 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8420	SBT7ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8424	SBT7ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8428	SBT7ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8430	SBT7ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8438	SBT7ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8440	SBT7REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8450	SBT7RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8458	SBT7WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8460	SBT7REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8470	SBT7RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8478	SBT7WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8480	SBT7REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8490	SBT7RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8498	SBT7WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-17: SYSTEM BUS TARGET PROTECTION GROUP 8 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8820	SBT8ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8824	SBT8ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8828	SBT8ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT8ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT8ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT8REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8850	SBT8RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8858	SBT8WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8860	SBT8REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8870	SBT8RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8878	SBT8WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-18: SYSTEM BUS TARGET PROTECTION GROUP 9 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT9ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT9ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT9ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT9ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT9ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT9REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT9RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT9WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT9REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT9RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT9WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-19: SYSTEM BUS TARGET PROTECTION GROUP 10 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
9020	SBT10ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9024	SBT10ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9028	SBT10ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9030	SBT10ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9038	SBT10ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9040	SBT10REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9050	SBT10RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9058	SBT10WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9060	SBT10REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9070	SBT10RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9078	SBT10WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-20: SYSTEM BUS TARGET PROTECTION GROUP 11 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9420	SBT11ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9424	SBT11ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9428	SBT11ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9430	SBT11ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9438	SBT11ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9440	SBT11REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9450	SBT11RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9458	SBT11WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9460	SBT11REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9470	SBT11RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9478	SBT11WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-21: SYSTEM BUS TARGET PROTECTION GROUP 12 REGISTER MAP

Virtual Address (BF90_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
9820	SBT12ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
9824	SBT12ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9828	SBT12ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9830	SBT12ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9838	SBT12ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9840	SBT12REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9850	SBT12RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9858	SBT12WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-22: SYSTEM BUS TARGET PROTECTION GROUP 13 REGISTER MAP

Virtual Address (BF91_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8420	SBT13ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8424	SBT13ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8428	SBT13ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8430	SBT13ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8438	SBT13ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8440	SBT13REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8450	SBT13RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8458	SBT13WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8460	SBT13REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8470	SBT13RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8478	SBT13WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-23: SYSTEM BUS TARGET PROTECTION GROUP 14 REGISTER MAP

Virtual Address (BF91_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8820	SBT14ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8824	SBT14ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8828	SBT14ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT14ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT14ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT14REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8850	SBT14RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8858	SBT14WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8860	SBT14REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8870	SBT14RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8878	SBT14WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-24: SYSTEM BUS TARGET PROTECTION GROUP 15 REGISTER MAP

Virtual Address (BF91_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8C20	SBT15ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT15ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT15ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT15ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT15ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT15REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT15RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT15WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-25: SYSTEM BUS TARGET PROTECTION GROUP 16 REGISTER MAP

Virtual Address (BF92_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
C420	SBT16ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
C424	SBT16ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
C428	SBT16ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
C430	SBT16ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
C438	SBT16ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
C440	SBT16REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
C450	SBT16RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
C458	SBT16WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
C460	SBT16REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
C470	SBT16RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
C478	SBT16WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
C480	SBT16REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
C490	SBT16RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
C498	SBT16WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
C4A0	SBT16REG3	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
C4B0	SBT16RD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
C4B8	SBT16WR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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TABLE 4-25: SYSTEM BUS TARGET PROTECTION GROUP 16 REGISTER MAP (CONTINUED)

Virtual Address (BF92_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C4C0	SBT16REG4	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
C4D0	SBT16RD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
C4D8	SBT16WR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-7: System Bus Targets and Associated Protection Registers for the actual reset values.

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REGISTER 4-2: SBFLAG0: SYSTEM BUS STATUS FLAG REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	T0PGV0(1)	T3PGV	T6PGV	T2PGV	T5PGV	T4PGV	T1PGV

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-7 **Unimplemented:** Read as ‘0’

bit 6 **T0PGV0:** Target 0 (System Bus 0) Permission Group Violation Status bit(1)
1 = Target 0 (System Bus 0) is reporting a Permission Group (PG) violation
0 = Target 0 (System Bus 0) is not reporting a PG violation

bit 5 **T3PGV:** Target 3 (RAM Bank 2) Permission Group Violation Status bit
1 = Target 3 is reporting a Permission Group (PG) violation
0 = Target 3 is not reporting a PG violation

bit 4 **T6PGV:** Target 6 (EBI) Permission Group Violation Status bit
1 = Target 6 is reporting a Permission Group (PG) violation
0 = Target 6 is not reporting a PG violation

bit 3 **T2PGV:** Target 2 (RAM Bank 1) Permission Group Violation Status bit
1 = Target 2 is reporting a Permission Group (PG) violation
0 = Target 2 is not reporting a PG violation

bit 2 **T5GV:** Target 5 (DDR2 Target 1 and Target 2) Permission Group Violation Status bit
1 = Target 5 is reporting a Permission Group (PG) violation
0 = Target 5 is not reporting a PG violation

bit 1 **T4PGV:** Target 4 (DDR2 Target 0) Permission Group Violation Status bit
1 = Target 4 is reporting a Permission Group (PG) violation
0 = Target 4 is not reporting a PG violation

bit 0 **T1PGV:** Target 1 (Flash Memory) Permission Group Violation Status bit
1 = Target 1 is reporting a Permission Group (PG) violation
0 = Target 1 is not reporting a PG violation

Note 1: System Bus 0 represents an internal sub-system element and should be treated as a general System Bus violation.

Note: All errors are cleared at the source (that is, SBTxELOG1, SBTxELOG2, SBTxECLRS, or SBTxECLRM registers).

REGISTER 4-3: SBFLAG1: SYSTEM BUS STATUS FLAG REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	T0PGV1(1)	T12PGV(2)	T11PGV	T10PGV	T9PGV	T8PGV	T7PGV

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-7 **Unimplemented:** Read as ‘0’

bit 6 **T0PGV1:** Target 1 (System Bus 1) Permission Group Violation Status bit(1)
1 = Target 0 (System Bus 1) is reporting a Permission Group (PG) violation
0 = Target 0 (System Bus 1) is not reporting a PG violation

bit 5 **T12PGV:** Target Group 12 (GLCD, GPU, DDR2PHY, DDR2SFR) Permission Group Violation Status bit(2)
1 = Target group 12 is reporting a Permission Group (PG) violation
0 = Target group 12 is not reporting a PG violation

bit 4 **T11PGV:** Target 11 (PB5) Permission Group Violation Status bit
1 = Target 11 is reporting a Permission Group (PG) violation
0 = Target 11 is not reporting a PG violation

bit 3 **T10PGV:** Target 10 (PB4) Permission Group Violation Status bit
1 = Target 10 is reporting a Permission Group (PG) violation
0 = Target 10 is not reporting a PG violation

bit 2 **T9PGV:** Target 9 (PB3) Permission Group Violation Status bit
1 = Target 9 is reporting a Permission Group (PG) violation
0 = Target 9 is not reporting a PG violation

bit 1 **T8PGV:** Target 8 (PB2) Permission Group Violation Status bit
1 = Target 8 is reporting a Permission Group (PG) violation
0 = Target 8 is not reporting a PG violation

bit 0 **T7PGV:** Target 7 (PB1) Permission Group Violation Status bit
1 = Target 7 is reporting a Permission Group (PG) violation
0 = Target 7 is not reporting a PG violation

Note 1: System Bus 1 represents an internal sub-system element and should be treated as a general System Bus violation.

2: This bit reports violations on Targets 14 (GLCD), 18 (GPU), 20 (DDR2PHY), and 21 (DDR2SFR).

Note: All errors are cleared at the source (i.e., SBTxELOG1, SBTxELOG2, SBTxECLRS, or SBTxECLRM registers).

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REGISTER 4-4: SBFLAG2: SYSTEM BUS STATUS FLAG REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	T0PGV2(1)	T15PGV(2)	T14PGV	T13PGV

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3 **T0PGV2:** Target 0 (System Bus 2) Permission Group Violation Status bit(1)
1 = Target 0 (System Bus 2) is reporting a Permission Group (PG) violation
0 = Target 0 (System Bus 2) is not reporting a PG violation

bit 2 **T15PGV:** Target Group 15 (USB, Crypto, RNG, SDHC) Permission Group Violation Status bit(2)
1 = Target group 15 is reporting a Permission Group (PG) violation
0 = Target group 15 is not reporting a PG violation

bit 1 **T14PGV:** Target 14 (PB6) Permission Group Violation Status bit
1 = Target 14 is reporting a Permission Group (PG) violation
0 = Target 14 is not reporting a PG violation

bit 0 **T13PGV:** Target 13 (SQI) Permission Group Violation Status bit
1 = Target 13 is reporting a Permission Group (PG) violation
0 = Target 13 is not reporting a PG violation

Note 1: System Bus 2 represents an internal sub-system element and should be treated as a general System Bus violation.

2: This bit reports violations on Targets 10 (USB), 12 (Crypto), 13 (RNG) and 19 (SDHC).

Note: All errors are cleared at the source (i.e., SBTxELOG1, SBTxELOG2, SBTxECLRS, or SBTxECLRM registers).

REGISTER 4-5: SBFLAG3: SYSTEM BUS STATUS FLAG REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	T0PGV3(1)	T16PGV

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-2 **Unimplemented:** Read as ‘0’

bit 1 **T0PGV3:** Target 0 (System Bus 3) Permission Group Violation Status bit(1)
1 = Target 0 (System Bus 3) is reporting a Permission Group (PG) violation
0 = Target 0 (System Bus 3) is not reporting a PG violation

bit 0 **T16PGV:** Target 16 (DDR2 Target 3 and Target 4) Permission Group Violation Status bit
1 = Target 16 is reporting a Permission Group (PG) violation
0 = Target 16 is not reporting a PG violation

Note 1: System Bus 3 represents an internal sub-system element and should be treated as a general System Bus violation.

Note: All errors are cleared at the source (i.e., SBTxELOG1, SBTxELOG2, SBTxECLRS, or SBTxECLRM registers).

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REGISTER 4-6: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0, C	U-0	U-0	U-0	R/W-0, C	R/W-0, C	R/W-0, C	R/W-0, C
	MULTI	—	—	—	CODE<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	INITID<7:0>							
7:0	R-0	R-0	R-0	R-0	U-0	R-0	R-0	R-0
	REGION<3:0>				—	CMD<2:0>		

Legend:	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31 **MULTI:** Multiple Permission Violations Status bit
This bit is cleared by writing a '1'.
1 = Multiple errors have been detected
0 = No multiple errors have been detected

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CODE<3:0>:** Error Code bits
Indicates the type of error that was detected. These bits are cleared by writing a '1'.
1111 = Reserved
1101 = Reserved
•
•
•
0011 = Permission violation
0010 = Reserved
0001 = Reserved
0000 = No error

bit 23-16 **Unimplemented:** Read as '0'

Note: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

REGISTER 4-6: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13) (CONTINUED)

bit 15-8 **INITID<7:0>:** Initiator ID of Requester bits
11111111 = Reserved
.
.
.
00001111 = Reserved
00001110 = SDHC
00001101 = GPU
00001100 = GLCD
00001011 = Crypto Engine
00001010 = Flash Controller
00001001 = SQI1
00001000 = CAN2
00000111 = CAN1
00000110 = Ethernet Write
00000101 = Ethernet Read
00000100 = USB
00000011 = DMA Write
00000010 = DMA Read
00000001 = CPU
00000000 = Reserved

bit 7-4 **REGION<3:0>:** Requested Region Number bits
1111 - 0000 = Target's region that reported a permission group violation

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **CMD<2:0>:** Transaction Command of the Requester bits
111 = Reserved
110 = Reserved
101 = Write (a non-posted write)
100 = Reserved
011 = Read (a locked read caused by a Read-Modify-Write transaction)
010 = Read
001 = Write
000 = Idle

Note: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

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REGISTER 4-7: SBTxELOG2: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 2 ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	GROUP<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-3 **Unimplemented:** Read as '0'

bit 1-0 **GROUP<1:0>:** Requested Permissions Group bits
- 11 = Group 3
- 10 = Group 2
- 01 = Group 1
- 00 = Group 0

Note: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

REGISTER 4-8: SBTxECON: SYSTEM BUS TARGET 'x' ERROR CONTROL REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ERRP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ERRP:** Error Control bit
- 1 = Report protection group violation errors
- 0 = Do not report protection group violation errors

Note: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

REGISTER 4-8: SBTxECON: SYSTEM BUS TARGET 'x' ERROR CONTROL REGISTER ('x' = 0-13) (CONTINUED)

bit 23-0 **Unimplemented:** Read as '0'

Note:	Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

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REGISTER 4-9: SBTxECLRS: SYSTEM BUS TARGET 'x' SINGLE ERROR CLEAR REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Single Error on Read bit

A single error as reported via SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

REGISTER 4-10: SBTxECLRM: SYSTEM BUS TARGET 'x' MULTIPLE ERROR CLEAR REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

Note: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

REGISTER 4-10: SBTxECLRM: SYSTEM BUS TARGET 'x' MULTIPLE ERROR CLEAR REGISTER ('x' = 0-13) (CONTINUED)

bit 0 **CLEAR:** Clear Multiple Errors on Read bit

Multiple errors as reported via SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note:	Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

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REGISTER 4-11: SBTxREGy: SYSTEM BUS TARGET 'x' REGION 'y' REGISTER ('x' = 0-13; 'y' = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W0	R/W-0	R/W0	R/W-0	R/W0	R/W-0	R/W0	R/W-0
	BASE<21:14>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASE<13:6>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	U-0
	BASE<5:0>						PRI	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	SIZE<4:0>					—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-10 **BASE<21:0>:** Region Base Address bits

bit 9 **PRI:** Region Priority Level bit
`1` = Level 2
`0` = Level 1

bit 8 **Unimplemented:** Read as '`0`'

bit 7-3 **SIZE<4:0>:** Region Size bits
Permissions for a region are only active is the SIZE is non-zero.
`11111` = Region size = $2^{(SIZE-1)}$ x 1024 (bytes)
•
•
•
`00001` = Region size = $2^{(SIZE-1)}$ x 1024 (bytes)
`00000` = Region is not present

bit 2-0 **Unimplemented:** Read as '`0`'

Note 1: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-7: System Bus Targets and Associated Protection Registers for more information.

REGISTER 4-12: SBTxRDy: SYSTEM BUS TARGET 'x' REGION 'y' READ PERMISSIONS REGISTER ('x' = 0-13; 'y' = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **Group3:** Group3 Read Permissions bits
- 1 = Privilege Group 3 has read permission
- 0 = Privilege Group 3 does not have read permission

bit 2 **Group2:** Group2 Read Permissions bits
- 1 = Privilege Group 2 has read permission
- 0 = Privilege Group 2 does not have read permission

bit 1 **Group1:** Group1 Read Permissions bits
- 1 = Privilege Group 1 has read permission
- 0 = Privilege Group 1 does not have read permission

bit 0 **Group0:** Group0 Read Permissions bits
- 1 = Privilege Group 0 has read permission
- 0 = Privilege Group 0 does not have read permission

Note 1: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-7: System Bus Targets and Associated Protection Registers for more information.

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REGISTER 4-13: SBTxWRy: SYSTEM BUS TARGET 'x' REGION 'y' WRITE PERMISSIONS REGISTER ('x' = 0-13; 'y' = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **Group3:** Group 3 Write Permissions bits
1 = Privilege Group 3 has write permission
0 = Privilege Group 3 does not have write permission

bit 2 **Group2:** Group 2 Write Permissions bits
1 = Privilege Group 2 has write permission
0 = Privilege Group 2 does not have write permission

bit 1 **Group1:** Group 1 Write Permissions bits
1 = Privilege Group 1 has write permission
0 = Privilege Group 1 does not have write permission

bit 0 **Group0:** Group 0 Write Permissions bits
1 = Privilege Group 0 has write permission
0 = Privilege Group 0 does not have write permission

Note 1: Refer to Table 4-7: System Bus Targets and Associated Protection Registers for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-7: System Bus Targets and Associated Protection Registers for more information.

NOTES:

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5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The PIC32MZ DAK/DAL/DAR/DAS devices contain an internal Flash program memory for executing user code, which includes the following features:

- Two Flash banks for live update support
- Dual boot support
- Write protection for program and Boot Flash
- ECC support

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip website.

Note: In the PIC32MZ DAK/DAL/DAR/DAS devices, the Flash page size is 16 KB (4K IW) and the row size is 2 KB (512 IW).

5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0600	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	PFSWAP	BFSWAP	—	—	NVMOP<3:0>				0000
0610	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
0620	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
0630	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
0640	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
0650	NVMDATA2	31:16	NVMDATA2<31:0>																0000
		15:0																	0000
0660	NVMDATA3	31:16	NVMDATA3<31:0>																0000
		15:0																	0000
0670	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
0680	NVMPWP(1)	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
0690	NVMBWP(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LBWPULOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPULOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF
06A0	NVMCON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	00xx
		15:0	—	—	—	—	—	—	—	—	SWAPLOCK<1:0>		—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	U-0
	WR(1)	WREN(1)	WRERR(1)	LVDERR(1)	—	—	—	—
7:0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	PFSWAP(3)	BFSWAP(3,4)	—	—	NVMOP<3:0>			

Legend:	HS = Hardware Set	HC = Cleared by Hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **WR:** Write Control bit(1)

This bit cannot be cleared and can be set only when WREN = 1 and the unlock sequence has been performed.
1 = Initiate a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit(1)

1 = Enable writes to the WR bit and the SWAP bit and disables writes to the NVMOP<3:0> bits
0 = Disable writes to WR bit and the SWAP bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11-8 **Unimplemented:** Read as ‘0’

bit 7 **PFSWAP:** Program Flash Bank Swap Control bit(3)

1 = Program Flash Bank 2 is mapped to the lower mapped region and program Flash Bank 1 is mapped to the upper mapped region
0 = Program Flash Bank 1 is mapped to the lower mapped region and program Flash Bank 2 is mapped to the upper mapped region

Note 1: These bits are only Reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This operation results in a “no operation” (NOP) when the Dynamic Flash ECC Configuration bits = 00 (FECCCON<1:0> (DVCFG0<9:8>)), which enables ECC at all times. For all other FECCCON<1:0> bit settings, this command will execute, but will not write the ECC bits for the word and can cause DED errors if dynamic Flash ECC is enabled (FECCCON<1:0> = 01). Refer to **Section 52. “Flash Program Memory with Support for Live Update”** (DS60001193) for information regarding ECC and Flash programming.

3: This bit can only be modified when the WREN bit = 0, the NVMKEY unlock sequence is satisfied, and the SWAPLOCK<1:0> bits (NVMCON2<7:6>) are cleared to ‘0’.

4: The BFSWAP value is determined by the values the user programmed Sequence Numbers in each boot panel.

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER (CONTINUED)

bit 6 **BFSWAP:** Boot Flash Bank Swap Control bit(3,4)

1 = Boot Flash Bank 2 is mapped to the lower boot region and Boot Flash Bank 1 is mapped to the upper mapped region

0 = Boot Flash Bank 1 is mapped to the lower boot region and Boot Flash Bank 2 is mapped to the upper mapped region

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits

These bits are only writable when WREN = 0.

1111 = Reserved

•
•
•

1000 = Reserved

0111 = Program erase operation: erase all of program Flash memory (all pages must be unprotected, PWP<23:0> = 0x000000)

0110 = Upper program Flash memory erase operation: erases only the upper mapped region of program Flash (all pages in that region must be unprotected)

0101 = Lower program Flash memory erase operation: erases only the lower mapped region of program Flash (all pages in that region must be unprotected)

0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected

0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected

0010 = Quad Word (128-bit) program operation: programs the 128-bit Flash word selected by NVMADDR, if it is not write-protected

0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected(2)

0000 = No operation

Note 1: These bits are only Reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This operation results in a "no operation" (NOP) when the Dynamic Flash ECC Configuration bits = 00 (FECCCON<1:0> (DVCFG0<9:8>)), which enables ECC at all times. For all other FECCCON<1:0> bit settings, this command will execute, but will not write the ECC bits for the word and can cause DED errors if dynamic Flash ECC is enabled (FECCCON<1:0> = 01). Refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) for information regarding ECC and Flash programming.

3: This bit can only be modified when the WREN bit = 0, the NVMKEY unlock sequence is satisfied, and the SWAPLOCK<1:0> bits (NVMCON2<7:6>) are cleared to '0'.

4: The BFSWAP value is determined by the values the user programmed Sequence Numbers in each boot panel.

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REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** Unlock Register bits
These bits are write-only, and read as ‘0’ on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** Flash Address bits(1)

NVMOP<3:0> Selection	Flash Address Bits (NVMADDR<31:0>)
Page Erase	Address identifies the page to erase (NVMADDR<13:0> are ignored).
Row Program	Address identifies the row to program (NVMADDR<11:0> are ignored).
Word Program	Address identifies the word to program (NVMADDR<1:0> are ignored).
Quad Word Program	Address identifies the quad word (128-bit) to program (NVMADDR<3:0> bits are ignored).

Note 1: For all other NVMOP<3:0> bit settings, the Flash address is ignored.

Note: The bits in this register are only Reset by a Power-on Reset (POR) and are not affected by other reset sources.

REGISTER 5-4: NVMDATAx: FLASH DATA REGISTER (x = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATA<31:0>:** Flash Data bits
Word Program: Writes NVMDATA0 to the target Flash address defined in NVMADDR
Quad Word Program: Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the Least Significant Instruction Word.

Note: The bits in this register are only Reset by a Power-on Reset (POR) and are not affected by other reset sources.

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits
The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only Reset by a Power-on Reset (POR) and are not affected by other reset sources.

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REGISTER 5-6: NVMPWP: PROGRAM FLASH WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	PWPULOCK	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<23:16>							
15:8	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **PWPULOCK:** Program Flash Memory Page Write-protect Unlock bit
`1` = Register is not locked and can be modified
`0` = Register is locked and cannot be modified
This bit is only clearable and cannot be set except by any reset.

bit 30-24 **Unimplemented:** Read as ‘`0`’

bit 23-0 **PWP<23:0>:** Flash Program Write-protect (Page) Address bits
Physical memory below address 0x1Dxxxxxx is write protected, where ‘xxxxxx’ is specified by PWP<23:0>. When PWP<23:0> has a value of ‘`0`’, write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

REGISTER 5-7: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	LBWPULOCK	—	—	LBWP4(1)	LBWP3(1)	LBWP2(1)	LBWP1(1)	LBWP0(1)
7:0	R/W-1	r-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	UBWPULOCK	—	—	UBWP4(1)	UBWP3(1)	UBWP2(1)	UBWP1(1)	UBWP0(1)

Legend:		r = Reserved	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **LBWPULOCK:** Lower Boot Alias Write-protect Unlock bit
1 = LBWPx bits are not locked and can be modified
0 = LBWPx bits are locked and cannot be modified
This bit is only clearable and cannot be set except by any reset.

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12 **LBWP4:** Lower Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC10000 through 0x1FC13FFF enabled
0 = Write protection for physical address 0x01FC10000 through 0x1FC13FFF disabled

bit 11 **LBWP3:** Lower Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC0C000 through 0x1FC0FFFF enabled
0 = Write protection for physical address 0x01FC0C000 through 0x1FC0FFFF disabled

bit 10 **LBWP2:** Lower Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC08000 through 0x1FC0BFFF enabled
0 = Write protection for physical address 0x01FC08000 through 0x1FC0BFFF disabled

bit 9 **LBWP1:** Lower Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC04000 through 0x1FC07FFF enabled
0 = Write protection for physical address 0x01FC04000 through 0x1FC07FFF disabled

bit 8 **LBWP0:** Lower Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC00000 through 0x1FC03FFF enabled
0 = Write protection for physical address 0x01FC00000 through 0x1FC03FFF disabled

bit 7 **UBWPULOCK:** Upper Boot Alias Write-protect Unlock bit
1 = UBWPx bits are not locked and can be modified
0 = UBWPx bits are locked and cannot be modified
This bit is only user-clearable and cannot be set except by any reset.

bit 6 **Reserved:** This bit is reserved for use by development tools

bit 5 **Unimplemented:** Read as ‘0’

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

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REGISTER 5-7: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

bit 4 **UBWP4:** Upper Boot Alias Page 4 Write-protect bit(1)

1 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF enabled
0 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF disabled

bit 3 **UBWP3:** Upper Boot Alias Page 3 Write-protect bit(1)

1 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF enabled
0 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF disabled

bit 2 **UBWP2:** Upper Boot Alias Page 2 Write-protect bit(1)

1 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF enabled
0 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF disabled

bit 1 **UBWP1:** Upper Boot Alias Page 1 Write-protect bit(1)

1 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF enabled
0 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF disabled

bit 0 **UBWP0:** Upper Boot Alias Page 0 Write-protect bit(1)

1 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF enabled
0 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF disabled

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

REGISTER 5-8: NVMCON2: PROGRAMMING CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SWAPLOCK<1:0>(1)		—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-6 **SWAPLOCK<1:0>:** Program Flash Memory Page Write-protect Unlock bits(1)

11 = PFSWAP and BFSWP in the NVMCON register are Not Writable and SWAPLOCK<1:0> is Not Writable
10 = PFSWAP and BFSWP in the NVMCON register are Not Writable and SWAPLOCK<1:0> is Writable
01 = PFSWAP and BFSWP in the NVMCON register are Not Writable and SWAPLOCK<1:0> is Writable
00 = PFSWAP and BFSWP in the NVMCON register are Writable and SWAPLOCK<1:0> is Writable

bit 5-0 **Unimplemented:** Read as ‘0’

Note 1: These bits can only be modified when the NVMKEY unlock sequence is satisfied and the SWAPLOCK<1:0> bits ≠ 11. If the SWAPLOCK<1:0> bits == 11, only a Reset can clear these bits.

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6.0 RESETS

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

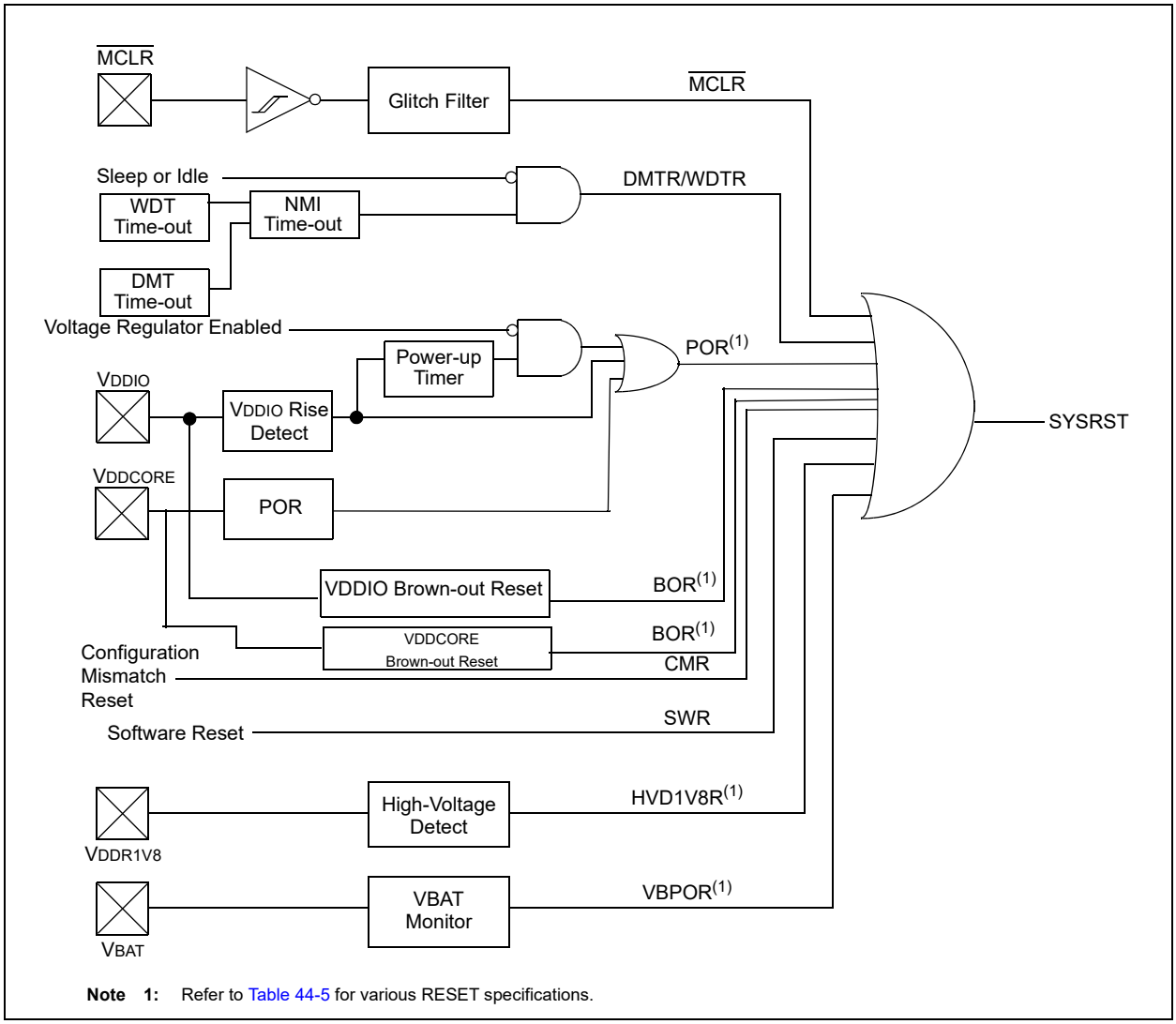
The Reset module combines all Reset sources and controls the device System Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- VBAT Power-on Reset (VBPOR)
- High Voltage Detect Reset (HVD1V8R) on V_{DDR1V8}
- Master Clear Reset pin ($\overline{MCLR}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

All types of device Reset will set a corresponding Status bit in the RCON register (see Register 6-1) to indicate the type of reset.

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



Note 1: Refer to Table 44-5 for various RESET specifications.

6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1240	RCON	31:16	—	—	HVD1V8R	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	VBPOR	VBAT	C003
		15:0	—	—	—	—	—	DPSLP	CMR	—	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR	0003
1250	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
1260	RNMICON	31:16	—	—	—	—	—	—	DMTO	WDTO	SWNMI	—	—	—	GNMI	HLVD	CF	WDTS	0000
		15:0	NMICNT<15:0>																0000
1270	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VREGS	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0, HS	U-0	RW-0, HC	R/W-0, HC	U-0	U-0
	—	—	HVD1V8R	—	BCFGERR	BCFGFAIL	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1, HS	R/W-1, HS
	—	—	—	—	—	—	VBPOR	VBAT
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0
	—	—	—	—	—	DPSLP(1)	CMR	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR(1)	POR(1)

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Reserved:** Read as ‘11’

bit 29 **HVD1V8R:** V_{DDR1V8} (DDR2) High Voltage Detect Flag bit
1 = A high voltage condition on the V_{DDR1V8} voltage has occurred
0 = A high voltage condition on the V_{DDR1V8} voltage has not occurred

bit **Unimplemented:** Read as ‘0’

bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit
1 = An error occurred during a read of the primary configuration registers
0 = No error occurred during a read of the primary configuration registers

bit 26 **BCFGFAIL:** Primary/Secondary Configuration Registers Error Flag bit
1 = An error occurred during a read of the primary and alternate configuration registers
0 = No error occurred during a read of the primary and alternate configuration registers

bit 25-18 **Unimplemented:** Read as ‘0’

bit 17 **VBPOR:** VBPOR Mode Flag bit
1 = A V_{BAT} domain POR has occurred
0 = A V_{BAT} domain POR has not occurred

bit 16 **VBAT:** VBAT Mode Flag bit
1 = A POR exit from V_{BAT} has occurred (a true POR must be established with the valid V_{BAT} voltage on the V_{BAT} pin)
0 = A POR exit from V_{BAT} has not occurred

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10 **DPSLP:** Deep Sleep Mode Flag bit(1)
1 = Deep Sleep mode has occurred
0 = Deep Sleep mode has not occurred

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **Unimplemented:** Read as ‘0’

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **DMTO:** Deadman Timer Time-out Flag bit
1 = A DMT time-out has occurred
0 = A DMT time-out has not occurred

Note 1: User software must clear this bit to view the next detection.

REGISTER 6-1: RCON: RESET CONTROL REGISTER

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view the next detection.

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REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1,2)

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as ‘0’

bit 0 **SWRST:** Software Reset Trigger bit(1,2)
1 = Enable software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to the **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

2: Once this bit is set, any read of the RSWRST register will cause a reset to occur.

REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMTO	WDTO
23:16	R/W-0	U-0	U-0	U-0	R/W-0	HS,R/W-0	R/W-0	R/W-0
	SWNMI	—	—	—	GNMI	HLVD	CF	WDTS
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **DMTO:** Deadman Timer Time-out Flag bit
1 = DMT time-out has occurred and caused a NMI
0 = DMT time-out has not occurred
Setting this bit will cause a DMT NMI event, and NMICNT will begin counting.

bit 24 **WDTO:** Watchdog Timer Time-Out Flag bit
1 = WDT time-out has occurred and caused a NMI
0 = WDT time-out has not occurred
Setting this bit will cause a WDT NMI event, and MNICNT will begin counting.

bit 23 **SWNMI:** Software NMI Trigger.
1 = An NMI will be generated
0 = An NMI will not be generated

bit 22-20 **Unimplemented:** Read as ‘0’

bit 19 **GNMI:** General NMI bit
1 = A general NMI event has been detected or a user-initiated NMI event has occurred
0 = A general NMI event has not been detected

Setting GNMI to a ‘1’ causes a user-initiated NMI event. This bit is also set by writing 0x4E to the NMIKEY<7:0> (INTCON<31:24>) bits.

bit 18 **HLVD:** High/Low-Voltage Detect bit
1 = HLVD has detected a low-voltage condition and caused an NMI
0 = HLVD has not detected a low-voltage condition
Note: When this bit is cleared inside NMI before exiting ISR the low voltage condition may still present. This low voltage condition can be checked by monitoring HLVDCON<HLEVT> inside or outside of ISR.

Note 1: If a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is cleared before this counter reaches ‘0’, no device Reset is asserted. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit is written. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

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REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

bit 17 **CF:** Clock Fail Detect bit
1 = FSCM has detected clock failure and caused an NMI
0 = FSCM has not detected clock failure

Setting this bit will cause a a CF NMI event, but will not cause a clock switch to the BFRC.

Note: On a clock fail event, if enabled by the FCKSM<1:0> bits (DEVCFG1<15:14>) = ‘0b11, this bit and the OSCCON<CF> bit will be set. The user software must clear both the bits inside the CF NMI handler before exiting the ISR. Software or hardware settings of the CF bit (OSCCON<3>) will cause a CF NMI event and an automatic clock switch to the Backup FRC (BFRC) provided the FCKSM<1:0> = 0b11. Unlike the CF bit (OSCCON<3>), software or hardware settings of the CF bit (RNMICON<17>) will cause a CF NMI event but will not cause a clock switch to the BFRC. After a Clock Fail event, a successful user software clock switch if implemented, hardware will automatically clear the CF bit (RNMICON<17>) but not the CF bit (OSCCON<3>). The CF bit (OSCCON<3>) must be cleared by software using the OSCCON register unlock procedure.

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep
0 = WDT time-out has not occurred during Sleep mode

Setting this bit will cause a WDT NMI.

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI reset counter.
1111111111111111-0000000000000001 = Number of SYSCLK cycles before a device Reset occurs(1)
0000000000000000 = No delay between NMI assertion and device Reset event

Note 1: If a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is cleared before this counter reaches ‘0’, no device Reset is asserted. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit is written. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

REGISTER 6-4: PWRCON: POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	VREGS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as ‘0’

bit 0 **VREGS:** Voltage Regulator Stand-by Enable bit
1 = Voltage regulator will remain active during Sleep
0 = Voltage regulator will go to Stand-by mode during Sleep

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7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192), which are available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The PIC32MZ DAK/DAL/DAR/DAS devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Controller module exists outside of the CPU and prioritizes the interrupt events before presenting them to the CPU.

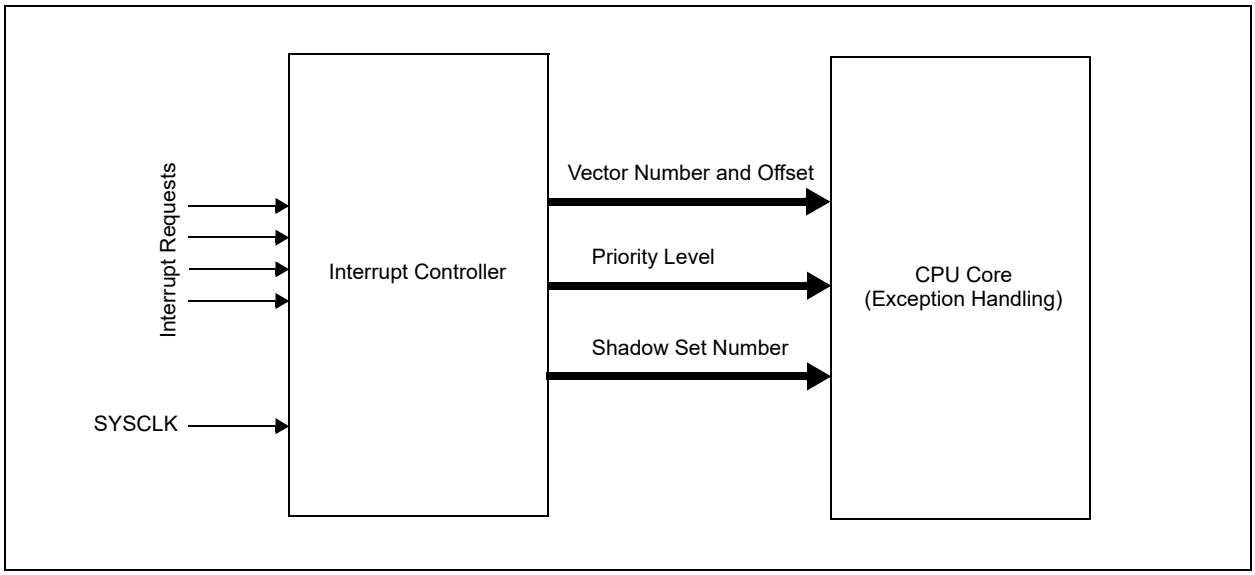
The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 "CPU Exceptions"**.

The Interrupt Controller module includes the following features:

- Up to 210 interrupt sources and vectors with dedicated programmable offsets, eliminating the need for redirection
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable sub-priority levels within each priority
- Seven shadow register sets that can be used for any priority level, eliminating software context switch and reducing interrupt latency
- Software can generate any interrupt

Figure 7-1 shows the block diagram for the Interrupt Controller and CPU exceptions.

FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM



7.1 CPU Exceptions

CPU coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® microAptiv™ MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).	0xBFC0_0000	BEV, ERL	—	—	`_on_reset`
Soft Reset	Assertion of a software Reset.	0xBFC0_0000	BEV, SR, ERL	—	—	`_on_reset`
DSS	EJTAG debug single step.	0xBFC0_0480	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480	—	DINT	—	—
NMI	Assertion of NMI signal.	0xBFC0_0000	BEV, NMI, ERL	—	—	`_nmi_handler`
Machine Check	TLB write that conflicts with an existing entry.	EBASE+0x180	MCHECK, EXL	—	0x18	`_general_exception_handler`
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2.	IPL<2:0>	—	0x00	See Table 7-2.
Deferred Watch	Deferred watch (unmasked by K|DM=>!(K|DM) transition).	EBASE+0x180	WP, EXL	—	0x17	`_general_exception_handler`
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480	—	DIB	—	—
WATCH	A reference to an address that is in one of the Watch registers (fetch).	EBASE+0x180	EXL	—	0x17	`_general_exception_handler`
AdEL	Fetch address alignment error. Fetch reference to protected address.	EBASE+0x180	EXL	—	0x04	`_general_exception_handler`
TLBL	Fetch TLB miss or fetch TLB hit to page with V = 0.	EBASE if Status.EXL = 0	—	—	0x02	—
		EBASE+0x180 if Status.EXL == 1	—	—	0x02	`_general_exception_handler`
TLBL Execute-Inhibit	An instruction fetch matched a valid TLB entry that had the XI bit set.	EBASE+0x180	EXL	—	0x14	`_general_exception_handler`
IBE	Instruction fetch bus error.	EBASE+0x180	EXL	—	0x06	`_general_exception_handler`

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TABLE 7-1: MIPS32® microAptiv™ MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Instruction Validity Exceptions	An instruction could not be completed because it was not allowed to access the required resources (Coprocessor Unusable) or was illegal (Reserved Instruction). If both exceptions occur on the same instruction, the Coprocessor Unusable Exception takes priority over the Reserved Instruction Exception.	EBASE+0x180	EXL	—	0x0A or 0x0B	`_general_exception_handler`
Execute Exception	An instruction-based exception occurred: Integer overflow, trap, system call, breakpoint, floating point, or DSP ASE state disabled exception.	EBASE+0x180	EXL	—	0x08-0x0C	`_general_exception_handler`
Tr	Execution of a trap (when trap condition is true).	EBASE+0x180	EXL	—	0x0D	`_general_exception_handler`
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).	0xBFC0_0480	—	DDBL or DDBS	—	—
WATCH	A reference to an address that is in one of the Watch registers (data).	EBASE+0x180	EXL	—	0x17	`_general_exception_handler`
AdEL	Load address alignment error. User mode load reference to kernel address.	EBASE+0x180	EXL	—	0x04	`_general_exception_handler`
AdES	Store address alignment error. User mode store to kernel address.	EBASE+0x180	EXL	—	0x05	`_general_exception_handler`
TLBL	Load TLB miss or load TLB hit to page with V = 0.	EBASE+0x180	EXL	—	0x02	`_general_exception_handler`
TLBS	Store TLB miss or store TLB hit to page with V = 0.	EBASE+0x180	EXL	—	0x03	`_general_exception_handler`
DBE	Load or store bus error.	EBASE+0x180	EXL	—	0x07	`_general_exception_handler`
DDBL	EJTAG data hardware breakpoint matched in load data compare.	0xBFC0_0480	—	DDBL	—	—
CBrk	EJTAG complex breakpoint.	0xBFC0_0480	—	DIBIMPR, DDBLIMPR, and/or DDBSIMPR	—	—
Lowest Priority						

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7.2 Interrupts

The PIC32MZ DAK/DAL/DAR/DAS family of devises use variable offsets for vector spacing. This allows the interrupt vector spacing to be configured according to application needs. A unique interrupt vector offset can be set for each vector using its associated OFFx register.

For additional information on the Variable Offset feature, refer to the **8.5.2 "Variable Offset"** in **Section 8. "Interrupt Controller"** (DS60001108) of the *"PIC32 Family Reference Manual"*.

Table 7-2 provides the Interrupt IRQ, vector and bit location information.

TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Highest Natural Order Priority								
Core Timer Interrupt	_CORE_TIMER_VECTOR	0	OFF000<17:1>	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software Interrupt 0	_CORE_SOFTWARE_0_VECTOR	1	OFF001<17:1>	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software Interrupt 1	_CORE_SOFTWARE_1_VECTOR	2	OFF002<17:1>	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External Interrupt 0	_EXTERNAL_0_VECTOR	3	OFF003<17:1>	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
Timer1	_TIMER_1_VECTOR	4	OFF004<17:1>	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
Input Capture 1 Error	_INPUT_CAPTURE_1_ERROR_VECTOR	5	OFF005<17:1>	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
Input Capture 1	_INPUT_CAPTURE_1_VECTOR	6	OFF006<17:1>	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	Yes
Output Compare 1	_OUTPUT_COMPARE_1_VECTOR	7	OFF007<17:1>	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
External Interrupt 1	_EXTERNAL_1_VECTOR	8	OFF008<17:1>	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
Timer2	_TIMER_2_VECTOR	9	OFF009<17:1>	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
Input Capture 2 Error	_INPUT_CAPTURE_2_ERROR_VECTOR	10	OFF010<17:1>	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	Yes
Input Capture 2	_INPUT_CAPTURE_2_VECTOR	11	OFF011<17:1>	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	Yes
Output Compare 2	_OUTPUT_COMPARE_2_VECTOR	12	OFF012<17:1>	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
External Interrupt 2	_EXTERNAL_2_VECTOR	13	OFF013<17:1>	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Timer3	_TIMER_3_VECTOR	14	OFF014<17:1>	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
Input Capture 3 Error	_INPUT_CAPTURE_3_ERROR_VECTOR	15	OFF015<17:1>	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	Yes
Input Capture 3	_INPUT_CAPTURE_3_VECTOR	16	OFF016<17:1>	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
Output Compare 3	_OUTPUT_COMPARE_3_VECTOR	17	OFF017<17:1>	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
External Interrupt 3	_EXTERNAL_3_VECTOR	18	OFF018<17:1>	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer4	_TIMER_4_VECTOR	19	OFF019<17:1>	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
Input Capture 4 Error	_INPUT_CAPTURE_4_ERROR_VECTOR	20	OFF020<17:1>	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
Input Capture 4	_INPUT_CAPTURE_4_VECTOR	21	OFF021<17:1>	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes
Output Compare 4	_OUTPUT_COMPARE_4_VECTOR	22	OFF022<17:1>	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	No

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

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TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
External Interrupt 4	_EXTERNAL_4_VECTOR	23	OFF023<17:1>	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	No
Timer5	_TIMER_5_VECTOR	24	OFF024<17:1>	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	No
Input Capture 5 Error	_INPUT_CAPTURE_5_ERROR_VECTOR	25	OFF025<17:1>	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	Yes
Input Capture 5	_INPUT_CAPTURE_5_VECTOR	26	OFF026<17:1>	IFS0<26>	IEC0<26>	IPC6<20:18>	IPC6<17:16>	Yes
Output Compare 5	_OUTPUT_COMPARE_5_VECTOR	27	OFF027<17:1>	IFS0<27>	IEC0<27>	IPC6<28:26>	IPC6<25:24>	No
Timer6	_TIMER_6_VECTOR	28	OFF028<17:1>	IFS0<28>	IEC0<28>	IPC7<4:2>	IPC7<1:0>	No
Input Capture 6 Error	_INPUT_CAPTURE_6_ERROR_VECTOR	29	OFF029<17:1>	IFS0<29>	IEC0<29>	IPC7<12:10>	IPC7<9:8>	Yes
Input Capture 6	_INPUT_CAPTURE_6_VECTOR	30	OFF030<17:1>	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	Yes
Output Compare 6	_OUTPUT_COMPARE_6_VECTOR	31	OFF031<17:1>	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
Timer7	_TIMER_7_VECTOR	32	OFF032<17:1>	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
Input Capture 7 Error	_INPUT_CAPTURE_7_ERROR_VECTOR	33	OFF033<17:1>	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	Yes
Input Capture 7	_INPUT_CAPTURE_7_VECTOR	34	OFF034<17:1>	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	Yes
Output Compare 7	_OUTPUT_COMPARE_7_VECTOR	35	OFF035<17:1>	IFS1<3>	IEC1<3>	IPC8<28:26>	IPC8<25:24>	No
Timer8	_TIMER_8_VECTOR	36	OFF036<17:1>	IFS1<4>	IEC1<4>	IPC9<4:2>	IPC9<1:0>	No
Input Capture 8 Error	_INPUT_CAPTURE_8_ERROR_VECTOR	37	OFF037<17:1>	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	Yes
Input Capture 8	_INPUT_CAPTURE_8_VECTOR	38	OFF038<17:1>	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	Yes
Output Compare 8	_OUTPUT_COMPARE_8_VECTOR	39	OFF039<17:1>	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	No
Timer9	_TIMER_9_VECTOR	40	OFF040<17:1>	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	No
Input Capture 9 Error	_INPUT_CAPTURE_9_ERROR_VECTOR	41	OFF041<17:1>	IFS1<9>	IEC1<9>	IPC10<12:10>	IPC10<9:8>	Yes
Input Capture 9	_INPUT_CAPTURE_9_VECTOR	42	OFF042<17:1>	IFS1<10>	IEC1<10>	IPC10<20:18>	IPC10<17:16>	Yes
Output Compare 9	_OUTPUT_COMPARE_9_VECTOR	43	OFF043<17:1>	IFS1<11>	IEC1<11>	IPC10<28:26>	IPC10<25:24>	No
ADC Global Interrupt	_ADC_VECTOR	44	OFF044<17:1>	IFS1<12>	IEC1<12>	IPC11<4:2>	IPC11<1:0>	Yes
ADC FIFO Interrupt	_ADC_FIFO_VECTOR	45	OFF045<17:1>	IFS1<13>	IEC1<13>	IPC11<12:10>	IPC11<9:8>	Yes
ADC Digital Comparator 1	_ADC_DC1_VECTOR	46	OFF046<17:1>	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
ADC Digital Comparator 2	_ADC_DC2_VECTOR	47	OFF047<17:1>	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	Yes
ADC Digital Comparator 3	_ADC_DC3_VECTOR	48	OFF048<17:1>	IFS1<16>	IEC1<16>	IPC12<4:2>	IPC12<1:0>	Yes
ADC Digital Comparator 4	_ADC_DC4_VECTOR	49	OFF049<17:1>	IFS1<17>	IEC1<17>	IPC12<12:10>	IPC12<9:8>	Yes
ADC Digital Comparator 5	_ADC_DC5_VECTOR	50	OFF050<17:1>	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	Yes
ADC Digital Comparator 6	_ADC_DC6_VECTOR	51	OFF051<17:1>	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

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TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Digital Filter 1	_ADC_DF1_VECTOR	52	OFF052<17:1>	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	Yes
ADC Digital Filter 2	_ADC_DF2_VECTOR	53	OFF053<17:1>	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
ADC Digital Filter 3	_ADC_DF3_VECTOR	54	OFF054<17:1>	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
ADC Digital Filter 4	_ADC_DF4_VECTOR	55	OFF055<17:1>	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes
ADC Digital Filter 5	_ADC_DF5_VECTOR	56	OFF056<17:1>	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
ADC Digital Filter 6	_ADC_DF6_VECTOR	57	OFF057<17:1>	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
ADC Fault	_ADC_FAULT_VECTOR	58	OFF058<17:1>	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	Yes
ADC Data 0	_ADC_DATA0_VECTOR	59	OFF059<17:1>	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
ADC Data 1	_ADC_DATA1_VECTOR	60	OFF060<17:1>	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
ADC Data 2	_ADC_DATA2_VECTOR	61	OFF061<17:1>	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
ADC Data 3	_ADC_DATA3_VECTOR	62	OFF062<17:1>	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	Yes
ADC Data 4	_ADC_DATA4_VECTOR	63	OFF063<17:1>	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	Yes
ADC Data 5	_ADC_DATA5_VECTOR	64	OFF064<17:1>	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	Yes
ADC Data 6	_ADC_DATA6_VECTOR	65	OFF065<17:1>	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
ADC Data 7	_ADC_DATA7_VECTOR	66	OFF066<17:1>	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
ADC Data 8	_ADC_DATA8_VECTOR	67	OFF067<17:1>	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
ADC Data 9	_ADC_DATA9_VECTOR	68	OFF068<17:1>	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
ADC Data 10	_ADC_DATA10_VECTOR	69	OFF069<17:1>	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
ADC Data 11	_ADC_DATA11_VECTOR	70	OFF070<17:1>	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
ADC Data 12	_ADC_DATA12_VECTOR	71	OFF071<17:1>	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
ADC Data 13	_ADC_DATA13_VECTOR	72	OFF072<17:1>	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
ADC Data 14	_ADC_DATA14_VECTOR	73	OFF073<17:1>	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
ADC Data 15	_ADC_DATA15_VECTOR	74	OFF074<17:1>	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	Yes
ADC Data 16	_ADC_DATA16_VECTOR	75	OFF075<17:1>	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	Yes
ADC Data 17	_ADC_DATA17_VECTOR	76	OFF076<17:1>	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	Yes
ADC Data 18	_ADC_DATA18_VECTOR	77	OFF077<17:1>	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	Yes
ADC Data 19	_ADC_DATA19_VECTOR	78	OFF078<17:1>	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	Yes
ADC Data 20	_ADC_DATA20_VECTOR	79	OFF079<17:1>	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	Yes
ADC Data 21	_ADC_DATA21_VECTOR	80	OFF080<17:1>	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	Yes

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

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TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 22	_ADC_DATA22_VECTOR	81	OFF081<17:1>	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	Yes
ADC Data 23	_ADC_DATA23_VECTOR	82	OFF082<17:1>	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	Yes
ADC Data 24	_ADC_DATA24_VECTOR	83	OFF083<17:1>	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	Yes
ADC Data 25	_ADC_DATA25_VECTOR	84	OFF084<17:1>	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	Yes
ADC Data 26	_ADC_DATA26_VECTOR	85	OFF085<17:1>	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	Yes
ADC Data 27	_ADC_DATA27_VECTOR	86	OFF086<17:1>	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	Yes
ADC Data 28	_ADC_DATA28_VECTOR	87	OFF087<17:1>	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	Yes
ADC Data 29	_ADC_DATA29_VECTOR	88	OFF088<17:1>	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	Yes
ADC Data 30	_ADC_DATA30_VECTOR	89	OFF089<17:1>	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	Yes
ADC Data 31	_ADC_DATA31_VECTOR	90	OFF090<17:1>	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	Yes
ADC Data 32	_ADC_DATA32_VECTOR	91	OFF091<17:1>	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	Yes
ADC Data 33	_ADC_DATA33_VECTOR	92	OFF092<17:1>	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	Yes
ADC Data 34	_ADC_DATA34_VECTOR	93	OFF093<17:1>	IFS2<29>	IEC2<29>	IPC23<12:10>	IPC23<9:8>	Yes
ADC Data 35	_ADC_DATA35_VECTOR	94	OFF094<17:1>	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
ADC Data 36	_ADC_DATA36_VECTOR	95	OFF095<17:1>	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	Yes
ADC Data 37	_ADC_DATA37_VECTOR	96	OFF096<17:1>	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	Yes
ADC Data 38	_ADC_DATA38_VECTOR	97	OFF097<17:1>	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	Yes
ADC Data 39	_ADC_DATA39_VECTOR	98	OFF098<17:1>	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	Yes
ADC Data 40	_ADC_DATA40_VECTOR	99	OFF099<17:1>	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	Yes
ADC Data 41	_ADC_DATA41_VECTOR	100	OFF100<17:1>	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	Yes
ADC Data 42	_ADC_DATA42_VECTOR	101	OFF101<17:1>	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	Yes
ADC Data 43	_ADC_DATA43_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
USB Suspend/Resume Event	_USB_SR_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	No
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
Core Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes
System Bus Protection Violation	_SYSTEM_BUS_PROTECTION_VECTOR	106	OFF106<17:1>	IFS3<10>	IEC3<10>	IPC26<20:18>	IPC26<17:16>	Yes
Crypto Engine Event	_CRYPTO_VECTOR	107	OFF107<17:1>	IFS3<11>	IEC3<11>	IPC26<28:26>	IPC26<25:24>	Yes
Reserved	—	108	—	—	—	—	—	—
SPI1 Fault	_SPI1_FAULT_VECTOR	109	OFF109<17:1>	IFS3<13>	IEC3<13>	IPC27<12:10>	IPC27<9:8>	Yes

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TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
SPI1 Receive Done	_SPI1_RX_VECTOR	110	OFF110<17:1>	IFS3<14>	IEC3<14>	IPC27<20:18>	IPC27<17:16>	Yes
SPI1 Transfer Done	_SPI1_TX_VECTOR	111	OFF111<17:1>	IFS3<15>	IEC3<15>	IPC27<28:26>	IPC27<25:24>	Yes
UART1 Fault	_UART1_FAULT_VECTOR	112	OFF112<17:1>	IFS3<16>	IEC3<16>	IPC28<4:2>	IPC28<1:0>	Yes
UART1 Receive Done	_UART1_RX_VECTOR	113	OFF113<17:1>	IFS3<17>	IEC3<17>	IPC28<12:10>	IPC28<9:8>	Yes
UART1 Transfer Done	_UART1_TX_VECTOR	114	OFF114<17:1>	IFS3<18>	IEC3<18>	IPC28<20:18>	IPC28<17:16>	Yes
I2C1 Bus Collision Event	_I2C1_BUS_VECTOR	115	OFF115<17:1>	IFS3<19>	IEC3<19>	IPC28<28:26>	IPC28<25:24>	Yes
I2C1 Client Event	_I2C1_CLIENT_VECTOR	116	OFF116<17:1>	IFS3<20>	IEC3<20>	IPC29<4:2>	IPC29<1:0>	Yes
I2C1 Host Event	_I2C1_HOST_VECTOR	117	OFF117<17:1>	IFS3<21>	IEC3<21>	IPC29<12:10>	IPC29<9:8>	Yes
PORTA Input Change Interrupt	_CHANGE_NOTICE_A_VECTOR	118	OFF118<17:1>	IFS3<22>	IEC3<22>	IPC29<20:18>	IPC29<17:16>	Yes
PORTB Input Change Interrupt	_CHANGE_NOTICE_B_VECTOR	119	OFF119<17:1>	IFS3<23>	IEC3<23>	IPC29<28:26>	IPC29<25:24>	Yes
PORTC Input Change Interrupt	_CHANGE_NOTICE_C_VECTOR	120	OFF120<17:1>	IFS3<24>	IEC3<24>	IPC30<4:2>	IPC30<1:0>	Yes
PORTD Input Change Interrupt	_CHANGE_NOTICE_D_VECTOR	121	OFF121<17:1>	IFS3<25>	IEC3<25>	IPC30<12:10>	IPC30<9:8>	Yes
PORTE Input Change Interrupt	_CHANGE_NOTICE_E_VECTOR	122	OFF122<17:1>	IFS3<26>	IEC3<26>	IPC30<20:18>	IPC30<17:16>	Yes
PORTF Input Change Interrupt	_CHANGE_NOTICE_F_VECTOR	123	OFF123<17:1>	IFS3<27>	IEC3<27>	IPC30<28:26>	IPC30<25:24>	Yes
PORTG Input Change Interrupt	_CHANGE_NOTICE_G_VECTOR	124	OFF124<17:1>	IFS3<28>	IEC3<28>	IPC31<4:2>	IPC31<1:0>	Yes
PORTH Input Change Interrupt	_CHANGE_NOTICE_H_VECTOR	125	OFF125<17:1>	IFS3<29>	IEC3<29>	IPC31<12:10>	IPC31<9:8>	Yes
PORTJ Input Change Interrupt	_CHANGE_NOTICE_J_VECTOR	126	OFF126<17:1>	IFS3<30>	IEC3<30>	IPC31<20:18>	IPC31<17:16>	Yes
PORTK Input Change Interrupt	_CHANGE_NOTICE_K_VECTOR	127	OFF127<17:1>	IFS3<31>	IEC3<31>	IPC31<28:26>	IPC31<25:24>	Yes
PMP	_PMP_VECTOR	128	OFF128<17:1>	IFS4<0>	IEC4<0>	IPC32<4:2>	IPC32<1:0>	Yes
PMP Error	_PMP_ERROR_VECTOR	129	OFF129<17:1>	IFS4<1>	IEC4<1>	IPC32<12:10>	IPC32<9:8>	Yes
Comparator 1 Interrupt	_COMPARATOR_1_VECTOR	130	OFF130<17:1>	IFS4<2>	IEC4<2>	IPC32<20:18>	IPC32<17:16>	No
Comparator 2 Interrupt	_COMPARATOR_2_VECTOR	131	OFF131<17:1>	IFS4<3>	IEC4<3>	IPC32<28:26>	IPC32<25:24>	No
USB General Event	_USB_VECTOR	132	OFF132<17:1>	IFS4<4>	IEC4<4>	IPC33<4:2>	IPC33<1:0>	Yes
USB DMA Event	_USB_DMA_VECTOR	133	OFF133<17:1>	IFS4<5>	IEC4<5>	IPC33<12:10>	IPC33<9:8>	Yes
DMA Channel 0	_DMA0_VECTOR	134	OFF134<17:1>	IFS4<6>	IEC4<6>	IPC33<20:18>	IPC33<17:16>	No
DMA Channel 1	_DMA1_VECTOR	135	OFF135<17:1>	IFS4<7>	IEC4<7>	IPC33<28:26>	IPC33<25:24>	No
DMA Channel 2	_DMA2_VECTOR	136	OFF136<17:1>	IFS4<8>	IEC4<8>	IPC34<4:2>	IPC34<1:0>	No
DMA Channel 3	_DMA3_VECTOR	137	OFF137<17:1>	IFS4<9>	IEC4<9>	IPC34<12:10>	IPC34<9:8>	No
DMA Channel 4	_DMA4_VECTOR	138	OFF138<17:1>	IFS4<10>	IEC4<10>	IPC34<20:18>	IPC34<17:16>	No

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TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
DMA Channel 5	_DMA5_VECTOR	139	OFF139<17:1>	IFS4<11>	IEC4<11>	IPC34<28:26>	IPC34<25:24>	No
DMA Channel 6	_DMA6_VECTOR	140	OFF140<17:1>	IFS4<12>	IEC4<12>	IPC35<4:2>	IPC35<1:0>	No
DMA Channel 7	_DMA7_VECTOR	141	OFF141<17:1>	IFS4<13>	IEC4<13>	IPC35<12:10>	IPC35<9:8>	No
SPI2 Fault	_SPI2_FAULT_VECTOR	142	OFF142<17:1>	IFS4<14>	IEC4<14>	IPC35<20:18>	IPC35<17:16>	Yes
SPI2 Receive Done	_SPI2_RX_VECTOR	143	OFF143<17:1>	IFS4<15>	IEC4<15>	IPC35<28:26>	IPC35<25:24>	Yes
SPI2 Transfer Done	_SPI2_TX_VECTOR	144	OFF144<17:1>	IFS4<16>	IEC4<16>	IPC36<4:2>	IPC36<1:0>	Yes
UART2 Fault	_UART2_FAULT_VECTOR	145	OFF145<17:1>	IFS4<17>	IEC4<17>	IPC36<12:10>	IPC36<9:8>	Yes
UART2 Receive Done	_UART2_RX_VECTOR	146	OFF146<17:1>	IFS4<18>	IEC4<18>	IPC36<20:18>	IPC36<17:16>	Yes
UART2 Transfer Done	_UART2_TX_VECTOR	147	OFF147<17:1>	IFS4<19>	IEC4<19>	IPC36<28:26>	IPC36<25:24>	Yes
I2C2 Bus Collision Event	_I2C2_BUS_VECTOR	148	OFF148<17:1>	IFS4<20>	IEC4<20>	IPC37<4:2>	IPC37<1:0>	Yes
I2C2 Client Event	_I2C2_CLIENT_VECTOR	149	OFF149<17:1>	IFS4<21>	IEC4<21>	IPC37<12:10>	IPC37<9:8>	Yes
I2C2 Host Event	_I2C2_HOST_VECTOR	150	OFF150<17:1>	IFS4<22>	IEC4<22>	IPC37<20:18>	IPC37<17:16>	Yes
Control Area Network 1	_CAN1_VECTOR	151	OFF151<17:1>	IFS4<23>	IEC4<23>	IPC37<28:26>	IPC37<25:24>	Yes
Control Area Network 2	_CAN2_VECTOR	152	OFF152<17:1>	IFS4<24>	IEC4<24>	IPC38<4:2>	IPC38<1:0>	Yes
Ethernet Interrupt	_ETHERNET_VECTOR	153	OFF153<17:1>	IFS4<25>	IEC4<25>	IPC38<12:10>	IPC38<9:8>	Yes
SPI3 Fault	_SPI3_FAULT_VECTOR	154	OFF154<17:1>	IFS4<26>	IEC4<26>	IPC38<20:18>	IPC38<17:16>	Yes
SPI3 Receive Done	_SPI3_RX_VECTOR	155	OFF155<17:1>	IFS4<27>	IEC4<27>	IPC38<28:26>	IPC38<25:24>	Yes
SPI3 Transfer Done	_SPI3_TX_VECTOR	156	OFF156<17:1>	IFS4<28>	IEC4<28>	IPC39<4:2>	IPC39<1:0>	Yes
UART3 Fault	_UART3_FAULT_VECTOR	157	OFF157<17:1>	IFS4<29>	IEC4<29>	IPC39<12:10>	IPC39<9:8>	Yes
UART3 Receive Done	_UART3_RX_VECTOR	158	OFF158<17:1>	IFS4<30>	IEC4<30>	IPC39<20:18>	IPC39<17:16>	Yes
UART3 Transfer Done	_UART3_TX_VECTOR	159	OFF159<17:1>	IFS4<31>	IEC4<31>	IPC39<28:26>	IPC39<25:24>	Yes
I2C3 Bus Collision Event	_I2C3_BUS_VECTOR	160	OFF160<17:1>	IFS5<0>	IEC5<0>	IPC40<4:2>	IPC40<1:0>	Yes
I2C3 Client Event	_I2C3_CLIENT_VECTOR	161	OFF161<17:1>	IFS5<1>	IEC5<1>	IPC40<12:10>	IPC40<9:8>	Yes
I2C3 Host Event	_I2C3_HOST_VECTOR	162	OFF162<17:1>	IFS5<2>	IEC5<2>	IPC40<20:18>	IPC40<17:16>	Yes
SPI4 Fault	_SPI4_FAULT_VECTOR	163	OFF163<17:1>	IFS5<3>	IEC5<3>	IPC40<28:26>	IPC40<25:24>	Yes
SPI4 Receive Done	_SPI4_RX_VECTOR	164	OFF164<17:1>	IFS5<4>	IEC5<4>	IPC41<4:2>	IPC41<1:0>	Yes
SPI4 Transfer Done	_SPI4_TX_VECTOR	165	OFF165<17:1>	IFS5<5>	IEC5<5>	IPC41<12:10>	IPC41<9:8>	Yes
Real Time Clock	_RTCC_VECTOR	166	OFF166<17:1>	IFS5<6>	IEC5<6>	IPC41<20:18>	IPC41<17:16>	No
Flash Control Event	_FLASH_CONTROL_VECTOR	167	OFF167<17:1>	IFS5<7>	IEC5<7>	IPC41<28:26>	IPC41<25:24>	No

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TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Prefetch Module SEC Event	_PREFETCH_VECTOR	168	OFF168<17:1>	IFS5<8>	IEC5<8>	IPC42<4:2>	IPC42<1:0>	Yes
SQI1 Event	_SQI1_VECTOR	169	OFF169<17:1>	IFS5<9>	IEC5<9>	IPC42<12:10>	IPC42<9:8>	Yes
UART4 Fault	_UART4_FAULT_VECTOR	170	OFF170<17:1>	IFS5<10>	IEC5<10>	IPC42<20:18>	IPC42<17:16>	Yes
UART4 Receive Done	_UART4_RX_VECTOR	171	OFF171<17:1>	IFS5<11>	IEC5<11>	IPC42<28:26>	IPC42<25:24>	Yes
UART4 Transfer Done	_UART4_TX_VECTOR	172	OFF172<17:1>	IFS5<12>	IEC5<12>	IPC43<4:2>	IPC43<1:0>	Yes
I2C4 Bus Collision Event	_I2C4_BUS_VECTOR	173	OFF173<17:1>	IFS5<13>	IEC5<13>	IPC43<12:10>	IPC43<9:8>	Yes
I2C4 Client Event	_I2C4_CLIENT_VECTOR	174	OFF174<17:1>	IFS5<14>	IEC5<14>	IPC43<20:18>	IPC43<17:16>	Yes
I2C4 Host Event	_I2C4_HOST_VECTOR	175	OFF175<17:1>	IFS5<15>	IEC5<15>	IPC43<28:26>	IPC43<25:24>	Yes
SPI5 Fault	_SPI5_FAULT_VECTOR	176	OFF176<17:1>	IFS5<16>	IEC5<16>	IPC44<4:2>	IPC44<1:0>	Yes
SPI5 Receive Done	_SPI5_RX_VECTOR	177	OFF177<17:1>	IFS5<17>	IEC5<17>	IPC44<12:10>	IPC44<9:8>	Yes
SPI5 Transfer Done	_SPI5_TX_VECTOR	178	OFF178<17:1>	IFS5<18>	IEC5<18>	IPC44<20:18>	IPC44<17:16>	Yes
UART5 Fault	_UART5_FAULT_VECTOR	179	OFF179<17:1>	IFS5<19>	IEC5<19>	IPC44<28:26>	IPC44<25:24>	Yes
UART5 Receive Done	_UART5_RX_VECTOR	180	OFF180<17:1>	IFS5<20>	IEC5<20>	IPC45<4:2>	IPC45<1:0>	Yes
UART5 Transfer Done	_UART5_TX_VECTOR	181	OFF181<17:1>	IFS5<21>	IEC5<21>	IPC45<12:10>	IPC45<9:8>	Yes
I2C5 Bus Collision Event	_I2C5_BUS_VECTOR	182	OFF182<17:1>	IFS5<22>	IEC5<22>	IPC45<20:18>	IPC45<17:16>	Yes
I2C5 Client Event	_I2C5_CLIENT_VECTOR	183	OFF183<17:1>	IFS5<23>	IEC5<23>	IPC45<28:26>	IPC45<25:24>	Yes
I2C5 Host Event	_I2C5_HOST_VECTOR	184	OFF184<17:1>	IFS5<24>	IEC5<24>	IPC46<4:2>	IPC46<1:0>	Yes
SPI6 Fault	_SPI6_FAULT_VECTOR	185	OFF185<17:1>	IFS5<25>	IEC5<25>	IPC46<12:10>	IPC46<9:8>	Yes
SPI6 Receive Done	_SPI6_RX_VECTOR	186	OFF186<17:1>	IFS5<26>	IEC5<26>	IPC46<20:18>	IPC46<17:16>	Yes
SPI6 Transfer Done	_SPI6_TX_VECTOR	187	OFF187<17:1>	IFS5<27>	IEC5<27>	IPC46<28:26>	IPC46<25:24>	Yes
UART6 Fault	_UART6_FAULT_VECTOR	188	OFF188<17:1>	IFS5<28>	IEC5<28>	IPC47<4:2>	IPC47<1:0>	Yes
UART6 Receive Done	_UART6_RX_VECTOR	189	OFF189<17:1>	IFS5<29>	IEC5<29>	IPC47<12:10>	IPC47<9:8>	Yes
UART6 Transfer Done	_UART6_TX_VECTOR	190	OFF190<17:1>	IFS5<30>	IEC5<30>	IPC47<20:18>	IPC47<17:16>	Yes
SDHC Interrupt	_SDHC_VECTOR	191	OFF191<17:1>	IFS5<31>	IEC5<31>	IPC47<28:26>	IPC47<25:24>	Yes
GLCD Interrupt	_GLCD_VECTOR	192	OFF192<17:1>	IFS6<0>	IEC6<0>	IPC48<4:2>	IPC48<1:0>	Yes/No(2)
GPU Interrupt	_GPU_VECTOR	193	OFF193<17:1>	IFS6<1>	IEC6<1>	IPC48<12:10>	IPC48<9:8>	Yes
Reserved	—	—	—	—	—	—	—	—
CTMU Interrupt	_CTMU_VECTOR	195	OFF195<17:1>	IFS6<3>	IEC6<3>	IPC48<28:26>	IPC48<25:24>	Yes
ADC End of Scan	_ADC_EOS_VECTOR	196	OFF196<17:1>	IFS6<4>	IEC6<4>	IPC49<4:2>	IPC49<1:0>	Yes

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

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TABLE 7-2: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Analog Circuit Ready	_ADC_ARDY_VECTOR	197	OFF197<17:1>	IFS6<5>	IEC6<5>	IPC49<12:10>	IPC49<9:8>	Yes
ADC Update Ready	_ADC_URDY_VECTOR	198	OFF198<17:1>	IFS6<6>	IE6<6>	IPC49<20:18>	IPC49<17:16>	Yes
ADC0 Early Interrupt	_ADC0_EARLY_VECTOR	199	OFF199<17:1>	IFS6<7>	IEC6<7>	IPC49<28:26>	IPC49<25:24>	Yes
ADC1 Early Interrupt	_ADC1_EARLY_VECTOR	200	OFF200<17:1>	IFS6<8>	IEC6<8>	IPC50<4:2>	IPC50<1:0>	Yes
ADC2 Early Interrupt	_ADC2_EARLY_VECTOR	201	OFF201<17:1>	IFS6<9>	IEC6<9>	IPC50<12:10>	IPC50<9:8>	Yes
ADC3 Early Interrupt	_ADC3_EARLY_VECTOR	202	OFF202<17:1>	IFS6<10>	IEC6<10>	IPC50<20:18>	IPC50<17:16>	Yes
ADC4 Early Interrupt	_ADC4_EARLY_VECTOR	203	OFF203<17:1>	IFS6<11>	IEC6<11>	IPC50<28:26>	IPC50<25:24>	Yes
Reserved	—	—	—	—	—	—	—	—
ADC Group Early Interrupt Request	_ADC_EARLY_VECTOR	205	OFF205<17:1>	IFS6<13>	IEC6<13>	IPC51<12:10>	IPC51<9:8>	Yes
ADC7 Early Interrupt	_ADC7_EARLY_VECTOR	206	OFF206<17:1>	IFS6<14>	IEC6<14>	IPC51<20:18>	IPC51<17:16>	Yes
ADC0 Warm Interrupt	_ADC0_WARM_VECTOR	207	OFF207<17:1>	IFS6<15>	IEC6<15>	IPC51<28:26>	IPC51<25:24>	Yes
ADC1 Warm Interrupt	_ADC1_WARM_VECTOR	208	OFF208<17:1>	IFS6<16>	IEC6<16>	IPC52<4:2>	IPC52<1:0>	Yes
ADC2 Warm Interrupt	_ADC2_WARM_VECTOR	209	OFF209<17:1>	IFS6<17>	IEC6<17>	IPC52<12:10>	IPC52<9:8>	Yes
ADC3 Warm Interrupt	_ADC3_WARM_VECTOR	210	OFF210<17:1>	IFS6<18>	IEC6<18>	IPC52<20:18>	IPC52<17:16>	Yes
ADC4 Warm Interrupt	_ADC4_WARM_VECTOR	211	OFF211<17:1>	IFS6<19>	IEC6<19>	IPC52<28:26>	IPC52<25:24>	Yes
Reserved	—	—	—	—	—	—	—	—
Reserved	—	—	—	—	—	—	—	—
ADC7 Warm Interrupt	_ADC7_WARM_VECTOR	214	OFF214<17:1>	IFS6<22>	IEC6<22>	IPC53<20:18>	IPC53<17:16>	Yes
MPLL Fault Interrupt	_MPLL_FAULT_VECTOR	215	OFF215<17:1>	IFS6<23>	IEC6<23>	IPC53<28:26>	IPC53<25:24>	Yes
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See the Family Features tables (Table 1 through Table 2) for the list of available peripherals.

2: Upon Reset, the GLCD interrupt (both HSYNC and VSYNC) are persistent. However, through the IRQCON bit (GLCDINT<31>), the type of interrupt can be changed to non-persistent.

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7.3 Interrupt Control Registers

TABLE 7-3: INTERRUPT REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	INTCON	31:16	NMIKEY<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
0010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
0020	INT-STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
0030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
0040	IFS0	31:16	OC6IF	IC6IF	IC6EIF	T6IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
0050	IFS1	31:16	ADCD4IF	ADCD3IF	ADCD2IF	ADCD1IF	ADCD0IF	ADCFLTIF	ADCDF6IF	ADCDF5IF	ADCDF4IF	ADCDF3IF	ADCDF21IF	ADCDF1IF	ADCDC6IF	ADCDC5IF	ADCDC4IF	ADCDC3IF	0000
		15:0	ADCDC2IF	ADCDC1IF	ADCFIFOIF	ADCIF	OC9IF	IC9IF	IC9EIF	T9IF	OC8IF	IC8IF	IC8EIF	T8IF	OC7IF	IC7IF	IC7EIF	T7IF	0000
0060	IFS2	31:16	ADCD36IF	ADCD35IF	ADCD34IF	ADCD33IF	ADCD32IF	ADCD31IF	ADCD30IF	ADCD29IF	ADCD28IF	ADCD27IF	ADCD26IF	ADCD25IF	ADCD24IF	ADCD23IF	ADCD22IF	ADCD21IF	0000
		15:0	ADCD20IF	ADCD19IF	ADCD18IF	ADCD17IF	ADCD16IF	ADCD15IF	ADCD14IF	ADCD13IF	ADCD12IF	ADCD11IF	ADCD10IF	ADCD9IF	ADCD8IF	ADCD7IF	ADCD6IF	ADCD5IF	0000
0070	IFS3	31:16	CNKIF	CNJIF	CNHIF	CNGIF	CNFIF	CNEIF	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	0000
		15:0	SPI1TXIF	SPI1RXIF	SPI1EIF	—	CRPTIF(2)	SBIF	CFDCIF	CPCIF	USBSRIF	ADCD43IF	ADCD42IF	ADCD41IF	ADCD40IF	ADCD39IF	ADCD38IF	ADCD37IF	0000
0080	IFS4	31:16	U3TXIF	U3RXIF	U3EIF	SPI3TXIF	SPI3RXIF	SPI3EIF	ETHIF	CAN2IF	CAN1IF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	0000
		15:0	SPI2RXIF	SPI2EIF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	USBDMAIF	USBIF	CMP2IF	CMP1IF	PMPEIF	PMPIF	0000
0090	IFS5	31:16	SDHCIF	U6TXIF	U6RXIF	U6EIF	SPI6TX	SPI6RXIF	SPI6IF	I2C5MIF	I2C5SIF	I2C5BIF	U5TXIF	U5RXIF	U5EIF	SPI5TXIF	SPI5RXIF	SPI5EIF	0000
		15:0	I2C4MIF	I2C4SIF	I2C4BIF	U4TXIF	U4RXIF	U4EIF	SQI1IF	PREIF	FCEIF	RTCCIF	SPI4TXIF	SPI4RXIF	SPI4EIF	I2C3MIF	I2C3SIF	I2C3BIF	0000
00A0	IFS6	31:16	—	—	—	—	—	—	—	—	MPLLFLTIF	ADC7WIF	—	—	ADC4WIF	ADC3WIF	ADC2WIF	ADC1WIF	0000
		15:0	ADC0WIF	ADC7EIF	ADCGRPIF	—	ADC4EIF	ADC3EIF	ADC2EIF	ADC1EIF	ADC0EIF	ADCURDYIF	ADCARDYIF	ADCEOSIF	CTMUIF	—	GPUIF	GLCDIF	0000
00C0	IEC0	31:16	OC6IE	IC6IE	IC6EIE	T6IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
00D0	IEC1	31:16	ADCD4IE	ADCD3IE	ADCD2IE	ADCD1IE	ADCD0IE	ADCFLTIE	ADCDF6IE	ADCDF5IE	ADCDF4IE	ADCDF3IE	ADCDF2IE	ADCDF1IE	ADCDC6IE	ADCDC5IE	ADCDC4IE	ADCDC3IE	0000
		15:0	ADCDC2IE	ADCDC1IE	ADCFIFOIE	ADCIE	OC9IE	IC9IE	IC9EIE	T9IE	OC8IE	IC8IE	IC8EIE	T8IE	OC7IE	IC7IE	IC7EIE	T7IE	0000
00E0	IEC2	31:16	ADCD36IE	ADCD35IE	ADCD34IE	ADCD33IE	ADCD32IE	ADCD31IE	ADCD30IE	ADCD29IE	ADCD28IE	ADCD27IE	ADCD26IE	ADCD25IE	ADCD24IE	ADCD23IE	ADCD22IE	ADCD21IE	0000
		15:0	ADCD20IE	ADCD19IE	ADCD18IE	ADCD17IE	ADCD16IE	ADCD15IE	ADCD14IE	ADCD13IE	ADCD12IE	ADCD11IE	ADCD10IE	ADCD9IE	ADCD8IE	ADCD7IE	ADCD6IE	ADCD5IE	0000
00F0	IEC3	31:16	CNKIE	CNJIE	CNHIE	CNGIE	CNFIE	CNEIE	CNDIE	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	0000
		15:0	SPI1TXIE	SPI1RXIE	SPI1EIE	—	CRPTIE(2)	SBIE	CFDCIE	CPCIE	USBSRIE	ADCD43IE	ADCD42IE	ADCD41IE	ADCD40IE	ADCD39IE	ADCD38IE	ADCD37IE	0000
0100	IEC4	31:16	U3TXIE	U3RXIE	U3EIE	SPI3TXIE	SPI3RXIE	SPI3EIE	ETHIE	CAN2IE	CAN1IE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	0000
		15:0	SPI2RXIE	SPI2EIE	DMA7IE	DMA6IE	DMA5IE	DMA4IE	DMA3IE	DMA2IE	DMA1IE	DMA0IE	USBDMAIE	USBIE	CMP2IE	CMP1IE	PMPEIE	PMPIE	0000
0110	IEC5	31:16	SDHCIE	U6TXIE	U6RXIE	U6EIE	SPI6TXIE	SPI6RXIE	SPI6IE	I2C5MIE	I2C5SIE	I2C5BIE	U5TXIE	U5RXIE	U5EIE	SPI5TXIE	SPI5RXIE	SPI5EIE	0000
		15:0	I2C4MIE	I2C4SIE	I2C4BIE	U4TXIE	U4RXIE	U4EIE	SQI1IE	PREIE	FCEIE	RTCCIE	SPI4TXIE	SPI4RXIE	SPI4EIE	I2C3MIE	I2C3SIE	I2C3BIE	0000
0120	IEC6	31:16	—	—	—	—	—	—	—	—	MPLLFLTIE	ADC7WIE	—	—	ADC4WIE	ADC3WIE	ADC2WIE	ADC1WIE	0000
		15:0	ADC0WIE	ADC7EIE	ADCGRPIE	—	ADC4EIE	ADC3EIE	ADC2EIE	ADC1EIE	ADC0EIE	ADCURDYIE	ADCARDYIE	ADCEOSIE	CTMUIE	—	GPUIE	GLCDIE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is only available on devices with a Crypto module.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0140	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
0150	IPC1	31:16	—	—	—	OC1IP<2:0>			OC1IS<1:0>		—	—	—	IC1IP<2:0>			IC1IS<1:0>		0000
		15:0	—	—	—	IC1EIP<2:0>			IC1EIS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
0160	IPC2	31:16	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	IC2EIP<2:0>			IC2EIS<1:0>		0000
		15:0	—	—	—	T2IP<2:0>			T2IS<1:0>		—	—	—	INT1IP<2:0>			INT1IS<1:0>		0000
0170	IPC3	31:16	—	—	—	IC3EIP<2:0>			IC3EIS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
		15:0	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
0180	IPC4	31:16	—	—	—	T4IP<2:0>			T4IS<1:0>		—	—	—	INT3IP<2:0>			INT3IS<1:0>		0000
		15:0	—	—	—	OC3IP<2:0>			OC3IS<1:0>		—	—	—	IC3IP<2:0>			IC3IS<1:0>		0000
0190	IPC5	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	IC4EIP<2:0>			IC4EIS<1:0>		0000
01A0	IPC6	31:16	—	—	—	OC5IP<2:0>			OC5IS<1:0>		—	—	—	IC5IP<2:0>			IC5IS<1:0>		0000
		15:0	—	—	—	IC5EIP<2:0>			IC5EIS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000
01B0	IPC7	31:16	—	—	—	OC6IP<2:0>			OC6IS<1:0>		—	—	—	IC6IP<2:0>			IC6IS<1:0>		0000
		15:0	—	—	—	IC6EIP<2:0>			IC6EIS<1:0>		—	—	—	T6IP<2:0>			T6IS<1:0>		0000
01C0	IPC8	31:16	—	—	—	OC7IP<2:0>			OC7IS<1:0>		—	—	—	IC7IP<2:0>			IC7IS<1:0>		0000
		15:0	—	—	—	IC7EIP<2:0>			IC7EIS<1:0>		—	—	—	T7IP<2:0>			T7IS<1:0>		0000
01D0	IPC9	31:16	—	—	—	OC8IP<2:0>			OC8IS<1:0>		—	—	—	IC8IP<2:0>			IC8IS<1:0>		0000
		15:0	—	—	—	IC8EIP<2:0>			IC8EIS<1:0>		—	—	—	T8IP<2:0>			T8IS<1:0>		0000
01E0	IPC10	31:16	—	—	—	OC9IP<2:0>			OC9IS<1:0>		—	—	—	IC9IP<2:0>			IC9IS<1:0>		0000
		15:0	—	—	—	IC9EIP<2:0>			IC9EIS<1:0>		—	—	—	T9IP<2:0>			T9IS<1:0>		0000
01F0	IPC11	31:16	—	—	—	ADCDC2IP<2:0>			ADCDC2IS<1:0>		—	—	—	ADCDC1IP<2:0>			ADCDC1IS<1:0>		0000
		15:0	—	—	—	ADCFIFOIP<2:0>			ADCFIFOIS<1:0>		—	—	—	ADCIP<2:0>			ADCIS<1:0>		0000
0200	IPC12	31:16	—	—	—	ADCDC6IP<2:0>			ADCDC6S<1:0>		—	—	—	ADCDC5IP<2:0>			ADCDC5IS<1:0>		0000
		15:0	—	—	—	ADCDC4IP<2:0>			ADCDC4IS<1:0>		—	—	—	ADCDC3IP<2:0>			ADCDC3IS<1:0>		0000
0210	IPC13	31:16	—	—	—	ADCDF4IP<2:0>			ADCDF4IS<1:0>		—	—	—	ADCDF3IP<2:0>			ADCDF3IS<1:0>		0000
		15:0	—	—	—	ADCDF2IP<2:0>			ADCDF2IS<1:0>		—	—	—	ADCDF1IP<2:0>			ADCDF1IS<1:0>		0000
0220	IPC14	31:16	—	—	—	ADCD0IP<2:0>			ADCD0IS<1:0>		—	—	—	ADCFLTIP<2:0>			ADCFLTIS<1:0>		0000
		15:0	—	—	—	ADCDF6IP<2:0>			ADCDF6IS<1:0>		—	—	—	ADCDF5IP<2:0>			ADCDF5IS<1:0>		0000
0230	IPC15	31:16	—	—	—	ADCD4IP<2:0>			ADCD4IS<1:0>		—	—	—	ADCD3IP<2:0>			ADCD3IS<1:0>		0000
		15:0	—	—	—	ADCD2IP<2:0>			ADCD2IS<1:0>		—	—	—	ADCD1IP<2:0>			ADCD1IS<1:0>		0000
0240	IPC16	31:16	—	—	—	ADCD8IP<2:0>			ADCD8IS<1:0>		—	—	—	ADCD7IP<2:0>			ADCD7IS<1:0>		0000
		15:0	—	—	—	ADCD6IP<2:0>			ADCD6IS<1:0>		—	—	—	ADCD5IP<2:0>			ADCD5IS<1:0>		0000
0250	IPC17	31:16	—	—	—	ADCD12IP<2:0>			ADCD12IS<1:0>		—	—	—	ADCD11IP<2:0>			ADCD11IS<1:0>		0000
		15:0	—	—	—	ADCD10IP<2:0>			ADCD10IS<1:0>		—	—	—	ADCD9IP<2:0>			ADCD9IS<1:0>		0000
0260	IPC18	31:16	—	—	—	ADCD16IP<2:0>			ADCD16IS<1:0>		—	—	—	ADCD15IP<2:0>			ADCD15IS<1:0>		0000
		15:0	—	—	—	ADCD14IP<2:0>			ADCD14IS<1:0>		—	—	—	ADCD13IP<2:0>			ADCD13IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0270	IPC19	31:16	—	—	—	ADCD20IP<2:0>			ADCD20IS<1:0>		—	—	—	ADCD19IP<2:0>			ADCD19IS<1:0>		0000
		15:0	—	—	—	ADCD18IP<2:0>			ADCD18IS<1:0>		—	—	—	ADCD17IP<2:0>			ADCD17IS<1:0>		0000
0280	IPC20	31:16	—	—	—	ADCD24IP<2:0>			ADCD24IS<1:0>		—	—	—	ADCD23IP<2:0>			ADCD23IS<1:0>		0000
		15:0	—	—	—	ADCD22IP<2:0>			ADCD22IS<1:0>		—	—	—	ADCD21IP<2:0>			ADCD21IS<1:0>		0000
0290	IPC21	31:16	—	—	—	ADCD28IP<2:0>			ADCD28IS<1:0>		—	—	—	ADCD27IP<2:0>			ADCD27IS<1:0>		0000
		15:0	—	—	—	ADCD26IP<2:0>			ADCD26IS<1:0>		—	—	—	ADCD25IP<2:0>			ADCD25IS<1:0>		0000
02A0	IPC22	31:16	—	—	—	ADCD32IP<2:0>			ADCD32IS<1:0>		—	—	—	ADCD31IP<2:0>			ADCD31IS<1:0>		0000
		15:0	—	—	—	ADCD30IP<2:0>			ADCD30IS<1:0>		—	—	—	ADCD29IP<2:0>			ADCD29IS<1:0>		0000
02B0	IPC23	31:16	—	—	—	ADCD36IP<2:0>			ADCD36IS<1:0>		—	—	—	ADCD35IP<2:0>			ADCD35IS<1:0>		0000
		15:0	—	—	—	ADCD34IP<2:0>			ADCD34IS<1:0>		—	—	—	ADCD33IP<2:0>			ADCD33IS<1:0>		0000
02C0	IPC24	31:16	—	—	—	ADCD40IP<2:0>			ADCD40IS<1:0>		—	—	—	ADCD39IP<2:0>			ADCD39IS<1:0>		0000
		15:0	—	—	—	ADCD38IP<2:0>			ADCD38IS<1:0>		—	—	—	ADCD37IP<2:0>			ADCD37IS<1:0>		0000
02D0	IPC25	31:16	—	—	—	USBSRIP<2:0>			USBSRIS<1:0>		—	—	—	ADCD43IP<2:0>			ADCD43IS<1:0>		0000
		15:0	—	—	—	ADCD42IP<2:0>			ADCD42IS<1:0>		—	—	—	ADCD41IP<2:0>			ADCD41IS<1:0>		0000
02E0	IPC26	31:16	—	—	—	CRPTIP<2:0>(2)			CRPTIS<1:0>(2)		—	—	—	SBIP<2:0>			SBIS<1:0>		0000
		15:0	—	—	—	CFDCIP<2:0>			CFDCIS<1:0>		—	—	—	CPCIP<2:0>			CPCIS<1:0>		0000
02F0	IPC27	31:16	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
		15:0	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		—	—	—	—	—	—	—	—	0000
0300	IPC28	31:16	—	—	—	I2C1BIP<2:0>			I2C1BIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
		15:0	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	U1EIP<2:0>			U1EIS<1:0>		0000
0310	IPC29	31:16	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
		15:0	—	—	—	I2C1MIP<2:0>			I2C1MIS<1:0>		—	—	—	I2C1SIP<2:0>			I2C1SIS<1:0>		0000
0320	IPC30	31:16	—	—	—	CNFIP<2:0>			CNFIS<1:0>		—	—	—	CNEIP<2:0>			CNEIS<1:0>		0000
		15:0	—	—	—	CNDIP<2:0>			CNDIS<1:0>		—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
0330	IPC31	31:16	—	—	—	CNKIP<2:0>			CNKIS<1:0>		—	—	—	CNJIP<2:0>			CNJIS<1:0>		0000
		15:0	—	—	—	CNHIP<2:0>			CNHIS<1:0>		—	—	—	CNGIP<2:0>			CNGIS<1:0>		0000
0340	IPC32	31:16	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
		15:0	—	—	—	PMPEIP<2:0>			PMPEIS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
0350	IPC33	31:16	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
		15:0	—	—	—	USBDMAIP<2:0>			USBDMAIS<1:0>		—	—	—	USBIP<2:0>			USBIS<1:0>		0000
0360	IPC34	31:16	—	—	—	DMA5IP<2:0>			DMA5IS<1:0>		—	—	—	DMA4IP<2:0>			DMA4IS<1:0>		0000
		15:0	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
0370	IPC35	31:16	—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		0000
		15:0	—	—	—	DMA7IP<2:0>			DMA7IS<1:0>		—	—	—	DMA6IP<2:0>			DMA6IS<1:0>		0000
0380	IPC36	31:16	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
		15:0	—	—	—	U2EIP<2:0>			U2EIS<1:0>		—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		0000
0390	IPC37	31:16	—	—	—	CAN1IP<2:0>			CAN1IS<1:0>		—	—	—	I2C2MIP<2:0>			I2C2MIS<1:0>		0000
		15:0	—	—	—	I2C2SIP<2:0>			I2C2SIS<1:0>		—	—	—	I2C2BIP<2:0>			I2C2BIS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
03A0	IPC38	31:16	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>		—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		0000
		15:0	—	—	—	ETHIP<2:0>			ETHIS<1:0>		—	—	—	CAN2IP<2:0>			CAN2IS<1:0>		0000
03B0	IPC39	31:16	—	—	—	U3TXIP<2:0>			U3TXIS<1:0>		—	—	—	U3RXIP<2:0>			U3RXIS<1:0>		0000
		15:0	—	—	—	U3EIP<2:0>			U3EIS<1:0>		—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
03C0	IPC40	31:16	—	—	—	SPI4EIP<2:0>			SPI4EIS<1:0>		—	—	—	I2C3MIP<2:0>			I2C3MIS<1:0>		0000
		15:0	—	—	—	I2C3SIP<2:0>			I2C3SIS<1:0>		—	—	—	I2C3BIP<2:0>			I2C3BIS<1:0>		0000
03D0	IPC41	31:16	—	—	—	FCEIP<2:0>			FCEIS<1:0>		—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
		15:0	—	—	—	SPI4TXIP<2:0>			SPI4TXIS<1:0>		—	—	—	SPI4RXIP<2:0>			SPI4RXIS<1:0>		0000
03E0	IPC42	31:16	—	—	—	U4RXIP<2:0>			U4RXIS<1:0>		—	—	—	U4EIP<2:0>			U4EIS<1:0>		0000
		15:0	—	—	—	SQI1IP<2:0>			SQI1IS<1:0>		—	—	—	PREIP<2:0>			PREIS<1:0>		0000
03F0	IPC43	31:16	—	—	—	I2C4MIP<2:0>			I2C4MIS<1:0>		—	—	—	I2C4SIP<2:0>			I2C4SIS<1:0>		0000
		15:0	—	—	—	I2C4BIP<2:0>			I2C4BIS<1:0>		—	—	—	U4TXIP<2:0>			U4TXIS<1:0>		0000
0400	IPC44	31:16	—	—	—	U5EIP<2:0>			U5EIS<1:0>		—	—	—	SPI5TXIP<2:0>			SPI5TXIS<1:0>		0000
		15:0	—	—	—	SPI5RXIP<2:0>			SPI5RXIS<1:0>		—	—	—	SPI5EIP<2:0>			SPI5EIS<1:0>		0000
0410	IPC45	31:16	—	—	—	I2C5SIP<2:0>			I2C5SIS<1:0>		—	—	—	I2C5BIP<2:0>			I2C5BIS<1:0>		0000
		15:0	—	—	—	U5TXIP<2:0>			U5TXIS<1:0>		—	—	—	U5RXIP<2:0>			U5RXIS<1:0>		0000
0420	IPC46	31:16	—	—	—	SPI6TXIP<2:0>			SPI6TXIS<1:0>		—	—	—	SPI6RXIP<2:0>			SPI6RXIS<1:0>		0000
		15:0	—	—	—	SPI6EIP<2:0>			SPI6EIS<1:0>		—	—	—	I2C5MIP<2:0>			I2C5MIS<1:0>		0000
0430	IPC47	31:16	—	—	—	SDHCIP<2:0>			SDHC1IS<1:0>		—	—	—	U6TXIP<2:0>			U6TXIS<1:0>		0000
		15:0	—	—	—	U6RXIP<2:0>			U6RXIS<1:0>		—	—	—	U6EIP<2:0>			U6EIS<1:0>		0000
0440	IPC48	31:16	—	—	—	CTMU1IP<2:0>			CTMU1IS<1:0>		—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	GPUIP<2:0>			GPU1IS<1:0>		—	—	—	GLCDIP<2:0>			GLCDIS<1:0>		0000
0450	IPC49	31:16	—	—	—	ADC0EIP<2:0>			ADC0EIS<1:0>		—	—	—	ADCURDYIP<2:0>			ADCURDYIS<1:0>		0000
		15:0	—	—	—	ADCARDYIP<2:0>			ADCARDYIS<1:0>		—	—	—	ADCEOSIP<2:0>			ADCEOSIS<1:0>		0000
0460	IPC50	31:16	—	—	—	ADC4EIP<2:0>			ADC4EIS<1:0>		—	—	—	ADC3EIP<2:0>			ADC3EIS<1:0>		0000
		15:0	—	—	—	ADC2EIP<2:0>			ADC2EIS<1:0>		—	—	—	ADC1EIP<2:0>			ADC1EIS<1:0>		0000
0470	IPC51	31:16	—	—	—	ADC0WIP<2:0>			ADC0WIS<1:0>		—	—	—	ADC7EIP<2:0>			ADC7EIS<1:0>		0000
		15:0	—	—	—	ADCGRPIP<2:0>			ADCGRPIS<1:0>		—	—	—	—	—	—	—	—	0000
0480	IPC52	31:16	—	—	—	ADC4WIP<2:0>			ADC4WIS<1:0>		—	—	—	ADC3WIP<2:0>			ADC3WIS<1:0>		0000
		15:0	—	—	—	ADC2WIP<2:0>			ADC2WIS<1:0>		—	—	—	ADC1WIP<2:0>			ADC1WIS<1:0>		0000
0490	IPC53	31:16	—	—	—	MPLLFLTIP<2:0>			MPLLFLTIS<1:0>		—	—	—	ADC7WIP<2:0>			ADC7WIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0540	OFF000	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0544	OFF001	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0548	OFF002	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

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054C	OFF003	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0550	OFF004	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0554	OFF005	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0558	OFF006	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
055C	OFF007	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0560	OFF008	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0564	OFF009	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0568	OFF010	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
056C	OFF011	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0570	OFF012	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0574	OFF013	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0578	OFF014	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
057C	OFF015	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0580	OFF016	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0584	OFF017	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0588	OFF018	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
058C	OFF019	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0590	OFF020	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0594	OFF021	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

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0598	OFF022	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
059C	OFF023	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05A0	OFF024	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05A4	OFF025	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05A8	OFF026	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05AC	OFF027	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05B0	OFF028	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05B4	OFF029	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05B8	OFF030	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05BC	OFF031	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C0	OFF032	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C4	OFF033	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C8	OFF034	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05CC	OFF035	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D0	OFF036	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D4	OFF037	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D8	OFF038	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05DC	OFF039	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E0	OFF040	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05E4	OFF041	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E8	OFF042	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05EC	OFF043	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F0	OFF044	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F4	OFF045	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F8	OFF046	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05FC	OFF047	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0600	OFF048	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0604	OFF049	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0608	OFF059	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
060C	OFF051	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0610	OFF052	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0614	OFF053	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0618	OFF054	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
061C	OFF055	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0620	OFF056	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0624	OFF057	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0628	OFF058	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
062C	OFF059	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0630	OFF060	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0634	OFF061	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0638	OFF062	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
063C	OFF063	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0640	OFF064	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0644	OFF065	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0648	OFF066	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
064C	OFF067	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0650	OFF068	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0654	OFF069	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0658	OFF070	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
065C	OFF071	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0660	OFF072	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0664	OFF073	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0668	OFF074	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
066C	OFF075	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0670	OFF076	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0674	OFF077	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0678	OFF078	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
067C	OFF079	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0680	OFF080	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0684	OFF081	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0688	OFF082	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
068C	OFF083	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0690	OFF084	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0694	OFF085	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0698	OFF086	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
069C	OFF087	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A0	OFF088	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A4	OFF089	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A8	OFF090	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06AC	OFF091	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06B0	OFF092	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06B4	OFF093	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06B8	OFF094	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06BC	OFF095	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06C0	OFF096	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06C4	OFF097	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
06C8	OFF098	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06CC	OFF099	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06D0	OFF100	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06D4	OFF101	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06D8	OFF102	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06DC	OFF103	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06E0	OFF104	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06E4	OFF105	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06E8	OFF106	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06EC	OFF107	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F4	OFF109	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F8	OFF110	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06FC	OFF111	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0700	OFF112	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0704	OFF113	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0708	OFF114	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
070C	OFF115	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0710	OFF116	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0714	OFF117	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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0718	OFF118	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
071C	OFF119	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0720	OFF120	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0724	OFF121	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0728	OFF122	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
072C	OFF123	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0730	OFF124	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0734	OFF125	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0738	OFF126	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
073C	OFF127	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0740	OFF128	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0744	OFF129	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0748	OFF130	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
074C	OFF131	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0750	OFF132	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0754	OFF133	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0758	OFF134	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
075C	OFF135	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0760	OFF136	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0764	OFF137	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0768	OFF138	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
076C	OFF139	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0770	OFF140	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0774	OFF141	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0778	OFF142	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
077C	OFF143	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0780	OFF144	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0784	OFF145	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0788	OFF146	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
078C	OFF147	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0790	OFF148	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0794	OFF149	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0798	OFF150	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
079C	OFF151	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A0	OFF152	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A4	OFF153	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A8	OFF154	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07AC	OFF155	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07B0	OFF156	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B4	OFF157	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B8	OFF158	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07BC	OFF159	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C0	OFF160	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C4	OFF161	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C8	OFF162	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07CC	OFF163	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D0	OFF164	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D4	OFF165	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D8	OFF166	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07DC	OFF167	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E4	OFF169	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E8	OFF170	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07EC	OFF171	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F0	OFF172	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F4	OFF173	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F8	OFF174	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
07FC	OFF175	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0800	OFF176	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0804	OFF177	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0808	OFF178	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
080C	OFF179	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0810	OFF180	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0814	OFF181	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0818	OFF182	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
081C	OFF183	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0820	OFF184	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0824	OFF185	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0828	OFF186	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
082C	OFF187	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0830	OFF188	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0834	OFF189	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0838	OFF190	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
083C	OFF191	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0840	OFF192	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0844	OFF193	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
084C	OFF195	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0850	OFF196	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0854	OFF197	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0858	OFF198	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
085C	OFF199	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0860	OFF200	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0864	OFF201	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0868	OFF202	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
086C	OFF203	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0874	OFF205	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0878	OFF206	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
087C	OFF207	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0880	OFF208	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0884	OFF209	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0888	OFF210	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08A4	OFF211	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0898	OFF214	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
089C	OFF215	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMIKEY<7:0>							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	MVEC	—	TPC<2:0>		
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **NMIKEY<7:0>:** Non-Maskable Interrupt Key bits
When the correct key (0x4E) is written, a software NMI will be generated. The status is indicated by the GNMI bit (RNMICON<19>).

bit 23-13 **Unimplemented:** Read as ‘0’

bit 12 **MVEC:** Multi Vector Configuration bit
1 = Interrupt controller configured for multi-vectored mode
0 = Interrupt controller configured for single vectored mode

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
001 = Interrupts of group priority 1 start the Interrupt Proximity timer
000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
`1xxx` = Reserved (by default, an interrupt with a priority level of 7 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 7 uses Shadow Set 7
`0110` = Interrupt with a priority level of 7 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 7 uses Shadow Set 1
`0000` = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
`1xxx` = Reserved (by default, an interrupt with a priority level of 6 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 6 uses Shadow Set 7
`0110` = Interrupt with a priority level of 6 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 6 uses Shadow Set 1
`0000` = Interrupt with a priority level of 6 uses Shadow Set 0

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
`1xxx` = Reserved (by default, an interrupt with a priority level of 5 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 5 uses Shadow Set 7
`0110` = Interrupt with a priority level of 5 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 5 uses Shadow Set 1
`0000` = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
`1xxx` = Reserved (by default, an interrupt with a priority level of 4 uses Shadow Set 0)
`0111` = Interrupt with a priority level of 4 uses Shadow Set 7
`0110` = Interrupt with a priority level of 4 uses Shadow Set 6
•
•
•
`0001` = Interrupt with a priority level of 4 uses Shadow Set 1
`0000` = Interrupt with a priority level of 4 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = `0`.

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REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)

1xxx = Reserved (by default, an interrupt with a priority level of 3 uses Shadow Set 0)
0111 = Interrupt with a priority level of 3 uses Shadow Set 7
0110 = Interrupt with a priority level of 3 uses Shadow Set 6
.
.
.
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)

1xxx = Reserved (by default, an interrupt with a priority level of 2 uses Shadow Set 0)
0111 = Interrupt with a priority level of 2 uses Shadow Set 7
0110 = Interrupt with a priority level of 2 uses Shadow Set 6
.
.
.
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)

1xxx = Reserved (by default, an interrupt with a priority level of 1 uses Shadow Set 0)
0111 = Interrupt with a priority level of 1 uses Shadow Set 7
0110 = Interrupt with a priority level of 1 uses Shadow Set 6
.
.
.
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit

1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

REGISTER 7-3: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	SRIPL<2:0>(1)		
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SIRQ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as ‘0’

bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits for Single Vector Mode bits(1)
111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits
11111111-00000000 = The last interrupt request number serviced by the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits
Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

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REGISTER 7-5: IFSx: INTERRUPT FLAG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS9	IFS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS7	IFS6	IFS5	IFS4	IFS3	IFS2	IFS1	IFS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS31-IFS0:** Interrupt Flag Status bits
`1` = Interrupt request has occurred
`0` = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-2 for the exact bit definitions.

REGISTER 7-6: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC31-IEC0:** Interrupt Enable bits
`1` = Interrupt is enabled
`0` = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-2 for bit definitions.

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Sub-priority bits
11 = Interrupt sub-priority is 3
10 = Interrupt sub-priority is 2
01 = Interrupt sub-priority is 1
00 = Interrupt subdirectory is 0

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Sub-priority bits
11 = Interrupt sub-priority is 3
10 = Interrupt sub-priority is 2
01 = Interrupt sub-priority is 1
00 = Interrupt sub-priority is 0

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-10 **IP1<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for bit definitions.

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REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)

bit 9-8 **IS1<1:0>:** Interrupt Sub-priority bits
- 11 = Interrupt sub-priority is 3
- 10 = Interrupt sub-priority is 2
- 01 = Interrupt sub-priority is 1
- 00 = Interrupt sub-priority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP0<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- .
- .
- .
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 1-0 **IS0<1:0>:** Interrupt Sub-priority bits
- 11 = Interrupt sub-priority is 3
- 10 = Interrupt sub-priority is 2
- 01 = Interrupt sub-priority is 1
- 00 = Interrupt sub-priority is 0

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for bit definitions.

REGISTER 7-8: OFFx: INTERRUPT VECTOR ADDRESS OFFSET REGISTER (x = 0-190)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	VOFF<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VOFF<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	VOFF<7:1>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 17-1 **VOFF<17:1>:** Interrupt Vector ‘x’ Address Offset bits

bit 0 **Unimplemented:** Read as ‘0’

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8.0 OSCILLATOR CONFIGURATION

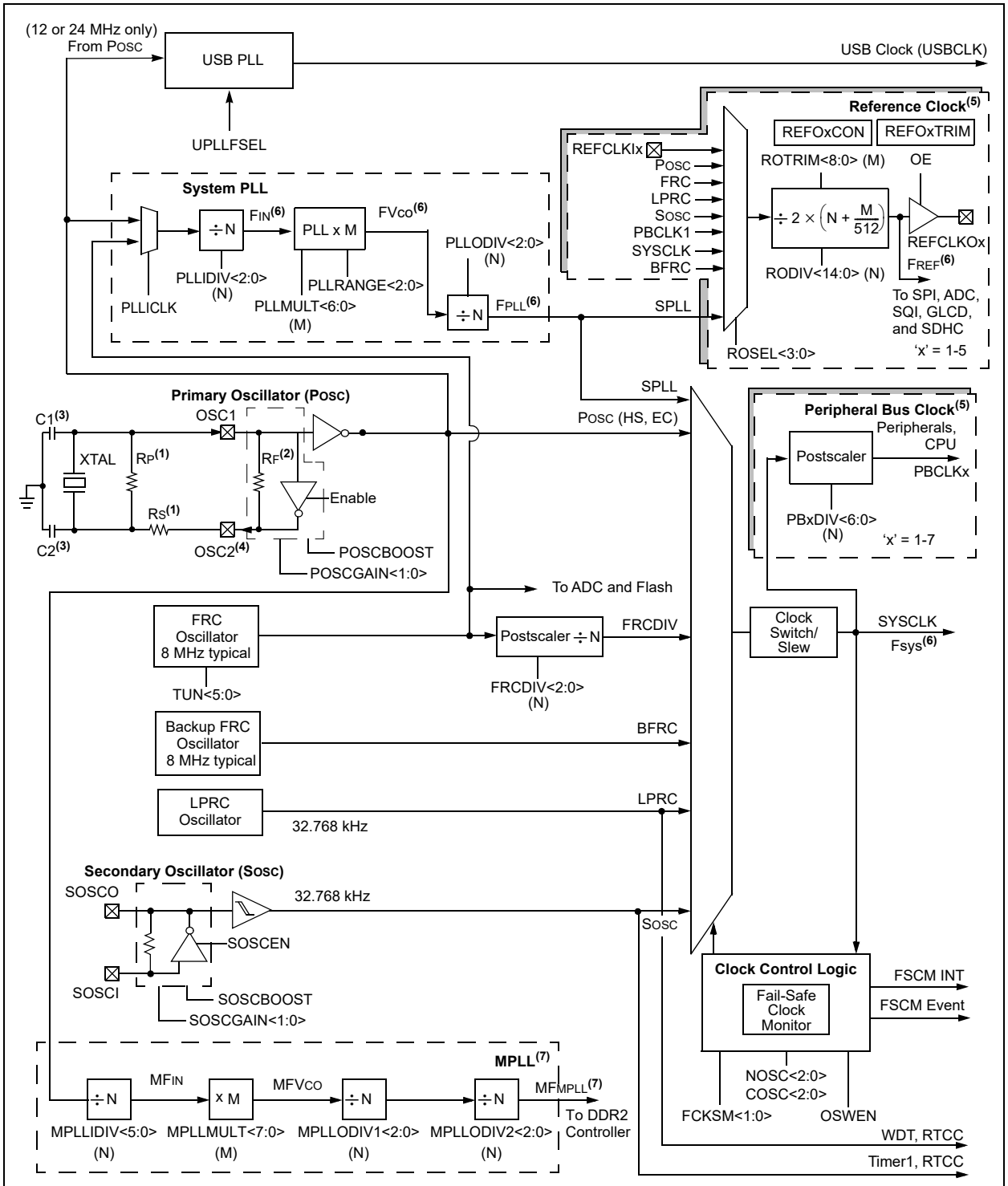
Note: This data sheet summarizes the features of the PIC32MZ DAK/DAL/DAR/DAS family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip website (www.microchip.com/PIC32).

The PIC32MZ DAK/DAL/DAR/DAS oscillator system has the following modules and features:

- Five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown with dedicated Back-up FRC (BFRC)
- Dedicated On-Chip PLL for DDR2 and USB modules
- Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility

A block diagram of the oscillator system is provided in Figure 8-1. The clock distribution is shown in Table 8-1.

FIGURE 8-1: PIC32MZ DAK/DAL/DAR/DAS FAMILY OSCILLATOR DIAGRAM



Notes:

1. A series resistor, R_S, may be required for AT strip cut crystals, or to eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, R_P, with a value of 1 MΩ.
2. The internal feedback resistor, R_F, is typically in the range of 2 to 10 MΩ.
3. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the "*PIC32 Family Reference Manual*" for help in determining the best oscillator components.
4. PBCLK1 divided by 2 is available on the OSC2 pin in certain clock modes.
5. Shaded regions indicate multiple instantiations of a peripheral or feature.
6. Refer to Table 44-24 in **Section 44.0 "Electrical Characteristics"** for frequency limitations.
7. Memory Phase-Locked Loop (MPLL) is controlled through the CFGMPLL register (see **41.0 "Special Features"** for details). MF_{MPLL} drives the DDR2 PHY and is the source clock (DDRCK, $\overline{DDRCK}$) for DDR2 SDRAM.

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TABLE 8-1: SYSTEM AND PERIPHERAL CLOCK DISTRIBUTION

Peripheral	Clock Source																	
	FRC	LPRC	SOSC	SYSCLK	USBCLK	MPLL	PBCLK1(1)	PBCLK2	PBCLK3	PBCLK4	PBCLK5	PBCLK6	PBCLK7	REFCLKO1	REFCLKO2	REFCLKO3	REFCLKO4	REFOCLK5
CPU													X					
WDT		X		X			X(3)											
DMT				X			X(3)						X					
GLCD				X(3)														X(6)
GPU				X														
DDR2C				X(3)		X												
SDHC											X(3)						X	
Flash	X(2)			X(2)							X(2)							
ADC	X			X					X(3)							X		
Comparator									X(3)									
CTMU									X(3)									
Crypto											X(3)							
RNG											X(3)							
USB					X						X(3)							
USBCR(7)											X(3)							
CAN											X(3)							
Ethernet											X(3)							
PMP								X(3)										
I^2C								X(3)										
UART								X(3)										
RTCC		X	X									X(3)						
EBI				X														
SQI											X(3)				X			
SPI								X						X				
Timers		X	X(4)						X									
Output Compare									X									
Input Capture									X									
Ports										X(3)								
DMA				X														
Interrupts				X														
Prefetch				X														
OSC2 Pin							X(5)											
DSCTRL(8)				X								X						
HLVD							X(3)											

Note 1: PBCLK1 is used by system modules and cannot be turned off.
2: SYSCLK/PBCLK5 is used to fetch data from/to the Flash Controller, while the FRC clock is used for programming.
3: Special Function Register (SFR) access only.
4: Timer1 only.
5: PBCLK1 divided by 2 is available on the OSC2 pin in certain clock modes.
6: REFCLKO5 is used for the Pixel Clock. .
7: USBCR is the Clock/Reset Control block for the USB.
8: DSCTRL is the Deep Sleep Control Block.

8.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MZ DAK/DAL/DAR/DAS oscillator system includes a Fail-safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the BFRC oscillator and triggers a NMI. The BFRC is an untuned 8 MHz oscillator that will drive the SYSCLK during FSCM event. When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode both the SYSCLK and the FSCM halt, which prevents FSCM detection.

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8.2 Oscillator Control Registers

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets(1)
1200	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			DRMEN	—	SLP2SPD	—	—	—	—	—	0020
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	—	—	SLPEN	CF	—	SOSCEN	OSWEN	xx0x
1210	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						00xx
1220	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>							01xx
		15:0	—	—	—	—	—	PLLIDIV<2:0>			PLLICLK	—	—	—	—	PLLRANGE<2:0>			0x0x
1280	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
1290	REFO1TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12A0	REFO2CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	—	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12B0	REFO2TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12C0	REFO3CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12D0	REFO3TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12E0	REFO4CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12F0	REFO4TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1300	REFO5CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	—	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
1310	REFO5TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1340	PB1DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1350	PB2DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1360	PB3DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1370	PB4DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

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TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets(1)
1380	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1390	PB6DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8803
13A0	PB7DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
13C0	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0000
13D0	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

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REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FRCDIV<2:0>		
23:16	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	DRMEN	—	SLP2SPD	—	—	—	—	—
15:8	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0, HS	U-0	R/W-y	R/W-y
	CLKLOCK	—	—	SLPEN	CF	—	SOSCEN	OSWEN(1)

Legend:	y = Value set from Configuration bits on POR		HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits
- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2
- 000 = FRC divided by 1 (default setting)

bit 23 **DRMEN:** Dream Mode Enable bit
- 1 = Dream mode is enabled
- 0 = Dream mode is disabled

bit 22 **Unimplemented:** Read as ‘0’

bit 21 **SLP2SPD:** Sleep Two-speed Start-up Control bit
- 1 = Use FRC as SYSCLK until the selected clock is ready
- 0 = Use the selected clock directly

bit 20-15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits
- 111 = System PLL (SPLL)
- 110 = Back-up Fast RC (BFRC) Oscillator
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Reserved
- 010 = Primary Oscillator (POSC) (HS or EC)
- 001 = System PLL (SPLL)
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

bit 11 **Unimplemented:** Read as ‘0’

Note 1: The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is ‘1’. When IESO = 0, the reset value is ‘0’.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits
- 111 = System PLL (SPLL)
- 110 = Reserved
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Reserved
- 010 = Primary Oscillator (POSC) (HS or EC)
- 001 = System PLL (SPLL)
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit
- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Enable Secondary Oscillator
- 0 = Disable Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit(1)
- 1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
- 0 = Oscillator switch is complete

Note 1: The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

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REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

100000 = Center frequency -2%
100001 =
•
•
•
111111 =
000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)
000001 =
•
•
•
011110 =
011111 = Center frequency +2%

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

REGISTER 8-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—					PLLIDIV<2:0>		
7:0	R/W-y	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	PLLICLK	—	—	—	—	PLLRANGE<2:0>		

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits

111 = Reserved
110 = Reserved
101 = PLL Divide by 32
100 = PLL Divide by 16
011 = PLL Divide by 8
010 = PLL Divide by 4
001 = PLL Divide by 2
000 = Reserved

The default setting is specified by the FPLLODIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 “Special Features”** for information.

bit 23 **Unimplemented:** Read as ‘0’

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits

1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

The default setting is specified by the FPLLMULT<6:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 “Special Features”** for information.

bit 15-11 **Unimplemented:** Read as ‘0’

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

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REGISTER 8-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

bit 10-8 **PLLIDIV<2:0>:** System PLL Input Clock Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

The default setting is specified by the FPLLIDIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information. If the PLLICLK is set for FRC, this setting is ignored by the PLL and the divider is set to Divide-by-1.

bit 7 **PLLICLK:** System PLL Input Clock Source bit

1 = FRC is selected as the input to the System PLL
0 = POSC is selected as the input to the System PLL
The POR default is specified by the FPLLICLK Configuration bit in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information.

bit 6-3 **Unimplemented:** Read as '0'

bit 2-0 **PLLRANGE<2:0>:** System PLL Frequency Range Selection bits

111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

The default setting is specified by the FPLLRNG<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 34-5 in **Section 34.0 "Special Features"** for information.

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

REGISTER 8-4: REFOxCON: REFERENCE OSCILLATOR CONTROL REGISTER ('x' = 1-5)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits

This value specifies 1/2 period of the reference clock in the source clocks.

111111111111111 = REFO clock is Base clock frequency divided by 65,534 (32,767*2)

111111111111110 = REFO clock is Base clock frequency divided by 65,532 (32,766*2)

•

•

•

000000000000011 = REFO clock is Base clock frequency divided by 6 (3*2)

000000000000010 = REFO clock is Base clock frequency divided by 4 (2*2)

000000000000001 = REFO clock is Base clock frequency divided by 2 (1*2)

000000000000000 = REFO is the same frequency as Base Clock (no divider)

bit 15 **ON:** Output Enable bit(1)

1 = Reference Oscillator Module enabled

0 = Reference Oscillator Module disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit

1 = Reference clock is driven out on REFCLKOx pin

0 = Reference clock is not driven out on REFCLKOx pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)

1 = Reference Oscillator Module output continues to run in Sleep

0 = Reference Oscillator Module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit

1 = Divider switch is in progress

0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)

1 = Reference clock request is active

0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.

2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

4: REFCLKI2 and REFCLKI5 do not exist and are therefore not selectable.

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REGISTER 8-4: REFOxCON: REFERENCE OSCILLATOR CONTROL REGISTER ('x' = 1-5)

bit 3-0 **ROSEL**<3:0>: Reference Clock Source Select bits(3)
1111 = Reserved
•
•
•
1001 = BFRC
1000 = REFCLKIx (4)
0111 = System PLL output
0110 = Reserved
0101 = Sosc
0100 = LPRC
0011 = FRC
0010 = Posc
0001 = PBCLK1
0000 = SYSCLK

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
4: REFCLKI2 and REFCLKI5 do not exist and are therefore not selectable.

REGISTER 8-5: REFOxTRIM: REFERENCE OSCILLATOR TRIM REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits
`111111111` = 511/512 divisor added to RODIV value
`111111110` = 510/512 divisor added to RODIV value
•
•
•
`100000000` = 256/512 divisor added to RODIV value
•
•
•
`000000010` = 2/512 divisor added to RODIV value
`000000001` = 1/512 divisor added to RODIV value
`000000000` = 0 divisor added to RODIV value

bit 22-0 **Unimplemented:** Read as '`0`'

Note 1: While the ON bit (REFOxCON<15>) is '`1`', writes to this register do not take effect until the DIVSWEN bit is also set to '`1`'.
2: Do not write to this register when the ON bit (REFOxCON<15>) is not equal to the ACTIVE bit (REFOxCON<8>).
3: Specified values in this register do not take effect if RODIV<14:0> (REFOxCON<30:16>) = 0.

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REGISTER 8-6: PBxDIV: PERIPHERAL BUS 'x' CLOCK DIVISOR CONTROL REGISTER ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	U-0	R-1	U-0	U-0	U-0
	ON(1)	—	—	—	PBDIVRDY	—	—	—
7:0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	PBDIV<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Peripheral Bus 'x' Output Clock Enable bit(1)
1 = Output clock is enabled
0 = Output clock is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **PBDIVRDY:** Peripheral Bus 'x' Clock Divisor Ready bit
1 = Clock divisor logic is not switching divisors and the PBxDIV<6:0> bits may be written
0 = Clock divisor logic is currently switching values and the PBxDIV<6:0> bits cannot be written

bit 10-7 **Unimplemented:** Read as '0'

bit 6-0 **PBDIV<6:0>:** Peripheral Bus 'x' Clock Divisor Control bits
1111111 = PBCLKx is SYSCLK divided by 128
1111110 = PBCLKx is SYSCLK divided by 127
•
•
•
0000011 = PBCLKx is SYSCLK divided by 4
0000010 = PBCLKx is SYSCLK divided by 3
0000001 = PBCLKx is SYSCLK divided by 2 (default value for x < 7)
0000000 = PBCLKx is SYSCLK divided by 1 (default value for x ≥ 7)

Note 1: The clock for peripheral bus 1 cannot be turned off. Therefore, the ON bit in the PB1DIV register cannot be written as a '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 8-7: SLEWCON: OSCILLATOR SLEW CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SYSDIV<3:0>(1)			
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SLWDIV<2:0>		
7:0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R-0, HS, HC
	—	—	—	—	—	UPEN	DNEN	BUSY

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as ‘0’

bit 19-16 **SYSDIV<3:0>:** System Clock Divide Control bits(1)

1111 = SYSCLK is divided by 16
1110 = SYSCLK is divided by 15
•
•
•
0010 = SYSCLK is divided by 3
0001 = SYSCLK is divided by 2
0000 = SYSCLK is not divided

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-8 **SLWDIV<2:0>:** Slew Divisor Steps Control bits

These bits control the maximum division steps used when slewing during a frequency change.
111 = Steps are divide by 128, 64, 32, 16, 8, 4, 2, and then no divisor
110 = Steps are divide by 64, 32, 16, 8, 4, 2, and then no divisor
101 = Steps are divide by 32, 16, 8, 4, 2, and then no divisor
100 = Steps are divide by 16, 8, 4, 2, and then no divisor
011 = Steps are divide by 8, 4, 2, and then no divisor
010 = Steps are divide by 4, 2, and then no divisor
001 = Steps are divide by 2, and then no divisor
000 = No divisor is used during slewing
The steps apply in reverse order (i.e., 2, 4, 8, etc.) during a downward frequency change.

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **UPEN:** Upward Slew Enable bit

1 = Slewing enabled for switching to a higher frequency
0 = Slewing disabled for switching to a higher frequency

bit 1 **DNEN:** Downward Slew Enable bit

1 = Slewing enabled for switching to a lower frequency
0 = Slewing disabled for switching to a lower frequency

bit 0 **BUSY:** Clock Switching Slewing Active Status bit

1 = Clock frequency is being actively slewed to the new frequency
0 = Clock switch has reached its final value

Note 1: The SYSDIV<3:0> bit settings are ignored if both UPEN and DNEN = 0, and SYSCLK will be divided by 1.

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CLKSTAT: OSCILLATOR CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	R-0	R-0	U-0	R-0	U-0	R-0
	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **SPLLRDY:** System PLL (SPLL) Ready Status bit
1 = SPLL is ready
0 = SPLL is not ready

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **LPRCRDY**: Low-Power RC (LPRC) Oscillator Ready Status bit
1 = LPRC is stable and ready
0 = LPRC is disabled or not operating

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready Status bit
1 = SOSC is stable and ready
0 = SOSC is disabled or not operating

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready Status bit
1 = POSC is stable and ready
0 = POSC is disabled or not operating

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready Status bit
1 = FRC is stable and ready
0 = FRC is disabled for not operating

9.0 PREFETCH MODULE

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 41. "Prefetch Module for Devices with L1 CPU Cache"** (DS60001183), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Prefetch module is a performance enhancing module that is included in PIC32MZ DAK/DAL/DAR/DAS family devices. When running at high-clock rates, Wait states must be inserted into Program Flash Memory (PFM) read transactions to meet the access time of the PFM. Wait states can be hidden to the core by prefetching and storing instructions in a temporary holding area that the CPU can access quickly. Although the data path to the CPU is 32 bits wide, the data path to the PFM is 128 bits wide. This wide data path provides the same bandwidth to the CPU as a 32-bit path running at four times the frequency.

The Prefetch module holds a subset of PFM in temporary holding spaces known as lines. Each line contains a tag and data field. Normally, the lines hold a copy of what is currently in memory to make instructions or data available to the CPU without Flash Wait states.

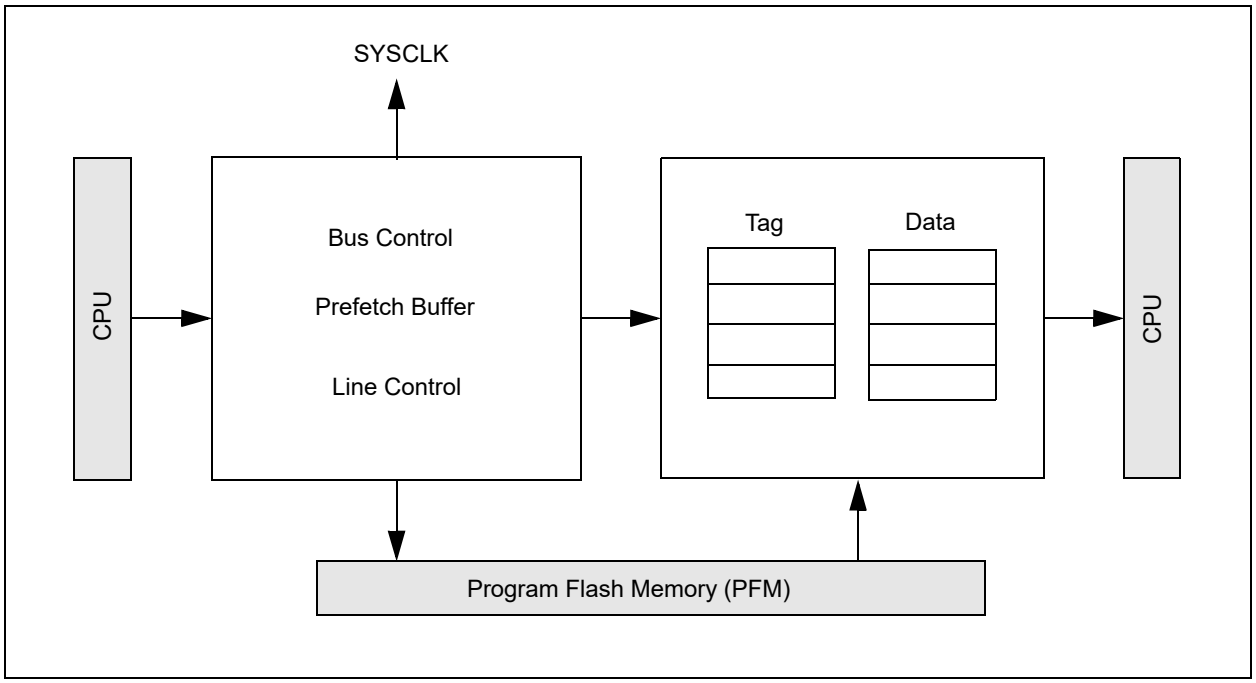
9.1 Features

The Prefetch module includes the following key features:

- 4x16 byte fully-associative lines
- One line for CPU instructions
- One line for CPU data
- Two lines for peripheral data
- 16-byte parallel memory fetch
- Configurable predictive prefetch
- Error detection and correction

A simplified block diagram of the Prefetch module is shown in Figure 9-1.

FIGURE 9-1: PREFETCH MODULE BLOCK DIAGRAM



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9.2 Prefetch Control Registers

TABLE 9-1: PREFETCH REGISTER MAP

Virtual Address (BF8E_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	PRECON	31:16	—	—	—	—	—	PFMSECEN	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	PREFEN<1:0>		—	PFMWS<2:0>			0007
0010	PRESTAT	31:16	—	—	—	—	PFMDED	PFMSEC	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PFMSECCNT<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 9-1: PRECON: PREFETCH MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
	—	—	—	—	—	PFMSECEN	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	PREFEN<1:0>		—	PFMWS<2:0>(1)		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Write ‘0’; ignore read

bit 26 **PFMSECEN:** Flash SEC Interrupt Enable bit
1 = Generate an interrupt when the PFMSEC bit (PRESTAT<26>) is set
0 = Do not generate an interrupt when the PFMSEC bit is set

bit 25-6 **Unimplemented:** Write ‘0’; ignore read

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits
11 = Enable predictive prefetch for any address
10 = Enable predictive prefetch for CPU instructions and CPU data
01 = Enable predictive prefetch for CPU instructions only
00 = Disable predictive prefetch

bit 3 **Unimplemented:** Write ‘0’; ignore read

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSCLK Wait States bits(1)
111 = Seven Wait states
•
•
•
010 = Two Wait states
001 = One Wait state
000 = Zero Wait states

Note 1: For the Wait states to SYSCLK relationship, refer to Table 44-15 in **Section44.0 “Electrical Characteristics”**.

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Register 9-1: PRESTAT: Prefetch Module Status Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
	—	—	—	—	PFMDED	PFMSEC	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PFMSECCNT<7:0>							

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Write ‘0’; ignore read

bit 27 **PFMDED:** Flash Double-bit Error Detected (DED) Status bit
This bit is set in hardware and can only be cleared (i.e., set to ‘0’) in software.
1 = A DED error has occurred
0 = A DED error has not occurred

bit 26 **PFMSEC:** Flash Single-bit Error Corrected (SEC) Status bit
1 = A SEC error occurred when PFMSECCNT<7:0> was equal to zero
0 = A SEC error has not occurred

bit 25-8 **Unimplemented:** Write ‘0’; ignore read

bit 7-0 **PFMSECCNT<7:0>:** Flash SEC Count bits
11111111 - 00000000 = SEC count

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

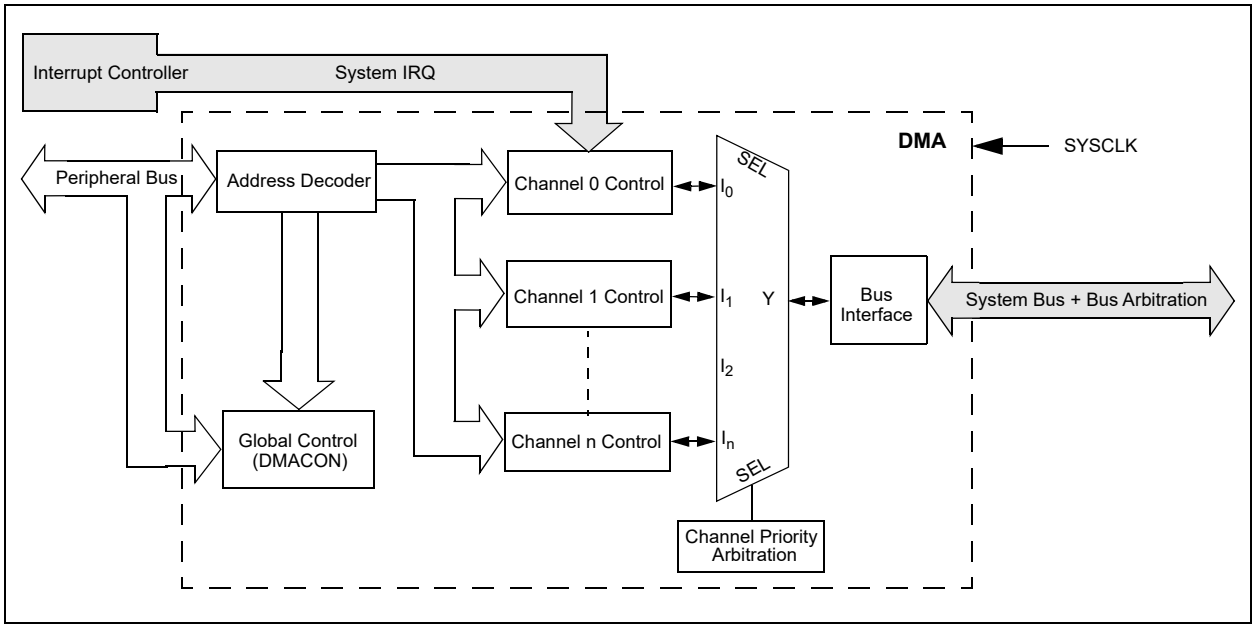
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Direct Memory Access (DMA) Controller is a bus host module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the device such as SPI, UART, PMP, etc., or memory itself.

Following are some of the key features of the DMA Controller module:

- Eight identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Up to 2-byte Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent error address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



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10.1 DMA Control Registers

TABLE 10-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
1010	DMASTAT	31:16	RDWR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	DMACH<2:0>			0000
1020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

TABLE 10-2: DMA CRC REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
1040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
1050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1060	DCH0CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1090	DCH0SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
10A0	DCH0DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
10B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
10C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
10D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
10E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
10F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
1100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
1120	DCH1CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1150	DCH1SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
1160	DCH1DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
11A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
11B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
11C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
11D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
11E0	DCH2CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
11F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1210	DCH2SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
1220	DCH2DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
1230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
12A0	DCH3CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
12B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
12C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
12D0	DCH3SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
12E0	DCH3DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
12F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
1340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
1360	DCH4CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1370	DCH4ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1380	DCH4INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1390	DCH4SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
13A0	DCH4DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
13B0	DCH4SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
13C0	DCH4DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
13D0	DCH4SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
13E0	DCH4DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
13F0	DCH4CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
1400	DCH4CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1410	DCH4DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
1420	DCH5CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1430	DCH5ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1440	DCH5INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1450	DCH5SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
1460	DCH5DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
1470	DCH5SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1480	DCH5DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1490	DCH5SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
14A0	DCH5DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
14B0	DCH5CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
14C0	DCH5CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
14D0	DCH5DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
14E0	DCH6CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
14F0	DCH6ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1500	DCH6INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1510	DCH6SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
1520	DCH6DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
1530	DCH6SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1540	DCH6DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1550	DCH6SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1560	DCH6DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1570	DCH6CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
1580	DCH6CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1590	DCH6DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx
15A0	DCH7CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	7700
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
15B0	DCH7ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
15C0	DCH7INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
15D0	DCH7SSA	31:16	CHSSA<31:0>																xxxx
		15:0																	xxxx
15E0	DCH7DSA	31:16	CHDSA<31:0>																xxxx
		15:0																	xxxx
15F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																xxxx
1600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																xxxx
1610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																xxxx
1640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 10-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	ON	—	—	SUSPEND	DMABUSY	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** DMA On bit
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active and is transferring data
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as ‘0’

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REGISTER 10-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RDWR	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	DMACH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **RDWR:** Read/Write Status bit
1 = Last DMA bus access when an error was detected was a read
0 = Last DMA bus access when an error was detected was a write

bit 30-3 **Unimplemented:** Read as ‘0’

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel when an error was detected.

REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access when an error was detected.

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO(1)	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>(1)				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP(1)	CRCTYP	—	—	CRCCH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as ‘0’

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
- 00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit(1)
- 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as ‘0’

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):
- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as ‘0’

bit 12-8 **PLEN<4:0>:** Polynomial Length bits(1)

When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):
These bits are unused.

When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):
Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

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REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 6 **CRCAPP:** CRC Append Mode bit(1)
- 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
- 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination

bit 5 **CRCTYP:** CRC Type Selection bit
- 1 = The CRC module will calculate an IP header checksum
- 0 = The CRC module will calculate a LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
- 111 = CRC is assigned to Channel 7
- 110 = CRC is assigned to Channel 6
- 101 = CRC is assigned to Channel 5
- 100 = CRC is assigned to Channel 4
- 011 = CRC is assigned to Channel 3
- 010 = CRC is assigned to Channel 2
- 001 = CRC is assigned to Channel 1
- 000 = CRC is assigned to Channel 0

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 10-5: DCRCDATA: DMA CRC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits
Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return ‘0’ on any read.

When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always ‘0’. Data written to this register is converted and read back in 1’s complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return ‘0’ on any read.

REGISTER 10-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits
When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

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REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPIGN<7:0>							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
	CHBUSY	—	CHIPGNEN	—	CHPATLEN	—	—	CHCHNS(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN(2)	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **CHPIGN<7:0>:** Channel Register Data bits
Pattern Terminate mode:
Any byte matching these bits during a pattern match may be ignored during the pattern match determination when the CHPIGNEN bit is set. If a byte is read that is identical to this data byte, the pattern match logic will treat it as a “don’t care” when the pattern matching logic is enabled and the CHPIGEN bit is set.

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15 **CHBUSY:** Channel Busy bit
1 = Channel is active or has been enabled
0 = Channel is inactive or has been disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **CHPIGNEN:** Enable Pattern Ignore Byte bit
1 = Treat any byte that matches the CHPIGN<7:0> bits as a “don’t care” when pattern matching is enabled
0 = Disable this feature

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **CHPATLEN:** Pattern Length bit
1 = 2 byte length
0 = 1 byte length

bit 10-9 **Unimplemented:** Read as ‘0’

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
1 = Channel is enabled
0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
1 = Channel start/abort events will be registered, even if the channel is disabled
0 = Channel start/abort events will be ignored if the channel is disabled

bit 5 **CHCHN:** Channel Chain Enable bit
1 = Allow channel to be chained
0 = Do not allow channel to be chained

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).
2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER (CONTINUED)

bit 4 **CHAEN:** Channel Automatic Enable bit

1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit

1 = An event has been detected
0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits

11 = Channel has priority 3 (highest)
10 = Channel has priority 2
01 = Channel has priority 1
00 = Channel has priority 0

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

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REGISTER 10-8: DCHxECON: DMA CHANNEL x EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0>(1)							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0>(1)							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•
•
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)

11111111 = Interrupt 255 will initiate a DMA transfer

•
•
•

00000001 = Interrupt 1 will initiate a DMA transfer
00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a ‘1’
0 = This bit always reads ‘0’

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a ‘1’
0 = This bit always reads ‘0’

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match
0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as ‘0’

Note 1: See **Table 7-2: “Interrupt IRQ, Vector and Bit Location”** for the list of available interrupt IRQ sources.

REGISTER 10-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
0 = No interrupt is pending

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REGISTER 10-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER (CONTINUED)

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
- 1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
- 0 = No interrupt is pending

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
- 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
- 0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
- 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
- 0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
- 1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
- 0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
- 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
- 0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
- 1 = A channel address error has been detected
  Either the source or the destination address is invalid.
- 0 = No interrupt is pending

REGISTER 10-10: DCHxSSA: DMA CHANNEL x SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.

Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL x DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.

Note: This must be the physical address of the destination.

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REGISTER 10-12: DCHxSSIZ: DMA CHANNEL x SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size

.

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0000000000000010 = 2 byte source size

0000000000000001 = 1 byte source size

0000000000000000 = 65,536 byte source size

REGISTER 10-13: DCHxDSIZ: DMA CHANNEL x DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size

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.

0000000000000010 = 2 byte destination size

0000000000000001 = 1 byte destination size

0000000000000000 = 65,536 byte destination size

REGISTER 10-14: DCHxSPTR: DMA CHANNEL x SOURCE POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHSPTR<15:0>:** Channel Source Pointer bits

1111111111111111 = Points to byte 65,535 of the source

•
•
•

0000000000000001 = Points to byte 1 of the source

0000000000000000 = Points to byte 0 of the source

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 10-15: DCHxDPTR: DMA CHANNEL x DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHDPTR<15:0>:** Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination

•
•
•

0000000000000001 = Points to byte 1 of the destination

0000000000000000 = Points to byte 0 of the destination

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REGISTER 10-16: DCHxCSIZ: DMA CHANNEL x CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event

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0000000000000010 = 2 bytes transferred on an event

0000000000000001= 1 byte transferred on an event

0000000000000000 = 65,536 bytes transferred on an event

REGISTER 10-17: DCHxCPTR: DMA CHANNEL x CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHCPTR<15:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event

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0000000000000001 = 1 byte has been transferred since the last event

0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 10-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHPDAT<15:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All other modes:
Unused.

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NOTES:

11.0 HI-SPEED USB WITH ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MZ DAK/DAL/DAR/DAS family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 51. "Hi-Speed USB with On-The-Go (OTG)"** (DS60001326) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web ite (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 embedded host, device, or OTG implementation with a minimum of external components.

The module supports Hi-Speed, Full-Speed, or Low-Speed in any of the operating modes. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the RAM controller, packet encode/decode, UTM synchronization, endpoint control, a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is illustrated in Figure 11-1.

The USB module includes the following features:

- USB Hi-Speed, Full-Speed, and Low-Speed support for host and device
- USB OTG support with one or more Hi-Speed, Full-Speed, or Low-Speed device
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Integrated 8-channel DMA to access system RAM and Flash
- Seven transmit endpoints and seven receive endpoints, in addition to Endpoint 0
- Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) support
- Suspend and resume signaling support
- Dynamic FIFO sizing
- Integrated RAM for the FIFOs, eliminating the need for system RAM for the FIFOs
- Link power management support

Note 1: The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

2: If the USB module is used, the Primary Oscillator (POSC) is limited to either 12 MHz or 24 MHz.

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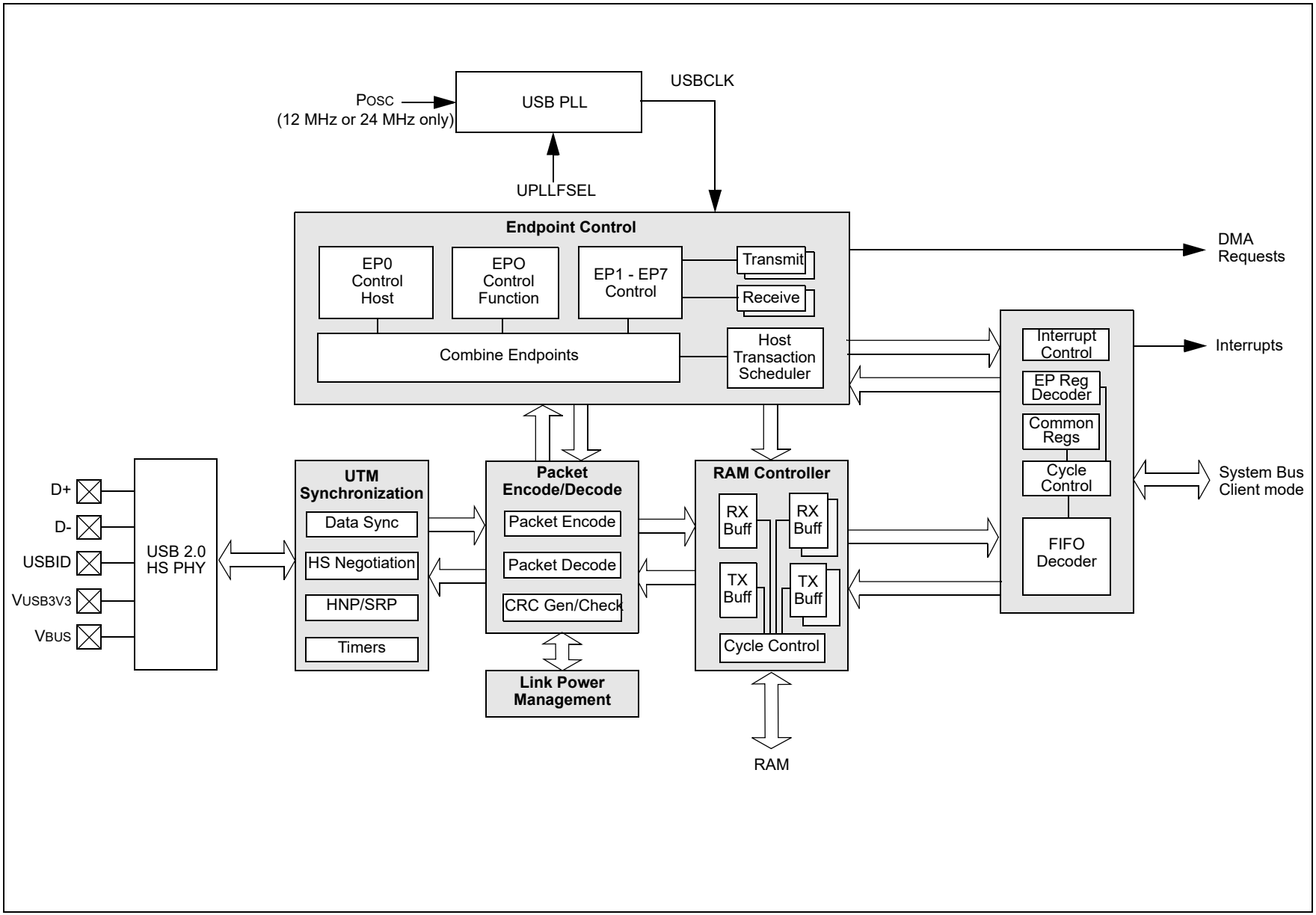
FIGURE 11-1: PIC32MZ DAK/DAL/DAR/DAS FAMILY USB INTERFACE DIAGRAM



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11.1 USB OTG Control Registers

TABLE 11-1: USB REGISTER MAP 1

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3000	USBCSR0	31:16	—	—	—	—	—	—	—	—	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF	0000
		15:0	ISOUPD(1)	SOFT CONN(1)	HSEN	HSMODE	RESET	RESUME	SUSP MODE	SUSPEN	—	FUNC<6:0>(1)							2000
			—(2)	—(2)								—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	
3004	USBCSR1	31:16	—	—	—	—	—	—	—	—	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE	00FF
		15:0	—	—	—	—	—	—	—	—	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—	0000
3008	USBCSR2	31:16	VBUSIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE	VBUSIF	SESSREQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF	0600
		15:0	—	—	—	—	—	—	—	—	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—	00FE
300C	USBCSR3	31:16	FORCEHST	FIFOACC	FORCEFS	FORCEHS	PACKET	TESTK	TESTJ	NAK	—	—	—	—	ENDPOINT<3:0>				0000
		15:0	—	—	—	—	—	RFRMNUM<10:0>											0000
3010	USB IE0CSR0(3)	31:16	—	—	—	—	—(1)	—(1)	—(1)	FLSHFIFO	SVC SETEND(1)	SVCRPR(1)	SEND STALL(1)	SETUP END(1)	DATAEND(1)	SENT STALL(1)	TXPKT RDY	RXPKT RDY	0000
							DISPING(2)	DTWREN(2)	DATA TGGL(2)		NAK TMOUT(2)	STATPKT(2)	REQPKT(2)	ERROR(2)	SETUP PKT(2)	RXSTALL(2)			0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3018	USB IE0CSR2(3)	31:16	—	—	—	NAKLIM<4:0>(2)					SPEED<1:0>(2)		—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RXCNT<6:0>							0000
301C	USB IE0CSR3(3)	31:16	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID	—	—	—	—	—	—	—	—	xx00
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	USB IENCSR0(4)	31:16	AUTOSET	ISO(1)	MODE	DMA REQEN	FRC DATTG	DMA REQMD	—(1)	—(1)	INCOMP TX(1)	CLRDT	SENT STALL(1)	SEND STALL(1)	FLUSH	UNDER RUN(1)	FIFONE	TXPKT RDY	0000
				—					DTWREN(2)	DATA TGGL(2)	NAK TMOUT(2)		RXSTALL(2)	SETUPPKT(2)		ERROR(2)			0000
		15:0	MULT<4:0>					TXMAXP<10:0>											0000
3014	USB IENCSR1(4)	31:16	AUTOCLR	ISO(1)	DMA REQEN	DISNYET(1)	DMA REQMD	—(1)	—(1)	INCOM PRX	CLRDT	SENTSTALL(1)	SENDSTALL(1)	FLUSH	DATAERR(1)	OVERRUN(1)	FIFOFULL	RXPKT RDY	0000
				AUTORQ(2)		PIDERR(2)		DATA TWEN(2)	DATA TGGL(2)			RXSTALL(2)	REQPKT(2)		DERR-NAKT(1)	ERROR(2)			0000
		15:0	MULT<4:0>					RXMAXP<10:0>											0000
3018	USB IENCSR2(4)	31:16	TXINTERV<7:0>(2)								SPEED<1:0>(2)		PROTOCOL<1:0>		TEP<3:0>				0000
		15:0	—	—	RXCNT<13:0>														0000
301C	USB IENCSR3(1,3)	31:16	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	RXINTERV<7:0>								SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>				0000
3020	USB FIFO0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3024	USB FIFO1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

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TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3028	USB FIFO2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
302C	USB FIFO3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3030	USB FIFO4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3034	USB FIFO5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3038	USB FIFO6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
303C	USB FIFO7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3060	USBOTG	31:16	—	—	—	RXDPB	RXFIFOSZ<3:0>				—	—	—	TXDPB	TXFIFOSZ<3:0>				0000
		15:0	—	—	—	—	—	—	TXEDMA	RXEDMA	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION	0088
3064	USB FIFOA	31:16	—	—	—	RXFIFOAD<12:0>													0000
		15:0	—	—	—	TXFIFOAD<12:0>													0000
306C	USB HWVER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC	VERMAJOR<4:0>					VERMINOR<9:0>										0800
3078	USB INFO	31:16	VPLEN<7:0>								WTCON<3:0>				WTID<3:0>				3C5C
		15:0	DMACHANS<3:0>				RAMBITS<3:0>				RXENDPTS<3:0>				TXENDPTS<3:0>				8C77
307C	USB EOFRST	31:16	—	—	—	—	—	—	NRSTX	NRST	LSEOF<7:0>								0072
		15:0	FSEOF<7:0>								HSEOF<7:0>								7780
3080	USB E0TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
3084	USB E0RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3088	USB E1TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
308C	USB E1RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
3090	USB E2TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
3094	USB E2RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
3098	USB E3TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

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TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
309C	USB E3RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
30A0	US BE4TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
30A4	USB E4RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
30A8	USB E5TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
30AC	USB E5RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
30B0	USB E6TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
30B4	USB E6RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
30B8	USB E7TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>							0000
30BC	USB E7RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>							0000
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>							0000
3100	USB E0CSR0	31:16	Indexed by the same bits in USBIE0CSR0																0000
		15:0																	0000
3108	USB E0CSR2	31:16	Indexed by the same bits in USBIE0CSR2																0000
		15:0																	0000
310C	USB E0CSR3	31:16	Indexed by the same bits in USBIE0CSR3																0000
		15:0																	0000
3110	USB E1CSR0	31:16	Indexed by the same bits in USBIE1CSR0																0000
		15:0																	0000
3114	USB E1CSR1	31:16	Indexed by the same bits in USBIE1CSR1																0000
		15:0																	0000
3118	USB E1CSR2	31:16	Indexed by the same bits in USBIE1CSR2																0000
		15:0																	0000
311C	USB E1CSR3	31:16	Indexed by the same bits in USBIE1CSR3																0000
		15:0																	0000
3120	USB E2CSR0	31:16	Indexed by the same bits in USBIE2CSR0																0000
		15:0																	0000
3124	USB E2CSR1	31:16	Indexed by the same bits in USBIE2CSR1																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

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TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3128	USB E2CSR2	31:16	Indexed by the same bits in USBIE2CSR2																0000
		15:0																	0000
312C	USB E2CSR3	31:16	Indexed by the same bits in USBIE2CSR3																0000
		15:0																	0000
3130	USB E3CSR0	31:16	Indexed by the same bits in USBIE3CSR0																0000
		15:0																	0000
3134	USB E3CSR1	31:16	Indexed by the same bits in USBIE3CSR1																0000
		15:0																	0000
3138	USB E3CSR2	31:16	Indexed by the same bits in USBIE3CSR2																0000
		15:0																	0000
313C	USB E3CSR3	31:16	Indexed by the same bits in USBIE3CSR3																0000
		15:0																	0000
3140	USB E4CSR0	31:16	Indexed by the same bits in USBIE4CSR0																0000
		15:0																	0000
3144	USB E4CSR1	31:16	Indexed by the same bits in USBIE4CSR1																0000
		15:0																	0000
3148	USB E4CSR2	31:16	Indexed by the same bits in USBIE4CSR2																0000
		15:0																	0000
314C	USB E4CSR3	31:16	Indexed by the same bits in USBIE4CSR3																0000
		15:0																	0000
3150	USB E5CSR0	31:16	Indexed by the same bits in USBIE5CSR0																0000
		15:0																	0000
3154	USB E5CSR1	31:16	Indexed by the same bits in USBIE5CSR1																0000
		15:0																	0000
3158	USB E5CSR2	31:16	Indexed by the same bits in USBIE5CSR2																0000
		15:0																	0000
315C	USB E5CSR3	31:16	Indexed by the same bits in USBIE5CSR3																0000
		15:0																	0000
3160	USB E6CSR0	31:16	Indexed by the same bits in USBIE6CSR0																0000
		15:0																	0000
3164	USB E6CSR1	31:16	Indexed by the same bits in USBIE6CSR1																0000
		15:0																	0000
3168	USB E6CSR2	31:16	Indexed by the same bits in USBIE6CSR2																0000
		15:0																	0000
316C	USB E6CSR3	31:16	Indexed by the same bits in USBIE6CSR3																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

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TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3170	USB E7CSR0	31:16	Indexed by the same bits in USBIE7CSR0																0000
		15:0																	0000
3174	USB E7CSR1	31:16	Indexed by the same bits in USBIE7CSR1																0000
		15:0																	0000
3178	USB E7CSR2	31:16	Indexed by the same bits in USBIE7CSR2																0000
		15:0																	0000
317C	USB E7CSR3	31:16	Indexed by the same bits in USBIE7CSR3																0000
		15:0																	0000
3200	USB DMAINT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DMA8IF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF	0000
3204	USB DMA1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3208	USB DMA1A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
320C	USB DMA1N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3214	USB DMA2C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3218	USB DMA2A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
321C	USB DMA2N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3224	USB DMA3C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3228	USB DMA3A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
322C	USB DMA3N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3234	USB DMA4C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3238	USB DMA4A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
323C	USB DMA4N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3244	USB DMA5C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

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TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3248	USB DMA5A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
324C	USB DMA5N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3254	USB DMA6C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3258	USB DMA6A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
325C	USB DMA6N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3264	USB DMA7C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3268	USB DMA7A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
326C	USB DMA7N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3274	USB DMA8C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	DMABRSTM<1:0>		DMAERR	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN	0000
3278	USB DMA8A	31:16	DMAADDR<31:16>																0000
		15:0	DMAADDR<15:0>																0000
327C	USB DMA8N	31:16	DMACOUNT<31:16>																0000
		15:0	DMACOUNT<15:0>																0000
3304	USB E1RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
3308	USB E2RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
330C	USB E3RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
3310	USB E4RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
3314	USB E5RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
3318	USB E6RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000
331C	USB E7RPC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RQPKTCNT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

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TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3340	USB DPBFD	31:16	—	—	—	—	—	—	—	—	EP7TXD	EP6TXD	EP5TXD	EP4TXD	EP3TXD	EP2TXD	EP1TXD	—	0000
		15:0	—	—	—	—	—	—	—	—	EP7RXD	EP6RXD	EP5RXD	EP4RXD	EP3RXD	EP2RXD	EP1RXD	—	0000
3344	USB TMCON1	31:16	THHSRTN<15:0>																05E6
		15:0	TUCH<15:0>																4074
3348	USB TMCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	THSBT<3:0>				0000
3360	USB LPMR1	31:16	—	—	LPM ERRIE	LPM RESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTOIE	—	—	—	LPMNAK(1)	LPMEN<1:0>		LPMRES	LPMXMT	0000
														__(2)	__(2)	__(2)			0000
		15:0	ENDPOINT<3:0>				—	—	—	RMTWAK	HIRD<3:0>				LNKSTATE<3:0>				0000
3364	USB LMPR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	LPMFADDR<6:0>							—	—	LPMERR(1)	LPMRES	LPMNC	LPMACK	LPMNY	LPMST	0000
													__(2)						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

TABLE 11-2: USB REGISTER MAP 2

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
4000	USB CRCON	31:16	—	—	—	—	—	USBIF	USBRF	USBWKUP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	USB IDOVEN	USB IDVAL	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF
15:8	R/W-0	R/W-0	R/W-1	R-0, HS	R-0	R/W-0	R-0, HC	R/W-0
	ISOUPD	SOFTCONN	HSEN	HSMODE	RESET	RESUME	SUSPMODE	SUSPEN
	—	—						
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	FUNC<6:0>						
		—	—	—	—	—	—	—

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-17 **EP7TXIF:EP1TXIF:** Endpoint ‘n’ TX Interrupt Flag bit
1 = Endpoint has a transmit interrupt to be serviced
0 = No interrupt event

bit 16 **EP0IF:** Endpoint 0 Interrupt bit
1 = Endpoint 0 has an interrupt to be serviced
0 = No interrupt event

All EPxTX and EP0 bits are cleared when the byte is read. Therefore, these bits must be read independently from the remaining bits in this register to avoid accidental clearing.

bit 15 **ISOUPD:** ISO Update bit (*Device mode only; unimplemented in Host mode*)
1 = USB module will wait for a SOF token from the time TXPKTRDY is set before sending the packet
0 = No change in behavior

This bit only affects endpoints performing isochronous transfers when in *Device mode*. This bit is unimplemented in *Host mode*.

bit 14 **SOFTCONN:** Soft Connect/Disconnect Feature Selection bit
1 = The USB D+/D- lines are enabled and active
0 = The USB D+/D- lines are disabled and are tri-stated

This bit is only available in *Device mode*.

bit 13 **HSEN:** Hi-Speed Enable bit
1 = The USB module will negotiate for Hi-Speed mode when the device is reset by the hub
0 = Module only operates in Full-Speed mode

bit 12 **HSMODE:** Hi-Speed Mode Status bit
1 = Hi-Speed mode successfully negotiated during USB reset
0 = Module is not in Hi-Speed mode

In *Device mode*, this bit becomes valid when a USB reset completes. In *Host mode*, it becomes valid when the RESET bit is cleared.

bit 11 **RESET:** Module Reset Status bit
1 = Reset signaling is present on the bus
0 = Normal module operation

In *Device mode*, this bit is read-only. In *Host mode*, this bit is read/write.

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0 (CONTINUED)

bit 10 **RESUME:** Resume from Suspend control bit
1 = Generate Resume signaling when the device is in Suspend mode
0 = Stop Resume signaling

In *Device mode*, the software should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In *Host mode*, the software should clear this bit after 20 ms.

bit 9 **SUSPMODE:** Suspend Mode status bit
1 = The USB module is in Suspend mode
0 = The USB module is in Normal operations

This bit is read-only in Device mode. In Host mode, it can be set by software, and is cleared by hardware.

bit 8 **SUSPEN:** Suspend Mode Enable bit
1 = Suspend mode is enabled
0 = Suspend mode is not enabled

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FUNC<6:0>:** Device Function Address bits

These bits are only available in Device mode. This field is written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets.

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REGISTER 11-2: USBCSR1: USB CONTROL STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	U-0
	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-17 **EP7TXIE:EP1TXIE:** Endpoint ‘n’ Transmit Interrupt Enable bits
1 = Endpoint Transmit interrupt events are enabled
0 = Endpoint Transmit interrupt events are not enabled

bit 16 **EP0IE:** Endpoint 0 Interrupt Enable bit
1 = Endpoint 0 interrupt events are enabled
0 = Endpoint 0 interrupt events are not enabled

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-1 **EP7RXIF:EP1RXIF:** Endpoint ‘n’ RX Interrupt bit
1 = Endpoint has a receive event to be serviced
0 = No interrupt event

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
	VBUSIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE
23:16	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	VBUSIF	SESSRQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	U-0
	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **VBUSIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled

bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled

bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled

bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled

bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled

bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled

bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled

bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled

bit 23 **VBUSIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt

bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected

bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected

bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

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REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2 (CONTINUED)

bit 19 **SOFIF:** Start of Frame Interrupt bit
1 = A new frame has started
0 = No start of frame detected

bit 18 **RESETIF:** Reset/Babble Interrupt bit
1 = In *Host mode*, indicates babble is detected. In *Device mode*, indicates reset signaling is detected on the bus.
0 = No reset/babble detected

bit 17 **RESUMEIF:** Resume Interrupt bit
1 = Resume signaling is detected on the bus while USB module is in Suspend mode
0 = No Resume signaling detected

bit 16 **SUSPIF:** Suspend Interrupt bit
1 = Suspend signaling is detected on the bus *(Device mode)*
0 = No suspend signaling detected

bit 15-8 **Unimplemented:** Read as '0'

bit 7-1 **EP7RXIE:EP1RXIE:** Endpoint 'n' Receive Interrupt Enable bit
1 = Receive interrupt is enabled for this endpoint
0 = Receive interrupt is not enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 11-4: USBCSR3: USB CONTROL STATUS REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FORCEHST	FIFOACC	FORCEFS	FORCEHS	PACKET	TESTK	TESTJ	NAK
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ENDPOINT<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	RFRMUM<10:8>		
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RFRMNUM<7:0>							

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FORCEHST:** Test Mode Force Host Select bit
1 = Forces USB module into *Host mode*, regardless of whether it is connected to any peripheral
0 = Normal operation

bit 30 **FIFOACC:** Test Mode Endpoint 0 FIFO Transfer Force bit
1 = Transfers the packet in the Endpoint 0 TX FIFO to the Endpoint 0 RX FIFO
0 = No transfer

bit 29 **FORCEFS:** Test mode Force Full-Speed Mode Select bit
This bit is only active if FORCEHST = 1.
1 = Forces USB module into Full-Speed mode. Undefined behavior if FORCEHS = 1.
0 = If FORCEHS = 0, places USB module into Low-Speed mode.

bit 28 **FORCEHS:** Test mode Force Hi-Speed Mode Select bit
This bit is only active if FORCEHST = 1.
1 = Forces USB module into Hi-Speed mode. Undefined behavior if FORCEFS = 1.
0 = If FORCEFS = 0, places USB module into Low-Speed mode.

bit 27 **PACKET:** Test_Packet Test Mode Select bit
This bit is only active if module is in Hi-Speed mode.
1 = The USB module repetitively transmits on the bus a 53-byte test packet. Test packet must be loaded into the Endpoint 0 FIFO before the test mode is entered.
0 = Normal operation

bit 26 **TESTK:** Test_K Test Mode Select bit
1 = Enters Test_K test mode. The USB module transmits a continuous K on the bus.
0 = Normal operation
This bit is only active if the USB module is in Hi-Speed mode.

bit 25 **TESTJ:** Test_J Test Mode Select bit
1 = Enters Test_J test mode. The USB module transmits a continuous J on the bus.
0 = Normal operation
This bit is only active if the USB module is in Hi-Speed mode.

bit 24 **NAK:** Test_SE0_NAK Test Mode Select bit
1 = Enter Test_SE0_NAK test mode. The USB module remains in Hi-Speed mode but responds to any valid IN token with a NAK
0 = Normal operation
This mode is only active if module is in Hi-Speed mode.

bit 23-20 **Unimplemented:** Read as ‘0’

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REGISTER 11-4: USBCSR3: USB CONTROL STATUS REGISTER 3 (CONTINUED)

bit 19-16 **ENDPOINT<3:0>:** Endpoint Registers Select bits
`1111` = Reserved
•
•
•
`1000` = Reserved
`0111` = Endpoint 7
•
•
•
`0000` = Endpoint 0
These bits select which endpoint registers are accessed through addresses 3010-301F.

bit 15-11 **Unimplemented:** Read as '`0`'

bit 10-0 **RFRMNUM<10:0>:** Last Received Frame Number bits

REGISTER 11-5: USBIE0CSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0, HC	R/W-0	R/W-0, HC
	—	—	—	—	—	—	—	FLSHFIFO
					DISPING	DTWREN	DATATGGL	
23:16	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/C-0, HS	R/W-0, HS	R-0, HS	R-0	R-0
	SVCSETEND	SVCRPR	SENDSTALL	SETUPEND	DATAEND	SENTSTALL	TXPKTRDY	RXPKTRDY
	NAKTMOUT	STATPKT	REQPKT	ERROR	SETUPPKT	RXSTALL		
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27 **DISPING:** Disable Ping tokens control bit (*Host mode*)
1 = USB Module will not issue PING tokens in data and status phases of a Hi-Speed Control transfer
0 = Ping tokens are issued

bit 26 **DTWREN:** Data Toggle Write Enable bit (*Host mode*)
1 = Enable the current state of the Endpoint 0 data toggle to be written. Automatically cleared.
0 = Disable data toggle write

bit 25 **DATATGGL:** Data Toggle bit (*Host mode*)
When read, this bit indicates the current state of the Endpoint 0 data toggle.
If DTWREN = 1, this bit is writable with the desired setting.
If DTWREN = 0, this bit is read-only.

bit 24 **FLSHFIFO:** Flush FIFO Control bit
1 = Flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset and the TXPKTRDY/RXPKTRDY bit is cleared. Automatically cleared when the operation completes. Should only be used when TXPKTRDY/RXPKTRDY = 1.
0 = No Flush operation

bit 23 **SVCSETEND:** Clear SETUPEND Control bit (*Device mode*)
1 = Clear the SETUPEND bit in this register. This bit is automatically cleared.
0 = Do not clear

NAKTMOUT: NAK Time-out Control bit (*Host mode*)
1 = Endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the NAKLIM<4:0> bits (USBICSR<28:24>)
0 = Allow the endpoint to continue

bit 22 **SVCRPR:** Serviced RXPKTRDY Clear Control bit (*Device mode*)
1 = Clear the RXPKTRDY bit in this register. This bit is automatically cleared.
0 = Do not clear

STATPKT: Status Stage Transaction Control bit (*Host mode*)
1 = When set at the same time as the TXPKTRDY or REQPKT bit is set, performs a status stage transaction
0 = Do not perform a status stage transaction

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REGISTER 11-5: USBIE0CSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 0) (CONTINUED)

bit 21 **SENDSTALL:** Send Stall Control bit (*Device mode*)
1 = Terminate the current transaction and transmit a STALL handshake. This bit is automatically cleared.
0 = Do not send STALL handshake.

REQPKT: IN transaction Request Control bit (*Host mode*)
1 = Request an IN transaction. This bit is cleared when the RXPKTRDY bit is set.
0 = Do not request an IN transaction

bit 20 **SETUPEND:** Early Control Transaction End Status bit (*Device mode*)
1 = A control transaction ended before the DATAEND bit has been set. An interrupt will be generated and the FIFO flushed at this time.
0 = Normal operation
This bit is cleared by writing a '1' to the SVCSETEND bit in this register.

ERROR: No Response Error Status bit (*Host mode*)
1 = Three attempts have been made to perform a transaction with no response from the peripheral. An interrupt is generated.
0 = Clear this flag. Software must write a '0' to this bit to clear it.

bit 19 **DATAEND:** End of Data Control bit (*Device mode*)
The software sets this bit when:
- Setting TXPKTRDY for the last data packet
- Clearing RXPKTRDY after unloading the last data packet
- Setting TXPKTRDY for a zero length data packet

Hardware clears this bit.

SETUPPKT: Send a SETUP token Control bit (*Host mode*)
1 = When set at the same time as the TXPKTRDY bit is set, the module sends a SETUP token instead of an OUT token for the transaction
0 = Normal OUT token operation
Setting this bit also clears the Data Toggle.

bit 18 **SENTSTALL:** STALL sent status bit (*Device mode*)
1 = STALL handshake has been transmitted
0 = Software clear of bit

RXSTALL: STALL handshake received Status bit (*Host mode*)
1 = STALL handshake was received
0 = Software clear of bit

bit 17 **TXPKTRDY:** TX Packet Ready Control bit
1 = Data packet has been loaded into the FIFO. It is cleared automatically.
0 = No data packet is ready for transmit

bit 16 **RXPKTRDY:** RX Packet Ready Status bit
1 = Data packet has been received. Interrupt is generated (when enabled) when this bit is set.
0 = No data packet has been received
This bit is cleared by setting the SVCRPR bit.

bit 15-0 **Unimplemented:** Read as '0'

REGISTER 11-6: USBIE0CSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	NAKLIM<4:0>				
23:16	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SPEED<1:0>		—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	RXCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-24 **NAKLIM<4:0>:** Endpoint 0 NAK Limit bits

The number of frames/microframes (Hi-Speed transfers) after which Endpoint 0 should time-out on receiving a stream of NAK responses.

bit 23-22 **SPEED<1:0>:** Operating Speed Control bits
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-7 **Unimplemented:** Read as ‘0’

bit 6-0 **RXCNT<6:0>:** Receive Count bits

The number of received data bytes in the Endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while the RXPKTRDY bit is set.

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REGISTER 11-7: USBIE0CSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-0	R-x	R-x	R-x	R-1	R-0
	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **MPRXEN:** Automatic Amalgamation Option bit
1 = Automatic amalgamation of bulk packets is done
0 = No automatic amalgamation

bit 30 **MPTXEN:** Automatic Splitting Option bit
1 = Automatic splitting of bulk packets is done
0 = No automatic splitting

bit 29 **BIGEND:** Byte Ordering Option bit
1 = Big Endian ordering
0 = Little Endian ordering

bit 28 **HBRXEN:** High-bandwidth RX ISO Option bit
1 = High-bandwidth RX ISO endpoint support is selected
0 = No High-bandwidth RX ISO support

bit 27 **HBTXEN:** High-bandwidth TX ISO Option bit
1 = High-bandwidth TX ISO endpoint support is selected
0 = No High-bandwidth TX ISO support

bit 26 **DYNFIFOS:** Dynamic FIFO Sizing Option bit
1 = Dynamic FIFO sizing is supported
0 = No Dynamic FIFO sizing

bit 25 **SOFTCONE:** Soft Connect/Disconnect Option bit
1 = Soft Connect/Disconnect is supported
0 = Soft Connect/Disconnect is not supported

bit 24 **UTMIDWID:** UTMI+ Data Width Option bit
Always ‘0’, indicating 8-bit UTMI+ data width

bit 23-0 **Unimplemented:** Read as ‘0’

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AUTOSET	ISO	MODE	DMAREQEN	FRCDATTG	DMAREQMD	—	—
		—					DATAWEN	DATATGGL
23:16	R/W-0, HS	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0	R/W-0, HS	R/W-0	R/W-0, HC
	INCOMPTX	CLRDT	SENTSTALL	SENDSTALL	FLUSH	UNDERRUN	FIFONE	TXPKTRDY
	NAKTMOUT		RXSTALL	SETUPPKT		ERROR		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					TXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXMAXP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **AUTOSET:** Auto Set Control bit

1 = TXPKTRDY will be automatically set when data of the maximum packet size (value in TXMAXP) is loaded into the TX FIFO. If a packet of less than the maximum packet size is loaded, then TXPKTRDY will have to be set manually.

0 = TXPKTRDY must be set manually for all packet sizes

bit 30 **ISO:** Isochronous TX Endpoint Enable bit (Device mode)

1 = Enables the endpoint for Isochronous transfers

0 = Disables the endpoint for Isochronous transfers and enables it for Bulk or Interrupt transfers.

This bit only has an effect in Device mode. In Host mode, it always returns zero.

bit 29 **MODE:** Endpoint Direction Control bit

1 = Endpoint is TX

0 = Endpoint is RX

This bit only has any effect where the same endpoint FIFO is used for both TX and RX transactions.

bit 28 **DMAREQEN:** Endpoint DMA Request Enable bit

1 = DMA requests are enabled for this endpoint

0 = DMA requests are disabled for this endpoint

bit 27 **FRCDATTG:** Force Endpoint Data Toggle Control bit

1 = Forces the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.

0 = No forced behavior

bit 26 **DMAREQMD:** Endpoint DMA Request Mode Control bit

1 = DMA Request Mode 1

0 = DMA Request Mode 0

This bit must not be cleared either before or in the same cycle as the DMAREQEN bit is cleared.

bit 25 **DATAWEN:** Data Toggle Write Enable bit (Host mode)

1 = Enable the current state of the TX Endpoint data toggle (DATATGGL) to be written

0 = Disables writing the DATATGGL bit

bit 24 **DATATGGL:** Data Toggle Control bit (Host mode)

When read, this bit indicates the current state of the TX Endpoint data toggle. If DATAWEN = 1, this bit may be written with the required setting of the data toggle. If DATAWEN = 0, any value written to this bit is ignored.

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REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7) (CONTINUED)

bit 23 **INCOMPTX:** Incomplete TX Status bit (Device mode)

1 = For high-bandwidth Isochronous endpoint, a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts

0 = Normal operation

In anything other than isochronous transfers, this bit will always return 0.

NAKTMOUT: NAK Time-out status bit (Host mode)

1 = TX endpoint is halted following the receipt of NAK responses for longer than the NAKLIM setting

0 = Written by software to clear this bit

bit 22 **CLRDT:** Clear Data Toggle Control bit

1 = Resets the endpoint data toggle to 0

0 = Do not clear the data toggle

bit 21 **SENTSTALL:** STALL handshake transmission status bit (Device mode)

1 = STALL handshake is transmitted. The FIFO is flushed and the TXPKTRDY bit is cleared.

0 = Written by software to clear this bit

RXSTALL: STALL receipt bit (Host mode)

1 = STALL handshake is received. Any DMA request in progress is stopped, the FIFO is completely flushed and the TXPKTRDY bit is cleared.

0 = Written by software to clear this bit

bit 20 **SENDSTALL:** STALL handshake transmission control bit (Device mode)

1 = Issue a STALL handshake to an IN token

0 = Terminate stall condition

This bit has no effect when the endpoint is being used for Isochronous transfers.

SETUPPKT: Definition bit (Host mode)

1 = When set at the same time as the TXPKTRDY bit is set, send a SETUP token instead of an OUT token for the transaction. This also clears the Data Toggle.

0 = Normal OUT token for the transaction

bit 19 **FLUSH:** FIFO Flush control bit

1 = Flush the latest packet from the endpoint TX FIFO. The FIFO pointer is reset, the TXPKTRDY bit is cleared and an interrupt is generated.

0 = Do not flush the FIFO

bit 18 **UNDERRUN:** Underrun status bit (Device mode)

1 = An IN token has been received when the TXPKTRDY bit is not set.

0 = Written by software to clear this bit.

ERROR: Handshake failure status bit (Host mode)

1 = Three attempts have been made to send a packet and no handshake packet has been received

0 = Written by software to clear this bit.

bit 17 **FIFONE:** FIFO Not Empty status bit

1 = There is at least 1 packet in the TX FIFO

0 = TX FIFO is empty

bit 16 **TXPKTRDY:** TX Packet Ready Control bit

The software sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. This bit is also automatically cleared prior to loading a second packet into a double-buffered FIFO.

REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7) (CONTINUED)

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **TXMAXP<10:0>:** Maximum TX Payload per transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

TXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

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REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R-0	R/W-0
	AUTOCLR	ISO	DMAREQEN	DISNYET	DMAREQMD	—	—	INCOMPRX
		AUTORQ		PIDERR		DATATWEN	DATATGGL	
23:16	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0, HC	R-0, HS	R/W-0, HS	R-0, HS, HC	R/W-0, HS
	CLRDT	SENTSTALL	SENDSTALL	FLUSH	DATAERR	OVERRUN	FIFOFULL	RXPKTRDY
		RXSTALL	REQPKT		DERRNAKT	ERROR		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					RXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXMAXP<7:0>							

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **AUTOCLR:** RXPKTRDY Automatic Clear Control bit

1 = RXPKTRDY will be automatically cleared when a packet of RXMAXP bytes has been unloaded from the RX FIFO. When packets of less than the maximum packet size are unloaded, RXPKTRDY will have to be cleared manually. When using a DMA to unload the RX FIFO, data is read from the RX FIFO in 4-byte chunks regardless of the RXMAXP.

0 = No automatic clearing of RXPKTRDY

This bit should not be set for high-bandwidth Isochronous endpoints.

bit 30 **ISO:** Isochronous Endpoint Control bit (*Device mode*)

1 = Enable the RX endpoint for Isochronous transfers

0 = Enable the RX endpoint for Bulk/Interrupt transfers

AUTORQ: Automatic Packet Request Control bit (*Host mode*)

1 = REQPKT will be automatically set when RXPKTRDY bit is cleared.

0 = No automatic packet request

This bit is automatically cleared when a short packet is received.

bit 29 **DMAREQEN:** DMA Request Enable Control bit

1 = Enable DMA requests for the RX endpoint.

0 = Disable DMA requests for the RX endpoint.

bit 28 **DISNYET:** Disable NYET Handshakes Control/PID Error Status bit (*Device mode*)

1 = In Bulk/Interrupt transactions, disables the sending of NYET handshakes. All successfully received RX packets are ACKed including at the point at which the FIFO becomes full.

0 = Normal operation.

In Bulk/Interrupt transactions, this bit only has any effect in Hi-Speed mode, in which mode it should be set for all Interrupt endpoints.

PIDERR: PID Error Status bit (*Host mode*)

1 = In ISO transactions, this indicates a PID error in the received packet.

0 = No error

bit 27 **DMAREQMD:** DMA Request Mode Selection bit

1 = DMA Request Mode 1

0 = DMA Request Mode 0

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 26 **DATATWEN:** Data Toggle Write Enable Control bit (*Host mode*)

1 = DATATGGL can be written
0 = DATATGGL is not writable

bit 25 **DATATGGL:** Data Toggle bit (*Host mode*)

When read, this bit indicates the current state of the endpoint data toggle.

If DATATWEN = 1, this bit may be written with the required setting of the data toggle.

If DATATWEN = 0, any value written to this bit is ignored.

bit 24 **INCOMPRX:** Incomplete Packet Status bit

1 = The packet in the RX FIFO during a high-bandwidth Isochronous/Interrupt transfer is incomplete because parts of the data were not received
0 = Written by then software to clear this bit

In anything other than Isochronous transfer, this bit will always return 0.

bit 23 **CLRDT:** Clear Data Toggle Control bit

1 = Reset the endpoint data toggle to 0
0 = Leave endpoint data toggle alone

bit 22 **SENTSTALL:** STALL Handshake Status bit (*Device mode*)

1 = STALL handshake is transmitted
0 = Written by the software to clear this bit

RXSTALL: STALL Handshake Receive Status bit (*Host mode*)

1 = A STALL handshake has been received. An interrupt is generated.
0 = Written by the software to clear this bit

bit 21 **SENDSTALL:** STALL Handshake Control bit (*Device mode*)

1 = Issue a STALL handshake
0 = Terminate stall condition

REQPKT: IN Transaction Request Control bit (*Host mode*)

1 = Request an IN transaction.
0 = No request

This bit is cleared when RXPKTRDY is set.

bit 20 **FLUSH:** Flush FIFO Control bit

1 = Flush the next packet to be read from the endpoint RX FIFO. The FIFO pointer is reset and the RXPKTRDY bit is cleared. This should only be used when RXPKTRDY is set. If the FIFO is double-buffered, FLUSH may need to be set twice to completely clear the FIFO.
0 = Normal FIFO operation

This bit is automatically cleared.

bit 19 **DATAERR:** Data Packet Error Status bit (*Device mode*)

1 = The data packet has a CRC or bit-stuff error.
0 = No data error

This bit is cleared when RXPKTRDY is cleared. This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

DERRNAKT: Data Error/NAK Time-out Status bit (*Host mode*)

1 = The data packet has a CRC or bit-stuff error. In Bulk mode, the RX endpoint is halted following the receipt of NAK responses for longer than the time set as the NAK limit.
0 = No data or NAK time-out error

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REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

ERROR: No Data Packet Received Status bit (*Host mode*)

1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.

0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

bit 17 **FIFOFULL:** FIFO Full Status bit

1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space

bit 16 **RXPKTRDY:** Data Packet Reception Status bit

1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies RXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by RXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

Note: Transfer size greater than RxMaxP is handled by DMA Mode 1 only.

REGISTER 11-10: USBIENCSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXINTERV<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			
15:8	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	RXCNT<13:8>					
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXCNT<7:0>							

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **TXINTERV<7:0>:** Endpoint TX Polling Interval/NAK Limit bits (*Host mode*)

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and interpretation for these bits:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low/Full	0x01 to 0xFF	Polling interval is ‘m’ frames.
	High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames.
Isochronous	Full or High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames/microframes.
Bulk	Full or High	0x02 to 0x10	NAK limit is $2^{(m-1)}$ frames/microframes. A value of ‘0’ or ‘1’ disables the NAK time-out function.

bit 23-22 **SPEED<1:0>:** TX Endpoint Operating Speed Control bits (*Host mode*)
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-20 **PROTOCOL<1:0>:** TX Endpoint Protocol Control bits
11 = Interrupt
10 = Bulk
01 = Isochronous
00 = Control

bit 19-16 **TEP<3:0>:** TX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **RXCNT<13:0>:** Receive Count bits

The number of received data bytes in the endpoint RX FIFO. The value returned changes as the contents of the FIFO change and is only valid while RXPKTRDY is set.

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REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXINTERV<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **RXFIFOSZ<3:0>:** Receive FIFO Size bits
`1111` = Reserved
`1110` = Reserved
`1101` = 8192 bytes
`1100` = 4096 bytes
•
•
•
`0011` = 8 bytes
`0010` = Reserved
`0001` = Reserved
`0000` = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 27-24 **TXFIFOSZ<3:0>:** Transmit FIFO Size bits
`1111` = Reserved
`1110` = Reserved
`1101` = 8192 bytes
`1100` = 4096 bytes
•
•
•
`0011` = 8 bytes
`0010` = Reserved
`0001` = Reserved
`0000` = Reserved or endpoint has not been configured

This register only has this interpretation when dynamic sizing is not selected. It is not valid where dynamic FIFO sizing is used.

bit 23-16 **Unimplemented:** Read as ‘`0`’

REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7) (CONTINUED)

bit 15-8 **RXINTERV<7:0>:** Endpoint RX Polling Interval/NAK Limit bits

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and meaning for this field:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low/Full	0x01 to 0xFF	Polling interval is ‘m’ frames.
	High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames.
Isochronous	Full or High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames/microframes.
Bulk	Full or High	0x02 to 0x10	NAK limit is $2^{(m-1)}$ frames/microframes. A value of ‘0’ or ‘1’ disables the NAK time-out function.

bit 7-6 **SPEED<1:0>:** RX Endpoint Operating Speed Control bits
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 5-4 **PROTOCOL<1:0>:** RX Endpoint Protocol Control bits
11 = Interrupt
10 = Bulk
01 = Isochronous
00 = Control

bit 3-0 **TEP<3:0>:** RX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

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REGISTER 11-12: USBFIFOx: USB FIFO DATA REGISTER ‘x’ (‘x’ = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** USB Transmit/Receive FIFO Data bits

Writes to this register loads data into the TxFIFO for the corresponding endpoint. Reading from this register unloads data from the RxFIFO for the corresponding endpoint.

Transfers may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all transfers associated with one packet must be of the same width so that data is consistently byte-, word- or double-word aligned. The last transfer may contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXDPB	RXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXDPB	TXFIFOSZ<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	TXEDMA	RXEDMA
7:0	R-1	R-0	R-0	R-0	R-0	R-0	R/W-0, HC	R/W-0
	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28 **RXDPB:** RX Endpoint Double-packet Buffering Control bit
1 = Double-packet buffer is supported. This doubles the size set in RXFIFOSZ.
0 = Double-packet buffer is not supported

bit 27-24 **RXFIFOSZ<3:0>:** RX Endpoint FIFO Packet Size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = 4096 bytes
1000 = 2048 bytes
0111 = 1024 bytes
0110 = 512 bytes
0101 = 256 bytes
0100 = 128 bytes
0011 = 64 bytes
0010 = 32 bytes
0001 = 16 bytes
0000 = 8 bytes

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20 **TXDPB:** TX Endpoint Double-packet Buffering Control bit
1 = Double-packet buffer is supported. This doubles the size set in TXFIFOSZ.
0 = Double-packet buffer is not supported

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REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 19-16 **TXFIFOSZ<3:0>:** TX Endpoint FIFO packet size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = 4096 bytes
1000 = 2048 bytes
0111 = 1024 bytes
0110 = 512 bytes
0101 = 256 bytes
0100 = 128 bytes
0011 = 64 bytes
0010 = 32 bytes
0001 = 16 bytes
0000 = 8 bytes

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **TXEDMA:** TX Endpoint DMA Assertion Control bit
1 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.
0 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 8 **RXEDMA:** RX Endpoint DMA Assertion Control bit
1 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.
0 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 7 **BDEV:** USB Device Type bit
1 = USB is operating as a 'B' device
0 = USB is operating as an 'A' device

bit 6 **FSDEV:** Full-Speed/Hi-Speed device detection bit (*Host mode*)
1 = A Full-Speed or Hi-Speed device has been detected being connected to the port
0 = No Full-Speed or Hi-Speed device detected

bit 5 **LSDEV:** Low-Speed Device Detection bit (*Host mode*)
1 = A Low-Speed device has been detected being connected to the port
0 = No Low-Speed device detected

bit 4-3 **VBUS<1:0>:** VBUS Level Detection bits
11 = Above VBUS Valid
10 = Above AValid, below VBUS Valid
01 = Above Session End, below AValid
00 = Below Session End

bit 2 **HOSTMODE:** Host Mode bit
1 = USB module is acting as a Host
0 = USB module is not acting as a Host

bit 1 **HOSTREQ:** Host Request Control bit
'B' device only:
1 = USB module initiates the Host Negotiation when Suspend mode is entered. This bit is cleared when Host Negotiation is completed.
0 = Host Negotiation is not taking place

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 0 **SESSION:** Active Session Control/Status bit

'A' device:

1 = Start a session

0 = End a session

'B' device:

1 = (Read) Session has started or is in progress, (Write) Initiate the Session Request Protocol

0 = When USB module is in Suspend mode, clearing this bit will cause a software disconnect

Clearing this bit when the USB module is not suspended will result in undefined behavior.

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REGISTER 11-14: USBFIFOA: USB FIFO ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXFIFOAD<12:8>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXFIFOAD<7:0>							
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXFIFOAD<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXFIFOAD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-16 **RXFIFOAD<12:0>:** Receive Endpoint FIFO Address bits

Start address of the endpoint FIFO in units of 8 bytes as follows:

1111111111111 = 0xFFF8
•
•
•
0000000000010 = 0x0010
0000000000001 = 0x0008
0000000000000 = 0x0000

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-0 **TXFIFOAD<12:0>:** Transmit Endpoint FIFO Address bits

Start address of the endpoint FIFO in units of 8 bytes as follows:

1111111111111 = 0xFFF8
•
•
•
0000000000010 = 0x0010
0000000000001 = 0x0008
0000000000000 = 0x0000

REGISTER 11-15: USBHWVER: USB HARDWARE VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-0
	RC	VERMAJOR<4:0>					VERMINOR<9:8>	
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERMINOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **RC:** Release Candidate bit
1 = USB module was created using a release candidate
0 = USB module was created using a full release

bit 14-10 **VERMAJOR<4:0>:** USB Module Major Version number bits
This read-only number is the Major version number for the USB module.

bit 9-0 **VERMINOR<9:0>:** USB Module Minor Version number bits
This read-only number is the Minor version number for the USB module.

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REGISTER 11-16: USBINFO: USB INFORMATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	VPLEN<7:0>							
23:16	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	WTCON<3:0>				WTID<3:0>			
15:8	R-1	R-0	R-0	R-0	R-1	R-1	R-0	R-0
	DMACHANS<3:0>				RAMBITS<3:0>			
7:0	R-0	R-1	R-1	R-1	R-0	R-1	R-1	R-1
	RXENDPTS<3:0>				TXENDPTS<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **VPLEN<7:0>:** VBUS pulsing charge length bits

Sets the duration of the VBUS pulsing charge in units of 546.1 µs. (The default setting corresponds to 32.77 ms.)

bit 23-20 **WTCON<3:0>:** Connect/Disconnect filter control bits

Sets the wait to be applied to allow for the connect/disconnect filter in units of 533.3 ns. The default setting corresponds to 2.667 µs.

bit 19-6 **WTID<3:0>:** ID delay valid control bits

Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. The default setting corresponds to 52.43ms.

bit 15-12 **DMACHANS<3:0>:** DMA Channels bits

These read-only bits provide the number of DMA channels in the USB module. For the PIC32MZ DAK/DAL/DAR/DAS family, this number is 8.

bit 11-8 **RAMBITS<3:0>:** RAM address bus width bits

These read-only bits provide the width of the RAM address bus. For the PIC32MZ DAK/DAL/DAR/DAS family, this number is 12.

bit 7-4 **RXENDPTS<3:0>:** Included RX Endpoints bits

This read-only register gives the number of RX endpoints in the design. For the PIC32MZ DAK/DAL/DAR/DAS family, this number is 7.

bit 3-0 **TXENDPTS<3:0>:** Included TX Endpoints bits

These read-only bits provide the number of TX endpoints in the design. For the PIC32MZ DAK/DAL/DAR/DAS family, this number is 7.

REGISTER 11-17: USBEOFRST: USB END-OF-FRAME/SOFT RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	NRSTX	NRST
23:16	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-0	R/W-1	R/W-0
	LSEOF<7:0>							
15:8	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-1	R/W-1	R/W-1
	FSEOF<7:0>							
7:0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R.W-0	R/W-0	R/W-0
	HSEOF<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **NRSTX:** Reset of XCLK Domain bit
1 = Reset the XCLK domain, which is clock recovered from the received data by the PHY
0 = Normal operation

bit 24 **NRST:** Reset of CLK Domain bit
1 = Reset the CLK domain, which is clock recovered from the peripheral bus
0 = Normal operation

bit 23-16 **LSEOF<7:0>:** Low-Speed EOF bits
These bits set the Low-Speed transaction in units of 1.067 µs (default setting is 121.6 µs) prior to the EOF to stop new transactions from beginning.

bit 15-8 **FSEOF<7:0>:** Full-Speed EOF bits
These bits set the Full-Speed transaction in units of 533.3 µs (default setting is 63.46 µs) prior to the EOF to stop new transactions from beginning.

bit 7-0 **HSEOF<7:0>:** Hi-Speed EOF bits
These bits set the Hi-Speed transaction in units of 133.3 µs (default setting is 17.07µs) prior to the EOF to stop new transactions from beginning.

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REGISTER 11-18: USBExTXA: USB ENDPOINT 'x' TRANSMIT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	TXHUBPRT<6:0>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULTTRAN	TXHUBADD<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	TXFADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-24 **TXHUBPRT<6:0>:** TX Hub Port bits (*Host mode*)
When a Low-Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, this field records the port number of that USB 2.0 hub.

bit 23 **MULTTRAN:** TX Hub Multiple Translators bit (*Host mode*)
1 = The USB 2.0 hub has multiple transaction translators
0 = The USB 2.0 hub has a single transaction translator

bit 22-16 **TXHUBADD<6:0>:** TX Hub Address bits (*Host mode*)
When a Low-Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, these bits record the address of the USB 2.0 hub.

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **TXFADDR<6:0>:** TX Functional Address bits (*Host mode*)
Specifies the address for the target function that is be accessed through the associated endpoint. It needs to be defined for each TX endpoint that is used.

REGISTER 11-19: USBExRXA: USB ENDPOINT 'x' RECEIVE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RXHUBPRT<6:0>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULTTRAN	RXHUBADD<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RXFADDR<6:0>						

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-24 **RXHUBPRT<6:0>:** RX Hub Port bits (*Host mode*)

When a Low- Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, this field records the port number of that USB 2.0 hub.

bit 23 **MULTTRAN:** RX Hub Multiple Translators bit (*Host mode*)

1 = The USB 2.0 hub has multiple transaction translators

0 = The USB 2.0 hub has a single transaction translator

bit 22-16 **TXHUBADD<6:0>:** RX Hub Address bits (*Host mode*)

When a Low-Speed or Full-Speed device is connected to this endpoint via a Hi-Speed USB 2.0 hub, these bits record the address of the USB 2.0 hub.

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **RXFADDR<6:0>:** RX Functional Address bits (*Host mode*)

Specifies the address for the target function that is be accessed through the associated endpoint. It needs to be defined for each RX endpoint that is used.

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REGISTER 11-20: USBDMAINT: USB DMA INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
	DMA8IF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	DMA3IF	DMA2IF	DMA1IF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **DMAxIF:** DMA Channel ‘x’ Interrupt bit

`1` = The DMA channel has an interrupt event

`0` = No interrupt event

All bits are cleared on a read of the register.

REGISTER 11-21: USBDMAxC: USB DMA CHANNEL ‘x’ CONTROL REGISTER (‘x’ = 1-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	DMABRSTM<1:0>		DMAERR
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMAEP<3:0>				DMAIE	DMAMODE	DMADIR	DMAEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as ‘0’

bit 10-9 **DMABRSTM<1:0>:** DMA Burst Mode Selection bit
- 11 = Burst Mode 3: INCR16, INCR8, INCR4 or unspecified length
- 10 = Burst Mode 2: INCR8, INCR4 or unspecified length
- 01 = Burst Mode 1: INCR4 or unspecified length
- 00 = Burst Mode 0: Bursts of unspecified length

bit 8 **DMAERR:** Bus Error bit
- 1 = A bus error has been observed on the input
- 0 = The software writes this to clear the error

bit 7-4 **DMAEP<3:0>:** DMA Endpoint Assignment bits

These bits hold the endpoint that the DMA channel is assigned to. Valid values are 0-7.

bit 3 **DMAIE:** DMA Interrupt Enable bit
- 1 = Interrupt is enabled for this channel
- 0 = Interrupt is disabled for this channel

bit 2 **DMAMODE:** DMA Transfer Mode bit
- 1 = DMA Mode1 Transfers
- 0 = DMA Mode0 Transfers

bit 1 **DMADIR:** DMA Transfer Direction bit
- 1 = DMA Read (TX endpoint)
- 0 = DMA Write (RX endpoint)

bit 0 **DMAEN:** DMA Enable bit
- 1 = Enable the DMA transfer and start the transfer
- 0 = Disable the DMA transfer

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REGISTER 11-22: USBDMAxA: USB DMA CHANNEL 'x' MEMORY ADDRESS REGISTER ('x' = 1-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMAADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMAADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMAADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Memory Address bits

This register identifies the current memory address of the corresponding DMA channel. The initial memory address written to this register during initialization must have a value such that its modulo 4 value is equal to '0'. The lower two bits of this register are read only and cannot be set by software. As the DMA transfer progresses, the memory address will increment as bytes are transferred.

REGISTER 11-23: USBDMAxN: USB DMA CHANNEL 'x' COUNT REGISTER ('X' = 1-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMACOUNT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMACOUNT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMACOUNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMACOUNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMACOUNT<31:0>:** DMA Transfer Count bits

This register identifies the current DMA count of the transfer. Software will set the initial count of the transfer which identifies the entire transfer length. As the count progresses this count is decremented as bytes are transferred.

REGISTER 11-24: USBExRPC: USB ENDPOINT 'x' REQUEST PACKET COUNT REGISTER (HOST MODE ONLY) ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RQPKTCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RQPKTCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RQPKTCNT<15:0>:** Request Packet Count bits

Sets the number of packets of size MAXP that are to be transferred in a block transfer. This register is only available in *Host mode* when AUTOREQ is set.

REGISTER 11-25: USBDPBFD: USB DOUBLE PACKET BUFFER DISABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	EP7TXD	EP6TXD	EP5TXD	EP4TXD	EP3TXD	EP2TXD	EP1TXD	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	EP7RXD	EP6RXD	EP5RXD	EP4RXD	EP3RXD	EP2RXD	EP1RXD	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as `0'

bit 23-17 **EP7TXD:EP1TXD:** TX Endpoint 'x' Double Packet Buffer Disable bits
1 = TX double packet buffering is disabled for endpoint 'x'
0 = TX double packet buffering is enabled for endpoint 'x'

bit 16-8 **Unimplemented:** Read as '0'

bit 7-1 **EP7RXD:EP1RXD:** RX Endpoint 'x' Double Packet Buffer Disable bits
1 = RX double packet buffering is disabled for endpoint 'x'
0 = RX double packet buffering is enabled for endpoint 'x'

bit 0 **Unimplemented:** Read as '0'

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REGISTER 11-26: USBTMCON1: USB TIMING CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	THHSRTN<15:8>							
23:16	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
	THHSRTN<7:0>							
15:8	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TUCH<15:8>							
7:0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0
	TUCH<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **THHSRTN:<15:0>:** Hi-Speed Resume Signaling Delay bits
These bits set the delay from the end of Hi-Speed resume signaling (acting as a Host) to enable the UTM normal operating mode.

bit 15-0 **TUCH<15:0>:** Chirp Time-out bits
These bits set the chirp time-out. This number, when multiplied by 4, represents the number of USB module clock cycles before the time-out occurs.

Note: Use of this register will allow the Hi-Speed time-out to be set to values that are greater than the maximum specified in the USB 2.0 specification, making the USB module non-compliant.

REGISTER 11-27: USBTMCON2: USB TIMING CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	THBST<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3-0 **THBST<3:0>:** High Speed Time-out Adder bits
These bits represent the value to be added to the minimum high speed time-out period of 736 bit times. The time-out period can be increased in increments of 64 Hi-Speed bit times (133 ns).

Note: Use of this register will allow the Hi-Speed time-out to be set to values that are greater than the maximum specified in the USB 2.0 specification, making the USB module non-compliant.

REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	LPMERRIE	LPMRESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTOIE
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC
	—	—	—	LPMNAK	LPMEN<1:0>		LPMRES	LPMXMT
15:8	R-0	R-0	R-0	R-0	U-0	U-0	U-0	R-0
	ENDPOINT<3:0>				—	—	—	RMTWAK
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	HIRD<3:0>				LNKSTATE<3:0>			

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as ‘0’

bit 29 **LPMERRIE:** LPM Error Interrupt Enable bit
1 = LPMERR interrupt is enabled
0 = LPMERR interrupt is disabled

bit 28 **LPMRESIE:** LPM Resume Interrupt Enable bit
1 = LPMRES interrupt is enabled
0 = LPMRES interrupt is disabled

bit 27 **LPMACKIE:** LPM Acknowledge Interrupt Enable bit
1 = Enable the LPMACK Interrupt
0 = Disable the LPMACK Interrupt

bit 26 **LPMNYIE:** LPM NYET Interrupt Enable bit
1 = Enable the LPMNYET Interrupt
0 = Disable the LPMNYET Interrupt

bit 25 **LPMSTIE:** LPM STALL Interrupt Enable bit
1 = Enable the LPMST Interrupt
0 = Disable the LPMST Interrupt

bit 24 **LPMTOIE:** LPM Time-out Interrupt Enable bit
1 = Enable the LPMTO Interrupt
0 = Disable the LPMTO Interrupt

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20 **LPMNAK:** LPM-only Transaction Setting bit
1 = All endpoints will respond to all transactions other than a LPM transaction with a NAK
0 = Normal transaction operation
Setting this bit to ‘1’ will only take effect after the USB module as been LPM suspended.

bit 19-18 **LPMEN<1:0>:** LPM Enable bits (*Device mode*)
11 = LPM Extended transactions are supported
10 = LPM and Extended transactions are not supported
01 = LPM mode is not supported but Extended transactions are supported
00 = LPM Extended transactions are supported

bit 17 **LPMRES:** LPM Resume bit
1 = Initiate resume (remote wake-up). Resume signaling is asserted for 50 µs.
0 = No resume operation
This bit is self-clearing.

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REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1 (CONTINUED)

bit 16 **LPMXMT:** LPM Transition to the L1 State bit

When in *Device mode*:

`1` = USB module will transition to the L1 state upon the receipt of the next LPM transaction. LPMEN must be set to `'0b11`. Both LPMXMT and LPMEN must be set in the same cycle.

`0` = Maintain current state

When LPMXMT and LPMEN are set, the USB module can respond in the following ways:

- If no data is pending (all TX FIFOs are empty), the USB module will respond with an ACK. The bit will self clear and a software interrupt will be generated.
- If data is pending (data resides in at least one TX FIFO), the USB module will respond with a NYET. In this case, the bit will not self clear however a software interrupt will be generated.

When in *Host mode*:

`1` = USB module will transmit an LPM transaction. This bit is self clearing, and will be immediately cleared upon receipt of any Token or three time-outs have occurred.

`0` = Maintain current state

bit 15-12 **ENDPOINT<3:0>:** LPM Token Packet Endpoint bits

This is the endpoint in the token packet of the LPM transaction.

bit 11-9 **Unimplemented:** Read as ‘0’

bit 8 **RMTWAK:** Remote Wake-up Enable bit

This bit is applied on a temporary basis only and is only applied to the current suspend state.

`1` = Remote wake-up is enabled

`0` = Remote wake-up is disabled

bit 7-4 **HIRD<3:0>:** Host Initiated Resume Duration bits

The minimum time the host will drive resume on the bus. The value in this register corresponds to an actual resume time of:

Resume Time = 50 µs + HIRD * 75 µs. The resulting range is 50 µs to 1200 µs.

bit 3-0 **LNKSTATE<3:0>:** Link State bits

This value is provided by the host to the peripheral to indicate what state the peripheral must transition to after the receipt and acceptance of a LPM transaction. The only valid value for this register is ‘`1`’ for Sleep State (L1). All other values are reserved.

REGISTER 11-29: USBLPMR2: USB LINK POWER MANAGEMENT CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	LPMFADDR<6:0>						
7:0	U-0	U-0	R-0	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	—	—	LPMERRIF	LPMRESIF	LPMNCIF	LPMACKIF	LPMNYIF	LPMSTIF

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14-8 **LPMFADDR<6:0>:** LPM Payload Function Address bits
These bits contain the address of the LPM payload function.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **LPMERRIF:** LPM Error Interrupt Flag bit (*Device mode*)
1 = An LPM transaction was received that had a LINKSTATE field that is not supported. The response will be a STALL.
0 = No error condition

bit 4 **LPMRESIF:** LPM Resume Interrupt Flag bit
1 = The USB module has resumed (for any reason)
0 = No Resume condition

bit 3 **LPMNCIF:** LPM NC Interrupt Flag bit
When in *Device mode*:
1 = The USB module received a LPM transaction and responded with a NYET due to data pending in the RX FIFOs.
0 = No NC interrupt condition

When in *Host mode*:
1 = A LPM transaction is transmitted and has failed to complete. The transaction will have failed because a timeout occurred or there were bit errors in the response for three attempts.
0 = No NC interrupt condition

bit 2 **LPMACKIF:** LPM ACK Interrupt Flag bit
When in *Device mode*:
1 = A LPM transaction was received and the USB Module responded with an ACK
0 = No ACK interrupt condition

When in *Host mode*:
1 = The LPM transaction is transmitted and the device responds with an ACK
0 = No ACK interrupt condition

bit 1 **LPMNYIF:** LPM NYET Interrupt Flag bit
When in *Device mode*:
1 = A LPM transaction is received and the USB Module responded with a NYET
0 = No NYET interrupt flag

When in *Host mode*:
1 = A LPM transaction is transmitted and the device responded with an NYET
0 = No NYET interrupt flag

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REGISTER 11-29: USBLPMR2: USB LINK POWER MANAGEMENT CONTROL REGISTER 2

bit 0 **LPMSTIF:** LPM STALL Interrupt Flag bit

When in *Device mode*:

1 = A LPM transaction was received and the USB Module responded with a STALL

0 = No Stall condition

When in *Host mode*:

1 = A LPM transaction was transmitted and the device responded with a STALL

0 = No Stall condition

REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R/W-1, HS
	—	—	—	—	—	USBIF	USBRF	USBWKUP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	r-1	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	USB IDOVEN	USB IDVAL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26 **USBIF:** USB General Interrupt Flag bit
1 = An event on the USB Bus has occurred
0 = No interrupt from USB module or interrupts have not been enabled

bit 25 **USBRF:** USB Resume Flag bit
1 = Resume from Suspend state. Device wake-up activity can be started.
0 = No Resume activity detected during Suspend, or not in Suspend state

bit 24 **USBWKUP:** USB Activity Status bit
1 = Connect, disconnect, or other activity on USB detected since last cleared
0 = No activity detected on USB

Note: This bit should be cleared just prior to entering sleep, but it should be checked that no activity has already occurred on USB before actually entering sleep.

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15 **Reserved:** Read as ‘1’

bit 14-10 **Unimplemented:** Read as ‘0’

bit 9 **USBIDOVEN:** USB ID Override Enable bit
1 = Enable use of USBIDVAL bit
0 = Disable use of USBIDVAL and instead use the PHY value

bit 8 **USBIDVAL:** USB ID Value bit
1 = ID override value is 1
0 = ID override value is 0

bit 7 **PHYIDEN:** PHY ID Monitoring Enable bit
1 = Enable monitoring of the ID bit from the USB PHY
0 = Disable monitoring of the ID bit from the USB PHY

bit 6 **VBUSMONEN:** VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in VBUS Valid range (between 4.4V and 4.75V)
0 = Disable monitoring for VBUS in VBUS Valid range

bit 5 **ASVALMONEN:** A-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for A-device (between 0.8V and 2.0V)
0 = Disable monitoring for VBUS in Session Valid range for A-device

bit 4 **BSVALMONEN:** B-Device VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session Valid range for B-device (between 0.8V and 4.0V)
0 = Disable monitoring for VBUS in Session Valid range for B-device

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REGISTER 11-30: USBCRCON: USB CLOCK/RESET CONTROL REGISTER (CONTINUED)

bit 3 **SENDMONEN:** Session End VBUS Monitoring for OTG Enable bit
1 = Enable monitoring for VBUS in Session End range (between 0.2V and 0.8V)
0 = Disable monitoring for VBUS in Session End range

bit 2 **USBIE:** USB General Interrupt Enable bit
1 = Enables general interrupt from USB module
0 = Disables general interrupt from USB module

bit 1 **USBRIE:** USB Resume Interrupt Enable bit
1 = Enable remote resume from suspend Interrupt
0 = Disable interrupt to a Remote Devices USB resume signaling

bit 0 **USBWKUPEN:** USB Activity Detection Interrupt Enable bit
1 = Enable interrupt for detection of activity on USB bus in Sleep mode
0 = Disable interrupt for detection of activity on USB bus in Sleep mode

12.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

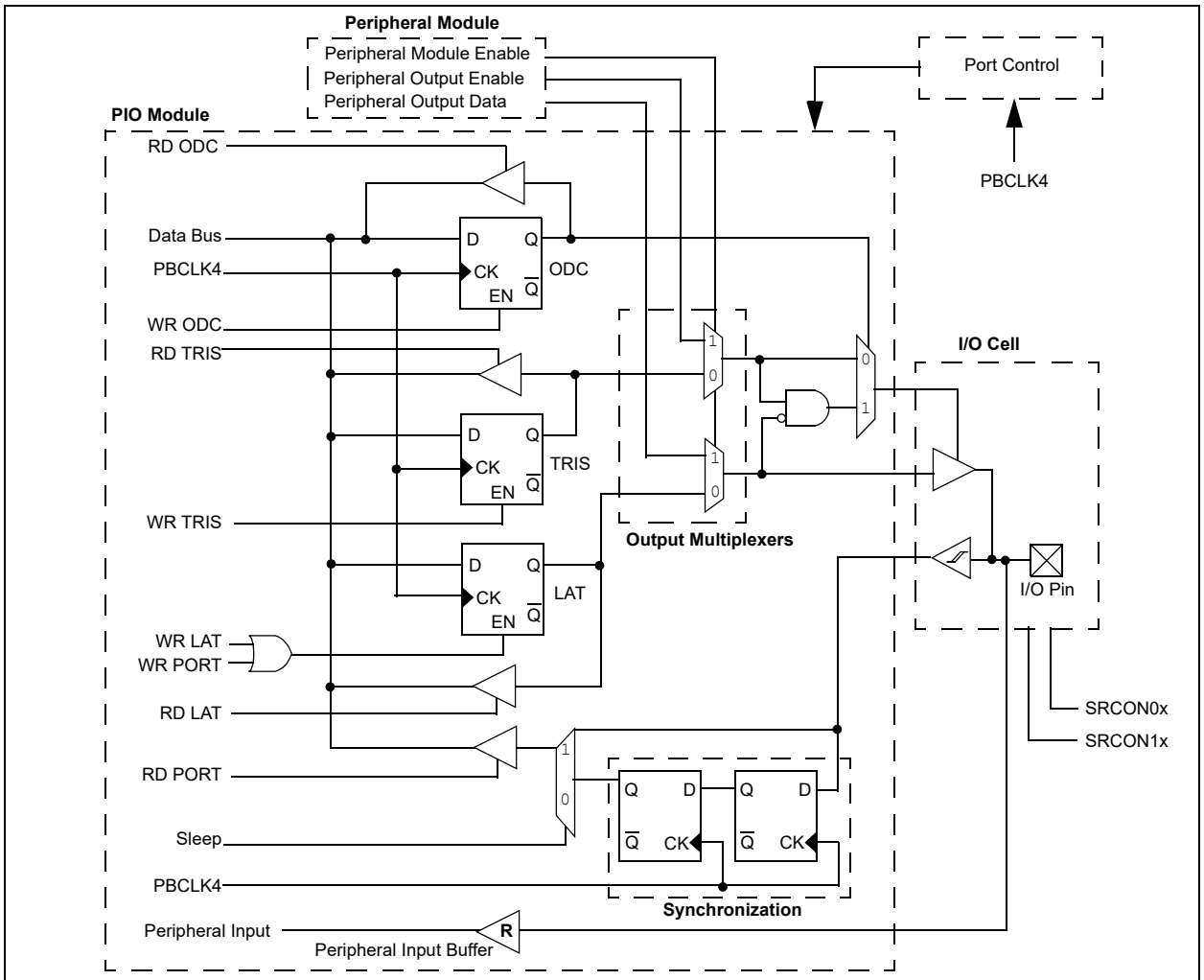
General purpose I/O pins are the simplest of peripherals. They allow the PIC32MZ DAK/DAL/DAR/DAS family of devices to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Some of the key features of the I/O ports are as follows:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



Legend: R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

Note: This block diagram is a general representation of a shared port/peripheral structure for illustration purposes only. The actual structure for any specific port/peripheral combination may be different than it is shown here.

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12.1 Parallel I/O (PIO) Ports

All port pins have ten registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

12.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than V_{DDIO} (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

Refer to the pin name tables (Table 4 and Table 7) for the available pins and their functionality.

12.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (V_{OH} or V_{OL}) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

12.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an NOP.

12.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MZ DAK/DAL/DAR/DAS devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx/CNNEx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins. CNENx enables a mismatch CN interrupt condition when the EDGEDETECT bit (CNCONx<11>) is not set. When the EDGEDETECT bit is set, CNNEx controls the negative edge while CNENx controls the positive.

The CNSTATx/CNFx registers indicate the status of change notice based on the setting of the EDGEDETECT bit. If the EDGEDETECT bit is set to '0', the CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit. If the EDGEDETECT bit is set to '1', the CNFx register indicates whether a change has occurred and through the CNNEx/CNENx registers the edge type of the change that occurred is also indicated.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

An additional control register (CNCONx) is shown in Register 12-3.

12.2 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

12.3 Slew Rate Registers

Each I/O pin can be configured for various types of slew rate control on its associated port. This is controlled by the Slew Rate Control bits in the SRCON1x and SRCON0x registers that are associated with each I/O port.

12.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

12.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation “RPn” in their full pin designation, where “RP” designates a remappable peripheral and “n” is the remappable port number.

12.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (UART, SPI, and CAN), general purpose timer clock inputs, timer-related peripherals (input capture and output compare), interrupt-on-change inputs, and reference clocks (input and output).

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

12.4.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

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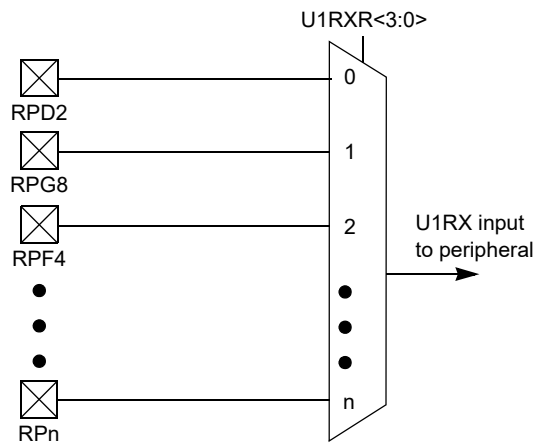
12.4.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 12-1, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-1.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 12-1: INPUT PIN SELECTION

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT3	INT3R	INT3R<3:0>	0000 = RPD2 0001 = RPG8 0010 = RPF4 0011 = Reserved 0100 = RPF1 0101 = RPB9 0110 = RPB10 0111 = RPC14 1000 = RPB5 1001 = Reserved 1010 = RPC1 1011 = RPD14 1100 = RPG1 1101 = RPA14 1110 = RPD6 1111 = Reserved
T2CK	T2CKR	T2CKR<3:0>	
T6CK	T6CKR	T6CKR<3:0>	
IC3	IC3R	IC3R<3:0>	
IC7	IC7R	IC7R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	
$\overline{\text{U2CTS}}$	U2CTSR	U2CTSR<3:0>	
U5RX	U5RXR	U5RXR<3:0>	
$\overline{\text{U6CTS}}$	U6CTSR	U6CTSR<3:0>	
SDI1	SDI1R	SDI1R<3:0>	
SDI3	SDI3R	SDI3R<3:0>	
SDI5	SDI5R	SDI5R<3:0>	
$\overline{\text{SS6}}$	SS6R	SS6R<3:0>	
REFCLKI1	REFCLKI1R	REFCLKI1R<3:0>	
INT4	INT4R	INT4R<3:0>	0000 = RPD3 0001 = RPG7 0010 = RPF5 0011 = RPD11 0100 = RPF0 0101 = RPB1 0110 = RPE5 0111 = RPC13 1000 = RPB3 1001 = Reserved 1010 = RPC4 1011 = Reserved 1100 = RPG0 1101 = RPA15 1110 = RPD7 1111 = Reserved
T5CK	T5CKR	T5CKR<3:0>	
T7CK	T7CKR	T7CKR<3:0>	
IC4	IC4R	IC4R<3:0>	
IC8	IC8R	IC8R<3:0>	
U3RX	U3RXR	U3RXR<3:0>	
$\overline{\text{U4CTS}}$	U4CTSR	U4CTSR<3:0>	
SDI2	SDI2R	SDI2R<3:0>	
SDI4	SDI4R	SDI4R<3:0>	
C1RX	C1RXR	C1RXR<3:0>	
REFCLKI4	REFCLKI4R	REFCLKI4R<3:0>	

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TABLE 12-1: INPUT PIN SELECTION (CONTINUED)

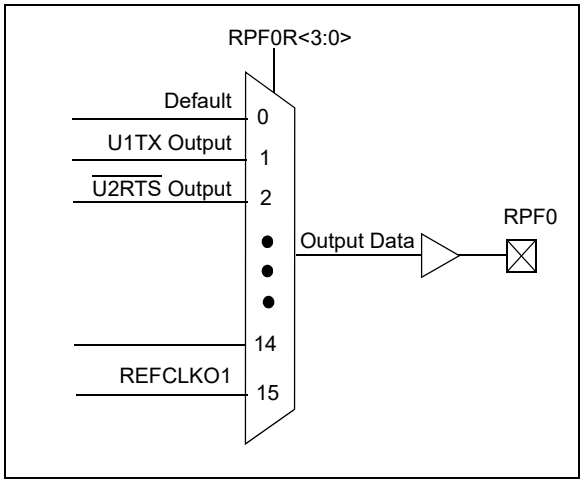
Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT2	INT2R	INT2R<3:0>	0000 = RPD9
T3CK	T3CKR	T3CKR<3:0>	0001 = Reserved
T8CK	T8CKR	T8CKR<3:0>	0010 = RPB8
IC2	IC2R	IC2R<3:0>	0011 = RPB15
IC5	IC5R	IC5R<3:0>	0100 = RPD4
IC9	IC9R	IC9R<3:0>	0101 = RPB0
$\overline{\text{U1CTS}}$	U1CTSR	U1CTSR<3:0>	0110 = RPE3
U2RX	U2RXR	U2RXR<3:0>	0111 = RPB7
$\overline{\text{U5CTS}}$	U5CTSR	U5CTSR<3:0>	1000 = Reserved
$\overline{\text{SS1}}$	SS1R	SS1R<3:0>	1001 = RPF12
$\overline{\text{SS3}}$	SS3R	SS3R<3:0>	1010 = RPD12
$\overline{\text{SS4}}$	SS4R	SS4R<3:0>	1011 = RPF8
$\overline{\text{SS5}}$	SS5R	SS5R<3:0>	1100 = RPC3
C2RX	C2RXR	C2RXR<3:0>	1101 = RPE9
			1110 = Reserved
			1111 = Reserved
INT1	INT1R	INT1R<3:0>	0000 = Reserved
T4CK	T4CKR	T4CKR<3:0>	0001 = RPG9
T9CK	T9CKR	T9CKR<3:0>	0010 = Reserved
IC1	IC1R	IC1R<3:0>	0011 = RPD0
IC6	IC6R	IC6R<3:0>	0100 = Reserved
$\overline{\text{U3CTS}}$	U3CTSR	U3CTSR<3:0>	0101 = RPB6
U4RX	U4RXR	U4RXR<3:0>	0110 = RPD5
U6RX	U6RXR	U6RXR<3:0>	0111 = RPB2
$\overline{\text{SS2}}$	SS2R	SS2R<3:0>	1000 = RPF3
SDI6	SDI6R	SDI6R<3:0>	1001 = Reserved
OCFA	OCFAR	OCFAR<3:0>	1010 = Reserved
REFCLKI3	REFCLKI3R	REFCLKI3R<3:0>	1011 = RPF2
			1100 = RPC2
			1101 = RPE8
			1110 = Reserved
			1111 = Reserved

12.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 12-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 12-2 and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPF0



12.4.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MZ DAK/DAL/DAR/DAS devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

12.4.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting the IOLOCK bit prevents writes to the control registers and clearing the IOLOCK bit allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

12.4.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

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TABLE 12-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect 0001 = U3TX 0010 = $\overline{\text{U4RTS}}$ 0011 = Reserved 0100 = Reserved 0101 = SDO1 0110 = SDO2 0111 = SDO3 1000 = Reserved 1001 = SDO5 1010 = $\overline{\text{SS6}}$ 1011 = OC3 1100 = OC6 1101 = REFCLKO4 1110 = C2OUT 1111 = C1TX
RPG8	RPG8R	RPG8R<3:0>	
RPF4	RPF4R	RPF4R<3:0>	
RPF1	RPF1R	RPF1R<3:0>	
RPB9	RPB9R	RPB9R<3:0>	
RPB10	RPB10R	RPB10R<3:0>	
RPB5	RPB5R	RPB5R<3:0>	
RPC1	RPC1R	RPC1R<3:0>	
RPD14	RPD14R	RPD14R<3:0>	
RPG1	RPG1R	RPG1R<3:0>	
RPA14	RPA14R	RPA14R<3:0>	
RPD6	RPD6R	RPD6R<3:0>	
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect 0001 = U1TX 0010 = $\overline{\text{U2RTS}}$ 0011 = U5TX 0100 = $\overline{\text{U6RTS}}$ 0101 = SDO1 0110 = SDO2 0111 = SDO3 1000 = SDO4 1001 = SDO5 1010 = Reserved 1011 = OC4 1100 = OC7 1101 = Reserved 1110 = Reserved 1111 = REFCLKO1
RPG7	RPG7R	RPG7R<3:0>	
RPF5	RPF5R	RPF5R<3:0>	
RPD11	RPD11R	RPD11R<3:0>	
RPF0	RPF0R	RPF0R<3:0>	
RPB1	RPB1R	RPB1R<3:0>	
RPE5	RPE5R	RPE5R<3:0>	
RPB3	RPB3R	RPB3R<3:0>	
RPC4	RPC4R	RPC4R<3:0>	
RPG0	RPG0R	RPG0R<3:0>	
RPA15	RPA15R	RPA15R<3:0>	
RPD7	RPD7R	RPD7R<3:0>	

TABLE 12-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD9	RPD9R	RPD9R<3:0>	0000 = No Connect 0001 = $\overline{\text{U3RTS}}$ 0010 = U4TX 0011 = Reserved 0100 = U6TX 0101 = $\overline{\text{SS1}}$ 0110 = Reserved 0111 = $\overline{\text{SS3}}$ 1000 = $\overline{\text{SS4}}$ 1001 = $\overline{\text{SS5}}$ 1010 = SDO6 1011 = OC5 1100 = OC8 1101 = Reserved 1110 = C1OUT 1111 = REFCLKO3
RPB8	RPB8R	RPB8R<3:0>	
RPB15	RPB15R	RPB15R<3:0>	
RPD4	RPD4R	RPD4R<3:0>	
RPB0	RPB0R	RPB0R<3:0>	
RPE3	RPE3R	RPE3R<3:0>	
RPB7	RPB7R	RPB7R<3:0>	
RPF12	RPF12R	RPF12R<3:0>	
RPD12	RPD12R	RPD12R<3:0>	
RPF8	RPF8R	RPF8R<3:0>	
RPC3	RPC3R	RPC3R<3:0>	
RPE9	RPE9R	RPE9R<3:0>	
RPG9	RPG9R	RPG9R<3:0>	0000 = No Connect 0001 = $\overline{\text{U1RTS}}$ 0010 = U2TX 0011 = $\overline{\text{U5RTS}}$ 0100 = U6TX 0101 = Reserved 0110 = $\overline{\text{SS2}}$ 0111 = Reserved 1000 = SDO4 1001 = Reserved 1010 = SDO6 1011 = OC2 1100 = OC1 1101 = OC9 1110 = Reserved 1111 = C2TX
RPD0	RPD0R	RPD0R<3:0>	
RPB6	RPB6R	RPB6R<3:0>	
RPD5	RPD5R	RPD5R<3:0>	
RPB2	RPB2R	RPB2R<3:0>	
RPF3	RPF3R	RPF3R<3:0>	
RPC2	RPC2R	RPC2R<3:0>	
RPE8	RPE8R	RPE8R<3:0>	
RPF2	RPF2R	RPF2R<3:0>	

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12.5 I/O Ports Control Registers

TABLE 12-3: PORTA REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	ANSA10	ANSA9	—	—	—	ANSA5	—	—	—	ANSA1	—	0622
0010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
0020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	—	—	RA10	RA9	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
0030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
0040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	—	—	ODCA10	ODCA9	—	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
0050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUA15	CNPUA14	—	—	—	CNPUA10	CNPUA9	—	CNPUA7	CNPUA6	CNPUA5	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
0060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDA15	CNPDA14	—	—	—	CNPDA10	CNPDA9	—	CNPDA7	CNPDA6	CNPDA5	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
0070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEA15	CNIEA14	—	—	—	CNIEA10	CNIEA9	—	CNIEA7	CNIEA6	CNIEA5	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
0090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATA15	CN STATA14	—	—	—	CN STATA10	CN STATA9	—	CN STATA7	CN STATA6	CN STATA5	CN STATA4	CN STATA3	CN STATA2	CN STATA1	CN STATA0	0000
00A0	CNNEA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEA15	CNNEA14	—	—	—	CNNEA10	CNNEA9	—	CNNEA7	CNNEA6	CNNEA5	CNNEA4	CNNEA3	CNNEA2	CNNEA1	CNNEA0	0000
00B0	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFA15	CNFA14	—	—	—	CNFA10	CNFA9	—	CNFA7	CNFA76	CNFA5	CNFA4	CNFA3	CNFA2	CNFA1	CNFA0	0000
00C0	SRCON0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1A15	SR1A14	—	—	—	SR1A10	SR1A9	—	SR1A7	SR1A6	SR1A5	SR1A4	SR1A3	SR1A2	SR1A1	SR1A0	0000
00D0	SRCON1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0A15	SR0A14	—	—	—	SR0A10	SR0A9	—	SR0A7	SR0A6	SR0A5	SR0A4	SR0A3	SR0A2	SR0A1	SR0A0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-4: PORTB REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB15	ANSB14	ANSB13	ANSB12	ANSB11	ANSB10	ANSB9	ANSB8	ANSB7	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	FFBF
0110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
0120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
0130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
0140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
0150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
0160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
0170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
0190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000
01A0	CNNEB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEB15	CNNEB14	CNNEB13	CNNEB12	CNNEB11	CNNEB10	CNNEB9	CNNEB8	CNNEB7	CNNEB6	CNNEB5	CNNEB4	CNNEB3	CNNEB2	CNNEB1	CNNEB0	0000
01B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB15	CNFB14	CNFB13	CNFB12	CNFB11	CNFB10	CNFB9	CNFB8	CNFB7	CNFB76	CNFB5	CNFB4	CNFB3	CNFB2	CNFB1	CNFB0	0000
01C0	SRCON0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1B15	SR1B14	SR1B13	SR1B12	SR1B11	SR1B10	SR1B9	SR1B8	SR1B7	SR1B6	SR1B5	SR1B4	SR1B3	SR1B2	SR1B1	SR1B0	0000
01D0	SRCON1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0B15	SR0B14	SR0B13	SR0B12	SR0B11	SR0B10	SR0B9	SR0B8	SR0B7	SR0B6	SR0B5	SR0B4	SR0B3	SR0B2	SR0B1	SR0B0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-5: PORTC REGISTER MAP

Virtual Address (BF86_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ANSC4	ANSC3	ANSC2	ANSC1	—	001E
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	—	—	TRISC12	—	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	—	901E
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	—	—	—	—	—	—	—	RC4	RC3	RC2	RC1	—	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	—	—	—	—	—	—	—	LATC4	LATC3	LATC2	LATC1	—	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	—	—	—	—	—	—	—	ODCC4	ODCC3	ODCC2	ODCC1	—	0000
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	—	—	—	—	—	—	—	CNPUC4	CNPUC3	CNPUC2	CNPUC1	—	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	—	—	—	—	—	—	—	CNPDC4	CNPDC3	CNPDC2	CNPDC1	—	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEC15	CNIEC14	CNIEC13	CNIEC12	—	—	—	—	—	—	—	CNIEC4	CNIEC3	CNIEC2	CNIEC1	—	0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC15	CNSTATC14	CNSTATC13	CNSTATC12	—	—	—	—	—	—	—	CNSTATC4	CNSTATC3	CNSTATC2	CNSTATC1	—	0000
02A0	CNNEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	—	—	—	—	—	—	—	CNNEC4	CNNEC3	CNNEC2	CNNEC1	—	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	—	—	—	—	—	—	—	CNFC4	CNFC3	CNFC2	CNFC1	—	0000
02C0	SRCON0C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1C15	SR1C14	SR1C13	SR1C12	—	—	—	—	—	—	—	SR1C4	SR1C3	SR1C2	SR1C1	—	0000
02D0	SRCON1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0C15	SR0C14	SR0C13	SR0C12	—	—	—	—	—	—	—	SR0C4	SR0C3	SR0C2	SR0C1	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-6: PORTD REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD15	ANSD14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	—	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FEFF
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	—	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	—	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	—	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	—	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	—	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	CNIED11	CNIED10	CNIED9	—	CNIED7	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	CNIED0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	—	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNED15	CNNED14	CNNED13	CNNED12	CNNED11	CNNED10	CNNED9	—	CNNED7	CNNED6	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	CNNED0	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFD15	CNFD14	CNFD13	CNFD12	CNFD11	CNFD10	CNFD9	—	CNFD7	CNFD6	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	CNFD0	0000
03C0	SRCON0D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1D15	SR1D14	SR1D13	SR1D12	SR1D11	SR1D10	SR1D9	—	SR1D7	SR1D6	SR1D5	SR1D4	SR1D3	SR1D2	SR1D1	SR1D0	0000
03D0	SRCON1D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0D15	SR0D14	SR0D13	SR0D12	SR0D11	SR0D10	SR0D9	—	SR0D7	SR0D6	SR0D5	SR0D4	SR0D3	SR0D2	SR0D1	SR0D0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-7: PORTE REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSE9	ANSE8	ANSE7	ANSE6	—	ANSE4	—	—	ANSE1	—	03D2
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0430	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDE9	CNPDE8	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIEE9	CNIEE8	CNIEE7	CNIEE6	CNIEE5	CNIEE4	CNIEE3	CNIEE2	CNIEE1	CNIEE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATE9	CN STATE8	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEE9	CNNEE8	CNNEE7	CNNEE6	CNNEE5	CNNEE4	CNNEE3	CNNEE2	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFE9	CNFE8	CNFE7	CNFE6	CNFE5	CNFE4	CNFE3	CNFE2	CNFE1	CNFE0	0000
04C0	SRCON0E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR1E9	SR1E8	SR1E7	SR1E6	SR1E5	SR1E4	SR1E3	SR1E2	SR1E1	SR1E0	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR0E9	SR0E8	SR0E7	SR0E6	SR0E5	SR0E4	SR0E3	SR0E2	SR0E1	SR0E0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-8: PORTF REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0500	ANSELF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ANSF13	ANSF12	—	—	—	—	—	—	—	—	—	—	—	—	3000
0510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	313F
0520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	—	—	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
0530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
0540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	—	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000
0550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPUF13	CNPUF12	—	—	—	CNPUF8	—	—	CNPUF5	CNPUF4	CNPUF3	CNPUF2	CNPUF1	CNPUF0	0000
0560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPDF13	CNPDF12	—	—	—	CNPDF8	—	—	CNPDF5	CNPDF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	0000
0570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNIEF13	CNIEF12	—	—	—	CNIEF8	—	—	CNIEF5	CNIEF4	CNIEF3	CNIEF2	CNIEF1	CNIEF0	0000
0590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CN STATF13	CN STATF12	—	—	—	CN STATF8	—	—	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	0000
05A0	CNNEF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNNEF13	CNNEF12	—	—	—	CNNEF8	—	—	CNNEF5	CNNEF4	CNNEF3	CNNEF2	CNNEF1	CNNEF0	0000
05B0	CNFF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNFF13	CNFF12	—	—	—	CNFF8	—	—	CNFF5	CNFF4	CNFF3	CNFF2	CNFF1	CNFF0	0000
05C0	SRCON0F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SR1F13	SR1F12	—	—	—	SR1F8	—	—	SR1F5	SR1F4	SR1F3	SR1F2	SR1F1	SR1F0	0000
05D0	SRCON1F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SR0F13	SR0F12	—	—	—	SR0F8	—	—	SR0F5	SR0F4	SR0F3	SR0F2	SR0F1	SR0F0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-9: PORTG REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSG15	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	83C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISG15	TRISG14	TRISG13	TRISG12	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	TRISG1	TRISG0	F3C3
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RG15	RG14	RG13	RG12	—	—	RG9	RG8	RG7	RG6	—	—	—	—	RG1	RG0	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATG15	LATG14	LATG13	LATG12	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	LATG1	LATG0	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCG15	ODCG14	ODCG13	ODCG12	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	ODCG1	ODCG0	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUG15	CNPUG14	CNPUG13	CNPUG12	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	CNPUG1	CNPUG0	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDG15	CNPDG14	CNPDG13	CNPDG12	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	CNPDG1	CNPDG0	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEG15	CNIEG14	CNIEG13	CNIEG12	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	CNIEG1	CNIEG0	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATG15	CN STATG14	CN STATG13	CN STATG12	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	CN STATG1	CN STATG0	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEG15	CNNEG14	CNNEG13	CNNEG12	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	CNNEG1	CNNEG0	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFG15	CNFG14	CNFG13	CNFG12	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	CNFG1	CNFG0	0000
06C0	SRCON0G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1G15	SR1G14	SR1G13	SR1G12	—	—	SR1G9	SR1G9	SR1G7	SR1G6	—	—	—	—	SR1G1	SR1G0	0000
06D0	SRCON1G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0G15	SR0G14	SR0G13	SR0G12	—	—	SR0G9	SR0G8	SR0G7	SR0G6	—	—	—	—	SR0G1	SR0G0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-10: PORTH REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0700	ANSELH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ANSH11	—	—	—	ANSH7	—	—	ANSH4	ANSH3	—	—	—	0898
0710	TRISH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISH15	TRISH14	TRISH13	TRISH12	TRISH11	TRISH10	TRISH9	TRISH8	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	FFFF
0720	PORTH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RH15	RH14	RH13	RH12	RH11	RH10	RH9	RH8	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	xxxx
0730	LATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATH15	LATH14	LATH13	LATH12	LATH11	LATH10	LATH9	LATH8	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	xxxx
0740	ODCH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCH15	ODCH14	ODCH13	ODCH12	ODCH11	ODCH10	ODCH9	ODCH8	ODCH7	ODCH6	ODCH5	ODCH4	ODCH3	ODCH2	ODCH1	ODCH0	0000
0750	CNPUH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUH15	CNPUH14	CNPUH13	CNPUH12	CNPUH11	CNPUH10	CNPUH9	CNPUH8	CNPUH7	CNPUH6	CNPUH5	CNPUH4	CNPUH3	CNPUH2	CNPUH1	CNPUH0	0000
0760	CNPDH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDH15	CNPDH14	CNPDH13	CNPDH12	CNPDH11	CNPDH10	CNPDH9	CNPDH8	CNPDH7	CNPDH6	CNPDH5	CNPDH4	CNPDH3	CNPDH2	CNPDH1	CNPDH0	0000
0770	CNCONH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0780	CNENH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEH15	CNIEH14	CNIEH13	CNIEH12	CNIEH11	CNIEH10	CNIEH9	CNIEH8	CNIEH7	CNIEH6	CNIEH5	CNIEH4	CNIEH3	CNIEH2	CNIEH1	CNIEH0	0000
0790	CNSTATH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATH15	CN STATH14	CN STATH13	CN STATH12	CN STATH11	CN STATH10	CN STATH9	CN STATH8	CN STATH7	CN STATH6	CN STATH5	CN STATH4	CN STATH3	CN STATH2	CN STATH1	CN STATH0	0000
07A0	CNNEH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEH15	CNNEH14	CNNEH13	CNNEH12	CNNEH11	CNNEH10	CNNEH9	CNNEH8	CNNEH7	CNNEH6	CNNEH5	CNNEH4	CNNEH3	CNNEH2	CNNEH1	CNNEH0	0000
07B0	CNFH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFH15	CNFH14	CNFH13	CNFH12	CNFH11	CNFH10	CNFH9	CNFH8	CNFH7	CNFH6	CNFH5	CNFH4	CNFH3	CNFH2	CNFH1	CNFH0	0000
07C0	SRCON0H	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1H15	SR1H14	SR1H13	SR1H12	SR1H11	SR1H10	SR1H9	SR1H8	SR1H7	SR1H6	SR1H5	SR1H4	SR1H3	SR1H2	SR1H1	SR1H0	0000
07D0	SRCON1H	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0H15	SR0H14	SR0H13	SR0H12	SR0H11	SR0H10	SR0H9	SR0H8	SR0H7	SR0H6	SR0H5	SR0H4	SR0H3	SR0H2	SR0H1	SR0H0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-11: PORTJ REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0800	ANSELJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSJ2	—	—	0004
0810	TRISJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISJ15	TRISJ14	TRISJ13	TRISJ12	TRISJ11	TRISJ10	TRISJ9	TRISJ8	TRISJ7	TRISJ6	TRISJ5	TRISJ4	TRISJ3	TRISJ2	TRISJ1	TRISJ0	FFFF
0820	PORTJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RJ15	RJ14	RJ13	RJ12	RJ11	RJ10	RJ9	RJ8	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	xxxx
0830	LATJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATJ15	LATJ14	LATJ13	LATJ12	LATJ11	LATJ10	LATJ9	LATJ8	LATJ7	LATJ6	LATJ5	LATJ4	LATJ3	LATJ2	LATJ1	LATJ0	xxxx
0840	ODCJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCJ15	ODCJ14	ODCJ13	ODCJ12	ODCJ11	ODCJ10	ODCJ9	ODCJ18	ODCJ7	ODCJ6	ODCJ5	ODCJ4	ODCJ3	ODCJ2	ODCJ1	ODCJ0	0000
0850	CNPUJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUJ15	CNPUJ14	CNPUJ13	CNPUJ12	CNPUJ11	CNPUJ10	CNPUJ9	CNPUJ8	CNPUJ7	CNPUJ6	CNPUJ5	CNPUJ4	CNPUJ3	CNPUJ2	CNPUJ1	CNPUJ0	0000
0860	CNPDJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDJ15	CNPDJ14	CNPDJ13	CNPDJ12	CNPDJ11	CNPDJ10	CNPDJ9	CNPDJ8	CNPDJ7	CNPDJ6	CNPDJ5	CNPDJ4	CNPDJ3	CNPDJ2	CNPDJ1	CNPDJ0	0000
0870	CNCONJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0880	CNENJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEJ15	CNIEJ14	CNIEJ13	CNIEJ12	CNIEJ11	CNIEJ10	CNIEJ9	CNIEJ8	CNIEJ7	CNIEJ6	CNIEJ5	CNIEJ4	CNIEJ3	CNIEJ2	CNIEJ1	CNIEJ0	0000
0890	CNSTATJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATJ15	CN STATJ14	CN STATJ13	CN STATJ12	CN STATJ11	CN STATJ10	CN STATJ9	CN STATJ8	CN STATJ7	CN STATJ6	CN STATJ5	CN STATJ4	CN STATJ3	CN STATJ2	CN STATJ1	CN STATJ0	0000
08A0	CNNEJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEJ15	CNNEJ14	CNNEJ13	CNNEJ12	CNNEJ11	CNNEJ10	CNNEJ9	CNNEJ8	CNNEJ7	CNNEJ6	CNNEJ5	CNNEJ4	CNNEJ3	CNNEJ2	CNNEJ1	CNNEJ0	0000
08B0	CNFJ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFJ15	CNFJ14	CNFJ13	CNFJ12	CNFJ11	CNFJ10	CNFJ9	CNFJ8	CNFJ7	CNFJ6	CNFJ5	CNFJ4	CNFJ3	CNFJ2	CNFJ1	CNFJ0	0000
08C0	SRCON0J	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1J15	SR1J14	SR1J13	SR1J12	SR1J11	SR1J10	SR1J9	SR1J8	SR1J7	SR1J6	SR1J5	SR1J4	SR1J3	SR1J2	SR1J1	SR1J0	0000
08D0	SRCON1J	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0J15	SR0J14	SR0J13	SR0J12	SR0J11	SR0J10	SR0J9	SR0J8	SR0J7	SR0J6	SR0J5	SR0J4	SR0J3	SR0J2	SR0J1	SR0J0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-12: PORTK REGISTER MAP

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0900	ANSELK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSK2	ANSK1	—	0006
0910	TRISK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISK7	TRISK6	TRISK5	TRISK4	TRISK3	TRISK2	TRISK1	TRISK0	00E9
0920	PORTK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RK7	RK6	RK5	RK4	RK3	RK2	RK1	RK0	xxxx
0930	LATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATK7	LATK6	LATK5	LATK4	LATK3	LATK2	LATK1	LATK0	xxxx
0940	ODCK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCK7	ODCK6	ODCK5	ODCK4	ODCK3	ODCK2	ODCK1	ODCK0	0000
0950	CNPUK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUK7	CNPUK6	CNPUK5	CNPUK4	CNPUK3	CNPUK2	CNPUK1	CNPUK0	0000
0960	CNPDK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDK7	CNPDK6	CNPDK5	CNPDK4	CNPDK3	CNPDK2	CNPDK1	CNPDK0	0000
0970	CNCONK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0980	CNENK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNIEK7	CNIEK6	CNIEK5	CNIEK4	CNIEK3	CNIEK2	CNIEK1	CNIEK0	0000
0990	CNSTATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATK7	CN STATK6	CN STATK5	CN STATK4	CN STATK3	CN STATK2	CN STATK1	CN STATK0	0000
09A0	CNNEK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNNEK7	CNNEK6	CNNEK5	CNNEK4	CNNEK3	CNNEK2	CNNEK1	CNNEK0	0000
09B0	CNFK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNFK7	CNFK6	CNFK5	CNFK4	CNFK3	CNFK2	CNFK1	CNFK0	0000
09C0	SRCON0K	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SR1K7	SR1K6	SR1K5	SR1K4	SR1K3	SR1K2	SR1K1	SR1K0	0000
09D0	SRCON1K	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SR0K7	SR0K6	SR0K5	SR0K4	SR0K3	SR0K2	SR0K1	SR0K0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 12-13: PERIPHERAL PIN SELECT INPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1404	INT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT1R<3:0>				0000
1408	INT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT2R<3:0>				0000
140C	INT3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT3R<3:0>				0000
1410	INT4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT4R<3:0>				0000
1418	T2CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T2CKR<3:0>				0000
141C	T3CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T3CKR<3:0>				0000
1420	T4CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T4CKR<3:0>				0000
1424	T5CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T5CKR<3:0>				0000
1428	T6CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T6CKR<3:0>				0000
142C	T7CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T7CKR<3:0>				0000
1430	T8CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T8CKR<3:0>				0000
1434	T9CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T9CKR<3:0>				0000
1438	IC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC1R<3:0>				0000
143C	IC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC2R<3:0>				0000
1440	IC3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC3R<3:0>				0000

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TABLE 12-13: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1444	IC4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC4R<3:0>				0000
1448	IC5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC5R<3:0>				0000
144C	IC6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC6R<3:0>				0000
1450	IC7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC7R<3:0>				0000
1454	IC8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC8R<3:0>				0000
1458	IC9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC9R<3:0>				0000
1460	OCFAR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	OCFAR<3:0>				0000
1468	U1RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1RXR<3:0>				0000
146C	U1CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1CTSR<3:0>				0000
1470	U2RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2RXR<3:0>				0000
1474	U2CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2CTSR<3:0>				0000
1478	U3RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U3RXR<3:0>				0000
147C	U3CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U3CTSR<3:0>				0000
1480	U4RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U4RXR<3:0>				0000
1484	U4CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U4CTSR<3:0>				0000

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Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1488	U5RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U5RXR<3:0>				0000
148C	U5CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U5CTSR<3:0>				0000
1490	U6RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U6RXR<3:0>				0000
1494	U6CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U6CTSR<3:0>				0000
149C	SDI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI1R<3:0>				0000
14A0	SS1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS1R<3:0>				0000
14A8	SDI2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI2R<3:0>				0000
14AC	SS2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS2R<3:0>				0000
14B4	SDI3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI3R<3:0>				0000
14B8	SS3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS3R<3:0>				0000
14C0	SDI4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI4R<3:0>				0000
14C4	SS4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS4R<3:0>				0000
14CC	SDI5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI5R<3:0>				0000
14D0	SS5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS5R<3:0>				0000
14D8	SDI6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI6R<3:0>				0000

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Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14DC	SS6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS6R<3:0>				0000
14E0	C1RXR(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C1RXR<3:0>				0000
14E4	C2RXR(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C2RXR<3:0>				0000
14E8	REFCLKI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI1R<3:0>				0000
14F0	REFCLKI3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI3R<3:0>				0000
14F4	REFCLKI4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKI4R<3:0>				0000

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TABLE 12-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1538	RPA14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA14R<3:0>				0000
153C	RPA15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA15R<3:0>				0000
1540	RPB0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB0R<3:0>				0000
1544	RPB1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB1R<3:0>				0000
1548	RPB2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB2R<3:0>				0000
154C	RPB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB3R<3:0>				0000
1554	RPB5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB5R<3:0>				0000
1558	RPB6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB6R<3:0>				0000
155C	RPB7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB7R<3:0>				0000
1560	RPB8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB8R<3:0>				0000
1564	RPB9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB9R<3:0>				0000
1568	RPB10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB10R<3:0>				0000
157C	RPB15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB15R<3:0>				0000
1584	RPC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC1R<3:0>				0000
1588	RPC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC2R<3:0>				0000
158C	RPC3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC3R<3:0>				0000
15B4	RPC13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC13R<3:0>				0000
15B8	RPC14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC14R<3:0>				0000
15C0	RPD0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD0R<3:0>				0000

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			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15C8	RPD2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD2R<3:0>				0000
15CC	RPD3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD3R<3:0>				0000
15D0	RPD4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD4R<3:0>				0000
15D4	RPD5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD5R<3:0>				0000
15D8	RPD6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD6R<3:0>				0000
15DC	RPD7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD7R<3:0>				0000
15E4	RPD9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD9R<3:0>				0000
15EC	RPD11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD11R<3:0>				0000
15F0	RPD12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD12R<3:0>				0000
15F8	RPD14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD14R<3:0>				0000
160C	RPE3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE3R<3:0>				0000
1614	RPE5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE5R<3:0>				0000
1620	RPE8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE8R<3:0>				0000
1624	RPE9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE9R<3:0>				0000
1640	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF0R<3:0>				0000
1644	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF1R<3:0>				0000
1648	RPF2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF2R<3:0>				0000
164C	RPF3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF3R<3:0>				0000
1650	RPF4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF4R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 12-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1654	RPF5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF5R<3:0>				0000
1660	RPF8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPF8R<3:0>				0000
1670	RPF12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG12R<3:0>				0000
1680	RPG0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
1684	RPG1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG1R<3:0>				0000
169C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG7R<3:0>				0000
16A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG8R<3:0>				0000
16A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPG9R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 12-1: [*pin name*]R: PERIPHERAL PIN SELECT INPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	[*pin name*]R<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3-0 **[*pin name*]R<3:0>:** Peripheral Pin Select Input bits
Where [*pin name*] refers to the pins that are used to configure peripheral input mapping. See Table for input pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

REGISTER 12-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RPnR<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3-0 **RPnR<3:0>:** Peripheral Pin Select Output bits
See Table for output pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

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REGISTER 12-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER ('x' = A – G)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	EDGE DETECT	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **EDGEDETECT:** Edge Detection Type Control bit
1 = Detects any edge on the pin (CNFx is used for the CN event)
0 = Detects any edge on the pin (CNSTATx is used for the CN event)

bit 10-0 **Unimplemented:** Read as '0'

13.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The PIC32MZ DAK/DAL/DAR/DAS devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the low-power Secondary Oscillator (SOSC) for real-time clock applications.

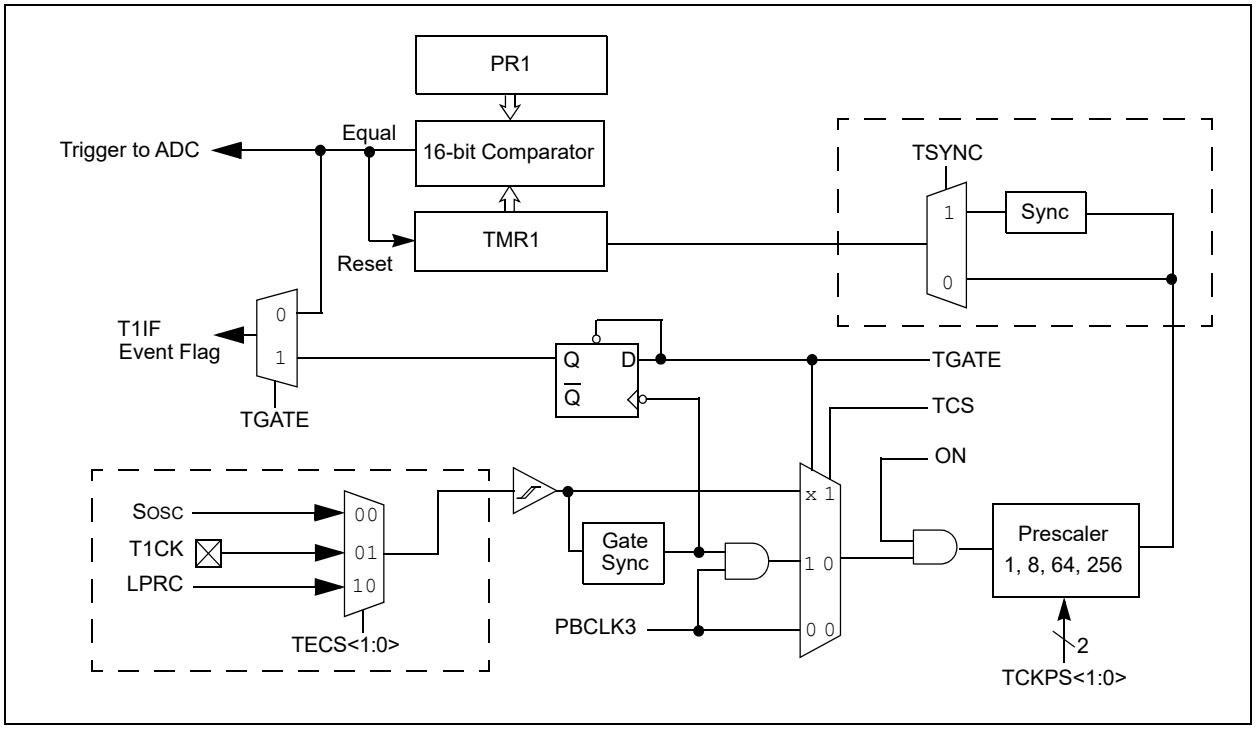
The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during Sleep mode and Idle mode
- Fast bit manipulation using CLR, SET, and INV registers
- Asynchronous mode can be used with the SOSC to function as a real-time clock
- ADC event trigger

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



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13.2 Timer1 Control Register

TABLE 13-1: TIMER1 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>		TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0010	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Timer On bit
1 = Timer is enabled
0 = Timer is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when device enters Idle mode
0 = Continue operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit
In Asynchronous Timer mode:
1 = Asynchronous write to TMR1 register in progress
0 = Asynchronous write to TMR1 register complete
In Synchronous Timer mode:
This bit is read as ‘0’.

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
11 = Reserved
10 = External clock comes from the LPRC
01 = External clock comes from the T1CK pin
00 = External clock comes from the SOSC

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as ‘0’

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REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit
When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit
1 = External clock is defined by the TECS<1:0> bits
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

14.0 TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

This family of devices features eight synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events.

The following modes are supported:

- Synchronous internal 16-bit timer
- Synchronous internal 16-bit gated timer
- Synchronous external 16-bit timer

Four 32-bit synchronous timers are available by combining Timer2 with Timer3, Timer4 with Timer5, Timer6 with Timer7, and Timer8 with Timer9.

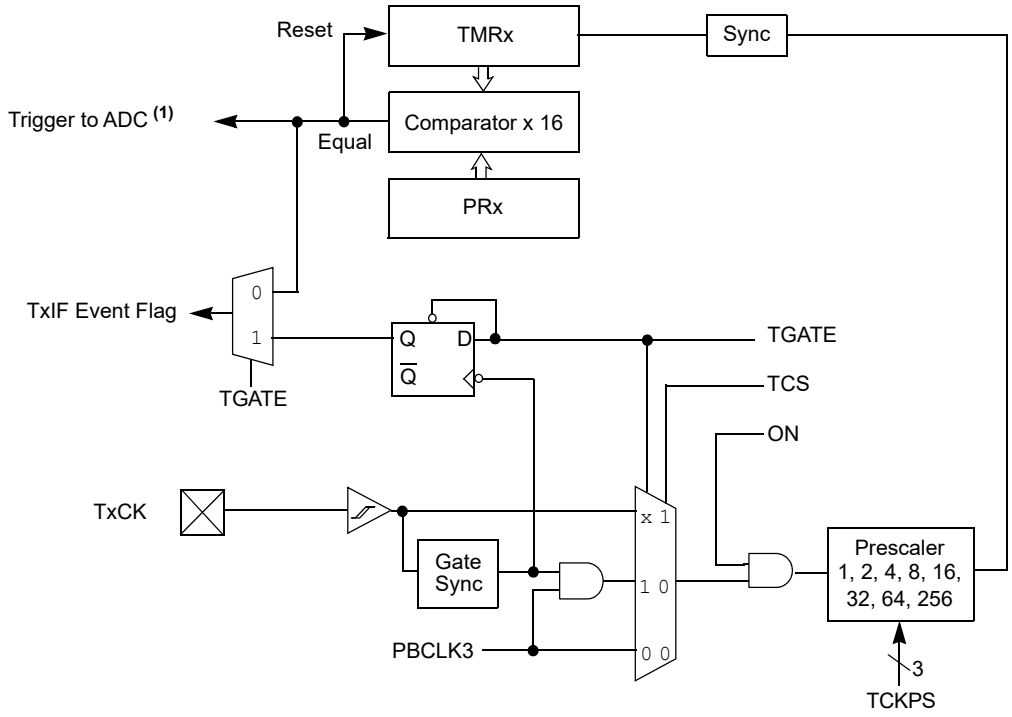
The 32-bit timers can operate in any one of following modes:

- Synchronous internal 32-bit timer
- Synchronous internal 32-bit gated timer
- Synchronous external 32-bit timer

14.1 Additional Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (Timer2 through Timer7 only)
- ADC event trigger (Timer3 and Timer5 only)
- Fast bit manipulation using CLR, SET and INV registers

FIGURE 14-1: TIMER2 THROUGH TIMER9 BLOCK DIAGRAM (16-BIT)



Note 1: The ADC event trigger is available on Timer3 and Timer5 only.

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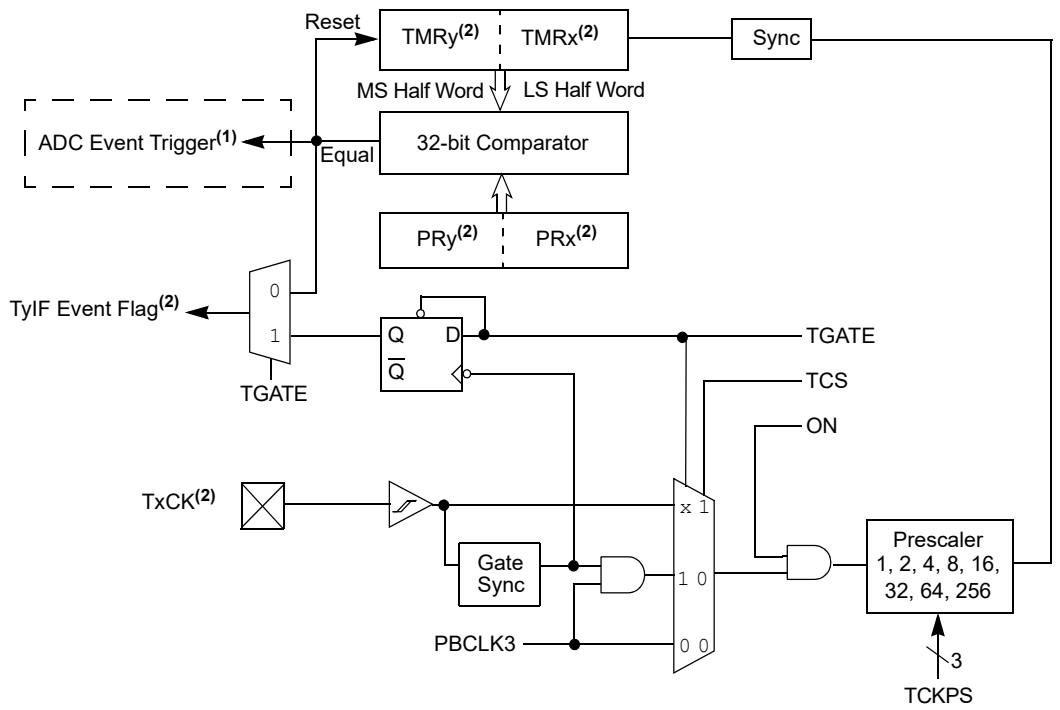
FIGURE 14-2: TIMER2/3, TIMER4/5, TIMER6/7, AND TIMER8/9 BLOCK DIAGRAM (32-BIT)



Note 1: ADC event trigger is available only on the Timer2/3 and TImer4/5 pairs.
2: In this diagram, ‘x’ represents Timer2, 4, 6, or 8, and ‘y’ represents Timer3, 5, 7, or 9.

14.2 Timer2-Timer9 Control Registers

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0210	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0220	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0400	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0410	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0420	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0600	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0610	TMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0620	PR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
0800	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
0810	TMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
0820	PR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF
0A00	T6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0A10	TMR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
0A20	PR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>																FFFF
0C00	T7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C10	TMR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
0C20	PR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>																FFFF
0E00	T8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0E10	TMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR4<15:0>																0000
0E20	PR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR4<15:0>																FFFF
1000	T9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
1010	TMR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR5<15:0>																0000
1020	PR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR5<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	SIDL(2)	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE(1)	TCKPS<2:0>(1)			T32(3)	—	TCS(1)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit(2)
1 = Discontinue operation when device enters Idle mode
0 = Continue operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored and is read as '0'.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits(1)
111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timer Mode Select bit(3)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers (Timer2, Timer4, Timer6, and Timer8).

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers.

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REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9) (CONTINUED)

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(1)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers (Timer2, Timer4, Timer6, and Timer8).

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers.

15.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following:

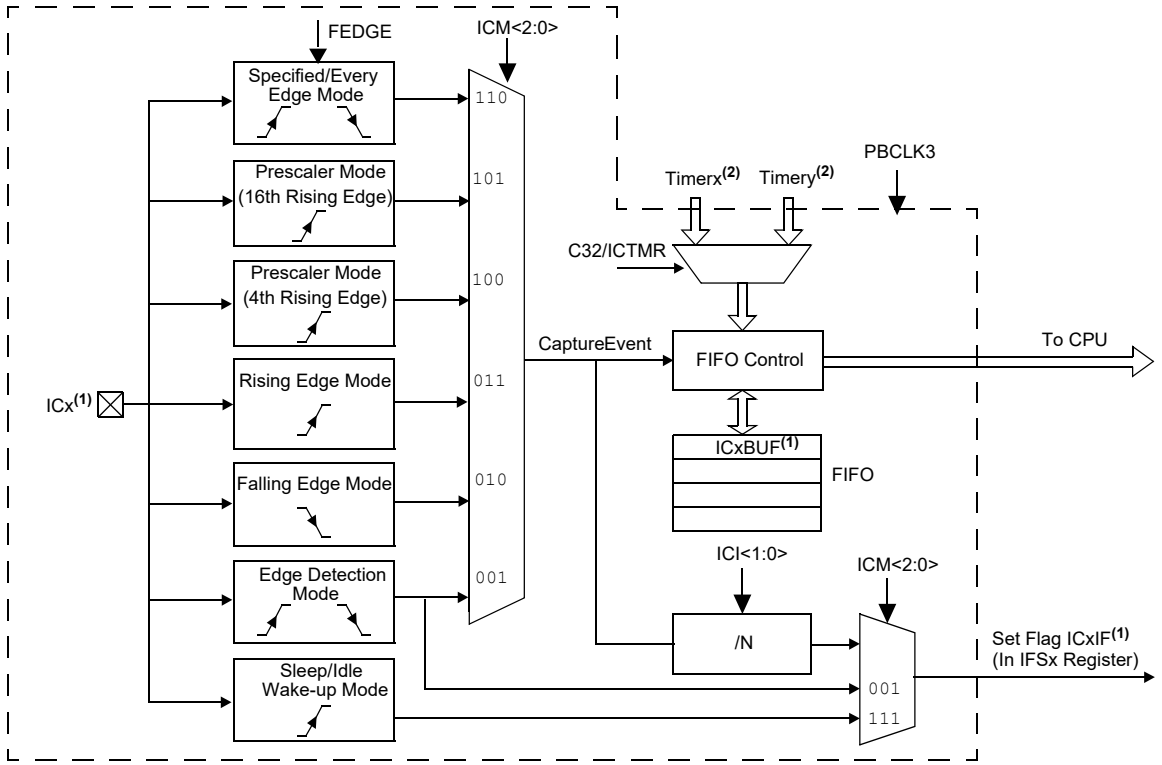
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of six 16-bit timers for the time base, or two of six 16-bit timers together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 15-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

2: See Table 15-1 for Timerx and Timery selections.

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The timer source for each Input Capture module depends on the setting of the ICACLK bit in the CFGCON register. The available configurations are shown in Table 15-1.

TABLE 15-1: TIMER SOURCE CONFIGURATIONS

Input Capture Module	Timerx	Timery
ICACLK (CFGCON<17>) = 0		
IC1 • • • IC9	Timer2 • • • Timer 2	Timer3 • • • Timer 3
ICACLK (CFGCON<17>) = 1		
IC1	Timer4	Timer5
IC2	Timer4	Timer5
IC3	Timer4	Timer5
IC4	Timer2	Timer3
IC5	Timer2	Timer3
IC6	Timer2	Timer3
IC7	Timer6	Timer7
IC8	Timer6	Timer7
IC9	Timer6	Timer7

15.1 Input Capture Control Registers

TABLE 15-2: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 9 REGISTER MAP

Virtual Address (BF84_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000	IC1CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																xxxx
		15:0																	xxxx
2200	IC2CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																xxxx
		15:0																	xxxx
2400	IC3CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																xxxx
		15:0																	xxxx
2600	IC4CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																xxxx
		15:0																	xxxx
2800	IC5CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																xxxx
		15:0																	xxxx
2A00	IC6CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2A10	IC6BUF	31:16	IC6BUF<31:0>																xxxx
		15:0																	xxxx
2C00	IC7CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2C10	IC7BUF	31:16	IC7BUF<31:0>																xxxx
		15:0																	xxxx
2E00	IC8CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2E10	IC8BUF	31:16	IC8BUF<31:0>																xxxx
		15:0																	xxxx
3000	IC9CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3010	IC9BUF	31:16	IC9BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 15-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Input Capture Module Enable bit
1 = Module enabled
0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Control bit
1 = Halt in CPU Idle mode
0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
1 = Capture rising edge first
0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
1 = 32-bit timer resource capture
0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is ‘1’)(1)
0 = Timery is the counter source for capture
1 = Timerx is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
1 = Input capture buffer is not empty; at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
101 = Prescaled Capture Event mode – every sixteenth rising edge
100 = Prescaled Capture Event mode – every fourth rising edge
011 = Simple Capture Event mode – every rising edge
010 = Simple Capture Event mode – every falling edge
001 = Edge Detect mode – every edge (rising and falling)
000 = Input Capture module is disabled

Note 1: Refer to Table 15-1 for Timerx and Timery selections.

16.0 OUTPUT COMPARE

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

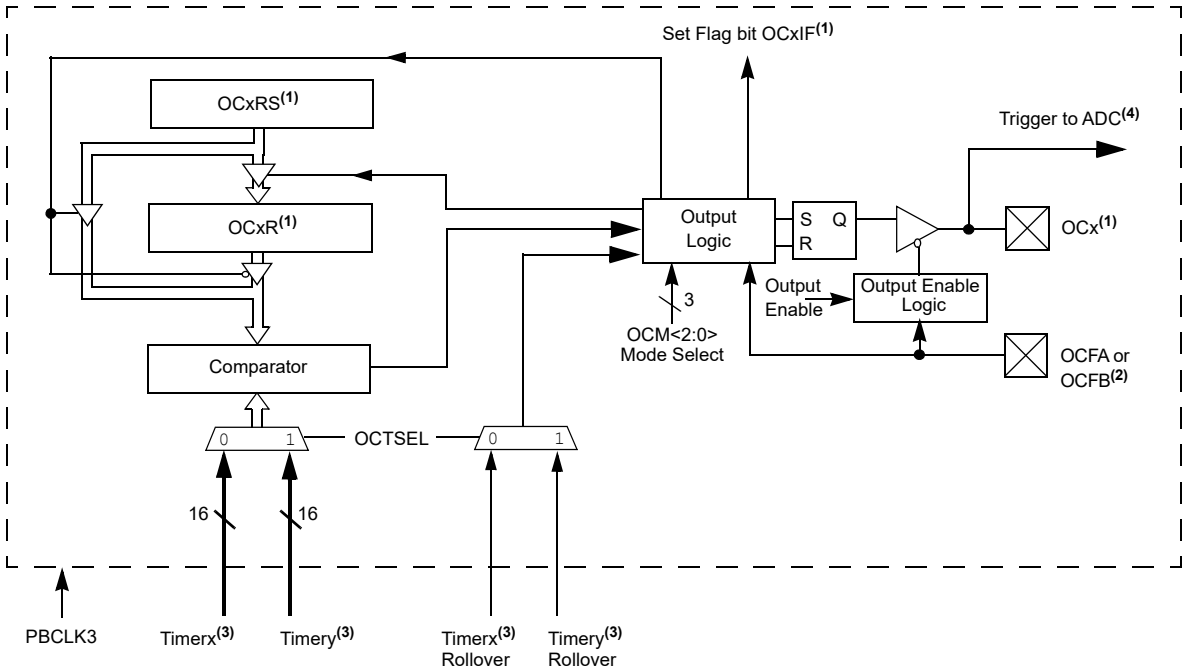
The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events.

For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are some of the key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base
- ADC event trigger

FIGURE 16-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 9.

2: The OCFA pin controls the OC1, OC3, and OC7-OC9 channels. The OCFB pin controls the OC4-OC6 channels.

3: Refer to Table 16-1 for Timerx and Timery selections.

4: The ADC event trigger is only available on OC1,OC3, and OC 5.

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The timer source for each Output Compare module depends on the setting of the OCACLK bit in the CFGCON register. The available configurations are shown in Table 16-1.

TABLE 16-1: TIMER SOURCE CONFIGURATIONS

Output Compare Module	Timerx	Timery
OCACLK (CFGCON<16>) = 0		
OC1 • • • OC9	Timer2 • • • Timer 2	Timer3 • • • Timer 3
OCACLK (CFGCON<16>) = 1		
OC1	Timer4	Timer5
OC2	Timer4	Timer5
OC3	Timer4	Timer5
OC4	Timer2	Timer3
OC5	Timer2	Timer3
OC6	Timer2	Timer3
OC7	Timer6	Timer7
OC8	Timer6	Timer7
OC9	Timer6	Timer7

16.1 Output Compare Control Registers

TABLE 16-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
4020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
4200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
4220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
4400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
4420	OC3RS	31:16	OC3RS<31:0>																xxxx
		15:0																	xxxx
4600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
4620	OC4RS	31:16	OC4RS<31:0>																xxxx
		15:0																	xxxx
4800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
4820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 16-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4A00	OC6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4A10	OC6R	31:16	OC6R<31:0>																xxxx
		15:0																	xxxx
4A20	OC6RS	31:16	OC6RS<31:0>																xxxx
		15:0																	xxxx
4C00	OC7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4C10	OC7R	31:16	OC7R<31:0>																xxxx
		15:0																	xxxx
4C20	OC7RS	31:16	OC7RS<31:0>																xxxx
		15:0																	xxxx
4E00	OC8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4E10	OC8R	31:16	OC8R<31:0>																xxxx
		15:0																	xxxx
4E20	OC8RS	31:16	OC8RS<31:0>																xxxx
		15:0																	xxxx
5000	OC9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5010	OC9R	31:16	OC9R<31:0>																xxxx
		15:0																	xxxx
5020	OC9RS	31:16 15:0	OC9RS<31:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 16-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT(1)	OCTSEL(2)	OCM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit
1 = Output Compare peripheral is enabled
0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters Idle mode
0 = Continue operation in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisions to the 32-bit timer source
0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(1)
1 = PWM Fault condition has occurred (cleared in HW only)
0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit(2)
1 = Timery is the clock source for this Output Compare module
0 = Timerx is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
111 = PWM mode on OCx; Fault pin enabled
110 = PWM mode on OCx; Fault pin disabled
101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
100 = Initialize OCx pin low; generate single output pulse on OCx pin
011 = Compare event toggles OCx pin
010 = Initialize OCx pin high; compare event forces OCx pin low
001 = Initialize OCx pin low; compare event forces OCx pin high
000 = Output compare peripheral is disabled but continues to draw current

Note 1: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.
2: Refer to Table 16-1 for Timerx and Timery selections.

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NOTES:

17.0 DEADMAN TIMER (DMT)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

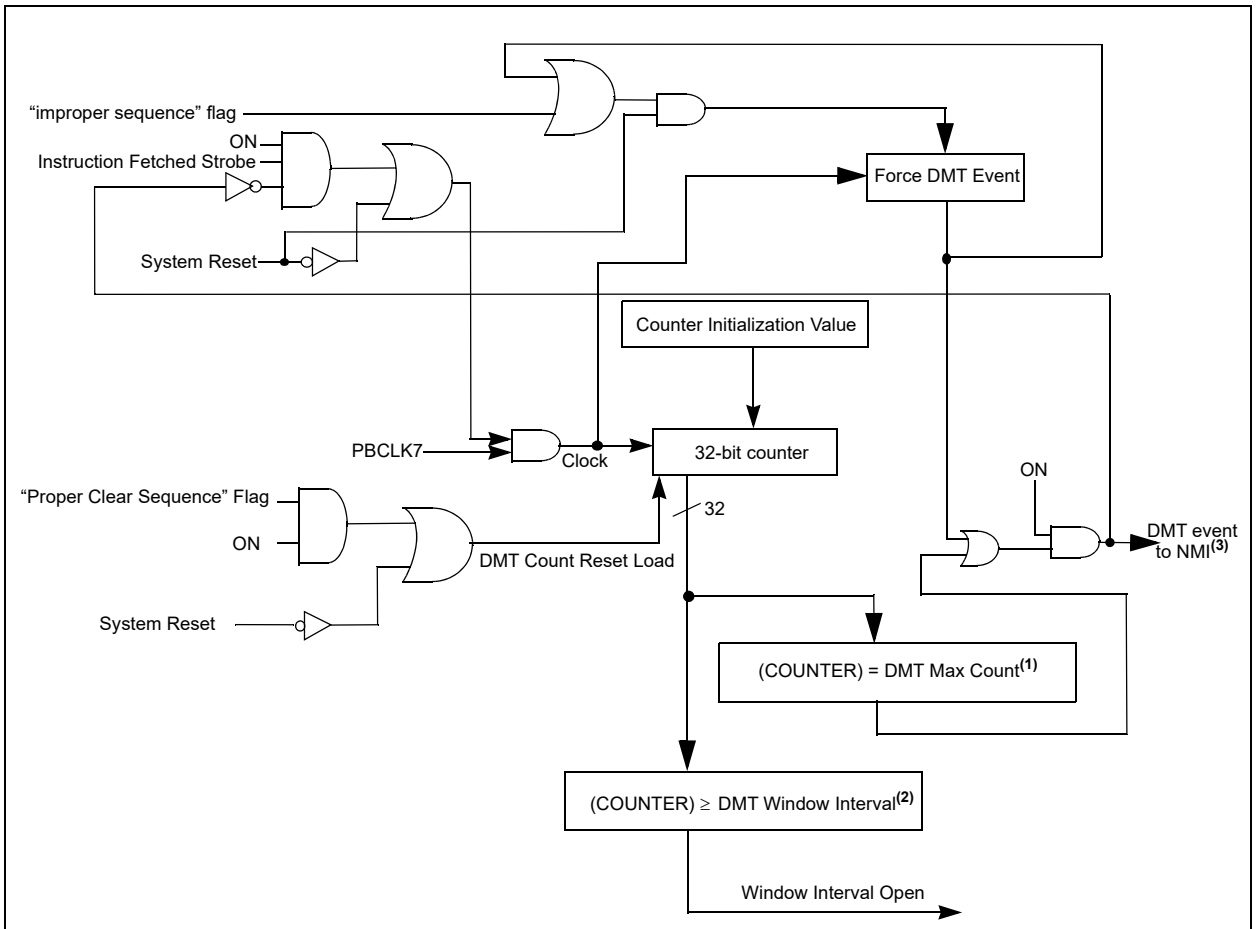
The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

The DMT consists of a 32-bit counter with a time-out count match value as specified by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.

A Deadman Timer is typically used in mission critical and safety critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 17-1 shows a block diagram of the Deadman Timer module.

FIGURE 17-1: DEADMAN TIMER BLOCK DIAGRAM



Note 1: DMT Max Count is controlled by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.
2: DMT Window Interval is controlled by the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.
3: Refer to **Section 6.0 "Resets"** for more information.

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17.1 Deadman Timer Control Registers

TABLE 17-1: DEADMAN TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0A00	DMTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0A10	DMTPRECLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STEP1<7:0>								—	—	—	—	—	—	—	—	0000
0A20	DMTCLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STEP2<7:0>								0000
0A30	DMTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
0A40	DMTCNT	31:16	COUNTER<31:0>																0000
		15:0																	0000
0A60	DMTPSCNT	31:16	PSCNT<31:0>																0000
		15:0																	0000
0A70	DMTPSINTV	31:16	PSINTV<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 17-1: DMTCON: DEADMAN TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Deadman Timer Module Enable bit(1)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is disabled

bit 13-0 **Unimplemented:** Read as '0'

Note 1: This bit only has control when FDMTEN (DEVCFG1<3>) = 0. Once set, the DMTCON.ON bit cannot be disabled by software.

REGISTER 17-2: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP1<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STEP1<7:0>:** Preclear Enable bits
01000000 = Enables the Deadman Timer Preclear (Step 1)
All other write patterns = Set BAD1 flag.
These bits are cleared when a DMT reset event occurs. STEP1<7:0> is also cleared if the STEP2<7:0> bits are loaded with the correct value in the correct sequence.

bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 17-3: DMTCLR: DEADMAN TIMER CLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP2<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STEP2<7:0>:** Clear Timer bits

00001000 = Clears STEP1<7:0>, STEP2<7:0> and the Deadman Timer if, and only if, preceded by correct loading of STEP1<7:0> bits in the correct sequence. The write to these bits may be verified by reading the DMTCNT bit and observing the counter being reset.

All other write patterns = Set BAD2 bit, the value of STEP1<7:0> will remain unchanged, and the new value being written STEP2<7:0> will be captured. These bits are also cleared when a DMT reset event occurs.

If the STEP2<7:0> bits are written without preceding with a correct loading of STEP1<7:0> bits, the BAD1 bit is set.

REGISTER 17-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HC	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R-0
	BAD1	BAD2	DMTEVENT					WINOPN

Legend:	HC = Cleared by Hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)		P = Programmable bit r = Reserved bit

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **BAD1:** Bad STEP1<7:0> Value Detect bit
1 = Incorrect STEP1<7:0> value or out of sequence write to STEP2<7:0> was detected
0 = Incorrect STEP1<7:0> value or out of sequence write to STEP2<7:0> was not detected

bit 6 **BAD2:** Bad STEP2<7:0> Value Detect bit
1 = Incorrect STEP2<7:0> value was detected
0 = Incorrect STEP2<7:0> value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit
1 = Deadman timer event was detected (counter expired or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)
0 = Deadman timer event was not detected

bit 4-1 **Unimplemented:** Read as ‘0’

bit 0 **WINOPN:** Deadman Timer Clear Window bit
1 = Deadman timer clear window is open
0 = Deadman timer clear window is not open

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REGISTER 17-5: DMTCNT: DEADMAN TIMER COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-8 **COUNTER<31:0>:** Read current contents of DMT counter

REGISTER 17-6: DMTPSCNT: POST STATUS CONFIGURE DMT COUNT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-8 **PSCNT<31:0>:** DMT Instruction Count Value Configuration Status bits
This is always the value of the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.

REGISTER 17-7: DMTPSINTV: POST STATUS CONFIGURE DMT INTERVAL STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)		P = Programmable bit	r = Reserved bit

bit 31-8 **PSINTV<31:0>:** DMT Window Interval Configuration Status bits
This is always the value of the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.

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NOTES:

18.0 WATCHDOG TIMER (WDT)

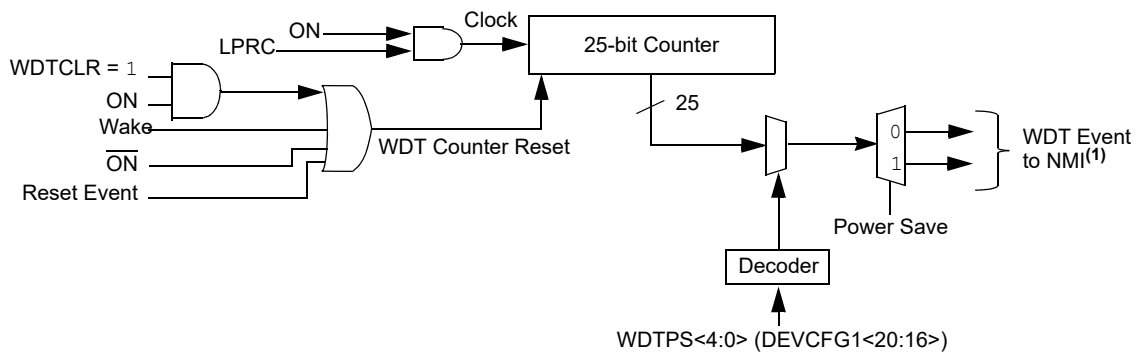
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

When enabled, the Watchdog Timer (WDT) operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle

FIGURE 18-1: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: Refer to **Section 6.0 "Resets"** for more information.

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18.1 Watchdog Timer Control Registers

TABLE 18-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0800	WDTCON(1)	31:16	WDTCLRKEY<15:0>																0000
		15:0	ON	—	—	RUNDIV<4:0>					—	—	SLPDIV<4:0>					WDTWINEN	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 18-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value 0x5743 to these bits using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The Watchdog Timer module is enabled
0 = The Watchdog Timer module is disabled

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RUNDIV<4:0>:** Watchdog Timer Postscaler Value in Run Mode bits
In Run mode, these bits are set to the values of the WDTPS<4:0> Configuration bits in DEVCFG1.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-1 **SLPDIV<4:0>:** Watchdog Timer Postscaler Value in Sleep Mode bits
In Sleep mode, these bits are set to the values of the SWDTPS <4:0> Configuration bits in DEVCFG4.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

Note 1: This bit only has control when FWDTEN (DEVCFG1<23>) = 0.

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NOTES:

19.0 DEEP SLEEP WATCHDOG TIMER (DSWDT)

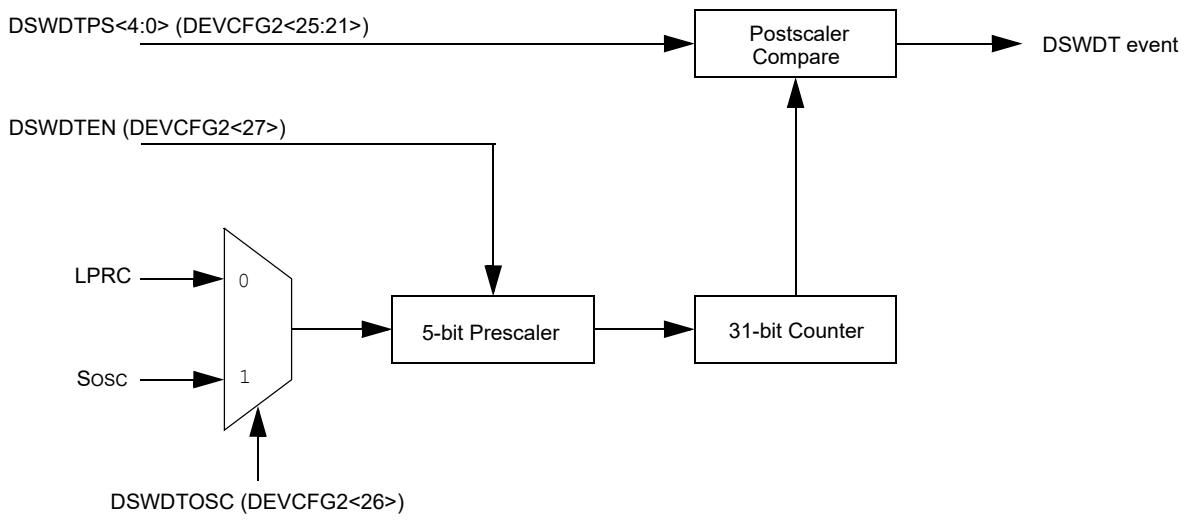
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Deep Sleep Watchdog Timer (DSWDT) is a dedicated Watchdog Timer for Deep Sleep mode operations of the device. The DSWDT is very useful in Battery-powered applications and in Low-Power modes of operations.

The primary function of the DSWDT is to automatically exit Deep Sleep mode after a prescribed amount of time has elapsed.

The DSWDT is controlled through the DEVCFG2 Configuration register at boot time (one-time programmable per POR). When enabled through the DSWDTEN bit in DEVCFG2, the DSWDT operates either from the internal Low-Power RC (LPRC) clock or from the Secondary Oscillator (SOSC). The clock selection for the DSWDT is done through the DSWDTOSC bit in the DEVCFG2 register.

FIGURE 19-1: DEEP SLEEP WATCHDOG TIMER BLOCK DIAGRAM



Example: When DSWDTOSC = `1`, DSWDTPS<4:0> bits = `00000`, and the SOSC is 32 kHz, the Watchdog delay is set to 1 ms.

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NOTES:

20.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

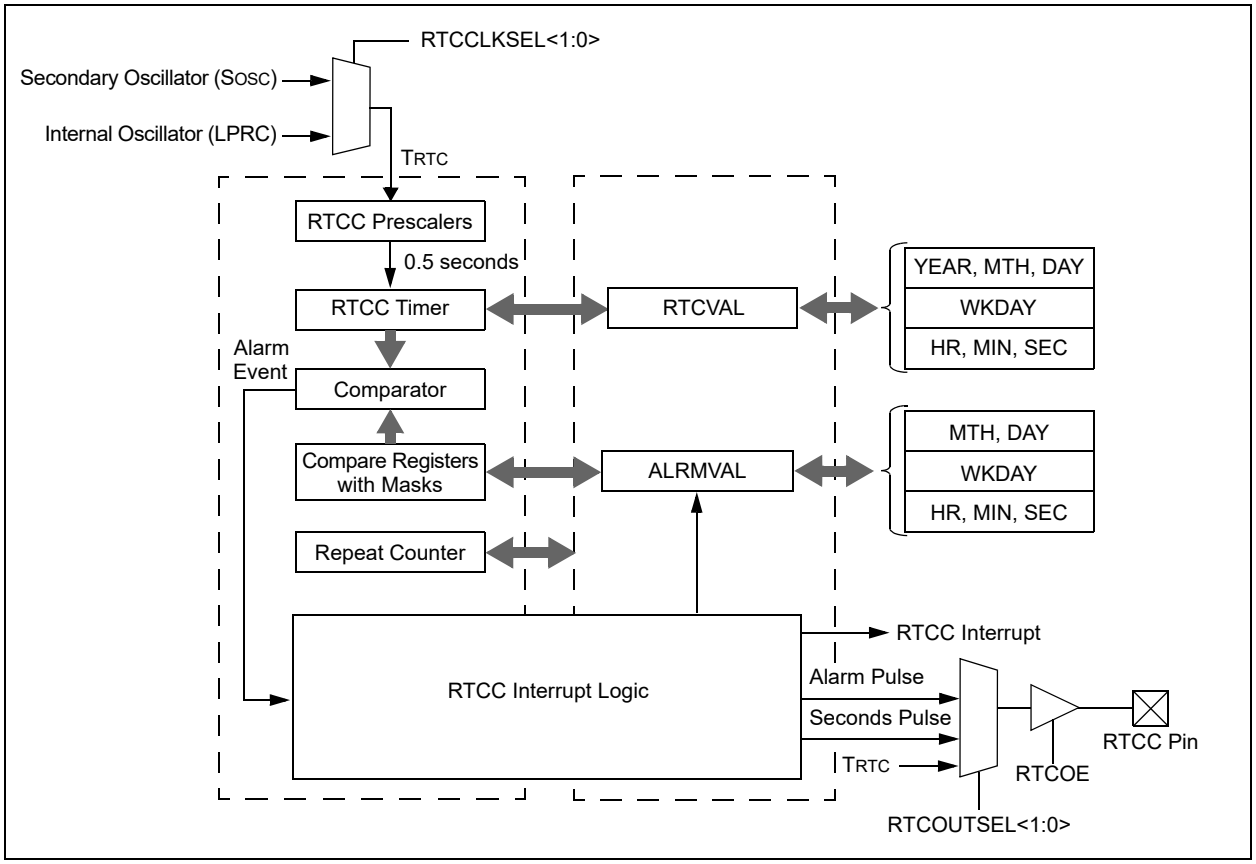
The RTCC module can operate in VBAT mode when there is a power loss on the VDDIO pin. The RTCC will continue to operate if the VBAT pin is powered on (it is usually connected to the battery).

The following are key features of the RTCC module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external crystal or internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

Note: The RTCC pin function is not available during VBAT operation.

FIGURE 20-1: RTCC BLOCK DIAGRAM



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20.1 RTCC Control Registers

TABLE 20-1: RTCC REGISTER MAP

Virtual Address (BF8C_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	RTCCLKSEL<1:0>		RTCOUTSEL<1:0>		RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0010	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0020	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0030	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx00
0040	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0050	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 20-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CAL<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAL<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	—	—	RTCCLKSEL<1:0>		RTC OUTSEL<1>(2)
7:0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0
	RTC OUTSEL<0>(2)	RTC CLKON	—	—	RTC WREN(3)	RTC SYNC	HALFSEC(4)	RTCOE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25-16 **CAL<9:0>:** Real-Time Clock Drift Calibration bits, which contain a signed 10-bit integer value

0111111111 = Maximum positive adjustment, adds 511 real-time clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 real-time clock pulse every one minute
0000000000 = No adjustment
1111111111 = Minimum negative adjustment, subtracts 1 real-time clock pulse every one minute
•
•
•
1000000000 = Minimum negative adjustment, subtracts 512 real-time clock pulses every one minute

bit 15 **ON:** RTCC On bit(1)

1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Disables RTCC operation when CPU enters Idle mode
0 = Continue normal operation when CPU enters Idle mode

bit 12-11 **Unimplemented:** Read as ‘0’

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to ‘0’ on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

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REGISTER 20-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

bit 10-9 **RTCCLKSEL<1:0>:** RTCC Clock Select bits

When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

11 = Reserved
10 = Reserved
01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)
00 = RTCC uses the internal 32 kHz oscillator (LPRC)

bit 8-7 **RTCOUTSEL<1:0>:** RTCC Output Data Select bits(2)

11 = Reserved
10 = RTCC Clock is presented on the RTCC pin
01 = Seconds Clock is presented on the RTCC pin
00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit

1 = RTCC Clock is actively running
0 = RTCC Clock is not running

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **RTCWREN:** Real-Time Clock Value Registers Write Enable bit(3)

1 = Real-Time Clock Value registers can be written to by the user
0 = Real-Time Clock Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** Real-Time Clock Value Registers Read Synchronization bit

1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = Real-time clock value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(4)

1 = Second half period of a second
0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit

1 = RTCC output is enabled
0 = RTCC output is not enabled

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

REGISTER 20-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN(1,2)	CHIME(2)	PIV(2)	ALRMSYNC	AMASK<3:0>(2)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ALRMEN:** Alarm Enable bit(1,2)

1 = Alarm is enabled
0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)

1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit

1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing.
0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is more than 32 real-time clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(2)

0000 = Every half-second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29, once every four years)
1010 = Reserved
1011 = Reserved
11xx = Reserved

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = ‘1’ (RTCCON<15>) and ALRMSYNC = 1.

Note: This register is reset only on a Power-on Reset (POR).

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REGISTER 20-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits[(2)]

`11111111` = Alarm will trigger 256 times

.

.

.

`00000000` = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = `1`.

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = `00` and CHIME = `0`.

2: This field should not be written when the RTCC ON bit = '`1`' (RTCCON<15>) and ALRMSYNC = `1`.

Note:	This register is reset only on a Power-on Reset (POR).

REGISTER 20-3: RTCTIME: REAL-TIME CLOCK TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **HR10<3:0>:** Binary-Coded Decimal Value of Hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary-Coded Decimal Value of Hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary-Coded Decimal Value of Minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary-Coded Decimal Value of Minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary-Coded Decimal Value of Seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary-Coded Decimal Value of Seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as ‘0’

Note: This register is writable only when the RTCWREN = 1 (RTCCON<3>).

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REGISTER 20-4: RTCDATE: REAL-TIME CLOCK DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<3:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **YEAR10<3:0>:** Binary-Coded Decimal Value of Years bits, 10 digits

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1 digit

bit 23-20 **MONTH10<3:0>:** Binary-Coded Decimal Value of Months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary-Coded Decimal Value of Days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary-Coded Decimal Value of Days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **WDAY01<3:0>:** Binary-Coded Decimal Value of Weekdays bits,1 digit; contains a value from 0 to 6

Note: This register is writable only when the RTCWREN = 1 (RTCCON<3>).

REGISTER 20-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **HR10<3:0>:** Binary Coded Decimal value of hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary Coded Decimal value of minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary Coded Decimal value of seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as ‘0’

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ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<1:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1 digit; contains a value from 0 to 6

21.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

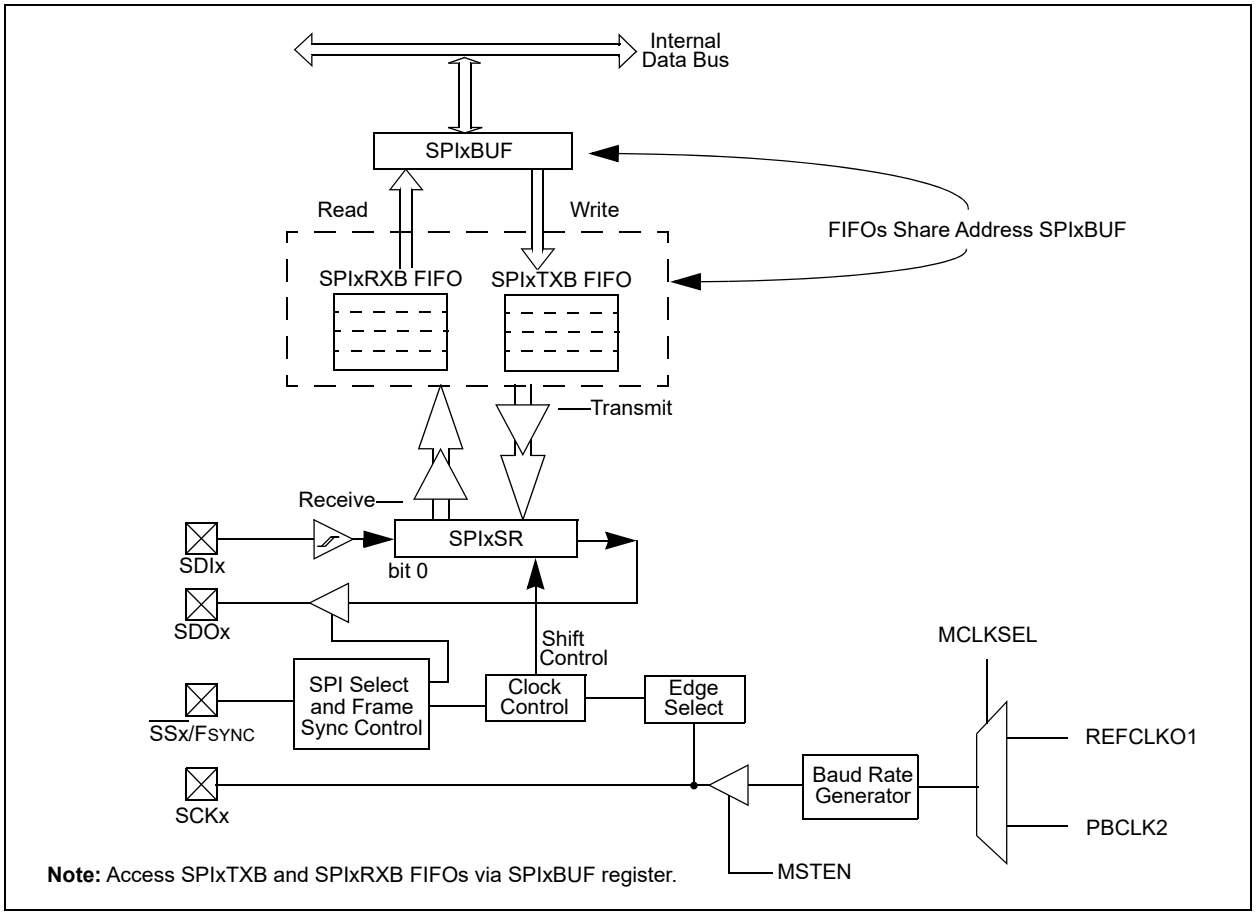
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), and so on.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Host and Client modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit:
  - FIFO buffers act as 4-level, 8-level, or 16-level deep FIFOs based on 8-bit, 16-bit, or 32-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep mode and Idle mode
- Audio Codec Support:
  - I^2S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 21-1: SPI/I^2S MODULE BLOCK DIAGRAM



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21.1 SPI Control Registers

TABLE 21-1: SPI1 THROUGH SPI6 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1000	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1010	SPI1STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	00A8
1020	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1030	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
1040	SPI1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00
1200	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1210	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
1220	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1230	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000
1240	SPI2CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000
1400	SPI3CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1410	SPI3STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
1420	SPI3BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1430	SPI3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000
1440	SPI3CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 21-1: SPI1 THROUGH SPI6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1600	SPI4CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1610	SPI4STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
1620	SPI4BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1630	SPI4BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000
1640	SPI4CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000
1800	SPI5CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1810	SPI5STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
1820	SPI5BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1830	SPI5BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000
1840	SPI5CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000
1A00	SPI6CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
1A10	SPI6STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
1A20	SPI6BUF	31:16	DATA<31:0>																0000
		15:0																	0000
1A30	SPI6BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	BRG<8:0>									0000
1A40	SPI6CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 21-1: SPIxCON: SPI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL(1)	—	—	—	—	—	SPIFE	ENHBUF(1)
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	DISSDO(4)	MODE32	MODE16	SMP	CKE(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP(3)	MSTEN	DISSDI(4)	STXISEL<1:0>		SRXISEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Client mode)
0 = Frame sync pulse output (Host mode)

bit 29 **FRMPOL:** Frame Sync / SPI Select Polarity bit (Framed SPI or Host Transmit modes only)
1 = Frame pulse or $\overline{SSx}$ pin is active-high
0 = Frame pulse or $\overline{SSx}$ is active-low

bit 28 **MSSEN:** Host Mode SPI Select Enable bit
1 = SPI select support enabled. The $\overline{SS}$ pin is automatically driven during transmission in Host mode. Polarity is determined by the FRMPOL bit.
0 = SPI select support is disabled.

bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
111 = Reserved
110 = Reserved
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character

bit 23 **MCLKSEL:** Host Clock Enable bit(1)
1 = REFCLKO1 is used by the Baud Rate Generator
0 = PBCLK2 is used by the Baud Rate Generator

bit 22-18 **Unimplemented:** Read as ‘0’

Note 1: This bit can only be written when the ON bit = 0. Refer to **Section 44.0 “Electrical Characteristics”** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to ‘0’ for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to ‘1’, regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 “Peripheral Pin Select (PPS)”** for more information).

REGISTER 21-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPI/I^2S Module On bit
1 = SPI/I^2S module is enabled
0 = SPI/I^2S module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **DISSDO:** Disable SDOx pin bit(4)
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
1	0	32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
0	1	16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
0	0	16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPI Data Input Sample Phase bit
Host mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Client mode (MSTEN = 0):
SMP value is ignored when SPI is used in Client mode. The module always uses SMP = 0.

bit 8 **CKE:** SPI Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)

bit 7 **SSEN:** SPI Select Enable (Client mode) bit
1 = $\overline{SSx}$ pin used for Client mode
0 = $\overline{SSx}$ pin not used for Client mode, pin controlled by port function.

bit 6 **CKP:** Clock Polarity Select bit(3)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

Note 1: This bit can only be written when the ON bit = 0. Refer to **Section 44.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 21-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

bit 5 **MSTEN:** Host Mode Enable bit
1 = Host mode
0 = Client mode

bit 4 **DISSDI:** Disable SDI bit(4)
1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
0 = SDI pin is controlled by the SPI module

bit 3-2 **STXISEL<1:0>:** SPI Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPI Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

Note 1: This bit can only be written when the ON bit = 0. Refer to **Section 44.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 21-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN(1)	—	—	—	AUDMONO(1,2)	—	AUDMOD<1:0>(1,2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit
1 = Data from RX FIFO is sign extended
0 = Data from RX FIFO is not sign extened

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
1 = Frame Error overflow generates error events
0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
1 = Receive overflow generates error events
0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
1 = Transmit Underrun Generates Error Events
0 = Transmit Underrun Does Not Generates Error Events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
1 = A ROV is not a critical error; during ROV data in the fifo is not overwritten by receive data
0 = A ROV is a critical error which stop SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
0 = A TUR is a critical error which stop SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit(1)
1 = Audio protocol enabled
0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as ‘0’

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
1 = Audio data is mono (Each data word is transmitted on both left and right channels)
0 = Audio data is stereo

bit 2 **Unimplemented:** Read as ‘0’

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit(1,2)
11 = PCM/DSP mode
10 = Right Justified mode
01 = Left Justified mode
00 = I^2S mode

Note 1: This bit can only be written when the ON bit = 0.
2: This bit is only valid for AUDEN = 1.

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REGISTER 21-3: SPIxSTAT: SPI STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **FRMERR:** SPI Frame Error status bit
1 = Frame error detected
0 = No Frame error detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as ‘0’

bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as ‘0’

REGISTER 21-3: SPIxSTAT: SPI STATUS REGISTER

bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit

1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty

Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.

Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit

1 = Transmit not yet started, SPITXB is full
0 = Transmit buffer is not full

Standard Buffer Mode:

Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.

Enhanced Buffer Mode:

Set when CWPTR + 1 = SRPTR; cleared otherwise

bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit

1 = Receive buffer, SPIxRXB is full
0 = Receive buffer, SPIxRXB is not full

Standard Buffer Mode:

Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer Mode:

Set when SWPTR + 1 = CRPTR; cleared otherwise

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NOTES:

22.0 SERIAL QUAD INTERFACE (SQI)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 46. "Serial Quad Interface (SQI)"** (DS60001244), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

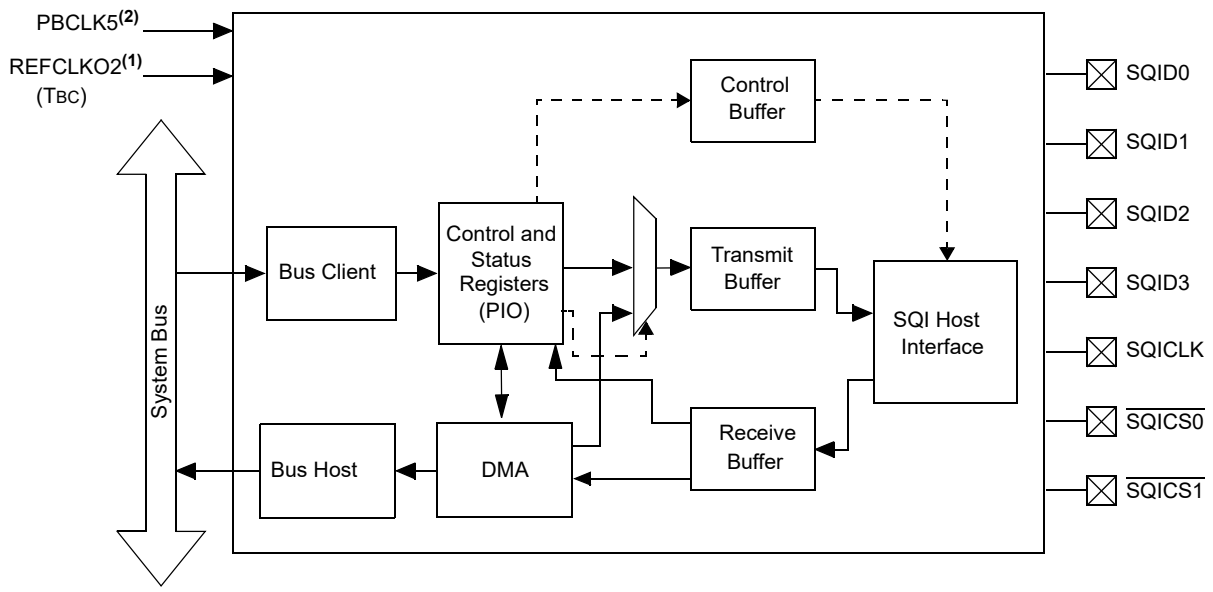
The SQI module is a synchronous serial interface that provides access to serial Flash memories and other serial devices. The SQI module supports Single Lane (identical to SPI), Dual Lane, and Quad Lane modes.

The following are some of the key features of the SQI module:

- Supports Single, Dual, and Quad Lane modes
- Supports Single Data Rate (SDR) and Double Data Rate (DDR) modes
- Programmable command sequence
- eXecute-In-Place (XIP)
- Data transfer:
  - Programmed I/O mode (PIO)
  - Buffer descriptor DMA
- Supports SPI Mode 0 and Mode 3
- Programmable Clock Polarity (CPOL) and Clock Phase (CPHA) bits
- Supports up to two Chip Selects
- Supports up to four bytes of Flash address
- Programmable interrupt thresholds
- 32-byte transmit data buffer
- 32-byte receive data buffer
- 4-word controller buffer

Note: Once the SQI module is configured, external devices are memory mapped into KSEG2 (see Figure 4-1 through Figure 4-2 in **Section 4.0 "Memory Organization"** for more information). The MMU must be enabled and the TLB must be set up to access this memory (see **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"* for more information).

FIGURE 22-1: SQI MODULE BLOCK DIAGRAM



Note 1: When configuring the REFCLKO2 clock source, a value of '0' for the ROTRIM<8:0> bits must be selected. REFCLKO2 must be turned on before SQI Special Function Registers (SFR) access.

2: This clock source is only used for SQI Special Function Register (SFR) access.

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22.1 SQI Control Registers

TABLE 22-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000	SQI1 XCON1	31:16	—	—	SDRCMD	DDRDATA	DDR DUMMY	DDR MODE	DDR ADDR	DDRCMD	DUMMYBYTES<2:0>			ADDRBYTES<2:0>			READOPCODE<7:6>		0000
		15:0	READOPCODE<5:0>						TYPEDATA<1:0>		TYPEDUMMY<1:0>		TYPEMODE<1:0>		TYPEADDR<1:0>		TYPECMD<1:0>		0000
2004	SQI1 XCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DEVSEL<1:0>		MODEBYTES<1:0>		MODECODE<7:0>								0000
2008	SQI1CFG	31:16	—	—	—	—	—	—	CSEN<1:0>		SQIEN	—	DATAEN<1:0>		CON BUFRST	RXBUFST	TXBUFST	RESET	0000
		15:0	—	—	—	BURSTEN	—	HOLD	WP	—	—	—	LSBF	CPOL	CPHA	MODE<2:0>			0000
200C	SQI1CON	31:16	—	—	—	—	—	—	—	SCHECK	DDRMODE	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>		0000
		15:0	TXRXCOUNT<15:0>																0000
2010	SQI1 CLKCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKDIV<10:8>			0000
		15:0	CLKDIV<7:0>								—	—	—	—	—	—	STABLE	EN	0000
2014	SQI1 CMDTHR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TXCMDTHR<5:0>						—	—	RXCMDTHR<5:0>						0000
2018	SQI1 INTTHR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TXINTTHR<5:0>						—	—	RXINTTHR<5:0>						0000
201C	SQI1 INTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEIE	PKT COMPIE	BD DONEIE	CON THRIE	CON EMPTYIE	CON FULLIE	RX THRIE	RX FULLIE	RX EMPTYIE	TX THRIE	TX FULLIE	TX EMPTYIE	0000
2020	SQI1 INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEIF	PKT COMPIF	BD DONEIF	CON THRIF	CON EMPTYIF	CON FULLIF	RX THRIF	RX FULLIF	RX EMPTYIF	TX THRIF	TX FULLIF	TX EMPTYIF	0000
2024	SQI1 TXDATA	31:16	TXDATA<31:16>																0000
		15:0	TXDATA<15:0>																0000
2028	SQI1 RXDATA	31:16	RXDATA<31:16>																0000
		15:0	RXDATA<15:0>																0000
202C	SQI1 STAT1	31:16	—	—	—	—	—	—	—	—	—	—	TXBUFFREE<5:0>						0000
		15:0	—	—	—	—	—	—	—	—	—	—	RXBUFCNT<5:0>						0000
2030	SQI1 STAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMDSTAT<1:0>		0000
		15:0	—	—	—	—	—	CONAVAIL<3:0>				SDID3	SDID2	SDID1	SDID0	—	RXUN	TXOV	00x0
2034	SQI1 BDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	START	POLLEN	DMAEN	0000
2038	SQI1BD CURADD	31:16	BDCURRADDR<31:16>																0000
		15:0	BDCURRADDR<15:0>																0000
2040	SQI1BD BASEADD	31:16	BDADDR<31:16>																0000
		15:0	BDADDR<15:0>																0000

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TABLE 22-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2044	SQI1BD STAT	31:16	—	—	—	—	—	—	—	—	—	—	BDSTATE<3:0>				DMA START	DMAACTV	0000
		15:0	BDCON<15:0>																0000
2048	SQI1BD POLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	POLLCON<15:0>																0000
204C	SQI1BD TXDSTAT	31:16	—	—	—	TXSTATE<3:0>				—	—	—	TXBUFCNT<5:0>						0000
		15:0	—	—	—	—	—	—	—	TXCURBUFLEN<8:0>									0000
2050	SQI1BD RXDSTAT	31:16	—	—	—	RXSTATE<3:0>				—	—	—	RXBUFCNT<5:0>						0000
		15:0	—	—	—	—	—	—	—	RXCURBUFLEN<8:0>									0000
2054	SQI1THR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	THRES<3:0>				0000
2058	SQI1INT SIGEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEISE	PKT DONEISE	BD DONEISE	CON THRISE	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE	0000
205C	SQI1 TAPCON	31:16	—	—	DDRCLKINDLY<5:0>						SDRDATINDLY<3:0>				DDRDATINDLY<3:0>				0000
		15:0	—	—	SDRCLKINDLY<5:0>						DATAOUTDLY<3:0>				CLKOUTDLY<3:0>				0000
2060	SQI1 MEMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	STATPOS	TYPESTAT<1:0>		STATBYTES<1:0>		0000
		15:0	STATCMD<15:0>																0000
2064	SQI1 XCON3	31:16	—	—	—	INIT1 SCHECK	INIT1COUNT<1:0>		INIT1TYPE<1:0>		INIT1CMD3<7:0>								0000
		15:0	INIT1CMD2<7:0>								INIT1CMD1<7:0>								0000
2068	SQI1 XCON4	31:16	—	—	—	INIT2 SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>		INIT2CMD3<7:0>								0000
		15:0	INIT2CMD2<7:0>								INIT2CMD1<7:0>								0000

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REGISTER 22-1: SQI1XCON1: SQI XIP CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	SDRCMD	DDRDATA	DDRDUMMY	DDRMODE	DDRADDR	DDRCMD(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DUMMYBYTES<2:0>			ADDRBYTES<2:0>			READOPCODE<7:6>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	READOPCODE<5:0>						TYPEDATA<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TYPEDUMMY<1:0>		TYPEMODE<1:0>		TYPEADDR<1:0>		TYPECMD<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as ‘0’

bit 29 **SDRCMD:** SQI Command in SDR Mode bit
1 = SQI command is in SDR mode and SQI data is in DDR mode
0 = SQI command is in DDR mode and SQI data is in DDR mode

bit 28 **DDRDATA:** SQI Data DDR Mode bit
1 = SQI data bytes are transferred in DDR mode
0 = SQI data bytes are transferred in SDR mode

bit 27 **DDRDUMMY:** SQI Dummy DDR Mode bit
1 = SQI dummy bytes are transferred in DDR mode
0 = SQI dummy bytes are transferred in SDR mode

bit 26 **DDRMODE:** SQI DDR Mode bit
1 = SQI mode bytes are transferred in DDR mode
0 = SQI mode bytes are transferred in SDR mode

bit 25 **DDRADDR:** SQI Address Mode bit
1 = SQI address bytes are transferred in DDR mode
0 = SQI address bytes are transferred in SDR mode

bit 24 **DDRCMD:** SQI DDR Command Mode bit(1)
1 = SQI command bytes are transferred in DDR mode
0 = SQI command bytes are transferred in SDR mode

bit 23-21 **DUMMYBYTES<2:0>:** Transmit Dummy Bytes bits
111 = Transmit seven dummy bytes after the address bytes
.
.
.
011 = Transmit three dummy bytes after the address bytes
010 = Transmit two dummy bytes after the address bytes
001 = Transmit one dummy bytes after the address bytes
000 = Transmit zero dummy bytes after the address bytes

Note 1: When DDRCMD is set to ‘0’, the SQI module will ignore the value in the SDRCMD bit.

REGISTER 22-1: SQI1XCON1: SQI XIP CONTROL REGISTER 1 (CONTINUED)

bit 20-18 **ADDRBYTES<2:0>:** Address Cycle bits

111 = Reserved
•
•
•
101 = Reserved
100 = Four address bytes
011 = Three address bytes
010 = Two address bytes
001 = One address bytes
000 = Zero address bytes

bit 17-10 **READOPCODE<7:0>:** Op code Value for Read Operation bits

These bits contain the 8-bit op code value for read operation.

bit 9-8 **TYPEDATA<1:0>:** SQI Type Data Enable bits

The boot controller will receive the data in Single Lane, Dual Lane, or Quad Lane.
11 = Reserved
10 = Quad Lane mode data is enabled
01 = Dual Lane mode data is enabled
00 = Single Lane mode data is enabled

bit 7-6 **TYPEDUMMY<1:0>:** SQI Type Dummy Enable bits

The boot controller will send the dummy in Single Lane, Dual Lane, or Quad Lane.
11 = Reserved
10 = Quad Lane mode dummy is enabled
01 = Dual Lane mode dummy is enabled
00 = Single Lane mode dummy is enabled

bit 5-4 **TYPEMODE<1:0>:** SQI Type Mode Enable bits

The boot controller will send the mode in Single Lane, Dual Lane, or Quad Lane.
11 = Reserved
10 = Quad Lane mode is enabled
01 = Dual Lane mode is enabled
00 = Single Lane mode is enabled

bit 3-2 **TYPEADDR<1:0>:** SQI Type Address Enable bits

The boot controller will send the address in Single Lane, Dual Lane, or Quad Lane.
11 = Reserved
10 = Quad Lane mode address is enabled
01 = Dual Lane mode address is enabled
00 = Single Lane mode address is enabled

bit 1-0 **TYPECMD<1:0>:** SQI Type Command Enable bits

The boot controller will send the command in Single Lane, Dual Lane, or Quad Lane.
11 = Reserved
10 = Quad Lane mode command is enabled
01 = Dual Lane mode command is enabled
00 = Single Lane mode command is enabled

Note 1: When DDRCMD is set to '0', the SQI module will ignore the value in the SDRCMD bit.

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REGISTER 22-2: SQI1XCON2: SQI XIP CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DEVSEL<1:0>		MODEBYTES<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MODECODE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11-10 **DEVSEL<1:0>:** Device Select bits
- 11 = Reserved
- 10 = Reserved
- 01 = Device 1 is selected
- 00 = Device 0 is selected

bit 9-8 **MODEBYTES<1:0>:** Mode Byte Cycle Enable bits
- 11 = Three cycles
- 10 = Two cycles
- 01 = One cycle
- 00 = Zero cycles

bit 7-0 **MODECODE<7:0>:** Mode Code Value bits
These bits contain the 8-bit code value for the mode bits.

REGISTER 22-3: SQI1CFG: SQI CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CSEN<1:0>	
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	SQIEN	—	DATAEN<1:0>		CON BUFRST	RX BUFRST	TX BUFRST	RESET
15:8	U-0	r-0	r-0	R/W-0	r-0	R/W-0	R/W-0	U-0
	—	—	—	BURSTEN(1)	—	HOLD	WP	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	LSBF	CPOL	CPHA	MODE<2:0>		

Legend:	HC = Hardware Cleared	r = Reserved	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25-24 **CSEN<1:0>:** Chip Select Output Enable bits
11 = Chip Select 0 and Chip Select 1 are used
10 = Chip Select 1 is used (Chip Select 0 is not used)
01 = Chip Select 0 is used (Chip Select 1 is not used)
00 = Chip Select 0 and Chip Select 1 are not used

bit 23 **SQIEN:** SQI Enable bit
1 = SQI module is enabled
0 = SQI module is disabled

bit 22 **Unimplemented:** Read as ‘0’

bit 21-20 **DATAEN<1:0>:** Data Output Enable bits
11 = Reserved
10 = SQID3-SQID0 outputs are enabled
01 = SQID1 and SQID0 data outputs are enabled
00 = SQID0 data output is enabled

bit 19 **CONBUFRST:** Control Buffer Reset bit
1 = A reset pulse is generated clearing the control buffer
0 = A reset pulse is not generated

bit 18 **RXBUFRST:** Receive Buffer Reset bit
1 = A reset pulse is generated clearing the receive buffer
0 = A reset pulse is not generated

bit 17 **TXBUFRST:** Transmit Buffer Reset bit
1 = A reset pulse is generated clearing the transmit buffer
0 = A reset pulse is not generated

bit 16 **RESET:** Software Reset Select bit
This bit is automatically cleared by the SQI module. All of the internal state machines and buffer pointers are reset by this reset pulse.
1 = A reset pulse is generated
0 = A reset pulse is not generated

bit 15 **Unimplemented:** Read as ‘0’

bit 14-13 **Reserved:** Must be programmed as ‘0’

Note 1: This bit must be programmed as ‘1’.

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REGISTER 22-3: SQI1CFG: SQI CONFIGURATION REGISTER (CONTINUED)

bit 12 **BURSTEN:** Burst Configuration bit[(1)]

1 = Burst is enabled
0 = Burst is not enabled

bit 11 **Reserved:** Must be programmed as '0'

bit 10 **HOLD:** Hold bit

In Single Lane or Dual Lane mode, this bit is used to drive the SQID3 pin, which can be used for devices with a HOLD input pin. The meaning of the values for this bit will depend on the device to which SQID3 is connected.

bit 9 **WP:** Write Protect bit

In Single Lane or Dual Lane mode, this bit is used to drive the SQID2 pin, which can be used with devices with a write-protect pin. The meaning of the values for this bit will depend on the device to which SQID2 is connected.

bit 8-6 **Unimplemented:** Read as '0'

bit 5 **LSBF:** Data Format Select bit

1 = LSB is sent or received first
0 = MSB is sent or received first

bit 4 **CPOL:** Clock Polarity Select bit

1 = Active-low SQICLK (SQICLK high is the Idle state)
0 = Active-high SQICLK (SQICLK low is the Idle state)

bit 3 **CPHA:** Clock Phase Select bit

1 = SQICLK starts toggling at the start of the first data bit
0 = SQICLK starts toggling at the middle of the first data bit

bit 2-0 **MODE<2:0>:** Mode Select bits

111 = Reserved
•
•
•
100 = Reserved
011 = XIP mode is selected (when this mode is entered, the module behaves as if executing in place (XIP), but uses the register data to control timing)
010 = DMA mode is selected
001 = CPU mode is selected (the module is controlled by the CPU in PIO mode. This mode is entered when leaving Boot or XIP mode)
000 = Reserved

Note 1: This bit must be programmed as '1'.

REGISTER 22-4: SQI1CON: SQI CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	r-0	R/W-0
	—	—	—	—	—	—	—	SCHECK(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DDRMODE	DASSERT	DEVSEL<1:0>		LANEMODE<1:0>		CMDINIT<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXRXCOUNT<7:0>							

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **Reserved:** Must be programmed as ‘0’

bit 24 **SCHECK:** Flash Status Check bit(1)
1 = Check the status of the Flash
0 = Do not check the status of the Flash

bit 23 **DDRMODE:** Double Data Rate Mode bit
1 = Set the SQI transfers to DDR mode
0 = Set the SQI transfers to SDR mode

bit 22 **DASSERT:** Chip Select Assert bit
1 = Chip Select is deasserted after transmission or reception of the specified number of bytes
0 = Chip Select is not deasserted after transmission or reception of the specified number of bytes

bit 21-20 **DEVSEL<1:0>:** SQI Device Select bits
11 = Reserved
10 = Reserved
01 = Select Device 1
00 = Select Device 0

bit 19-18 **LANEMODE<1:0>:** SQI Lane Mode Select bits
11 = Reserved
10 = Quad Lane mode
01 = Dual Lane mode
00 = Single Lane mode

bit 17-16 **CMDINIT<1:0>:** Command Initiation Mode Select bits
If it is Transmit, commands are initiated based on a write to the transmit register or the contents of TX buffer. If CMDINIT is Receive, commands are initiated based on reads to the read register or RX buffer availability.
11 = Reserved
10 = Receive
01 = Transmit
00 = Idle

bit 15-0 **TXRXCOUNT<15:0>:** Transmit/Receive Count bits
These bits specify the total number of bytes to transmit or received (based on CMDINIT).

Note 1: When this bit is set to ‘1’, the SQI module uses the SQI1MEMSTAT register to control the status check command process.

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REGISTER 22-5: SQI1CLKCON: SQI CLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CLKDIV<10:8>(1)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CLKDIV<7:0>(1)							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R/W-0
	—	—	—	—	—	—	STABLE	EN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-19 **Unimplemented:** Read as ‘0’

bit 18-8 **CLKDIV<10:0>:** SQI Clock TSQI Frequency Select bit(1)

10000000000 = Base clock TBC is divided by 2048
01000000000 = Base clock TBC is divided by 1024
00100000000 = Base clock TBC is divided by 512
00010000000 = Base clock TBC is divided by 256
00001000000 = Base clock TBC is divided by 128
00000100000 = Base clock TBC is divided by 64
00000010000 = Base clock TBC is divided by 32
00000001000 = Base clock TBC is divided by 16
00000000100 = Base clock TBC is divided by 8
00000000010 = Base clock TBC is divided by 4
00000000001 = Base clock TBC is divided by 2
00000000000 = Base clock TBC

Setting these bits to ‘00000000’ specifies the highest frequency of the SQI clock.

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **STABLE:** TSQI Clock Stable Select bit

This bit is set to ‘1’ when the SQI clock, TSQI, is stable after writing a ‘1’ to the EN bit.
1 = TSQI clock is stable
0 = TSQI clock is not stable

bit 0 **EN:** TSQI Clock Enable Select bit

When clock oscillation is stable, the SQI module will set the STABLE bit to ‘1’.
1 = Enable the SQI clock (TSQI) (when clock oscillation is stable, the SQI module sets the STABLE bit to ‘1’)
0 = Disable the SQI clock (TSQI) (the SQI module should stop its clock to enter a low power state); SFRs can still be accessed, as they use PBCLK5

Note 1: Refer to Table 44-40 in **44.0 “Electrical Characteristics”** for the maximum clock frequency specifications.

REGISTER 22-6: SQI1CMDTHR: SQI COMMAND THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TXCMDTHR<5:0>					
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	RXCMDTHR<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as ‘0’

bit 13-8 **TXCMDTHR<5:0>:** Transmit Command Threshold bits

In transmit initiation mode, the SQI module performs a transmit operation when transmit command threshold bytes are present in the TX buffer. These bits should usually be set to ‘1’ for normal Flash commands, and set to a higher value for page programming. For 16-bit mode, the value should be a multiple of 2.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RXCMDTHR<5:0>:** Receive Command Threshold bits(1)

In receive initiation mode, the SQI module attempts to perform receive operations to fetch the receive command threshold number of bytes in the receive buffer. If space for these bytes is not present in the buffer, the SQI will not initiate a transfer. For 16-bit mode, the value should be a multiple of 2.

If software performs any reads, thereby reducing the buffer count, hardware would initiate a receive transfer to make the buffer count equal to the value in these bits. If software would not like any more words latched into the buffer, command initiation mode needs to be changed to Idle before any buffer reads by software.

In the case of Boot/XIP mode, the SQI module will use the System Bus burst size, instead of the receive command threshold value.

Note 1: These bits should only be programmed when a receive is not active (i.e., during Idle mode or a transmit).

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REGISTER 22-7: SQI1INTTHR: SQI INTERRUPT THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TXINTTHR<5:0>					
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	RXINTTHR<5:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as ‘0’

bit 13-8 **TXINTTHR<5:0>:** Transmit Interrupt Threshold bits

A transmit interrupt is set when the transmit buffer has more space than the set number of bytes. For 16-bit mode, the value should be a multiple of 2.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RXINTTHR<5:0>:** Receive Interrupt Threshold bits

A receive interrupt is set when the receive buffer count is larger than or equal to the set number of bytes. For 16-bit mode, the value should be multiple of 2.

REGISTER 22-8: SQI1INTEN: SQI INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DMAEIE	PKTCOMPIE	BDDONEIE	CONTHRIE
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CONEMPTYIE	CONFULLIE	RXTHRIE	RXFULLIE	RXEMPTYIE	TXTHRIE	TXFULLIE	TXEMPTYIE

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11 **DMAEIE:** DMA Bus Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 10 **PKTCOMPIE:** DMA Buffer Descriptor Packet Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **BDDONEIE:** DMA Buffer Descriptor Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 8 **CONTHRIE:** Control Buffer Threshold Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **CONEMPTYIE:** Control Buffer Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **CONFULLIE:** Control Buffer Full Interrupt Enable bit
This bit enables an interrupt when the receive buffer is full.
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **RXTHRIE:** Receive Buffer Threshold Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **RXFULLIE:** Receive Buffer Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **RXEMPTYIE:** Receive Buffer Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **TXTHRIE:** Transmit Threshold Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **TXFULLIE:** Transmit Buffer Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **TXEMPTYIE:** Transmit Buffer Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

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REGISTER 22-9: SQI1INTSTAT: SQI INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
	—	—	—	—	DMA EIF	PKT COMPIF	BD DONEIF	CON THRIF
7:0	R/W-1, HS	R/W-0, HS	R/W-1, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS	R/W-0, HS	R/W-1, HS
	CON EMPTYIF	CON FULLIF	RXTHRIF(1)	RXFULLIF	RX EMPTYIF	TXTHRIF	TXFULLIF	TX EMPTYIF

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11 **DMAEIF:** DMA Bus Error Interrupt Flag bit
1 = DMA bus error has occurred
0 = DMA bus error has not occurred

bit 10 **PKTCOMPIF:** DMA Buffer Descriptor Processor Packet Completion Interrupt Flag bit
1 = DMA BD packet is complete
0 = DMA BD packet is in progress

bit 9 **BDDONEIF:** DMA Buffer Descriptor Done Interrupt Flag bit
1 = DMA BD process is done
0 = DMA BD process is in progress

bit 8 **CONTHRIF:** Control Buffer Threshold Interrupt Flag bit
1 = The control buffer has more than THRES words of space available
0 = The control buffer has less than THRES words of space available

bit 7 **CONEMPTYIF:** Control Buffer Empty Interrupt Flag bit
1 = Control buffer is empty
0 = Control buffer is not empty

bit 6 **CONFULLIF:** Control Buffer Full Interrupt Flag bit
1 = Control buffer is full
0 = Control buffer is not full

bit 5 **RXTHRIF:** Receive Buffer Threshold Interrupt Flag bit(1)
1 = Receive buffer has more than RXINTTHR words of space available
0 = Receive buffer has less than RXINTTHR words of space available

bit 4 **RXFULLIF:** Receive Buffer Full Interrupt Flag bit
1 = Receive buffer is full
0 = Receive buffer is not full

bit 3 **RXEMPTYIF:** Receive Buffer Empty Interrupt Flag bit
1 = Receive buffer is empty
0 = Receive buffer is not empty

Note 1: In the case of Boot/XIP mode, the POR value of the receive buffer threshold is zero. Therefore, this bit will be set to a ‘1’, immediately after a POR until a read request on the System Bus bus is received.

Note: The bits in the register are cleared by writing a '1' to the corresponding bit position.

REGISTER 22-9: SQI1INTSTAT: SQI INTERRUPT STATUS REGISTER (CONTINUED)

bit 2 **TXTHRIF:** Transmit Buffer Threshold Interrupt Flag bit
1 = Transmit buffer has more than TXINTTHR words of space available
0 = Transmit buffer has less than TXINTTHR words of space available

bit 1 **TXFULLIF:** Transmit Buffer Full Interrupt Flag bit
1 = The transmit buffer is full
0 = The transmit buffer is not full

bit 0 **TXEMPTYIF:** Transmit Buffer Empty Interrupt Flag bit
1 = The transmit buffer is empty
0 = The transmit buffer has content

Note 1: In the case of Boot/XIP mode, the POR value of the receive buffer threshold is zero. Therefore, this bit will be set to a '1', immediately after a POR until a read request on the System Bus bus is received.

Note: The bits in the register are cleared by writing a '1' to the corresponding bit position.

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REGISTER 22-10: SQI1TXDATA: SQI TRANSMIT DATA BUFFER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **TXDATA<31:0>:** Transmit Command Data bits

Data is loaded into this register before being transmitted. Just prior to the beginning of a data transfer, the data in TXDATA is loaded into the shift register (SFDR).

Multiple writes to TXDATA can occur even while a transfer is already in progress. There can be a maximum of eight commands that can be queued.

REGISTER 22-11: SQI1RXDATA: SQI RECEIVE DATA BUFFER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **RXDATA<31:0>:** Receive Data Buffer bits

At the end of a data transfer, the data in the shift register is loaded into the RXDATA register. This register works like a buffer. The depth of the receive buffer is eight words.

REGISTER 22-12: SQI1STAT1: SQI STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBUFFREE<5:0>					
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	RXBUFCNT<5:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as ‘0’

bit 21-16 **TXBUFFREE<5:0>:** Transmit buffer Available Word Space bits

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RXBUFCNT<5:0>:** Number of words of read data in the buffer

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REGISTER 22-13: SQI1STAT2: SQI STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	CMDSTAT<1:0>	
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	CONAVAIL<3:1>		
7:0	R-0	R-0	R-0	R-0	R-0	U-0	R-0	R-0
	CONAVAIL<0>	SQID3	SQID2	SQID1	SQID0	—	RXUN	TXOV

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-18 **Unimplemented:** Read as ‘0’

bit 17-16 **CMDSTAT<1:0>:** Current Command Status bits
These bits indicate the current command status.
11 = Reserved
10 = Receive
01 = Transmit
00 = Idle

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-7 **CONAVAIL<3:0>:** Control buffer Space Available bits
These bits indicate the available control word space.
1000 = 8 words are available
0111 = 7 words are available
•
•
•
0001 = 1 word is available
0000 = No words are available

bit 6 **SQID3:** SQID3 Status bit
1 = Data is present on SQID3
0 = Data is not present on SQID3

bit 5 **SQID2:** SQID2 Status bit
1 = Data is present on SQID2
0 = Data is not present on SQID2

bit 4 **SQID1:** SQID1 Status bit
1 = Data is present on SQID1
0 = Data is not present on SQID1

bit 3 **SQID0:** SQID0 Status bit
1 = Data is present on SQID0
0 = Data is not present on SQID0

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **RXUN:** Receive buffer Underflow Status bit
1 = Receive buffer Underflow has occurred
0 = Receive buffer underflow has not occurred

bit 0 **TXOV:** Transmit buffer Overflow Status bit
1 = Transmit buffer overflow has occurred
0 = Transmit buffer overflow has not occurred

REGISTER 22-14: SQI1BDCON: SQI BUFFER DESCRIPTOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	START	POLLEN	DMAEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as ‘0’

bit 2 **START:** Buffer Descriptor Processor Start bit
- 1 = Start the buffer descriptor processor
- 0 = Disable the buffer descriptor processor

bit 1 **POLLEN:** Buffer Descriptor Poll Enable bit
- 1 = BDP poll is enabled
- 0 = BDP poll is not enabled

bit 0 **DMAEN:** DMA Enable bit
- 1 = DMA is enabled
- 0 = DMA is disabled

REGISTER 22-15: SQI1BDCURADD: SQI BUFFER DESCRIPTOR CURRENT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCURRADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCURRADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCURRADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCURRADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **BDCURRADDR<31:0>:** Current Buffer Descriptor Address bits
These bits contain the address of the current descriptor being processed by the Buffer Descriptor Processor.

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REGISTER 22-16: SQI1BDBASEADD: SQI BUFFER DESCRIPTOR BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **BDADDR<31:0>:** DMA Base Address bits
These bits contain the physical address of the root buffer descriptor. This register should be updated only when the DMA is idle.

REGISTER 22-17: SQI1BDSTAT: SQI BUFFER DESCRIPTOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-x	R-x	R-x	R-x	R-x	R-x
	—	—	BDSTATE<3:0>				DMASTART	DMAACTV
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	BDCON<15:8>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	BDCON<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as ‘0’

bit 21-18 **BDSTATE<3:0>:** DMA Buffer Descriptor Processor State Status bits
These bits return the current state of the buffer descriptor processor:
5 = Fetched buffer descriptor is disabled
4 = Descriptor is done
3 = Data phase
2 = Buffer descriptor is loading
1 = Descriptor fetch request is pending
0 = Idle

bit 17 **DMASTART:** DMA Buffer Descriptor Processor Start Status bit
1 = DMA has started
0 = DMA has not started

bit 16 **DMAACTV:** DMA Buffer Descriptor Processor Active Status bit
1 = Buffer Descriptor Processor is active
0 = Buffer Descriptor Processor is idle

bit 15-0 **BDCON<15:0>:** DMA Buffer Descriptor Control Word bits
These bits contain the current buffer descriptor control word.

REGISTER 22-18: SQI1BDPOLLCON: SQI BUFFER DESCRIPTOR POLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLLCON<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **POLLCON<15:0>:** Buffer Descriptor Processor Poll Status bits
These bits indicate the number of cycles the BDP would wait before refetching the descriptor control word if the previous descriptor fetched was disabled.

REGISTER 22-19: SQI1BDTXDSTAT: SQI BUFFER DESCRIPTOR DMA TRANSMIT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	TXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	TXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	TXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-25 **TXSTATE<3:0>:** Current DMA Transmit State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as ‘0’

bit 20-16 **TXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal buffer space.

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **TXCURBUFLEN<7:0>:** Current DMA Transmit Buffer Length Status bits
These bits provide the length of the current DMA transmit buffer.

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REGISTER 22-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as ‘0’

bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal buffer space.

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **RXCURBUFLEN<7:0>:** Current DMA Receive Buffer Length Status bits
These bits provide the length of the current DMA receive buffer.

REGISTER 22-21: SQI1THR: SQI THRESHOLD CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	THRES<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3-0 **THRES<3:0>:** SQI Control Threshold Value bits
The SQI control threshold interrupt is asserted when the amount of space indicated by THRES<6:0> is available in the SQI control buffer.

REGISTER 22-22: SQI1INTSIGEN: SQI INTERRUPT SIGNAL ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DMAEISE	PKT DONEISE	BD DONEISE	CON THRISE
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11 **DMAEISE:** DMA Bus Error Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 10 **PKTDONEISE:** Receive Error Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 9 **BDDONEISE:** Transmit Error Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 8 **CONTHRISE:** Control Buffer Threshold Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 7 **CONEMPTYISE:** Control Buffer Empty Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 6 **CONFULLISE:** Control Buffer Full Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 5 **RXTHRISE:** Receive Buffer Threshold Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 4 **RXFULLISE:** Receive Buffer Full Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 3 **RXEMPTYISE:** Receive Buffer Empty Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 2 **TXTHRISE:** Transmit Buffer Threshold Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 1 **TXFULLISE:** Transmit Buffer Full Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

bit 0 **TXEMPTYISE:** Transmit Buffer Empty Interrupt Signal Enable bit
1 = Interrupt signal is enabled
0 = Interrupt signal is disabled

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REGISTER 22-23: SQI1TAPCON: SQI TAP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DDRCLKINDLY<5:0>					
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SDRDATINDLY<3:0>				DDRDATINDLY<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	SDRCLKINDLY<5:0>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUTDLY<3:0>				CLKOUTDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as ‘0’

bit 29-24 **DDRCLKINDLY<5:0>:** SQI Clock Input Delay in DDR Mode bits

These bits are used to add fractional delays to SQI Clock Input while sampling the incoming data in DDR mode.

111111 = 64 taps added on clock input
111110 = 63 taps added on clock input
•
•
•
000001 = 2 taps added on clock input
000000 = 1 tap added on clock input

bit 23-20 **SDRDATINDLY<3:0>:** SQI Data Input Delay in SDR Mode bits

These bits are used to add fractional delays to SQI Data Output while writing the data to the Flash in SDR mode.

1111 = 16 taps added on data input
1110 = 15 taps added on data input
•
•
•
0001 = 2 taps added on data input
0000 = 1 tap added on data input

bit 19-16 **DDRDATINDLY<3:0>:** SQI Data Output Delay in DDR Mode bits

These bits are used to add fractional delays to SQI Data Output while writing the data to the Flash in DDR mode.

1111 = 16 taps added on data input
1110 = 15 taps added on data input
•
•
•
0001 = 2 taps added on data input
0000 = 1 tap added on data input

bit 15-14 **Unimplemented:** Read as ‘0’

REGISTER 22-23: SQI1TAPCON: SQI TAP CONTROL REGISTER (CONTINUED)

bit 13-8 **SDRCLKINDLY<5:0>:** SQI Clock Input Delay in SDR Mode bits

These bits are used to add fractional delays to SQI Clock Input while sampling the incoming data in DDR mode.

`111111` = 64 taps added on clock input
`111110` = 63 taps added on clock input
•
•
•
`000001` = 2 taps added on clock input
`000000` = 1 tap added on clock input

bit 7-4 **DATAOUTDLY<3:0>:** SQI Data Output Delay bits

These bits are used to add fractional delays to SQI Data Output while writing the data to the Flash in all modes of operation.

`1111` = 16 taps added on data output
`1110` = 15 taps added on data output
•
•
•
`0001` = 2 taps added on data output
`0000` = 1 tap added on data output

bit 3-0 **CLKOUTDLY<3:0>:** SQI Clock Output Delay bits

These bits are used to add fractional delays to SQI Clock Output while writing the data to the Flash in all modes of operation.

`1111` = 16 taps added on clock output
`1110` = 15 taps added on clock output
•
•
•
`0001` = 2 taps added on clock output
`0000` = 1 tap added on clock output

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REGISTER 22-24: SQI1MEMSTAT: SQI MEMORY STATUS CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	STATPOS	STATTYPE<1:0>		STATBYTES<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATCMD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATCMD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as ‘0’

bit 20 **STATPOS:** Status Bit Position in Flash bit

Indicates the BUSY bit position in the Flash Status register. This bit is added to support all Flash types (with BUSY bit at 0 and at 7).

1 = BUSY bit position is bit 7 in status register
0 = BUSY bit position is bit 0 in status register

bit 19-18 **STATTYPE<1:0>:** Status Command Lane Mode bits

11 = Reserved
10 = Status command and read are executed in Quad Lane mode
01 = Status command and read are executed in Dual Lane mode
00 = Status command and read are executed in Single Lane mode

bit 17-16 **STATBYTES<1:0>:** Number of Status Bytes bits

11 = Reserved
10 = Status command is 2 bytes long
01 = Status command is 1 byte long
00 = Reserved

bit 15-0 **STATCMD<15:0>:** Status Command bits

The status check command is written into these bits

REGISTER 22-25: SQI1XCON3: SQI XIP CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INIT1SCHECK	INIT1COUNT<1:0>		INIT1TYPE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD3<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD2<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT1CMD1<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28 **INIT1SCHECK:** Flash Initialization 1 Command Status Check bit
1 = Check the status after executing the INIT1 commands
0 = Do not check the status

bit 27-26 **INIT1COUNT<1:0>:** Flash Initialization 1 Command Count bits
11 = INIT1CMD1, INIT1CMD2, and INIT1CMD3 are sent
10 = INIT1CMD1 and INIT1CMD2 are sent, but INIT1CMD3 is still pending
01 = INIT1CMD1 is sent, but INIT1CMD2 and INIT1CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT1TYPE<1:0>:** Flash Initialization 1 Command Type bits
11 = Reserved
10 = INIT1 commands are sent in Quad Lane mode
01 = INIT1 commands are sent in Dual Lane mode
00 = INIT1 commands are sent in Single Lane mode

bit 24-16 **INIT1CMD3<7:0>:** Flash Initialization Command 3 bits
Third command of the Flash initialization.

bit 15-8 **INIT1CMD2<7:0>:** Flash Initialization Command 2 bits
Second command of the Flash initialization.

bit 7-0 **INIT1CMD1<7:0>:** Flash Initialization Command 1 bits
First command of the Flash initialization.

Note: Some Flash devices require write enable and sector unprotect commands before write/read operations and this register is useful in working with those Flash types (XIP mode only)

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REGISTER 22-26: SQI1XCON4: SQI XIP CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INIT2SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD3<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD2<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD1<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28 **INIT2SCHECK:** Flash Initialization 2 Command Status Check bit
1 = Check the status after executing the INIT2 commands
0 = Do not check the status

bit 27-26 **INIT2COUNT<1:0>:** Flash Initialization 2 Command Count bits
11 = INIT2CMD1, INIT2CMD2, and INIT2CMD3 are sent
10 = INIT2CMD1 and INIT2CMD2 are sent, but INIT2CMD3 is still pending
01 = INIT2CMD1 is sent, but INIT2CMD2 and INIT2CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT2TYPE<1:0>:** Flash Initialization 2 Command Type bits
11 = Reserved
10 = INIT2 commands are sent in Quad Lane mode
01 = INIT2 commands are sent in Dual Lane mode
00 = INIT2 commands are sent in Single Lane mode

bit 24-16 **INIT2CMD3<7:0>:** Flash Initialization Command 3 bits
Third command of the Flash initialization.

bit 15-8 **INIT2CMD2<7:0>:** Flash Initialization Command 2 bits
Second command of the Flash initialization.

bit 7-0 **INIT2CMD1<7:0>:** Flash Initialization Command 1 bits
First command of the Flash initialization.

Note: Some Flash devices require write enable and sector unprotect commands before write/read operations and this register is useful in working with those Flash types (XIP mode only)

23.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The I^2C module provides complete hardware support for both Client and Multi-Host modes of the I^2C serial communication standard.

Each I^2C module has a 2-pin interface:

- SCLx pin is clock
- SDAx pin is data

Each I^2C module offers the following key features:

- I^2C interface supporting both host and client operation
- I^2C Client mode supports 7-bit and 10-bit addressing
- I^2C Host mode supports 7-bit and 10-bit addressing
- I^2C port allows bidirectional transfers between hosts and clients
- Serial clock synchronization for the I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^2C supports multi-host operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking
- SMBus support

Figure 23-1 illustrates the I^2C module block diagram.

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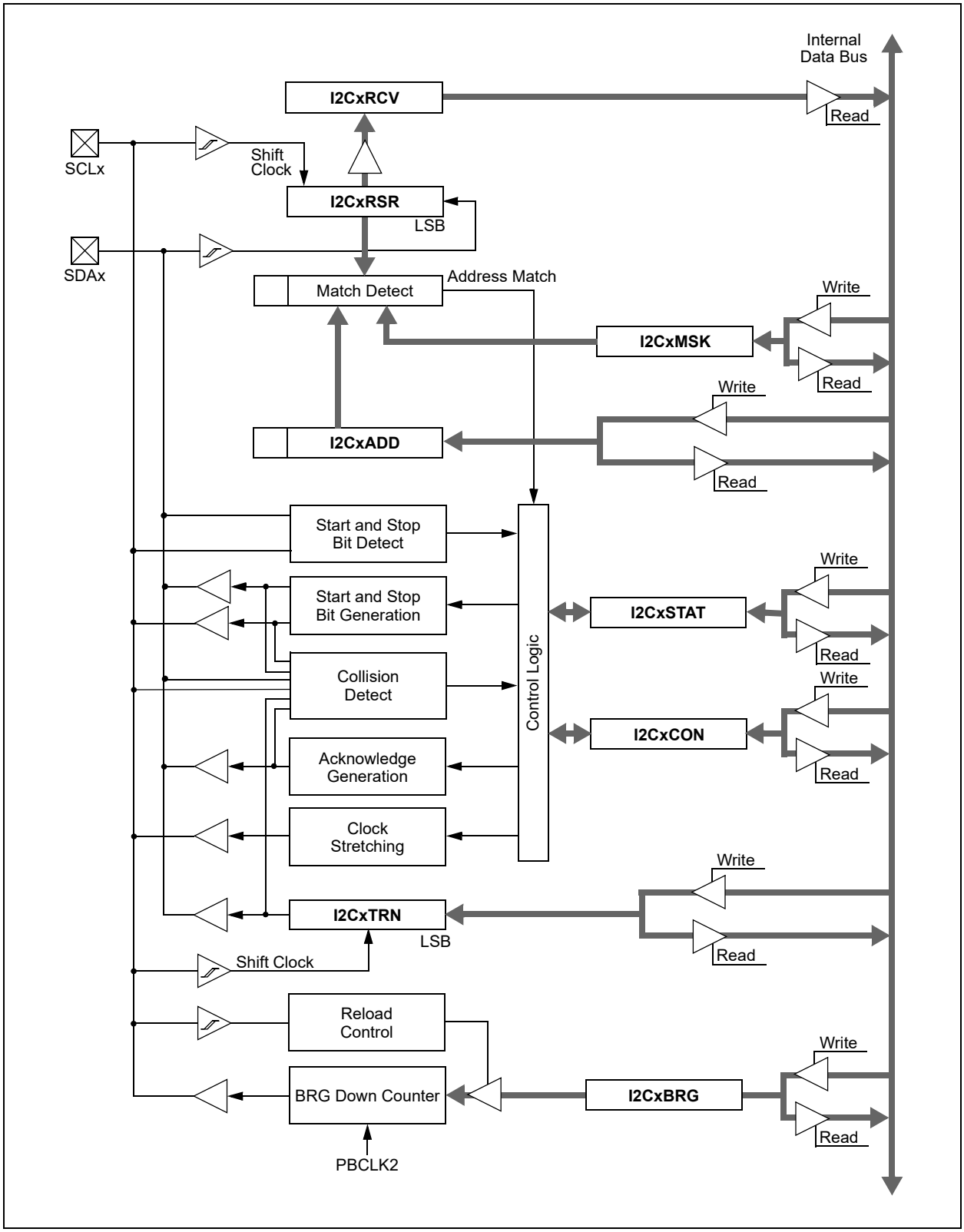
FIGURE 23-1: I²C BLOCK DIAGRAM



23.1 I²C Control Registers

TABLE 23-1: I2C1 THROUGH I2C5 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0010	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0020	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
0030	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
0040	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	I2C1BRG<15:0>																0000
0050	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C1TXDATA<7:0>								0000
0060	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C1RXDATA<7:0>								0000
0200	I2C2CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0210	I2C2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0220	I2C2ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
0230	I2C2MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	MSK<9:0>										0000
0240	I2C2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	I2C2BRG<15:0>																0000
0250	I2C2TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C2TXDATA<7:0>								0000
0260	I2C2RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C2RXDATA<7:0>								0000
0400	I2C3CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0410	I2C3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0420	I2C3ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 23-1: I2C1 THROUGH I2C5 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0430	I2C3MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
0440	I2C3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	I2C3BRG<15:0>																0000
0450	I2C3TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C3TXDATA<7:0>								0000
0460	I2C3RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C3RXDATA<7:0>								0000
0600	I2C4CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0610	I2C4STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0620	I2C4ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
0630	I2C4MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
0640	I2C4BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	I2C4BRG<15:0>																0000
0650	I2C4TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C4TXDATA<7:0>								0000
0660	I2C4RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C4RXDATA<7:0>								0000
0800	I2C5CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
0810	I2C5STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
0820	I2C5ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
0830	I2C5MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ADD<9:0>										0000
0840	I2C5BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	I2C5BRG<15:0>																0000
0850	I2C5TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C4TXDATA<7:0>								0000
0860	I2C5RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C4RXDATA<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 23-1: I2CxCON: I^{2}C CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:	HC = Cleared in Hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **PCIE:** Stop Condition Interrupt Enable bit (I^{2}C Client mode only)
- 1 = Enable interrupt on detection of Stop condition
- 0 = Stop detection interrupts are disabled

bit 21 **SCIE:** Start Condition Interrupt Enable bit (I^{2}C Client mode only)
- 1 = Enable interrupt on detection of Start or Restart conditions
- 0 = Start detection interrupts are disabled

bit 20 **BOEN:** Buffer Overwrite Enable bit (I^{2}C Client mode only)
- 1 = I2CxRCV is updated and $\overline{\text{ACK}}$ is generated for a received address/data byte, ignoring the state of the I2COV bit (I2CxSTAT<6>)only if the RBF bit (I2CxSTAT<2>) = 0
- 0 = I2CxRCV is only updated when the I2COV bit (I2CxSTAT<6>) is clear

bit 19 **SDAHT:** SDA Hold Time Selection bit
- 1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL
- 0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

bit 18 **SBCDE:** Client Mode Bus Collision Detect Enable bit (I^{2}C Client mode only)
- 1 = Enable client bus collision interrupts
- 0 = Client bus collision interrupts are disabled

bit 18 **AHEN:** Address Hold Enable bit (Client mode only)
- 1 = Following the 8th falling edge of SCL for a matching received address byte; SCLREL bit will be cleared and the SCL will be held low.
- 0 = Address holding is disabled

bit 16 **DHEN:** Data Hold Enable bit (I^{2}C Client mode only)
- 1 = Following the 8th falling edge of SCL for a received data byte; client hardware clears the SCLREL bit and SCL is held low
- 0 = Data holding is disabled

bit 15 **ON:** I^{2}C Enable bit
- 1 = Enables the I^{2}C module and configures the SDA and SCL pins as serial port pins
- 0 = Disables the I^{2}C module; all I^{2}C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

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REGISTER 23-1: I2CxCON: I^{2}C CONTROL REGISTER (CONTINUED)

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I^{2}C client)
1 = Release SCLx clock
0 = Hold SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of client transmission. Hardware clear at end of client reception.
If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of client transmission.

bit 11 **STRICT:** Strict I^{2}C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
0 = Strict I^{2}C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Client Address bit
1 = I2CxADD is a 10-bit client address
0 = I2CxADD is a 7-bit client address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control disabled
0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enable I/O pin thresholds compliant with SMBus specification
0 = Disable SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I^{2}C client)
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^{2}C client)
Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^{2}C host, applicable during host receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Send NACK during Acknowledge
0 = Send ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^{2}C host, applicable during host receive)
1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of host Acknowledge sequence.
0 = Acknowledge sequence not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^{2}C host)
1 = Enables Receive mode for I^{2}C. Hardware clear at end of eighth bit of host receive data byte.
0 = Receive sequence not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^{2}C host)
1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of host Stop sequence.
0 = Stop condition not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^{2}C host)
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of host Repeated Start sequence.
0 = Repeated Start condition not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^{2}C host)
1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of host Start sequence.
0 = Start condition not in progress

REGISTER 23-2: I2CxSTAT: I^{2}C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0, HS, HC	R-0, HS, HC	R/C-0, HS, HC	U-0	U-0	R/C-0, HS	R-0, HS, HC	R-0, HS, HC
	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS, SC	R/C-0, HS, SC	R-0, HS, HC	R/C-0, HS, HC	R/C-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF

Legend:	HS = Hardware Set	HC = Hardware Cleared	SC = Software Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	C = Clearable bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I^{2}C host, applicable to host transmit operation)
1 = NACK received from client
0 = ACK received from client
Hardware set or clear at end of client Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^{2}C host, applicable to host transmit operation)
1 = Host transmit is in progress (8 bits + ACK)
0 = Host transmit is not in progress
Hardware set at beginning of host transmission. Hardware clear at end of client Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (Valid in I^{2}C Client mode only)
1 = I^{2}C bus is in an Acknowledge sequence, set on 8th falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 12-11 **Unimplemented:** Read as ‘0’

bit 10 **BCL:** Host Bus Collision Detect bit
1 = A bus collision has been detected during a host operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

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REGISTER 23-2: I2CxSTAT: I^{2}C STATUS REGISTER (CONTINUED)

bit 5 **D_A:** Data/Address bit (when operating as I^{2}C client)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of client byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I^{2}C client)
1 = Read – indicates data transfer is output from client
0 = Write – indicates data transfer is input to client
Hardware set or clear after reception of I^{2}C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

24.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

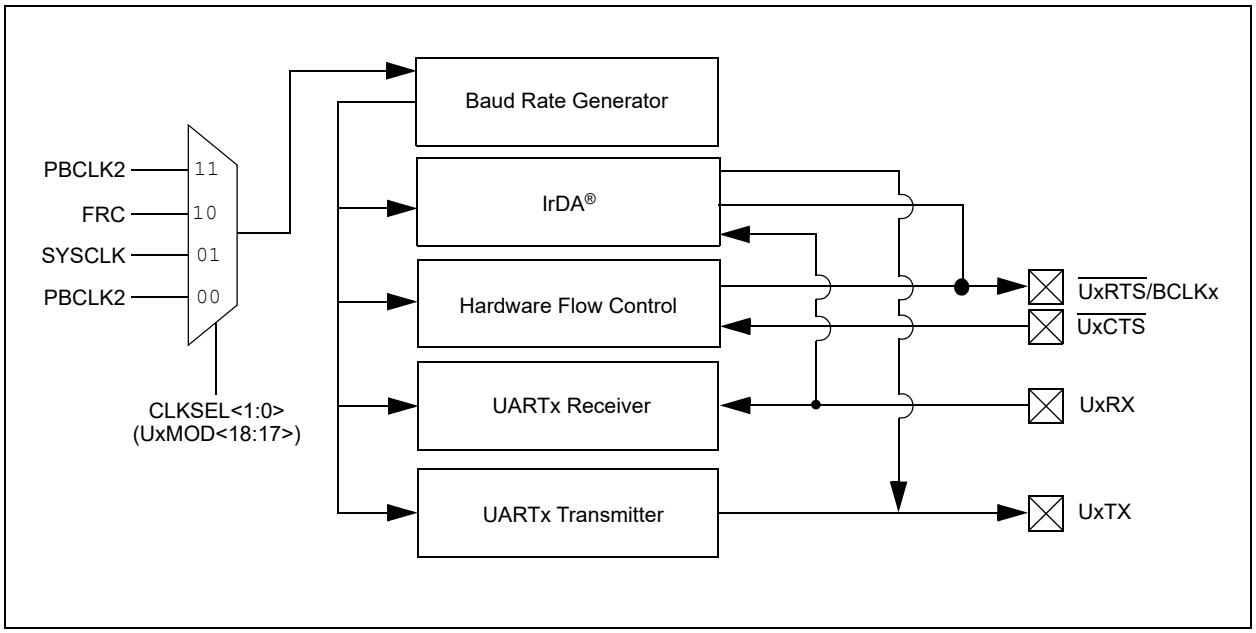
The UART module is one of the serial I/O modules available in the PIC32MZ DAK/DAL/DAR/DAS family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The key features of the UART module are as follows:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd, or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 25 Mbps at 100 MHz (PBCLK2)
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = `1`)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support
- Auto-baud support
- Ability to receive data during Sleep mode

Figure 24-1 illustrates a simplified block diagram of the UART module.

FIGURE 24-1: UART SIMPLIFIED BLOCK DIAGRAM



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24.1 UART Control Registers

TABLE 24-1: UART1 THROUGH UART6 REGISTER MAP

Virtual Address (BF82_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000	U1MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2010	U1STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2040	U1BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2200	U2MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2210	U2STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2220	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2230	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2240	U2BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2400	U3MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2410	U3STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2420	U3TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2430	U3RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2440	U3BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 24-1: UART1 THROUGH UART6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2600	U4MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2610	U4STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2620	U4TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2630	U4RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2640	U4BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2800	U5MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2810	U5STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2820	U5TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2830	U5RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2840	U5BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2A00	U6MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2A10	U6STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2A20	U6TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2A30	U6RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2A40	U6BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 24-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R-0, HS, HC	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		RUNOVF
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>(1)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:	HS = Hardware set	HC = Hardware cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23 **SLPEN:** Run During Sleep Enable bit
- 1 = UARTx BRG clock runs during Sleep mode
- 0 = UARTx BRG clock is turned off during Sleep mode

Note: SLPEN = 1 only applies if CLKSEL = FRC. All clocks, as well as the UART, are disabled in Deep Sleep mode.

bit 22 **ACTIVE:** UARTx Module Running Status bit
- 1 = UARTx module is active (UxMODE register should not be updated)
- 0 = UARTx module is not active (UxMODE register can be updated)

bit 21-19 **Unimplemented:** Read as ‘0’

bit 18-17 **CLKSEL<1:0>:** UARTx Module Clock Selection bits
- 11 = BRG clock is PBCLK2
- 10 = BRG clock is FRC
- 01 = BRG clock is SYSCLK (turned off in Sleep mode)
- 00 = BRG clock is PBCLK2 (turned off in Sleep mode)

bit 16 **RUNOVF:** Run During Overflow Condition Mode bit
- 1 = When an Overflow Error (OERR) condition is detected, the shift register continues to run to remain synchronized
- 0 = When an Overflow Error (OERR) condition is detected, the shift register stops accepting new data (Legacy mode)

bit 15 **ON:** UARTx Enable bit
- 1 = UARTx module is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
- 0 = UARTx module is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx, and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation in Idle mode

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **Section 12.4 “Peripheral Pin Select (PPS)”** for more information).

REGISTER 24-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Module Enable bits(1)
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
- 1 = Wake-up enabled
- 0 = Wake-up disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
- 1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
- 0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
- 1 = UxRX Idle state is '0'
- 0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
- 1 = High-Speed mode – 4x baud clock enabled
- 0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
- 11 = 9-bit data, no parity
- 10 = 8-bit data, odd parity
- 01 = 8-bit data, even parity
- 00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
- 1 = 2 Stop bits
- 0 = 1 Stop bit

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **Section 12.4 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 24-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MASK<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-25 **MASK<7:0>:** UARTx Address Match Mask bits

These bits are used to mask the ADDR<7:0> bits.

`11111111` = Corresponding ADDRx bits are used to detect the address match

Note: This setting allows the user to assign individual address as well as a group broadcast address to a UART.

`00000000` = Corresponding ADDRx bits are not used to detect the address match.

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

When the ADDEN bit is ‘`1`’, this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits

`11` = Reserved, do not use
`10` = Interrupt is generated and asserted while the transmit buffer is empty
`01` = Interrupt is generated and asserted when all characters have been transmitted
`00` = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

<u>If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is ‘`0`’):</u>
`1` = UxTX Idle state is ‘`0`’
`0` = UxTX Idle state is ‘`1`’

<u>If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is ‘`1`’):</u>
`1` = IrDA encoded UxTX Idle state is ‘`1`’
`0` = IrDA encoded UxTX Idle state is ‘`0`’

bit 12 **URXEN:** Receiver Enable bit

`1` = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = `1`)
`0` = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module

Note: The event of disabling an enabled receiver will release the RX pin to the PORT function; however, the receive buffers *will not* be reset. Disabling the receiver has no effect on the receive status flags.

bit 11 **UTXBRK:** Transmit Break bit

`1` = Send Break on next transmission. Start bit followed by twelve ‘`0`’ bits, followed by Stop bit; cleared by hardware upon completion
`0` = Break transmission is disabled or completed

REGISTER 24-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 10 **UTXEN:** Transmit Enable bit
1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)
0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset

Note: The event of disabling an enabled transmitter will release the TX pin to the PORT function and reset the transmit buffers to empty. Any pending transmission is aborted and data characters in the transmit buffers are lost. All transmit status flags are cleared and the TRMT bit is set

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
1 = Transmit buffer is full
0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

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Figure 24-2 and Figure 24-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 24-2: UART RECEPTION

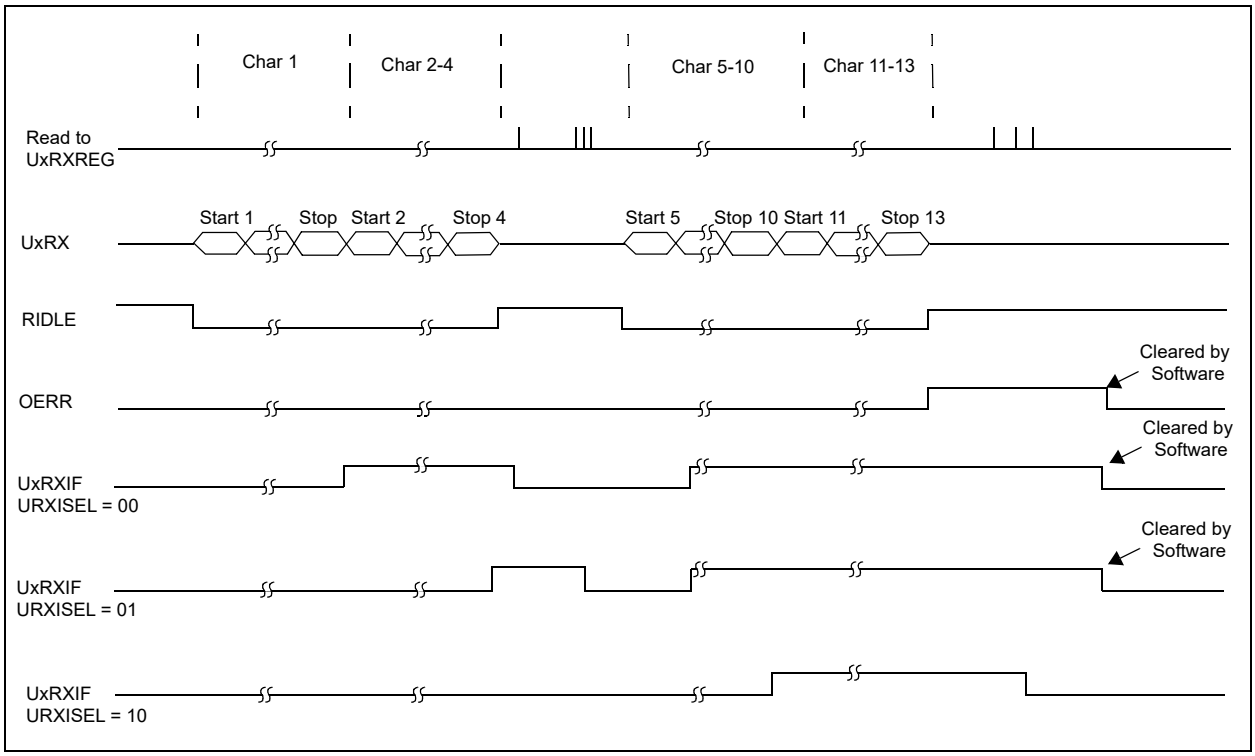
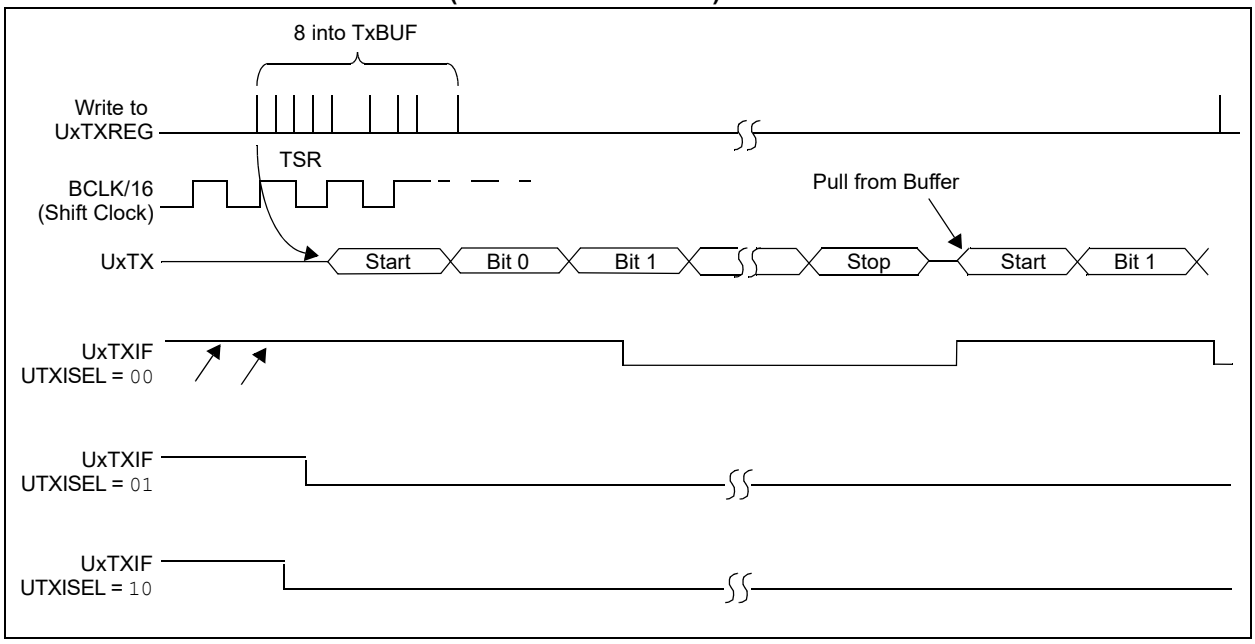


FIGURE 24-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



25.0 PARALLEL HOST PORT (PMP)

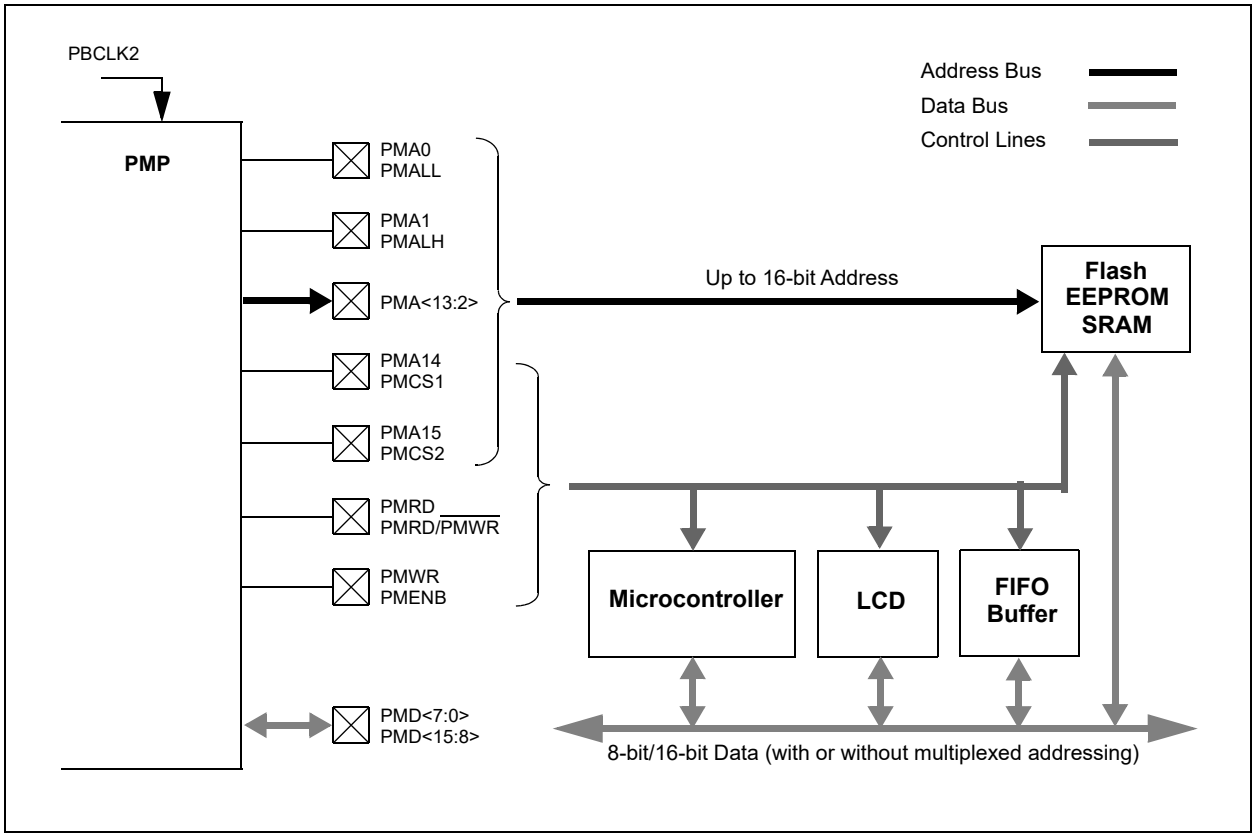
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

The following are key features of the PMP module:

- 8-bit,16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options:
  - Individual read and write strobes, or
  - Read/$\overline{\text{write}}$ strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Client Port (PSP) support:
  - Legacy addressable
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait states
- Operate during Sleep and Idle modes
- Separate configurable read/write registers or dual buffers for Host mode
- Fast bit manipulation using CLR, SET, and INV registers

FIGURE 25-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



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25.1 Control Registers

TABLE 25-1: PMP REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
E000	PMCON	31:16	—	—	—	—	—	—	—	—	RDSTART	—	—	—	—	—	DUALBUF	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
E010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
E020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CS2	CS1	ADDR<13:0>														0000
			ADDR15	ADDR14															0000
E030	PMDOUT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAOUT<15:0>																0000
E040	PMDIN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAIN<15:0>																0000
E050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN<15:0>																0000
E060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F
E070	PMWADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WCS2	WCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			WADDR15	WADDR14	WADDR<13:0>														0000
E080	PMRADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RCS2	RCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			RADDR15	RADDR14	RADDR<13:0>														0000
E090	PMRDIN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RDATAIN<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 25-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
	RDSTART	—	—	—	—	—	DUALBUF	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(2)		ALP(2)	CS2P(2)	CS1P(2)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23 **RDSTART:** Start Read on PMP Bus bit
This bit is cleared by hardware at the end of the read cycle.
1 = Start a read cycle on the PMP bus
0 = No effect

bit 22-18 **Unimplemented:** Read as ‘0’

bit 17 **DUALBUF:** PMP Dual Read/Write Buffer Enable bit
This bit is only valid in Host mode.
1 = PMP uses separate registers for reads and writes
Reads: PMRADDR and PMRDIN
Writes: PMRWADDR and PMDOUT
0 = PMP uses legacy registers for reads and writes
Reads/Writes: PMADDR and PMRDIN

bit 16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** PMP Enable bit(1)
1 = PMP enabled
0 = PMP disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = All 16 bits of address are multiplexed on PMD<15:0>
10 = All 16 bits of address are multiplexed on PMD<7:0>
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper 8 bits are on PMA<15:8>
00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

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REGISTER 25-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/PMWR port is enabled
0 = PMRD/PMWR port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
11 = Reserved
10 = PMCS1 and PMCS2 function as Chip Select
01 = PMCS1 functions as address bit 14; PMCS2 functions as Chip Select
00 = PMCS1 and PMCS2 function as address bits 14 and 15, respectively

bit 5 **ALP:** Address Latch Polarity bit(2)
1 = Active-high (PMALL and PMALH)
0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **CS2P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS2)
0 = Active-low ($\overline{\text{PMCS2}}$)

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Client Modes and Host mode 2 (MODE<1:0> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Host mode 1 (MODE<1:0> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Client modes and Host mode 2 (MODE<1:0> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)
For Host mode 1 (MODE<1:0> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 25-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0>(1)		WAITM<3:0>(1)				WAITE<1:0>(1)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **BUSY:** Busy bit (Host mode only)
- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Client mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

Note: These bits only control the generation of the PMP interrupt. The PMP Error (PMPE) is always generated.

bit 12-11 **INCM<1:0>:** Increment Mode bits
- 11 = Client mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<15:0> by 1 every read/write cycle(2)
- 01 = Increment ADDR<15:0> by 1 every read/write cycle(2)
- 00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit
- 1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer
- 0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
- 11 = Host mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>(3))
- 10 = Host mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>(3))
- 01 = Enhanced Client mode, control signals (PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>)
- 00 = Legacy PSP, control signals (PMRD, PMWR, PMCS and PMD<7:0>)

Note 1: Whenever WAITM<3:0> = 0000, the WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when the MODE16 = 1 (16-bit mode).

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REGISTER 25-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits(1)

11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits(1)

1111 = Wait of 16 TPB
•
•
•
0001 = Wait of 2 TPB
0000 = Wait of 1 TPB (default)

bit 1-0 **WAITE<1:0>:** Data Hold After Read/Write Strobe Wait States bits(1)

11 = Wait of 4 TPB
10 = Wait of 3 TPB
01 = Wait of 2 TPB
00 = Wait of 1 TPB (default)

For Read operations:
11 = Wait of 3 TPB
10 = Wait of 2 TPB
01 = Wait of 1 TPB
00 = Wait of 0 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, the WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when the MODE16 = 1 (16-bit mode).

REGISTER 25-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2(1)	CS1(3)	ADDR<13:8>					
	ADDR15(2)	ADDR14(4)						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **CS2:** Chip Select 2 bit(1)
- 1 = Chip Select 2 is active
- 0 = Chip Select 2 is inactive

bit 15 **ADDR<15>:** Target Address bit 15(2)

bit 14 **CS1:** Chip Select 1 bit(3)
- 1 = Chip Select 1 is active
- 0 = Chip Select 1 is inactive

bit 14 **ADDR<14>:** Target Address bit 14(4)

bit 13-0 **ADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
2: When the CSF<1:0> bits (PMCON<7:6>) = 00.
3: When the CSF<1:0> bits (PMCON<7:6>) = 10.
4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: If the DUALBUF bit (PMCON<17>) = 0, the bits in this register control both read and write target addressing. If the DUALBUF bit = 1, the bits in this register are not used. In this instance, use the PMRADDR register for Read operations and the PMWADDR register for Write operations.

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REGISTER 25-4: PMDOUT: PARALLEL PORT OUTPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **DATAOUT<15:0>:** Port Data Output bits

This register is used for Read operations in the Enhanced Parallel Client mode and Write operations for Dual Buffer Host mode.

In Dual Buffer Host mode, the DUALBUF bit (PMPCON<17>) = 1, a write to the MSB triggers the transaction on the PMP port. When MODE16 = 1, MSB = DATAOUT<15:8>. When MODE16 = 0, MSB = DATAOUT<7:0>.

Note: In Host mode, a read will return the last value written to the register. In Client mode, a read will return indeterminate results.

REGISTER 25-5: PMDIN: PARALLEL PORT INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **DATAIN<15:0>:** Port Data Input bits

This register is used for both PMP mode and Enhanced Parallel Client mode.

In Parallel Host mode, a write to the MSB triggers the write transaction on the PMP port. Similarly, a read to the MSB triggers the read transaction on the PMP port.

When MODE16 = 1, MSB = DATAIN<15:8>. When MODE16 = 0, MSB = DATAIN<7:0>.

Note: This register is not used in Dual Buffer Host mode (that is, DUALBUF bit (PMPCON<17>) = 1).

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REGISTER 25-6: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<15:14>(1)		PTEN<13:8>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<7:2>						PTEN<1:0>(2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Write ‘0’; ignore read

bit 15-14 **PTEN<15:14>:** PMCSx Address Port Enable bits
- 1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1(1)
- 0 = PMA15 and PMA14 function as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
- 1 = PMA<13:2> function as PMP address lines
- 0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits
- 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)
- 0 = PMA1 and PMA0 pads function as port I/O

Note 1: The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

REGISTER 25-7: PMSTAT: PARALLEL PORT STATUS REGISTER (CLIENT MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HS = Hardware Set	SC = Software Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
- 0 = An overflow has not occurred

Note: When this bit is set in Client mode, it will generate a PMP Error (PMPE) interrupt.

bit 13-12 **Unimplemented:** Read as ‘0’

bit 11-8 **IBxF:** Input Buffer ‘x’ Status Full bits
- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3-0 **OBxE:** Output Buffer ‘x’ Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

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REGISTER 25-8: PMWADDR: PARALLEL PORT WRITE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WCS2(1)	WCS1(3)	WADDR<13:8>					
	WADDR15(2)	WADDR14(4)						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **WCS2:** Chip Select 2 bit(1)

1 = Chip Select 2 is active
0 = Chip Select 2 is inactive

bit 15 **WADDR<15>:** Target Address bit 15(2)

bit 14 **WCS1:** Chip Select 1 bit(3)

1 = Chip Select 1 is active
0 = Chip Select 1 is inactive

bit 14 **WADDR<14>:** Target Address bit 14(4)

bit 13-0 **WADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
2: When the CSF<1:0> bits (PMCON<7:6>) = 00.
3: When the CSF<1:0> bits (PMCON<7:6>) = 10.
4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to ‘1’.

REGISTER 25-9: PMRADDR: PARALLEL PORT READ ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RCS2(1)	RCS1(3)	RADDR<13:8>					
	RADDR15(2)	RADDR14(4)						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **RCS2:** Chip Select 2 bit(1)

1 = Chip Select 2 is active
0 = Chip Select 2 is inactive (RADDR15 function is selected)

bit 15 **RADDR<15>:** Target Address bit 15(2)

bit 14 **RCS1:** Chip Select 1 bit(3)

1 = Chip Select 1 is active
0 = Chip Select 1 is inactive (RADDR14 function is selected)

bit 14 **RADDR<14>:** Target Address bit 14(4)

bit 13-0 **RADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
2: When the CSF<1:0> bits (PMCON<7:6>) = 00.
3: When the CSF<1:0> bits (PMCON<7:6>) = 10.
4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to ‘1’.

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REGISTER 25-10: PMRDIN: PARALLEL PORT READ INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RDATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RDATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **RDATAIN<15:0>:** Port Read Input Data bits

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to ‘1’ and exclusively for reads. If the DUALBUF bit is ‘0’, the PMDIN register (Register 25-5) is used for reads instead of PMRDIN.

26.0 EXTERNAL BUS INTERFACE (EBI)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 47. "External Bus Interface (EBI)"**, which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

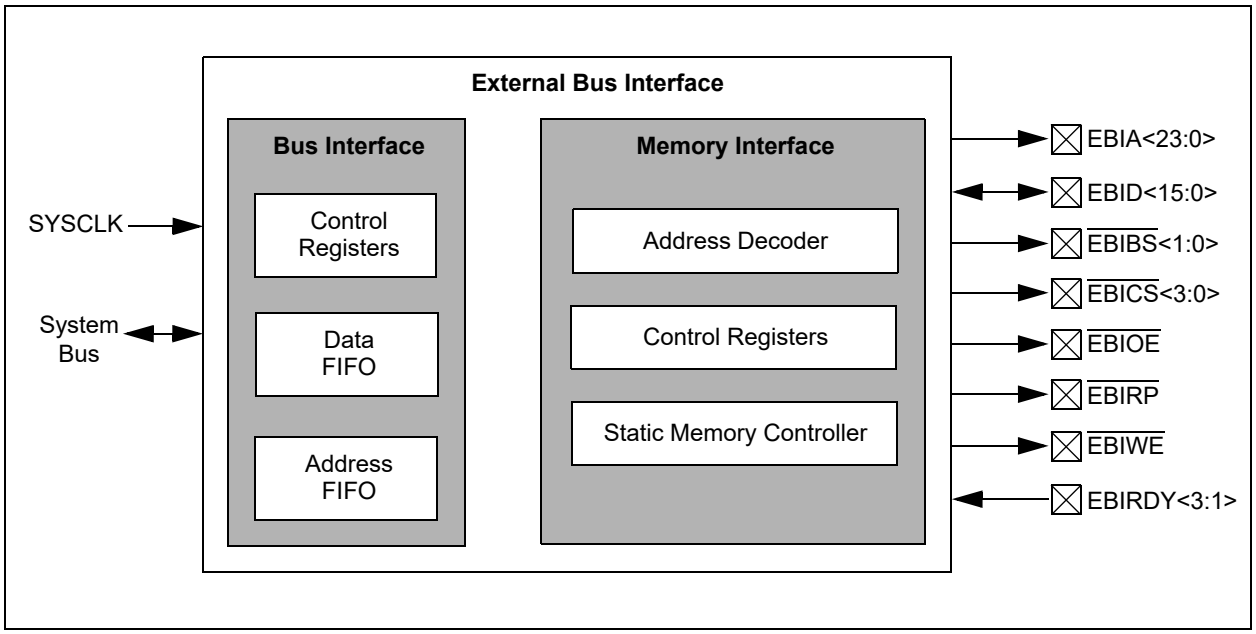
The External Bus Interface (EBI) module provides a high-speed, convenient way to interface external parallel memory devices to the PIC32MZ DAK/DAL/DAR/DAS family of devices.

With the EBI module, it is possible to connect asynchronous SRAM and NOR Flash devices, as well as non-memory devices such as camera sensors and LCDs.

Note 1: Once the EBI module is configured, external devices will be memory mapped and can be access from KSEG2 memory space (see Figure 4-1 through Figure 4-2 in **Section 4.0 "Memory Organization"** for more information). The MMU must be enabled and the TLB must be set up to access this memory (see **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"* for more information).

2: When using the EBI module, Graphics LCD (GLCD) Controller functionality is not available, as most of the I/O between the EBI module and the GLCD is shared.

FIGURE 26-1: EBI SYSTEM BLOCK DIAGRAM



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26.1 EBI Control Registers

TABLE 26-1: EBI REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1014	EBICS0	31:16	CSADDR<15:0>																2000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1018	EBICS1	31:16	CSADDR<15:0>																1000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
101C	EBICS2	31:16	CSADDR<15:0>																2040
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1020	EBICS3	31:16	CSADDR<15:0>																1040
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1054	EBIMSK0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0020
1058	EBIMSK1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0020
105C	EBIMSK2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0120
1060	EBIMSK3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0120
1094	EBISMT0	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>		TRC<5:0>						2D4B
1098	EBISMT1	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>		TRC<5:0>						2D4B
109C	EBISMT2	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>		TRC<5:0>						2D4B
10A0	EBIFTRPD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRPD<11:0>												00C8
10A4	EBISMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SMDWIDTH2<2:0>			SMDWIDTH1<2:0>			SMDWIDTH0<2:0>			—	—	—	—	—	—	SMRP	0201

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 26-1: EBICSx: EXTERNAL BUS INTERFACE CHIP SELECT REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CSADDR<15:0>:** Base Address for Device bits
Address in physical memory, which will select the external device.

bit 15-0 **Unimplemented:** Read as '0'

Note: Memory base address should be aligned on memory size boundary selected by the EBIMSKx<4:0>. For example, 2MB of memory can be assigned at base address 0x2000_0000 and 0x2020_0000, but not at 0x2010_0000.

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REGISTER 26-2: EBIMSKx: EXTERNAL BUS INTERFACE ADDRESS MASK REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	REGSEL<2:0>		
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MEMTYPE<2:0>			MEMSIZE<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **REGSEL<2:0>:** Timing Register Set for Chip Select 'x' bits

111 = Reserved
•
•
•
011 = Reserved
010 = Use EBISMT2
001 = Use EBISMT1
000 = Use EBISMT0

bit 7-5 **MEMTYPE<2:0>:** Select Memory Type for Chip Select 'x' bits

111 = Reserved
•
•
•
011 = Reserved
010 = NOR-Flash
001 = SRAM
000 = Reserved

bit 4-0 **MEMSIZE<4:0>:** Select Memory Size for Chip Select 'x' bits

11111 = Reserved
•
•
•
01010 = Reserved
01001 = 16 MB
01000 = 8 MB
00111 = 4 MB
00110 = 2 MB
00101 = 1 MB
00100 = 512 KB
00011 = 256 KB
00010 = 128 KB
00001 = 64 KB (smaller memories alias within this range)
00000 = Chip Select is not used

REGISTER 26-3: EBISMTx: EXTERNAL BUS INTERFACE STATIC MEMORY TIMING REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>	
23:16	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	PAGEMODE	TPRC<3:0>(1)				TBTA<2:0>(1)		
15:8	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
	TWP<5:0>(1)						TWR<1:0>(1)	
7:0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
	TAS<1:0>(1)		TRC<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **RDYMODE:** Data Ready Device Select bit
The device associated with register set 'x' is a data-ready device, and will use the EBIRDYx pin.
1 = EBIRDYx input is used
0 = EBIRDYx input is not used

bit 25-24 **PAGESIZE<1:0>:** Page Size for Page Mode Device bits
11 = 32-word page
10 = 16-word page
01 = 8-word page
00 = 4-word page

bit 23 **PAGEMODE:** Memory Device Page Mode Support bit
1 = Device supports Page mode
0 = Device does not support Page mode

bit 22-19 **TPRC<3:0>:** Page Mode Read Cycle Time bits(1)
Read cycle time is TPRC + 1 clock cycle.

bit 18-16 **TBTA<2:0>:** Data Bus Turnaround Time bits(1)
Clock cycles (0-7) for static memory between read-to-write, write-to-read, and read-to-read when Chip Select changes.

bit 15-10 **TWP<5:0>:** Write Pulse Width bits(1)
Write pulse width is TWP + 1 clock cycle.

bit 9-8 **TWR<1:0>:** Write Address/Data Hold Time bits(1)
Number of clock cycles to hold address or data on the bus.

bit 7-6 **TAS<1:0>:** Write Address Setup Time bits(1)
Clock cycles for address setup time. A value of '0' is only valid in the case of SSRAM.

bit 5-0 **TRC<5:0>:** Read Cycle Time bits(1)
Read cycle time is TRC + 1 clock cycle.

Note 1: Refer to **Section 47. "External Bus Interface (EBI)"** in the *"PIC32 Family Reference Manual"* for the EBI timing diagrams and additional information.

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REGISTER 26-4: EBIFTRPD: EXTERNAL BUS INTERFACE FLASH TIMING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	TRPD<11:8>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRPD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11-0 **TRPD<11:0>:** Flash Timing bits

These bits define the number of clock cycles to hold the external Flash memory in reset.

REGISTER 26-5: EBISMCON: EXTERNAL BUS INTERFACE STATIC MEMORY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
	SMDWIDTH2<2:0>			SMDWIDTH1<2:0>			SMDWIDTH0<2:1>	
7:0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
	SMDWIDTH0<0>	—	—	—	—	—	—	SMRP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-13 **SMDWIDTH2<2:0>:** Static Memory Width for Register EBISMT2 bits

111 = Reserved
110 = Reserved
101 = Reserved
100 = 8 bits
011 = Reserved
010 = Reserved
001 = Reserved
000 = 16 bits

bit 12-10 **SMDWIDTH1<2:0>:** Static Memory Width for Register EBISMT1 bits

111 = Reserved
110 = Reserved
101 = Reserved
100 = 8 bits
011 = Reserved
010 = Reserved
001 = Reserved
000 = 16 bits

bit 9-7 **SMDWIDTH0<2:0>:** Static Memory Width for Register EBISMT0 bits

111 = Reserved
110 = Reserved
101 = Reserved
100 = 8 bits
011 = Reserved
010 = Reserved
001 = Reserved
000 = 16 bits

bit 6-1 **Unimplemented:** Read as ‘0’

bit 0 **SMRP:** Flash Reset/Power-down mode Select bit

After a Reset, the controller internally performs a power-down for Flash, and then sets this bit to ‘1’.

1 = Flash is taken out of Power-down mode
0 = Flash is forced into Power-down mode

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NOTES:

27.0 CRYPTO ENGINE

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Crypto Engine is intended to accelerate applications that need cryptographic functions. By executing these functions in the hardware module, software overhead is reduced, and actions such as encryption, decryption, and authentication can execute much more quickly.

The Crypto Engine uses an internal descriptor-based DMA for efficient programming of the security association data and packet pointers (allowing scatter/gather data fetching). An intelligent state machine schedules the crypto engines based on the protocol selection and packet boundaries. The hardware engines can perform the encryption and authentication in sequence or in parallel.

Key features of the Crypto Engine are:

- Bulk ciphers and hash engines
- Integrated DMA to off-load processing:
  - Buffer descriptor-based
  - Secure association per buffer descriptor
- Some functions can execute in parallel

Bulk ciphers that are handled by the Crypto Engine include:

- AES:
  - 128-bit, 192-bit, and 256-bit key sizes
  - CBC, ECB, CTR, CFB, and OFB modes
- DES/TDES:
  - CBC, ECB, CFB, and OFB modes

Authentication engines that are available through the Crypto Engine include:

- SHA-1
- SHA-256
- MD-5
- AES-GCM
- HMAC operation (for all authentication engines)

The rate of data that can be processed by the Crypto Engine depends on a number of factors, including:

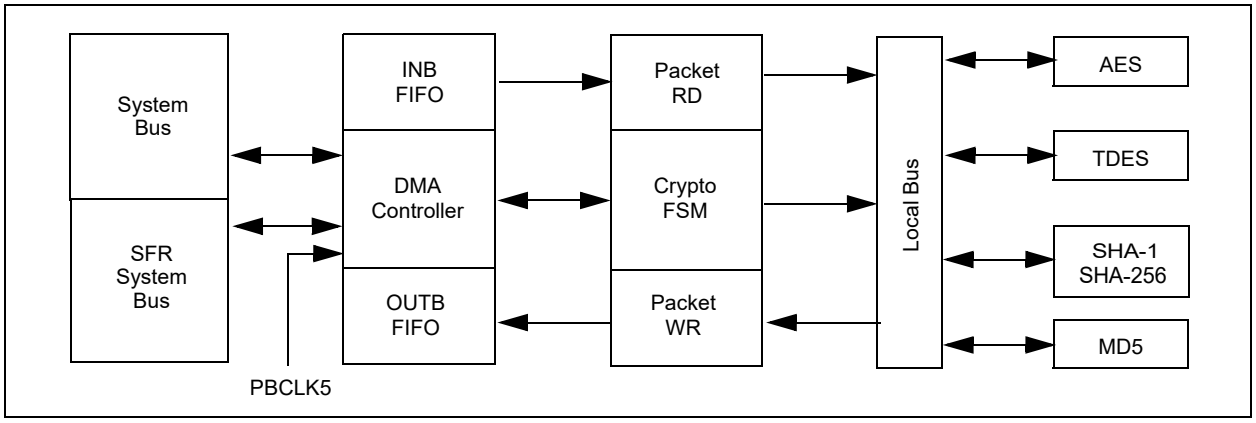
- Which engine is in use
- Whether the engines are used in parallel or in series
- The demands on source and destination memories by other parts of the system (i.e., CPU, DMA, etc.)
- The speed of PBCLK5, which drives the Crypto Engine

Table 27-1 provides typical performance for various engines. Figure 27-1 illustrates the Crypto Engine block diagram.

TABLE 27-1: CRYPTO ENGINE PERFORMANCE

Engine/ Algorithm	Performance Factor (Mbps/MHz)	Maximum Mbps (PBCLK5 = 100 MHz)
DES	14.4	1440
TDES	6.6	660
AES-128	9.0	900
AES-192	7.9	790
AES-256	7.2	720
MD5	15.6	1560
SHA-1	13.2	1320
SHA-256	9.3	930

FIGURE 27-1: CRYPTO ENGINE BLOCK DIAGRAM



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27.1 Crypto Engine Control Registers

TABLE 27-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>				START	ACTIVE	0000
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>								0000
5024	CETRLLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRLRLEN<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 27-1: CEVER: CRYPTO ENGINE REVISION, VERSION, AND ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **REVISION<7:0>:** Crypto Engine Revision bits

bit 23-16 **VERSION<7:0>:** Crypto Engine Version bits

bit 15-0 **ID<15:0>:** Crypto Engine Identification bits

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REGISTER 27-2: CECON: CRYPTO ENGINE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0, HC	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **SWAPOEN:** Swap Output Data Enable bit
1 = Output data is byte swapped when written by dedicated DMA
0 = Output data is not byte swapped when written by dedicated DMA

bit 6 **SWRST:** Software Reset bit
1 = Initiate a software reset of the Crypto Engine
0 = Normal operation

bit 5 **SWAPEN:** I/O Swap Enable bit
1 = TFDMA inputs and RFDMA outputs are swapped
0 = TFDMA inputs and RFDMA outputs are not swapped

bit 4-3 **Unimplemented:** Read as ‘0’

bit 2 **BDPCHST:** Buffer Descriptor Processor (BDP) Fetch Enable bit
This bit should be enabled only after all DMA descriptor programming is completed.
1 = BDP descriptor fetch is enabled
0 = BDP descriptor fetch is disabled

bit 1 **BDPPLEN:** Buffer Descriptor Processor Poll Enable bit
This bit should be enabled only after all DMA descriptor programming is completed.
1 = Poll for descriptor until valid bit is set
0 = Do not poll

bit 0 **DMAEN:** DMA Enable bit
1 = Crypto Engine DMA is enabled
0 = Crypto Engine DMA is disabled

REGISTER 27-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **BDPADDR<31:0>:** Current Buffer Descriptor Process Address Status bits
These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

REGISTER 27-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/w-0	R/w-0	R/w-0	R/w-0	R/w-0	R/w-0	R/w-0	R/w-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** DMA Base Address Status bits
These bits contain the base address of the DMA controller. After a reset, a fetch starts from this address.

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REGISTER 27-5: CESTAT: CRYPTO ENGINE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>	
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	BDSTATE				START	ACTIVE
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCTRL<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCTRL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **ERRMOD<2:0>:** Internal Error Mode Status bits
- 111 = Reserved
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CEK operation
- 010 = KEK operation
- 001 = Preboot authentication
- 000 = Normal operation

bit 28-26 **ERROP<2:0>:** Internal Error Operation Status bits
- 111 = Reserved
- 110 = Reserved
- 101 = Reserved
- 100 = Authentication
- 011 = Reserved
- 010 = Decryption
- 001 = Encryption
- 000 = Reserved

bit 25-24 **ERRPHASE<1:0>:** Internal Error Phase of DMA Status bits
- 11 = Destination data
- 10 = Source data
- 01 = Security Association (SA) access
- 00 = Buffer Descriptor (BD) access

bit 23-22 **Unimplemented:** Read as ‘0’

bit 21-18 **BDSTATE<3:0>:** Buffer Descriptor Processor State Status bits

These bits contain a number, which indicates the current state of the BDP:
- 1111 = Reserved

•
•
•

- 0111 = Reserved
- 0110 = SA fetch
- 0101 = Fetch BDP is disabled
- 0100 = Descriptor is done
- 0011 = Data phase
- 0010 = BDP is loading
- 0001 = Descriptor fetch request is pending
- 0000 = BDP is idle

bit 17 **START:** DMA Start Status bit
- 1 = DMA start has occurred
- 0 = DMA start has not occurred

REGISTER 27-5: CESTAT: CRYPTO ENGINE STATUS REGISTER (CONTINUED)

bit 16 **ACTIVE:** Buffer Descriptor Processor Status bit
`1` = BDP is active
`0` = BDP is idle

bit 15-0 **BDCTRL<15:0>:** Descriptor Control Word Status bits
These bits contain the current descriptor control word.

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REGISTER 27-6: CEINTSRC: CRYPTO ENGINE INTERRUPT SOURCE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3 **AREIF:** Access Response Error Interrupt bit
1 = Error occurred trying to access memory outside the Crypto Engine
0 = No error has occurred

bit 2 **PKTIF:** DMA Packet Completion Interrupt Status bit
1 = DMA packet was completed
0 = DMA packet was not completed

bit 1 **CBDIF:** BD Transmit Status bit
1 = Last BD transmit was processed
0 = Last BD transmit has not been processed

bit 0 **PENDIF:** Crypto Engine Interrupt Pending Status bit
1 = Crypto Engine interrupt is pending (this value is the result of an OR of all interrupts in the Crypto Engine)
0 = Crypto Engine interrupt is not pending

REGISTER 27-7: CEINTEN: CRYPTO ENGINE INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AREIE	PKTIE	BDPIE	PENDIE(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3 **AREIE:** Access Response Error Interrupt Enable bit
- 1 = Access response error interrupts are enabled
- 0 = Access response error interrupts are not enabled

bit 2 **PKTIE:** DMA Packet Completion Interrupt Enable bit
- 1 = DMA packet completion interrupts are enabled
- 0 = DMA packet completion interrupts are not enabled

bit 1 **BDPIE:** DMA Buffer Descriptor Processor Interrupt Enable bit
- 1 = BDP interrupts are enabled
- 0 = BDP interrupts are not enabled

bit 0 **PENDIE:** Host Interrupt Enable bit(1)
- 1 = Crypto Engine interrupts are enabled
- 0 = Crypto Engine interrupts are not enabled

Note 1: The PENDIE bit is a Global enable bit and must be enabled together with the other interrupts desired.

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REGISTER 27-8: CEPOLLCON: CRYPTO ENGINE POLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDPPLCON<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDPPLCON<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **BDPPLCON<15:0>:** Buffer Descriptor Processor Poll Control bits

These bits determine the number of cycles that the DMA transmit BDP would wait before refetching the descriptor control word if the previous descriptor fetched was disabled.

REGISTER 27-9: CEHDLEN: CRYPTO ENGINE HEADER LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HDRLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **HDRLEN<7:0>:** DMA Header Length bits

For every packet, skip this length of locations and start filling the data.

REGISTER 27-10: CETRLLEN: CRYPTO ENGINE TRAILER LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRLRLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **TRLRLEN<7:0>:** DMA Trailer Length bits

For every packet, skip this length of locations at the end of the current packet and start putting the next packet.

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27.2 Crypto Engine Buffer Descriptors

Host software creates a linked list of buffer descriptors and the hardware updates them. Table 27-3 provides a list of the Crypto Engine buffer descriptors, followed by format descriptions of each buffer descriptor (see Figure 27-2 through Figure 27-10).

TABLE 27-3: CRYPTO ENGINE BUFFER DESCRIPTORS

Name (see Note 1)		Bit 31/2315/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
BD_CTRL	31:24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
	23:16	—	SA_FETCH_EN	—	—	LAST_BD	LIFM	PKT_INT_EN	CBD_INT_EN
	15:8	BD_BUFLEN<15:8>							
	7:0	BD_BUFLEN<7:0>							
BD_SA_ADDR	31:24	BD_SAADDR<31:24>							
	23:16	BD_SAADDR<23:16>							
	15:8	BD_SAADDR<15:8>							
	7:0	BD_SAADR<7:0>							
BD_SCRADDR	31:24	BD_SRCADDR<31:24>							
	23:16	BD_SRCADDR<23:16>							
	15:8	BD_SRCADDR<15:8>							
	7:0	BD_SRCADDR<7:0>							
BD_DSTADDR	31:24	BD_DSTADDR<31:24>							
	23:16	BD_DSTADDR<23:16>							
	15:8	BD_DSTADDR<15:8>							
	7:0	BD_DSTADDR<7:0>							
BD_NXTPTR	31:24	BD_NXTADDR<31:24>							
	23:16	BD_NXTADDR<23:16>							
	15:8	BD_NXTADDR<15:8>							
	7:0	BD_NXTADDR<7:0>							
BD_UPDPTR	31:24	BD_UPDADDR<31:24>							
	23:16	BD_UPDADDR<23:16>							
	15:8	BD_UPDADDR<15:8>							
	7:0	BD_UPDADDR<7:0>							
BD_MSG_LEN	31:24	MSG_LENGTH<31:24>							
	23:16	MSG_LENGTH<23:16>							
	15:8	MSG_LENGTH<15:8>							
	7:0	MSG_LENGTH<7:0>							
BD_ENC_OFF	31:24	ENCR_OFFSET<31:24>							
	23:16	ENCR_OFFSET<23:16>							
	15:8	ENCR_OFFSET<15:8>							
	7:0	ENCR_OFFSET<7:0>							

Note 1: The buffer descriptor must be allocated in memory on a 64-bit boundary.

FIGURE 27-2: FORMAT OF BD_CTRL

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
23-16	—	SA_FETCH_EN	—	—	LAST_BD	LIFM	PKT_INT_EN	CBD_INT_EN
15-8	BD_BUFLEN<15:8>							
7-0	BD_BUFLEN<7:0>							

bit 31 **DESC_EN**: Descriptor Enable
`1` = The descriptor is owned by hardware. After processing the BD, hardware resets this bit to '`0`'.
`0` = The descriptor is owned by software

bit 30 **Unimplemented:** Must be written as '`0`'

bit 29-27 **CRY_MODE<2:0>:** Crypto Mode
`111` = Reserved
`110` = Reserved
`101` = Reserved
`100` = Reserved
`011` = CEK operation
`010` = KEK operation
`001` = Preboot authentication
`000` = Normal operation

bit 22 **SA_FETCH_EN:** Fetch Security Association From External Memory
`1` = Fetch SA from the SA pointer. This bit needs to be set to '`1`' for every new packet.
`0` = Use current fetched SA or the internal SA

bit 21-20 **Unimplemented:** Must be written as '`0`'

bit 19 **LAST_BD:** Last Buffer Descriptors
`1` = Last Buffer Descriptor in the chain
`0` = More Buffer Descriptors in the chain
After the last BD, the CEBDADDR goes to the base address in CEBDPADDR.

bit 18 **LIFM:** Last In Frame
In case of Receive Packets (from H/W-> Host), this field is filled by the Hardware to indicate whether the packet goes across multiple buffer descriptors. In case of transmit packets (from Host -> H/W), this field indicates whether this BD is the last in the frame.

bit 17 **PKT_INT_EN:** Packet Interrupt Enable
Generate an interrupt after processing the current buffer descriptor, if it is the end of the packet.

bit 16 **CBD_INT_EN:** CBD Interrupt Enable
Generate an interrupt after processing the current buffer descriptor.

bit 15-0 **BD_BUFLEN<15:0>:** Buffer Descriptor Length
This field contains the length of the buffer and is updated with the actual length filled by the receiver.

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FIGURE 27-3: FORMAT OF BD_SADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_SAADDR<31:24>							
23-16	BD_SAADDR<23:16>							
15-8	BD_SAADDR<15:8>							
7-0	BD_SAADDR<7:0>							

bit 31-0 **BD_SAADDR<31:0>:** Security Association IP Session Address
The sessions' SA pointer has the keys and IV values.

FIGURE 27-4: FORMAT OF BD_SADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_SAADDR<31:24>							
23-16	BD_SAADDR<23:16>							
15-8	BD_SAADDR<15:8>							
7-0	BD_SAADDR<7:0>							

bit 31-0 **BD_SAADDR<31:0>:** Security Association IP Session Address
The sessions' SA pointer has the keys and IV values.

FIGURE 27-5: FORMAT OF BD_SRCADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_SCRADDR<31:24>							
23-16	BD_SCRADDR<23:16>							
15-8	BD_SCRADDR<15:8>							
7-0	BD_SCRADDR<7:0>							

bit 31-0 **BD_SCRADDR:** Buffer Source Address
The source address of the buffer that needs to be passed through the PE-CRDMA for encryption or authentication. This address must be on a 32-bit boundary.

FIGURE 27-6: FORMAT OF BD_DSTADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_DSTADDR<31:24>							
23-16	BD_DSTADDR<23:16>							
15-8	BD_DSTADDR<15:8>							
7-0	BD_DSTADDR<7:0>							

bit 31-0 **BD_DSTADDR:** Buffer Destination Address
The destination address of the buffer that needs to be passed through the PE-CRDMA for encryption or authentication. This address must be on a 32-bit boundary.

FIGURE 27-7: FORMAT OF BD_NXTADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_NXTADDR<31:24>							
23-16	BD_NXTADDR<23:16>							
15-8	BD_NXTADDR<15:8>							
7-0	BD_NXTADDR<7:0>							

bit 31-0 **BD_NXTADDR:** Next BD Pointer Address Has Next Buffer Descriptor
The next buffer can be a next segment of the previous buffer or a new packet.

FIGURE 27-8: FORMAT OF BD_UPDPTR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_UPDADDR<31:24>							
23-16	BD_UPDADDR<23:16>							
15-8	BD_UPDADDR<15:8>							
7-0	BD_UPDADDR<7:0>							

bit 31-0 **BD_UPDADDR:** UPD Address Location
The update address has the location where the CRDMA results are posted. The updated results are the ICV values, key output values as needed.

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FIGURE 27-9: FORMAT OF BD_MSG_LEN

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	MSG_LENGTH<31:24>							
23-16	MSG_LENGTH<23:16>							
15-8	MSG_LENGTH<15:8>							
7-0	MSG_LENGTH<7:0>							

bit 31-0 **MSG_LENGTH:** Total Message Length

Total message length for the hash and HMAC algorithms in bytes. Total number of crypto bytes in case of GCM algorithm (LEN-C).

FIGURE 27-10: FORMAT OF BD_ENC_OFF

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	ENCR_OFFSET<31:24>							
23-16	ENCR_OFFSET<23:16>							
15-8	ENCR_OFFSET<15:8>							
7-0	ENCR_OFFSET<7:0>							

bit 31-0 **ENCR_OFFSET:** Encryption Offset

Encryption offset for the multi-task test cases (both encryption and authentication). The number of AAD bytes in the case of GCM algorithm (LEN-A).

27.3 Security Association Structure

Table 27-11 shows the Security Association Structure.

The Crypto Engine uses the Security Association to determine the settings for processing a Buffer Descriptor Processor. The Security Association contains the following features:

- Which algorithm to use
- Whether to use engines in parallel (for both authentication and encryption/decryption)
- The size of the key
- Authentication key
- Encryption/decryption key
- Authentication Initialization Vector (IV)
- Encryption IV

FIGURE 27-11: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_CTRL	31:24	—	—	VERIFY	—	NO_RX	OR_EN	ICVONLY	IRFLAG
	23:16	LNC	LOADIV	FB	FLAGS	—	—	—	ALGO<6>
	15:8	ALGO<5:0>						ENCTYPE	KEYSIZE<1>
	7:0	KEYSIZE<0>	MULTITASK<2:0>			CRYPTOALGO<3:0>			
SA_AUTHKEY1	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY2	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY3	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY4	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY5	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY6	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY7	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_AUTHKEY8	31:24	AUTHKEY<31:24>							
	23:16	AUTHKEY<23:16>							
	15:8	AUTHKEY<15:8>							
	7:0	AUTHKEY<7:0>							
SA_ENCKEY1	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							

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FIGURE 27-11: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_ENCKEY2	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY3	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY4	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY5	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY6	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY7	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_ENCKEY8	31:24	ENCKEY<31:24>							
	23:16	ENCKEY<23:16>							
	15:8	ENCKEY<15:8>							
	7:0	ENCKEY<7:0>							
SA_AUTHIV1	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV2	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV3	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV4	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV5	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV6	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV7	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							
	7:0	AUTHIV<7:0>							
SA_AUTHIV8	31:24	AUTHIV<31:24>							
	23:16	AUTHIV<23:16>							
	15:8	AUTHIV<15:8>							

FIGURE 27-11: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	7:0	AUTHIV<7:0>							

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FIGURE 27-11: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_ENCIV1	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV2	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV3	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV4	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							

Table 27-12 provides the Security Association control word structure.

The Crypto Engine fetches different structures for different flows and ensures that hardware fetches minimum words from SA required for processing. The structure is ready for hardware optimal data fetches.

FIGURE 27-12: FORMAT OF SA_CTRL

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	—	—	VERIFY	—	NO_RX	OR_EN	ICVONLY	IRFLAG
23-16	LNC	LOADIV	FB	FLAGS	—	—	—	ALGO<6>
15-8	ALGO<5:0>						ENC	KEY SIZE<1>
7-0	KEY SIZE<0>	MULTITASK<2:0>			CRYPTOALGO<3:0>			

bit 31-30 **Reserved:** Do not use

bit 29 **VERIFY:** NIST Procedure Verification Setting
1 = NIST procedures are to be used
0 = Do not use NIST procedures

bit 28 **Reserved:** Do not use

bit 27 **NO_RX:** Receive DMA Control Setting
1 = Only calculate ICV for authentication calculations
0 = Normal processing

bit 26 **OR_EN:** OR Register Bits Enable Setting
1 = OR the register bits with the internal value of the CSR register
0 = Normal processing

bit 25 **ICVONLY:** Incomplete Check Value Only Flag
This affects the SHA-1 algorithm only. It has no effect on the AES algorithm.
1 = Only three words of the HMAC result are available
0 = All results from the HMAC result are available

bit 24 **IRFLAG:** Immediate Result of Hash Setting
This bit is set when the immediate result for hashing is requested.
1 = Save the immediate result for hashing
0 = Do not save the immediate result

bit 23 **LNC:** Load New Keys Setting
1 = Load a new set of keys for encryption and authentication
0 = Do not load new keys

bit 22 **LOADIV:** Load IV Setting
1 = Load the IV from this Security Association
0 = Use the next IV

bit 21 **FB:** First Block Setting
This bit indicates that this is the first block of data to feed the IV value.
1 = Indicates this is the first block of data
0 = Indicates this is not the first block of data

bit 20 **FLAGS:** Incoming/Outgoing Flow Setting
1 = Security Association is associated with an outgoing flow
0 = Security Association is associated with an incoming flow

bit 19-17 **Reserved:** Do not use

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Figure 27-12: Format of SA_CTRL (Continued)

bit 16-10 **ALGO<6:0>:** Type of Algorithm to Use
`1xxxxxx` = HMAC 1
`x1xxxxx` = SHA-256
`xx1xxxx` = SHA1
`xxx1xxx` = MD5
`xxxx1xx` = AES
`xxxxx1x` = TDES
`xxxxxx1` = DES

bit 9 **ENC:** Type of Encryption Setting
`1` = Encryption
`0` = Decryption

bit 8-7 **KEYSIZE<1:0>:** Size of Keys in SA_AUTHKEYx or SA_ENCKEYx
`11` = Reserved; do not use
`10` = 256 bits
`01` = 192 bits
`00` = 128 bits(1)

bit 6-4 **MULTITASK<2:0>:** How to Combine Parallel Operations in the Crypto Engine
`111` = Parallel pass (decrypt and authenticate incoming data in parallel)
`101` = Pipe pass (encrypt the incoming data, and then perform authentication on the encrypted data)
`011` = Reserved
`010` = Reserved
`001` = Reserved
`000` = Encryption or authentication or decryption (no pass)

bit 3-0 **CRYPTOALGO<3:0>:** Mode of operation for the Crypto Algorithm
`1111` = Reserved
`1110` = AES_GCM (for AES processing)
`1101` = RCTR (for AES processing)
`1100` = RCBC_MAC (for AES processing)
`1011` = ROFB (for AES processing)
`1010` = RCFB (for AES processing)
`1001` = RCBC (for AES processing)
`1000` = REBC (for AES processing)
`0111` = TOFB (for Triple-DES processing)
`0110` = TCFB (for Triple-DES processing)
`0101` = TCBC (for Triple-DES processing)
`0100` = TECB (for Triple-DES processing)
`0011` = OFB (for DES processing)
`0010` = CFB (for DES processing)
`0001` = CBC (for DES processing)
`0000` = ECB (for DES processing)

Note 1: This setting does not alter the size of SA_AUTHKEYx or SA_ENCKEYx in the Security Association, only the number of bits of SA_AUTHKEYx and SA_ENCKEYx that are used.

NOTES:

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28.0 RANDOM NUMBER GENERATOR (RNG)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Random Number Generator (RNG) core implements a thermal noise-based, True Random Number Generator (TRNG) and a Pseudo-Random Number Generator (PRNG).

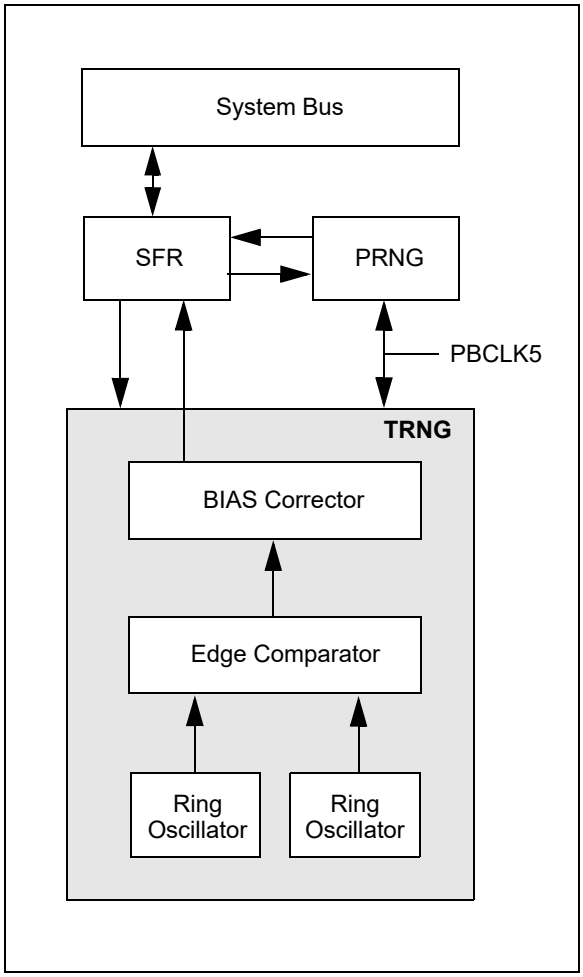
The TRNG uses multiple ring oscillators and the inherent thermal noise of integrated circuits to generate true random numbers that can initialize the PRNG.

The PRNG is a flexible LFSR, which is capable of manifesting a maximal length LFSR of up to 64-bits.

The following are key features of the Random Number Generator:

- TRNG:
  - Multi-Ring Oscillator based design
  - Built-in Bias Corrector
- PRNG:
  - LSFR-based
  - Up to 64-bit polynomial length
  - Programmable polynomial
  - TRNG can be seed value

FIGURE 28-1: RANDOM NUMBER GENERATOR BLOCK DIAGRAM



28.1 RNG Control Registers

TABLE 28-1: RANDOM NUMBER GENERATOR (RNG) REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6000	RNGVER	31:16	ID<15:0>																xxxx
		15:0	VERSION<7:0>								REVISION<7:0>								xxxx
6004	RNGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	LOAD	TRNGMODE	CONT	PRNGEN	TRNGEN	PLEN<7:0>								0064
6008	RNGPOLY1	31:16	POLY<31:0>																FFFF
		15:0																	0000
600C	RNGPOLY2	31:16	POLY<31:0>																FFFF
		15:0																	0000
6010	RNGNUMGEN1	31:16	RNG<31:0>																FFFF
		15:0																	FFFF
6014	RNGNUMGEN2	31:16	RNG<31:0>																FFFF
		15:0																	FFFF
6018	RNGSEED1	31:16	SEED<31:0>																0000
		15:0																	0000
601C	RNGSEED2	31:16	SEED<31:0>																0000
		15:0																	0000
6020	RNGCNT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RCNT<6:0>							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 28-1: RNGVER: RANDOM NUMBER GENERATOR VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-6 **ID<15:0>:** Block Identification bits

bit 15-8 **VERSION<7:0>:** Block Version bits

bit 7-0 **REVISION<7:0>:** Block Revision bits

REGISTER 28-2: RNGCON: RANDOM NUMBER GENERATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	LOAD	TRNGMODE(1)	CONT	PRNGEN	TRNGEN
7:0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	PLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12 **LOAD:** Device Select bit
This bit is self-clearing and is used to load the seed from the TRNG (i.e., the random value) as a seed to the PRNG.

bit 11 **TRNGMODE:** True Random Number Generator Mode bit(1)
1 = Enhanced TRNG mode is selected
0 = Normal TRNG mode is selected

bit 10 **CONT:** PRNG Number Shift Enable bit
1 = The PRNG random number is shifted every cycle
0 = The PRNG random number is shifted when the previous value is removed

bit 9 **PRNGEN:** PRNG Operation Enable bit
1 = PRNG operation is enabled
0 = PRNG operation is not enabled

bit 8 **TRNGEN:** TRNG Operation Enable bit
1 = TRNG operation is enabled
0 = TRNG operation is not enabled

bit 7-0 **PLEN<7:0>:** PRNG Polynomial Length bits
These bits contain the length of the polynomial used for the PRNG.

Note 1: This bit is effective only when the TRNGEN bit is set to ‘1’.

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REGISTER 28-3: RNGPOLYx: RANDOM NUMBER GENERATOR POLYNOMIAL REGISTER 'x' ('x' = 1 OR 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	POLY<31:24>							
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	POLY<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLY<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POLY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **POLY<31:0>:** PRNG LFSR Polynomial MSb/LSb bits (RNGPOLY1 = LSb, RNGPOLY2 = MSb)

REGISTER 28-4: RNGNUMGENx: RANDOM NUMBER GENERATOR REGISTER 'x' ('x' = 1 OR 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<31:24>							
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<23:16>							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<15:8>							
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RNG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **RNG<31:0>:** Current PRNG MSb/LSb Value bits (RNGNUMGEN1 = LSb, RNGNUMGEN2 = MSb)
Note: The RNGNUMGEN2 bit must be read before the RNGNUMGEN1 bit.

REGISTER 28-5: RNGSEEDx: TRUE RANDOM NUMBER GENERATOR SEED REGISTER 'x' ('x' = 1 OR 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SEED<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SEED<31:0>:** TRNG MSb/LSb Value bits (RNGSEED1 = LSb, RNGSEED2 = MSb)
Note: The RNGSEED2 bit must be read before the RNGSEED1 bit.

REGISTER 28-6: RNGCNT: TRUE RANDOM NUMBER GENERATOR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-7 **Unimplemented:** Read as '0'
bit 6-0 **RCNT<6:0>:** Number of Valid TRNG MSB 32 bits

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29.0 12-BIT HIGH-SPEED SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MZ DAK/DAL/DAR/DAS family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip website (www.microchip.com/PIC32).

The 12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) includes the following features:

- 12-bit resolution
- Six ADC modules with dedicated Sample and Hold (S&H) circuits
- Two dedicated ADC modules can be combined in Turbo mode to provide double conversion rate (clock sources for combined ADCs must be synchronous)
- Up to 45 analog input sources, in addition to the internal CTMU, VBAT, internal voltage reference and internal temperature sensor
- Single-ended and/or differential inputs
- Can operate during Sleep mode
- Supports touch sense applications
- Six digital comparators
- Six digital filters supporting two modes:
  - Oversampling mode
  - Averaging mode
- 16-word FIFO on ADC0 through ADC4 for increased throughput
- Early interrupt generation resulting in faster processing of converted data
- Designed for motor control, power conversion, and general purpose applications
- Operation during Sleep and Idle modes

A simplified block diagram of the ADC module is illustrated in Figure 29-1.

The 12-bit HS SAR ADC has up to five dedicated ADC modules (ADC0-ADC4) and one shared ADC module (ADC7). The dedicated ADC modules use a single input (or its alternate) and are intended for high-speed and precise sampling of time-sensitive or transient inputs. The the shared ADC module incorporates a multiplexer on the input to facilitate a larger group of inputs, with slower sampling, and provides flexible automated scanning option through the input scan logic.

For each ADC module, the analog inputs are connected to the S&H capacitor. The clock, sampling time, and output data resolution for each ADC module can be set independently. The ADC module performs the conversion of the input analog signal based on the configurations set in the registers. When conversion is complete, the final result is stored in the result buffer for the specific analog input and is passed to the digital filter and digital comparator if configured to use data from this particular sample. Input to ADCx mapping is illustrated in Figure 29-2.

29.1 Activation Sequence

Step 1: Initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00. Then, configure the AICPMPEN bit (ADCCON1<12> and the IOANCPEN bit (CFGCON<7>) = 1 if and only if VDD is less than 2.5V. The default is '0', which assumes VDD is greater than or equal to 2.5V.

Step 2: The user writes all the essential ADC configuration SFRs including the ADC control clock and all ADC core clocks setup:

- ADCCON1, keeping the ON bit = 0
- ADCCON2, especially paying attention to ADCDIV<6:0> and SAMC<9:0>
- ADCANCON, keeping all analog enables ANENx bit = 0, WKUPCLKCNT bit = 0xA
- ADCCON3, keeping all DIGEN5x = 0, especially paying attention to ADCSEL<1:0>, CONCLKDIV <5:0>, and VREFSEL<2:0>
- ADCxTIME, ADCDIVx<6:0>, and SAMCx<9:0>
- ADCTRGMODE, ADCIMCONx, ADCTRGSNS, ADCCSSx, ADCGIRQENx, ADCTRGx, ADCBASE
- Comparators, filters, and so on

Step 3: The user sets the ANENx bit to '1' for the ADC SAR Cores needed (which internally in the ADC module enables the control clock to generate by division the core clocks for the desired ADC SAR Cores, which in turn enables the bias circuitry for these ADC SAR Cores).

Step 4: The user sets the ON bit to '1', which enables the ADC control clock. The following ADCx activation sequence is to be followed at all times:

Step 5: The user waits for the interrupt/polls the BGVRRDY bit (ADCCON2<31>) and the WKRDYx bit (ADCANCON<15,13:8>) = 1, which signals that the device analog environment (band gap and VREF) is ready.

Step 6: Set the DIGENx bit (ADCCON3<15,13:8>) to '1', which enables the digital circuitry to immediately begin processing incoming triggers to perform data conversions.

Standard non-interleaved dedicated Class_1 ADCx throughput rate formula is shown in Equation 29-1.

EQUATION 29-1: THROUGHPUT RATE

ADC Throughput Rate = 1/((Sample time + Conversion time)(TAD))
= 1 / ((SAMC+# bit resolution+1)(TAD))

Example:
SAMC = 3 TAD, 12-bit mode, TAD = 20 ns = 50 MHz:
Throughput rate:
= 1 / ((3+13)(20 ns))
= 1/(16 * 20 ns)
= 3.125 msps

TABLE 29-1: PIC32MZXXDAXX INTERLEAVED ADC THROUGHPUT RATES

#No.of Interleaved ADC Possible	ADC TAD(min) = 20ns (50Mhz max)			
	12-bit (max.) msps	10-bit (max.) msps	8-bit (max.) msps	6-bit (max.) msps
1	3.125 msps	3.571 msps	4.167 msps	5.0 msps
2	6.250 msps	7.143 msps	8.333 msps	10.00 msps
3	8.330 msps	10.00 msps	12.50 msps	12.50 msps
4	12.50 msps	12.50 msps	16.667 msps	16.667 msps

Note: Interleaved ADCs in this context means connecting the same analog source signal to multiple dedicated Class_1 ADCs (i.e., ADC0-ADC5), and using independent staggered trigger sources accordingly for each interleaved ADC.

Note 1: Prior to enabling the ADC module, the user application must copy the ADC calibration data (DEVADC0-DEVADC4, DEVADC7; see Register 41-8) from the Configuration memory into the ADC Configuration registers (ADC0CFG-ADC4CFG, ADC7CFG).

2: If VDDIO is greater than 2.5V, set the AICPMPEN bit (ADCCON1<12>) and the IOANCPEN bit (CFGCON<7>) to '0'. If VDDIO is less than 2.5V, set both bits to '1'.

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FIGURE 29-1: ADC BLOCK DIAGRAM

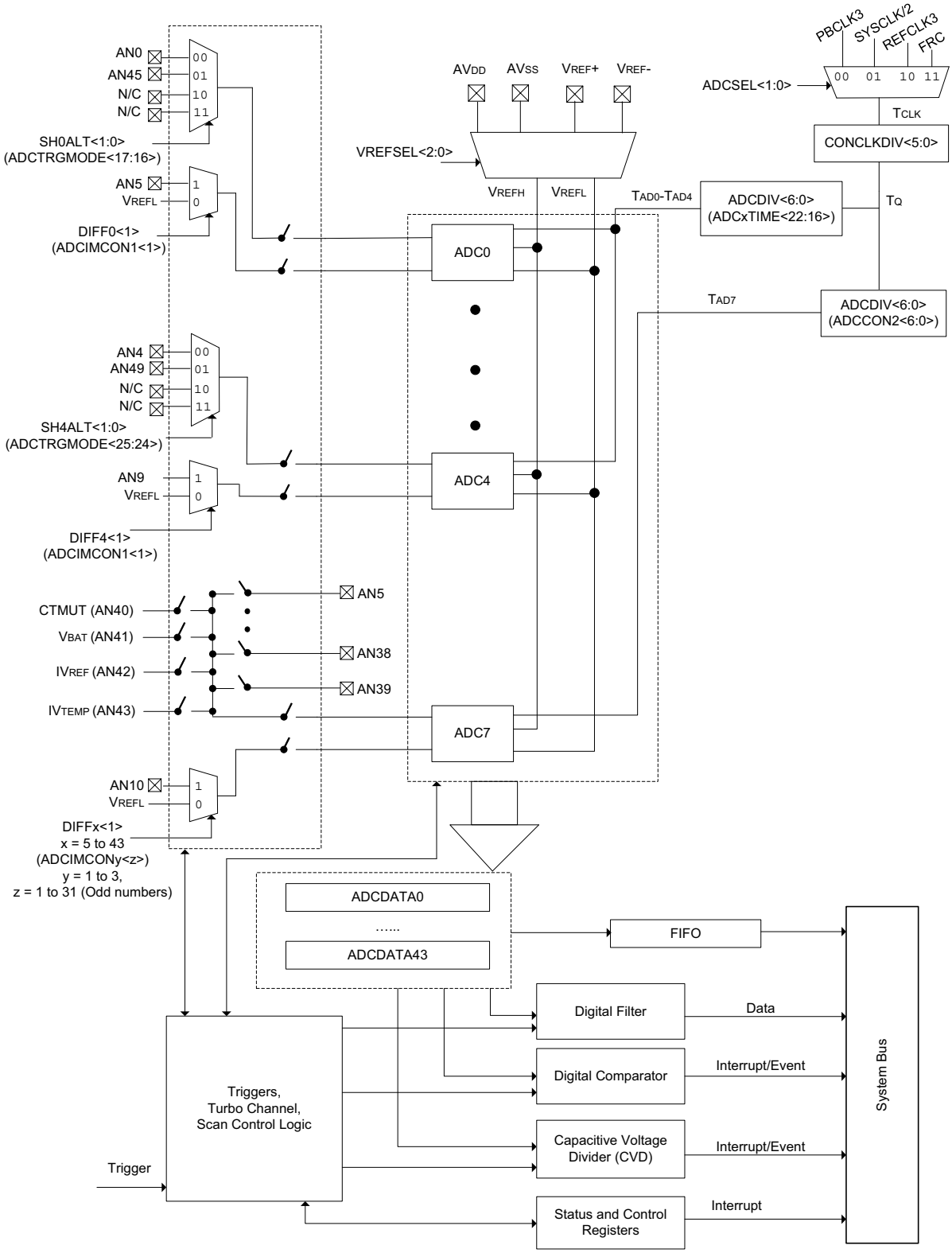

FIGURE 29-2: S&H BLOCK DIAGRAM

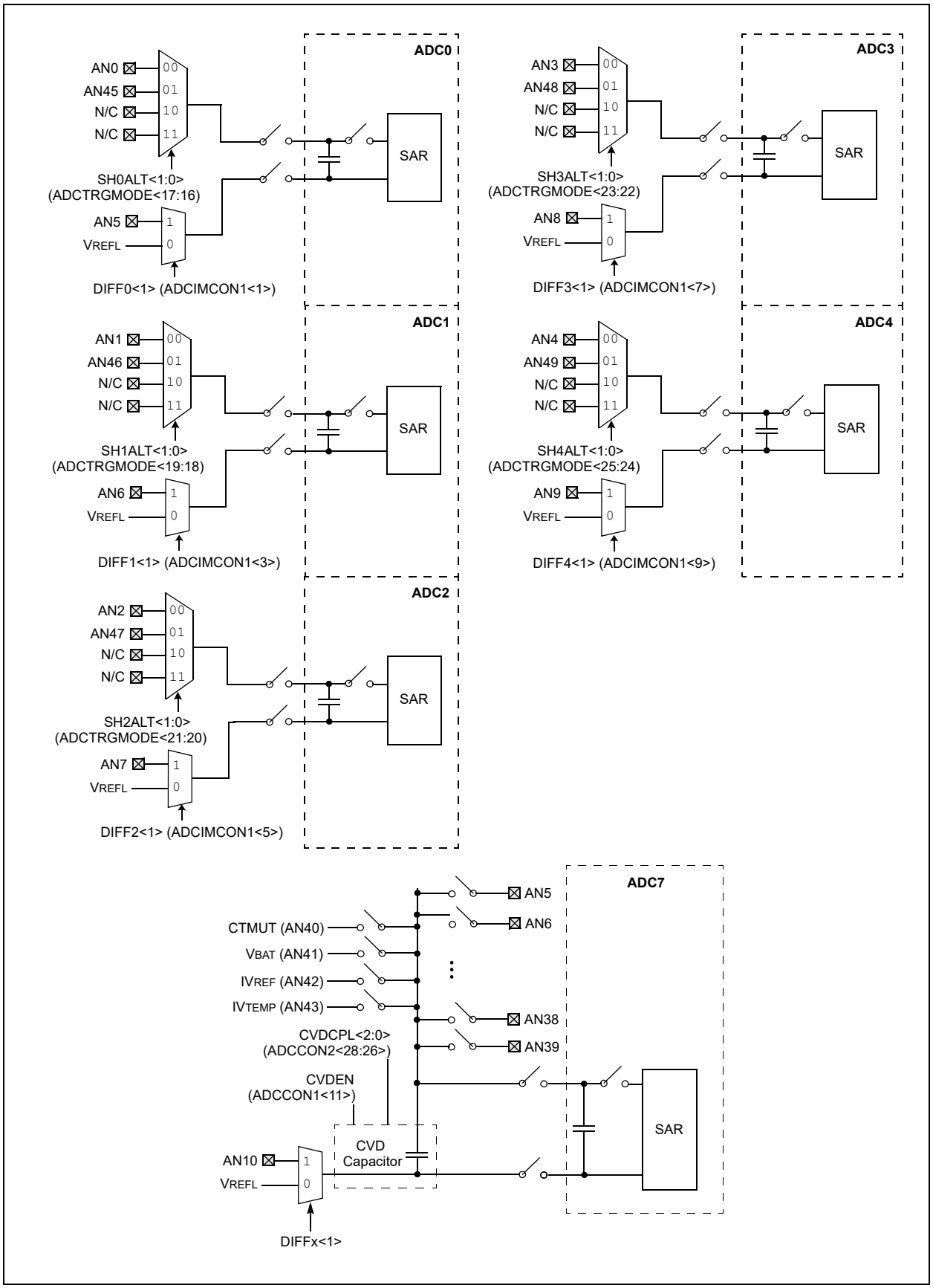

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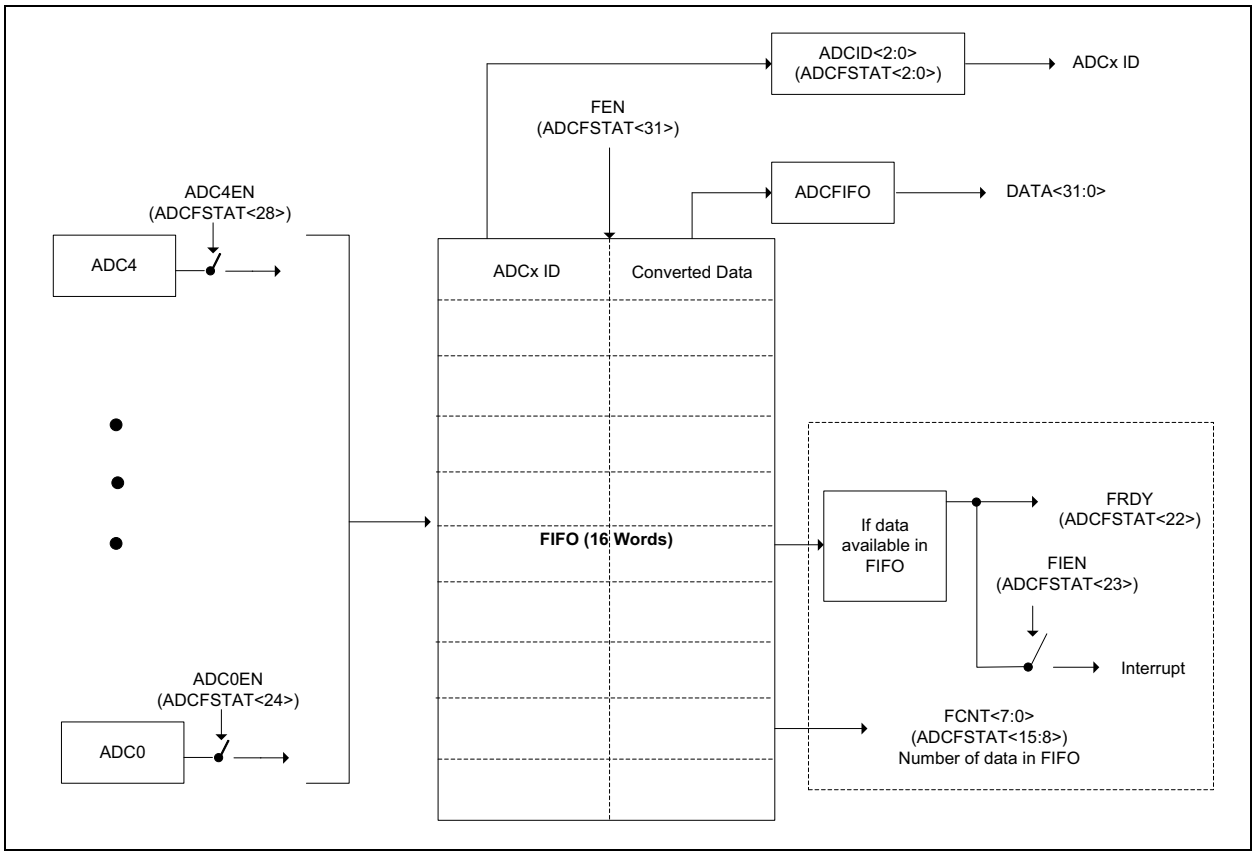
FIGURE 29-3: FIFO BLOCK DIAGRAM



29.2 ADC Control Registers

TABLE 29-2: ADC REGISTER MAP

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
B000	ADCCON1	31:16	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>			FRACT	SELRES<1:0>		STRGSRC<4:0>					0060
		15:0	ON	—	SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—	—	IRQVS<2:0>			STRGLVL	—	—	—	0000
B004	ADCCON2	31:16	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>			SAMC<9:0>										0000
		15:0	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>			—	ADCDIV<6:0>							0000
B008	ADCCON3	31:16	ADCSEL<1:0>		CONCLKDIV<5:0>						DIGEN7	—	—	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0	0000
		15:0	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT	GLSWTRG	GSWTRG	ADINSEL<5:0>						0000
B00C	ADCTRGMODE	31:16	—	—	—	—	—	—	SH4ALT<1:0>		SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>		0000
		15:0	—	—	—	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0	—	—	—	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0	0000
B010	ADCIMCON1	31:16	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8	0000
		15:0	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0	0000
B014	ADCIMCON2	31:16	DIFF31	SIGN31	DIFF30	SIGN30	DIFF29	SIGN29	DIFF28	SIGN28	DIFF27	SIGN27	DIFF26	SIGN26	DIFF25	SIGN25	DIFF24	SIGN24	0000
		15:0	DIFF23	SIGN23	DIFF22	SIGN22	DIFF21	SIGN21	DIFF20	SIGN20	DIFF19	SIGN19	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16	0000
B018	ADCIMCON3	31:16	—	—	—	—	—	—	—	—	DIFF43	SIGN43	DIFF42	SIGN42	DIFF41	SIGN41	DIFF40	SIGN40	0000
		15:0	DIFF39	SIGN39	DIFF38	SIGN38	DIFF37	SIGN37	DIFF36	SIGN36	DIFF35	SIGN35	DIFF34	SIGN34	DIFF33	SIGN33	DIFF32	SIGN32	0000
B020	ADCGIRQEN1	31:16	AGIEN31	AGIEN30	AGIEN29	AGIEN28	AGIEN27	AGIEN26	AGIEN25	AGIEN24	AGIEN23	AGIEN22	AGIEN21	AGIEN20	AGIEN19	AGIEN18	AGIEN17	AGIEN16	0000
		15:0	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0	0000
B024	ADCGIRQEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	AGIEN43	AGIEN42	AGIEN41	AGIEN40	AGIEN39	AGIEN38	AGIEN37	AGIEN36	AGIEN35	AGIEN34	AGIEN33	AGIEN32	0000
B028	ADCCSS1	31:16	CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25	CSS24	CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16	0000
		15:0	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
B02C	ADCCSS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	CSS43	CSS42	CSS41	CSS40	CSS39	CSS38	CSS37	CSS36	CSS35	CSS34	CSS33	CSS32	0000
B030	ADCDSTAT1	31:16	ARDY31	ARDY30	ARDY29	ARDY28	ARDY27	ARDY26	ARDY25	ARDY24	ARDY23	ARDY22	ARDY21	ARDY20	ARDY19	ARDY18	ARDY17	ARDY16	0000
		15:0	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0	0000
B034	ADCDSTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	ARDY43	ARDY42	ARDY41	ARDY40	ARDY39	ARDY38	ARDY37	ARDY36	ARDY35	ARDY34	ARDY33	ARDY32	0000
B038	ADCCMPEN1	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B03C	ADCCMP1	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B040	ADCCMPEN2	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B044	ADCCMP2	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B048	ADCCMPEN3	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

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TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
B04C	ADCCMP3	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B050	ADCCMPEN4	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B054	ADCCMP4	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B058	ADCCMPEN5	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B05C	ADCCMP5	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B060	ADCCMPEN6	31:16	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B064	ADCCMP6	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B068	ADCFLTR1	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B06C	ADCFLTR2	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B070	ADCFLTR3	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B074	ADCFLTR4	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B078	ADCFLTR5	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B07C	ADCFLTR6	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
B080	ADCTRG1	31:16	—	—	—	TRGSRC3<4:0>					—	—	—	TRGSRC2<4:0>					0000
		15:0	—	—	—	TRGSRC1<4:0>					—	—	—	TRGSRC0<4:0>					0000
B084	ADCTRG2	31:16	—	—	—	TRGSRC7<4:0>					—	—	—	TRGSRC6<4:0>					0000
		15:0	—	—	—	TRGSRC5<4:0>					—	—	—	TRGSRC4<4:0>					0000
B088	ADCTRG3	31:16	—	—	—	TRGSRC11<4:0>					—	—	—	TRGSRC10<4:0>					0000
		15:0	—	—	—	TRGSRC9<4:0>					—	—	—	TRGSRC8<4:0>					0000
B0A0	ADCCMPCON1	31:16	CVDDATA<15:0>																0000
		15:0	—	—	AINID<5:0>						ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0A4	ADCCMPCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0A8	ADCCMPCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

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TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
B0AC	ADCCMPCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B0	ADCCMPCON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B4	ADCCMPCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
B0B8	ADCFSTAT	31:16	FEN	—	—	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	FIEN	FRDY	FWROVERR	—	—	—	—	—	0000
		15:0	FCNT<7:0>								FSIGN	—	—	—	—	ADCID<2:0>			0000
B0BC	ADCFIFO	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B0C0	ADCBASE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADCBASE<15:0>																0000
B0D0	ADCTRGSNS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LVL11	LVL10	LVL9	LVL8	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0	0000
B0D4	ADC0TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0D8	ADC1TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0DC	ADC2TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0E0	ADC3TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0E4	ADC4TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		—	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
B0F0	ADCEIEN1	31:16	EIEN31	EIEN30	EIEN29	EIEN28	EIEN27	EIEN26	EIEN25	EIEN24	EIEN23	EIEN22	EIEN21	EIEN20	EIEN19	EIEN18	EIEN17	EIEN16	0000
		15:0	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0	0000
B0F4	ADCEIEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	EIEN43	EIEN42	EIEN41	EIEN40	EIEN39	EIEN38	EIEN37	EIEN36	EIEN35	EIEN34	EIEN33	EIEN32	0000
B0F8	ADCEISTAT1	31:16	EIRDY31	EIRDY30	EIRDY29	EIRDY28	EIRDY27	EIRDY26	EIRDY25	EIRDY24	EIRDY23	EIRDY22	EIRDY21	EIRDY20	EIRDY19	EIRDY18	EIRDY17	EIRDY16	0000
		15:0	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0	0000
B0FC	ADCEISTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	EIRDY43	EIRDY42	EIRDY41	EIRDY40	EIRDY39	EIRDY38	EIRDY37	EIRDY36	EIRDY35	EIRDY34	EIRDY33	EIRDY32	0000
B100	ADCANCON	31:16	—	—	—	—	WKUPCLKCNT<3:0>				WKIEN7	—	—	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0	0000
		15:0	WKRDY7	—	—	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0	ANEN7	—	—	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0	0000
B600	ADC0CFG(1)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B604	ADC1CFG1)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

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TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
B608	ADC2CFG[1)]	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B60C	ADC3CFG[1)]	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B610	ADC4CFG[1)]	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B61C	ADC7CFG[1)]	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
B640	ADCSYSCFG1	31:16	AN<31:16>																0000
		15:0	AN<15:0>																0000
B644	ADCSYSCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	AN<43:32>												0000
BA00	ADCDATA0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA04	ADCDATA1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA08	ADCDATA2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA0C	ADCDATA3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA10	ADCDATA4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA14	ADCDATA5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA18	ADCDATA6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA1C	ADCDATA7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA20	ADCDATA8	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA24	ADCDATA9	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA28	ADCDATA10	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA2C	ADCDATA11	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA30	ADCDATA12	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

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TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
BA34	ADCDATA13	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA38	ADCDATA14	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA3C	ADCDATA15	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA40	ADCDATA16	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA44	ADCDATA17	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA48	ADCDATA18	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA4C	ADCDATA19	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA50	ADCDATA20	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA54	ADCDATA21	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA58	ADCDATA22	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA5C	ADCDATA23	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA60	ADCDATA24	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA64	ADCDATA25	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA68	ADCDATA26	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA6C	ADCDATA27	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA70	ADCDATA28	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA74	ADCDATA29	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA78	ADCDATA30	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA7C	ADCDATA31	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

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TABLE 29-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
BA80	ADCDATA32	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA84	ADCDATA33	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA88	ADCDATA34	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA8C	ADCDATA35	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA90	ADCDATA36	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA94	ADCDATA37	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA98	ADCDATA38	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BA9C	ADCDATA39	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BAA0	ADCDATA40	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BAA4	ADCDATA41	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BAA8	ADCDATA42	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
BAAC	ADCDATA43	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

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REGISTER 29-1: ADCCON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>		
23:16	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRACT	SELRES<1:0>		STRGSRC<4:0>				
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	ON		SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	—	IRQVS<2:0>			STRGLVL	—	—	—

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **TRBEN:** Turbo Channel Enable bit
`1` = Enable the Turbo channel
`0` = Disable the Turbo channel

bit 30 **TRBERR:** Turbo Channel Error Status bit
`1` = An error occurred while setting the Turbo channel and Turbo channel function to be disabled regardless of the TRBEN bit being set to ‘`1`’.
`0` = Turbo channel error did not occur

Note: The status of this bit is valid only after the TRBEN bit is set.

bit 29-27 **TRBMST<2:0>:** Turbo Host ADCx bits
`111` = Reserved
`110` = ADC4 is selected as the Turbo Host
•
•
•
`000` = ADC0 is selected as the Turbo Host

bit 26-24 **TRBSLV<2:0>:** Turbo Client ADCx bits
`111` = Reserved
`110` = ADC4 is selected as the Turbo Client
•
•
•
`000` = ADC0 is selected as the Turbo Client

bit 23 **FRACT:** Fractional Data Output Format bit
`1` = Fractional
`0` = Integer

bit 22-21 **SELRES<1:0>:** Shared ADC (ADC7) Resolution bits
`11` = 12 bits (default)
`10` = 10 bits
`01` = 8 bits
`00` = 6 bits

Note: Changing the resolution of the ADC does not shift the result in the corresponding ADCDATAx register. The result will still occupy 12 bits with the corresponding lower unused bits set to ‘`0`’. For example, a resolution of 6 bits will result in ADCDATAx<5:0> being set to ‘`0`’, and ADCDATAx<11:6> holding the result.

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 “Output Compare”** and Figure 32-1 in **32.0 “Comparator”** for more information.

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REGISTER 29-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 20-16 **STRGSRC<4:0>:** Scan Trigger Source Select bits

11111 = Reserved
11110 = Reserved
11101 = CTMU Event
11100 = Reserved
.
.
.
01110 = Reserved
01101 = CTMU Event
01100 = Comparator 2 (C2OUT) (1)
01011 = Comparator 1 (C1OUT) (1)
01010 = OCMP5 (1)
01001 = OCMP3 (1)
01000 = OCMP1 (1)
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = Reserved
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge trigger (GSWTRG)
00000 = No Trigger

bit 15 **ON:** ADC Module Enable bit

1 = ADC module is enabled
0 = ADC module is disabled

Note: The ON bit should be set only after the ADC module has been configured.

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **AICPMPEN:** Analog Input Charge Pump Enable bit

1 = Analog input charge pump is enabled
0 = Analog input charge pump is disabled

Note 1: For proper analog operation at VDDIO less than 2.5V, the AICPMPEN bit and the IOANCPEN (CFGCON<7>) bit must be set to `1'. These bits should not be set if VDDIO is greater than 2.5V.

2: ADC throughput rate performance is reduced as defined in the table below if the AICPMPEN (ADCCON1<12>) bit and the IOANCPEN(CFGCON<7>) bit are set to '1'

ADC0	ADC1	ADC2	ADC3	ADC4	ADC7	Maximum combined
ON	OFF	OFF	OFF	OFF	OFF	2 MSPS
ON	ON	OFF	OFF	OFF	OFF	4 MSPS
ON	ON	ON	OFF	OFF	OFF	5 MSPS
OFF	OFF	OFF	ON	OFF	OFF	2 MSPS
OFF	OFF	OFF	ON	ON	OFF	4 MSPS
OFF	OFF	OFF	ON	ON	ON	5 MSPS
ON	ON	ON	ON	OFF	OFF	7 MSPS
ON	ON	ON	ON	ON	OFF	9 MSPS
ON	ON	ON	ON	ON	ON	10 MSPS

bit 11 **CVDEN:** Capacitive Voltage Division Enable bit

1 = CVD operation is enabled
0 = CVD operation is disabled

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 "Output Compare"** and Figure 32-1 in **32.0 "Comparator"** for more information.

REGISTER 29-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 10 **FSSCLKEN:** Fast Synchronous System Clock to ADC Control Clock bit

1 = Fast synchronous system clock to ADC control clock is enabled
0 = Fast synchronous system clock to ADC control clock is disabled

bit 9 **FSPBCLKEN:** Fast Synchronous Peripheral Clock to ADC Control Clock bit

1 = Fast synchronous peripheral clock to ADC control clock is enabled
0 = Fast synchronous peripheral clock to ADC control clock is disabled

bit 8-7 **Unimplemented:** Read as '0'

bit 6-4 **IRQVS<2:0>:** Interrupt Vector Shift bits

To determine interrupt vector address, this bit specifies the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with the ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

111 = Shift x left 7 bit position
110 = Shift x left 6 bit position
101 = Shift x left 5 bit position
100 = Shift x left 4 bit position
011 = Shift x left 3 bit position
010 = Shift x left 2 bit position
001 = Shift x left 1 bit position
000 = Shift x left 0 bit position

bit 3 **STRGLVL:** Scan Trigger High Level/Positive Edge Sensitivity bit

1 = Scan trigger is high level sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), the scan trigger will continue for all selected analog inputs, until the STRIG option is removed.
0 = Scan trigger is positive edge sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), only a single scan trigger will be generated, which will complete the scan of all selected analog inputs.

bit 2-0 **Unimplemented:** Read as '0'

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 "Output Compare"** and Figure 32-1 in **32.0 "Comparator"** for more information.

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REGISTER 29-2: ADCCON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>			SAMC<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	ADCDIV<6:0>						

Legend:	HC = Hardware Set	HS = Hardware Cleared	r = Reserved
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **BGVRRDY:** Band Gap Voltage/ADC Reference Voltage Status bit

1 = Both band gap voltage and ADC reference voltages (VREF) are ready
0 = Either or both band gap voltage and ADC reference voltages (VREF) are not ready

Data processing is valid only after BGVRRDY is set by hardware, so the application code must check that the BGVRRDY bit is set to ensure data validity. This bit set to ‘0’ when ON (ADCCON1<15>) = 0.

bit 30 **REFFLT:** Band Gap/VREF/AVDD BOR Fault Status bit

1 = Fault in band gap or the VREF voltage while the ON bit (ADCCON1<15>) was set. Most likely a band gap or VREF fault will be caused by a BOR of the analog VDDIO supply.
0 = Band gap and VREF voltage are working properly

This bit is cleared when the ON bit (ADCCON1<15>) = 0 and the BGVRRDY bit = 1.

bit 29 **EOSRDY:** End of Scan Interrupt Status bit

1 = All analog inputs are considered for scanning through the scan trigger (all analog inputs specified in the ADCCSS1 and ADCCSS2 registers) have completed scanning
0 = Scanning has not completed

This bit is cleared when ADCCON2<31:24> are read in software.

bit 28-26 **CVDCPL<2:0>:** Capacitor Voltage Divider (CVD) Setting bit

111 = 7 * 2.5 pF = 17.5 pF
110 = 6 * 2.5 pF = 15 pF
101 = 5 * 2.5 pF = 12.5 pF
100 = 4 * 2.5 pF = 10 pF
011 = 3 * 2.5 pF = 7.5 pF
010 = 2 * 2.5 pF = 5 pF
001 = 1 * 2.5 pF = 2.5 pF
000 = 0 * 2.5 pF = 0 pF

REGISTER 29-2: ADCCON2: ADC CONTROL REGISTER 2 (CONTINUED)

bit 25-16 **SAMC<9:0>:** Sample Time for the Shared ADC (ADC7) bits

1111111111 = 1025 T_{AD7}
•
•
•
0000000001 = 3 T_{AD7}
0000000000 = 2 T_{AD7}

Where T_{AD7} = period of the ADC conversion clock for the Shared ADC (ADC7) controlled by the ADCDIV<6:0> bits.

> **Note:** Unlike the high-speed Class 1 ADC modules, the trigger event for the shared Class-3 ADC7 module initiates the SAMC sampling sequence, rather than the convert sequence.
>
> Shared ADC7 Throughput rate:
>
> =((1/((Sample time + Conversion time) (T_{AD}))) / #of ADC inputs used in scan list)
>
> =((1/((SAMC + # bit resolution +1)(T_{AD}))) / #of ADC inputs used in scan list)
>
> For example:
>
> SCAN mode enabled with (2) ANx inputs in scan list (i.e., ADCCSSx<CSSY>), SAMC = 4
>
> T_{AD}, 12-bit mode, T_{AD} = 20ns = 50 MHz
>
> Throughput rate = ((1/ ((4+13)(20ns))) / 2)
>
> = ((1/ (17 * 20ns)) / 2)
>
> = 1,470588 msps

bit 15 **BGVRIEN:** Band Gap/V_{REF} Voltage Ready Interrupt Enable bit

1 = Interrupt will be generated when the BGVRDDY bit is set
0 = No interrupt is generated when the BGVRRDY bit is set

bit 14 **REFFLTIEN:** Band Gap/V_{REF} Voltage Fault Interrupt Enable bit

1 = Interrupt will be generated when the REFFLT bit is set
0 = No interrupt is generated when the REFFLT bit is set

bit 13 **EOSIEN:** End of Scan Interrupt Enable bit

1 = Interrupt will be generated when EOSRDY bit is set
0 = No interrupt is generated when the EOSRDY bit is set

bit 12 **ADCEIOVR:** Early Interrupt Request Override bit

1 = Early interrupt generation is not overridden and interrupt generation is controlled by the ADCEIEN1 and ADCEIEN2 registers
0 = Early interrupt generation is overridden and interrupt generation is controlled by the ADCGIRQEN1 and ADCGIRQEN2 registers

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **ADCEIS<2:0>:** Shared ADC (ADC7) Early Interrupt Select bits

These bits select the number of clocks (T_{AD7}) prior to the arrival of valid data that the associated interrupt is generated.

111 = The data ready interrupt is generated 8 ADC clocks prior to end of conversion
110 = The data ready interrupt is generated 7 ADC clocks prior to end of conversion
•
•
•
001 = The data ready interrupt is generated 2 ADC module clocks prior to end of conversion
000 = The data ready interrupt is generated 1 ADC module clock prior to end of conversion

> **Note:** All options are available when the selected resolution, set by the SELRES<1:0> bits (ADCCON1<22:21>), is 12-bit or 10-bit. For a selected resolution of 8-bit, options from '000' to '101' are valid. For a selected resolution of 6-bit, options from '000' to '011' are valid.

bit 7 **Unimplemented:** Read as '0'

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REGISTER 29-2: ADCCON2: ADC CONTROL REGISTER 2 (CONTINUED)

bit 6-0 **ADCDIV<6:0>:** Shared ADC (ADC7) Clock Divider bits

`1111111` = 254 * T_Q = T_{AD7}
•
•
•
`0000011` = 6 * T_Q = T_{AD7}
`0000010` = 4 * T_Q = T_{AD7}
`0000001` = 2 * T_Q = T_{AD7}
`0000000` = Reserved

The ADCDIV<6:0> bits divide the ADC control clock (T_Q) to generate the clock for the Shared ADC, ADC7 (T_{AD7}).

REGISTER 29-3: ADCCON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCSEL<1:0>		CONCLKDIV<5:0>					
23:16	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIGEN7	—	—	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R-0, HS, HC
	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP(1,2,3,4)	RQCNVRT
7:0	R/W-0	R/W, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GLSWTRG	GSWTRG	ADINSEL<5:0>					

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **ADCSEL<1:0>:** Analog-to-Digital Clock Source (TCLK) bits
11 = FRC
10 = REFCLK3
01 = System Clock (Tcy)
00 = PBCLK3

bit 29-24 **CONCLKDIV<5:0>:** Analog-to-Digital Control Clock (TQ) Divider bits
111111 = 64 * TCLK = TQ
•
•
•
000011 = 4 * TCLK = TQ
000010 = 3 * TCLK = TQ
000001 = 2 * TCLK = TQ
000000 = TCLK = TQ

bit 23 **DIGEN7:** Shared ADC (ADC7) Digital Enable bit
1 = ADC7 is digital enabled
0 = ADC7 is digital disabled

bit 22-21 **Unimplemented:** Read as ‘0’

bit 20 **DIGEN4:** ADC4 Digital Enable bit
1 = ADC4 is digital enabled
0 = ADC4 is digital disabled

bit 19 **DIGEN3:** ADC3 Digital Enable bit
1 = ADC3 is digital enabled
0 = ADC3 is digital disabled

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, using the SAMP bit will cause settings of the SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all the TRGSRCx<4:0> bits and the STRGSRC<4:0> bits should be set to ‘00000’ to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

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REGISTER 29-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 18 **DIGEN2:** ADC2 Digital Enable bit
1 = ADC2 is digital enabled
0 = ADC2 is digital disabled

bit 17 **DIGEN1:** ADC1 Digital Enable bit
1 = ADC1 is digital enabled
0 = ADC1 is digital disabled

bit 16 **DIGEN0:** ADC0 Digital Enable bit
1 = ADC0 is digital enabled
0 = ADC0 is digital disabled

bit 15-13 **VREFSEL<2:0>:** Voltage Reference (VREF) Input Selection bits

VREFSEL<2:0>	ADREF+	ADREF-
1xx	RESERVED: DO NOT USE	
011	EXTERNAL VREFH	EXTERNAL VREFL
010	AVDD	EXTERNAL VREFL
001	EXTERNAL VREFH	AVSS
000	AVDD	AVSS

bit 12 **TRGSUSP:** Trigger Suspend bit
1 = Triggers are blocked from starting a new analog-to-digital conversion, but the ADC module is not disabled
0 = Triggers are not blocked

bit 11 **UPDIEN:** Update Ready Interrupt Enable bit
1 = Interrupt will be generated when the UPDRDY bit is set by hardware
0 = No interrupt is generated

bit 10 **UPDRDY:** ADC Update Ready Status bit
1 = ADC SFRs can be updated
0 = ADC SFRs cannot be updated

Note: This bit is only active while the TRGSUSP bit is set and there are no more running conversions of any ADC modules.

bit 9 **SAMP:** Class 2 and Class 3 Analog Input Sampling Enable bit(1,2,3,4)
1 = The ADC S&H amplifier is sampling
0 = The ADC S&H amplifier is holding

bit 8 **RQCNVRT:** Individual ADC Input Conversion Request bit
This bit and its associated ADINSEL<5:0> bits enable the user to individually request an analog-to-digital conversion of an analog input through software.
1 = Trigger the conversion of the selected ADC input as specified by the ADINSEL<5:0> bits
0 = Do not trigger the conversion

Note: This bit is automatically cleared in the next ADC clock cycle.

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, using the SAMP bit will cause settings of the SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all the TRGSRCx<4:0> bits and the STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 29-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 7 **GLSWTRG:** Global Level Software Trigger bit

1 = Trigger conversion for ADC inputs that have selected the GLSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register

0 = Do not trigger an analog-to-digital conversion

bit 6 **GSWTRG:** Global Software Trigger bit

1 = Trigger conversion for ADC inputs that have selected the GSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register

0 = Do not trigger an analog-to-digital conversion

Note: This bit is automatically cleared in the next ADC clock cycle.

bit 5-0 **ADINSEL<5:0>:** Analog Input Select bits

These bits select the analog input to be converted when the RQCNVRT bit is set. As a general rule:

111111 = Reserved
•
•
•
101101 = Reserved
101100 = IVTEMP
101011 = IVREF
101010 = VBAT
101000 = CTMU
100111 = AN39
•
•
•
000001 = AN1
000000 = AN0

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, using the SAMP bit will cause settings of the SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all the TRGSRCx<4:0> bits and the STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

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REGISTER 29-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SH4ALT<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25-24 **SH4ALT<1:0>:** ADC4 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN49
- 00 = AN4

bit 23-22 **SH3ALT<1:0>:** ADC3 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN48
- 00 = AN3

bit 21-20 **SH2ALT<1:0>:** ADC2 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN47
- 00 = AN2

bit 19-18 **SH1ALT<1:0>:** ADC1 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN46
- 00 = AN1

bit 17-16 **SH0ALT<1:0>:** ADC0 Analog Input Select bit
- 11 = Reserved
- 10 = Reserved
- 01 = AN45
- 00 = AN0

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **STRGEN4:** ADC4 Presynchronized Triggers bit
- 1 = ADC4 uses presynchronized triggers
- 0 = ADC4 does not use presynchronized triggers

bit 11 **STRGEN3:** ADC3 Presynchronized Triggers bit
- 1 = ADC3 uses presynchronized triggers
- 0 = ADC3 does not use presynchronized triggers

bit 10 **STRGEN2:** ADC2 Presynchronized Triggers bit
- 1 = ADC2 uses presynchronized triggers
- 0 = ADC2 does not use presynchronized triggers

REGISTER 29-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

bit 9 **STRGEN1:** ADC1 Presynchronized Triggers bit
1 = ADC1 uses presynchronized triggers
0 = ADC1 does not use presynchronized triggers

bit 8 **STRGEN0:** ADC0 Presynchronized Triggers bit
1 = ADC0 uses presynchronized triggers
0 = ADC0 does not use presynchronized triggers

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **SSAMPEN4:** ADC4 Synchronous Sampling bit
1 = ADC4 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC4 does not use synchronous sampling

bit 3 **SSAMPEN3:** ADC3 Synchronous Sampling bit
1 = ADC3 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC3 does not use synchronous sampling

bit 2 **SSAMPEN2:** ADC2Synchronous Sampling bit
1 = ADC2 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC2 does not use synchronous sampling

bit 1 **SSAMPEN1:** ADC1 Synchronous Sampling bit
1 = ADC1 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC1 does not use synchronous sampling

bit 0 **SSAMPEN0:** ADC0 Synchronous Sampling bit
1 = ADC0 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC0 does not use synchronous sampling

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REGISTER 29-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **DIFF15:** AN15 Mode bit
1 = AN15 is using Differential mode
0 = AN15 is using Single-ended mode

bit 30 **SIGN:15** AN15 Signed Data Mode bit
1 = AN15 is using Signed Data mode
0 = AN15 is using Unsigned Data mode

bit 29 **DIFF14:** AN14 Mode bit
1 = AN14 is using Differential mode
0 = AN14 is using Single-ended mode

bit 28 **SIGN14:** AN14 Signed Data Mode bit
1 = AN14 is using Signed Data mode
0 = AN14 is using Unsigned Data mode

bit 27 **DIFF13:** AN13 Mode bit
1 = AN13 is using Differential mode
0 = AN13 is using Single-ended mode

bit 26 **SIGN13:** AN13 Signed Data Mode bit
1 = AN13 is using Signed Data mode
0 = AN13 is using Unsigned Data mode

bit 25 **DIFF12:** AN12 Mode bit
1 = AN12 is using Differential mode
0 = AN12 is using Single-ended mode

bit 24 **SIGN12:** AN12 Signed Data Mode bit
1 = AN12 is using Signed Data mode
0 = AN12 is using Unsigned Data mode

bit 23 **DIFF11:** AN11 Mode bit
1 = AN11 is using Differential mode
0 = AN11 is using Single-ended mode

bit 22 **SIGN11:** AN11 Signed Data Mode bit
1 = AN11 is using Signed Data mode
0 = AN11 is using Unsigned Data mode

bit 21 **DIFF10:** AN10 Mode bit
1 = AN10 is using Differential mode
0 = AN10 is using Single-ended mode

REGISTER 29-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 20 **SIGN10:** AN10 Signed Data Mode bit
1 = AN10 is using Signed Data mode
0 = AN10 is using Unsigned Data mode

bit 19 **DIFF9:** AN9 Mode bit
1 = AN9 is using Differential mode
0 = AN9 is using Single-ended mode

bit 18 **SIGN9:** AN9 Signed Data Mode bit
1 = AN9 is using Signed Data mode
0 = AN9 is using Unsigned Data mode

bit 17 **DIFF8:** AN 8 Mode bit
1 = AN8 is using Differential mode
0 = AN8 is using Single-ended mode

bit 16 **SIGN8:** AN8 Signed Data Mode bit
1 = AN8 is using Signed Data mode
0 = AN8 is using Unsigned Data mode

bit 15 **DIFF7:** AN7 Mode bit
1 = AN7 is using Differential mode
0 = AN7 is using Single-ended mode

bit 14 **SIGN7:** AN7 Signed Data Mode bit
1 = AN7 is using Signed Data mode
0 = AN7 is using Unsigned Data mode

bit 13 **DIFF6:** AN6 Mode bit
1 = AN6 is using Differential mode
0 = AN6 is using Single-ended mode

bit 12 **SIGN6:** AN6 Signed Data Mode bit
1 = AN6 is using Signed Data mode
0 = AN6 is using Unsigned Data mode

bit 11 **DIFF5:** AN5 Mode bit
1 = AN5 is using Differential mode
0 = AN5 is using Single-ended mode

bit 10 **SIGN5:** AN5 Signed Data Mode bit
1 = AN5 is using Signed Data mode
0 = AN5 is using Unsigned Data mode

bit 9 **DIFF4:** AN4 Mode bit
1 = AN4 is using Differential mode
0 = AN4 is using Single-ended mode

bit 8 **SIGN4:** AN4 Signed Data Mode bit
1 = AN4 is using Signed Data mode
0 = AN4 is using Unsigned Data mode

bit 7 **DIFF3:** AN3 Mode bit
1 = AN3 is using Differential mode
0 = AN3 is using Single-ended mode

bit 6 **SIGN3:** AN3 Signed Data Mode bit
1 = AN3 is using Signed Data mode
0 = AN3 is using Unsigned Data mode

bit 5 **DIFF2:** AN2 Mode bit
1 = AN2 is using Differential mode
0 = AN2 is using Single-ended mode

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REGISTER 29-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 4 **SIGN2:** AN2 Signed Data Mode bit
1 = AN2 is using Signed Data mode
0 = AN2 is using Unsigned Data mode

bit 3 **DIFF1:** AN1 Mode bit
1 = AN1 is using Differential mode
0 = AN1 is using Single-ended mode

bit 2 **SIGN1:** AN1 Signed Data Mode bit
1 = AN1 is using Signed Data mode
0 = AN1 is using Unsigned Data mode

bit 1 **DIFF0:** AN0 Mode bit
1 = AN0 is using Differential mode
0 = AN0 is using Single-ended mode

bit 0 **SIGN0:** AN0 Signed Data Mode bit
1 = AN0 is using Signed Data mode
0 = AN0 is using Unsigned Data mode

REGISTER 29-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF31	SIGN31	DIFF30	SIGN30	DIFF29	SIGN29	DIFF28	SIGN28
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF27	SIGN27	DIFF26	SIGN26	DIFF25	SIGN25	DIFF24	SIGN24
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF23	SIGN23	DIFF22	SIGN22	DIFF21	SIGN21	DIFF20	SIGN20
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF19	SIGN19	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **DIFF31:** AN31 Mode bit
1 = AN31 is using Differential mode
0 = AN31 is using Single-ended mode

bit 30 **SIGN31:** AN31 Signed Data Mode bit
1 = AN31 is using Signed Data mode
0 = AN31 is using Unsigned Data mode

bit 29 **DIFF30:** AN30 Mode bit
1 = AN30 is using Differential mode
0 = AN30 is using Single-ended mode

bit 28 **SIGN30:** AN30 Signed Data Mode bit
1 = AN30 is using Signed Data mode
0 = AN30 is using Unsigned Data mode

bit 27 **DIFF29:** AN29 Mode bit
1 = AN29 is using Differential mode
0 = AN29 is using Single-ended mode

bit 26 **SIGN29:** AN29 Signed Data Mode bit
1 = AN29 is using Signed Data mode
0 = AN29 is using Unsigned Data mode

bit 25 **DIFF28:** AN28 Mode bit
1 = AN28 is using Differential mode
0 = AN28 is using Single-ended mode

bit 24 **SIGN28:** AN28 Signed Data Mode bit
1 = AN28 is using Signed Data mode
0 = AN28 is using Unsigned Data mode

bit 23 **DIFF27:** AN27 Mode bit
1 = AN27 is using Differential mode
0 = AN27 is using Single-ended mode

bit 22 **SIGN27:** AN27 Signed Data Mode bit
1 = AN27 is using Signed Data mode
0 = AN27 is using Unsigned Data mode

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REGISTER 29-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2 (CONTINUED)

bit 21 **DIFF26:** AN26 Mode bit
1 = AN26 is using Differential mode
0 = AN26 is using Single-ended mode

bit 20 **SIGN26:** AN26 Signed Data Mode bit
1 = AN26 is using Signed Data mode
0 = AN26 is using Unsigned Data mode

bit 19 **DIFF25:** AN25 Mode bit
1 = AN25 is using Differential mode
0 = AN25 is using Single-ended mode

bit 18 **SIGN25:** AN25 Signed Data Mode bit
1 = AN25 is using Signed Data mode
0 = AN25 is using Unsigned Data mode

bit 17 **DIFF24:** AN24 Mode bit
1 = AN24 is using Differential mode
0 = AN24 is using Single-ended mode

bit 16 **SIGN24:** AN24 Signed Data Mode bit
1 = AN24 is using Signed Data mode
0 = AN24 is using Unsigned Data mode

bit 15 **DIFF23:** AN23 Mode bit
1 = AN23 is using Differential mode
0 = AN23 is using Single-ended mode

bit 14 **SIGN23:** AN23 Signed Data Mode bit
1 = AN23 is using Signed Data mode
0 = AN23 is using Unsigned Data mode

bit 13 **DIFF22:** AN22 Mode bit
1 = AN22 is using Differential mode
0 = AN22 is using Single-ended mode

bit 12 **SIGN22:** AN22 Signed Data Mode bit
1 = AN22 is using Signed Data mode
0 = AN22 is using Unsigned Data mode

bit 11 **DIFF21:** AN21 Mode bit
1 = AN21 is using Differential mode
0 = AN21 is using Single-ended mode

bit 10 **SIGN21:** AN21 Signed Data Mode bit
1 = AN21 is using Signed Data mode
0 = AN21 is using Unsigned Data mode

bit 9 **DIFF20:** AN20 Mode bit
1 = AN20 is using Differential mode
0 = AN20 is using Single-ended mode

bit 8 **SIGN20:** AN20 Signed Data Mode bit
1 = AN20 is using Signed Data mode
0 = AN20 is using Unsigned Data mode

bit 7 **DIFF19:** AN19 Mode bit
1 = AN19 is using Differential mode
0 = AN19 is using Single-ended mode

REGISTER 29-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2 (CONTINUED)

bit 6 **SIGN19:** AN19 Signed Data Mode bit
1 = AN19 is using Signed Data mode
0 = AN19 is using Unsigned Data mode

bit 5 **DIFF18:** AN18 Mode bit
1 = AN18 is using Differential mode
0 = AN18 is using Single-ended mode

bit 4 **SIGN18:** AN18 Signed Data Mode bit
1 = AN18 is using Signed Data mode
0 = AN18 is using Unsigned Data mode

bit 3 **DIFF17:** AN17 Mode bit
1 = AN17 is using Differential mode
0 = AN17 is using Single-ended mode

bit 2 **SIGN17:** AN17 Signed Data Mode bit
1 = AN17 is using Signed Data mode
0 = AN17 is using Unsigned Data mode

bit 1 **DIFF16:** AN16 Mode bit
1 = AN16 is using Differential mode
0 = AN16 is using Single-ended mode

bit 0 **SIGN16:** AN16 Signed Data Mode bit
1 = AN16 is using Signed Data mode
0 = AN16 is using Unsigned Data mode

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REGISTER 29-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF43	SIGN43	DIFF42	SIGN42	DIFF41	SIGN41	DIFF40	SIGN40
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF39	SIGN39	DIFF38	SIGN38	DIFF37	SIGN37	DIFF36	SIGN36
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF35	SIGN35	DIFF34	SIGN34	DIFF33	SIGN33	DIFF32	SIGN32

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23 **DIFF43:** AN43 Mode bit
1 = AN43 is using Differential mode
0 = AN43 is using Single-ended mode

bit 22 **SIGN43:** AN43 Signed Data Mode bit
1 = AN43 is using Signed Data mode
0 = AN43 is using Unsigned Data mode

bit 21 **DIFF42:** AN42 Mode bit
1 = AN42 is using Differential mode
0 = AN42 is using Single-ended mode

bit 20 **SIGN42:** AN42 Signed Data Mode bit
1 = AN42 is using Signed Data mode
0 = AN42 is using Unsigned Data mode

bit 19 **DIFF41:** AN41 Mode bit
1 = AN41 is using Differential mode
0 = AN41 is using Single-ended mode

bit 18 **SIGN41:** AN41 Signed Data Mode bit
1 = AN41 is using Signed Data mode
0 = AN41 is using Unsigned Data mode

bit 17 **DIFF40:** AN40 Mode bit
1 = AN40 is using Differential mode
0 = AN40 is using Single-ended mode

bit 16 **SIGN40:** AN40 Signed Data Mode bit
1 = AN40 is using Signed Data mode
0 = AN40 is using Unsigned Data mode

bit 15 **DIFF39:** AN39 Mode bit
1 = AN39 is using Differential mode
0 = AN39 is using Single-ended mode

bit 14 **SIGN39:** AN39 Signed Data Mode bit
1 = AN39 is using Signed Data mode
0 = AN39 is using Unsigned Data mode

REGISTER 29-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3 (CONTINUED)

bit 13 **DIFF38:** AN38 Mode bit
1 = AN38 is using Differential mode
0 = AN38 is using Single-ended mode

bit 12 **SIGN38:** AN38 Signed Data Mode bit
1 = AN38 is using Signed Data mode
0 = AN38 is using Unsigned Data mode

bit 11 **DIFF37:** AN37 Mode bit
1 = AN37 is using Differential mode
0 = AN37 is using Single-ended mode

bit 10 **SIGN37:** AN37 Signed Data Mode bit
1 = AN37 is using Signed Data mode
0 = AN37 is using Unsigned Data mode

bit 9 **DIFF36:** AN36 Mode bit
1 = AN36 is using Differential mode
0 = AN36 is using Single-ended mode

bit 8 **SIGN36:** AN36 Signed Data Mode bit
1 = AN36 is using Signed Data mode
0 = AN36 is using Unsigned Data mode

bit 7 **DIFF35:** AN35 Mode bit
1 = AN35 is using Differential mode
0 = AN35 is using Single-ended mode

bit 6 **SIGN35:** AN35 Signed Data Mode bit
1 = AN35 is using Signed Data mode
0 = AN35 is using Unsigned Data mode

bit 5 **DIFF34:** AN34 Mode bit
1 = AN34 is using Differential mode
0 = AN34 is using Single-ended mode

bit 4 **SIGN34:** AN34 Signed Data Mode bit
1 = AN34 is using Signed Data mode
0 = AN34 is using Unsigned Data mode

bit 3 **DIFF33:** AN33 Mode bit
1 = AN33 is using Differential mode
0 = AN33 is using Single-ended mode

bit 2 **SIGN33:** AN33 Signed Data Mode bit
1 = AN33 is using Signed Data mode
0 = AN33 is using Unsigned Data mode

bit 1 **DIFF32:** AN32 Mode bit
1 = AN32 is using Differential mode
0 = AN32 is using Single-ended mode

bit 0 **SIGN32:** AN32 Signed Data Mode bit
1 = AN32 is using Signed Data mode
0 = AN32 is using Unsigned Data mode

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REGISTER 29-8: ADCGIRQEN1: ADC GLOBAL INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN31	AGIEN30	AGIEN29	AGIEN28	AGIEN27	AGIEN26	AGIEN25	AGIEN24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN23	AGIEN22	AGIEN21	AGIEN20	AGIEN19	AGIEN18	AGIEN17	AGIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **AGIEN31:AGIEN0:** ADC Global Interrupt Enable bits

1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the ARDY*x* bit (‘*x*’ = 31-0) of the ADCDSTAT1 register)

0 = Interrupts are disabled

REGISTER 29-9: ADCGIRQEN2: ADC GLOBAL INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AGIEN43	AGIEN42	AGIEN41	AGIEN40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN39	AGIEN38	AGIEN37	AGIEN36	AGIEN35	AGIEN34	AGIEN33	AGIEN32

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11-0 **AGIEN43:AGIEN32** ADC Global Interrupt Enable bits

1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the ARDY*x* bit (‘*x*’ = 43-32) of the ADCDSTAT2 register)

0 = Interrupts are disabled

REGISTER 29-10: ADCCSS1: ADC COMMON SCAN SELECT REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25	CSS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CSS31:CSS0:** Analog Common Scan Select bits
`1` = Select AN*x* for input scan
`0` = Skip AN*x* for input scan

Note 1: In addition to setting the appropriate bits in this register, Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSS*x* bits. Refer to the bit descriptions in the ADCTRGx registers for selecting the STRIG option.

2: If a Class 1 or Class 2 input is included in the scan by setting the CSSx bit to ‘`1`’ and by setting the TRGSRCx<4:0> bits to STRIG mode (`'0b11`), the user application must ensure that no other triggers are generated for that input using the RQCNVRT bit in the ADCCON3 register or the hardware input or any digital filter. Otherwise, the scan behavior is unpredictable.

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REGISTER 29-11: ADCCSS2: ADC COMMON SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CSS43	CSS42	CSS41	CSS40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS39	CSS38	CSS37	CSS36	CSS35	CSS34	CSS33	CSS32

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11-0 **CSS43:CSS32:** Analog Common Scan Select bits
Analog inputs 43 to 32 are always Class 3, as there are only 32 triggers available.
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

REGISTER 29-12: ADCDSTAT1: ADC DATA READY STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY31	ARDY30	ARDY29	ARDY28	ARDY27	ARDY26	ARDY25	ARDY24
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY23	ARDY22	ARDY21	ARDY20	ARDY19	ARDY18	ARDY17	ARDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **ARDY31:ARDY0:** Conversion Data Ready for Corresponding Analog Input Ready bits
1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

REGISTER 29-13: ADCDSTAT2: ADC DATA READY STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	ARDY43	ARDY42	ARDY41	ARDY40
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ARDY39	ARDY38	ARDY37	ARDY36	ARDY35	ARDY34	ARDY33	ARDY32

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’
bit 11-0 **ARDY43:ARDY32:** Conversion Data Ready for Corresponding Analog Input Ready bits
1 = This bit is set when converted data is ready in the data register
0 = This bit is cleared when the associated data register is read

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REGISTER 29-14: ADCCMPENx: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER ('x' = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE31	CMPE30	CMPE29	CMPE28	CMPE27	CMPE26	CMPE25	CMPE24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE23	CMPE22	CMPE21	CMPE20	CMPE19	CMPE18	CMPE17	CMPE16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CMPE31:CMPE0:** ADC Digital Comparator '*x*' Enable bits

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: CMPE*x* = AN*x*, where '*x*' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).

2: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = `1`) can result in unpredictable behavior.

REGISTER 29-15: ADCCMPx: ADC DIGITAL COMPARATOR 'x' LIMIT VALUE REGISTER ('x' = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<15:8>(1,2,3)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<7:0>(1,2,3)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<15:8>(1,2,3)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<7:0>(1,2,3)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DCMPHI<15:0>:** Digital Comparator '*x*' High Limit Value bits(1,2,3)
These bits store the high limit value, which is used by digital comparator for comparisons with ADC converted data.

bit 15-0 **DCMPLO<15:0>:** Digital Comparator '*x*' Low Limit Value bits(1,2,3)
These bits store the low limit value, which is used by digital comparator for comparisons with ADC converted data.

Note 1: Changing theses bits while the Digital Comparator is enabled (ENDCMP = `1`) can result in unpredictable behavior.

2: The format of the limit values should match the format of the ADC converted value in terms of sign and fractional settings.

3: For Digital Comparator 0 used in CVD mode, the DCMPHI<15:0> and DCMPLO<15:0> bits must always be specified in signed format, as the CVD output data is differential and is always signed.

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REGISTER 29-16: ADCFLTRx: ADC DIGITAL FILTER ‘x’ REGISTER (‘x’ = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC
	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CHNLID<4:0>				
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	FLTRDATA<15:8>							
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	FLTRDATA<7:0>							

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **AFEN:** Digital Filter ‘*x*’ Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled and the AFRDY status bit is cleared

Note: If the ADCFLTRx<AFEN> = 1 then the ADCxTIME<SAMC> minimum must be ≥ to 0x004 or equivalent to ≥ 6 TADx. This will correspondingly reduce the maximum sampling rate possible.

bit 30 **DATA16EN:** Filter Significant Data Length bit
1 = All 16 bits of the filter output data are significant
0 = Only the first 12 bits are significant, followed by four zeros

Note: This bit is significant only if the DFMODE = 1 (Averaging Mode) and the FRACT (ADCCON1<23>) = 1 (Fractional Output Mode).

bit **DFMODE:** ADC Filter Mode bit
1 = Filter ‘*x*’ works in Averaging mode
0 = Filter ‘*x*’ works in Oversampling Filter mode (default)

bit 28-26 **OVRSAM<2:0>:** Oversampling Filter Ratio bits
If DFMODE is ‘0’:
111 = 128 samples (shift sum 3 bits to right, output data is in 15.1 format)
110 = 32 samples (shift sum 2 bits to right, output data is in 14.1 format)
101 = 8 samples (shift sum 1 bit to right, output data is in 13.1 format)
100 = 2 samples (shift sum 0 bits to right, output data is in 12.1 format)
011 = 256 samples (shift sum 4 bits to right, output data is 16 bits)
010 = 64 samples (shift sum 3 bits to right, output data is 15 bits)
001 = 16 samples (shift sum 2 bits to right, output data is 14 bits)
000 = 4 samples (shift sum 1 bit to right, output data is 13 bits)

If DFMODE is ‘1’:
111 = 256 samples (256 samples to be averaged)
110 = 128 samples (128 samples to be averaged)
101 = 64 samples (64 samples to be averaged)
100 = 32 samples (32 samples to be averaged)
011 = 16 samples (16 samples to be averaged)
010 = 8 samples (8 samples to be averaged)
001 = 4 samples (4 samples to be averaged)
000 = 2 samples (2 samples to be averaged)

bit 25 **AFGIEN:** Digital Filter ‘*x*’ Interrupt Enable bit
1 = Digital filter interrupt is enabled and is generated by the AFRDY status bit
0 = Digital filter is disabled

REGISTER 29-16: ADCFLTRx: ADC DIGITAL FILTER 'x' REGISTER ('x' = 1 THROUGH 6)

bit 24 **AFRDY:** Digital Filter '*x*' Data Ready Status bit
1 = Data is ready in the FLTRDATA<15:0> bits
0 = Data is not ready

Note: This bit is cleared by reading the FLTRDATA<15:0> bits or by disabling the Digital Filter module (by setting AFEN to '0').

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **CHNLID<4:0>:** Digital Filter Analog Input Selection bits
These bits specify the analog input to be used as the oversampling filter data source.
11111 = Reserved
•
•
•
01100 = Reserved
01011 = AN11
•
•
•
00001 = AN1
00000 = AN0

Note: Only the first 12 analog inputs, Class 1 (AN0-AN11) and Class 2 (AN5-AN11), can use a digital filter.

bit 15-0 **FLTRDATA<15:0>:** Digital Filter '*x*' Data Output Value bits
The filter output data is as per the fractional format set in the FRACT bit (ADCCON1<23>). The FRACT bit should not be changed while the filter is enabled. Changing the state of the FRACT bit after the operation of the filter ended will not update the value of the FLTRDATA<15:0> bits to reflect the new format.

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REGISTER 29-17: ADCTRG1: ADC TRIGGER SOURCE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC3<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC2<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC1<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-24 **TRGSRC3<4:0>:** Trigger Source for Conversion of Analog Input AN3 Select bits
11111 = Reserved
11110 = Reserved
11101 = CTMU Event
11100 = Reserved
•
•
•
01110 = Reserved
01101 = CTMU Event
01100 = Comparator 2 (C2OUT) (1)
01011 = Comparator 1 (C1OUT) (1)
01010 = OCMP5 (1)
01001 = OCMP3 (1)
01000 = OCMP1 (1)
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-16 **TRGSRC2<4:0>:** Trigger Source for Conversion of Analog Input AN2 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **TRGSRC1<4:0>:** Trigger Source for Conversion of Analog Input AN1 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **TRGSRC0<4:0>:** Trigger Source for Conversion of Analog Input AN0 Select bits
See bits 28-24 for bit value definitions.

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 “Output Compare”** and Figure 32-1 in **32.0 “Comparator”** for more information.

REGISTER 29-18: ADCTRG2: ADC TRIGGER SOURCE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC7<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC6<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC5<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC4<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-24 **TRGSRC7<4:0>:** Trigger Source for Conversion of Analog Input AN7 Select bits
11111 = Reserved
11110 = Reserved
11101 = CTMU Event
11100 = Reserved
•
•
•
01110 = Reserved
01101 = CTMU Event
01100 = Comparator 2 (C2OUT) (1)
01011 = Comparator 1 (C1OUT) (1)
01010 = OCMP5 (1)
01001 = OCMP3 (1)
01000 = OCMP1 (1)
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-16 **TRGSRC6<4:0>:** Trigger Source for Conversion of Analog Input AN6 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **TRGSRC5<4:0>:** Trigger Source for Conversion of Analog Input AN5 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **TRGSRC4<4:0>:** Trigger Source for Conversion of Analog Input AN4 Select bits
See bits 28-24 for bit value definitions.

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 “Output Compare”** and Figure 32-1 in **32.0 “Comparator”** for more information.

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REGISTER 29-19: ADCTRG3: ADC TRIGGER SOURCE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC11<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC10<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC9<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC8<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-24 **TRGSRC11<4:0>:** Trigger Source for Conversion of Analog Input AN11 Select bits
11111 = Reserved
11110 = Reserved
11101 = CTMU Event
11100 = Reserved
.
.
.
01110 = Reserved
01101 = CTMU Event
01100 = Comparator 2 (C2OUT) (1)
01011 = Comparator 1 (C1OUT) (1)
01010 = OCMP5 (1)
01001 = OCMP3 (1)
01000 = OCMP1 (1)
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-16 **TRGSRC10<4:0>:** Trigger Source for Conversion of Analog Input AN10 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **TRGSRC9<4:0>:** Trigger Source for Conversion of Analog Input AN9 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **TRGSRC8<4:0>:** Trigger Source for Conversion of Analog Input AN8 Select bits
See bits 28-24 for bit value definitions.

Note 1: The rising edge of the module output signal triggers an ADC conversion. See Figure 16-1 in **16.0 “Output Compare”** and Figure 32-1 in **32.0 “Comparator”** for more information.

REGISTER 29-20: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	CVDDATA<15:8>							
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	CVDDATA<7:0>							
15:8	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	AINID<5:0>					
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **CVDDATA<15:0>:** CVD Data Status bits
In CVD mode, these bits obtain the CVD differential output data (subtraction of CVD positive and negative measurement), whenever a Digital Comparator interrupt is generated. The value in these bits is compliant with the FRACT bit (ADCCON1<23>) and is always signed.

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **AINID<5:0>:** Digital Comparator 0 Analog Input Identification (ID) bits
When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by Digital Comparator 0.

Note: In normal ADC mode, only analog inputs <31:0> can be processed by the Digital Comparator 0. The Digital Comparator 0 also supports the CVD mode, in which all Class 2 and Class 3 analog inputs may be stored in the AINID<5:0> bits.

111111 = Reserved
.
.
.
101100 = Reserved
101011 = AN43 is being monitored
.
.
.
000001 = AN1 is being monitored
000000 = AN0 is being monitored

bit 7 **ENDCMP:** Digital Comparator 0 Enable bit
1 = Digital Comparator 0 is enabled
0 = Digital Comparator 0 is not enabled, and the DCMPED status bit (ADCCMP0CON<5>) is cleared

bit 6 **DCMPGIEN:** Digital Comparator 0 Global Interrupt Enable bit
1 = A Digital Comparator 0 interrupt is generated when the DCMPED status bit (ADCCMP0CON<5>) is set
0 = A Digital Comparator 0 interrupt is disabled

bit 5 **DCMPED:** Digital Comparator 0 “Output True” Event Status bit
The logical conditions under which the digital comparator gets “True” are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI, and IELOLO bits.

Note: This bit is cleared by reading the AINID<5:0> bits or by disabling the Digital Comparator module (by setting ENDCMP to ‘0’).

1 = Digital Comparator 0 output true event has occurred (output of Comparator is ‘1’)
0 = Digital Comparator 0 output is false (output of comparator is ‘0’)

bit 4 **IEBTWN:** Between Low/High Digital Comparator 0 Event bit
1 = Generate a digital comparator event when DCMPLO<15:0> ≤ DATA<31:0> < DCMPHI<15:0>
0 = Do not generate a digital comparator event

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REGISTER 29-20: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

bit 3 **IEHIHI:** High/High Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when DCMPHI<15:0> ≤ DATA<31:0>
0 = Do not generate an event

bit 2 **IEHILO:** High/Low Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when DATA<31:0> < DCMPHI<15:0>
0 = Do not generate an event

bit 1 **IELOHI:** Low/High Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when DCMPLO<15:0> ≤ DATA<31:0>
0 = Do not generate an event

bit 0 **IELOLO:** Low/Low Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when DATA<31:0> < DCMPLO<15:0>
0 = Do not generate an event

REGISTER 29-21: ADCCMPCONx: ADC DIGITAL COMPARATOR 'x' CONTROL REGISTER ('x' = 2 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	AINID<4:0>				
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **AINID<4:0>:** Digital Comparator '*x*' Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by the Digital Comparator.

Note: Only analog inputs <31:0> can be processed by the Digital Comparator module '*x*' ('*x*' = 1-5).

11111 = AN31 is being monitored
11110 = AN30 is being monitored
•
•
•
00001 = AN1 is being monitored
00000 = AN0 is being monitored

bit 7 **ENDCMP:** Digital Comparator '*x*' Enable bit

1 = Digital Comparator '*x*' is enabled
0 = Digital Comparator '*x*' is not enabled, and the DCMPED status bit (ADCCMP*x*CON<5>) is cleared

bit 6 **DCMPGIEN:** Digital Comparator '*x*' Global Interrupt Enable bit

1 = A Digital Comparator '*x*' interrupt is generated when the DCMPED status bit (ADCCMP*x*CON<5>) is set
0 = A Digital Comparator '*x*' interrupt is disabled

bit 5 **DCMPED:** Digital Comparator '*x*' "Output True" Event Status bit

The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI and IELOLO bits.

Note: This bit is cleared by reading the AINID<5:0> bits (ADCCMP0CON<13:8>) or by disabling the Digital Comparator module (by setting ENDCMP to '0').

1 = Digital Comparator '*x*' output true event has occurred (output of Comparator is '1')
0 = Digital Comparator '*x*' output is false (output of Comparator is '0')

bit 4 **IEBTWN:** Between Low/High Digital Comparator '*x*' Event bit

1 = Generate a digital comparator event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate a digital comparator event

bit 3 **IEHIHI:** High/High Digital Comparator '*x*' Event bit

1 = Generate a Digital Comparator '*x*' Event when the DCMPHI<15:0> bits ≤ DATA<31:0> bits
0 = Do not generate an event

bit 2 **IEHILO:** High/Low Digital Comparator '*x*' Event bit

1 = Generate a Digital Comparator '*x*' Event when the DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate an event

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REGISTER 29-21: ADCCMPCONx: ADC DIGITAL COMPARATOR ‘x’ CONTROL REGISTER (‘x’ = 2 THROUGH 6) (CONTINUED)

bit 1 **IELOHI:** Low/High Digital Comparator ‘*x*’ Event bit

1 = Generate a Digital Comparator ‘*x*’ Event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits
0 = Do not generate an event

bit 0 **IELOLO:** Low/Low Digital Comparator ‘*x*’ Event bit

1 = Generate a Digital Comparator ‘*x*’ Event when the DATA<31:0> bits < DCMPLO<15:0> bits
0 = Do not generate an event

REGISTER 29-22: ADCFSTAT: ADC FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FEN	—	—	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN
23:16	R/W-0	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	U-0	U-0
	FIEN	FRDY	FWROVERR	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FCNT<7:0>							
7:0	R-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	FSIGN	—	—	—	—	ADCID<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FEN:** FIFO Enable bit
1 = FIFO is enabled
0 = FIFO is disabled; no data is being saved into the FIFO

bit 30-29 **Unimplemented:** Read as ‘0’

bit 28-24 **ADC4EN:ADC0EN:** ADCx Enable bits (‘x’ = 0 through 4)
1 = Converted output data of ADCx is stored in the FIFO
0 = Converted output data of ADCx is not stored in the FIFO

Note: While using FIFO, the output data is additionally stored in the respective output data register (ADCDATAx).

bit 23 **FIEN:** FIFO Interrupt Enable bit
1 = FIFO interrupts are enabled; an interrupt is generated once the FRDY bit is set
0 = FIFO interrupts are disabled

bit 22 **FRDY:** FIFO Data Ready Interrupt Status bit
1 = FIFO has data to be read
0 = No data is available in the FIFO

Note: This bit is cleared when the FIFO output data in ADCFIFO has been read and there is no additional data ready in the FIFO (that is, the FIFO is empty).

bit 21 **FWROVERR:** FIFO Write Overflow Error Status bit
1 = A write overflow error in the FIFO has occurred (circular FIFO)
0 = A write overflow error in the FIFO has not occurred

Note: This bit is cleared after ADCFSTAT<23:16> are read by software.

bit 15-8 **FCNT<7:0>:** FIFO Data Entry Count Status bit
The value in these bits indicates the number of data entries in the FIFO.

bit 7 **FSIGN:** FIFO Sign Setting bit
This bit reflects the sign of data stored in the ADCFIFO register.

bit 6-3 **Unimplemented:** Read as ‘0’

bit 2-0 **ADCID<2:0>:** ADCx Identifier bits (‘x’ = 0 through 6)
These bits specify the ADC module whose data is stored in the FIFO.
111 = Reserved
110 = Reserved
100 = Converted data of ADC4 is store in FIFO
.
.
.
000 = Converted data of ADC0 is stored in FIFO

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REGISTER 29-23: ADCFIFO: ADC FIFO DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** FIFO Data Output Value bits

Note: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

REGISTER 29-24: ADCBASE: ADC BASE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **Unimplemented:** Read as ‘0’

bit 15-0 **ADCBASE<15:0>:** ADC ISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS<2:0> bits of the ADCCON1 register specifying the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where ‘x’ is the smallest active analog input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

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REGISTER 29-25: ADCDATAx: ADC OUTPUT DATA REGISTER ‘x’ (‘x’ = 0 THROUGH 43)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

Note 1: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

2: Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

REGISTER 29-26: ADCTRGSNS: ADC TRIGGER LEVEL/EDGE SENSITIVITY REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	LVL11	LVL10	LVL9	LVL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11-0 **LVL11:LVL0:** Trigger Level and Edge Sensitivity bits

1 = Analog input is sensitive to the high level of its trigger (level sensitivity implies retriggering as long as the trigger signal remains high)

0 = Analog input is sensitive to the positive edge of its trigger (this is the value after a reset)

Note 1: This register specifies the trigger level for analog inputs 0 to 11.

2: The higher analog input ID belongs to Class 3, and therefore, is only scan triggered. All Class 3 analog inputs use the Scan Trigger, for which the level/edge is defined by the STRGLVL bit (ADCCON1<3>).

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REGISTER 29-27: ADCxTIME: DEDICATED ADCx TIMING REGISTER ('x' = 0 THROUGH 4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
	—	—	—	ADCEIS<2:0>			SELRES<1:0>	
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	ADCDIV<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SAMC<9:8>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **ADCEIS<2:0>:** ADCx Early Interrupt Select bits

111 = The data ready interrupt is generated 8 ADC clocks prior to the end of conversion
110 = The data ready interrupt is generated 7 ADC clocks prior to the end of conversion
.
.
.
001 = The data ready interrupt is generated 2 ADC clocks prior to the end of conversion
000 = The data ready interrupt is generated 1 ADC clock prior to the end of conversion

Note: All options are available when the selected resolution, specified by the SELRES<1:0> bits (ADCxTIME<25:24>), is 12-bit or 10-bit. For a selected resolution of 8-bit, options from '000' to '101' are valid. For a selected resolution of 6-bit, options from '000' to '011' are valid.

bit 25-24 **SELRES<1:0>:** ADCx Resolution Select bits

11 = 12 bits
10 = 10 bits
01 = 8 bits
00 = 6 bits

Note: Changing the resolution of the ADC does not shift the result in the corresponding ADCDATAx register. The result will still occupy 12 bits, with the corresponding lower unused bits set to '0'. For example, a resolution of 6 bits will result in ADCDATAx<5:0> being set to '0', and ADCDATAx<11:6> holding the result.

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **ADCDIV<6:0>:** ADCx Clock Divisor bits

These bits divide the ADC control clock with period T_Q to generate the clock for ADCx (T_{ADx}).

1111111 = 254 * T_Q = T_{ADx}
.
.
.
0000011 = 6 * T_Q = T_{ADx}
0000010 = 4 * T_Q = T_{ADx}
0000001 = 2 * T_Q = T_{ADx}
0000000 = Reserved

bit 15-10 **Unimplemented:** Read as '0'

REGISTER 29-27: ADCxTIME: DEDICATED ADCx TIMING REGISTER (CONTINUED)('x' = 0

bit 9-0 **SAMC<9:0>:** ADCx Sample Time bits

Where TADx = period of the ADC conversion clock for the dedicated ADC controlled by the ADCDIV<6:0> bits.

1111111111 = 1025 TADx
.
.
.
0000000001 = 3 TADx
0000000000 = 2 TADx

Note: If the ADCFLTRx<AFEN> = 1 then the ADCxTIME<SAMC> min must be ≥ 0x004 or equivalent to ≥ 6 TADx. This will correspondingly reduce the max sampling rate possible.

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REGISTER 29-28: ADCEIEN1: ADC EARLY INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN31	EIEN30	EIEN29	EIEN28	EIEN27	EIEN26	EIEN25	EIEN24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN23	EIEN22	EIEN21	EIEN20	EIEN19	EIEN18	EIEN17	EIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0

Legend:	HS = Hardware Set	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **EIEN31:EIEN0:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 31-0) of the ADCEISTAT1 register)

0 = Interrupts are disabled

REGISTER 29-29: ADCEIEN2: ADC EARLY INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	EIEN43	EIEN42	EIEN41	EIEN40
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN39	EIEN38	EIEN37	EIEN36	EIEN35	EIEN34	EIEN33	EIEN32

Legend:	HS = Hardware Set	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as ‘0’

bit 11-0 **EIEN43:EIEN32:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 43-32) of the ADCEISTAT2 register)

0 = Interrupts are disabled

REGISTER 29-30: ADCEISTAT1: ADC EARLY INTERRUPT STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY31	EIRDY30	EIRDY29	EIRDY28	EIRDY27	EIRDY26	EIRDY25	EIRDY24
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY23	EIRDY22	EIRDY21	EIRDY20	EIRDY19	EIRDY18	EIRDY17	EIRDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **EIRDY31:EIRDY0:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN1 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

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REGISTER 29-31: ADCEISTAT2: ADC EARLY INTERRUPT STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	EIRDY43	EIRDY42	EIRDY41	EIRDY40
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY39	EIRDY38	EIRDY37	EIRDY36	EIRDY35	EIRDY34	EIRDY33	EIRDY32

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11-0 **EIRDY43:EIRDY32:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN2 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

REGISTER 29-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	WKUPCLKCNT<3:0>			
23:16	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WKIEN7	—	—	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0
15:8	R-0, HS, HC	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	WKRDY7	—	—	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ANEN7	—	—	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27-24 **WKUPCLKCNT<3:0>:** Wake-up Clock Count bits

These bits represent the number of ADC clocks required to warm-up the ADC module before it can perform conversion. Although the clocks are specific to each ADC, the WKUPCLKCNT bit is common to all ADC modules.

1111 = 2^{15} = 32,768 clocks
.
.
.
0110 = 2^6 = 64 clocks
0101 = 2^5 = 32 clocks
0100 = 2^4 = 16 clocks
0011 = 2^4 = 16 clocks
0010 = 2^4 = 16 clocks
0001 = 2^4 = 16 clocks
0000 = 2^4 = 16 clocks

bit 23 **WKIEN7:** Shared ADC (ADC7) Wake-up Interrupt Enable bit

1 = Enable interrupt and generate interrupt when the WKRDY7 status bit is set
0 = Disable interrupt

bit 22-21 **Unimplemented:** Read as ‘0’

bit 20-16 **WKIEN4:WKIEN0:** ADC4-ADC0 Wake-up Interrupt Enable bit

1 = Enable interrupt and generate interrupt when the WKRDYx status bit is set
0 = Disable interrupt

bit 15 **WKRDY7:** Shared ADC (ADC7) Wake-up Status bit

1 = ADC7 Analog and Bias circuitry ready after the wake-up count number $2^{WKUPEXP}$ clocks after setting ANEN7 to ‘1’
0 = ADC7 Analog and Bias circuitry is not ready

Note: This bit is cleared by hardware when the ANEN7 bit is cleared

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12-8 **WKRDY4:WKRDY0:** ADC4-ADC0 Wake-up Status bit

1 = ADCx Analog and Bias circuitry ready after the wake-up count number $2^{WKUPEXP}$ clocks after setting ANEN*x* to ‘1’
0 = ADCx Analog and Bias circuitry is not ready

Note: These bits are cleared by hardware when the ANEN*x* bit is cleared

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REGISTER 29-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit

1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.

0 = Analog and bias circuitry disabled

bit 5-6 **Unimplemented:** Read as '0'

bit 4-0 **ANEN4:ANEN0:** ADC4-ADC0 Analog and Bias Circuitry Enable bits

1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.

0 = Analog and bias circuitry disabled

REGISTER 29-33: ADCxCFG: ADCx CONFIGURATION REGISTER ('x' = 1 THROUGH 4 AND 7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCFG<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCFG<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCFG<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCFG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ADCCFG<31:0>:** ADC Module Configuration Data bits

Prior to enabling the ADC, these registers should be written with the corresponding value stored in DEVADCx in software during ADC initialization.

Note: These bits can only change when the applicable ANEN*x* bit in the ADCANCON register is cleared. These are calibration values determined at product test time and are provided to the user through DEVADCx fuse bits (see Register 41-8).

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REGISTER 29-34: ADCSYSCFG1: ADC SYSTEM CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
	AN<31:23>							
23:16	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
	AN<23:16>							
15:8	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
	AN<15:8>							
7:0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
	AN<7:0>							

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **AN<31:0>:** ADC Analog Input bits
These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

REGISTER 29-35: ADCSYSCFG2: ADC SYSTEM CONFIGURATION REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
	—	—	—	—	AN<43:40>			
7:0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS
	AN<39:32>							

Legend:	HS = Hardware Set	HC = Cleared by Software	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12-0 **AN<43:32>:** ADC Analog Input bits
These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

NOTES:

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30.0 CONTROLLER AREA NETWORK (CAN)

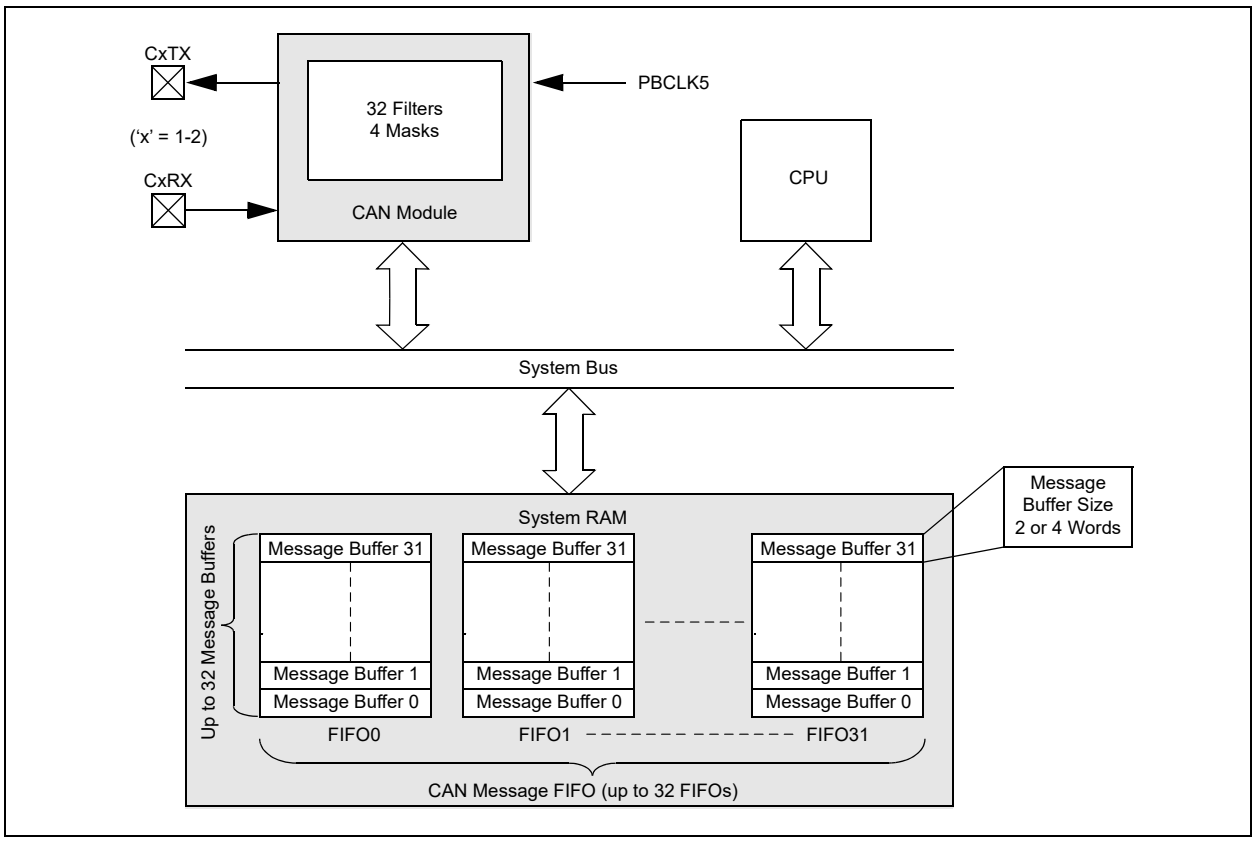
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
  - 32 message FIFOs
  - Each FIFO can have up to 32 messages for a total of 1024 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 32 acceptance filters for message filtering
  - Four acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
- Additional Features:
  - Loopback, Listen All Messages and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus host on the PIC32 System Bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 30-1 illustrates the general structure of the CAN module.

FIGURE 30-1: PIC32 CAN MODULE BLOCK DIAGRAM



30.1 CAN Control Registers

Note: The ‘i’ shown in register names denotes CAN1 or CAN2.

TABLE 30-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	C1CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
0010	C1CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>						0000
0020	C1INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
0030	C1VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
0040	C1TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
0050	C1FSTAT	31:16	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
0060	C1RXOVF	31:16	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
0070	C1TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
0080	C1RXM0	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
0090	C1RXM1	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00A0	C1RXM2	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00B0	C1RXM3	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00C0	C1FLTCON0	31:16	FLTEN3	MSEL3<1:0>		FSEL3<4:0>					FLTEN2	MSEL2<1:0>		FSEL2<4:0>					0000
		15:0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>					FLTEN0	MSEL0<1:0>		FSEL0<4:0>					0000
00D0	C1FLTCON1	31:16	FLTEN7	MSEL7<1:0>		FSEL7<4:0>					FLTEN6	MSEL6<1:0>		FSEL6<4:0>					0000
		15:0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>					FLTEN4	MSEL4<1:0>		FSEL4<4:0>					0000
00E0	C1FLTCON2	31:16	FLTEN11	MSEL11<1:0>		FSEL11<4:0>					FLTEN10	MSEL10<1:0>		FSEL10<4:0>					0000
		15:0	FLTEN9	MSEL9<1:0>		FSEL9<4:0>					FLTEN8	MSEL8<1:0>		FSEL8<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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TABLE 30-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
00F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000
0100	C1FLTCON4	31:16	FLTEN19	MSEL19<1:0>		FSEL19<4:0>					FLTEN18	MSEL18<1:0>		FSEL18<4:0>					0000
		15:0	FLTEN17	MSEL17<1:0>		FSEL17<4:0>					FLTEN16	MSEL16<1:0>		FSEL16<4:0>					0000
0110	C1FLTCON5	31:16	FLTEN23	MSEL23<1:0>		FSEL23<4:0>					FLTEN22	MSEL22<1:0>		FSEL22<4:0>					0000
		15:0	FLTEN21	MSEL21<1:0>		FSEL21<4:0>					FLTEN20	MSEL20<1:0>		FSEL20<4:0>					0000
0120	C1FLTCON6	31:16	FLTEN27	MSEL27<1:0>		FSEL27<4:0>					FLTEN26	MSEL26<1:0>		FSEL26<4:0>					0000
		15:0	FLTEN25	MSEL25<1:0>		FSEL25<4:0>					FLTEN24	MSEL24<1:0>		FSEL24<4:0>					0000
0130	C1FLTCON7	31:16	FLTEN31	MSEL31<1:0>		FSEL31<4:0>					FLTEN30	MSEL30<1:0>		FSEL30<4:0>					0000
		15:0	FLTEN29	MSEL29<1:0>		FSEL29<4:0>					FLTEN28	MSEL28<1:0>		FSEL28<4:0>					0000
0140-0330	C1RXFn (n = 0-31)	31:16	SID<10:0>											—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
0340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0																	0000
0350	C1FIFOCONn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
0360	C1FIFOINTn (n = 0)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
0370	C1FIFOUAn (n = 0)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
0380	C1FIFOCIn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000
0390-0B40	C1FIFOCONn C1FIFOINTn C1FIFOUAn C1FIFOCIn (n = 1-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
		31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
		31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 30-2: CAN2 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1000	C2CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
1010	C2CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>						0000
1020	C2INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
1030	C2VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
1040	C2TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
1050	C2FSTAT	31:16	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
1060	C2RXOVF	31:16	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
1070	C2TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
1080	C2RXM0	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
10A0	C2RXM1	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
10B0	C2RXM2	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
10B0	C2RXM3	31:16	SID<10:0>											—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
1010	C2FLTCON0	31:16	FLTEN3	MSEL3<1:0>		FSEL3<4:0>					FLTEN2	MSEL2<1:0>		FSEL2<4:0>					0000
		15:0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>					FLTEN0	MSEL0<1:0>		FSEL0<4:0>					0000
10D0	C2FLTCON1	31:16	FLTEN7	MSEL7<1:0>		FSEL7<4:0>					FLTEN6	MSEL6<1:0>		FSEL6<4:0>					0000
		15:0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>					FLTEN4	MSEL4<1:0>		FSEL4<4:0>					0000
10E0	C2FLTCON2	31:16	FLTEN11	MSEL11<1:0>		FSEL11<4:0>					FLTEN10	MSEL10<1:0>		FSEL10<4:0>					0000
		15:0	FLTEN9	MSEL9<1:0>		FSEL9<4:0>					FLTEN8	MSEL8<1:0>		FSEL8<4:0>					0000
10F0	C2FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 30-2: CAN2 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1100	C2FLTCON4	31:16	FLTEN19	MSEL19<1:0>		FSEL19<4:0>					FLTEN18	MSEL18<1:0>		FSEL18<4:0>					0000
		15:0	FLTEN17	MSEL17<1:0>		FSEL17<4:0>					FLTEN16	MSEL16<1:0>		FSEL16<4:0:					0000
1110	C2FLTCON5	31:16	FLTEN23	MSEL23<1:0>		FSEL23<4:0>					FLTEN22	MSEL22<1:0>		FSEL22<4:0>					0000
		15:0	FLTEN21	MSEL21<1:0>		FSEL21<4:0>					FLTEN20	MSEL20<1:0>		FSEL20<4:0>					0000
1120	C2FLTCON6	31:16	FLTEN27	MSEL27<1:0>		FSEL27<4:0>					FLTEN26	MSEL26<1:0>		FSEL26<4:0>					0000
		15:0	FLTEN25	MSEL25<1:0>		FSEL25<4:0>					FLTEN24	MSEL24<1:0>		FSEL24<4:0>					0000
1130	C2FLTCON7	31:16	FLTEN31	MSEL31<1:0>		FSEL31<4:0>					FLTEN30	MSEL30<1:0>		FSEL30<4:0>					0000
		15:0	FLTEN29	MSEL29<1:0>		FSEL29<4:0>					FLTEN28	MSEL28<1:0>		FSEL28<4:0>					0000
1140-1330	C2RXFn (n = 0-31)	31:16	SID<10:0>											—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
1340	C2FIFOBA	31:16	C2FIFOBA<31:0>																0000
		15:0																	0000
1350	C2FIFOCONn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
1360	C2FIFOINTn (n = 0)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
1370	C2FIFOUAn (n = 0)	31:16	C2FIFOUA<31:0>																0000
		15:0																	0000
1380	C2FIFOCIn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C2FIFOCI<4:0>					0000
1390-1B40	C2FIFOCONn C2FIFOINTn C2FIFOUAn C2FIFOCIn (n = 1-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
		31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
		31:16	C2FIFOUA<31:0>																0000
		15:0																	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C2FIFOCI<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 30-1: CiCON: CAN MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved - Do not use
101 = Reserved - Do not use
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as ‘0’

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

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REGISTER 30-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)

bit 13 **SIDLE:** CAN Stop in Idle bit
1 = CAN Stops operation when system enters Idle mode
0 = CAN continues operation when system enters Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **CANBUSY:** CAN Module is Busy bit
1 = The CAN module is active
0 = The CAN module is completely disabled

bit 10-5 **Unimplemented:** Read as '0'

bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
•
•
•
00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 30-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0>(1,4)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS(1)	SAM(2)	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0>(3)		BRP<5:0>					

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as ‘0’

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

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REGISTER 30-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits[4]

111 = Length is 8 x TQ

•

•

•

000 = Length is 1 x TQ

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits[3]

11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits

111111 = TQ = (2 x 64)/TPBCLK5
111110 = TQ = (2 x 63)/TPBCLK5

•

•

•

000001 = TQ = (2 x 2)/TPBCLK5
000000 = TQ = (2 x 1)/TPBCLK5

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

2: 3 Time bit sampling is not allowed for BRP < 2.

3: SJW ≤ SEG2PH.

4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

REGISTER 30-3: CiINT: CAN INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIF	WAKIF	CERRIF	SERRIF(1)	RBOVIF	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 30 **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 29 **CERRIE:** CAN Bus Error Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 28 **SERRIE:** System Error Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 27 **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 26-20 **Unimplemented:** Read as ‘0’

bit 19 **MODIE:** Mode Change Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 18 **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 17 **RBIE:** Receive Buffer Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 16 **TBIE:** Transmit Buffer Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

bit 15 **IVRIF:** Invalid Message Received Interrupt Flag bit
1 = An invalid messages interrupt has occurred
0 = An invalid message interrupt has not occurred

Note 1: This bit can only be cleared by turning the CAN module ON and OFF by clearing or setting the ON bit (CiCON<15>).

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REGISTER 30-3: CiINT: CAN INTERRUPT REGISTER (CONTINUED)

bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred

bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred

bit 12 **SERRIF:** System Error Interrupt Flag bit
1 = A system error occurred (typically an illegal address was presented to the System Bus)
0 = A system error has not occurred

bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred

bit 10-4 **Unimplemented:** Read as '0'

bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred

bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred

bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending

bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

Note 1: This bit can only be cleared by turning the CAN module ON and OFF by clearing or setting the ON bit (CiCON<15>).

REGISTER 30-4: CiVEC: CAN INTERRUPT CODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	FILHIT<4:0>				
7:0	U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	—	ICODE<6:0>(1)						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bit

11111 = Filter 31
11110 = Filter 30
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits(1)

1001000-1111111 = Reserved
1001000 = Invalid message received (IVRIF)
1000111 = CAN module mode change (MODIF)
1000110 = CAN timestamp timer (CTMRIF)
1000101 = Bus bandwidth error (SERRIF)
1000100 = Address error interrupt (SERRIF)
1000011 = Receive FIFO overflow interrupt (RBOVIF)
1000010 = Wake-up interrupt (WAKIF)
1000001 = Error Interrupt (CERRIF)
1000000 = No interrupt
0100000-0111111 = Reserved
0011111 = FIFO31 Interrupt (CiFSTAT<31> set)
0011110 = FIFO30 Interrupt (CiFSTAT<30> set)
•
•
•
0000001 = FIFO1 Interrupt (CiFSTAT<1> set)
0000000 = FIFO0 Interrupt (CiFSTAT<0> set)

Note 1: These bits are only updated for enabled interrupts.

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REGISTER 30-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as ‘0’
bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)
bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)
bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)
bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)
bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)
bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning
bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter
bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 30-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **FIFOIP<31:0>:** FIFOn Interrupt Pending bits
1 = One or more enabled FIFO interrupts are pending
0 = No FIFO interrupts are pending

REGISTER 30-7: CiRXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **RXOVF<31:0>:** FIFOn Receive Overflow Interrupt Pending bit
`1` = FIFO has overflowed
`0` = FIFO has not overflowed

REGISTER 30-8: CiTMR: CAN TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CANTS<15:0>:** CAN Time Stamp Timer bits
This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (CiCON<20>) is set.

bit 15-0 **CANTSPRE<15:0>:** CAN Time Stamp Timer Prescaler bits
`1111 1111 1111 1111` = CAN time stamp timer (CANTS) increments every 65,535 system clocks
•
•
•
`0000 0000 0000 0000` = CAN time stamp timer (CANTS) increments every system clock

Note 1: CiTMR will be frozen when CANCAP = `0`.
2: The CiTMR prescaler count will be Reset on any write to CiTMR (CANTSPRE will be unaffected).

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REGISTER 30-9: CiRXMN: CAN ACCEPTANCE FILTER MASK N REGISTER (N = 0, 1, 2 OR 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SID<10:3>							
23:16	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SID<2:0>			—	MIDE	—	EID<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
`1` = Include bit, SIDx, in filter comparison
`0` = Bit SIDx is ‘don’t care’ in filter operation

bit 20 **Unimplemented:** Read as ‘`0`’

bit 19 **MIDE:** Identifier Receive Mode bit
`1` = Match only message types (standard/extended address) that correspond to the EXID bit in filter
`0` = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented:** Read as ‘`0`’

bit 17-0 **EID<17:0>:** Extended Identifier bits
`1` = Include bit, EIDx, in filter comparison
`0` = Bit EIDx is ‘don’t care’ in filter operation

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = `100`).

REGISTER 30-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN3:** Filter 3 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
`11` = Acceptance Mask 3 is selected
`10` = Acceptance Mask 2 is selected
`01` = Acceptance Mask 1 is selected
`00` = Acceptance Mask 0 is selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
`11` = Acceptance Mask 3 is selected
`10` = Acceptance Mask 2 is selected
`01` = Acceptance Mask 1 is selected
`00` = Acceptance Mask 0 is selected

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘`0`’.

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REGISTER 30-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 15 **FLTEN1:** Filter 1 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits

11 = Acceptance Mask 3 is selected
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits

11 = Acceptance Mask 3 is selected
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN7	MSEL7<1:0>		FSEL7<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN6	MSEL6<1:0>		FSEL6<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN5	MSEL5<1:0>		FSEL5<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN4	MSEL4<1:0>		FSEL4<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN7:** Filter 7 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 30-29 **MSEL7<1:0>:** Filter 7 Mask Select bits
`11` = Acceptance Mask 3 is selected
`10` = Acceptance Mask 2 is selected
`01` = Acceptance Mask 1 is selected
`00` = Acceptance Mask 0 is selected

bit 28-24 **FSEL7<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN6:** Filter 6 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 22-21 **MSEL6<1:0>:** Filter 6 Mask Select bits
`11` = Acceptance Mask 3 is selected
`10` = Acceptance Mask 2 is selected
`01` = Acceptance Mask 1 is selected
`00` = Acceptance Mask 0 is selected

bit 20-16 **FSEL6<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘`0`’.

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REGISTER 30-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)

bit 15 **FLTEN5:** Filter 17 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL5<1:0>:** Filter 5 Mask Select bits

11 = Acceptance Mask 3 is selected
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL5<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4:** Filter 4 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL4<1:0>:** Filter 4 Mask Select bits

11 = Acceptance Mask 3 is selected
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL4<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN11	MSEL11<1:0>		FSEL11<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN10	MSEL10<1:0>		FSEL10<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN9	MSEL9<1:0>		FSEL9<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN8	MSEL8<1:0>		FSEL8<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN11:** Filter 11 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits
11 = Acceptance Mask 3 is selected
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 28-24 **FSEL11<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN10:** Filter 10 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits
11 = Acceptance Mask 3 is selected
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 20-16 **FSEL10<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘0’.

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REGISTER 30-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)

bit 15 **FLTEN9:** Filter 9 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL9<1:0>:** Filter 9 Mask Select bits

11 = Acceptance Mask 3 is selected
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL9<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN8:** Filter 8 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL8<1:0>:** Filter 8 Mask Select bits

11 = Acceptance Mask 3 is selected
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL8<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN15	MSEL15<1:0>		FSEL15<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN14	MSEL14<1:0>		FSEL14<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN13	MSEL13<1:0>		FSEL13<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN12	MSEL12<1:0>		FSEL12<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN15:** Filter 15 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 30-29 **MSEL15<1:0>:** Filter 15 Mask Select bits
`11` = Acceptance Mask 3 is selected
`10` = Acceptance Mask 2 is selected
`01` = Acceptance Mask 1 is selected
`00` = Acceptance Mask 0 is selected

bit 28-24 **FSEL15<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN14:** Filter 14 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 22-21 **MSEL14<1:0>:** Filter 14 Mask Select bits
`11` = Acceptance Mask 3 is selected
`10` = Acceptance Mask 2 is selected
`01` = Acceptance Mask 1 is selected
`00` = Acceptance Mask 0 is selected

bit 20-16 **FSEL14<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘`0`’.

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REGISTER 30-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)

bit 15 **FLTEN13:** Filter 13 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN19	MSEL19<1:0>		FSEL19<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN18	MSEL18<1:0>		FSEL18<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN17	MSEL17<1:0>		FSEL17<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN16	MSEL16<1:0>		FSEL16<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN19:** Filter 19 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 30-29 **MSEL19<1:0>:** Filter 19 Mask Select bits
`11` = Acceptance Mask 3 selected
`10` = Acceptance Mask 2 selected
`01` = Acceptance Mask 1 selected
`00` = Acceptance Mask 0 selected

bit 28-24 **FSEL19<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN18:** Filter 18 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 22-21 **MSEL18<1:0>:** Filter 18 Mask Select bits
`11` = Acceptance Mask 3 selected
`10` = Acceptance Mask 2 selected
`01` = Acceptance Mask 1 selected
`00` = Acceptance Mask 0 selected

bit 20-16 **FSEL18<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘`0`’.

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REGISTER 30-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4 (CONTINUED)

bit 15 **FLTEN17:** Filter 13 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL17<1:0>:** Filter 17 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL17<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN16:** Filter 16 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL16<1:0>:** Filter 16 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL16<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN23:** Filter 23 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
`11` = Acceptance Mask 3 selected
`10` = Acceptance Mask 2 selected
`01` = Acceptance Mask 1 selected
`00` = Acceptance Mask 0 selected

bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN22:** Filter 22 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
`11` = Acceptance Mask 3 selected
`10` = Acceptance Mask 2 selected
`01` = Acceptance Mask 1 selected
`00` = Acceptance Mask 0 selected

bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘`0`’.

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REGISTER 30-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5 (CONTINUED)

bit 15 **FLTEN21:** Filter 21 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL21<1:0>:** Filter 21 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL21<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN20:** Filter 20 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL20<1:0>:** Filter 20 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL20<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN27	MSEL27<1:0>		FSEL27<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN26	MSEL26<1:0>		FSEL26<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN25	MSEL25<1:0>		FSEL25<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN24	MSEL24<1:0>		FSEL24<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN27:** Filter 27 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 30-29 **MSEL27<1:0>:** Filter 27 Mask Select bits
`11` = Acceptance Mask 3 selected
`10` = Acceptance Mask 2 selected
`01` = Acceptance Mask 1 selected
`00` = Acceptance Mask 0 selected

bit 28-24 **FSEL27<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN26:** Filter 26 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 22-21 **MSEL26<1:0>:** Filter 26 Mask Select bits
`11` = Acceptance Mask 3 selected
`10` = Acceptance Mask 2 selected
`01` = Acceptance Mask 1 selected
`00` = Acceptance Mask 0 selected

bit 20-16 **FSEL26<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘`0`’.

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REGISTER 30-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6 (CONTINUED)

bit 15 **FLTEN25:** Filter 25 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL25<1:0>:** Filter 25 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL25<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN24:** Filter 24 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL24<1:0>:** Filter 24 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL24<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN31	MSEL31<1:0>		FSEL31<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN30	MSEL30<1:0>		FSEL30<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN29	MSEL29<1:0>		FSEL29<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN28	MSEL28<1:0>		FSEL28<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN31:** Filter 31 Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 30-29 **MSEL31<1:0>:** Filter 31 Mask Select bits
`11` = Acceptance Mask 3 selected
`10` = Acceptance Mask 2 selected
`01` = Acceptance Mask 1 selected
`00` = Acceptance Mask 0 selected

bit 28-24 **FSEL31<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN30:** Filter 30Enable bit
`1` = Filter is enabled
`0` = Filter is disabled

bit 22-21 **MSEL30<1:0>:** Filter 30Mask Select bits
`11` = Acceptance Mask 3 selected
`10` = Acceptance Mask 2 selected
`01` = Acceptance Mask 1 selected
`00` = Acceptance Mask 0 selected

bit 20-16 **FSEL30<4:0>:** FIFO Selection bits
`11111` = Message matching filter is stored in FIFO buffer 31
`11110` = Message matching filter is stored in FIFO buffer 30
•
•
•
`00001` = Message matching filter is stored in FIFO buffer 1
`00000` = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is ‘`0`’.

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REGISTER 30-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7 (CONTINUED)

bit 15 **FLTEN29:** Filter 29 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL29<1:0>:** Filter 29 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL29<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN28:** Filter 28 Enable bit

1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL28<1:0>:** Filter 28 Mask Select bits

11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL28<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-18: CiRXFn: CAN ACCEPTANCE FILTER N REGISTER 7 (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SID<10:3>							
23:16	R/W-x	R/W-x	R/W-x	U-0	R/W-0	U-0	R/W-x	R/W-x
	SID<2:0>			—	EXID	—	EID<17:16>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Message address bit SIDx must be ‘1’ to match filter
0 = Message address bit SIDx must be ‘0’ to match filter

bit 20 **Unimplemented:** Read as ‘0’

bit 19 **EXID:** Extended Identifier Enable bits
1 = Match only messages with extended identifier addresses
0 = Match only messages with standard identifier addresses

bit 18 **Unimplemented:** Read as ‘0’

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Message address bit EIDx must be ‘1’ to match filter
0 = Message address bit EIDx must be ‘0’ to match filter

Note: This register can only be modified when the filter is disabled (FLTENn = 0).

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REGISTER 30-19: CiFIFOBA: CAN MESSAGE BUFFER BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CiFIFOBA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CiFIFOBA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CiFIFOBA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0(1)	R-0(1)
	CiFIFOBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CiFIFOBA<31:0>:** CAN FIFO Base Address bits

These bits define the base address of all message buffers. Individual message buffers are located based on the size of the previous message buffers. This address is a physical address. Note that bits <1:0> are read-only and read ‘0’, forcing the messages to be 32-bit word-aligned in device RAM.

Note 1: This bit is unimplemented and will always read ‘0’, which forces word-alignment of messages.

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

REGISTER 30-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	FSIZE<4:0>(1)				
15:8	U-0	S/HC-0	S/HC-0	R/W-0	U-0	U-0	U-0	U-0
	—	FRESET	UINC	DONLY(1)	—	—	—	—
7:0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXEN	TXABAT(2)	TXLARB(3)	TXERR(3)	TXREQ	RTREN	TXPR<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as ‘0’

bit 20-16 **FSIZE<4:0>:** FIFO Size bits(1)

11111 = FIFO is 32 messages deep

•

•

•

00010 = FIFO is 3 messages deep
00001 = FIFO is 2 messages deep
00000 = FIFO is 1 message deep

bit 15 **Unimplemented:** Read as ‘0’

bit 14 **FRESET:** FIFO Reset bits

1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset. After setting, the user should poll if this bit is clear before taking any action
0 = No effect

bit 13 **UINC:** Increment Head/Tail bit

TXEN = 1: (FIFO configured as a Transmit FIFO)
When this bit is set the FIFO head will increment by a single message

TXEN = 0: (FIFO configured as a Receive FIFO)
When this bit is set the FIFO tail will increment by a single message

bit 12 **DONLY:** Store Message Data Only bit(1)

TXEN = 1: (FIFO configured as a Transmit FIFO)
This bit is not used and has no effect.

TXEN = 0: (FIFO configured as a Receive FIFO)
1 = Only data bytes will be stored in the FIFO
0 = Full message is stored, including identifier

bit 11-8 **Unimplemented:** Read as ‘0’

bit 7 **TXEN:** TX/RX Buffer Selection bit

1 = FIFO is a Transmit FIFO
0 = FIFO is a Receive FIFO

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).

2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

3: This bit is reset on any read of this register or when the FIFO is reset.

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REGISTER 30-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER (n = 0 THROUGH 31)

bit 6 **TXABAT:** Message Aborted bit(2)

1 = Message was aborted
0 = Message completed successfully

bit 5 **TXLARB:** Message Lost Arbitration bit(3)

1 = Message lost arbitration while being sent
0 = Message did not loose arbitration while being sent

bit 4 **TXERR:** Error Detected During Transmission bit(3)

1 = A bus error occured while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQ:** Message Send Request

TXEN = 1: (FIFO configured as a Transmit FIFO)
Setting this bit to '1' requests sending a message.
The bit will automatically clear when all the messages queued in the FIFO are successfully sent
Clearing the bit to '0' while set ('1') will request a message abort.

TXEN = 0: (FIFO configured as a Receive FIFO)
This bit has no effect.

bit 2 **RTREN:** Auto RTR Enable bit

1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXPR<1:0>:** Message Transmit Priority bits

11 = Highest Message Priority
10 = High Intermediate Message Priority
01 = Low Intermediate Message Priority
00 = Lowest Message Priority

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).

2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

3: This bit is reset on any read of this register or when the FIFO is reset.

REGISTER 30-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	TXNFULLIF(1)	TXHALFIF	TXEMPTYIF(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
	—	—	—	—	RXOVFLIF	RXFULLIF(1)	RXHALFIF(1)	RXNEMPTYIF(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as ‘0’

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a Transmit Buffer)
1 = FIFO is not full
0 = FIFO is full

TXEN = 0: (FIFO configured as a Receive Buffer)
Unused, reads ‘0’

Note 1: This bit is read-only and reflects the status of the FIFO.

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REGISTER 30-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER (n = 0 THROUGH 31)

bit 9 **TXHALFIF:** FIFO Transmit FIFO Half Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a Transmit Buffer)
1 = FIFO is ≤ half full
0 = FIFO is > half full

TXEN = 0: (FIFO configured as a Receive Buffer)
Unused, reads '0'

bit 8 **TXEMPTYIF:** Transmit FIFO Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a Transmit Buffer)
1 = FIFO is empty
0 = FIFO is not empty, at least 1 message queued to be transmitted

TXEN = 0: (FIFO configured as a Receive Buffer)
Unused, reads '0'

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **RXOVFLIF:** Receive FIFO Overflow Interrupt Flag bit

TXEN = 1: (FIFO configured as a Transmit Buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a Receive Buffer)
1 = Overflow event has occurred
0 = No overflow event occured

bit 2 **RXFULLIF:** Receive FIFO Full Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a Transmit Buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a Receive Buffer)
1 = FIFO is full
0 = FIFO is not full

bit 1 **RXHALFIF:** Receive FIFO Half Full Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a Transmit Buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a Receive Buffer)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **RXNEMPTYIF:** Receive Buffer Not Empty Interrupt Flag bit(1)

TXEN = 1: (FIFO configured as a Transmit Buffer)
Unused, reads '0'

TXEN = 0: (FIFO configured as a Receive Buffer)
1 = FIFO is not empty, has at least 1 message
0 = FIFO is empty

Note 1: This bit is read-only and reflects the status of the FIFO.

REGISTER 30-22: CiFIFOUAn: CAN FIFO USER ADDRESS REGISTER (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUAn<31:24>							
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUAn<23:16>							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUAn<15:8>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-0(1)	R-0(1)
	CiFIFOUAn<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CiFIFOUAn<31:0>:** CAN FIFO User Address bits

TXEN = 1: (FIFO configured as a Transmit Buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a Receive Buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit will always read ‘0’, which forces byte-alignment of messages.

Note: This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

REGISTER 30-23: CiFIFOCIN: CAN MODULE MESSAGE INDEX REGISTER (n = 0 THROUGH 31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	CiFIFOCI<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as ‘0’

bit 4-0 **CiFIFOCIn<4:0>:** CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a Transmit Buffer)
A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a Receive Buffer)
A read of this register will return an index to the message that the FIFO will use to save the next message.

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31.0 ETHERNET CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 35. "Ethernet Controller"** (DS60001155), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Ethernet controller is a bus host module that interfaces with an off-chip Physical Layer (PHY) to implement a complete Ethernet node in a system.

Key features of the Ethernet Controller include:

- Supports 10/100 Mbps data transfer rates
- Supports full-duplex and half-duplex operation
- Supports RMII and MII PHY interface
- Supports MIIM PHY management interface
- Supports both manual and automatic Flow Control
- RAM descriptor-based DMA operation for both receive and transmit path
- Fully configurable interrupts
- Configurable receive packet filtering
  - CRC check
  - 64-byte pattern match
  - Broadcast, multicast and unicast packets
  - Magic Packet™
  - 64-bit hash table
  - Runt packet
- Supports packet payload checksum calculation
- Supports various hardware statistics counters

Figure 31-1 illustrates a block diagram of the Ethernet controller.

FIGURE 31-1: ETHERNET CONTROLLER BLOCK DIAGRAM

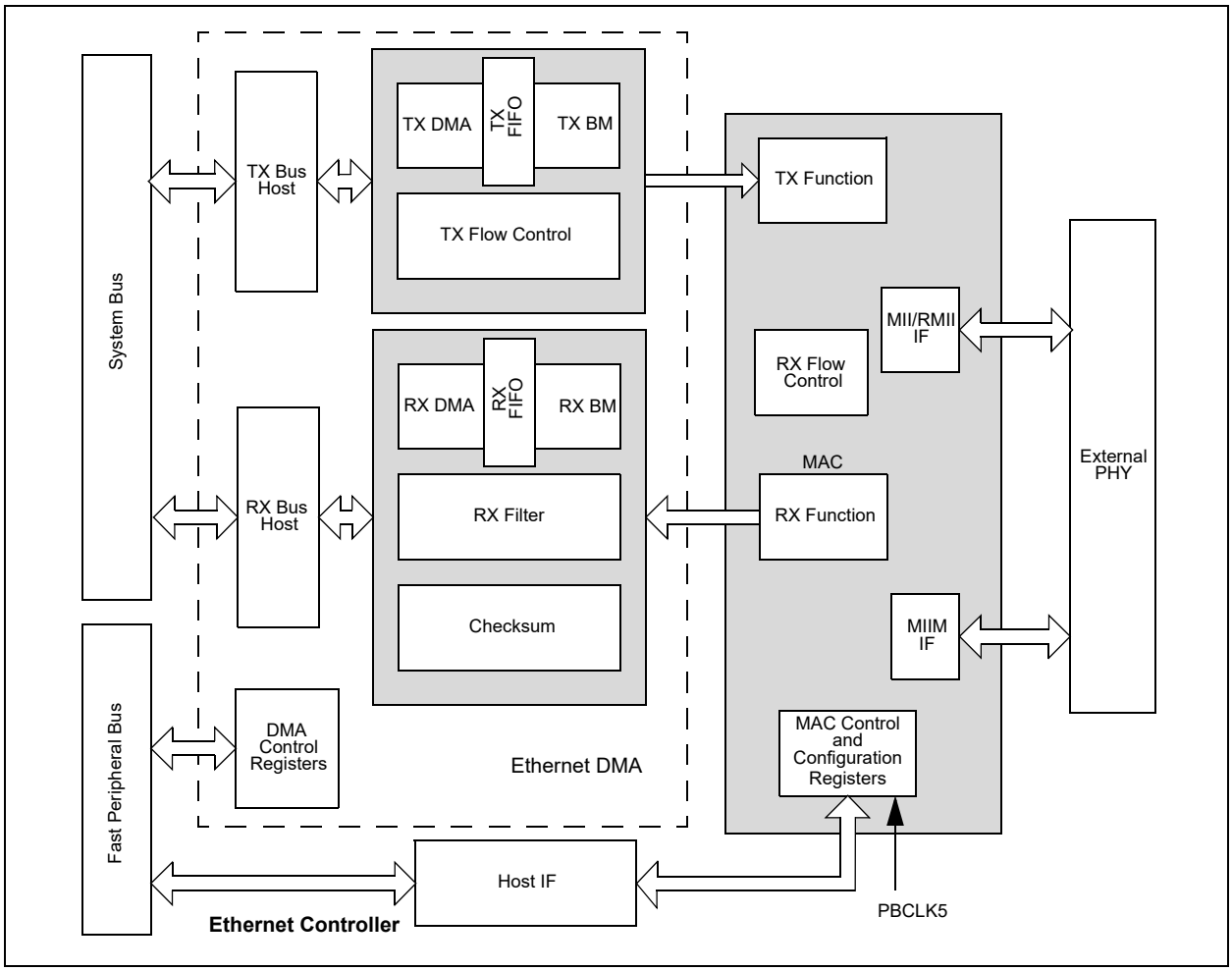

Table 31-1 and Table 31-2 show two interfaces and the associated pins that can be used with the Ethernet Controller.

TABLE 31-1: MII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXCLK	Transmit Clock
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
ETXD2	Transmit Data
ETXD3	Transmit Data
ETXERR	Transmit Error
ERXCLK	Receive Clock
ERXDV	Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXD2	Receive Data
ERXD3	Receive Data
ERXERR	Receive Error
ECRS	Carrier Sense
ECOL	Collision Indication

TABLE 31-2: RMII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 1)

Pin Name	Description
EMDC	Management Clock
EMDIO	Management I/O
ETXEN	Transmit Enable
ETXD0	Transmit Data
ETXD1	Transmit Data
EREFCLK	Reference Clock
ECRSDV	Carrier Sense – Receive Data Valid
ERXD0	Receive Data
ERXD1	Receive Data
ERXERR	Receive Error

Note: Ethernet controller pins that are not used by the selected interface can be used by other peripherals.

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31.1 Ethernet Control Registers

TABLE 31-3: ETHERNET CONTROLLER REGISTER SUMMARY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2000	ETHCON1	31:16	PTV<15:0>																0000
		15:0	ON	—	SIDL	—	—	—	TXRTS	RXEN	AUTOFC	—	—	MANFC	—	—	—	BUFCDEC	0000
2010	ETHCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	RXBUFSZ<6:0>							—	—	—	—	0000
2020	ETHTXST	31:16	TXSTADDR<31:16>																0000
		15:0	TXSTADDR<15:2>														—	—	0000
2030	ETHRXST	31:16	RXSTADDR<31:16>																0000
		15:0	RXSTADDR<15:2>														—	—	0000
2040	ETHHT0	31:16	HT<31:0>																0000
		15:0																	0000
2050	ETHHT1	31:16	HT<63:32>																0000
		15:0																	0000
2060	ETHPMM0	31:16	PMM<31:0>																0000
		15:0																	0000
2070	ETHPMM1	31:16	PMM<63:32>																0000
		15:0																	0000
2080	ETHPMCS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMCS<15:0>																0000
2090	ETHPMO	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMO<15:0>																0000
20A0	ETHRXFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	HTEN	MPEN	—	NOTPM	PMMODE<3:0>				CRC ERREN	CRC OKEN	RUNT ERREN	RUNTEN	UCEN	NOT MEEN	MCEN	BCEN	0000
20B0	ETHRXWM	31:16	—	—	—	—	—	—	—	—	RXFWM<7:0>								0000
		15:0	—	—	—	—	—	—	—	—	RXEWM<7:0>								0000
20C0	ETHIEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TX BUSEIE	RX BUSEIE	—	—	—	EW MARKIE	FW MARKIE	RX DONEIE	PK TPENDIE	RX ACTIE	—	TX DONEIE	TX ABORTIE	RX BUFNAIE	RX OVFLWIE	0000
20D0	ETHIRQ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	TXBUSE	RXBUSE	—	—	—	EWMARK	FWMARK	RXDONE	PKTPEND	RXACT	—	TXDONE	TXABORT	RXBUFNA	RXOVFLW	0000
20E0	ETHSTAT	31:16	—	—	—	—	—	—	—	—	BUFCNT<7:0>								0000
		15:0	—	—	—	—	—	—	—	—	BUSY	TXBUSY	RXBUSY	—	—	—	—	—	0000
2100	ETH RXOVFLOW	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVFLWCNT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: Reset values default to the factory programmed value.

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TABLE 31-3: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2110	ETH FRMTXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMTXOKCNT<15:0>																0000
2120	ETH SCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SCOLFRMCNT<15:0>																0000
2130	ETH MCOLFRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MCOLFRMCNT<15:0>																0000
2140	ETH FRMRXOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FRMRXOKCNT<15:0>																0000
2150	ETH FCSERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FCSERRCNT<15:0>																0000
2160	ETH ALGNERR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALGNERRCNT<15:0>																0000
2200	EMAC1 CFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN	—	—	—	LOOPBACK	TXPAUSE	RXPAUSE	PASSALL	RXENABLE	800D
2210	EMAC1 CFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	EXCESS DFR	BP NOBKOFF	NOBKOFF	—	—	LONGPRE	PUREPRE	AUTOPAD	VLANPAD	PAD ENABLE	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX	4082
2220	EMAC1 IPGT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	B2BIPKTGP<6:0>							0012
2230	EMAC1 IPGR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	NB2BIPKTGP1<6:0>							—	NB2BIPKTGP2<6:0>							0C12
2240	EMAC1 CLRT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CWINDOW<5:0>						—	—	—	—	RETX<3:0>				370F
2250	EMAC1 MAXF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MACMAXF<15:0>																05EE
2260	EMAC1 SUPP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	RESET RMII	—	—	SPEED RMII	—	—	—	—	—	—	—	—	1000
2270	EMAC1 TEST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	TESTBP	TESTPAUSE	SHRTQNTA	0000
2280	EMAC1 MCFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RESET MGMT	—	—	—	—	—	—	—	—	—	CLKSEL<3:0>				NOPRE	SCANINC	0020
2290	EMAC1 MCMD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCAN	READ	0000
22A0	EMAC1 MADR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PHYADDR<4:0>					—	—	—	REGADDR<4:0>					0100

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: Reset values default to the factory programmed value.

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TABLE 31-3: ETHERNET CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
22B0	EMAC1 MWTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MWTD<15:0>																0000
22C0	EMAC1 MRDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	MRDD<15:0>																0000
22D0	EMAC1 MIND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	LINKFAIL	NOTVALID	SCAN	MIIMBUSY	0000
2300	EMAC1 SA0(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	STNADDR6<7:0>								STNADDR5<7:0>								xxxx
2310	EMAC1 SA1(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	STNADDR4<7:0>								STNADDR3<7:0>								xxxx
2320	EMAC1 SA2(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	STNADDR2<7:0>								STNADDR1<7:0>								xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: Reset values default to the factory programmed value.

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REGISTER 31-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTV<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTV<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	TXRTS	RXEN(1)
7:0	R/W-0	U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
	AUTOFC	—	—	MANFC	—	—	—	BUFCDEC

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **PTV<15:0>:** PAUSE Timer Value bits

PAUSE Timer Value used for Flow Control.
This register should only be written when RXEN (ETHCON1<8>) is not set.

These bits are only used for Flow Control operations.

bit 15 **ON:** Ethernet ON bit

1 = Ethernet module is enabled
0 = Ethernet module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Ethernet Stop in Idle Mode bit

1 = Ethernet module transfers are paused during Idle mode
0 = Ethernet module transfers continue during Idle mode

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **TXRTS:** Transmit Request to Send bit

1 = Activate the TX logic and send the packet(s) defined in the TX EDT
0 = Stop transmit (when cleared by software) or transmit done (when cleared by hardware)

After the bit is written with a ‘1’, it will clear to a ‘0’ whenever the transmit logic has finished transmitting the requested packets in the Ethernet Descriptor Table (EDT). If a ‘0’ is written by the CPU, the transmit logic finishes the current packet’s transmission and then stops any further.

This bit only affects TX operations.

bit 8 **RXEN:** Receive Enable bit(1)

1 = Enable RX logic, packets are received and stored in the RX buffer as controlled by the filter configuration
0 = Disable RX logic, no packets are received in the RX buffer

This bit only affects RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to ‘0’), and then the RX changes applied.

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REGISTER 31-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)

bit 7 **AUTOFC:** Automatic Flow Control bit

1 = Automatic Flow Control is enabled
0 = Automatic Flow Control is disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **MANFC:** Manual Flow Control bit

1 = Manual Flow Control is enabled
0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every 128 * PTV<15:0>/2 TX clock cycles until the bit is cleared.

Note: For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **BUFCDEC:** Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

This bit is only used for RX operations.

Note 1: It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

REGISTER 31-2: ETHCON2: ETHERNET CONTROLLER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RXBUFSZ<6:4>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RXBUFSZ<3:0>				—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as ‘0’

bit 10-4 **RXBUFSZ<6:0>:** RX Data Buffer Size for All RX Descriptors (in 16-byte increments) bits

1111111 = RX data Buffer size for descriptors is 2032 bytes

•

•

•

1100000 = RX data Buffer size for descriptors is 1536 bytes

•

•

•

0000011 = RX data Buffer size for descriptors is 48 bytes
0000010 = RX data Buffer size for descriptors is 32 bytes
0000001 = RX data Buffer size for descriptors is 16 bytes
0000000 = Reserved

bit 3-0 **Unimplemented:** Read as ‘0’

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

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REGISTER 31-3: ETHTXST: ETHERNET CONTROLLER TX PACKET DESCRIPTOR START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	TXSTADDR<7:2>						—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-2 **TXSTADDR<31:2>:** Starting Address of First Transmit Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be ‘00’).

bit 1-0 **Unimplemented:** Read as ‘0’

Note 1: This register is only used for TX operations.
2: This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

REGISTER 31-4: ETHRXST: ETHERNET CONTROLLER RX PACKET DESCRIPTOR START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	RXSTADDR<7:2>						—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-2 **RXSTADDR<31:2>:** Starting Address of First Receive Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be ‘00’).

bit 1-0 **Unimplemented:** Read as ‘0’

Note 1: This register is only used for RX operations.
2: This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

REGISTER 31-5: ETHHT0: ETHERNET CONTROLLER HASH TABLE 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **HT<31:0>:** Hash Table Bytes 0-3 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

REGISTER 31-6: ETHHT1: ETHERNET CONTROLLER HASH TABLE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HT<39:32>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **HT<63:32>:** Hash Table Bytes 4-7 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

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REGISTER 31-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **PMM<31:24>:** Pattern Match Mask 3 bits
bit 23-16 **PMM<23:16>:** Pattern Match Mask 2 bits
bit 15-8 **PMM<15:8>:** Pattern Match Mask 1 bits
bit 7-0 **PMM<7:0>:** Pattern Match Mask 0 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 31-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<39:32>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **PMM<63:56>:** Pattern Match Mask 7 bits
bit 23-16 **PMM<55:48>:** Pattern Match Mask 6 bits
bit 15-8 **PMM<47:40>:** Pattern Match Mask 5 bits
bit 7-0 **PMM<39:32>:** Pattern Match Mask 4 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 31-9: ETHPMCS: ETHERNET CONTROLLER PATTERN MATCH CHECKSUM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’
bit 15-8 **PMCS<15:8>:** Pattern Match Checksum 1 bits
bit 7-0 **PMCS<7:0>:** Pattern Match Checksum 0 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 31-10: ETHPMO: ETHERNET CONTROLLER PATTERN MATCH OFFSET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’
bit 15-0 **PMO<15:0>:** Pattern Match Offset 1 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

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REGISTER 31-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HTEN	MPEN	—	NOTPM	PMMODE<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CRCERREN	CRCOKEN	RUNTERREN	RUNTEN	UCEN	NOTMEEN	MCEN	BCEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **HTEN:** Enable Hash Table Filtering bit
1 = Enable Hash Table Filtering
0 = Disable Hash Table Filtering

bit 14 **MPEN:** Magic Packet™ Enable bit
1 = Enable Magic Packet Filtering
0 = Disable Magic Packet Filtering

bit 13 **Unimplemented:** Read as ‘0’

bit 12 **NOTPM:** Pattern Match Inversion bit
1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
0 = The Pattern Match Checksum must match for a successful Pattern Match to occur
This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

bit 11-8 **PMMODE<3:0>:** Pattern Match Mode bits
1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)(1,3)
1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)(1,1)
0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)(1)
0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)(1)
0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)(1)
0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)(1)
0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)(1)
0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)(1)
0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)(1)
0000 = Pattern Match is disabled; pattern match is always unsuccessful

Note 1: XOR = True when either one or the other conditions are true, but not both.
2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

REGISTER 31-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER (CONTINUED)

bit 7 **CRCERREN:** CRC Error Collection Enable bit
1 = The received packet CRC must be invalid for the packet to be accepted
0 = Disable CRC Error Collection filtering
This bit allows the user to collect all packets that have an invalid CRC.

bit 6 **CRCOKEN:** CRC OK Enable bit
1 = The received packet CRC must be valid for the packet to be accepted
0 = Disable CRC filtering
This bit allows the user to reject all packets that have an invalid CRC.

bit 5 **RUNTERREN:** Runt Error Collection Enable bit
1 = The received packet must be a runt packet for the packet to be accepted
0 = Disable Runt Error Collection filtering

This bit allows the user to collect all packets that are runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes (when CRCOKEN = 0) or any packet with a size of less than 64 bytes that has a valid CRC (when CRCOKEN = 1).

bit 4 **RUNTEN:** Runt Enable bit
1 = The received packet must not be a runt packet for the packet to be accepted
0 = Disable Runt filtering

This bit allows the user to reject all runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes.

bit 3 **UCEN:** Unicast Enable bit
1 = Enable Unicast Filtering
0 = Disable Unicast Filtering

This bit allows the user to accept all unicast packets whose Destination Address matches the Station Address.

bit 2 **NOTMEEN:** Not Me Unicast Enable bit
1 = Enable Not Me Unicast Filtering
0 = Disable Not Me Unicast Filtering

This bit allows the user to accept all unicast packets whose Destination Address does not match the Station Address.

bit 1 **MCEN:** Multicast Enable bit
1 = Enable Multicast Filtering
0 = Disable Multicast Filtering

This bit allows the user to accept all Multicast Address packets.

bit 0 **BCEN:** Broadcast Enable bit
1 = Enable Broadcast Filtering
0 = Disable Broadcast Filtering

This bit allows the user to accept all Broadcast Address packets.

Note 1: XOR = True when either one or the other conditions are true, but not both.
2: This Hash Table Filter match is active regardless of the value of the HTEN bit.
3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

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REGISTER 31-12: ETHRXWM: ETHERNET CONTROLLER RECEIVE WATERMARKS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXFWM<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXEWM<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-16 **RXFWM<7:0>:** Receive Full Watermark bits

The software controlled RX Buffer Full Watermark Pointer is compared against the RX BUFCNT to determine the full watermark condition for the FWMARK interrupt and for enabling Flow Control when automatic Flow Control is enabled. The Full Watermark Pointer should always be greater than the Empty Watermark Pointer.

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **RXEWM<7:0>:** Receive Empty Watermark bits

The software controlled RX Buffer Empty Watermark Pointer is compared against the RX BUFCNT to determine the empty watermark condition for the EWMARK interrupt and for disabling Flow Control when automatic Flow Control is enabled. The Empty Watermark Pointer should always be less than the Full Watermark Pointer.

Note: This register is only used for RX operations.

REGISTER 31-13: ETHIEN: ETHERNET CONTROLLER INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	TXBUSEIE(1)	RXBUSEIE(2)	—	—	—	EWMARKIE(2)	FWMARKIE(2)
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONEIE(2)	PKTPENDIE(2)	RXACTIE(2)	—	TXDONEIE(1)	TXABORTIE(1)	RXBUFNAIE(2)	RXOVFLWIE(2)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14 **TXBUSEIE:** Transmit BVCI Bus Error Interrupt Enable bit(1)
1 = Enable TXBUS Error Interrupt
0 = Disable TXBUS Error Interrupt

bit 13 **RXBUSEIE:** Receive BVCI Bus Error Interrupt Enable bit(2)
1 = Enable RXBUS Error Interrupt
0 = Disable RXBUS Error Interrupt

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **EWMARKIE:** Empty Watermark Interrupt Enable bit(2)
1 = Enable EWMARK Interrupt
0 = Disable EWMARK Interrupt

bit 8 **FWMARKIE:** Full Watermark Interrupt Enable bit(2)
1 = Enable FWMARK Interrupt
0 = Disable FWMARK Interrupt

bit 7 **RXDONEIE:** Receiver Done Interrupt Enable bit(2)
1 = Enable RXDONE Interrupt
0 = Disable RXDONE Interrupt

bit 6 **PKTPENDIE:** Packet Pending Interrupt Enable bit(2)
1 = Enable PKTPEND Interrupt
0 = Disable PKTPEND Interrupt

bit 5 **RXACTIE:** RX Activity Interrupt Enable bit(2)
1 = Enable RXACT Interrupt
0 = Disable RXACT Interrupt

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **TXDONEIE:** Transmitter Done Interrupt Enable bit(1)
1 = Enable TXDONE Interrupt
0 = Disable TXDONE Interrupt

bit 2 **TXABORTIE:** Transmitter Abort Interrupt Enable bit(1)
1 = Enable TXABORT Interrupt
0 = Disable TXABORT Interrupt

bit 1 **RXBUFNAIE:** Receive Buffer Not Available Interrupt Enable bit(2)
1 = Enable RXBUFNA Interrupt
0 = Disable RXBUFNA Interrupt

bit 0 **RXOVFLWIE:** Receive FIFO Overflow Interrupt Enable bit(2)
1 = Enable RXOVFLW Interrupt
0 = Disable RXOVFLW Interrupt

Note 1: This bit is only used for TX operations.
2: This bit is only used for RX operations.

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REGISTER 31-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	TXBUSE	RXBUSE	—	—	—	EWMARK	FWMARK
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONE	PKTPEND	RXACT	—	TXDONE	TXABORT	RXBUFNA	RXOVFLW

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14 **TXBUSE:** Transmit BVCI Bus Error Interrupt bit(2)

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the TX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a ‘1’ to the CLR register.

bit 13 **RXBUSE:** Receive BVCI Bus Error Interrupt bit(2)

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the RX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a ‘1’ to the CLR register.

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **EWMARK:** Empty Watermark Interrupt bit(2)

1 = Empty Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a ‘0’ or a ‘1’ has no effect.

bit 8 **FWMARK:** Full Watermark Interrupt bit(2)

1 = Full Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a ‘0’ or a ‘1’ has no effect.

Note 1: This bit is only used for TX operations.
2: This bit is are only used for RX operations.

Note: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 31-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

bit 7 **RXDONE:** Receive Done Interrupt bit(2)

1 = RX packet was successfully received
0 = No interrupt pending

This bit is set whenever an RX packet is successfully received. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 6 **PKTPEND:** Packet Pending Interrupt bit(2)

1 = RX packet pending in memory
0 = RX packet is not pending in memory

This bit is set when the BUFCNT counter has a value other than '0'. It is cleared by either a Reset or by writing the BUFCDEC bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 5 **RXACT:** Receive Activity Interrupt bit(2)

1 = RX packet data was successfully received
0 = No interrupt pending

This bit is set whenever RX packet data is stored in the RXBM FIFO. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONE:** Transmit Done Interrupt bit(2)

1 = TX packet was successfully sent
0 = No interrupt pending

This bit is set when the currently transmitted TX packet completes transmission, and the Transmit Status Vector is loaded into the first descriptor used for the packet. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 2 **TXABORT:** Transmit Abort Condition Interrupt bit(2)

1 = TX abort condition occurred on the last TX packet
0 = No interrupt pending

This bit is set when the MAC aborts the transmission of a TX packet for one of the following reasons:

- Jumbo TX packet abort
- Underrun abort
- Excessive defer abort
- Late collision abort
- Excessive collisions abort

This bit is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 1 **RXBUFNA:** Receive Buffer Not Available Interrupt bit(2)

1 = RX Buffer Descriptor Not Available condition has occurred
0 = No interrupt pending

This bit is set by a RX Buffer Descriptor Overrun condition. It is cleared by either a Reset or a CPU write of a '1' to the CLR register.

bit 0 **RXOVFLW:** Receive FIFO Over Flow Error bit(2)

1 = RX FIFO Overflow Error condition has occurred
0 = No interrupt pending

RXOVFLW is set by the RXBM Logic for an RX FIFO Overflow condition. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

Note 1: This bit is only used for TX operations.
2: This bit is are only used for RX operations.

Note:	It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

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REGISTER 31-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFCNT<7:0>(1)							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ETHBUSY(5)	TXBUSY(2,6)	RXBUSY(3,6)	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits(1)

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

Note: BUFCNT will not be cleared when ON is set to ‘0’. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **ETHBUSY:** Ethernet Module busy bit(4,5)

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction
0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

Note 1: This bit is only used for RX operations.
2: This bit is only affected by TX operations.
3: This bit is only affected by RX operations.
4: This bit is affected by TX and RX operations.
5: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
6: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

REGISTER 31-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER (CONTINUED)

bit 6 **TXBUSY:** Transmit Busy bit(2,6)

1 = TX logic is receiving data
0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

bit 5 **RXBUSY:** Receive Busy bit(3,6)

1 = RX logic is receiving data
0 = RX logic is idle

This bit indicates that a packet is currently being received. A change in this status bit is not necessarily reflected by the RXDONE interrupt, as RX packets may be aborted or rejected by the RX filter.

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is only used for RX operations.
2: This bit is only affected by TX operations.
3: This bit is only affected by RX operations.
4: This bit is affected by TX and RX operations.
5: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
6: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

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REGISTER 31-16: ETHRXOVFLOW: ETHERNET CONTROLLER RECEIVE OVERFLOW STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXOVFLWCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **RXOVFLWCNT<15:0>:** Dropped Receive Frames Count bits

Increment counter for frames accepted by the RX filter and subsequently dropped due to internal receive error (RXFIFO overrun). This event also sets the RXOVFLW bit (ETHIRQ<0>) interrupt flag.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are ‘0’.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 31-17: ETHFRMTXOK: ETHERNET CONTROLLER FRAMES TRANSMITTED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMTXOKCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **FRMTXOKCNT<15:0>:** Frame Transmitted OK Count bits
Increment counter for frames successfully transmitted.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are ‘0’.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

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REGISTER 31-18: ETHSCOLFRM: ETHERNET CONTROLLER SINGLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCOLFRMCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **SCOLFRMCNT<15:0>:** Single Collision Frame Count bits
Increment count for frames that were successfully transmitted on the second try.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are ‘0’.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 31-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits
Increment count for frames that were successfully transmitted after there was more than one collision.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are ‘0’.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

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REGISTER 31-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMRXOKCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are ‘0’.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 31-21: ETHFCSERR: ETHERNET CONTROLLER FRAME CHECK SEQUENCE ERROR STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FCSERRCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FCSERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **FCSERRCNT<15:0>:** FCS Error Count bits

Increment count for frames received with FCS error and the frame length in bits is an integral multiple of 8 bits.

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are ‘0’.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

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REGISTER 31-22: ETHALGNERR: ETHERNET CONTROLLER ALIGNMENT ERRORS STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **ALGNERRCNT<15:0>:** Alignment Error Count bits

Increment count for frames with alignment errors. Note that an alignment error is a frame that has an FCS error and the frame length in bits is not an integral multiple of 8 bits (also known as dribble nibble)

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are ‘0’.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

REGISTER 31-23: EMAC1CFG1: ETHERNET CONTROLLER MAC CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	SOFT RESET	SIM RESET	—	—	RESET RMCS	RESET RFUN	RESET TMCS	RESET TFUN
7:0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
	—	—	—	LOOPBACK	TX PAUSE	RX PAUSE	PASSALL	RX ENABLE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **SOFTRESET:** Soft Reset bit
Setting this bit will put the MACMII in reset. Its default value is ‘1’.

bit 14 **SIMRESET:** Simulation Reset bit
Setting this bit will cause a reset to the random number generator within the Transmit Function.

bit 13-12 **Unimplemented:** Read as ‘0’

bit 11 **RESETRMCS:** Reset MCS/RX bit
Setting this bit will put the MAC Control Sub-layer/Receive domain logic in reset.

bit 10 **RESETRFUN:** Reset RX Function bit
Setting this bit will put the MAC Receive function logic in reset.

bit 9 **RESETTMCS:** Reset MCS/TX bit
Setting this bit will put the MAC Control Sub-layer/TX domain logic in reset.

bit 8 **RESETTFUN:** Reset TX Function bit
Setting this bit will put the MAC Transmit function logic in reset.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **LOOPBACK:** MAC Loopback mode bit
1 = MAC Transmit interface is loop backed to the MAC Receive interface
0 = MAC normal operation

bit 3 **TXPAUSE:** MAC TX Flow Control bit
1 = PAUSE Flow Control frames are allowed to be transmitted
0 = PAUSE Flow Control frames are blocked

bit 2 **RXPAUSE:** MAC RX Flow Control bit
1 = The MAC acts upon received PAUSE Flow Control frames
0 = Received PAUSE Flow Control frames are ignored

bit 1 **PASSALL:** MAC Pass all Receive Frames bit
1 = The MAC will accept all frames regardless of type (Normal vs. Control)
0 = The received Control frames are ignored

bit 0 **RXENABLE:** MAC Receive Enable bit
1 = Enable the MAC receiving of frames
0 = Disable the MAC receiving of frames

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 31-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 25/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	EXCESS DFR	BPNOBK OFF	NOBK OFF	—	—	LONGPRE	PUREPRE
7:0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	AUTO PAD(1,2)	VLAN PAD(1,2)	PAD ENABLE(1,3)	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14 **EXCESSDER:** Excess Defer bit

1 = The MAC will defer to carrier indefinitely as per the Standard
0 = The MAC will abort when the excessive deferral limit is reached

bit 13 **BPNOBKOFF:** Backpressure/No Backoff bit

1 = The MAC after incidentally causing a collision during backpressure will immediately retransmit without backoff reducing the chance of further collisions and ensuring transmit packets get sent
0 = The MAC will not remove the backoff

bit 12 **NOBKOFF:** No Backoff bit

1 = Following a collision, the MAC will immediately retransmit rather than using the Binary Exponential Back-off algorithm as specified in the Standard
0 = Following a collision, the MAC will use the Binary Exponential Backoff algorithm

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9 **LONGPRE:** Long Preamble Enforcement bit

1 = The MAC only allows receive packets which contain preamble fields less than 12 bytes in length
0 = The MAC allows any length preamble as per the Standard

bit 8 **PUREPRE:** Pure Preamble Enforcement bit

1 = The MAC will verify the content of the preamble to ensure it contains 0x55 and is error-free. A packet with errors in its preamble is discarded
0 = The MAC does not perform any preamble checking

bit 7 **AUTOPAD:** Automatic Detect Pad Enable bit(1,2)

1 = The MAC will automatically detect the type of frame, either tagged or untagged, by comparing the two octets following the source address with 0x8100 (VLAN Protocol ID) and pad accordingly
0 = The MAC does not perform automatic detection

Note 1: Table 31-4 provides a description of the pad function based on the configuration of this register.
2: This bit is ignored if the PADENABLE bit is cleared.
3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

REGISTER 31-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

bit 6 **VLANPAD:** VLAN Pad Enable bit(1,2)

1 = The MAC will pad all short frames to 64 bytes and append a valid CRC
0 = The MAC does not perform padding of short frames

bit 5 **PADENABLE:** Pad/CRC Enable bit(1,3)

1 = The MAC will pad all short frames
0 = The frames presented to the MAC have a valid length

bit 4 **CRCENABLE:** CRC Enable1 bit

1 = The MAC will append a CRC to every frame whether padding was required or not. Must be set if the PADENABLE bit is set.
0 = The frames presented to the MAC have a valid CRC

bit 3 **DELAYCRC:** Delayed CRC bit

This bit determines the number of bytes, if any, of proprietary header information that exist on the front of the IEEE 802.3 frames.

1 = Four bytes of header (ignored by the CRC function)
0 = No proprietary header

bit 2 **HUGEFRM:** Huge Frame enable bit

1 = Frames of any length are transmitted and received
0 = Huge frames are not allowed for receive or transmit

bit 1 **LENGTHCK:** Frame Length checking bit

1 = Both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the transmit/receive statistics vector.
0 = Length/Type field check is not performed

bit 0 **FULLDPLX:** Full-Duplex Operation bit

1 = The MAC operates in Full-Duplex mode
0 = The MAC operates in Half-Duplex mode

Note 1: Table 31-4 provides a description of the pad function based on the configuration of this register.
2: This bit is ignored if the PADENABLE bit is cleared.
3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

TABLE 31-4: PAD OPERATION

Type	AUTOPAD	VLANPAD	PADENABLE	Action
Any	x	x	0	No pad, check CRC
Any	0	0	1	Pad to 60 Bytes, append CRC
Any	x	1	1	Pad to 64 Bytes, append CRC
Any	1	0	1	If untagged: Pad to 60 Bytes, append CRC If VLAN tagged: Pad to 64 Bytes, append CRC

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REGISTER 31-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	B2BIPKTGP<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-7 **Unimplemented:** Read as ‘0’

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 31-26: EMAC1IPGR: ETHERNET CONTROLLER MAC NON-BACK-TO-BACK INTERPACKET GAP REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
	—	NB2BIPKTGP1<6:0>						
7:0	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
	—	NB2BIPKTGP2<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14-8 **NB2BIPKTGP1<6:0>:** Non-Back-to-Back Interpacket Gap Part 1 bits

This is a programmable field representing the optional carrierSense window referenced in section 4.2.3.2.1 “Deference” of the IEEE 80.23 Specification. If carrier is detected during the timing of IPGR1, the MAC defers to carrier. If, however, carrier becomes after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision, thus ensuring fair access to medium. Its range of values is 0x0 to IPGR2. Its recommend value is 0xC (12d).

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **NB2BIPKTGP2<6:0>:** Non-Back-to-Back Interpacket Gap Part 2 bits

This is a programmable field representing the non-back-to-back Inter-Packet-Gap. Its recommended value is 0x12 (18d), which represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps).

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 31-27: EMAC1CLRT: ETHERNET CONTROLLER MAC COLLISION WINDOW/RETRY LIMIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	CWINDOW<5:0>					
7:0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	—	RETX<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as ‘0’

bit 13-8 **CWINDOW<5:0>:** Collision Window bits

This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **RETX<3:0>:** Retransmission Maximum bits

This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts (attemptLimit) to be 0xF (15d). Its default is ‘0xF’.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 31-28: EMAC1MAXF: ETHERNET CONTROLLER MAC MAXIMUM FRAME LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	MACMAXF<15:8>(1)							
7:0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
	MACMAXF<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **MACMAXF<15:0>:** Maximum Frame Length bits(1)

These bits reset to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter/longer maximum length restriction is desired, program this 16-bit field.

Note 1: If a proprietary header is allowed, this bit should be adjusted accordingly. For example, if 4-byte headers are prepended to frames, MACMAXF could be set to 1527 octets. This would allow the maximum VLAN tagged frame plus the 4-byte header.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 31-29: EMAC1SUPP: ETHERNET CONTROLLER MAC PHY SUPPORT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
	—	—	—	—	RESETRMII(1)	—	—	SPEEDRMII(1)
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as ‘0’

bit 11 **RESETRMII:** Reset RMII Logic bit(1)
1 = Reset the MAC RMII module
0 = Normal operation.

bit 10-9 **Unimplemented:** Read as ‘0’

bit 8 **SPEEDRMII:** RMII Speed bit(1)
This bit configures the Reduced MII logic for the current operating speed.
1 = RMII is running at 100 Mbps
0 = RMII is running at 10 Mbps

bit 7-0 **Unimplemented:** Read as ‘0’

Note 1: This bit is only used for the RMII module.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 31-30: EMAC1TEST: ETHERNET CONTROLLER MAC TEST REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TESTBP	TESTPAUSE(1)	SHRTQNTA(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as ‘0’

bit 2 **TESTBP:** Test Backpressure bit

1 = The MAC will assert backpressure on the link. Backpressure causes preamble to be transmitted, raising carrier sense. A transmit packet from the system will be sent during backpressure.

0 = Normal operation

bit 1 **TESTPAUSE:** Test PAUSE bit(1)

1 = The MAC Control sub-layer will inhibit transmissions, just as if a PAUSE Receive Control frame with a non-zero pause time parameter was received

0 = Normal operation

bit 0 **SHRTQNTA:** Shortcut PAUSE Quanta bit(1)

1 = The MAC reduces the effective PAUSE Quanta from 64 byte-times to 1 byte-time

0 = Normal operation

Note 1: This bit is only used for testing purposes.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 31-31: EMAC1MCFG: ETHERNET CONTROLLER MAC MII MANAGEMENT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RESETMGMT	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLKSEL<3:0>(1)				NOPRE	SCANINC

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **RESETMGMT:** Test Reset MII Management bit
1 = Reset the MII Management module
0 = Normal Operation

bit 14-6 **Unimplemented:** Read as ‘0’

bit 5-2 **CLKSEL<3:0>:** MII Management Clock Select 1 bits(1)
These bits are used by the clock divide logic in creating the MII Management Clock (MDC), which the IEEE 802.3 Specification defines to be no faster than 2.5 MHz. Some PHYs support clock rates up to 12.5 MHz.

bit 1 **NOPRE:** Suppress Preamble bit
1 = The MII Management will perform read/write cycles without the 32-bit preamble field. Some PHYs support suppressed preamble
0 = Normal read/write cycles are performed

bit 0 **SCANINC:** Scan Increment bit
1 = The MII Management module will perform read cycles across a range of PHYs. The read cycles will start from address 1 through the value set in EMAC1MADR<PHYADDR>
0 = Continuous reads of the same PHY

Note 1: Table 31-5 describes the clock divider encoding.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE 31-5: MIIM CLOCK SELECTION

MIIM Clock Select	EMAC1MCFG<5:2>
TPBCLK5 divided by 4	000x
TPBCLK5 divided by 6	0010
TPBCLK5 divided by 8	0011
TPBCLK5 divided by 10	0100
TPBCLK5 divided by 14	0101
TPBCLK5 divided by 20	0110
TPBCLK5 divided by 28	0111
TPBCLK5 divided by 40	1000
TPBCLK5 divided by 48	1001
TPBCLK5 divided by 50	1010
Undefined	Any other combination

REGISTER 31-32: EMAC1MCMD: ETHERNET CONTROLLER MAC MII MANAGEMENT COMMAND REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SCAN	READ

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-2 **Unimplemented:** Read as ‘0’

bit 1 **SCAN:** MII Management Scan Mode bit
- 1 = The MII Management module will perform read cycles continuously (for example, useful for monitoring the Link Fail)
- 0 = Normal Operation

bit 0 **READ:** MII Management Read Command bit
- 1 = The MII Management module will perform a single read cycle. The read data is returned in the EMAC1MRDD register
- 0 = The MII Management module will perform a write cycle. The write data is taken from the EMAC1MWTD register

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 31-33: EMAC1MADR: ETHERNET CONTROLLER MAC MII MANAGEMENT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	—	—	—	PHYADDR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	REGADDR<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ’0’

bit 12-8 **PHYADDR<4:0>:** MII Management PHY Address bits

This field represents the 5-bit PHY Address field of Management cycles. Up to 31 PHYs can be addressed (0 is reserved).

bit 7-5 **Unimplemented:** Read as ’0’

bit 4-0 **REGADDR<4:0>:** MII Management Register Address bits

This field represents the 5-bit Register Address field of Management cycles. Up to 32 registers can be accessed.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 31-34: EMAC1MWTD: ETHERNET CONTROLLER MAC MII MANAGEMENT WRITE DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MWTD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MWTD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ’0’

bit 15-0 **MWTD<15:0>:** MII Management Write Data bits

When written, a MII Management write cycle is performed using the 16-bit data and the preconfigured PHY and Register addresses from the EMAC1MADR register.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 31-35: EMAC1MRDD: ETHERNET CONTROLLER MAC MII MANAGEMENT READ DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MRDD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MRDD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **MRDD<15:0>:** MII Management Read Data bits

Following a MII Management Read Cycle, the 16-bit data can be read from this location.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

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REGISTER 31-36: EMAC1MIND: ETHERNET CONTROLLER MAC MII MANAGEMENT INDICATORS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	LINKFAIL	NOTVALID	SCAN	MIIMBUSY

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3 **LINKFAIL:** Link Fail bit

When ‘1’ is returned - indicates link fail has occurred. This bit reflects the value last read from the PHY status register.

bit 2 **NOTVALID:** MII Management Read Data Not Valid bit

When ‘1’ is returned - indicates an MII management read cycle has not completed and the Read Data is not yet valid.

bit 1 **SCAN:** MII Management Scanning bit

When ‘1’ is returned - indicates a scan operation (continuous MII Management Read cycles) is in progress.

bit 0 **MIIMBUSY:** MII Management Busy bit

When ‘1’ is returned - indicates MII Management module is currently performing an MII Management Read or Write cycle.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

REGISTER 31-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR6<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR5<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits
These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits
These bits hold the fifth transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

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REGISTER 31-38: EMAC1SA1: ETHERNET CONTROLLER MAC STATION ADDRESS 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR4<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR3<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-8 **STNADDR4<7:0>:** Station Address Octet 4 bits
These bits hold the fourth transmitted octet of the station address.

bit 7-0 **STNADDR3<7:0>:** Station Address Octet 3 bits
These bits hold the third transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

REGISTER 31-39: EMAC1SA2: ETHERNET CONTROLLER MAC STATION ADDRESS 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR2<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR1<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Maintain as ‘0’; ignore read

bit 15-8 **STNADDR2<7:0>:** Station Address Octet 2 bits
These bits hold the second transmitted octet of the station address.

bit 7-0 **STNADDR1<7:0>:** Station Address Octet 1 bits
These bits hold the most significant (first transmitted) octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

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32.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

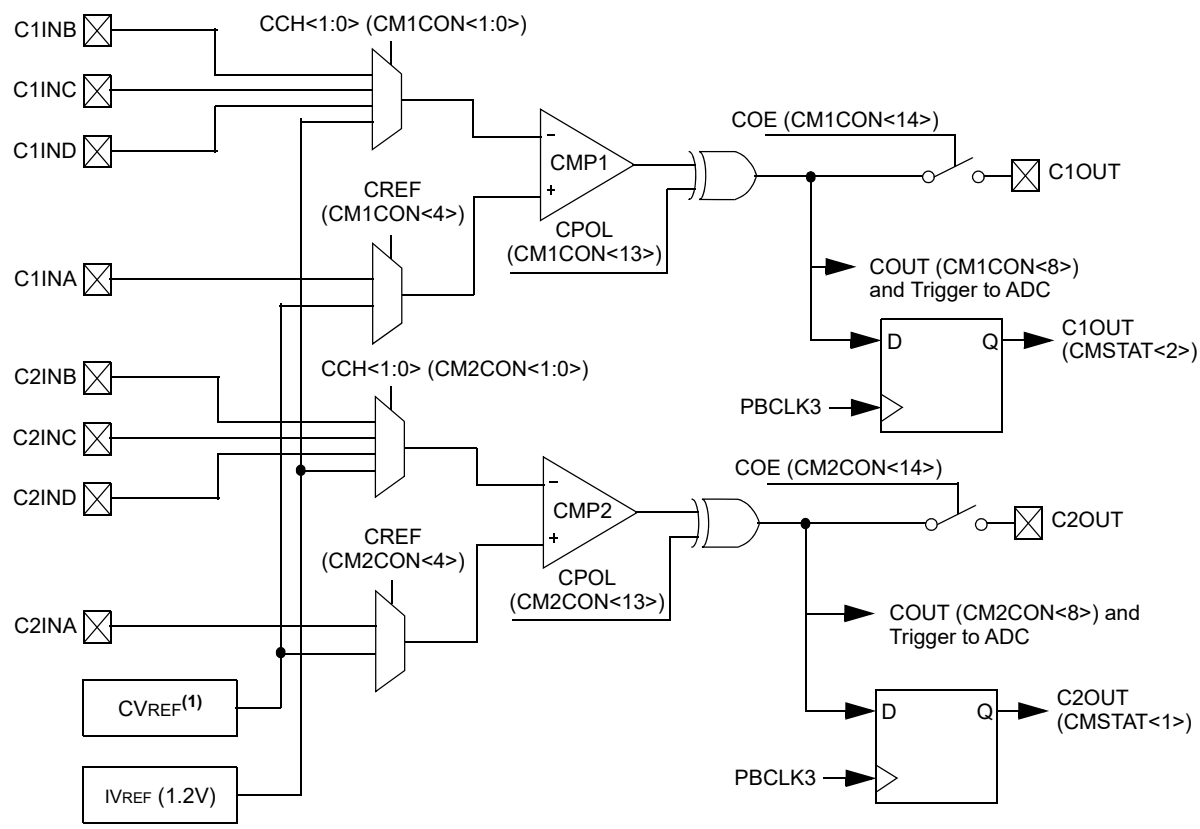
The Analog Comparator module consists of two comparators that can be configured in a variety of ways.

The following are key features of the Analog Comparator module:

- Differential inputs
- Rail-to-rail operation
- Selectable output polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference
  - Comparator voltage reference (CVREF)
- Selectable interrupt generation

A block diagram of the comparator module is illustrated in Figure 32-1.

FIGURE 32-1: COMPARATOR BLOCK DIAGRAM



Note 1: Internally connected. See **Section 33.0 "Comparator Voltage Reference (CVREF)"** for more information.

32.1 Comparator Control Registers

TABLE 32-1: COMPARATOR REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
C010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
C060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 32-1: CMxCON: COMPARATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON	COE	CPOL(1)	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25-24 **Unimplemented:** Read as ‘0’

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Comparator ON bit
- 1 = Module is enabled. Setting this bit does not affect the other bits in this register
- 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit
- 1 = Comparator output is driven on the output CxOUT pin
- 0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit(1)
- 1 = Output is inverted
- 0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as ‘0’

bit 8 **COUT:** Comparator Output bit
- 1 = Output of the Comparator is a ‘1’
- 0 = Output of the Comparator is a ‘0’

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
- 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
- 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
- 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
- 00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **CREF:** Comparator Positive Input Configure bit
- 1 = Comparator non-inverting input is connected to the internal CVREF
- 0 = Comparator non-inverting input is connected to the CxINA pin

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator
- 11 = Comparator inverting input is connected to the IVREF
- 10 = Comparator inverting input is connected to the CxIND pin
- 01 = Comparator inverting input is connected to the CxINC pin
- 00 = Comparator inverting input is connected to the CxINB pin

Note 1: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

REGISTER 32-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	C2OUT	C1OUT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in IDLE Control bit
1 = All Comparator modules are disabled in IDLE mode
0 = All Comparator modules continue to operate in the IDLE mode

bit 12-2 **Unimplemented:** Read as ‘0’

bit 1 **C2OUT:** Comparator Output bit
1 = Output of Comparator 2 is a ‘1’
0 = Output of Comparator 2 is a ‘0’

bit 0 **C1OUT:** Comparator Output bit
1 = Output of Comparator 1 is a ‘1’
0 = Output of Comparator 1 is a ‘0’

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33.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

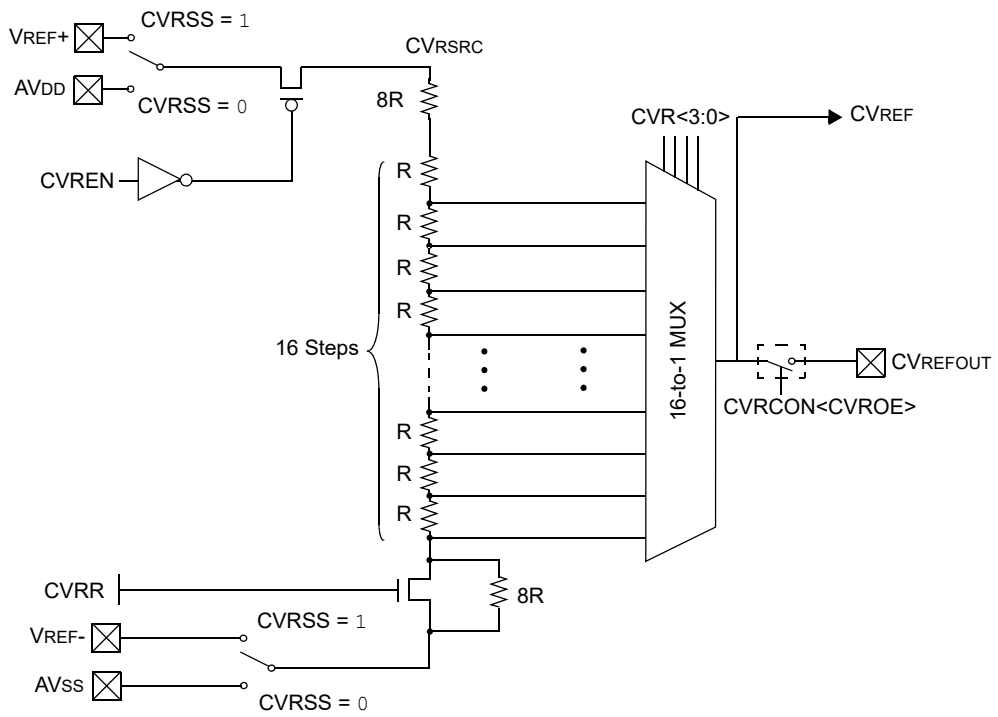
The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDDIO/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The comparator voltage reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

A block diagram of the CVREF module is illustrated in Figure 33-1.

FIGURE 33-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



33.1 Comparator Voltage Reference Control Registers

TABLE 33-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0E00	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 33-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON	—	—	—	—	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	CVROE	CVRR	CVRSS	CVR<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Comparator Voltage Reference On bit
1 = Module is enabled
Setting this bit does not affect other bits in the register.
0 = Module is disabled and does not consume current.
Clearing this bit does not affect the other bits in the register.

bit 14-7 **Unimplemented:** Read as ‘0’

bit 6 **CVROE:** CV_{REFOUT} Enable bit
1 = Voltage level is output on CV_{REFOUT} pin
0 = Voltage level is disconnected from CV_{REFOUT} pin

bit 5 **CVRR:** CV_{REF} Range Selection bit
1 = 0 to 0.67 CV_{RSRC}, with CV_{RSRC}/24 step size
0 = 0.25 CV_{RSRC} to 0.75 CV_{RSRC}, with CV_{RSRC}/32 step size

bit 4 **CVRSS:** CV_{REF} Source Selection bit
1 = Comparator voltage reference source, $CV_{RSRC} = (V_{REF}+) – (V_{REF}-)$
0 = Comparator voltage reference source, $CV_{RSRC} = AV_{DD} – AV_{SS}$

bit 3-0 **CVR<3:0>:** CV_{REF} Value Selection $0 \leq CVR<3:0> \leq 15$ bits
When CVRR = 1:
$CV_{REF} = (CVR<3:0>/24) \bullet (CV_{RSRC})$
When CVRR = 0:
$CV_{REF} = 1/4 \bullet (CV_{RSRC}) + (CVR<3:0>/32) \bullet (CV_{RSRC})$

NOTES:

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34.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

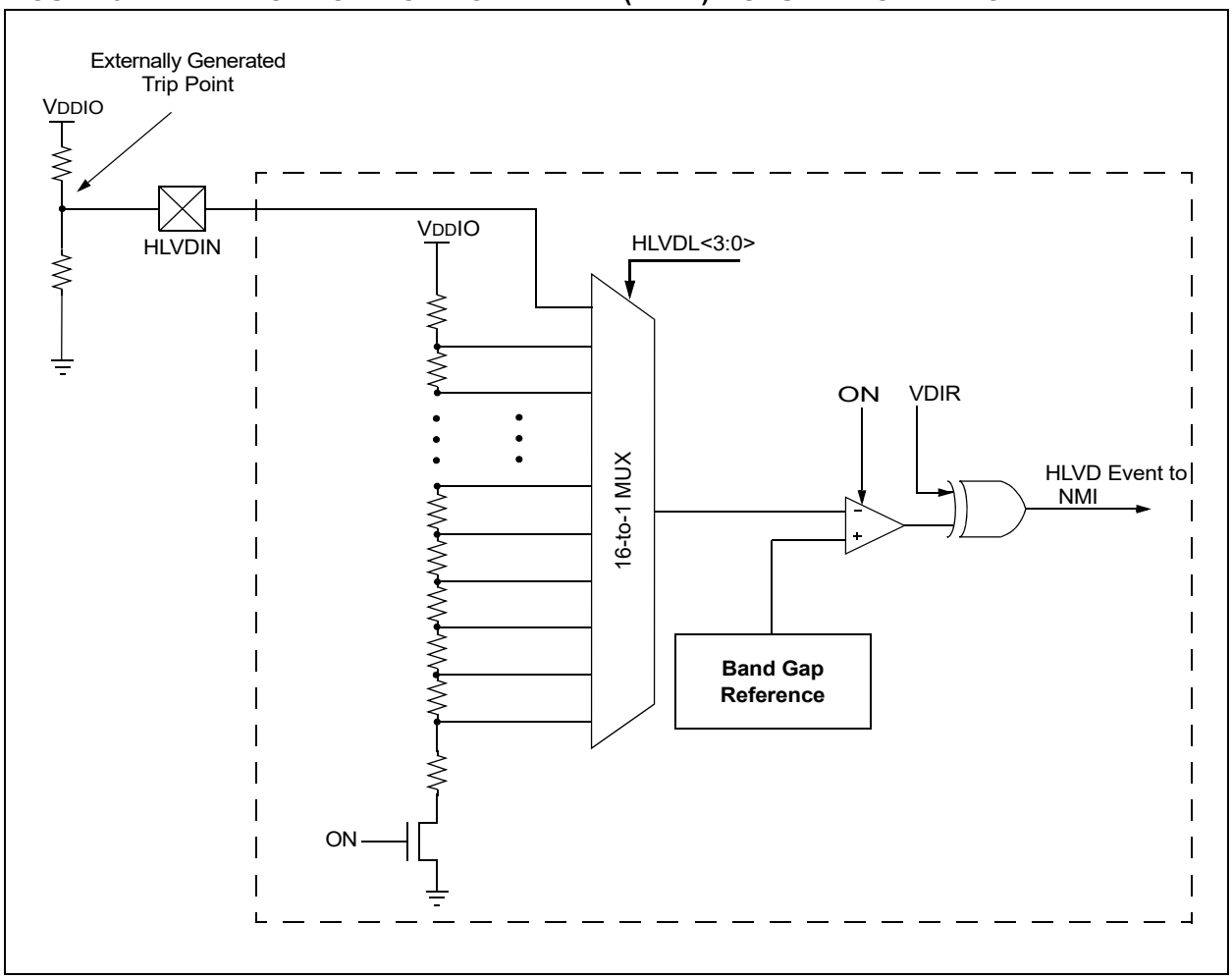
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 38. "High/Low-Voltage Detect (HLVD)"** (DS60001408), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

The HLVD module provides the following features:

- Hysteresis detection
- Low-to-high or high-to-low voltage change detection
- Generation of Non-Maskable Interrupts (NMI)
- LVDIN pin to provide external voltage trip point

FIGURE 34-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



34.1 Control Registers

TABLE 34-1: HIGH/LOW-VOLTAGE DETECT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1800	HLVDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	VDIR	BGVST	—	HLEVT	HLEVTOUTDIS	—	—	—	HLVDL<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 34-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	R/W-0	HS,HC,R-0	r-1	HS,HC,R-0
	ON	—	—	—	VDIR	BGVST	—	HLEVT
7:0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	HLEVTOUTDIS(2)	—	—	—	HLVDL<3:0>(1)			

Legend:	HS = Hardware Set	HC = Hardware Cleared	r = Reserved bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** HLVD Module Enable bit
1 = HLVD module is enabled
0 = HLVD module is disabled

bit 14-12 **Unimplemented:** Read as ‘0’

bit 11 **VDIR:** Voltage Change Direction Select bit
1 = Event occurs when voltage equals or exceeds the trip point (HLVDL<3:0>)
0 = Event occurs when voltage equals or falls below the trip point (HLVDL<3:0>)

bit 10 **BGVST:** Band Gap Reference Voltages Stable Status bit
1 = Indicates internal band gap voltage references is stable
0 = Indicates internal band gap voltage reference is not stable
This bit is readable when the HLVD module is disabled (ON = 0).

bit 9 **Reserved:** Read as ‘1’

bit 8 **HLEVT:** High/Low-Voltage Detection Event Status bit
1 = Indicates HLVD Event is active
0 = Indicates HLVD Event is not active

bit 7 **HLEVTOUTDIS:** High/Low-Voltage Detection Event Output Disable bit(2)
1 = Enables HLVD Event output
0 = Disable HLVD Event output

bit 6-4 **Unimplemented:** Read as ‘0’

Note 1: To avoid false HLVD events, all HLVD module setting changes should occur only when the module is disabled (ON = 0). See Table 44-6 in **44.0 “Electrical Characteristics”** for the actual trip points.

2: Once this bit is set to '1', it can only be cleared by disabling or enabling the HLVD module (or through the HLVDMD bit).

REGISTER 34-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit Select bits(1)

1111 = Selects analog input on HLVDIN
1110 = Reserved; do not use
1101 = Reserved; do not use
1100 = Reserved; do not use
1011 = Selects trip point 11
1010 = Selects trip point 10
1001 = Selects trip point 9
1000 = Selects trip point 8
0111 = Selects trip point 7
0110 = Selects trip point 6
0101 = Selects trip point 5
0100 = Selects trip point 4
0011 = Reserved; do not use
0010 = Reserved; do not use
0001 = Reserved; do not use
0000 = Reserved; do not use

Note 1: To avoid false HLVD events, all HLVD module setting changes should occur only when the module is disabled (ON = 0). See Table 44-6 in **44.0 "Electrical Characteristics"** for the actual trip points.

2: Once this bit is set to '1', it can only be cleared by disabling or enabling the HLVD module (or through the HLVDMD bit).

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35.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

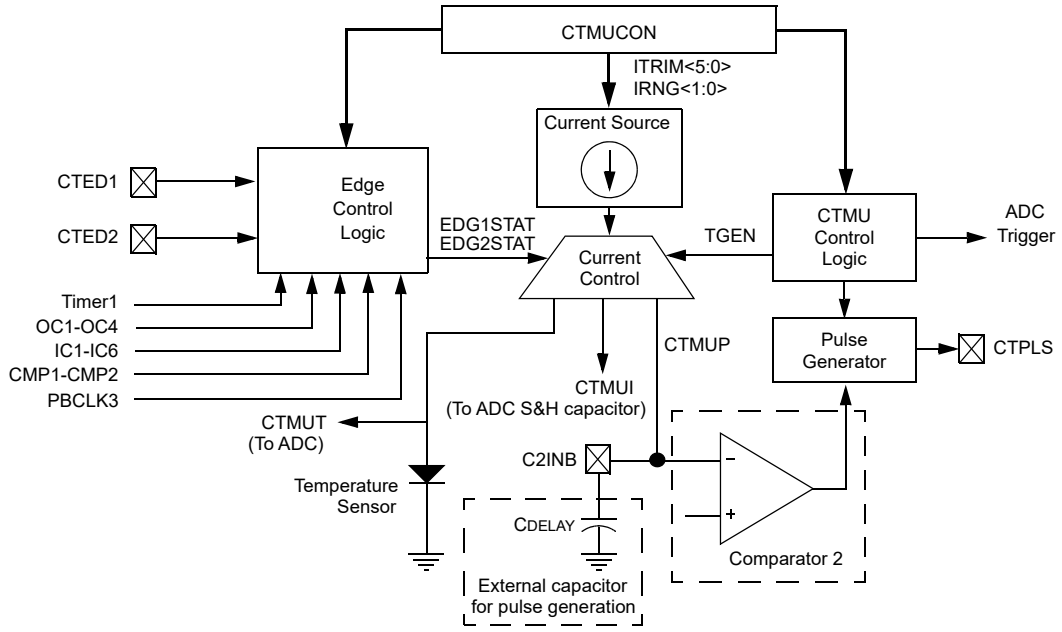
The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Up to 35 channels available for capacitive or time measurement input (AN5 to AN39)
- On-chip precision current source
- 16-edge input trigger sources
- Selection of edge or level-sensitive inputs
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- Control of current source during auto-sampling
- Four current source ranges
- Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 35-1.

FIGURE 35-1: CTMU BLOCK DIAGRAM



Current Control Selection	TGEN	EDG1STAT, EDG2STAT
CTMUT	0	EDG1STAT = EDG2STAT
CTMUI	0	EDG1STAT ≠ EDG2STAT
CTMUP	1	EDG1STAT ≠ EDG2STAT
No Connect	1	EDG1STAT = EDG2STAT

35.1 CTMU Control Registers

TABLE 35-1: CTMU REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C200	CTMUCON	31:16	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
		15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	ITRIM<5:0>						IRNG<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

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REGISTER 35-1: CTMUCON: CTMU CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	CTMUSIDL	TGEN(1)	EDGEN	EDGSEQEN	IDISSEN(2)	CTTRIG
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ITRIM<5:0>						IRNG<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **EDG1MOD:** Edge1 Edge Sampling Select bit
- 1 = Input is edge-sensitive
- 0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit
- 1 = Edge1 programmed for a positive edge response
- 0 = Edge1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits
- 1111 = Reserved
- 1110 = C2OUT pin is selected
- 1101 = C1OUT pin is selected
- 1100 = IC6 Capture Event is selected
- 1011 = IC5 Capture Event is selected
- 1010 = IC4 Capture Event is selected
- 1001 = IC3 Capture Event is selected
- 1000 = IC2 Capture Event is selected
- 0111 = IC1 Capture Event is selected
- 0110 = OC4 Capture Event is selected
- 0101 = OC3 Capture Event is selected
- 0100 = OC2 Capture Event is selected
- 0011 = CTED1 pin is selected
- 0010 = CTED2 pin is selected
- 0001 = OC1 Compare Event is selected
- 0000 = Timer1 Event is selected

bit 25 **EDG2STAT:** Edge2 Status bit

Indicates the status of Edge2 and can be written to control edge source
- 1 = Edge2 has occurred
- 0 = Edge2 has not occurred

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<2:0> bits must be set to ‘1110’ to select the C2OUT pin.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to ‘1’, performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 44-19) in **Section 44.0 “Electrical Characteristics”** for current values.

4: This bit setting is not available for the CTMU temperature diode.

REGISTER 35-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 24 **EDG1STAT:** Edge1 Status bit
Indicates the status of Edge1 and can be written to control edge source
1 = Edge1 has occurred
0 = Edge1 has not occurred

bit 23 **EDG2MOD:** Edge2 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 22 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge2 programmed for a positive edge response
0 = Edge2 programmed for a negative edge response

bit 21-18 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = Reserved
1110 = C2OUT pin is selected
1101 = C1OUT pin is selected
1100 = PBCLK3
1011 = IC5 Capture Event is selected
1010 = IC4 Capture Event is selected
1001 = IC3 Capture Event is selected
1000 = IC2 Capture Event is selected
0111 = IC1 Capture Event is selected
0110 = OC4 Capture Event is selected
0101 = OC3 Capture Event is selected
0100 = OC2 Capture Event is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 17-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ON Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** Stop-in-Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit(1)
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge1 must occur before Edge2 can occur
0 = No edge sequence is needed

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<2:0> bits must be set to '1110' to select the C2OUT pin.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 44-19) in **Section 44.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

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REGISTER 35-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
`1` = Analog current source output is grounded
`0` = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
`1` = Trigger output is enabled
`0` = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
`011111` = Maximum positive change from nominal current
`011110`
•
•
•
`000001` = Minimum positive change from nominal current
`000000` = Nominal current output specified by IRNG<1:0>
`111111` = Minimum negative change from nominal current
•
•
•
`100010`
`100001` = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
`11` = 100 times base current
`10` = 10 times base current
`01` = Base current level
`00` = 1000 times base current(4)

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<2:0> bits must be set to '`1110`' to select the C2OUT pin.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '`1`', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 44-19) in **Section 44.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

NOTES:

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36.0 GRAPHICS LCD (GLCD) CONTROLLER

Note 1: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 54. "Graphics LCD Controller"** (DS60001379), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The Graphics LCD (GLCD) Controller is designed to directly interface with display panels with up to 24-bit color depth.

The GLCD Controller transfers display data from a memory device and formats it for a display device. The memory may be internal RAM or DDR2.

The parallel interface at the pins will operate at standard 3.3V output, requires 28 pins for 24-bit color, and is shared by general purpose I/O functions.

Key features of the GLCD Controller include:

- Supports up to a 50 MHz Pixel Clock (dependent on DDR2 bandwidth and GLCD system BUS bandwidth)
- Up to 800x480 (WVGA) with Overlay and smaller with three Overlay layers. High resolution is possible with smaller displays.
- Color depths: 8-bit, 16-bit, 18-bit, and 24-bit

  Note: 16-bit color depth is supported through the GLCDMODE bit (CFGCON2<30>). When set, functions shared with GD0, GD1, GD2, GD8, GD9, GD16, GD17, GD18 are available for general purpose use.
- Up to three design timing layers, each including:
  - Configurable Alpha blending
  - Configurable Stride and Pitch
- Input formats: RGBA8888, ARGB8888, RGB888, RGB565, RGBA5551, YUYV, RGB332, LUT8, and Gray-scale
- Output formats: RGB888, RGB666, BT.656
- Dithering for 18-bit displays
- High-quality YUV conversion
- Global color palette look-up table (CLUT) supporting 256 colors
- Global gamma correction, brightness and contrast support
- Programmable cursors supporting 16 colors
- Programmable polarity on HSYNC, VSYNC, DE, and PCLK
- Integrated DMA to offload the CPU
- Programmable (level/edge) interrupt on HSYNC and VSYNC

The following table provides the RGB color mapping in 16 bit and 24 bit modes with GLCD output signals.

TABLE 36-1:RGB COLOR MAPPING

GLCD signal on pin	GD23	GD22	GD21	GD20	GD19	GD18	GD17	GD16	GD15	GD14	GD13	GD12	GD11	GD10	GD9	GD8	GD7	GD6	GD5	GD4	GD3	GD2	GD1	GD0
24 bit color	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0
16 bit color	B7	B6	B5	B4	B3	x	x	x	G7	G6	G5	G4	G3	G2	x	x	R7	R6	R5	R4	R3	x	x	x

Figure 36-1 shows a block diagram of the GLCD Controller interface.

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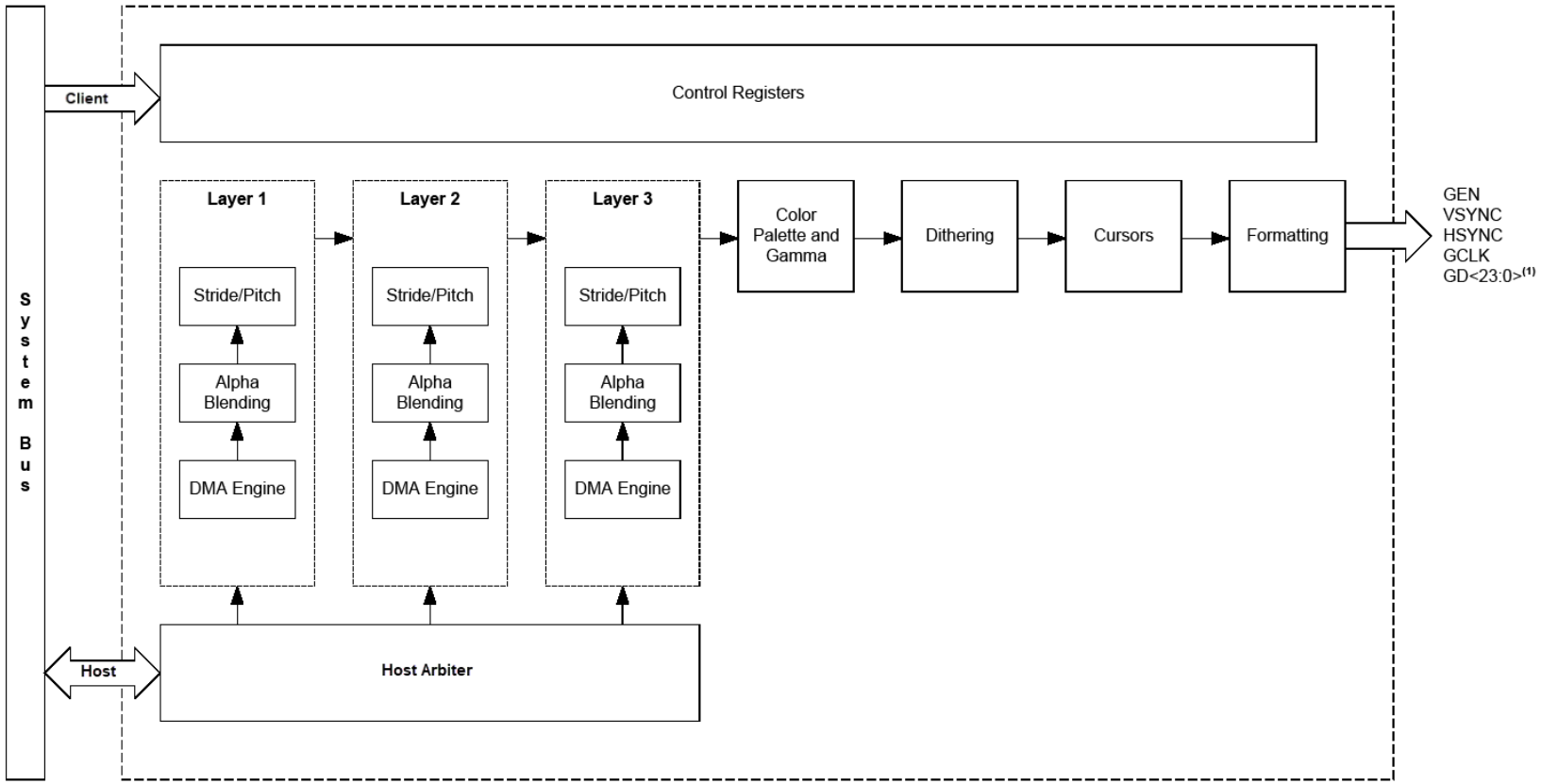
FIGURE 36-1: GRAPHICS LCD CONTROLLER BLOCK DIAGRAM



Note 1: R<7:0> = GD<7:0>; G<7:0> = GD<15:8>; B<7:0> = GD<23:16>.

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36.1 Graphics LCD Controller Control Registers

TABLE 36-1: GRAPHICS LCD CONTROLLER REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0	All Resets
A000	GLCD MODE	31:16	LCDEN	CURSOR EN	—	VSYNC POL	HSYNC POL	DEPOL	—	DITHER	VSYNC CYC	PCLK POL	—	PGRAMP EN	FORCE BLANK	—	—	—	0000
		15:0	—	—	—	—	—	—	YUV OUTPUT	FORMAT CLK	RGBSEQ<2:0>			—	—	—	—	—	0000
A004	GLCD CLKCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0401
		15:0	—	—	LPREFETCH<5:0>						—	—	CLKDIV<5:0>						0000
A008	GLCD BGCOLOR	31:16	RED<7:0>								GREEN<7:0>								0000
		15:0	BLUE<7:0>								ALPHA<7:0>								0000
A00C	GLCDRES	31:16	—	—	—	—	RESX<10:0>												0000
		15:0	—	—	—	—	RESY<10:0>												0000
A014	GLCD FPORCH	31:16	—	—	—	—	FPORCHX<10:0>												0000
		15:0	—	—	—	—	FPORCHY<10:0>												0000
A018	GLCD BLANKING	31:16	—	—	—	—	BLANKINGX<10:0>												0000
		15:0	—	—	—	—	BLANKINGY<10:0>												0000
A01C	GLCD BPORCH	31:16	—	—	—	—	BPORCHX<10:0>												0000
		15:0	—	—	—	—	BPORCHY<10:0>												0000
A020	GLCD CURSOR	31:16	—	—	—	—	CURSORX<10:0>												0000
		15:0	—	—	—	—	CURSORY<10:0>												0000
A030	GLCD L0MODE	31:16	LAYEREN	DISA BIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>								0000
		15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>				0000
A034	GLCD L0START	31:16	—	—	—	—	STARTX<10:0>												0000
		15:0	—	—	—	—	STARTY<10:0>												0000
A038	GLCD L0SIZE	31:16	—	—	—	—	SIZEX<10:0>												0000
		15:0	—	—	—	—	SIZEY<10:0>												0000
A03C	GLCD L0BADDR	31:16	BASEADDR<31:16>																0000
		15:0	BASEADDR<15:0>																0000
A040	GLCD L0STRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRIDE<15:0>																0000
A044	GLCD L0RES	31:16	—	—	—	—	RESX<10:0>												0000
		15:0	—	—	—	—	RESY<10:0>												0000
A050	GLCD L1MODE	31:16	LAYEREN	DISA BIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>								0000
		15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: For the PIXELxy bits, x = 0-31 and y = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

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TABLE 36-1: GRAPHICS LCD CONTROLLER REGISTER MAP (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bit 31/15	Bit 30/14	Bit 29/13	Bit 28/12	Bit 27/11	Bit 26/10	Bit 25/9	Bit 24/8	Bit 23/7	Bit 22/6	Bit 21/5	Bit 20/4	Bit 19/3	Bit 118/2	Bit 17/1	Bit 16/0	All Resets
A054	GLCD L1START	31:16	—	—	—	—	STARTX<10:0>												0000
		15:0	—	—	—	—	STARTY<10:0>												0000
A058	GLCD L1SIZE	31:16	—	—	—	—	SIZEX<10:0>												0000
		15:0	—	—	—	—	SIZEY<10:0>												0000
A05C	GLCD L1BADDR	31:16	BASEADDR<31:16>																0000
		15:0	BASEADDR<15:0>																0000
A060	GLCD L1STRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRIDE<15:0>																0000
A064	GLCD L1RES	31:16	—	—	—	—	RESX<10:0>												0000
		15:0	—	—	—	—	RESY<10:0>												0000
A070	GLCD L2MODE	31:16	LAYEREN	DISA BIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—	ALPHA<7:0>								0000
		15:0	DESTBLEND<3:0>				SRCBLEND<3:0>				—	—	—	—	COLORMODE<3:0>				0000
A074	GLCD L2START	31:16	—	—	—	—	STARTX<10:0>												0000
		15:0	—	—	—	—	STARTY<10:0>												0000
A078	GLCD L2SIZE	31:16	—	—	—	—	SIZEX<10:0>												0000
		15:0	—	—	—	—	SIZEY<10:0>												0000
A07C	GLCD L2BADDR	31:16	BASEADDR<31:16>																0000
		15:0	BASEADDR<15:0>																0000
A080	GLCD L2STRIDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRIDE<15:0>																0000
A084	GLCDL2RES	31:16	—	—	—	—	RESX<10:0>												0000
		15:0	—	—	—	—	RESY<10:0>												0000
A0F8	GLCDINT	31:16	IRQCON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HSYNCINT	VSYNCINT	0001
A0FC	GLCDSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	LROW	—	VSYNC	HSYNC	DE	ACTIVE	0000
A400 through A7FC	GLCDCLUTx ('x' = 0-255)	31:16	—	—	—	—	—	—	—	—	RED<7:0>								0000
		15:0	GREEN<7:0>								BLUE<7:0>								0000
A800 through A9FC	GLCD CURDATAx ('x' = 0-127)	31:16	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				0000
		15:0	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				PIXELxy<3:0>(1)				0000
AA00 through AA40	GLCD CURLUTx ('x' = 0-15)	31:16	—	—	—	—	—	—	—	—	RED<7:0>								0000
		15:0	GREEN<7:0>								BLUE<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: For the PIXELxy bits, x = 0-31 and y = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

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REGISTER 36-1: GLCDMODE: GRAPHICS LCD CONTROLLER MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	LCDEN	CURSOR EN	—	VSYNC POL	HSYNC POL	DEPOL	—	DITHER
23:16	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	VSYNC CYC	PCLKPOL	—	PGRAMP EN	FORCE BLANK	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	YUV OUTPUT	FORMAT CLK
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	RGBSEQ<2:0>			—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **LCDEN:** LCD Controller Module Enable bit
1 = LCD Controller module is enabled
0 = LCD Controller module is not enabled

bit 30 **CURSOREN:** Programmable Cursor Enable bit
1 = Programmable cursor is enabled
0 = Programmable cursor is enabled

bit 29 **Unimplemented:** Read as ‘0’

bit 28 **VSYNCPOL:** Vertical Sync Polarity bit
1 = VSYNC polarity is negative
0 = VSYNC polarity is positive

bit 27 **HSYNCPOL:** Horizontal Sync Polarity bit
1 = HSYNC polarity is negative
0 = HSYNC polarity is positive

bit 26 **DEPOL:** DE Polarity bit
1 = DE polarity is negative
0 = DE polarity is positive

bit 25 **Unimplemented:** Read as ‘0’

bit 24 **DITHER:** Dithering Enable bit
1 = Dithering is enabled
0 = Dithering is not enabled

bit 23 **VSYNCCYC:** Vertical Sync for Single Cycle Per Line Enable bit
1 = VSYNC for a single cycle per line is enabled
0 = VSYNC for a single cycle per line is not enabled

bit 22 **PCLKPOL:** Pixel Clock Out Polarity bit
1 = Pixel clock out polarity is negative
0 = Pixel clock out polarity is positive

bit 21 **Unimplemented:** Read as ‘0’

bit 20 **PGRAMPEN:** Palette Gamma Ramp Enable bit
1 = Palette gamma ramp is enabled
0 = Palette gamma ramp is not enabled

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REGISTER 36-1: GLCDMODE: GRAPHICS LCD CONTROLLER MODE REGISTER (CONTINUED)

bit 19 **FORCEBLANK:** Force Output to Blank bit
- 1 = Forces output to blank
- 0 = No effect

bit 18-10 **Unimplemented:** Read as '0'

bit 9 **YUVOUTPUT:** YUV Output Enable bit
- 1 = YUV is enabled
- 0 = RGB is enabled

bit 8 **FORMATCLK:** Formatting Clock Divide Enable bit
- 1 = Formatting clock is not divided
- 0 = Formatting clock is divided

bit 7-5 **RGBSEQ<2:0>:** RGB Sequential Modes bit
- 111 = BT.656
- 110 = YUYV
- 101 = Reserved
- 100 = Reserved
- 011 = Reserved
- 010 = Reserved
- 001 = Reserved
- 000 = Parallel RGB (RGB888, RGB666, RGB332)

bit 4-0 **Unimplemented:** Read as '0'

REGISTER 36-2: GLCDCLKCON: GRAPHICS LCD CONTROLLER CLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	LPREFETCH<5:0>					
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLKDIV<5:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as ‘0’

bit 13-8 **LPREFETCH<5:0>:** Lines Prefetch bits

These bits represent the number of lines to be prefetched before starting the frame (through DMA). The maximum value is $2^{LPREFETCH} = 32$.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **CLKDIV<5:0>:** Clock Divider bits

111111 = Reserved
111110 = Reserved
•
•
•
011111 = Divided by 31
011110 = Divided by 30
011101 = Divided by 29
•
•
•
000011 = Divided by 3
000010 = Divided by 2
000001 = Divided by 1
000000 = Divided by 0

Note: If the value of CLKDIV<5:0> is even, PCLK = (REFCLKO5/CLKDIV) with a duty cycle of 50%. If the value of CLKDIV<5:0> is odd, PCLK = (REFCLKO5/CLKDIV) with a duty cycle of 60% to 40%.

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REGISTER 36-3: GLCDBGCOLOR: GRAPHICS LCD CONTROLLER BACKGROUND COLOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RED<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GREEN<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLUE<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALPHA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **RED<7:0>:** Color Red as Background bits
These bits specify that the color red is to be used as the background color.

bit 23-16 **GREEN<7:0>:** Color Green as Background bits
These bits specify that the color green is to be used as the background color.

bit 15-8 **BLUE<7:0>:** Color Blue as Background bits
These bits specify that the color blue is to be used as the background color.

bit 7-0 **ALPHA<7:0>:** Color Alpha as Background bits
These bits specify that the color alpha is to be used as the background color.

Note: If all of the bits in this register are set (RED, GREEN, BLUE and ALPHA), RGBA color is used as the background.

REGISTER 36-4: GLCDRES: GRAPHICS LCD CONTROLLER RESOLUTION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESX<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-16 **RESX<10:0>:** X Dimension Pixel Resolution bits
These bits specify the pixel resolution for the X dimension.

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-0 **RESY<10:0>:** Y Dimension Pixel Resolution bits
These bits specify the pixel resolution for the Y dimension.

REGISTER 36-5: GLCDFPORCH: GRAPHICS LCD CONTROLLER FRONT PORCH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FPORCHX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FPORCHX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FPORCHY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FPORCHY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-16 **FPORCHX<10:0>:** X Dimension Front Porch Lines bits
These bits specify the front porch X dimension lines.

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-0 **FPORCHY<10:0>:** Y Dimension Front Porch Pixel Clocks bits
These bits specify the front porch Y dimension pixel clocks.

REGISTER 36-6: GLCDBLANKING: GRAPHICS LCD CONTROLLER BLANKING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BLANKINGX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLANKINGX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BLANKINGY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLANKINGY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-16 **BLANKINGX<10:0>:** X Dimension Blanking Period bits
These bits specify the HSYNC pulse length for the X dimension blanking period.

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-0 **BLANKINGY<10:0>:** Y Dimension Blanking Period bits
These bits specify the VSYNC lines for the Y dimension blanking period.

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REGISTER 36-7: GLCDBPORCH: GRAPHICS LCD CONTROLLER BACK PORCH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BPORCHX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BPORCHX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	BPORCHY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BPORCHY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-16 **BPORCHX<10:0>:** X Dimension Back Porch Lines bits
These bits specify the front porch X dimension lines.

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-0 **BPORCHY<10:0>:** Y Dimension Back Porch Pixel Clocks bits
These bits specify the front porch Y dimension pixel clocks.

REGISTER 36-8: GLCDCURSOR: GRAPHICS LCD CONTROLLER CURSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CURSORX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CURSORX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CURSORY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CURSORY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-16 **CURSORX<10:0>:** Cursor X Dimension Position bits
These bits specify the X dimension position of the cursor

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-0 **CURSORY<10:0>:** Cursor Y Dimension Position bits
These bits specify the Y dimension position of the cursor

REGISTER 36-9: GLCDLxMODE: GRAPHICS LCD CONTROLLER LAYER 'x' MODE REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	LAYEREN	DISABIFIL	FORCE ALPHA	MUL ALPHA	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALPHA<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DESTBLEND<3:0>				SRCBLEND<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	COLORMODE<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **LAYEREN:** Layer Enable bit
1 = Layer is enabled
0 = Layer is not enabled

bit 30 **DISABIFIL:** Disable Bilinear Filtering bit
1 = Bilinear filtering is enabled
0 = Bilinear filtering is not enabled

bit 29 **FORCEALPHA:** Force Alpha with Global Alpha bit
1 = Force alpha with global alpha is enabled
0 = Force alpha with global alpha is not enabled

bit 28 **MULALPHA:** Premultiply Image Alpha bit
1 = Premultiply image alpha is enabled
0 = Premultiply image alpha is not enabled

bit 27-24 **Unimplemented:** Read as '0'

bit 23-16 **ALPHA<7:0>:** Layer Alpha bits
These bits contain the Layer Alpha value ranging from 0 to 0xFF.

bit 15-12 **DESTBLEND<3:0>:** Destinary Blending Function bits
1111 = Reserved
1110 = Reserved
1101 = Blend inverted destination
1100 = Reserved
1011 = Reserved
1010 = Blend alpha destination
1001 = Reserved
1000 = Reserved
0111 = Blend inverted source and inverted global
0110 = Blend inverted global
0101 = Blend inverted source
0100 = Blend alpha source and alpha global
0011 = Blend alpha global
0010 = Blend alpha source
0001 = Blend white
0000 = Blend black

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REGISTER 36-9: GLCDLxMODE: GRAPHICS LCD CONTROLLER LAYER 'x' MODE REGISTER ('x' = 0-2) (CONTINUED)

bit 11-8 **SRCBLEND<3:0>:** Source Blending Function bits

1111 = Reserved
1110 = Reserved
1101 = Blend inverted destination
1100 = Reserved
1011 = Reserved
1010 = Blend alpha destination
1001 = Reserved
1000 = Reserved
0111 = Blend inverted source and inverted global
0110 = Blend inverted global
0101 = Blend inverted source
0100 = Blend alpha source and alpha global
0011 = Blend alpha global
0010 = Blend alpha source
0001 = Blend white
0000 = Blend black

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **COLORMODE<3:0>:** Color Mode bits

1111 = Reserved
1110 = Reserved
1101 = Reserved
1100 = Reserved
1011 = RGB888 color format
1010 = YUYV color format
1001 = L4 gray scale/palette format
1000 = L1 gray scale/palette format
0111 = L8 gray scale/palette format
0110 = 32-bit ARGB8888 color format
0101 = 16-bit RGB565 color format
0100 = 8-bit RGB332 color format
0011 = Reserved
0010 = 32-bit RGBA8888 color format
0001 = 16-bit RGBA5551 color format
0000 = 8-bit color palette look-up table (LUT8)

REGISTER 36-10: GLCDLxSTART: GRAPHICS LCD CONTROLLER LAYER 'x' START REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	STARTX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STARTX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	STARTY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STARTY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **STARTX<10:0>:** Layer Start X Dimension bits
These bits specify the pixel offset of the starting X dimension of the layer.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **STARTY<10:0>:** Layer Start Y Dimension bits
These bits specify the pixel offset of the starting Y dimension of the layer.

REGISTER 36-11: GLCDLxSIZE: GRAPHICS LCD CONTROLLER LAYER 'x' SIZE REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SIZEX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SIZEX<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SIZEY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SIZEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-16 **SIZEX<10:0>:** Layer Size X Dimension bits
These bits specify the pixel size of the layer in the X dimension.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-0 **SIZEY<10:0>:** Layer size Y Dimension bits
These bits specify the pixel size of the layer in the Y dimension.

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REGISTER 36-12: GLCDLxBADDR: GRAPHICS LCD CONTROLLER LAYER 'x' BASE ADDRESS REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** Base Address of the Framebuffer bits
These bits specify the base address of the framebuffer.

REGISTER 36-13: GLCDLxSTRIDE: GRAPHICS LCD CONTROLLER LAYER 'x' STRIDE REGISTER ('x' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STRIDE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STRIDE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'
bit 15-0 **STRIDE<15:0>:** Layer Stride bits
These bits specify the distance from line to line in bytes.

REGISTER 36-14: GLCDLxRES: GRAPHICS LCD CONTROLLER LAYER ‘x’ RESOLUTION REGISTER (‘x’ = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESX<10:8>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESX<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RESY<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RESY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-16 **RESX<10:0>:** X Dimension Layer Pixel Resolution bits
These bits specify the layer pixel resolution in the X dimension.

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10-0 **RESY<10:0>:** Y Dimension Layer Pixel Resolution bits
These bits specify the layer pixel resolution in the Y dimension.

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REGISTER 36-15: GLCDINT: GRAPHICS LCD CONTROLLER INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	IRQCON	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	HSYNCINT	VSYNCINT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **IRQCON:** IRQ Triggering Control bit
1 = Edge triggering is enabled
0 = Level triggering is enabled

bit 30-2 **Unimplemented:** Read as ‘0’

bit 1 **HYSNNCINT:** HSYNC Interrupt Enable bit
1 = HSYNC interrupt is enabled
0 = HSYNC interrupt is not enabled

bit 0 **VSYNCINT:** VSYNC Interrupt Enable bit
1 = VSYNC interrupt is enabled
0 = VSYNC interrupt is not enabled

REGISTER 36-16: GLCDSTAT: GRAPHICS LCD CONTROLLER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0	U-0	R-0	R-0	R-0	R-0
	—	—	LROW	—	VSYNC	HSYNC	DE	ACTIVE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as ‘0’

bit 5 **LROW:** Last Row bit
1 = Last row is currently being displayed
0 = Last row is not currently being displayed

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **VSYNC:** VSYNC Signal Level bit
This bit returns the VSYNC signal level.
Note: This bit is set 0 after VSYNC Interrupt.

bit 2 **HSYNC:** HSYNC Signal Level bit
This bit returns the HSYNC signal level.
Note: This bit is set to 0 after HSYNC interrupt.

bit 1 **DE:** DE Signal Level bit
This bit returns the DE signal level.

bit 0 **ACTIVE:** Active bit
1 = LCD Controller is not in active vertical blanking
0 = LCD Controller is in active vertical blanking

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REGISTER 36-17: GLCDCLUTx: GRAPHICS LCD CONTROLLER GLOBAL COLOR LOOKUP TABLE REGISTER x ('x'=0-255)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RED<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GREEN<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLUE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **RED<7:0>:** Global Color Lookup Table Red Component bits

bit 15-8 **GREEN<7:0>:** Global Color Lookup Table Green Component bits

bit 7-0 **BLUE<7:0>:** Global Color Lookup Table Blue Component bits

REGISTER 36-18: GLCDCURDATAx: GRAPHICS LCD CONTROLLER CURSOR DATA 'n' REGISTER ('n' = 0-127)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PIXELxy<3:0>(1)				PIXELxy<3:0>(1)			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 27-24 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 23-20 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 19-16 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 15-12 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 11-8 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 7-4 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)
bit 3-0 **PIXELxy<3:0>:** Pixel 'xy' Color Lookup bits(1)

Note 1: For the PIXELxy bits, x = 0-31 and y = 0-31 (i.e., GLCDCURDATA0 contains PIXEL00 through PIXEL07 with PIXEL00 in the most significant nibble).

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REGISTER 36-19: GLCDCURLUTx: GRAPHICS LCD CONTROLLER CURSOR LUT REGISTER 'x' ('x' = 0-15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RED<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GREEN<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BLUE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **RED<7:0>:** Cursor Lookup Table Red Component bit

bit 15-8 **GREEN<7:0>:** Cursor Lookup Table Green Component bit

bit 7-0 **BLUE<7:0>:** Cursor Lookup Table Blue Component bit

Note: The bits in this register contain the 8-bit RGB color value (0-255).

37.0 2-D GRAPHICS PROCESSING UNIT (GPU)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The 2-D Graphics Processing Unit manipulates and alters the contents of the frame buffer in system RAM or DDR2 memory to accelerate the rendering of images for eventual pixel display. Hardware acceleration is brought to numerous 2-D applications, such as graphics user interfaces (menus, objects, and so on).

The 2-D GPU also provides accelerated on-the-fly rendering of vertical and horizontal lines, rectangles, copying of a rectangular area between different locations in memory. Once initiated, the hardware will perform the rendering through DMA, which makes the CPU available for other tasks.

A block diagram showing the interface for the 2-D Graphics Processing Unit is provided in Figure 37-1.

Note: For this peripheral, no hardware interface is documented. Use the Nano-2D Library, which is available in MPLAB Harmony, to manage this module.

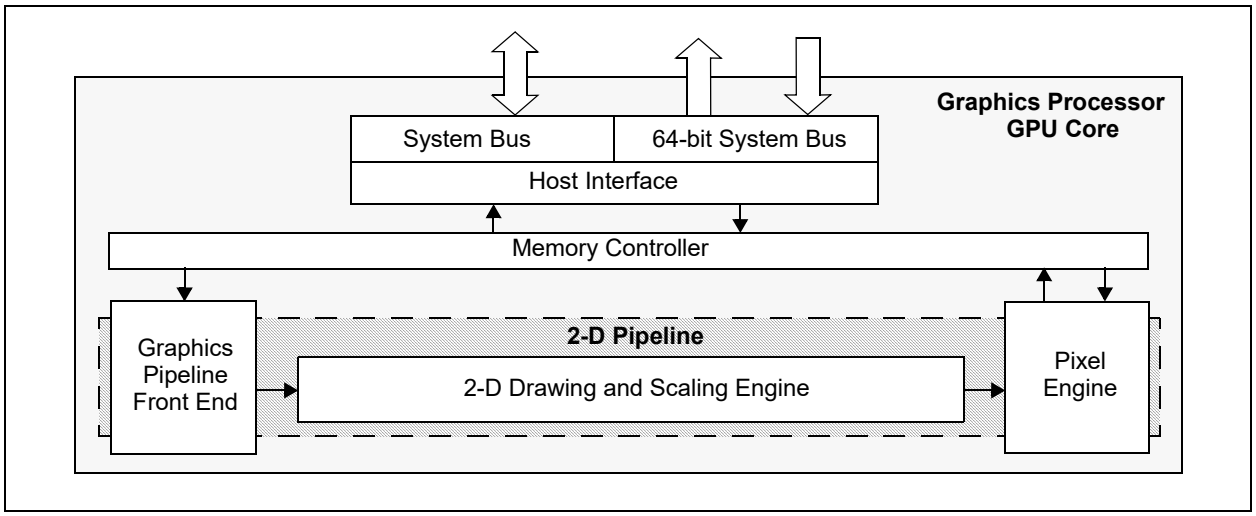
The following are key features of the 2-D Graphics Processing Unit:

- 64-bit bus access to memory (higher throughput)
- Global clock gating (low power)
- Command buffers
- Fixed Functions:
  - Line draw
  - Rectangle fill
  - Rectangle clear
  - Bit blit (stretch/shrink/filter)
  - Programmable raster operation (ROP2), with full alpha blending and transparency
- Source data formats:
  - RGBA8888, RGB565, RGB5551, 8-bit Index
- Destination data formats:
  - RGBA8888, RGB565, RGB5551
- Dithering (18-bit)
- Orientation in 90-degree steps
- Clipping

Note 1: For RGB source formats, their related swizzle formats, such as ARGB and RGBA are supported.

2: The GPU is enabled and ready out of POR. However, the GPU can be soft Reset at run-time using the GPURESET bit (CFGCON2<0>). Make sure that the GPUMD bit is set to '0' and wait 10 µs before toggling the GPURESET bit to achieve proper soft Reset.

FIGURE 37-1: 2-D GRAPHICS PROCESSING UNIT BLOCK DIAGRAM



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NOTES:

38.0 DDR2 SDRAM CONTROLLER

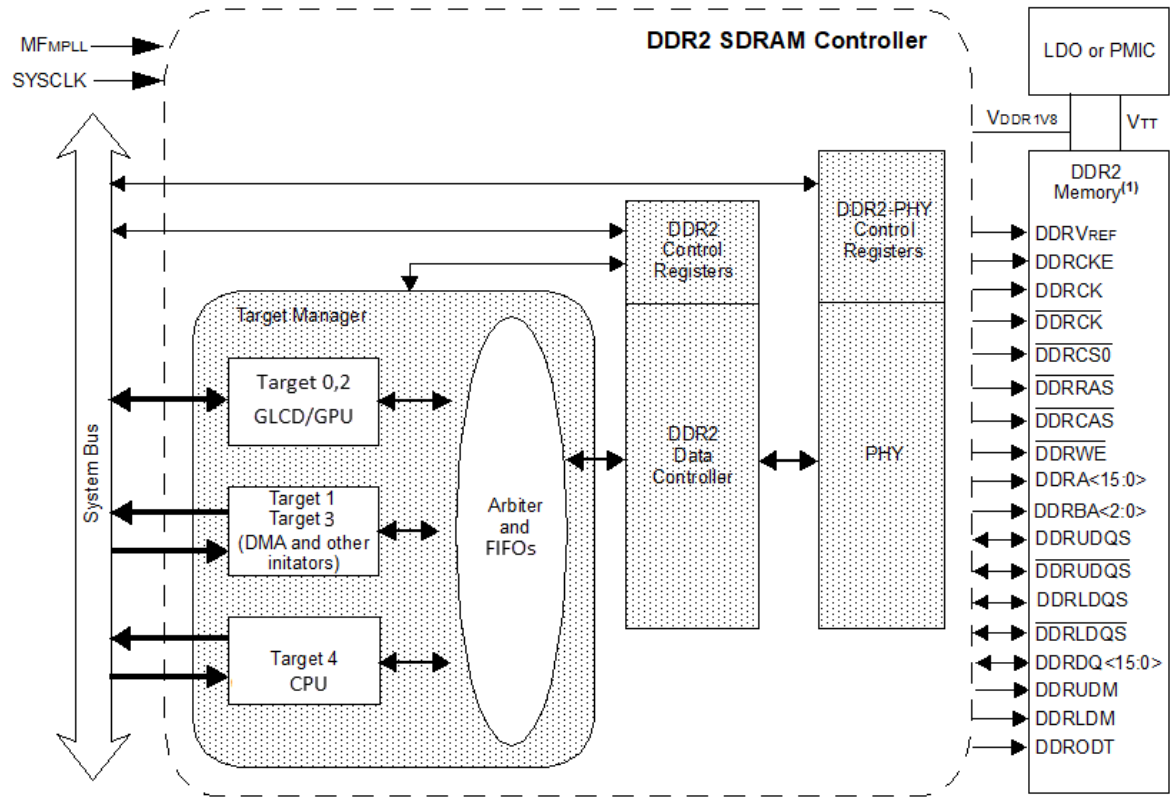
Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 55. "DDR SDRAM Controller"** (DS60001321'), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The DDR2 SDRAM Controller implements the controls for an internal memory bus interface using the Dual Data Rate version 2 (DDR2) protocol and electrical interface that adheres to the JEDEC Standard JESD79-2F (Nov. 2009).

The component consists of a DDR2 SDRAM Controller Core with configurable options and a DDR2 Physical Interface.

A block diagram showing how these components interface is provided in Figure 38-1.

FIGURE 38-1: DDR2 SDRAM CONTROLLER BLOCK DIAGRAM



Note 1: Internal DDR2 memory interface.

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38.1 Control Registers

TABLE 38-1: DDR SDRAM CONTROLLER REGISTER SUMMARY

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8000	DDR TSEL	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TSEL<7:0>								0000
8004	DDR MINLIM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	MINLIMIT<4:0>					0000
8008	DDR RQPER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RQPER<7:0>								0000
800C	DDR MINCMD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	MINCMD<7:0>								0000
8010	DDR MEMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INITDN	STINIT	0000
8014	DDR MEMCFG0	31:16	—	AP CHRGEN	—	CLHADDR<4:0>					—	—	—	CSADDR<4:0>					0000
		15:0	—	—	—	BNKADDR<4:0>					—	—	—	RWADDR<4:0>					0000
8018	DDR MEMCFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	RWADDRMSK<12:0>													0000
801C	DDR MEMCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CLADDRHMSK<12:0>													0000
8020	DDR MEMCFG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CLADDRLMSK<12:0>													0000
8024	DDR MEMCFG4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CSADDRMSK<2:0>			—	—	—	BNKADDRMSK<2:0>			0000
8028	DDR REFCFG	31:16	—	—	—	—	—	MAXREFS<2:0>			REFDLY<7:0>								0000
		15:0	REFCNT<15:0>																0000
802C	DDR PWRCFG	31:16	—	—	—	—	—	—	—	—	—	PCHRG PWRDN	SLFREFDLY<9:4>						0000
		15:0	SLFREFDLY<3:0>				PWRDNDLY<7:0>								ASLF REFEN	APWR DNEN	—	—	0000
8030	DDR DLYCFG0	31:16	RMWDLY<3:0>				R2WDLY>3:0>				W2WCSDLY<3:0>				W2WDLY<3:0>				0000
		15:0	R2RCSDLY<3:0>				R2RDLY<3:0>				W2RCSDLY<3:0>				W2RDLY<3:0>				0000
8034	DDR DLYCFG1	31:16	—	SLFREF EXDLY8	NXTDAT AVDLY4	W2R CSDLY4	W2R DLY4>	W2PCHRG DLY4	PWRDNEXDLY<5:0>						PWRDNMINDLY<3:0>				0000
		15:0	SLFREFEXDLY<7:0>								SLFREFMINDLY<7:0>								0000
8038	DDR DLYCFG2	31:16	RBENDDLY<3:0>				PCHRG2RASDLY<3:0>				RAS2CASDLY<3:0>				RAS2RASDLY<3:0>				0000
		15:0	W2PCHRGDLY<3:0>				R2PCHRGDLY<3:0>				—	—	—	—	PCHRGALLDLY<3:0>				0000
803C	DDR DLYCFG3	31:16	—	—	—	—	—	—	—	—	—	—	FAWTDLY<5:0>						0000
		15:0	—	—	RAS2RASSBNKDLY<5:0>						—	—	—	RAS2PCHRGDLY<4:0>					0000
8040	DDR ODTCFG	31:16	—	—	—	—	—	—	—	—	—	ODTWLEN<2:0>			—	ODTRLEN<2:0>			0000
		15:0	ODTWDLY<3:0>				ODTRDLY<3:0>				ODTCSEN<7:0>								0000
8044	DDR XFERCFG	31:16	BIGEN-DIAN	—	—	—	MAXBURST<3:0>				—	—	—	—	RDATENDLY<3:0>				0000
		15:0	—	—	—	—	—	—	—	—	NXTDATAVDLY<3:0>				NXTDATRQDLY<3:0>				0000

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TABLE 38-1: DDR SDRAM CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8048	DDR CMDISSUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	VALID	NUMHOSTCMDS<3:0>				0000
804C	DDR ODTENCFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODTWEN	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODTREN	0000
8050	DDR MEMWIDTH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HALF RATE	—	—	—	0000
8080	DDR CMD10	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
8084	DDR CMD11	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
8088	DDR CMD12	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
808C	DDR CMD13	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
8090	DDR CMD14	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
8094	DDR CMD15	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
8098	DDR CMD16	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD<27:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
809C	DDR CMD17	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80A0	DDR CMD18	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80A4	DDR CMD19	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000

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TABLE 38-1: DDR SDRAM CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
80A8	DDR CMD110	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80AC	DDR CMD111	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80B0	DDR CMD112	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80B4	DDR CMD113	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80B8	DDR CMD114	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD<27:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80BC	DDR CMD115	31:16	MDALCMD<7:0>								WEN CMD2	CASCMD2	RASCMD2	CSCMD2<7:3>					0000
		15:0	CSCMD2<2:0>			CLKEN CMD2	WEN CMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKEN CMD1	0000
80C0	DDR CMD20	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80C4	DDR CMD21	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80C8	DDR CMD22	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80CC	DDR CMD23	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80D0	DDR CMD24	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80D4	DDR CMD25	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80D8	DDR CMD26	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80DC	DDR CMD27	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80E0	DDR CMD28	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80E4	DDR CMD29	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000

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TABLE 38-1: DDR SDRAM CONTROLLER REGISTER SUMMARY (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
80E8	DDR CMD210	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80EC	DDR CMD211	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80F0	DDR CMD212	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80F4	DDR CMD213	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80F8	DDR CMD214	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
80FC	DDR CMD215	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>				0000
		15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>								0000
9100	DDR SCLSTART	31:16	—	—	SCL PHCAL	SCL START	—	SCLEN	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCL UBPASS	SCL LBPASS	0000
910C	DDR SCLLAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—				0000
		15:0	—	—	—	—	—	—	—	—	DDRCLKDLY<3:0>				CAPCLKDLY<3:0>				0000
9118	DDR SCLCFG0	31:16	—	—	—	—	—	—	—	ODTCSW	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RCASLAT<3:0>				—	—	DDR2	BURST8	0000
911C	DDR SCLCFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	DBL REFDLY	WCASLAT<3:0>				—	—	—	—	—	—	—	SCLSEN	0000
9120	DDR PHYPADCON	31:16	—	PREAMBDLY<1:0>		RCVREN	—	—	—	—	DRVSTRPFET<3:0>				DRVSTRNFET<3:0>				0000
		15:0	—	HALF RATE	WR CMDDLY	—	—	—	NOEXT DLL	EOEN CLKCYC	ODTPUCAL<1:0>		ODTPDCAL<1:0>		ADDC DRVSEL	DAT DRVSEL	ODTEN	ODTSEL	0000
9124	DDR PHYDLLR	31:16	DLYSTVAL<3:0>				—	DIS RECALIB	RECALIBCNT<17:8>										0000
		15:0	RECALIBCNT<7:0>								—	—	—	—	—	—	—	—	0000
9128	DDR PHYDLLCTRL	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DDRDLLTRIM<7:0>								0000
9140	DDR PHYCLKDLY	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	SCL UBPASS	SCL LBPASS	—	CLKDLYDELTA<2:0>			0000
915C	DDR ADLLBYP	31:16	—	—	—	—	—	—	—	ANL DLLBYP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
916C	DDR SCLCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLLANSEL<1:0>		0000
9188	DDR PHYSCLADR	31:16	SCLBANKADR<2:0>			SCLCOLADR<12:0>													0000
		15:0	SCLROWADR<15:0>																0000

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REGISTER 38-1: DDRTSEL: DDR TARGET SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TSEL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **TSEL<7:0>:** Target Select bits

These bits select the target to program arbitration parameters. This field must be set before an arbitration parameter is programmed for a target. The value in this field represents the target number (0-4) multiplied by the field size of the arbitration parameter.

REGISTER 38-2: DDRMINLIM: DDR MINIMUM BURST LIMIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MINLIMIT<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as ‘0’

bit 4-0 **MINLIMIT<4:0>:** Minimum Burst Limit bits

These bits determine the minimum number of DDR bursts (two cycles per burst) that a target must have uninterrupted access to without interference from another target.

Note: The TSEL<7:0> bits (DDRTSEL<7:0>) must be programmed with the target number multiplied by the size of the MINLIMIT field (5) before this register is used to program the minimum burst limit for that target.

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REGISTER 38-3: DDRRQPER: DDR REQUEST PERIOD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RQPER<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **RQPER<7:0>:** Request Period bits

These bits in conjunction with the MINCMD<7:0> bits (DDRMINCMD<7:0>), determine the percentage of total bandwidth that is allocated to the target. If the number of DDR bursts specified by MINCMD<7:0> are not serviced for the target when it has been requesting access for (RQPER<7:0> * 4) number of clocks, the target's requests are treated with high priority until this condition becomes satisfied.

Note: The TSEL<7:0> bits (DDRTSEL<7:0>) must be programmed with the target number multiplied by the size of the MINLIMIT field (5) before this register is used to program the minimum burst limit for that target.

REGISTER 38-4: DDRMINCMD: DDR MINIMUM COMMAND REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	MINCMD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **MINCMD<7:0>:** Minimum Command bits

These bits in conjunction with the RQPER<7:0> bits (DDRRQPER<7:0>) determine the percentage of total bandwidth that is allocated to the target. If the number of DDR bursts specified by MINCMD<7:0> are not serviced for the target when it has been requesting access for (RQPER<7:0> * 4) number of clocks, then the target's requests are treated with high priority until this condition becomes satisfied.

Note: The TSEL<7:0> bits (DDRTSEL<7:0>) must be programmed with the target number multiplied by the size of the MINLIMIT field (5) before this register is used to program the minimum burst limit for that target.

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REGISTER 38-5: DDRMEMCON: DDR MEMORY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	INITDN	STINIT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-2 **Unimplemented:** Read as ‘0’

bit 1 **INITDN:** Memory Initialize Done bit

Set by software after memory initialization is completed to enable controller for regular operation.

1 = All commands have been issued; the controller is enabled for regular operation
0 = Controller not enabled for regular operation

bit 0 **STINIT:** Memory Initialize Start bit

Set by software after the memory initialization commands are loaded into the DDRCMD registers to start memory initialization.

1 = Start memory initialization
0 = Do not start memory initialization

REGISTER 38-6: DDRMEMCFG0: DDR MEMORY CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	APCHRGEN	—	CLHADDR<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CSADDR<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	BNKADDR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RWADDR<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30 **APCHRGEN:** Automatic Precharge Enable bit

When set, this bit issues an auto-precharge command to close the bank at the end of every user command. If the command accesses more than one bank before completing, all banks accessed are auto-precharged.

1 = Issue an auto-precharged command

0 = Do not issue an auto-precharged command

bit 29 **Unimplemented:** Read as ‘0’

bit 28-24 **CLHADDR<4:0>:** Column Address Shift bits

These bits specify how many bits the controller address must be right-shifted to put the high part of the column address to the immediate left of the low part of the column address. Used in conjunction with CLADDRHMSK (DDRMEMCFG2<26:0>) and CLADDRLMASK (DDRMEMCFG3<26:0>).

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-16 **CSADDR<4:0>:** Chip Select Shift bits

These bits specify which bits of user address space are used to derive the Chip Select address for the DDR memory. Used in conjunction with CSADDRMASK (DDRMEMCFG4<10:8>).

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **BNKADDR<4:0>:** Bank Address Select Shift bits

These bits specify which bits of user address space are used to derive the bank address for the DDR memory. Used in conjunction with BNKADDRMASK (DDRMEMCFG4<2:0>).

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RWADDR<4:0>:** Row Address Select Shift bits

These bits specify which bits of user address space are used to derive the row address for the DDR memory. Used in conjunction with RWADDRMSK (DDRMEMCFG1<12:0>).

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REGISTER 38-7: DDRMEMCFG1: DDR MEMORY CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RWADDRMSK<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RWADDRMSK<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12-0 **RWADDRMSK<12:0>:** Row Address Mask bits

These bits, which are used in conjunction with the RWADDR<4:0> bits (DDRMEMCFG0<4:0>), specify which bits of user address space are used to derive the row address for the DDR memory.

REGISTER 38-8: DDRMEMCFG2: DDR MEMORY CONFIGURATION REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CLADDRHMSK<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CLADDRHMSK<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12-0 **CLADDRHMSK<12:0>:** Column Address High Mask bits

These bits, which are used in conjunction with the CLADDR<4:0> bits (DDRMEMCFG0<28:24>) and the CLADDRLMASK<12:0> bits (DDRMEMCFG3<12:0>), specify which bits of user address space are used to derive the column address for the DDR memory.

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REGISTER 38-9: DDRMEMCFG3: DDR MEMORY CONFIGURATION REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CLADDRLMSK<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CLADDRLMSK<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12-0 **CLADDRLMSK<12:0>:** Column Address Low Mask bits

These bits, which are used in conjunction with the CLADDR<4:0> bits (DDRMEMCFG0<28:24>) and the CLADDRHMASK<12:0> bits (DDRMEMCFG2<12:0>), specify which bits of user address space are used to derive the column address for the DDR memory.

REGISTER 38-10: DDRMEMCFG4: DDR MEMORY CONFIGURATION REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	CSADDRMSK<2>
7:0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CSADDRMSK<1:0>		—	—	—	BNKADDRMSK<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as ‘0’

bit 8-6 **CSADDRMSK<2:0>:** Chip Select Address Mask bits

These bits, which are used in conjunction with the CSADDR<4:0> bits (DDRMEMCFG0<20:16>), determine which bits of user address space are used to derive the Chip Select address for the DDR memory.

bit 5-3 **Unimplemented:** Read as ‘0’

bit 2-0 **BNKADDRMSK<2:0>:** Bank Address Mask bits

These bits, which are used in conjunction with the BNKADDR<4:0> bits (DDRMEMCFG0<12:8>), determine which bits of user address space are used to derive the bank address for the DDR memory.

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REGISTER 38-11: DDRREFCFG: DDR REFRESH CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	MAXREFS<2:0>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFDLY<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-24 **MAXREFS<2:0>:** Maximum Pending Refreshes bits

These bits specify the maximum number of refreshes that may be pending at any time. If there is any idle time when one or more refreshes are pending, the pending refreshes are issued continuously until a new request is received. If there is no idle time while MAXREFS <2:0> refreshes are pending, subsequent requests are stopped until at least one burst of pending refreshes can be issued.

bit 23-16 **REFDLY<7:0>:** Minimum Refresh-to-Refresh Delay bits

These bits specify the minimum number of clocks required between refreshes.

bit 15-0 **REFCNT<15:0>:** Refresh Count bits

These bits specify the number of clock cycles corresponding to the average periodic refresh interval.

REGISTER 38-12: DDRPWRCFG: DDR POWER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PCHRGPWRDN	SLFREFDLY<9:4>					
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SLFREFDLY<3:0>				PWDNDLY<7:4>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	PWDNDLY<3:0>				ASLFREFEN	APWRDNEN	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **PCHRGPWDN:** Precharge Power Down Only bit

Allow automatic entry into Precharge Power Down mode but not into active Power Down mode. If any rows are open they will be Precharged before DDR SDRAM is put into Precharge Power Down mode.
1 = Allow automatic entry into Precharge Power Down mode.
0 = Do not allow automatic entry into Precharge Power Down mode.

bit 21-12 **SLFREFDLY<9:0>:** Self Refresh Delay bits

Specifies the minimum number of clock cycles of idle time the controller needs to wait before automatic entry into Self Refresh mode. Value represents number of clocks multiplied by 1024.
111111111 = 2111452 clocks
….
000000001 = 1024 clocks

bit 11-4 **PWDNDLY<7:0>:** Refresh Count bits

Specifies the minimum number of clock cycles of idle time the controller needs to wait before automatic entry into Power Down mode (Active or Precharge). Value represents number of clocks multiplied by 4.
11111111 = 1020 clocks
….
00000001 = 4 clocks

bit 3 **ASLFREFEN:** Automatic Self Refresh Enable bit

1 = Allow automatic entry into Self Refresh mode.
0 = Do not allow automatic entry into Self Refresh mode.

bit 2 **APWRDNEN:** Automatic Power Down Enable bit

1 = Allow automatic entry into Power Down mode.
0 = Do not allow automatic entry into Power Down mode.

bit 1-0 **Unimplemented:** Read as ‘0’

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REGISTER 38-13: DDRDLYCFG0: DDR DELAY CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RMWDLY<3:0>				R2WDLY<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2WCSDLY<3:0>				W2WDLY<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	R2RCSDLY<3:0>				R2RDLY<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2RCSDLY<3:0>				W2RDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **RMWDLY<3:0>:** Read-Modify-Write Delay bits

These bits specify the minimum number of clocks required between the read and write commands issued for a read-modify-write operation.

bit 27-24 **R2WDLY<3:0>:** Read-to-Write Delay bits

These bits specify the minimum number of clocks required between a read command and write command. Commands may be to the same or different Chip Selects.

bit 23-20 **W2WCSDLY<3:0>:** Write-to-Write Chip Select Delay bits

These bits specify the minimum number of clocks required between two write commands to different Chip Selects.

bit 19-16 **W2WDLY<3:0>:** Write-to-Write Delay bits

These bits specify the minimum number of clocks required between two write commands to the same Chip Select.

bit 15-12 **R2RCSDLY<3:0>:** Read-to-Read Chip Select Delay bits

These bits specify the minimum number of clocks required between two read commands to different Chip Selects.

bit 11-8 **R2RDLY<3:0>:** Read-to-Read Delay bits

These bits specify the minimum number of clocks required between two read commands to the same Chip Select.

bit 7-4 **W2RCSDLY<3:0>:** Write-to-Read Chip Select Delay bits

These bits specify the minimum number of clocks required between a write command and a read command to different Chip Selects.

bit 3-0 **W2RDLY<3:0>:** Write-to-Read Delay bits

These bits specify the minimum number of clocks required between a write command and a read command to the same Chip Select.

REGISTER 38-14: DDRDLYCFG1: DDR DELAY CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	SLFREF EXDLY<8>	NXTDAT AVDLY<4>	W2RCS DLY<4>	W2RDLY<4>	W2PCHRG-DLY<4>	PWRDNEXDLY<5:4>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWRDNEXDLY<3:0>				PWRDNMINDLY <3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SLFREFEXDLY<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SLFREFMINDLY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30 **SLFREFEXDLY:** Self Refresh Exit Delay bit 8

This bit specifies the minimum number of clocks required before normal operation after exiting Self Refresh mode.

bit 29 **NXTDATAVDLY:** Next Data Available Delay bit 4

These bits specify the minimum number of clock cycles required between a Write command and the write data transfer handshake signal “next data request”. Also, see the NXTDATAVDLY<3:0> bits (DDRXFERCFG<7:4>).

bit 28 **W2RCSDLY:** Write-to-Read Chip Select Delay bit 4

This bit specify the minimum number of clocks required between a write command and a read command to different Chip Selects. Also, see W2RCSDLY<3:0> (DDRDLYCFG0<7:4>).

bit 27 **W2RDLY:** Write-to-Read Delay bit 4

This bit specifies the minimum number of clocks required between a write command and a read command to the same Chip Select. Also, see W2RDLY<3:0> (DDRDLYCFG0<3:0>).

bit 26 **W2PCHRGDLY:** Write to Precharge Delay bit 4

These bits specify the minimum number of clocks required from a Write command to a Precharge command to the same bank as the write. Also, see WPCHRGDLY<3:0> (DDRDLYCFG2<15:12>).

bit 25-20 **PWRDNEXDLY<5:0>:** Power Down Exit Delay bits

These bits specify the minimum number of clocks required before normal operation after exiting Power Down mode.

bit 19-16 **PWRDNMINDLY<3:0>:** Power Down Minimum Delay bits

These bits specify the minimum number of clocks to stay in Power Down mode after entering it.

bit 15-8 **SLFREFEXDLY<7:0>:** Self Refresh Exit Delay bits

These bits specify the minimum number of clocks required before normal operation after exiting Self Refresh mode.

bit 7-0 **SLFREFMINDLY<7:0>:** Self Refresh Minimum Delay bits

These bits specify the minimum number of clocks to stay in Self Refresh mode after entering it.

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REGISTER 38-15: DDRDLYCFG2: DDR DELAY CONFIGURATION REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RBENDDLY<3:0>				PCHRG2RASDLY<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RAS2CASDLY<3:0>				RAS2RASDLY <3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2PCHRGDLY<3:0>				R2PCHRGDLY<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	PCHRGALLDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **RBENDDLY<3:0>:** Read Burst End Delay bits

These bits specify the minimum number of clocks required from issue of a Read command to the read data burst completion.

bit 27-24 **PCHRG2RASDLY<3:0>:** Precharge-to-RAS Delay bits

These bits specify the minimum number of clocks required from a Precharge command to a RAS command to the same bank.

bit 23-20 **RAS2CASDLY<3:0>:** RAS-to-CAS Delay bits

These bits specify the minimum number of clocks required from a RAS command to a CAS command to the same bank.

bit 19-16 **RAS2RASDLY<3:0>:** Write-to-Read Delay bits

These bits specify the minimum number of clocks required from a RAS command to a RAS command to a different bank on the same Chip Select.

bit 15-12 **W2PCHRGDLY<3:0>:** Write-to-Precharge Delay bits 3-0

These bits specify the minimum number of clocks required from a Write command to a Precharge command to the same bank as the write.

An overflow bit (DDRDLYCFG1<26>) is provided for delays greater than 15 clock cycles.

bit 11-8 **R2PCHRGDLY<3:0>:** Read-to-Precharge Delay bits

These bits specify the minimum number of clocks required from a read command to a Precharge command to the same bank as the read.

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **PCHRGALLDLY<3:0>:** Precharge All Delay bits

These bits specify the minimum number of clocks required from a Precharge all banks command to an Activate or Refresh command.

REGISTER 38-16: DDRDLYCFG3: DDR DELAY CONFIGURATION REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	FAWTDLY<5:0>					
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	RAS2RASSBNKDLY<5:0>					
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RAS2PCHRGDLY<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as ‘0’

bit 21-16 **FAWTDLY<5:0>:** Four Activate Window Time Delay bits
These bits specify the minimum number of clocks within which only four banks may be opened.

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RAS2RASSBNKDLY<5:0>:** RAS-to-RAS Same Bank Delay bits
These bits specify the minimum number of clocks required between RAS commands to the same bank.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RAS2PCHRGDLY<4:0>:** RAS-to-Precharge Delay bits
These bits specify the minimum number of clocks required from a RAS command to a Precharge command to the same bank.

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REGISTER 38-17: DDRODTCFG: DDR ON-DIE TERMINATION CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	ODTWLEN<2:0>			—	ODTRLEN<2:0>		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	OTDWDLY<3:0>				OTDRDLY<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	OTDCSEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22-20 **ODTWLEN<2:0>:** On-Die Termination Write Length bits
These bits specify the number of clocks ODT is turned on for writes.

bit 19 **Unimplemented:** Read as ‘0’

bit 18-16 **ODTRLEN<2:0>:** On-Die Termination Read Length bits
These bits specify the number of clocks ODT is turned on for reads.

bit 15-12 **ODTWDLY<3:0>:** On-Die Termination Write Delay bits
These bits specify the number of clocks after a Write command before turning on ODT to the DDR.

bit 11-8 **ODTRDLY<3:0>:** On-Die Termination Read Delay bits
These bits specify the number of clocks after a Read command before turning on ODT to the DDR.

bit 7-0 **ODTCSEN<7:0>:** On-Die Termination Chip Select Enable bits
These bits are used with the DDRODTENCFG register (Register 38-20) to program the ODT control for each Chip Select. The value in this field represents the number of Chip Selects multiplied by the Chip Select number to be programmed.

REGISTER 38-18: DDRXFERCFG: DDR TRANSFER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0
	BIGENDIAN	—	—	—	MAXBURST<3:0>			
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RDATENDLY<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NXTDATAVDLY<3:0>				NXTDATRQDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **BIGENDIAN:** Big Endian bit
`1` = Data is big endian format
`0` = Data is little endian format

bit 30-28 **Unimplemented:** Read as ‘`0`’

bit 27-24 **MAXBURST<3:0>:** Maximum Command Burst Count bits
These bits specify the maximum number of commands that can be written to the DDR controller in Burst mode.

bit 23-20 **Unimplemented:** Read as ‘`0`’

bit 19-16 **RDATENDLY<3:0>:** PHY Read Data Enable Delay bits
These bits specify the minimum number of clocks Required between issuing a Read command to the PHY and when the “read data enable” signal to the PHY is asserted.

bit 15-8 **Unimplemented:** Read as ‘`0`’

bit 7-4 **NXTDATAVDLY<3:0>:** Next Data Available Delay bits
These bits specify the minimum number of clock cycles required between issuing a Read command and the read data being received.

bit 3-0 **NXTDATRQDLY<3:0>:** Next Data Request Delay bits
These bits specify the minimum number of clock cycles required between issuing a Write command and the write data transfer handshake signal “next data request”.

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REGISTER 38-19: DDRCMDISSUE: DDR COMMAND ISSUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	VALID	NUMHOSTCMDS<3:0>			

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as ‘0’

bit 4 **VALID:** Host Command Valid bit

When written with a '1', this bit indicates to the controller that the data in the Host command registers are valid, and should be transmitted to the SDRAM. This bit is cleared by hardware when all data has been transmitted.

bit 3-0 **NUMHOSTCMDS<3:0>:** Number of Host Commands bits

The number of Host commands to be transmitted to the SDRAM.

REGISTER 38-20: DDRODTENCFG: DDR ON-DIE TERMINATION ENABLE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ODTWEN
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ODTREN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-17 **Unimplemented:** Read as ‘0’

bit 16 **ODTWEN:** On-Die Termination Write Enable bit

1 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT enabled for data reads

0 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT disabled for data reads

bit 15-1 **Unimplemented:** Read as ‘0’

bit 0 **ODTREN:** On-Die Termination Read Enable bit

1 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT enabled for data writes

0 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT disabled for data writes

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REGISTER 38-21: DDRMEMWIDTH: DDR MEMORY WIDTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	—	—	—	—	HALFRATE	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as ‘0’

bit 3 **HALFRATE:** Half-rate Mode bit

The PIC32 always operates in Half-rate mode. This bit must be set during initialization.

1 = Half-rate mode

0 = Full-rate mode

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 38-22: DDRCMD1*x*: DDR HOST COMMAND 1 REGISTER '*x*' ('*x*' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MDALCMD<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7>
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSCMD1<6:0>							CLKENCMD1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **MDALCMD<7:0>:** Mode Address Low Command bits
These bits specify the value to be driven on the SDRAM address bits 7 through 0 when issuing the command.

bit 23 **WENCMD2:** Write Enable Command 2 bit
This bit specifies the value to be driven on WE_N on the second and subsequent cycles of issuing the command

bit 22 **CASCMD2:** Column Address Strobe Command 2 bit
This bit specifies the value to be driven on CAS_N on the second and subsequent cycles of issuing the command

bit 21 **RASCMD2:** Row Address Strobe Command 2 bit
This bit specifies the value to be driven on RAS_N on the second and subsequent cycles of issuing the command

bit 20-13 **CSCMD2<7:0>:** Chip Select Command 2 bits
These bits specify the value to be driven on the CS_N signals (maximum of 8) on the second and subsequent cycles of issuing the command.

bit 12 **CLKENCMD2:** Clock Enable Command 2 bit
This bit specifies the value to be driven on CKE on the second and subsequent cycles of issuing the command.

bit 11 **WENCMD1:** Write Enable Command 1 bit
This bit specifies the value to be driven on the WE_N on the first cycle of issuing the command.

bit 10 **CASCMD1:** Column Address Strobe Command 1 bit
This bit specifies the value to be driven on the CAS_N on the first cycle of issuing the command.

bit 9 **RASCMD1:** Row Address Strobe Command 1 bit
This bit specifies the value to be driven on the RAS_N on the first cycle of issuing the command.

bit 8-1 **CSCMD1<7:0>:** Chip Select Command 1 bit
These bits specify the value to be driven on the CS_N signals (maximum of 8) on the first cycle of issuing the command.

bit 0 **CLKENCMD1:** Clock Enable Command 1 bit
This bit specifies the value to be driven on CKE on the first cycle of issuing the command.

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REGISTER 38-23: DDRCMD2*x*: DDR HOST COMMAND 2 REGISTER '*x*' ('*x*' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	WAIT<8:5>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAIT<4:0>					BNKADDRCMD<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MDADDRHCMD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-11 **WAIT<8:0>:** Wait Command bits

These bits specify the number of clock cycles to wait after issuing a command before issuing the next command.

bit 10-8 **BNKADDRCMD<2:0>:** Bank Address Command bit

These bits specify the value to be driven on the bank address bits when issuing the command.

bit 7-0 **MDADDRHCMD<7:0>:** Mode Address High Command bits

These bits specify the value to be driven on the SDRAM address bits 15 through 8 when issuing the command.

REGISTER 38-24: DDRSCLSTART: DDL SELF CALIBRATION LOGIC START REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	U-0	W-0	U-0	R/W-0
	—	—	SCL PHCAL	SCL START	—	SCLEN	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	SCLUB PASS(1)	SCLLB PASS(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Write as ‘0’

bit 29 **SCLPHCAL:** Start Phase Self-calibration Logic bit
1 = Phase calibration is enabled
0 = Phase calibration is disabled

bit 28 **SCLSTART:** Start Self Calibration Logic bit
1 = Start self calibration
0 = Do not start self calibration

Note: This bit is cleared by hardware when the SCL process is complete.

bit 27 **Unimplemented:** Write as ‘0’

bit 26 **SCLEN:** Self Calibration Logic Enable bit
1 = Enable dynamic self calibration logic
0 = Disable dynamic self calibration logic

Note: Enabling dynamic self calibration may impact performance.

bit 25-2 **Unimplemented:** Write as ‘0’

bit 1 **SCLUBPASS:** Self Calibration Logic Upper Data Byte Status bit(1)
1 = Self calibration logic for upper data byte passed
0 = Self calibration logic for upper data byte failed

bit 0 **SCLLBPASS:** Self Calibration Logic Lower Data Byte Status bit(1)
1 = Self calibration logic for lower data byte passed
0 = Self calibration logic for lower data byte failed

Note 1: This bit is set by hardware when the SCL process has passed and is complete.

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REGISTER 38-25: DDRSCLLAT: DDL SELF CALIBRATION LOGIC LATENCY REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-1	R/W-1	R/W-0	U-0	U-0	R/W-1	R/W-0
	DDRCLKDLY<3:0>				CAPCLKDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-4 **DDRCLKDLY<3:0>:** DDR Clock Delay bit
Recommended value is 4.

bit 3-0 **CAPCLKDLY<3:0>:** Capture Clock Delay bit
Recommended value is 3.

REGISTER 38-26: DDRSCLCFG0: DDR SCL CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
	—	—	—	—	—	—	—	ODTCSW
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-0	R/W-1	R/W-1	U-0	U-0	R/W-0	R/W-1
	RCASLAT<3:0>				—	—	DDR2	BURST8

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as ‘0’

bit 24 **ODTCSW:** On-Die Termination Chip Select Write bit
1 = ODT is turned on to the DRAM on CS0 during writes performed by the SCL
0 = ODT is turned off to the DRAM on CS0 during writes performed by the SCL.

bit 23-8 **Unimplemented:** Read as ‘0’

bit 7-4 **RCASLAT<3:0>:** Read CAS Latency bits
DRAM read CAS latency in clock cycles

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **DDR2:** DDR2 bit
1 = DDR2 is connected
0 = DDR2 is not connected

bit 0 **BURST8:** PHY Burst 8 bit
1 = DRAM is in burst 8 mode while running SCL test
0 = DRAM is in burst 4 mode while running SCL test

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REGISTER 38-27: DDRSCLCFG1: DDR SCL CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
	—	—	—	DBLREFDLY	WCASLAT<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
	—	—	—	—	—	—	—	SCLCSEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12 **DBLREFDLY:** Double Reference Delay bit

Determines whether the PHY will delay an SCL operation following an acknowledge by one or two time intervals. The time interval is a function of the hardware design.

1 = SCL operation delay doubled

0 = SCL operation delay not doubled

bit 11-8 **WCASLAT<3:0>:** Write CAS Latency bits

DRAM write CAS latency in clock cycles.

bit 7-1 **Unimplemented:** Read as ‘0’

bit 0 **SCLCSEN:** SCL Chip Select Enable bit

1 = Run SCL on Chip Select 0

0 = Do not run SCL on Chip Select 0

REGISTER 38-28: DDRPHYPADCON: DDR PHY PAD CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-1	R/W-0	R/W-1	U-0	U-0	U-0	U-0
	—	PREAMBDLY<1:0>		RCVREN	—	—	—	—
23:16	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	DRVSTRPFET<3:0>				DRVSTRNFET<3:0>			
15:8	U-0	R/W-1	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	HALFRATE	WR CMDDLY	—	—	—	NOEXTDLL	EOEN CLKCYC
7:0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	ODTPUCAL<1:0>		ODTPDCAL<1:0>		ADDC DRVDLY	DAT DRVSEL	ODTEN	ODTSEL

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30-29 **PREAMBDLY<1:0>:** Preamble Delay bits
Controls the length of the preamble for writes.
11 = Reserved
10 = 1 cycle preamble
01 = 1.5 cycle preamble
00 = 2 cycle preamble

bit 28 **RCVREN:** Receiver Enable bit
1 = Pad receivers on bidirectional I/Os are turned on
0 = Pad receivers on bidirectional I/Os are turned off

bit 27-24 **Unimplemented:** Read as ‘0’

bit 23-20 **DRVSTRPFET<3:0>:** PFET Drive Strength bits
Pad PFET driver output impedance adjustment control
1111 = Maximum drive strength
•
•
•
0000 = Minimum drive strength.

bit 19-16 **DRVSTRNFET<3:0>:** NFET Drive Strength bits
Pad NFET driver output impedance adjustment control
1111 = Maximum drive strength
•
•
•
0000 = Minimum drive strength.

bit 15 **Unimplemented:** Read as ‘0’

bit 14 **HALFRATE:** Half Rate bit
1 = Controller clock is running at half rate with respect to PHY
0 = Controller clock is running at full rate with respect to PHY

bit 13 **WRCMDDLY:** Write Command Delay bit
This bit should be set to ‘1’ if Write Latency (WL) is an even number.
1 = Write command delay
0 = No Write command delay

bit 12-10 **Unimplemented:** Read as ‘0’

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REGISTER 38-28: DDRPHYPADCON: DDR PHY PAD CONTROL REGISTER (CONTINUED)

bit 9 **NOEXTDLL:** No External DLL bit
1 = Use internal digital DLL.
0 = Use external DLL.

bit 8 **EOENCLKCYC:** Extra Output Enable bit
1 = Drive pad output enables for an extra clock cycle after a write burst
0 = Do not drive pad output enables for an extra clock cycle after a write burst

bit 7-6 **ODTPUCAL<1:0>:** On-Die Termination Pull-up Calibration bits
11 = Maximum ODT impedance
•
•
•
00 = Minimum ODT impedance

bit 5-4 **ODTPFDCAL<1:0>:** On-Die Termination Pull-down Calibration bits
11 = Maximum ODT impedance
•
•
•
00 = Minimum ODT impedance

bit 3 **ADDCDRVSEL:** Address and Control Pads Drive Strength Select bit
1 = Full drive strength
0 = 60% driver strength

bit 2 **DATDRVSEL:** Data Pad Drive Strength Select bit
1 = Full Drive Strength
0 = 60% Drive Strength

bit 1 **ODTEN:** On-Die Termination Enable bit
1 = ODT Enabled
0 = ODT Disabled

bit 0 **ODTSEL:** On-Die Termination Select bit
1 = 150 ohm On-Die Termination
0 = 75 ohm On-Die Termination

REGISTER 38-29: DDRPHYDLLR: DDR PHY DLL RECALIBRATE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	DLYSTVAL<3:0>				—	DISRECALIB	RECALIBCNT<17:16>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RECALIBCNT<15:8>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RECALIBCNT<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **DLYSTVAL<3:0>:** Delay Start Value bits
Start value of the digital DLL delay line. Recommended value is ‘0011’.

bit 27 **Unimplemented:** Read as ‘0’

bit 26 **DISRECALIB:** Disable Recalibration bit
1 = Do not recalibrate the digital DLL after the first time
0 = Recalibrate the digital DLL in accordance with the value of the RECALIBCNT<17:0> bits

bit 25-8 **RECALIBCNT<17:0>:** Recalibration Count bits
Determines the period of recalibration of the digital DLL in units of (256 * PHY clock cycles).

bit 7-0 **Unimplemented:** Read as ‘0’

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REGISTER 38-30: DDRPHYDLLCTRL: DDR PHY TRIM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	r-x	r-x
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DDRDLLTRIM<7:0>							

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-10 **Unimplemented:** Read as ‘0’

bit 9-8 **Reserved:** Write as ‘0’

bit 7-0 **DDRDLLTRIM<7:0>:** Trim Setting bits

These bits control the Trim settings for adjusting the output time of the bank address and control signals with respect to data signals (DQ/DQS). The recommended value is 0x1.

REGISTER 38-31: DDRPHYCLKDLY: DDR CLOCK DELTA DELAY REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0	R-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	SCLUBPASS(1)	SCLLBPASS(1)	—	CLKDLYDELTA<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as ‘0

bit 5 **SCLUBPASS:** Self Calibration Logic Upper Data Byte Status bit (1)

1 = Self calibration logic for upper data byte is passed

0 = Self calibration logic for upper data byte is failed

bit 4 **SCLLBPASS:** Self Calibration Logic Lower Data Byte Status bit(1)

1 = Self calibration logic for lower data byte is passed

0 = Self calibration logic for lower data byte is failed

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **CLKDLYDELTA<2:0>:** DDR Clock Delay Delta bits

These bits indicate the SCL latency setting programmed per byte lane.

`111` = 7 DDR clocks
`110` = 6 DDR clocks
•
•
•
`000` = 0 DDR clocks

These bits are automatically programmed by the SCL logic and can also be programmed by the user, and are specifically useful for SCL retires.

Note 1: These bits indicate the same status as the SCLLBPASS (DDRSCLSTART<0>) and SCLUBPASS (DDRSCLSTART<0>) bits.

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REGISTER 38-32: DDRADLLBYP: DDR ANALOG DLL BYPASS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ANLDLLBYP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as ‘0’

bit 24 **ANLDLLBYP:** Bypass Analog DLL bit

1 = Bypass the Analog DLL and use the PHY Digital DLL

0 = Reserved; do not use

bit 23-0 **Unimplemented:** Read as ‘0’

REGISTER 38-33: DDRSCLCFG2: DDR SCL CONFIGURATION REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SCLLANSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-2 **Unimplemented:** Read as ‘0’

bit 1-0 **SCLLANSEL<1:0>:** Memory Lane Select bits

These bits can be used to run the SCL on a limited number of lanes rather than all lanes by default. Lanes with the corresponding bit set are not checked by SCL.

11 = Reserved; do not use

10 = Use the upper byte lane

01 = Use the lower byte lane

00 = Use both lanes

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REGISTER 38-34: DDRPHYSCLADR: DDR PHY SCL ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCLBANKADR<2:0>			SCLCOLADR<12:8>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCLCOLADR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCLROWADR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SCLROWADR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **SCLBANKADR<2:0>:** SCL Bank Address bits
These bits define the bank address to use when running SCL.

bit 28-16 **SCLCOLADR<12:0>:** SCL Column Address bits
These bits define the column address to use when running SCL.

bit 15-0 **SCLROWADR<15:0>:** SCL Row Address bits
These bits define the row address to use when running SCL.

39.0 SECURE DIGITAL HOST CONTROLLER (SDHC)

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 57. "Secure Digital Host Controller (SDHC)"** (DS60001334), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The SDHC module uses a 32-bit System Bus host and client interface to connect the Host system and standard card interface on the device side.

The core has a built-in DMA controller so that data can be automatically transferred between system memory and the SD/SDIO/eMMC card without intervention from the CPU.

The SDHC module includes the following features:

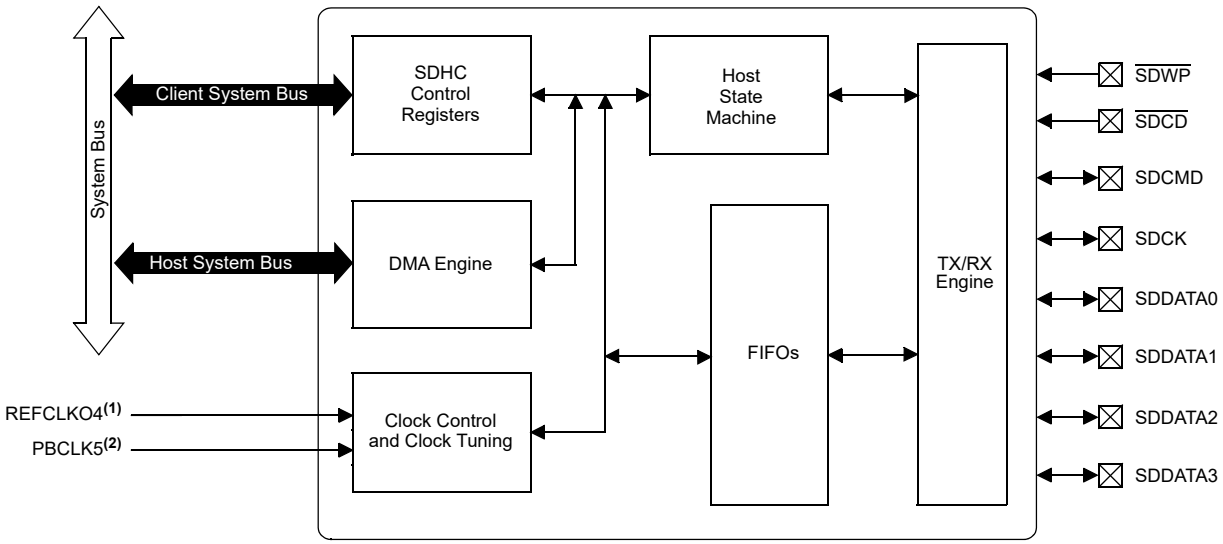
- SD Association specification compliance:
  - SD Host Controller Simplified Specification, version 2.00
  - Physical Layer Simplified Specification, version 2.00
  - SDIO Simplified Specification, version 2.00
- eMMC Standard: JESD84-A441
- Default and High-Speed modes of operation
- 1-bit or 4-bit data transfers
- Built-in clock divider
- PIO and ADMA modes of data transfer
- 3.3V operation
- Interrupt support
- Stop at block gap

A block diagram of the SDHC module is provided in Figure 39-1.

Note 1: Transmit and receive buffer addresses in ADMA mode must be word-aligned. When multiple descriptors are used to transfer a single block, all but the last descriptor must have a transfer size in multiples of four.

2: REFCLKO4 must be less or equal to PBCLK5 when used as SDHC clock.

FIGURE 39-1: SECURE DIGITAL HOST CONTROLLER (SDHC) BLOCK DIAGRAM



Note 1: When configuring the REFCLKO4 clock source, a value of '0' for the ROTRIM<8:0> bits must be selected. REFCLKO4 must be turned on before SDHC Special Function Registers (SFR) access.

2: This clock source is only used for SDHC Special Function Register (SFR) access.

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39.1 Control Registers

TABLE 39-1: SDHC SFR SUMMARY

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
C004	SDHC BLKCON	31:16	BCOUNT<15:0>																0000
		15:0	—	—	—	—	—	—	BSIZE<9:0>										0000
C008	SDHC ARG	31:16	ARG<31:16>																0000
		15:0	ARG<15:0>																0000
C00C	SDHC MODE	31:16	—	—	CIDX<5:0>						CTYPE<1:0>		DPSEL	CIDXCEN	CCRCCEN	—	RESPTYPE<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	BSEL	DTXDSEL	ACEN<1:0>		BCEN	DMAEN	0000
C010	SHDC RESP0	31:16	RESP<31:16>																0000
		15:0	RESP<15:0>																0000
C014	SHDC RESP1	31:16	RESP<31:16>																0000
		15:0	RESP<15:0>																0000
C018	SHDC RESP2	31:16	RESP<31:16>																0000
		15:0	RESP<15:0>																0000
C01C	SHDC RESP3	31:16	RESP<31:16>																0000
		15:0	RESP<15:0>																0000
C020	SHDC DATA	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
C024	SDHC STAT1	31:16	—	—	—	—	—	—	—	CMDSLVL	DATA3SLVL	DATA2SLVL	DATA1SLVL	DATA0SLVL	WPSLVL	CDSLVL	CARDST	CARDINS	0000
		15:0	—	—	—	—	BREN	BWEN	RDACTIVE	WRACTIVE	—	—	—	—	—	DLACTIVE	CINHDAT	CINHCMD	0000
C028	SDHC CON1	31:16	—	—	—	—	—	WKONREM	WKONINS	WKONINT	—	—	—	—	INTBG	RDWTCON	CONTREQ	SBGREQ	0000
		15:0	—	—	—	—	—	—	—	SDBP	CDSSEL	CDTLVL	—	DMASEL<1:0>		HSEN	DTXWIDTH	—	0000
C02C	SDHC CON2	31:16	—	—	—	—	—	SWRDATA	SWRCMD	SWRALL	—	—	—	—	DTOC<3:0>				0000
		15:0	SDCLKDIV<7:0>								—	—	—	—	—	SDCLKEN	ICLKSTABLE	ICLKEN	0000
C030	SDHC INTSTAT	31:16	—	—	—	—	—	—	ADEIF	ACEIF	CLEIF	DEBEIF	DCRCEIF	DTOEIF	CIDXEIF	CEBEIF	CCRCEIF	CTOEIF	0000
		15:0	EIF	—	—	—	—	—	—	CARDIF	CARDRIF	CARDIIF	BRRDYIF	BWRDYIF	DMAIF	BGIF	TXCIF	CCIF	0000
C034	SDHC INTEN	31:16	—	—	—	—	—	—	ADEIE	AACEIE	CLEIE	DEBEIE	DCRCEIE	DTOEIE	CIDXEIE	CDEBEIE	CCRCEIE	CTOEIE	0000
		15:0	FTZIE	—	—	—	—	—	—	CARDIE	CARDRIE	CARDIIE	BRRDYIE	BWRDYIE	DMAIE	BGIE	TXCIE	CCE	0000
C038	SDHC INTSEN	31:16	—	—	—	—	—	—	ADEISE	ACEISE	CLEISE	DEBEISE	DCRCEISE	DTOEISE	CIDXEISE	CEBEISE	CEBEISE	CCRCEISE	0000
		15:0	FTZEISE	—	—	—	—	—	—	CARDISE	CARDRISE	CARDIISE	BRRDYISE	BWRDYISE	DMAISE	BGISE	TXCISE	CCISE	0000
C03C	SDHC STAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNISSE	—	—	ACIDXE	ACEBE	ACCRCE	ACTOE	ACNEXEC	0000
C040	SDHC CAP	31:16	SLOTTYPE<1:0>		ASYNCINT	—	—	—	—	VOLT3V3	SRESUME	—	HISPEED	—	ADMA2	—	MBLEN<1:0>		2000
		15:0	BASECLK<7:0>								TOCLKU	—	TOCLKFREQ<5:0>						0000
C048	SDHC MAXCAP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	MC3V3<7:0>								0000
C050	SDHCFE	31:16	—	—	—	—	—	—	FEAE	FEACE	FECLE	FEDEBE	FEDCRCE	FEDTOE	FEIDXE	FECEBE	FECCRCE	FECTOE	0000
		15:0	—	—	—	—	—	—	—	—	FECNIACE	—	—	FEACIDXE	FEACEBE	FEACCRCE	FEACTOE	FEACNEE	0000

Legend: '—' = unimplemented; read as '0'.

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TABLE 39-1: SDHC SFR SUMMARY (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C054	SDHC AESTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	ALMERR	AERRST<1:0>		0000
C058	SDHC AADDR	31:16	ADDR<31:16>																0000
		15:0	ADDR<15:0>																0000

Legend: '—' = unimplemented; read as '0'.

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REGISTER 39-1: SDHCBLKCON: SDHC BLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCOUNT<15:8>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCOUNT<7:0>(1)							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	BSIZE<9:8>(2)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BSIZE<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **BCOUNT<31:0>:** Blocks Count for Current Transfer bits(1)
These bits represent the number of blocks. The software sets this value between 1 and 65,535 blocks and the SDHC decrements the count after each block transfer and stops when the count reaches zero.
0xFFFF = 65,535 blocks
0x0002 = 2 blocks
0x0001 = 1 block
0x0000 = Stop count Blocks Count for Current Transfer bits

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9-0 **BSIZE<9:0>:** Transfer Block Size bits(2)
These bits specify the block size of the data transfer for CMD17, CMD18, CMD24, CMD25, and CMD53.
0x200 = 512 bytes
0x1FF = 511 bytes
•
•
•
0x002 = 2 bytes
0x001 = 1 byte
0x000 = No data transfer

Note 1: These bits are used only when the BCEN bit (SDHCMODE<1>) is set to '1' and is valid only for multiple block transfers. The BCOUNT<15:0> bits need not be set if the BSIZE bit (SDHCMODE<5>) is set to '0'.

2: These bits can only be accessed when no transactions are in progress. Read operations during transfers will return an invalid value and write operations to these bits will be ignored.

REGISTER 39-2: SDHCARG: SDHC ARGUMENT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARG<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARG<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARG<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **ARG<31:0>:** Command Argument bits

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REGISTER 39-3: SDHCMODE: SDHC MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CIDX<5:0>(1)					
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CTYPE<1:0>		DPSEL	CIDXCEN(2)	CCRCCEN(3)	—	RESPTYPE<1:0>	
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	BSEL	DTXDSEL	ACEN<1:0>		BCEN	DMAEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as ‘0’

bit 29-24 **CIDX<5:0>:** Command Index bits(1)
These bits represent the command number (0-63).

bit 23-22 **CTYPE<1:0>:** Command Type bits
11 = Abort
10 = Resume
01 = Suspend
00 = Normal

bit 21 **DPSEL:** Data Present Select bit
1 = Data is present
0 = Data is not present

bit 20 **CIDXCEN:** Command Index Check Enable bit(2)
1 = Command index check is enabled
0 = Command index check is disabled

bit 19 **CCRCCEN:** Command CRC Check Enable bit(3)
1 = Command CRC check is enabled
0 = Command CRC check is disabled

bit 18 **Unimplemented:** Read as ‘0’

bit 17-16 **RESPTYPE<1:0>:** Response Type Select bits
11 = Response length 48; check busy after response
10 = Response length 48
01 = Response length 136
00 = No response

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5 **BSEL:** Multiple/Single Block Select bit
1 = Multiple block, set when issuing multiple transfer commands using DAT lines
0 = Single block

Note 1: Refer to bits 45-40 of the command format in the *“SD Host Controller Simplified Specification”* (version 2.00).

2: If these bits are set to '1', the SDHC will check the index field in the response to see if it has the same value as the CIDX<5:0> bits, if not, it will be reported as a command index error.

3: If these bits are set to '1', the SDHC will check the CRC field in the response and reports a command CRC error upon a CRC error detection.

REGISTER 39-3: SDHCMODE: SDHC MODE REGISTER (CONTINUED)

bit 4 **DTXDSEL:** Data Transfer Direction Select bit
1 = Read (card to SDHC)
0 = Write (SDHC to card)

bit 3-2 **ACEN<1:0>:** Auto CMD12 Enable bits
Auto CMD12 is used to stop multiple-block read/write operations.
11 = Reserved
10 = Reserved
01 = Auto CMD12 is enabled
00 = Auto CMD 12 is disabled

bit 1 **BCEN:** Block Count Enable Bit
1 = Block count is enabled
0 = Block count is disabled

bit 0 **DMAEN:** DMA Enable bit
1 = DMA (ADMA) is used to transfer data
0 = CPU is used to transfer data

Note 1: Refer to bits 45-40 of the command format in the *"SD Host Controller Simplified Specification"* (version 2.00).

2: If these bits are set to '1', the SDHC will check the index field in the response to see if it has the same value as the CIDX<5:0> bits, if not, it will be reported as a command index error.

3: If these bits are set to '1', the SDHC will check the CRC field in the response and reports a command CRC error upon a CRC error detection.

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REGISTER 39-4: SDHCRESPx: SDHC RESPONSE REGISTER 'x' ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RESP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **RESP<31:0>:** Response bits
These bits indicate the bit positions of Responses [31:0] defined in the *"SD Host Controller Simplified Specification* (version 2.00). Refer to Table 39-2 for full bit definitions.

TABLE 39-2: RESPONSE BIT DEFINITION FOR EACH RESPONSE TYPE

Response Type (see Note 1)	Response Meaning	Response Register
R1, R1b (normal response)	Card status	SDHCRESP0<31:0>
R1b (Auto CMD12 response)	Card status for Auto CMD12	SDHCRESP3<31:0>
R2 (CID, CSD register)	CID or CSD register	SDHCRESP0<31:0> SDHCRESP1<31:0> SDHCRESP2<31:0> SDHCRESP3<31:0>
R3 (OCR register)	OCR register for memory	SDHCRESP0<31:0>
R4 (OCR register)	OCR register for I/O, etc.	SDHCRESP0<31:0>
R5, R5b	SDIO response	SDHCRESP0<31:0>
R6 (published RCA response)	New published RCA<31:16>, etc.	SDHCRESP0<31:0>

Note 1: For additional information, refer to the "*SD Host Controller Simplified Specification"* (version 2.00), the "*Physical Layer Simplified Specification"* (version 2.00), and the *"SDIO Simplified Specification"* (version 2.00). These documents are available for download by visiting the SD Association web site at: http://www.sdcard.org/downloads/pls/simplified_specs/archive/index.html

REGISTER 39-5: SDHCDATA: SDHC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** Buffer Data bits
These bits are used to access bits 31 through 0 of the internal data buffer.

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REGISTER 39-6: SDHCSTAT1: SDHC STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-x, HC
	—	—	—	—	—	—	—	CMDSLVL
23:16	R-x, HC	R-x, HC	R-x, HC	R-x, HC	R-x, HC	R-x, HC	R-x, HC	R-x, HC
	DATA3SLVL	DATA2SLVL	DATA1SLVL	DATA0SLVL	WPSLVL	CDSLVL	CARDST	CARDINS
15:8	U-0	U-0	U-0	U-0	R-0, HC	R-0, HC	R-0, HC	R-0, HC
	—	—	—	—	BREN	BWEN	RDACTIVE	WRACTIVE
7:0	U-0	U-0	U-0	U-0	U-0	R-0, HC	R-0, HC	R-0, HC
	—	—	—	—	—	DLACTIVE	CINHDAT	CINHCMD

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as ‘0’

bit 24 **CMDSLVL:** Command Line Signal Level bit
1 = CMD line is high
0 = CMD line is low

bit 23 **DATA3SLVL:** DATA3 Signal Level bit
1 = DAT3 line is high
0 = DAT3 line is low

bit 22 **DATA2SLVL:** DATA2 Signal Level bit
1 = DAT2 line is high
0 = DAT2 line is low

bit 21 **DATA1SLVL:** DATA1 Signal Level bit
1 = DAT1 line is high
0 = DAT1 line is low

bit 20 **DATA0SLVL:** DATA0 Signal Level bit
1 = DAT0 line is high
0 = DAT0 line is low

bit 19 **WPSLVL:** Write-protect Signal Level bit
1 = Write-protect is disabled
0 = Write-protect is enabled

bit 18 **CDSLVL:** Card Detect Signal Level bit
1 = Card is present
0 = Card is not present

bit 17 **CARDST:** Card State Stable bit
1 = No card or inserted
0 = Reset or debouncing

bit 16 **CARDINS:** Card Inserted bit
1 = Card inserted
0 = Reset or debouncing or no card

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11 **BREN:** Buffer Read Enable bit
1 = Buffer read is enabled
0 = Buffer read is disabled

Note: This register is used to recover from errors and for debugging.

REGISTER 39-6: SDHCSTAT1: SDHC STATUS REGISTER 1 (CONTINUED)

bit 10 **BWEN:** Buffer Write Enable bit
1 = Buffer write is enabled
0 = Buffer write is disabled

bit 9 **RDACTIVE:** Read Transfer Active bit
1 = Data is being transferred
0 = No valid data

bit 8 **WRACTIVE:** Write Transfer Active bit
1 = Data is being transferred
0 = No valid data

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **DLACTIVE:** DAT Line Active bit
1 = DAT line is active
0 = DAT line is inactive

bit 1 **CINHDAT:** Command Inhibit (DAT) bit
1 = A command that uses the DAT line cannot be issued
0 = A command that uses the DAT line can be issued

bit 0 **CINHCMD:** Command Inhibit (CMD) bit
1 = A command cannot be issued
0 = A command can only be issued using the CMD line

Note: This register is used to recover from errors and for debugging.

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REGISTER 39-7: SDHCCON1: SDHC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WKONREM	WKONINS	WKONINT
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	HC, R/W-0	R/W-0
	—	—	—	—	INTBG	RDWTCON	CONTREQ	SBGREQ
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	SDBP
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	CDSSEL	CDTLVL	—	DMASEL<1:0>		HSEN	DTXWIDTH	—

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26 **WKONREM:** Wake-up Event Enable on SD Card Removal bit
1 = Wake-up event is enabled
0 = Wake-up event is disabled

bit 25 **WKONINS:** Wake-up Event Enable on SD Card Insertion bit
1 = Wake-up event is enabled
0 = Wake-up event is disabled

bit 24 **WKONINT:** Wake-up Event Enable on SD Card Interrupt bit
1 = Wake-up event is enabled
0 = Wake-up event is disabled

bit 23-20 **Unimplemented:** Read as ‘0’

bit 19 **INTBG:** Interrupt at Block Gap bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **RDWTCON:** Read Wait Control bit
1 = Read wait control is enabled
0 = Read wait control is disabled

bit 17 **CONTREQ:** Continue Request bit
A write to this bit is ignored if STOPREQ is set to ‘1’.
1 = Restart
0 = No effect

bit 16 **SBGREQ:** Stop at Block Gap Request bit
1 = Stop
0 = Transfer

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8 **SDBP:** SD Bus Power bit
1 = Bus power is on
0 = Bus power is off

bit 7 **CDSSEL:** Card Detect Signal Selection bit
1 = The card detect test level is select (for test purposes)
0 = SDCDx is selected (for normal use)

bit 6 **CDTLVL:** Card Detect Test Level bit
1 = Card is inserted
0 = Card is not inserted

REGISTER 39-7: SDHCCON1: SDHC CONTROL REGISTER 1 (CONTINUED)

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **DMASEL<1:0>:** DMA Select bits
11 = Reserved
10 = 32-bit address ADMA2 is selected
01 = Reserved
00 = Reserved

bit 2 **HSEN:** High-Speed Enable bit
1 = High-Speed mode is enabled
0 = Normal Speed mode is enabled

bit 1 **DTXWIDTH:** Data Transfer Width bit
1 = 4-bit mode
0 = 1-bit mode

bit 0 **Unimplemented:** Read as '0'

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REGISTER 39-8: SDHCCON2: SDHC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0, HC	R/W-0, HC	R/W-0, HC
	—	—	—	—	—	SWRDATA	SWRCMD	SWRALL
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DTOC<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SDCLKDIV<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SDCLKEN	ICLK STABLE	ICLKEN

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26 **SWRDATA:** Software Reset for DATA Line bit
1 = DMA and part of the data logic are reset
0 = Continue operation

bit 25 **SWRCMD:** Software Reset for CMD Line bit
1 = Clears Present State and Interrupt Status registers and CMD bits
0 = Continue operation

bit 24 **SWRALL:** Software Reset for All bit
1 = Issue reset command and reinitialize the SD card
0 = Divided Clock mode is selected

bit 23-20 **Unimplemented:** Read as ‘0’

bit 19-16 **DTOC<3:0>:** Data Time-out Counter Value bits
1111 = Reserved
1110 = Time-out clock x 2^{27}
.
.
.
0001 = Time-out clock x 2^{14}
0000 = Time-out clock x 2^{13}

bit 15-8 **SDCLKDIV<7:0>:** SDCLK Divider Select bits
When 8-bit Divided Clock mode is selected:
0x80 - Base clock divided by 256
0x40 - Base clock divided by 128
0x20 - Base clock divided by 64
0x10 - Base clock divided by 32
0x08 - Base clock divided by 16
0x04 - Base clock divided by 8
0x02 - Base clock divided by 4
0x01 - Base clock divided by 2
0x00 - Base clock

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **SDCLKEN:** SD Clock Enable bit
1 = SD clock is enabled
0 = SD clock is disabled

bit 1 **ICLKSTABLE:** Internal Clock Stable bit
1 = Internal clock is ready
0 = Internal clock is not ready

bit 0 **ICLKEN:** Internal Clock Enable bit
1 = Oscillate
0 = Stop

REGISTER 39-9: SDHCINTSTAT: SDHC INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HC	R/W-0, HC
	—	—	—	—	—	—	ADEIF	ACEIF
23:16	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	CLEIF	DEBEIF	DCRCEIF	DTOEIF	CIDXEIF	CEBEIF	CCRCEIF	CTOEIF
15:8	R-0, HC	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HC
	EIF	—	—	—	—	—	—	CARDIF
7:0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	CARDRIF	CARDIIF	BRRDYIF	BWRDYIF	DMAIF	BGIF	TXCIF	CEIF

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **ADEIF:** ADMA Error Interrupt Flag bit
1 = ADMA error has occurred
0 = ADMA error has not occurred

bit 24 **ACEIF:** Auto CMD12 Error Interrupt Flag bit
1 = Auto CMD12 error has occurred
0 = Auto CMD12 error has not occurred

bit 23 **CLEIF:** Current-Limit Error Interrupt Flag bit
1 = Current-limit error has occurred
0 = Current-limit error has not occurred

bit 22 **DEBEIF:** Data End Bit Error Interrupt Flag bit
1 = Data End bit error has occurred
0 = Data End bit error has not occurred

bit 21 **DCRCEIF:** Data CRC Error Interrupt Flag bit
1 = Data CRC error has occurred
0 = Data CRC error has not occurred

bit 20 **DTOEIF:** Data Time-out Error Interrupt Flag bit
1 = Data time-out error has occurred
0 = Data time-out error has not occurred

bit 19 **CIDXEIF:** Command Index Error Interrupt Flag bit
1 = Command index error has occurred
0 = Command index error has not occurred

bit 18 **CEBEIF:** Command End Bit Error Interrupt Flag bit
1 = End bit error was generated
0 = End bit error was not generated

bit 17 **CCRCEIF:** Command CRC Error Interrupt Flag bit
1 = Command CRC error has occurred
0 = Command CRC error has not occurred

bit 16 **CTOEIF:** Command Time-out Error Interrupt Flag bit
1 = Command time-out error has occurred
0 = Command time-out error has not occurred

bit 15 **EIF:** Error Interrupt Flag bit
This bit is set if any or all bits, 0 through 9, in this register are set.
1 = Error was detected
0 = No error was detected

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REGISTER 39-9: SDHCINTSTAT: SDHC INTERRUPT STATUS REGISTER (CONTINUED)

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CARDIF:** Card Interrupt Status bit
1 = Generate card interrupt
0 = Do not generate card interrupt

bit 7 **CARDRIF:** Card Removal Interrupt Flag bit
1 = Card has been removed
0 = Card state is stable or debouncing

bit 6 **CARDIIF:** Card Insertion Interrupt Flag bit
1 = Card has been inserted
0 = Card state is stable or debouncing

bit 5 **BRRDYIF:** Buffer Read Ready Interrupt Flag bit
1 = Ready to read buffer
0 = Not ready to read buffer

bit 4 **BWRDYIF:** Buffer Write Ready Interrupt Flag bit
1 = Ready to write buffer
0 = Not ready to write buffer

bit 3 **DMAIF:** DMA Interrupt Status bit
1 = DMA interrupt was generated
0 = DMA interrupt was not generated

bit 2 **BGIF:** Block Gap Interrupt Flag bit
1 = Transaction stopped at block gap
0 = No block gap event has occurred

bit 1 **TXEIF:** Transfer Complete Interrupt Flag bit
1 = Command execution has completed
0 = Command execution has not completed

bit 0 **CEIF:** Command Complete Interrupt Flag bit
1 = Command is complete
0 = Command is not complete

REGISTER 39-10: SDHCINTEN: SDHC INTERRUPT FLAG ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HC	R/W-0, HC
	—	—	—	—	—	—	ADEFIE	ACEFIE
23:16	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	CLEFIE	DEBEFIE	DCRCEFIE	DTOEFIE	CIDXEFIE	CDEBEFIE	CCRCEFIE	CTOEFIE
15:8	R-0, HC	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HC
	FTZIE	—	—	—	—	—	—	CARDIE
7:0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	CARDRIE	CARDIIE	BRRDYIE	BWRDYIE	DMAIE	BGIE	TXEIE	CEIE

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 21-26 **Unimplemented:** Read as ‘0’

bit 25 **ADEFIE:** ADMA Interrupt Flag Error Enable bit
1 = ADMA error interrupt flag is enabled
0 = ADMA error interrupt flag is masked

bit 24 **ACEFIE:** Auto CMD12 Interrupt Flag Error Enable bit
1 = Auto CMD12 error interrupt flag is enabled
0 = Auto CMD12 error interrupt flag is masked

bit 23 **CLEFIE:** Current-Limit Interrupt Flag Error Enable bit
1 = Current-limit error interrupt flag is enabled
0 = Current-limit error interrupt flag is masked

bit 22 **DEBEFIE:** Data End Bit Interrupt Flag Error Enable bit
1 = Data End bit error interrupt flag is enabled
0 = Data End error interrupt flag is masked

bit 21 **DCRCEFIE:** Data CRC Interrupt Flag Error Enable bit
1 = Data CRC error interrupt flag is enabled
0 = Data CRC error interrupt flag is masked

bit 20 **DTOEFIE:** Data Time-out Interrupt Flag Error Enable bit
1 = Data time-out error interrupt flag is enabled
0 = Data time-out error interrupt flag is masked

bit 19 **CIDXEFIE:** Command Index Interrupt Flag Error Enable bit
1 = Command index error interrupt flag is enabled
0 = Command index error interrupt flag is masked

bit 18 **CDEBEFIE:** Command End Bit Interrupt Flag Error Enable bit
1 = Command End bit error interrupt flag is enabled
0 = Command End bit error interrupt flag is masked

bit 17 **CCRCEFIE:** Command CRC Interrupt Flag Error Enable bit
1 = Command CRC error interrupt flag is enabled
0 = Command CRC error interrupt flag is masked

bit 16 **CTOEFIE:** Command Time-out Interrupt Flag Error Enable bit
1 = Command time-out error interrupt flag is enabled
0 = Command time-out error interrupt flag is masked

bit 15 **FTZIE:** Fixed to Zero Interrupt Flag Enable bit
This bit is set if any or all bits, 0 through 9, in this register are set.
1 = Error was detected
0 = No error was detected

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REGISTER 39-10: SDHCINTEN: SDHC INTERRUPT FLAG ENABLE REGISTER (CONTINUED)

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CARDIE:** Card Interrupt Flag Enable bit
1 = Card interrupt flag is enabled
0 = Card interrupt flag is masked

bit 7 **CARDRIE:** Card Removal Interrupt Flag Enable bit
1 = Card removal interrupt flag is enabled
0 = Card removal interrupt flag is masked

bit 6 **CARDIIE:** Card Insertion Interrupt Flag Enable bit
1 = Card insertion interrupt flag is enabled
0 = Card insertion interrupt flag is masked

bit 5 **BRRDYIE:** Buffer Read Ready Interrupt Flag Enable bit
1 = Buffer read ready interrupt flag is enabled
0 = Buffer read ready interrupt flag is masked

bit 4 **BWRDYIE:** Buffer Write Ready Interrupt Flag Enable bit
1 = Buffer write ready interrupt flag is enabled
0 = Buffer write ready interrupt flag is masked

bit 3 **DMAIE:** DMA Interrupt Flag Enable bit
1 = DMA interrupt flag is enabled
0 = DMA interrupt flag is masked

bit 2 **BGIE:** Block Gap Interrupt Flag Enable bit
1 = Block gap event interrupt flag is enabled
0 = Block gap event interrupt flag is masked

bit 1 **TXEIE:** Transfer Complete Interrupt Flag Enable bit
1 = Transfer complete interrupt flag is enabled
0 = Transfer complete interrupt flag is masked

bit 0 **CEIE:** Command Complete Interrupt Flag Enable bit
1 = Command complete interrupt flag is enabled
0 = Command complete interrupt flag is masked

REGISTER 39-11: SDHCINTSEN: SDHC INTERRUPT SIGNAL ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HC	R/W-0, HC
	—	—	—	—	—	—	ADEISE	ACEISE
23:16	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	CLEISE	DEBEISE	DCRCEISE	DTOEISE	CIDXEISE	CEBEISE	CCRCEISE	CTOEISE
15:8	R-0, HC	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HC
	FTZEISE	—	—	—	—	—	—	CARDISE
7:0	R/W-1, HC	R/W-1, HC	R/W-1, HC	R/W-1, HC	R/W-1, HC	R/W-1, HC	R/W-1, HC	R/W-1, HC
	CARDRISE	CARDIISE	BRRDYISE	BWRDYISE	DMAISE	BGISE	TXEISE	CEISE

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **ADEISE:** ADMA Error Interrupt Signal Enable bit
1 = ADMA error signal is enabled
0 = ADMA error signal is masked

bit 24 **ACEISE:** Auto CMD12 Error Interrupt Signal Enable bit
1 = Auto CMD12 error signal is enabled
0 = Auto CMD12 error signal is masked

bit 23 **CLEISE:** Current-Limit Error Interrupt Signal Enable bit
1 = Current-limit error signal is enabled
0 = Current-limit error signal is masked

bit 22 **DEBEISE:** Data End Bit Error Interrupt Signal Enable bit
1 = Data end bit error signal is enabled
0 = Data end bit error signal is masked

bit 21 **DCRCEISE:** Data CRC Error Interrupt Signal Enable bit
1 = Data CRC error signal is enabled
0 = Data CRC error signal is masked

bit 20 **DTOEISE:** Data Time-out Error Interrupt Signal Enable bit
1 = Data time-out error signal is enabled
0 = Data time-out error signal is masked

bit 19 **CIDXEISE:** Command Index Error Interrupt Signal Enable bit
1 = Command index error signal is enabled
0 = Command index error signal is masked

bit 18 **CEBEISE:** Command End Bit Error Interrupt Signal Enable bit
1 = Command End bit error signal is enabled
0 = Command End bit error signal is masked

bit 17 **CCRCEISE:** Command CRC Error Interrupt Signal Enable bit
1 = Command CRC error signal is enabled
0 = Command CRC error signal is masked

bit 16 **CTOEISE:** Command Time-out Error Interrupt Signal Enable bit
1 = Command time-out error signal is enabled
0 = Command time-out error signal is masked

bit 15 **FTZEISE:** Fixed to Zero Error Interrupt Signal Enable bit
This bit is set if any or all bits, 0 through 9, in this register are set.
1 = Error was detected
0 = No error was detected

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REGISTER 39-11: SDHCINTSEN: SDHC INTERRUPT SIGNAL ENABLE REGISTER (CONTINUED)

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CARDISE:** Card Interrupt Signal Enable bit
1 = Card interrupt signal is enabled
0 = Card interrupt signal is masked

bit 7 **CARDRISE:** Card Removal Interrupt Signal Enable bit
1 = Card removal signal is enabled
0 = Card removal signal is masked

bit 6 **CARDIISE:** Card Insertion Interrupt Signal Enable bit
1 = Card insertion signal is enabled
0 = Card insertion signal is masked

bit 5 **BRRDYISE:** Buffer Read Ready Interrupt Signal Enable bit
1 = Buffer read ready signal is enabled
0 = Buffer read ready signal is masked

bit 4 **BWRDYISE:** Buffer Write Ready Interrupt Signal Enable bit
1 = Buffer write ready signal is enabled
0 = Buffer write ready signal is masked

bit 3 **DMAISE:** DMA Interrupt Signal Enable bit
1 = DMA interrupt signal is enabled
0 = DMA interrupt signal is masked

bit 2 **BGISE:** Block Gap Interrupt Signal Enable bit
1 = Block gap event signal is enabled
0 = Block gap event signal is masked

bit 1 **TXEISE:** Transfer Complete Interrupt Signal Enable bit
1 = Transfer complete signal is enabled
0 = Transfer complete signal is masked

bit 0 **CEISE:** Command Complete Interrupt Signal Enable bit
1 = Command complete signal is enabled
0 = Command complete signal is masked

REGISTER 39-12: SDHCSTAT2: SDHC STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HC	U-0	U-0	R-0, HC	R-0, HC	R-0, HC	R-0, HC	R-0, HC
	CNISSE	—	—	ACIDXE	ACEBE	ACCRCE	ACTOE	ACNEXEC

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **CNISSE:** Command Not Issued by Auto CMD12 Error bit
1 = Command was not issued
0 = No error

bit 6-5 **Unimplemented:** Read as ‘0’

bit 4 **ACIDXE:** Auto CMD12 Index Error bit
1 = Index error was generated
0 = Index error was not generated

bit 3 **ACEBE:** Auto CMD12 End Bit Error bit
1 = End bit error was generated
0 = End bit error was not generated

bit 2 **ACCRCE:** Auto CMD12 CRC Error bit
1 = CRC error was generated
0 = CRC error was not generated

bit 1 **ACTOE:** Auto CMD12 Time-out Error bit
1 = Time-out error was generated
0 = Time-out error was not generated

bit 0 **ACNEXEC:** Auto CMD12 Not Executed bit
1 = Auto CMD12 was not executed
0 = Auto CMD12 was executed

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REGISTER 39-13: SDHCCAP: SDHC CAPABILITIES REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-1	U-0	U-0	U-0	U-0	R-1, HS
	SLOTTYPE<1:0>		ASYNCINT	—	—	—	—	VOLT3V3
23:16	R-1, HS	U-1	R-1, HS	U-0	R-1, HS	U-0	R-0, HS	R-0, HS
	SRESUME	—	HISPEED	—	ADMA2	—	MBLEN<1:0>	
15:8	R-1, HS	R-1, HS	R-0, HS	R-0, HS	R-1, HS	R-0, HS	R-0, HS	R-0, HS
	BASECLK<7:0>							
7:0	R-1	U-0	R-0	R-1	R-1	R-0	R-0	R-1
	TOCLKU	—	TOCLKFREQ<5:0>					

Legend:		HS = Hardware settable	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **SLOTTYPE<1:0>:** Slot Type
- 11 = UHS-II Multiple Embedded Devices
- 10 = Shared Bus Slot (SD Mode)
- 01 = Embedded Slot for One Device
- 00 = Removable Card Slot

bit 29 **ASYNCINT:** Asynchronization Interrupt Support (SD Mode Only)
- 1 = Asynchronous Interrupt Supported
- 0 = Asynchronous Interrupt not Supported

bit 28-25 **Unimplemented:** Read as ‘0’

bit 24 **VOLT3V3:** 3.3V Voltage Support bit
- 1 = Voltage of 3.3V is supported

bit 23 **SRESUME:** Suspend/Resume Support bit
- 1 = Suspend/resume is supported
- 0 = Suspend/resume is not supported

bit 22 **Unimplemented:** Read as ‘1’

bit 21 **HISPEED:** High-Speed Support bit
- 1 = High speed is supported
- 0 = High speed is not supported

bit 20 **Unimplemented:** Read as ‘0’

bit 19 **ADMA2:** ADMA2 Support bit
- 1 = ADMA2 is supported
- 0 = ADMA2 is not supported

bit 18 **Unimplemented:** Read as ‘0’

bit 17-16 **MBLEN<1:0>:** Maximum Block Length bits
- 11 = Reserved
- 10 = 2048
- 01 = 1024
- 00 = 512

REGISTER 39-13: SDHCCAP: SDHC CAPABILITIES REGISTER (CONTINUED)

bit 15-8 **BASECLK<7:0>:** Base Clock Frequency for SDCLK bits

111111 = 63 MHz
111110 = 62 MHz
111101 = 61 MHz
•
•
•
000010 = 2 MHz
000001 = 1 MHz
000000 = Reserved

bit 7 **TOCLKU:** Time-out Clock Unit bit

1 = Time-out clock unit is in kHz
0 = Time-out clock unit is in MHz

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **TOCLKFREQ<5:0>:** Time-out Clock Frequency bits

The TOCLKU bit defines the unit, either kHz or MHz, of these bit values.

111111 = 63 kHz or 63 MHz
111110 = 62 kHz or 62 MHz
111101 = 61 kHz or 61 MHz
•
•
•
000010 = 2 kHz or 2 MHz
000001 = 1 kHz or 1 MHz
000000 = Reserved

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REGISTER 39-14: SDHCMAXCAP: SDHC MAXIMUM CURRENT CAPABILITIES REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x, HS	R-x, HS	R-x, HS	R-x, HS	R-x, HS	R-x, HS	R-x, HS	R-x, HS
	MC3V3<7:0>							

Legend:		HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **MC3V3<7:0>:** Maximum Current for 3.3V bits

11111111 = 1020 mA
11111110 = 1016 mA
11111101 = 1012 mA
.
.
.
00000011 = 12 mA
00000010 = 8 mA
00000001 = 4 mA
00000000 = Reserved

REGISTER 39-15: SDHCFE: SDHC FORCE EVENT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC	W-0, HC
	—	—	—	—	—	—	FEADE	FEACE
23:16	W-0, HC	W-0, HC	W-0, HC	W-0, HC	W-0, HC	W-0, HC	W-0, HC	W-0, HC
	FECLE	FEDEBE	FEDCRCE	FEDTOE	FEIDXE	FECEBE	FECCRCE	FECTOE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	W-0	U-0	U-0	W-0	W-0	W-0	W-0	W-0
	FECNIACE	—	—	FEACIDXE	FEACEBE	FEACCRCE	FEACTOE	FEACNEE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **FEADE:** Force Event for ADMA Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 24 **FEACE:** Force Event for Auto CMD 12 Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 23 **FECLE:** Force Event for Current-Limit Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 22 **FEDEBE:** Force Event for Data End Bit Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 21 **FEDCRCE:** Force Event for Data CRC Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 20 **FEDTOE:** Force Event for Data Time-out Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 19 **FEIDXE:** Force Event for Command Index Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 18 **FECEBE:** Force Event for Command End Bit Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 17 **FECCRCE:** Force Event for Command CRC Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 16 **FECTOE:** Force Event for Command Time-out Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 15-8 **Unimplemented:** Read as ‘0’

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REGISTER 39-15: SDHCFE: SDHC FORCE EVENT REGISTER (CONTINUED)

bit 7 **FECNIACE:** Force Event for Command Not Issued by Auto CMD12 Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **FEACIDXE:** Force Event for Auto CMD12 Index Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 3 **FEACEBE:** Force Event for Auto CMD12 End Bit Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 2 **FEACCRCE:** Force Event for Auto CMD12 CRC Error bit

bit 1 **FEACTOE:** Force Event for Auto CMD12 Time-out Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

bit 0 **FEACNEE:** Force Event for Auto CMD12 Not Executed Error bit
1 = Interrupt was generated
0 = Interrupt was not generated

REGISTER 39-16: SDHCADESTAT: SDHC ADMA ERROR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0, HC	R-0, HC	R-0, HC
	—	—	—	—	—	ADLMERR	ADERRST<1:0>	

Legend:		HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as ‘0’

bit 2 **ADLMERR:** ADMA Length Mismatch Error bit
1 = Length mismatch error has occurred
0 = Length mismatch error has not occurred

bit 1-0 **ADERRST<1:0>:** ADMA Error State bits
11 = Data transfer error
10 = Reserved
01 = Fetch descriptor error
00 = Stop DMA error

REGISTER 39-17: SDHCAADDR: SDHC ADMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **ADDR<31:0>:** ADMA Address Register bits
These bits contain the address of the executing command of the ADMA descriptor table.

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NOTES:

40.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

This section describes the power-saving features on the PIC32MZ DAK/DAL/DAR/DAS devices. These devices have multiple power domains and offer various methods and modes that allow the user to balance the power consumption with device performance.

40.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the speed of PBCLK7, or selecting a lower power clock source (that is, LPRC or SOSC).

In addition, the Peripheral Bus Scaling mode is available for each peripheral bus where peripherals are clocked at reduced speed by selecting a higher divider for the associated PBCLKx, or by disabling the clock completely.

40.2 Power-Saving with CPU Halted

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

40.2.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted and the associated clocks are disabled. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep mode.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the peripheral bus clocks will start running and the device will enter into Idle mode.

40.2.2 IDLE MODE

In Idle mode, the CPU is Halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

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40.2.3 DEEP SLEEP MODE

Deep Sleep mode brings the device into its lowest power consumption state without requiring the use of external switches to remove power from the device.

- **Deep Sleep**
  In this mode, the CPU, RAM and most peripherals are powered down. Power is maintained to the DSGPR0 register and one or more of the RTCC, DSWDT and DSGPR1 through DSGPR32 registers.

Which of these peripherals is active depends on the state of the following register bits when Deep Sleep mode is entered:

- **RTCDIS (DSCON<12>)**
  This bit must be set to disable the RTCC in Deep Sleep mode (see Register 40-1).
- **DSWDTEN (DEVCFG2<27>)**
  This Configuration bit must be set to enable the DSWDT register in Deep Sleep mode (see Register 41-5)
- **DSGPREN (DSCON<13>)**
  This bit must be set to enable the DSGPR1 through DSGPR32 registers in Deep Sleep mode (see Register 40-1).

Note:	The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, the Deep Sleep Control registers must be written twice.

In addition to the conditionally enabled peripherals described above, the $\overline{\text{MCLR}}$ filter and INT0 pin are enabled in Deep Sleep mode.

40.2.4 VBAT MODE

VBAT mode is similar to Deep Sleep mode, except that the device is powered from the VBAT pin. VBAT mode is controlled strictly by hardware, without any software intervention. Device enters VBAT mode upon VDDCORE Power-on Reset (refer to Table 44-4 for definitions of VPORCORE and VBATSW). An external power source must be connected to the VBAT pin before power is removed from VDDIO/VDDCORE to enter VBAT mode. VBAT is the lowest battery-powered mode that can maintain an RTCC. Wake-up from VBAT mode can only occur when VDDIO/VDDCORE is reapplied. The wake-up will appear to be a POR to the rest of the device.

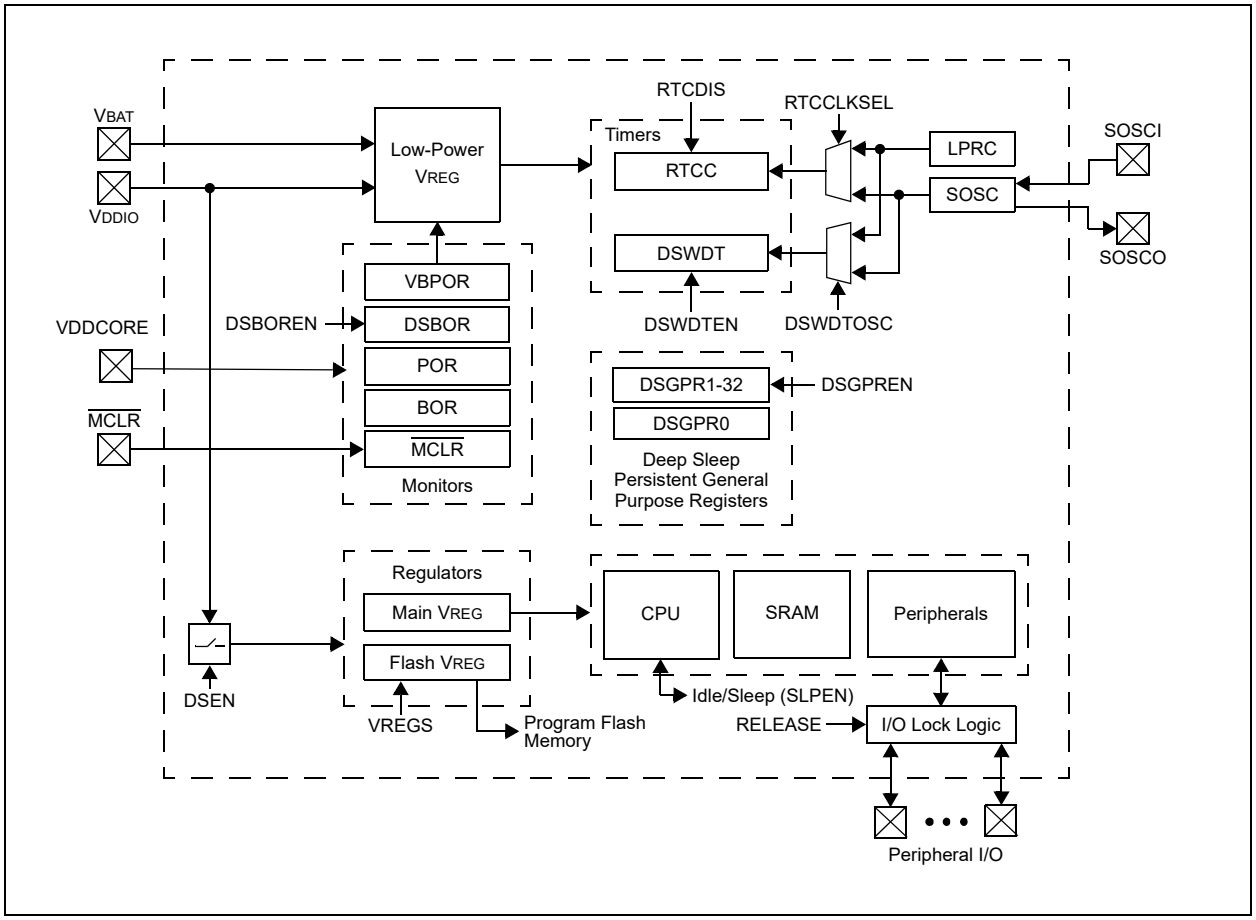
In VBAT mode, the Deep Sleep Watchdog Timer is disabled. The RTCC and DSGPR1 through DSGPR32 registers may be enabled or disabled depending on the state of the RTCDIS bit (DSCON<12>) and the DSGPREN bit (DSCON<13>), respectively. Deep Sleep Persistent General Purpose Register 0 (DSGPR0) is always enabled in VBAT mode.

40.2.5 XLP POWER-SAVING MODES

Figure 40-1 shows a block diagram of the system domain for XLP devices and the related power-saving features. The various blocks are controlled by the following Configuration bit settings and SFRs:

- DSBOREN (DEVCFG2<20>)
- DSEN (DSCON<15>)
- DSGPREN (DSCON<13>)
- DSWDTEN (DEVCFG2<27>)
- DSWDTOSC (DEVCFG2<26>)
- RELEASE (DSCON<0>)
- RTCCLKSEL (RTCCON <9:8>)
- RTCDIS (DSCON<12>)
- SLPEN (OSCCON<4>)
- VREGS (PWRCON<0>)

FIGURE 40-1: XLP DEVICE BLOCK DIAGRAM



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40.3 Deep Sleep (DSCTRL) Control Registers

TABLE 40-1: POWER-SAVING MODES REGISTER SUMMARY

Virtual Address (BF8C_#)	Register Name(2)	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	DSCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DSEN	—	DSGPREN	RTCDIS	—	—	—	RTCCWDIS	—	—	—	—	—	—	DSBOR	RELEASE	0000
0210	DSWAKE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	DSINT0	DSFLT	—	—	DSWDT	DSRTC	DSMCLR	—	—	0000
0220	DSGPR0(1)	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0240	DSGPR1	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0244	DSGPR2	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0248	DSGPR3	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
024C	DSGPR4	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0250	DSGPR5	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0254	DSGPR6	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0258	DSGPR7	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
025C	DSGPR8	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0260	DSGPR9	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0264	DSGPR10	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0268	DSGPR11	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice.

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TABLE 40-1: POWER-SAVING MODES REGISTER SUMMARY

Virtual Address (BF8C_#)	Register Name(2)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets(1)
026C	DSGPR12	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0270	DSGPR13	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0274	DSGPR14	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0278	DSGPR15	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
027C	DSGPR16	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0280	DSGPR17	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0284	DSGPR18	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0288	DSGPR19	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
028C	DSGPR20	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0290	DSGPR21	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0294	DSGPR22	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0298	DSGPR23	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
029C	DSGPR24	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02A0	DSGPR25	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02A4	DSGPR26	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice.

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TABLE 40-1: POWER-SAVING MODES REGISTER SUMMARY

Virtual Address (BF8C_#)	Register Name(2)	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
02A8	DSGPR27	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02AC	DSGPR28	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02B0	DSGPR29	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02B4	DSGPR30	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02B8	DSGPR31	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
02BC	DSGPR32	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice.

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REGISTER 40-1: DSCON: DEEP SLEEP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	HC, R/W-y	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	DSEN(1)	—	DSGPREN	RTCDIS	—	—	—	RTCCWDIS
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DSBOR(2)	RELEASE

Legend:	HC = Hardware Cleared	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **DSEN:** Deep Sleep Enable bit(1)
- 1 = Deep Sleep mode is entered on a WAIT instruction
- 0 = Sleep mode is entered on a WAIT instruction

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **DSGPREN:** General Purpose Registers Enable bit
- 1 = General purpose register retention is enabled in Deep Sleep mode
- 0 = No general purpose register retention in Deep Sleep mode

bit 12 **RTCDIS:** RTCC Module Disable bit
- 1 = RTCC module is not enabled
- 0 = RTCC module is enabled

bit 11-9 **Unimplemented:** Read as ‘0’

bit 8 **RTCCWDIS:** RTCC Wake-up Disable bit
- 1 = Wake-up from RTCC is disabled
- 0 = Wake-up from RTCC is enabled

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit(2)
- 1 = DSBOREN was enabled and VDDIO dropped below the DSBOR threshold during Deep Sleep(2)
- 0 = DSBOREN was disabled, or VDDIO did not drop below the DSBOR threshold during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit
- 1 = Upon waking from Deep Sleep, the I/O pins maintain their previous states
- 0 = Release I/O pins and allow their respective TRIS and LAT bits to control their states

Note 1: To enter Deep Sleep mode, Sleep mode must be executed after setting the DSEN bit.

2: Unlike all other events, a Deep Sleep Brown-out Reset (BOR) event will not cause a wake-up from Deep Sleep mode; this bit is present only as a status bit.

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REGISTER 40-2: DSWAKE: DEEP SLEEP WAKE-UP SOURCE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
	—	—	—	—	—	—	—	DSINT0
7:0	R/W-0, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0
	DSFLT	—	—	DSWDT	DSRTC	DSMCLR	—	—

Legend:		HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as ‘0’

bit 8 **DSINT0:** Interrupt-on-Change bit
1 = Interrupt-on-change was asserted during Deep Sleep
0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 **DSFLT:** Deep Sleep Fault Detected bit
1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted
0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as ‘0’

bit 4 **DSWDT:** Deep Sleep Watchdog Timer Time-out bit
1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep
0 = The Deep Sleep Watchdog Timer did not time-out during Deep Sleep

bit 3 **DSRTC:** Real-Time Clock and Calendar Alarm bit
1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep
0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 **DSMCLR:** $\overline{\text{MCLR}}$ Event bit
1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep
0 = The $\overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1-0 **Unimplemented:** Read as ‘0’

Note: All bits in this register are cleared when the DSEN bit (DSCON<15>) is set.

REGISTER 40-3: DSGPRX: DEEP SLEEP PERSISTENT GENERAL PURPOSE REGISTER 'x' (x = 0 THROUGH 32)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 Deep Sleep Persistent General Purpose bits

Note: The contents of the DSGPR0 register are retained, even in Deep Sleep and VBAT modes. The DSPGR1 through DSPGR32 registers are disabled by default in Deep Sleep and VBAT modes, but can be enabled with the DSGPREN bit (DSCON<13>). All register bits are reset only if a V_{DDCORE} Power-on Reset (POR) event outside of Deep-Sleep mode.

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40.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 40-2 for additional information.

Note: Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module through the PMDx bits.

Note: When a peripheral is disabled with the PMD register, it resets the Interrupt Enable Control (IECx) and Interrupt Priority Control (IPCx) registers. When the peripheral is re-enabled with the PMD register, the IECx and IPCx registers must be configured again.

TABLE 40-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0040	PMD1	31:16	—	—	—	HVD1V8	—	—	—	—	—	—	—	HLVDMD	—	—	—	—	0000
		15:0	—	—	—	CVRMD	—	—	—	CTMUMD	—	—	—	—	—	—	—	ADCMD	0000
0050	PMD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP2MD	CMP1MD	0000
0060	PMD3	31:16	—	—	—	—	—	—	—	OC9MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
		15:0	—	—	—	—	—	—	—	IC9MD	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
0070	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	T9MD	T8MD	T7MD	T6MD	T5MD	T4MD	T3MD	T2MD	T1MD	0000
0080	PMD5	31:16	—	—	CAN2MD	CAN1MD	—	—	—	USBMD	—	—	—	I2C5MD	I2C4MD	I2C3MD	I2C2MD	I2C1MD	0000
		15:0	—	—	SPI6MD	SPI5MD	SPI4MD	SPI3MD	SPI2MD	SPI1MD	—	—	U6MD	U5MD	U4MD	U3MD	U2MD	U1MD	0000
0090	PMD6	31:16	—	—	—	ETHMD	—	—	—	—	SQI1MD	—	SDHCMD	GLCDMD	—	GPUMD	EBIMD	PMPMD	0000
		15:0	—	—	—	REFO5MD	REFO4MD	REFO3MD	REFO2MD	REFO1MD	—	—	—	—	—	—	—	—	0000
00A0	PMD7	31:16	—	—	—	DDR2CMD	—	—	—	—	—	CRYPTMD	—	RNGMD	—	—	—	—	1000
		15:0	—	—	—	—	—	—	—	—	—	—	—	DMAMD	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

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TABLE 40-3: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral	PMDx Bit Name	Register Name and Bit Location
ADC	ADCMD	PMD1<0>
CTMU	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
High/Low-Voltage Detect	HLVDMD	PMD1<20>
HVD	HVD1V8	PMD1<28>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Input Capture 6	IC6MD	PMD3<5>
Input Capture 7	IC7MD	PMD3<6>
Input Capture 8	IC8MD	PMD3<7>
Input Capture 9	IC9MD	PMD3<8>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Output Compare 6	OC6MD	PMD3<21>
Output Compare 7	OC7MD	PMD3<22>
Output Compare 8	OC8MD	PMD3<23>
Output Compare 9	OC9MD	PMD3<24>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
Timer6	T6MD	PMD4<5>
Timer7	T7MD	PMD4<6>
Timer8	T8MD	PMD4<7>
Timer9	T9MD	PMD4<8>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
UART6	U6MD	PMD5<5>
SPI1	SPI1MD	PMD5<8>

Note 1: The USB module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

2: This peripheral is not available on all devices. Refer to the pin feature tables (Table 2 through Table 4) to determine availability.

TABLE 40-3: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS (CONTINUED)

Peripheral	PMDx Bit Name	Register Name and Bit Location
SPI2	SPI2MD	PMD5<9>
SPI3	SPI3MD	PMD5<10>
SPI4	SPI4MD	PMD5<11>
SPI5	SPI5MD	PMD5<12>
SPI6	SPI6MD	PMD5<13>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
I2C3	I2C3MD	PMD5<18>
I2C4	I2C4MD	PMD5<19>
I2C5	I2C5MD	PMD5<20>
USB(1)	USBMD	PMD5<24>
CAN1	CAN1MD	PMD5<28>
CAN2	CAN2MD	PMD5<29>
Reference Clock Output 1	REFO1MD	PMD6<8>
Reference Clock Output 2	REFO2MD	PMD6<9>
Reference Clock Output 3	REFO3MD	PMD6<10>
Reference Clock Output 4	REFO4MD	PMD6<11>
Reference Clock Output 5	REFO5MD	PMD6<12>
PMP	PMPMD	PMD6<16>
EBI	EBIMD	PMD6<17>
2-D GPU	GPUMD	PMD6<18>
GLCD	GLCDMD	PMD6<20>
SDHC	SDHCMD	PMD6<21>
SQI1	SQI1MD	PMD6<23>
Ethernet	ETHMD	PMD6<28>
DMA	DMAMD	PMD7<4>
RNG	RNGMD	PMD7<20>
Crypto(2)	CRYPTMD	PMD7<22>
DDR2 SDRAM Controller(2)	DDR2CMD	PMD7<28>

Note 1: The USB module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

2: This peripheral is not available on all devices. Refer to the pin feature tables (Table 2 through Table 4) to determine availability.

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40.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. The PIC32MZ DAK/DAL/DAR/DAS devices include two features to prevent alterations to enabled or disabled peripherals:

- Control Register Lock Sequence
- Configuration Bit Select Lock

40.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting the PMDLOCK bit prevents writes to the control registers and clearing the PMDLOCK bit allows writes.

To set or clear the PMDLOCK bit, an unlock sequence must be executed. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

40.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If the PMDLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

41.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129), which are available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 website (www.microchip.com/pic32).

The PIC32MZ DAK/DAL/DAR/DAS family of devices include the following key features intended to maximize application flexibility and reliability and minimize cost through elimination of external components.

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)
- Internal temperature sensor

41.1 Configuration Bits

The PIC32MZ DAK/DAL/DAR/DAS family of devices contain two Boot Flash memories (Boot Flash 1 and Boot Flash 2), each with an associated configuration space. These configuration spaces can be programmed to contain various device configurations. Configuration space that is aliased by the Lower Boot Alias memory region is used to provide values for the following Configuration registers. Refer to **4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

- DEVSIGN0/ADEVSIGN0: Device Signature Word 0 Register
- DEVCP0/ADEVCP0: Device Code-Protect 0 Register
- DEVCFG0/ADEVCFG0: Device/Alternate Device Configuration Word 0
- DEVCFG1/ADEVCFG1: Device Configuration Word 1
- DEVCFG2/ADEVCFG2: Device Configuration Word 2
- DEVCFG3/ADEVCFG3: Device Configuration Word 3
- DEVCFG4/ADEVCFG4: Device Configuration Word 4
- DEVADCx: Device ADC Calibration Word 'x' ('x' = 0-4, 7)

The following run-time programmable Configuration registers provide additional configuration control:

- CFGCON: Configuration Control Register
- CFGEBIA: External Bus Interface Address Pin Configuration Register
- CFGEBIC: External Bus Interface Control Pin Configuration Register
- CFGPG: Permission Group Configuration Register
- CFGCON2: Configuration Control Register 2
- CFGMPLL: Memory PLL Configuration Register

In addition, the DEVID register (see Register 41-15) provides device and revision information and the DEVSN0 and DEVSN3 registers contain a unique serial number of the device (see Register 41-16).

Note: Do not use word program operation (NVMOP<3:0> = `0001`) when programming the device words that are described in this chapter.

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41.2 Registers

TABLE 41-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FFBC	DEVCFG4	31:16	—	—	—	SWDTPS<4;0>					—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFC0	DEVCFG3	31:16	—	—	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN	—	—	—	—	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
FFC4	DEVCFG2	31:16	—	UPLLFSEL	—	FDSEN	DSWDTEN	DSWDTOSC	DSWDTPS<4:0>					DSBOREN	—	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
FFC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
FFCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	POSCAGC	—	POSCTYPE<1:0>		—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>		—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
FFD0	DEVCP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD4	DEVCP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFD8	DEVCP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFDC	DEVCP0	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE0	DEVSIGN3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE4	DEVSIGN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFE8	DEVSIGN1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FFEC	DEVSIGN0	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 41-2: ADEVCFG: ALTERNATE DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FF3C	ADEVCFG4	31:16	—	—	—	SWDTPS<4;0>					—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF40	ADEVCFG3	31:16	—	—	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN	—	—	—	—	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
FF44	ADEVCFG2	31:16	—	UPLLFSEL	—	FDSEN	DSWDTEN	DSWDTOSC	DSWDTPS<4:0>					DSBOREN	—	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
FF48	ADEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
FF4C	ADEVCFG0	31:16	—	EJTAGBEN	—	—	POSCAGC	—	POSCTYPE<1:0>		—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>		—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
FF50	ADEVCP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF54	ADEVCP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF58	ADEVCP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF5C	ADEVCP0	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF60	ADEVSIGN3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF64	ADEVSIGN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF68	ADEVSIGN1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
FF6C	ADEVSIGN0	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 41-3: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets(1)
0000	CFGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	USBSSEN	IOANCPEN	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0000
00C0	CFGEBIA	31:16	—	—	—	—	—	—	—	—	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN	0000
		15:0	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN	0000
00D0	CFGEBIC	31:16	EBI RDYINV3	EBI RDYINV2	EBI RDYINV1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—	—	—	—	—	—	—	EBI RDYLVL	EBIRPEN	0000
		15:0	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0	0000
00E0	CFGPG	31:16	—	—	GPUPG<1:0>		GLCDPG<1:0>		CRYPTPG<1:0>		FCPG<1:0>		SQI1PG<1:0>		SDHCPG<1:0>		ETHPG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		—	—	USBPG<1:0>		—	—	DMAPG<1:0>		—	—	CPUPG<1:0>		0000
00F0	CFGCON2	31:16	GLCDPINEN	GLCDMODE	SDCDEN	SDWPEN	—	—	SDWRFTHR<9:0>										0000
		15:0	—	—	SDRDFTHR<9:0>										—	SDWPPOL	—	GPURESET	0000
0100	CFGMPLL	31:16	MPLLRDY	MPLLDIS	MPLLODIV2<2:0>			MPLLODIV1<2:0>			MPLL VREGRDY	MPLL VREGDIS	—	—	—	—	—	—	7F40
		15:0	MPLLMULT<7:0>								INTVREFCON<1:0>		MPLLIDIV<5:0>						FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: Reset values are dependent on the specific device.

TABLE 41-4: DEVICE SERIAL NUMBER SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets(1)
4020	DEVSN0	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx
4024	DEVSN1	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx
4028	DEVSN2	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx
402C	DEVSN3	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: Reset values are dependent on the device variant.

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TABLE 41-5: DEVICE ADC CALIBRATION SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	DEVADC0	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
4004	DEVADC1	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
4008	DEVADC2	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
400C	DEVADC3	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
4010	DEVADC4	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
401C	DEVADC7	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx

Legend: x = unknown value on Reset.
Note 1: Reset values are dependent on the device variant.

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REGISTER 41-1: DEVSIGN0/ADEVSIGN0: DEVICE SIGNATURE WORD 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as ‘0’

bit 30-0 **Reserved:** Write as ‘1’

Note: The DEVSIGN1 through DEVSIGN3 registers, and ADEVSIGN1 through ADEVSIGN3 registers are used for Quad Word programming operation when programming the DEVSIGN0/ADESIGN0 registers, and do not contain any valid information.

REGISTER 41-2: DEVCP0/ADEVCP0: DEVICE CODE-PROTECT 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	R/P	r-1	r-1	r-1	r-1
	—	—	—	CP	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Reserved:** Write as ‘1’

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection is disabled
0 = Protection is enabled

bit 27-0 **Reserved:** Write as ‘1’

Note: The DEVCP1 through DEVCP3 registers, and ADEVCP1 through ADEVCP3 registers are used for Quad Word programming operation when programming the DEVCP0/ADEVCP0 registers, and do not contain any valid information.

REGISTER 41-3: DEVCFG0/ADEVCFG0: DEVICE/ALTERNATE DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-x	R/P	r-1	r-1	R/P	r-1	R/P	R/P
	—	EJTAGBEN	—	—	POSCAGC	—	POSCAGCDLY<1:0>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	POSCFGAIN<1:0>		POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>	
15:8	R/P	R/P	R/P	R/P	r-y	R/P	R/P	R/P
	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>	
7:0	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>	

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** The reset value of this bit is the same as DEVSIGN0<31>.

bit 30 **EJTAGBEN:** EJTAG Boot Enable bit

`1` = Normal EJTAG functionality
`0` = Reduced EJTAG functionality

bit 29-28 **Reserved:** Write as ‘`1`’

bit 27 **POSCAGC:** Primary Oscillator Automatic Gain Control bit

`1` = Automatic gain control is enabled (default)
`0` = Manual oscillator gain control

When the POSCAGC bit is enabled and POSC HS mode is selected, DEVCFG1<9:8> = ‘`0b10` (i.e., POSCMOD), the Primary Oscillator will automatically do a linear search to find the lowest power/gain setting to guarantee oscillation with the users crystal.

Note: If the POSCMOD<1:0> bits (DEVCFG1/ADEVCFG1<9:8>_ = ‘`0b00` (i.e., POSCMOD = EC mode), the POSCAGC bit must be set to ‘`0`’. POSCMOD = EC mode with POSCAGC = `1` is not permitted and will result in no oscillation.

bit 26 **Reserved:** Write as ‘`1`’

bit 25-24 **POSCAGCDLY<1:0>:** Primary Crystal AGC Gain Search Step Settling Time Control bits

`11` = Approximately (25 ms, default)
`10` = Approximately (6.25 ms)
`01` = Approximately (400 ms)
`00` = Approximately (100 ms)

Note 1: When the POSCAGC bit (DEVCFG0<27>) = `0` (i.e., manual oscillator gain control), these bits are not used. They are only used when AGC is enabled.

2: For POSC HS mode (DEVCFG1<9:8> = ‘`0b10`), the default setting should meet the user crystal requirements. Internally, there are a maximum of 16 and a minimum of one AGC linear gain search steps the logic may utilize before locking. A lock will occur when the crystal is oscillating and the amplitude of the crystal signal is between a max and min fixed internal threshold. The POSCAGCDLY is the time for each of the possible AGC search steps settling time to allow the crystal to startup and amplitude stabilize before determining if a lock is true or to continue to search for the required gain. The POSCAGCDLY<1:0> bits represent a balance between start-up time and crystal power optimization. The lower the POSCAGCDLY delay time the faster the crystal start-up time but potentially at a higher crystal power level. The higher the POSCAGCDLY delay time the slower the crystal start-up time but with a better crystal power optimization level (i.e., less power).

3: For resonators, due to their long start-up times it may be necessary to use a longer AGC gain step settling time. Note that resonators are not validated on PIC32MZ DAK/DAL/DAR/DAS devices.

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REGISTER 41-3: DEVCFG0/ADEVCFG0: DEVICE/ALTERNATE DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 23-22 **POSCFGAIN<1:0>:** Primary Crystal Oscillator Fine Gain Control bits

11 = Gain is G3 (default)
10 = Gain is G2
01 = Gain is G1
00 = Gain is G0

Note 1: G3 > G2 > G1 > G0.

2: When the POSCAGC bit (DEVCFG0<27>) = 1 (i.e., automatic gain control), or the POSCMOD<1:0> bits (DEVCFG1/ADEVCFG1<9:8>) ≠ ‘0b10 (i.e., HS Crystal mode), the POSCGAIN<1:0> bits are not used.

3: These bits are used in conjunction with DEVCFG0/ADEVCFG0<20:19>. In almost all cases, the crystal fine gain default setting of ‘0b11 will work with the users course gain setting selection.

bit 21 **POSCBOOST:** Primary Oscillator Boost bit

1 = Uses internal XTAL feedback gain resistor (Default, in which case the user application should not use any external XTAL feedback resistor in the crystal circuit)
0 = Disconnects the internal XTAL feedback resistor

bit 20-19 **POSCGAIN<1:0>:** Primary Crystal Oscillator Coarse Gain Control bits

11 = Gain Level 3 (highest)
10 = Gain Level 2
01 = Gain Level 1
00 = Gain Level 0 (lowest)

Note 1: G3 > G2 > G1 > G0.

2: When the POSCAGC bit (DEVCFG0<27>) = 1 (i.e., automatic gain control), or the POSCMOD<1:0> bits (DEVCFG1/ADEVCFG1<9:8>) ≠ ‘0b10 (i.e., HS crystal mode), the POSCGAIN<1:0> bits are not used.

bit 18 **SOSCBOOST:** Secondary Oscillator Kick Start Programmability bit

1 = Start up and operate with high-power SOSC internal buffer only. This option will consume more current than allowed in the XLP specifications.
0 = Start up with internal SOSC high-power buffer, and then switch to low-power buffer when the SOSC is stable.

bit 17-16 **SOSCGAIN<1:0>:** Secondary Oscillator Gain Control bits

If SOSCGAIN<2> = 0:
11 = Gain is G3 (default)
10 = Gain is G2
01 = Gain is G1
00 = Gain is G0

Note: G3 > G2 > G1 > G0.

bit 15 **SMCLR:** Soft Master Clear Enable bit

1 = MCLR pin generates a normal system Reset
0 = MCLR pin generates a POR

bit 14-12 **DBGPER<2:0>:** Debug Mode CPU Access Permission bits

1xx = Allow CPU access to Permission Group 2 permission regions
x1x = Allow CPU access to Permission Group 1 permission regions
xx1 = Allow CPU access to Permission Group 0 permission regions
0xx = Deny CPU access to Permission Group 2 permission regions
x0x = Deny CPU access to Permission Group 1 permission regions
xx0 = Deny CPU access to Permission Group 0 permission regions

Note: When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** This bit is controlled by debugger/emulator development tools and should not be modified by the user.

REGISTER 41-3: DEVCFG0/ADEVCFG0: DEVICE/ALTERNATE DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 10 **FSLEEP:** Flash Sleep Mode bit

1 = Flash is powered down when the device is in Sleep mode
0 = Flash power down is controlled by the VREGS bit (PWRCON<0>)

bit 9-8 **FECCCON<1:0>:** Dynamic Flash ECC Configuration bits

11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

Note: Upon a device POR, the value of these bits are copied by hardware into CFGCON<5:4> bits, (i.e. ECCCON<1:0>.

bit 7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit

1 = Boot code and Exception code is MIPS32
(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
0 = Boot code and Exception code is microMIPS
(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit

1 = Trace features in the CPU are enabled
0 = Trace features in the CPU are disabled

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits

11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit

1 = JTAG is enabled
0 = JTAG is disabled

Note 1: On Reset, this Configuration bit is copied into JTAGEN (CFGCON<3>). If JTAGEN (DEVCFG0<2>) = 0, the JTAGEN bit cannot be set to '1' by the user application at run-time, as JTAG is always disabled. However, if JTAGEN (DEVCFG0<2>) = 1, the user application may enable/disable JTAG at run-time by simply writing JTAGEN (CFGCON<3> as required.

2: This bit sets the value of the JTAGEN bit in the CFGCON register.

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)

11 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Disabled
10 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Enabled
01 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Disabled
00 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Enabled

Note: When the FJTAGEN or JTAGEN bits are equal to '0', this prevents 4-wire JTAG debugging, but not PGECx/PGEDx debugging.

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REGISTER 41-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>				
15:8	R/P	R/P	r-1	r-1	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	IESO	FSOSCEN	DMTINV<2:0>			FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **FDMTEN:** Deadman Timer enable bit
`1` = Deadman Timer is enabled and *cannot* be disabled by software
`0` = Deadman Timer is disabled and *can* be enabled by software

Note: Once set, the DMTCON.ON bit cannot be disabled by software.

bit 30-26 **DMTCNT<4:0>:** Deadman Timer Count Select bits
`11111` = Reserved
.
.
.
`11000` = Reserved
`10111` = 2^{31} (2147483648)
`10110` = 2^{30} (1073741824)
`10101` = 2^{29} (536870912)
`10100` = 2^{28} (268435456)
.
.
.
`00001` = 2^{9} (512)
`00000` = 2^{8} (256)

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
`11` = Window size is 25%
`10` = Window size is 37.5%
`01` = Window size is 50%
`00` = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
`1` = Watchdog Timer is enabled and cannot be disabled by software
`0` = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
`1` = Watchdog Timer is in non-Window mode
`0` = Watchdog Timer is in Window mode

bit 21 **WDTSPGM:** Watchdog Timer Stop During Flash Programming bit
`1` = Watchdog Timer stops during Flash programming
`0` = Watchdog Timer runs during Flash programming (for read/execute while programming Flash applications)

REGISTER 41-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitoring Selection Configuration bits

11 = Software Clock switching is enabled and clock monitoring is enabled
10 = Software Clock switching is disabled and clock monitoring is enabled
01 = Software Clock switching is enabled and clock monitoring is disabled
00 = Software Clock switching is disabled and clock monitoring is disabled

bit 13-11 **Reserved:** Write as '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit

1 = CLKO output is disabled
0 = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits

11 = POSC is disabled
10 = HS Oscillator mode is selected
01 = Reserved
00 = EC mode is selected (this mode must not be selected if the POSCAGC bit (DEVCFG0/ADEVCFG0<27>) is equal to '1')

bit 7 **IESO:** Internal External Switchover bit

1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **FSOSCEN:** Secondary Oscillator Enable bit

1 = Enable SOSC
0 = Disable SOSC

bit 5-3 **DMTINV<2:0>:** Deadman Timer Count Window Interval bits

111 = Window/Interval value is 127/128 counter value
110 = Window/Interval value is 63/64 counter value
101 = Window/Interval value is 31/32 counter value
100 = Window/Interval value is 15/16 counter value
011 = Window/Interval value is 7/8 counter value
010 = Window/Interval value is 3/4 counter value
001 = Window/Interval value is 1/2 counter value
000 = Window/Interval value is zero

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REGISTER 41-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits

111 = SPLL
110 = Reserved
101 = LPRC
100 = Sosc
011 = Reserved
010 = Posc (HS, EC)
001 = SPLL
000 = FRC divided by FRCDIV<2:0> bits (FRCDIV)

REGISTER 41-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/P	r-1	R/P	R/P	R/P	R/P	R/P
	—	UPLLFSEL	—	FDSEN	DSWDTEN	DSWDTOSC	DSWDTPS<4:3>	
23:16	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	DSWDTPS<2:0>			DSBOREN	—	FPLLODIV<2:0>		
15:8	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	FPLLMULT<6:0>						
7:0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as ‘1’

bit 30 **UPLLFSEL:** USB PLL Input Frequency Select bit
1 = UPLL input clock is 24 MHz
0 = UPLL input clock is 12 MHz

bit 29 **Reserved:** Write as ‘1’

bit 28 **FDSEN:** Deep Sleep Enable bit
1 = Deep Sleep mode is entered on a `WAIT` instruction
0 = Sleep mode is entered on a `WAIT` instruction

Note: User must clear this bit to '0' to prevent CPU going into Deep Sleep mode on a WAIT instruction.

bit 27 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit
1 = Enable the Deep Sleep Watchdog Timer (DSWDT) during Deep Sleep mode
0 = Disable the DSWDT during Deep Sleep mode

bit 26 **DSWDTOSC:** Deep Sleep Watchdog Timer Reference Clock Select bit
1 = Select the LPRC Oscillator as the DSWDT reference clock
0 = Select the Secondary Oscillator as the DSWDT reference clock

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REGISTER 41-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 25-21 **DSWDTPS<4:0>:** Deep Sleep Watchdog Timer Postscale Select bits

11111 = $1:2^{36}$
11110 = $1:2^{35}$
11101 = $1:2^{34}$
11100 = $1:2^{33}$
11011 = $1:2^{32}$
11010 = $1:2^{31}$
11001 = $1:2^{30}$
11000 = $1:2^{29}$
10111 = $1:2^{28}$
10110 = $1:2^{27}$
10101 = $1:2^{26}$
10100 = $1:2^{25}$
10011 = $1:2^{24}$
10010 = $1:2^{23}$
10001 = $1:2^{22}$
10000 = $1:2^{21}$
01111 = $1:2^{20}$
01110 = $1:2^{19}$
01101 = $1:2^{18}$
01100 = $1:2^{17}$
01011 = $1:2^{16}$
01010 = $1:2^{15}$
01001 = $1:2^{14}$
01000 = $1:2^{13}$
00111 = $1:2^{12}$
00110 = $1:2^{11}$
00101 = $1:2^{10}$
00100 = $1:2^{9}$
00011 = $1:2^{8}$
00010 = $1:2^{7}$
00001 = $1:2^{6}$
00000 = $1:2^{5}$

bit 20 **DSBOREN:** Deep Sleep BOR Enable bit

1 = Enable BOR during Deep Sleep mode
0 = Disable BOR during Deep Sleep mode

bit 19 **Reserved:**Write as ‘1’

bit 18-16 **FPLLODIV<2:0>:** Default System PLL Output Divisor bits

111 = PLL output divided by 32
110 = PLL output divided by 32
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 2

bit 15 **Reserved:** Write as ‘1’

REGISTER 41-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 14-8 **FPLLMULT<6:0>:** System PLL Feedback Divider bits

1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

bit 7 **FPLLICLK:** System PLL Input Clock Select bit

1 = FRC is selected as input to the System PLL
0 = POSC is selected as input to the System PLL

bit 6-4 **FPLLRNG<2:0>:** System PLL Divided Input Clock Frequency Range bits

111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

bit 3 **Reserved:** Write as '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

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REGISTER 41-6: DEVCFG3/ADEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	R/P	R/P	R/P	r-1	R/P	R/P
	—	—	IOL1WAY	PMDL1WAY	PGL1WAY	—	FETHIO	FMIIEN
23:16	r-1	r-1	r-1	r-1	R/P	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-30 **Reserved:** Write as ‘1’

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27 **PGL1WAY:** Permission Group Lock One Way Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 26 **Reserved:** Write as ‘1’

bit 25 **FETHIO:** Ethernet I/O Pin Selection Configuration bit
1 = Default Ethernet I/O pins
0 = Alternate Ethernet I/O pins

This bit is ignored for devices that do not have an alternate Ethernet pin selection.

bit 24 **FMIIEN:** Ethernet MII Enable Configuration bit
1 = MII is enabled
0 = RMII is enabled

bit 23-16 **Reserved:** Write as ‘1’

bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

REGISTER 41-7: DEVCFG4/ADEVCFG4: DEVICE CONFIGURATION WORD 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	R/P	R/P	R/P	R/P	R/P
	—	—	—	SWDTPS<4:0>				
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Reserved:** Write as ‘1’

bit 29-24 **SWDTPS<4:0>:** Sleep Mode Watchdog Timer Postscale Select bits

10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

bit 31-29 **Reserved:** Write as ‘1’

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REGISTER 41-8: DEVADCx: DEVICE ADC CALIBRATION WORD ‘x’ (‘x’ = 0-4, 7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	ADCFG<31:24>							
23:16	R	R	R	R	R	R	R	R
	ADCFG<23:16>							
15:8	R	R	R	R	R	R	R	R
	ADCFG<15:8>							
7:0	R	R	R	R	R	R	R	R
	ADCFG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **ADCFG<31:0>:** Calibration Data for the ADC Module bits

This data must be copied to the corresponding ADCxCFG register. Refer to **Section 28.0 “Pipelined Analog-to-Digital Converter (ADC)”** for more information.

REGISTER 41-9: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	ICACLK(1)	OCACLK(1)
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	IOLOCK(1)	PMDLOCK(1)	PGLOCK(1)	—	—	USBSSEN(1)
7:0	R/W-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	U-0	R/W-1
	IOANCPEN	—	ECCCON<1:0>		JTAGEN(2)	TROEN	—	TDOEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-18 **Unimplemented:** Read as ‘0’

bit 17 **ICACLK:** Input Capture Alternate Clock Selection bit(1)

1 = Input Capture modules use an alternative Timer pair as their timebase clock
0 = All Input Capture modules use Timer2/3 as their timebase clock

bit 16 **OCACLK:** Output Compare Alternate Clock Selection bit(1)

1 = Output Compare modules use an alternative Timer pair as their timebase clock
0 = All Output Compare modules use Timer2/3 as their timebase clock

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit(1)

1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.

bit 12 **PMDLOCK:** Peripheral Module Disable bit(1)

1 = Peripheral module is locked. Writes to PMD registers is not allowed.
0 = Peripheral module is not locked. Writes to PMD registers is allowed.

bit 11 **PGLOCK:** Permission Group Lock bit(1)

1 = Permission Group registers are locked. Writes to PG registers are not allowed.
0 = Permission Group registers are not locked. Writes to PG registers are allowed.

bit 10-9 **Unimplemented:** Read as ‘0’

bit 8 **USBSSEN:** USB Suspend Sleep Enable bit(1)

Enables features for USB PHY clock shutdown in Sleep mode.

1 = USB PHY clock is shut down when Sleep mode is active
0 = USB PHY clock continues to run when Sleep is active

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. “Oscillators with Enhanced PLL”** (DS60001250) in the *“PIC32 Family Reference Manual”* for details.

2: The JTAGEN bit is only available at run-time when the JTAGEN (DEVCFG0<2>) fuse bit is set at start-up.

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REGISTER 41-9: CFGCON: CONFIGURATION CONTROL REGISTER (CONTINUED)

bit 7 **IOANCPEN:** I/O Analog Charge Pump Enable bit

1 = Charge pumps are enabled
0 = Charge pumps are disabled

Note 1: For proper analog operation at VDD is less than 2.5V, the AICPMPEN bit (ADCCON1<12>) must be = 1 and the IOANCPEN bit must be set to '1'; however, the charge pumps will consume additional current. These bits should not be set if VDD is greater than 2.5V.

2: ADC throughput rate performance is reduced as defined in the table below if ADCCON1<AICPMPEN> = 1 and CFGCON<IOANCPEN> = 1.

ADC0	ADC1	ADC2	ADC3	ADC4	ADC7	Maximum combined
ON	OFF	OFF	OFF	OFF	OFF	2 MSPS
ON	ON	OFF	OFF	OFF	OFF	4 MSPS
ON	ON	ON	OFF	OFF	OFF	5 MSPS
OFF	OFF	OFF	ON	OFF	OFF	2 MSPS
OFF	OFF	OFF	ON	ON	OFF	4 MSPS
OFF	OFF	OFF	ON	ON	ON	5 MSPS
ON	ON	ON	ON	OFF	OFF	7 MSPS
ON	ON	ON	ON	ON	OFF	9 MSPS
ON	ON	ON	ON	ON	ON	10 MSPS

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **ECCCON<1:0>:** Flash ECC Configuration bits

11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

bit 3 **JTAGEN:** JTAG Port Enable bit(2)

1 = Enable the JTAG port
0 = Disable the JTAG port

bit 2 **TROEN:** Trace Output Enable bit

1 = Enable trace outputs and start trace clock (trace probe must be present)
0 = Disable trace outputs and stop trace clock

bit 1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG

1 = 2-wire JTAG protocol uses TDO
0 = 2-wire JTAG protocol does not use TDO

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: The JTAGEN bit is only available at run-time when the JTAGEN (DEVCFG0<2>) fuse bit is set at start-up.

REGISTER 41-10: CFGEBIA: EXTERNAL BUS INTERFACE ADDRESS PIN CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-0 **EBIA23EN:EBIA0EN:** EBI Address Pin Enable bits

1 = EBIAx pin is enabled for use by EBI
0 = EBIAx pin has is available for general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

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REGISTER 41-11: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0
	EBI RDYINV3	EBI RDYINV2	EBI RDYINV1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	EBIRDYLVL	EBIRPEN
15:8	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **EBIRDYINV3:** EBIRDY3 Inversion Control bit
1 = Invert EBIRDY3 pin before use
0 = Do not invert EBIRDY3 pin before use

bit 30 **EBIRDYINV2:** EBIRDY2 Inversion Control bit
1 = Invert EBIRDY2 pin before use
0 = Do not invert EBIRDY2 pin before use

bit 29 **EBIRDYINV1:** EBIRDY1 Inversion Control bit
1 = Invert EBIRDY1 pin before use
0 = Do not invert EBIRDY1 pin before use

bit 28 **Unimplemented:** Read as ‘0’

bit 27 **EBIRDYEN3:** EBIRDY3 Pin Enable bit
1 = EBIRDY3 pin is enabled for use by the EBI module
0 = EBIRDY3 pin is available for general use

bit 26 **EBIRDYEN2:** EBIRDY2 Pin Enable bit
1 = EBIRDY2 pin is enabled for use by the EBI module
0 = EBIRDY2 pin is available for general use

bit 25 **EBIRDYEN1:** EBIRDY1 Pin Enable bit
1 = EBIRDY1 pin is enabled for use by the EBI module
0 = EBIRDY1 pin is available for general use

bit 24-18 **Unimplemented:** Read as ‘0’

bit 17 **EBIRDYLVL:** EBIRDYx Pin Sensitivity Control bit
1 = Use level detect for EBIRDYx pins
0 = Use edge detect for EBIRDYx pins

bit 16 **EBIRPEN:** $\overline{\text{EBIRP}}$ Pin Sensitivity Control bit
1 = $\overline{\text{EBIRP}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIRP}}$ pin is available for general use

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **EBIWEEN:** $\overline{\text{EBIWE}}$ Pin Enable bit
1 = $\overline{\text{EBIWE}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIWE}}$ pin is available for general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

REGISTER 41-11: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER (CONTINUED)

bit 12 **EBIOEEN:** $\overline{\text{EBIOE}}$ Pin Enable bit
1 = $\overline{\text{EBIOE}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIOE}}$ pin is available for general use

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **EBIBSEN1:** $\overline{\text{EBIBS1}}$ Pin Enable bit
1 = $\overline{\text{EBIBS1}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIBS1}}$ pin is available for general use

bit 8 **EBIBSEN0:** $\overline{\text{EBIBS0}}$ Pin Enable bit
1 = $\overline{\text{EBIBS0}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIBS0}}$ pin is available for general use

bit 7 **EBICSEN3:** $\overline{\text{EBICS3}}$ Pin Enable bit
1 = $\overline{\text{EBICS3}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS3}}$ pin is available for general use

bit 6 **EBICSEN2:** $\overline{\text{EBICS2}}$ Pin Enable bit
1 = $\overline{\text{EBICS2}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS2}}$ pin is available for general use

bit 5 **EBICSEN1:** $\overline{\text{EBICS1}}$ Pin Enable bit
1 = $\overline{\text{EBICS1}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS1}}$ pin is available for general use

bit 4 **EBICSEN0:** $\overline{\text{EBICS0}}$ Pin Enable bit
1 = $\overline{\text{EBICS0}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS0}}$ pin is available for general use

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **EBIDEN1:** EBI Data Upper Byte Pin Enable bit
1 = EBID<15:8> pins are enabled for use by the EBI module
0 = EBID<15:8> pins have reverted to general use

bit 0 **EBIDEN01:** EBI Data Upper Byte Pin Enable bit
1 = EBID<7:0> pins are enabled for use by the EBI module
0 = EBID<7:0> pins have reverted to general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

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REGISTER 41-12: CFGPG: PERMISSION GROUP CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	GPUPG<1:0>		GLCDPG<1:0>		CRYPTPG<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FCPG<1:0>		SQI1PG<1:0>		SDHCPG<1:0>		ETHPG<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	CAN2PG<1:0>		CAN1PG<1:0>		—	—	USBPG<1:0>	
7:0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	DMAPG<1:0>		—	—	CPUPG<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 31-30 **Unimplemented:** Read as ‘0’

bit 29-28 **GPUPG<1:0>:** 2D Graphics Processing Unit Permission Group bits
- 11 = Initiator is assigned to Permission Group 3
- 10 = Initiator is assigned to Permission Group 2
- 01 = Initiator is assigned to Permission Group 1
- 00 = Initiator is assigned to Permission Group 0

bit 27-26 **GLCDPG<1:0>:** Graphics LCD Controller Permission Group bits
Same definition as bits 29-28.

bit 25-24 **CRYPTPG<1:0>:** Crypto Engine Permission Group bits
Same definition as bits 29-28.

bit 23-22 **FCPG<1:0>:** Flash Control Permission Group bits
Same definition as bits 29-28.

bit 21-20 **SQI1PG<1:0>:** SQI Module Permission Group bits
Same definition as bits 29-28.

bit 19-18 **SDHCPG<1:0>:** Secure Digital Host Controller Permission Group bits
Same definition as bits 29-28.

bit 17-16 **ETHPG<1:0>:** Ethernet Module Permission Group bits
Same definition as bits 29-28.

bit 15-14 **CAN2PG<1:0>:** CAN2 Module Permission Group bits
Same definition as bits 29-28.

bit 13-12 **CAN1PG<1:0>:** CAN1 Module Permission Group bits
Same definition as bits 29-28.

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9-8 **USBPG<1:0>:** USB Module Permission Group bits
Same definition as bits 29-28.

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DMAPG<1:0>:** DMA Module Permission Group bits
Same definition as bits 29-28.

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **CPUPG<1:0>:** CPU Permission Group bits
Same definition as bits 29-28.

REGISTER 41-13: CFGCON2: CONFIGURATION CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	GLCDPINEN	GLCDMODE(1)	SDCDEN	SDWPEN	—	—	SDWRFTHR<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SDWRFTHR<7:0>							
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	SDRDFTHR<9:4>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	r-1	R/W-0	U-0	R/W-0
	SDRDFTHR<3:0>				—	SDWPPOL	—	GPURESET

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **GLCDPINEN:** Graphics Display Pin Enable bit
1 = GLCD pins are used by the GLCD module
0 = GLCD pins are available for general purpose use

bit 30 **GLCDMODE:** Graphics Display Mode bit(1)
1 = GLCD pins are set to RGB565 mode. Other GDx pins are available for general purpose use.
0 = GLCD pins are set to RGB888 mode

bit 29 **SDCDEN:** SD Card Detect Pin Enable bit
1 = $\overline{\text{SDCD}}$ pin is enabled for use by SDHC
0 = $\overline{\text{SDCD}}$ pin is available for general purpose use

bit 28 **SDWPEN:** SD card Write Protect Enable bit
1 = $\overline{\text{SDWP}}$ pin is enabled for use by SDHC
0 = $\overline{\text{SDWP}}$ pin is available for general purpose use

bit 27-26 **Unimplemented:** Read as ‘0’

bit 25-16 **SDWRFTHR<9:0>:** SDHC Write FIFO Threshold bits
SDHC FIFO threshold value in bytes (FIFO size is 512 bytes).

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-4 **SDRDFTHR<9:0>:** SDHC Read FIFO Threshold bits
SDHC FIFO threshold value in bytes (FIFO size is 512 bytes).

bit 3 **Reserved:** Read as ‘1’

bit 2 **SDWPPOL:** SD card Write Protect Polarity bit
1 = $\overline{\text{SDWP}}$ pin is Active-High
0 = $\overline{\text{SDWP}}$ pin is Active-Low

Note: This bit supports SD cards with different write-protect polarity types.

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **GPURESET:** GPU Reset Bit
1 = Hold GPU in RESET
0 = Release RESET to the GPU module

Note: This bit is only used if the GPU functionality is to be enabled or disabled at run-time. Writing to this bit requires the GPUMD bit (PMD6<18>) be set to '0' (GPU is enabled).

Note 1: To use GLCD in RGB888 mode, the GLCDMODE bit should be set to ‘0’, which will turn-off the general purpose I/O functionality on six additional pins. Refer to the specific package in **“Device Pin Tables”** for information on GDx pin sharing.

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REGISTER 41-14: CFGMPLL: MEMORY PLL CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	MPLLRDY	MPLLDIS	MPLLODIV2<2:0>			MPLLODIV1<2:0>		
23:16	R-0	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
	MPLL VREGRDY	MPLL VREGDIS	—	—	—	—	—	—
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	MPLLMULT<7:0>							
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	INTVREFCON<1:0>		MPLLIDIV<5:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **MPLLRDY:** Memory PLL Status bit
- 1 = MPLL clock is stable and is ready for use
- 0 = MPLL clock is not ready. Initializing DDR2 SDRAM when the clock is not ready will result in undefined behavior.

bit 30 **MPLLDIS:** MPLL Disable bit
- 1 = MPLL is disabled
- 0 = MPLL is enabled

Note: Clear this bit only after the MPLLVREGRDY bit is set to ‘1’.

bit 29-27 **MPLLODIV2<2:0>:** MPLL Output Divider 2 bits
- 111 = MPLL second stage output is divided by 7
- 110 = MPLL second stage output is divided by 6
- 101 = MPLL second stage output is divided by 5
- 100 = MPLL second stage output is divided by 4
- 011 = MPLL second stage output is divided by 3
- 010 = MPLL second stage output is divided by 2
- 001 = MPLL second stage output is divided by 1
- 000 = Reserved

Note: The Value in this field must be less than MPLLODIV1. Unless it is necessary, setting these bits to '001' (MPLL second stage output is divided by 1) will produce less clock jitter.

bit 26-24 **MPLLODIV1<2:0>:** MPLL Output Divider 1 bits
See bits 29-27 for available selections.

bit 23 **MPLLVREGRDY:** MPLL Voltage Regulator Ready bit
- 1 = MPLL voltage regulator is ready for use
- 0 = MPLL voltage regulator is not ready or is disabled

bit 22 **MPLLVREGDIS:** MPLL Voltage regulator Disable bit
- 1 = MPLL voltage regulator is disabled
- 0 = MPLL voltage regulator is enabled

bit 21-16 **Unimplemented:** Read as ‘0’

REGISTER 41-14: CFGMPLL: MEMORY PLL CONFIGURATION REGISTER (CONTINUED)

bit 15-8 **MPLLMULT<7:0>:** MPLL Multiplier bits

11111111 = Reserved
11111110 = Reserved
•
•
•
10100001 = Reserved
10100000 = Multiply by 160
10011111 = Multiply by 159
•
•
•
00010000 = Multiply by 16
00001111 = Reserved
•
•
•
00000000 = Reserved

bit 7-6 **INTVREFCON<1:0>:** Internal DDRV$_{REF}$ Control bits

11 = Enable the internal DDRVREF circuit and drive the DDRVREF pin to VDDR1V8/2
10 = Disable the internal DDRV$_{REF}$ circuit and drive the DDRVREF pin to V$_{SS1V8}$
01 = Disable the internal DDRV$_{REF}$ circuit and drive the DDRVREF pin to V$_{DDR1V8}$
00 = Use the external DDRV$_{REF}$ circuit

Note 1: Set the INTVREFCON<1:0> bits to the desired state before applying V$_{DDR1V8}$.

2: Add 0.1 uF and 0.01 uF capacitors in parallel between the DDRVREF pin and ground, when the DDRVREF pin is used. When external reference is selected, the DDRVREF pin can be provided by dividing VDDR1V8 by 1K ohm +/-1% resistor divider.

bit 5-0 **MPLLIDIV<5:0>:** MPLL Input Divider bits

111111 = MPLL input clock is divider by 63
111110 = MPLL input clock is divider by 62
•
•
•
000001 = MPLL input clock is divider by 1
000000 = Reserved

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REGISTER 41-15: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0>(1)				DEVID<27:24>(1)			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16>(1)							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8>(1)							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID(1)

Note 1: See the *“PIC32 Flash Programming Specification”* (DS60001145) for a list of Revision and Device ID values.

REGISTER 41-16: DEVSNx: DEVICE SERIAL NUMBER REGISTER ‘x’ (‘x’ = 0, 1,2,3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	SN<31:24>							
23:16	R	R	R	R	R	R	R	R
	SN<23:16>							
15:8	R	R	R	R	R	R	R	R
	SN<15:8>							
7:0	R	R	R	R	R	R	R	R
	SN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **SN<31:0>:** Device Unique Serial Number bits

Note: These registers contain a value, programmed during factory production test, that is unique to each unit and are user read only. These values are persistent and not erased even when a new application code is programmed into the device. These values can be used if desired as an encryption key in combination with the Microchip encryption library.

41.3 High-Voltage Detect (HVD1V8) on VDDR1V8

The High-Voltage Detect (HVD) module monitors the DDR2 PHY voltage at the VDDR1V8 supply voltage (1.8V). If a dangerously high voltage is detected, the device is held in reset as long as the HVD condition persists.

Recovery from an HVD event is indicated by the HVD1V8R bit (RCON<29>).

41.4 On-Chip Voltage Regulator

The core and digital logic for all PIC32MZ DA devices is designed to operate at a nominal 1.2V. To simplify system designs, devices in the PIC32MZ DAK/DAL/DAR/DAS family incorporate an on-chip regulator providing the required core logic voltage from VDDCORE.

41.4.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

41.4.2 ON-CHIP REGULATOR AND BOR

PIC32MZ DAK/DAL/DAR/DAS devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset (BOR). This event is captured by the BOR Flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 44.1 "DC Characteristics"**.

41.5 On-chip Temperature Sensor

PIC32MZ DA devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **Section 44.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **Section 29.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** for more information).

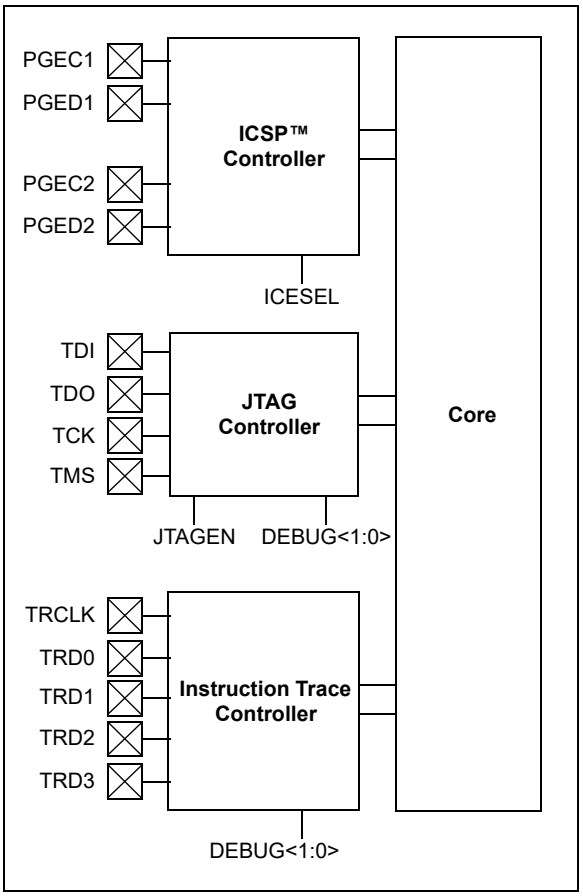
41.6 Programming and Diagnostics

PIC32MZ DAK/DAL/DAR/DAS devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 41-1: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS



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NOTES:

42.0 INSTRUCTION SET

The PIC32MZ Graphics (DAK/DAL/DAR/DAS) Family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32MZ DAK/DAL/DAR/DAS family *does not* support the following features:

- Core extend instructions
- Coprocessor 2 instructions

Note:	Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set" which is available for download* at www.imgtec.com for more information.

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NOTES:

43.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

43.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

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43.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8-bit, 16-bit, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

43.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

43.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

43.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

43.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

43.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

43.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

43.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

43.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDIOMIN}$ and $V_{DDIOMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

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43.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip website (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

43.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

44.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MZ DAK/DAL/DAR/DAS electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MZ DAK/DAL/DAR/DAS devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

ABSOLUTE MAXIMUM RATINGS

(see Note1)

Ambient temperature under bias ..... -40°C to +105°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DDIO}, V_{DDCORE}, and V_{BAT} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on V_{DDR1V8} pin with respect to V_{SS1V8} ..... -0.5V to +1.98V
Voltage on DDR2 pins with respect to V_{SS1V8} ..... -0.3V to (V_{DDR1V8} + 0.3V)
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DDIO} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DDIO} \geq 2.2V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DDIO} < 2.2V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on D+ or D- pin with respect to V_{USB3V3} ..... -0.3V to (V_{USB3V3} + 0.3V)
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +5.5V
Maximum current out of V_{SS} pin(s) ..... 500 mA
Maximum current into V_{DDIO} pin(s) **(Note 2)** ..... 200 mA
Maximum current into VDDCORE pin(s) **(Note 2)** ..... 300 mA
Maximum current into VDDR1V8 pin(s) **(Note 2)** ..... 270 mA
Maximum current out of VSS1V8 pin(s) ..... 270 mA
Maximum current sunk/sourced by DDR2 pin ..... 22 mA
Maximum current sunk/sourced by any 4x I/O pin **(Note 4)** ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin **(Note 4)** ..... 25 mA
Maximum current sunk/sourced by any 12x I/O pin **(Note 4)** ..... 33 mA
Maximum current sunk by all ports **(Note 5)** ..... 150 mA
Maximum current sourced by all ports **(Note 2, Note 5)** ..... 150 mA

ESD Qualification:

Human Body Model (HBM) per JESD22-A114 ..... 2000V
Machine Model (MM) per JESD22-A115 ..... 200V
Changed Device Model (CDM) AEC Q100-011 (ANSI/ESD STM 5.3.1) 500V

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 44-2).

3: See the pin name tables (Table 4 through Table 7) for the 5V tolerant pins.

4: Characterized, but not tested. Refer to parameters DO10, DO20, and DO20a for the 4x, 8x, and 12x I/O pin lists.

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44.1 DC Characteristics

TABLE 44-1: OPERATING MIPS VS. VOLTAGE

Characteristic	V_{DDIO} Range (in Volts) (Note 1)	V_{DDCORE} Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comments
				PIC32MZ DAK/DAL/ DAR/DAS Devices	
DC5	2.2V-3.6V	1.7V-1.9V	-40°C to +105°C	200 MHz	—

Note 1: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages. Refer to Table 44-5 for Reset values.

TABLE 44-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
V-Temperature Devices					
Operating Junction Temperature Range	T_J	-40	—	+130	°C
Operating Ambient Temperature Range	T_A	-40	—	+105	°C
Power Dissipation: Internal Chip Power Dissipation (Device without internal DDR2): $P_{INT} = V_{DDIO} \times (I_{DDIO} - \Sigma I_{OH}) + V_{DDCORE} \times I_{DDCORE}$ Internal Chip Power Dissipation (Device with internal DDR2): $P_{INT} = V_{DDIO} \times (I_{DDIO} - \Sigma I_{OH}) + V_{DDCORE} \times I_{DDCORE} + V_{DDR1V8} \times I_{DDR1V8}$ **I/O Pin Power Dissipation:** $P_{I/O} = \Sigma (\{V_{DDIO} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 44-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typ.	Max.	Unit
Package Thermal Resistance, 169-pin LFBGA (11x11x1.4 mm)(1)	θ_{JA}	25	—	°C/W
Package Thermal Resistance, 169-pin LFBGA (11x11x1.56 mm)(1,2)	θ_{JA}	23.5	—	°C/W
Package Thermal Resistance, 176-pin LQFP (20x20x1.45 mm)(1)	θ_{JA}	20	—	°C/W

Note 1: Junction to ambient thermal resistance, Theta-JA (θ_{JA}) numbers are achieved by package simulations.

2: Devices with internal DDR2 SDRAM.

TABLE 44-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	V_{DDIO}	I/O Supply Voltage **(Note 1)**	2.2	—	3.6	V	—
DC11	V_{DDCORE}	Core Supply Voltage **(Note 1)**	1.7	1.8	1.9	V	—
DC12	SV_{DDIO}/ SV_{DDCORE}	**V_{DDIO}/V_{DDCORE} Rise Rate** to Ensure Internal Power-on Reset Signal **(Note 2)**	0.000011	—	1.1	V/µs	300 ms to 3 µs @ 3.3v
DC13	V_{BAT}	Battery Supply Voltage	2.2	—	3.6	V	—
DC14	V_{DDR1V8}	DDR Memory Supply Voltage	1.7	1.8	1.9	V	—
DC15	$DDRV_{REF}$(3)	DDR Reference Voltage	0.49 x V_{DDR1V8}	0.50 x V_{DDR1V8}	0.51 x V_{DDR1V8}	V	—

Note 1: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages. Refer to Table 44-5 for Reset values.

2: Voltage on V_{DDIO} must always be greater than or equal to V_{DDCORE} during power-up.

3: Add 0.1 uF and 0.01 uF capacitors in parallel between the DDRVREF pin and ground, when the DDRVREF pin is used. When external reference is selected, the DDRVREF pin can be provided by dividing VDDR1V8 by 1K ohm +/-1% resistor divider.

TABLE 44-5: ELECTRICAL CHARACTERISTICS: RESETS

DC CHARACTERISTICS (Note 1)			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
RST10	V_{PORIO}	V_{DDIO} POR Voltage **(Note 2)**	—	—	1.80	V	—
RST11	$V_{PORCORE}$ /V_{BATSW}	V_{DDCORE} POR Voltage **(Note 2)** V_{DDCORE} to V_{BAT} Switch Voltage **(Note 3)**	—	—	Vss+0.3	V	Failure to meet this specification when power cycling the part may lead to unexpected and abnormal behavior.
RST12	V_{BORIO}	BOR Event on V_{DDIO} transition high-to-low **(Note 4)**	1.89	—	1.95	V	—
RST13	V_{PORBAT}	POR Event on V_{BAT} **(Note 4)**	1.35	—	2.0	V	—
RST14	V_{HVD1V8}	High Voltage Detect on V_{DDR1V8} pins	2.16	—	2.24	V	—
RST15	$V_{BORCORE}$	BOR Event on V_{DDCORE} transition high-to-low **(Note 4)**	1.59	—	1.67	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: This is the limit to which V_{DDIO}/V_{DDCORE} must be lowered to ensure Power-on Reset.

3: Device enters VBAT mode upon V_{DDCORE} Power-on Reset.

4: Overall functional device operation below operating voltages guaranteed (but not characterized) until Reset is issued. All device Analog modules, when enabled, will function, but with degraded performance below operating voltages.

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TABLE 44-6: LOW-VOLTAGE DETECT CHARACTERISTICS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp					
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
LV10	V_{HLVD}	HLVD Voltage on V_{DDIO} Transition high to low	HLVDL<3:0> = 0100(1)	3.45	3.52	3.59	V	—
			HLVDL<3:0> = 0101	3.12	3.29	3.40	V	—
			HLVDL<3:0> = 0110	2.94	3.00	3.05	V	—
			HLVDL<3:0> = 0111	2.74	2.79	2.85	V	—
			HLVDL<3:0> = 1000	2.65	2.70	2.75	V	—
			HLVDL<3:0> = 1001	2.45	2.50	2.55	V	—
			HLVDL<3:0> = 1010	2.35	2.40	2.49	V	—
			HLVDL<3:0> = 1011	2.26	2.30	2.4	V	—
LV11	V_{THL}	Voltage on HLVDIN Pin Transition	HLVDL<3:0> = 1111	1.98	1.20	1.22	V	—

Note 1: Trip points for values of LVD<3:0>, from ‘0000’ to ‘0011’, are not implemented, and ‘1100,’ ‘1101’ to ‘1110’ are reserved.

TABLE 44-7: DC CHARACTERISTICS: OPERATING CURRENT

DC CHARACTERISTICS(1,2)			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp	
Parameter No.	**Typical(3)**	**Maximum**	**Units**	**Conditions**
I/O Operating Current (I_{DDIO}): Peripherals Enabled (PMDx=0, ON(PBxDIV<15>)=1)				
DC20	1.2	1.7	mA	8 MHz
DC21	1.8	2.2	mA	100 MHz(4)
DC22	2.7	3.3	mA	200 MHz
DC23	2.7	3.3	mA	200 MHz (L1 Cache and Prefetch modules disabled)(4)
I/O Operating Current (I_{DDCORE}): Peripherals Enabled (PMDx=0, ON(PBxDIV<15>)=1)				
DC20a	20	45	mA	8 MHz
DC21a	78	106	mA	100 MHz(4)
DC22a	144	172	mA	200 MHz
DC23a	127	154	mA	200 MHz (L1 Cache and Prefetch modules disabled)(4)
I/O Operating Current (I_{DDIO}): Peripherals Disabled (PMDx=1, ON(PBxDIV<15>)=0)				
DC24	1.2	1.7	mA	8 MHz,
DC25	1.8	2.2	mA	100 MHz(4)
DC26	2.7	3.3	mA	200 MHz
DC27	2.7	3.3	mA	200 MHz (L1 Cache and Prefetch modules disabled)(4)
I/O Operating Current (I_{DDCORE}): Peripherals Disabled (PMDx=1, ON(PBxDIV<15>)=0)				
DC24a	18	37	mA	8 MHz, Maximum column value is at +85°C
DC24b	18	44	mA	8 MHz, Maximum column value is at +105°C
DC25a	57	85	mA	100 MHz(4)
DC26a	105	133	mA	200 MHz
DC27a	90	114	mA	200 MHz (L1 Cache and Prefetch modules disabled)(4)

Note 1: A device's I_{DD} supply current is mainly a function of the operating voltage and frequency. Other factors, such as Peripheral Bus Clock (PBCLK) frequency, number of peripheral modules enabled, internal code execution pattern, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for I_{DD} measurements are as follows:
- V_{DDR1V8} = 1.8V
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin. MPLL is turned OFF.
- USB PLL is disabled (USBMD = `1`), V_{USB3V3} is connected to V_{SS}
- CPU, Program Flash, and SRAM data memory are operational, Program Flash memory Wait states are equal to two
- L1 Cache and Prefetch modules are enabled, unless otherwise specified in conditions.
- No peripheral modules are operating, (Module internal ON bit = `0`)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}. DDR2 controller and DDR2 memory both are not initialized and are in default state.
- $\overline{MCLR}$ = V_{DDIO}
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled
- I/O Analog Charge Pump is disabled (IOANCPEN bit (CFGCON<7>) = `0`)
- ADC Input Charge Pump is disabled (AICPMPEN bit (ADCCON1<12> = `0`)
- All Peripheral Bus Clocks, except PBCLK7, are disabled (ON bit (PBxDIV<15>) = `0`, x = 2 through 6)

3: Data in "Typical" column is at 3.3V, +25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: This parameter is characterized, but not tested in manufacturing.

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TABLE 44-8: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})				
DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp	
Parameter No.	**Typical(2)**	**Maximum**	**Units**	**Conditions**
Idle Current (I_{IDLE}): Core Off, Clock on Base Current (1)				
DC30	18	35	mA	8 MHz(3), Maximum column value is at +85°C
DC30a	18	43	mA	8MHz(3), Maximum column value is at +105°C
DC31	45	70	mA	100 MHz(3)
DC32	70	123	mA	200 MHz
DDR2 Controller and DDR2 memory IDLE current (4)				
DC33	18	30	mA	MPLL is turned OFF

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- V_{DDR1V8} = 1.8V
- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}, PBCLKx divisor = 1:2 ('x' ≠ 7)
- CPU is in Idle mode (CPU core Halted)
- No peripheral modules are operating, (Module internal ON bit = 0), but the associated PMD bit is cleared (except USBMD)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}. DDR2 controller and DDR2 memory both are not initialized and are in default state.
- $\overline{MCLR}$ = V_{DDIO}
- RTCC and JTAG are disabled
- I/O Analog Charge Pump is disabled (IOANCPEN bit (CFGCON<7>) = 0)
- ADC Input Charge Pump is disabled (AICPMPEN bit (ADCCON1<12> = 0)

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

4: Applicable only to devices with internal DDR2.

TABLE 44-9: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS(1,2)			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp		
Param. No.	**Typical(2)**	**Maximum**	**Units**	**Conditions**	
Power-Down Current (I_{PD}) (Note 1)					
DC40k	7.5	14	mA	-40°C	Sleep(1)
DC40l	8	14	mA	+25°C	
DC40m	15	25	mA	+85°C	
DC40n	19	36	mA	+105°C	
Module Differential Current					
DC44a	50	350	μA	3.6V	Watchdog Timer Current: ΔI_{WDT}(3)
DC44b	3.5	5	mA	3.6V	ADC Current: ΔI_{ADC}(3,4)
DC44c	50	350	μA	3.6V	Deadman Timer Current: ΔI_{DMT}

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}
- CPU is in Sleep mode
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (Module internal ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DDIO}
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0; IOANCPEN = 0)

2: Data in the “Typical” column is at 3.3V, unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Voltage regulator is operational (VREGS = 1).

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TABLE 44-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
	V_{IL}	**Input Low Voltage**					
DI10		I/O Pins with PMP	V_{SS}	—	0.15 * V_{DDIO}	V	—
		I/O Pins	V_{SS}	—	0.2 * V_{DDIO}	V	—
DI18		SDAx, SCLx	V_{SS}	—	0.3 * V_{DDIO}	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	V_{SS}	—	0.8	V	SMBus enabled **(Note 4)**
	V_{IH}	**Input High Voltage**					
DI20		I/O Pins not 5V-tolerant(5)	0.65 * V_{DDIO}	—	V_{DDIO}	V	**(Note 4)**
		I/O Pins 5V-tolerant with PMP(5)	0.65 * V_{DDIO}	—	5.5	V	**(Note 4)**
		I/O Pins 5V-tolerant(5)	0.65 * V_{DDIO}	—	5.5	V	—
DI28a		SDAx, SCLx on non-5V tolerant pins(5)	0.65 * V_{DDIO}	—	V_{DDIO}	V	SMBus disabled **(Note 4)**
DI29a		SDAx, SCLx on non-5V tolerant pins(5)	2.1	—	V_{DDIO}	V	SMBus enabled, 2.2V ≤ V_{PIN} ≤ 5.5 **(Note 4)**
DI28b		SDAx, SCLx on 5V tolerant pins(5)	0.65 * V_{DDIO}	—	5.5	V	SMBus disabled **(Note 4)**
DI29b		SDAx, SCLx on 5V tolerant pins(5	2.1	—	5.5	V	SMBus enabled, 2.2V ≤ V_{PIN} ≤ 5.5 **(Note 4)**
DI30	I_{CNPU}	**Pull-up Current**	-460	-300	-50	µA	V_{DDIO} = 3.3V, V_{PIN} = V_{SS}
DI31	I_{CNPD}	**Pull-down Current(4)**	50	175	400	µA	V_{DDIO} = 3.3V, V_{PIN} = V_{DDIO}
	I_{IL}	**Input Leakage Current (Note 3)**					
DI50		I/O Ports	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DDIO}, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DDIO}, Pin at high-impedance
DI55		$\overline{MCLR}$(2)	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DDIO}
DI56		OSC1	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DDIO}, HS mode

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the pin name tables (Table 4 through Table 7) for the 5V-tolerant pins.

TABLE 44-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO10	V_{OL}	**Output Low Voltage** I/O Pins 4x Sink Driver Pins - RA0-RA3, RA9, RA10, RA14, RA15 RB0, RB4, RB6, RB7, RB10, RB11, RB12, RB14 RC12,RC15 RD6, RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8, RF12 RG15 RH0, RH1, RH4-RH14 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	0.4	V	I_{OL} ≤ 10 mA, V_{DDIO} = 3.3V
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA4, RA5 RB2, RB3, RB5, RB8, RB9, RB13, RB14, RB15 RC1-RC4 RD0-RD3, RD9, RD10, RD12, RD13 RE0-RE7 RF0, RF1, RF4, RF5, RF13 RG0, RG1, RG6, RG7, RG8, RG9 RH2, RH3, RH7, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	0.4	V	I_{OL} ≤ 15 mA, V_{DDIO} = 3.3V
		Output Low Voltage I/O Pins: 12x Sink Driver Pins - RA6, RA7 RD4, RD5 RG12-RG14	—	—	0.4	V	I_{OL} ≤ 20 mA, V_{DDIO} = 3.3V

Note 1: Parameters are characterized, but not tested.

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TABLE 44-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO20	VOH	**Output High Voltage** I/O Pins 4x Sink Driver Pins - RA0-RA3, RA9, RA10, RA14, RA15 RB0, RB4, RB6, RB7, RB10, RB11, RB12, RB14 RC12, RC15 RD6, RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8, RF12 RG15 RH0, RH1, RH4-RH14 RJ0-RJ2, RJ8, RJ9, RJ11	2.4	—	—	V	IOH ≥ -10 mA, VDDIO = 3.3V
		Output High Voltage I/O Pins: 8x Sink Driver Pins - RA4, RA5 RB2, RB3, RB5, RB8, RB9, RB13, RB14, RB15 RC1-RC4 RD0-RD3, RD9, RD10, RD12, RD13 RE0-RE7 RF0, RF1, RF4, RF5, RF13 RG0, RG1, RG6, RG7, RG8, RG9 RH2, RH3, RH7, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	2.4	—	—	V	IOH ≥ -15 mA, VDDIO = 3.3V
		Output High Voltage I/O Pins: 12x Source Driver Pins - RA6, RA7 RD4, RD5 RG12-RG14	2.4	—	—	V	IOH ≥ -20 mA, VDDIO = 3.3V

Note 1: Parameters are characterized, but not tested.

TABLE 44-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO20a	V_{OH1}	**Output High Voltage** I/O Pins 4x Sink Driver Pins - RA0-RA3, RA9, RA10, RA14, RA15 RB0, RB4, RB6, RB7, RB10, RB11, RB12, RB14 RC12-RC15 RD6, RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8, RF12 RG15 RH0, RH1, RH4-RH14 RJ0-RJ2, RJ8, RJ9, RJ11	1.5	—	—	V	I_{OH} ≥ -14 mA, V_{DDIO} = 3.3V
			2.0	—	—	V	I_{OH} ≥ -12 mA, V_{DDIO} = 3.3V
			3.0	—	—	V	I_{OH} ≥ -7 mA, V_{DDIO} = 3.3V
		Output High Voltage I/O Pins: 8x Sink Driver Pins - RA4, RA5 RB2, RB3, RB5, RB8, RB9, RB10, RB13, RB14, RB15 RC1-RC4 RD0-RD3, RD9, RD10, RD12, RD13 RE0-RE7 RF0, RF1, RF4, RF5, RF13 RG0, RG1, RG6, RG7, RG8, RG9 RH2, RH3, RH7, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	1.5	—	—	V	I_{OH} ≥ -22 mA, V_{DDIO} = 3.3V
			2.0	—	—	V	I_{OH} ≥ -18 mA, V_{DDIO} = 3.3V
			3.0	—	—	V	I_{OH} ≥ -10 mA, V_{DDIO} = 3.3V
		Output High Voltage I/O Pins: 12x Source Driver Pins - RA6, RA7 RD4, RD5 RG12-RG14	1.5	—	—	V	I_{OH} ≥ -32 mA, V_{DDIO} = 3.3V
			2.0	—	—	V	I_{OH} ≥ -25 mA, V_{DDIO} = 3.3V
			3.0	—	—	V	I_{OH} ≥ -14 mA, V_{DDIO} = 3.3V

Note 1: Parameters are characterized, but not tested.

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TABLE 44-12: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DI60a	I_{ICL}	**Input Low Injection Current**	0	—	-5(2,5)	mA	This parameter applies to all pins, with the exception of RB10. Maximum I_{ICH} current for this exception is 0 mA.
DI60b	I_{ICH}	**Input High Injection Current**	0	—	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, SOSCI, and RB10. Maximum I_{ICH} current for these exceptions is 0 mA.
DI60c	$\sum I_{ICT}$	**Total Input Injection Current (sum of all I/O and control pins)**	-20(6)	—	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| I_{ICL} + | I_{ICH} |) ≤ $\sum I_{ICT}$

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: V_{IL} source < (V_{SS} - 0.3). Characterized but not tested.

3: V_{IH} source > (V_{DDIO} + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to V_{DDIO}, and therefore, cannot tolerate any “positive” input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., V_{IH} Source > (V_{DDIO} + 0.3) or V_{IL} source < (V_{SS} - 0.3)).

6: Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, I_{ICL} = (((Vss - 0.3) - V_{IL} source) / Rs). If **Note 3**, I_{ICH} = ((I_{ICH} source - (V_{DDIO} + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (V_{SS} - 0.3) ≤ V_{SOURCE} ≤ (V_{DDIO} + 0.3), injection current = 0.

TABLE 44-13: SD HOST CONTROLLER I/O SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SD10	V_{OH}	Output High Voltage	2.4	—	—	V	I_{OH} ≥ 20 mA, V_{DDIO} = 3.3V
SD11	V_{OL}	Output Low Voltage	—	—	0.4	V	I_{OL} ≤ 20 mA, V_{DDIO} = 3.3V
SD12	V_{IH}	Input High Voltage	0.65*V_{DDIO}	—	V_{DDIO}	V	—
SD13	V_{IL}	Input Low Voltage	V_{SS}	—	0.2*V_{DDIO}	V	—

TABLE 44-14: DC CHARACTERISTICS: PROGRAM MEMORY(3)

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
D130a	E_P	Cell Endurance	10,000	—	—	E/W	Without ECC
D130b			20,000	—	—	E/W	With ECC
D131	V_{PR}	V_{DDCORE} for Read	$V_{DDCOREMIN}$	—	$V_{DDCOREMAX}$	V	—
D132	V_{PEW}	V_{DDCORE} for Erase or Write	$V_{DDCOREMIN}$	—	$V_{DDCOREMAX}$	V	—
D134a	T_{RETD}	Characteristic Retention	10	—	—	Year	Without ECC
D134b			20	—	—	Year	With ECC
D135	I_{DDP}	Supply Current during Programming	—	—	30	mA	—
D136	T_{RW}	Row Write Cycle Time **(Notes 2, 4)**	—	66813	—	FRC Cycles	—
D137	T_{QWW}	Quad Word Write Cycle Time **(Note 4)**	—	773	—	FRC Cycles	—
D138	T_{WW}	Word Write Cycle Time **(Note 4)**	—	383	—	FRC Cycles	—
D139	T_{CE}	Chip Erase Cycle Time **(Note 4)**	—	515373	—	FRC Cycles	—
D140	T_{PFE}	All Program Flash (Upper and Lower regions) Erase Cycle Time **(Note 4)**	—	256909	—	FRC Cycles	—
D141	T_{PBE}	Program Flash (Upper or Lower regions) Erase Cycle Time **(Note 4)**	—	128453	—	FRC Cycles	—
D142	T_{PGE}	Page Erase Cycle Time **(Note 4)**	—	128453	—	FRC Cycles	—

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: The minimum PBCLK5 for row programming is 4 MHz.

3: Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

4: Translating this value to seconds depends on FRC accuracy (see Table 44-26) and FRC tuning values (see the OSCTUN register: Register 8-2).

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TABLE 44-15: DC CHARACTERISTICS: PROGRAM FLASH MEMORY WAIT STATES

DC CHARACTERISTICS	Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp		
Required Flash Wait States(1)	**SYSCLK**	**Units**	**Conditions**
With ECC:			
0 Wait states	0 < SYSCLK ≤ 60	MHz	—
1 Wait state	60 < SYSCLK ≤ 120		
2 Wait states	120 < SYSCLK ≤ 200		
Without ECC:			
0 Wait states	0 < SYSCLK ≤ 74	MHz	—
1 Wait state	74 < SYSCLK ≤ 140		
2 Wait states	140 < SYSCLK ≤ 200		

Note 1: To use Wait states, the Prefetch module must be enabled (PREFEN<1:0> ≠ 00) and the PFMWS<2:0> bits must be written with the desired Wait state value.

TABLE 44-16: DC CHARACTERISTICS: DDR2 SDRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No. (Note 1)	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DDRM12	I_{DD0}	Operating Current, One Bank Active Precharge	—	—	60	mA	**Note 2**
DDRM13	I_{DD1}	Operating Current, One Bank Active-Read Precharge	—	—	70	mA	**Note 2**
DDRM14	I_{DD2}	Precharge Power-Down Current	—	—	6	mA	**Note 3**
DDRM15	I_{DD3}	Precharge Stand-by Current	—	—	40	mA	**Note 2**
DDRM16	I_{DD4}	Precharge Quiet Stand-by Current	—	—	35	mA	**Note 4**
DDRM17	I_{DD5}	Active Power-Down Current	—	—	15	mA	**Note 3**
DDRM18	I_{DD6}	Active Stand-by Current	—	—	50	mA	**Note 2**
DDRM19	I_{DD7}	Operating Burst Read Current	—	—	105	mA	**Note 2**
DDRM20	I_{DD8}	Operating Burst Write Current	—	—	110	mA	**Note 2**
DDRM21	I_{DD9}	Burst Refresh Current	—	—	70	mA	**Note 2**

Note 1: These parameters are characterized, but not tested in manufacturing. The specifications are only valid after the memory is initialized.

2: DDRCKE is high, $\overline{\text{DDRCS0}}$ is high between valid commands. Address, control, and data bus inputs are switching.

3: DDRCKE is low. Other control and address inputs are stable. Data bus inputs are floating.

4: DDRCKE is high and $\overline{\text{DDRCS0}}$ is high. Other control and address inputs are stable. Data bus inputs are floating.

5: DDRCKE is low and DDRCK/$\overline{\text{DDRCK}}$ are low. Other control and address inputs are floating. Data bus inputs are floating.

6: DDRCKE is high and $\overline{\text{DDRCS0}}$ is high between valid commands. Address bus inputs are stable. Data bus inputs are switching.

TABLE 44-16: DC CHARACTERISTICS: DDR2 SDRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No. (Note 1)	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DDRM22	I_{DD10}	Self-Refresh Current	—	—	6	mA	**Note 5**
DDRM23	I_{DD11}	Operating Bank Interleave Read Current	—	—	135	mA	**Note 6**

Note 1: These parameters are characterized, but not tested in manufacturing. The specifications are only valid after the memory is initialized.

2: DDRCKE is high, $\overline{\text{DDRCS0}}$ is high between valid commands. Address, control, and data bus inputs are switching.

3: DDRCKE is low. Other control and address inputs are stable. Data bus inputs are floating.

4: DDRCKE is high and $\overline{\text{DDRCS0}}$ is high. Other control and address inputs are stable. Data bus inputs are floating.

5: DDRCKE is low and DDRCK/$\overline{\text{DDRCK}}$ are low. Other control and address inputs are floating. Data bus inputs are floating.

6: DDRCKE is high and $\overline{\text{DDRCS0}}$ is high between valid commands. Address bus inputs are stable. Data bus inputs are switching.

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TABLE 44-17: COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±10	—	mV	AVDD = VDDIO, AVSS = VSS
D301	VICM	Input Common Mode Voltage	0.8	—	2.7	V	AVDD = 3.3V AVSS = VSS **(Note 2)**
D302a	CMRR	Common Mode Rejection Ratio	45	—	—	dB	AVDD = 3.3V AVSS = VSS
D303b	TRESP	Large Signal Response Time	—	50	80	ns	VCM = VDD/2 in 200 mV steps **(Note 2)**
D303b	TSRESP	Small Signal Response Time	—	100	160	ns	VCM = VDD/2 in 100mV **(Note 2)**
D304	ON2OV	Comparator Enabled to Output Valid	—	—	10	μs	Comparator module is configured before setting the comparator ON bit **(Note 2)**
D305	IVREF	Internal Voltage Reference	—	1.2	—	V	—
D306	VHYST	Input Hysteresis Voltage	48	120	192	mV	—
D307	TRISE	Output Rise Time	—	20	—	ns	Refer to parameter DO56.
D308	TFALL	Output Fall Time	—	20	—	ns	Refer to parameter DO56.

Note 1: These parameters are characterized but not tested.

2: The Comparator module is functional at VBORIOMIN < VDDIO < VDDIOMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

TABLE 44-18: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	—	—	10	μs	See **Note 1**
D313	DACREFH	CVREF Input Voltage Reference Range	AVSS	—	AVDD	V	CVRSRC with CVRSS = 0
			VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24		CVRCON<CVRR> = 1
			—	—	DACREFH/32		CVRCON<CVRR> = 0
D316	DACACC	Absolute Accuracy(2)	—	—	1/4	LSB	DACREFH/24, CVRCON<CVRR> = 1
			—	—	1/2	LSB	DACREFH/32, CVRCON<CVRR> = 0

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

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TABLE 44-19: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU CURRENT SOURCE							
CTMUI1	I_{OUT1}	Base Range(1)	0.33	0.55	0.81	μA	CTMUCON<1:0> = 01
CTMUI2	I_{OUT2}	10x Range(1)	3.3	5.5	8.1	μA	CTMUCON<1:0> = 10
CTMUI3	I_{OUT3}	100x Range(1)	33	55	81	μA	CTMUCON<1:0> = 11
CTMUI4	I_{OUT4}	1000x Range(1)	330	550	810	μA	CTMUCON<1:0> = 00
CTMUFV1	V_F	Temperature Diode Forward Voltage(1,2)	0.598	0.602	0.609	V	TA = +25ºC, CTMUCON<1:0> = 01
			0.656	0.662	0.667	V	TA = +25ºC, CTMUCON<1:0> = 10
			0.720	0.721	0.728	V	TA = +25ºC, CTMUCON<1:0> = 11
CTMUFV2	V_{FVR}	Temperature Diode Rate of Change(1,2)	-1.33	-1.44	-1.59	mV/ºC	CTMUCON<1:0> = 01
			-1.23	-1.32	-1.45	mV/ºC	CTMUCON<1:0> = 10
			-1.10	-1.18	-1.30	mV/ºC	CTMUCON<1:0> = 11

Note 1: Nominal value at center point of current trim range (CTMUCON<7:2> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- V_{REF+} = AV_{DD} = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a `while(1)` statement
- Device operating from the FRC with no PLL

TABLE 44-20: GLCD CONTROLLER DC SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
GD10	V_{OH}	Output High Voltage	2.4	—	—	V	I_{OH} ≥ 20 mA, V_{DDIO} = 3.3V
GD11	V_{OL}	Output Low Voltage	—	—	0.4	V	I_{OL} ≤ 20 mA, V_{DDIO} = 3.3V
GD12	V_{IH}	Input High Voltage	0.65*V_{DDIO}	—	V_{DDIO}	V	—
GD13	V_{IL}	Input Low Voltage	V_{SS}	—	0.2*V_{DDIO}	V	—

44.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC32MZ DAK/DAL/DAR/DAS device AC characteristics and timing parameters.

FIGURE 44-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

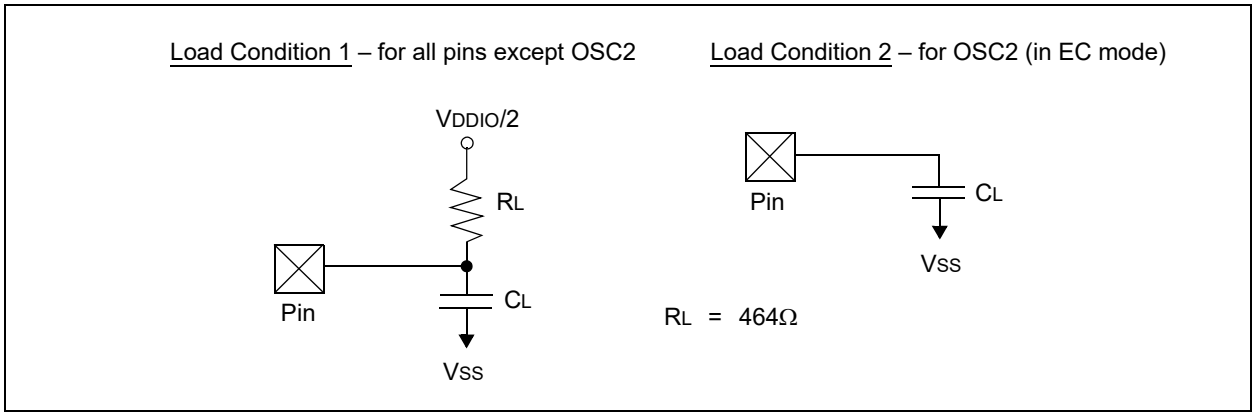

TABLE 44-21: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO56	C_L	All I/O pins	—	—	50	pF	EC mode for OSC2
DO58	C_B	SCLx, SDAx	—	—	400	pF	In I^2C mode
DO59	C_{SQI}	All SQI pins	—	—	10	pF	—

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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FIGURE 44-2: EXTERNAL CLOCK TIMING

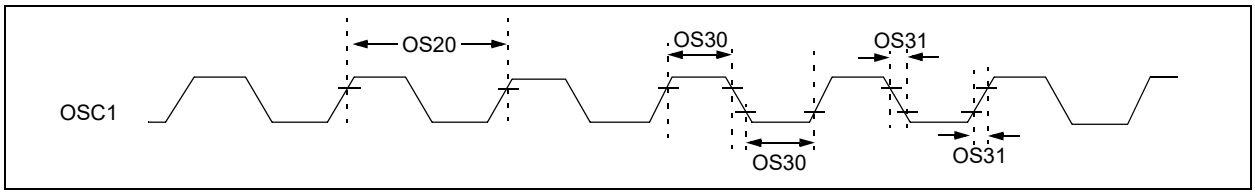

TABLE 44-22: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	64	MHz	EC **(Note 2)**
OS13		Oscillator Crystal Frequency	4	—	32	MHz	HS **(Note 2)**
OS15			32	32.768	100	kHz	SOSC **(Note 2)**
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.375 x TOSC	—	—	ns	EC **(Note 2)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	7.5	ns	EC **(Note 2)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 2)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 2)**
OS42	GM	External Oscillator Transconductance (Primary Oscillator Only)	—	400	—	µA/V	VDDIO = 3.3V, TA = +25°C **(Note 2)**

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are characterized but are not tested.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 44-23: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OS51	FSYS	System Frequency	DC	—	200	MHz	USB module disabled, and GPU disabled
			40	—	200	MHz	GPU enabled
			60	—	200	MHz	USB module enabled
OS55a	FPB	Peripheral Bus Frequency	DC	—	100	MHz	For PBCLKx, ‘x’ < 7
OS55b			DC	—	200	MHz	For PBCLK7
OS55c			60	—	100	MHz	For PBCLK5, when USB module is enabled.
OS56	FREF	Reference Clock Frequency	—	—	50	MHz	For REFCLKI1, REFCLKI3, REFCLKI4, REFCLKO1, REFCLKO3, and REF-CLKO4 pins

TABLE 44-24: SPLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OS50	FIN	PLL Input Frequency Range	5	—	64	MHz	ECPLL, HSPLL, FRCPLL modes
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	100	µs	—
OS53	DCLK	CLKO Stability(2) (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period
OS54	FVCO	PLL VCO Frequency Range	350	—	700	MHz	—
OS54a	FPLL	PLL Output Frequency Range	10	—	200	MHz	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{CommunicationClock}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

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TABLE 44-25: MPLL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MP10	MF_{IN}	MPLL Input Frequency	8	—	64	MHz	—
MP11	MFV_{CO}	MPLL Vco Frequency Range	400	—	1600	MHz	—
MP12	MF_{MPLL}	MPLL Output Frequency	8	—	200	MHz	—
MP13	M_{LOCK}	MPLL Start-up Time (Lock Time)	—	—	1500 x 1/MF_{IN}	µs	—
MP14	M_{PJ}	MPLL Period Jitter	—		0.015	%	—
MP15	M_{CJ}	MPLL Cycle Jitter	—	—	0.02	%	—
MP16	M_{LTJ}	MPLL Long-term Jitter	—	—	0.5	%	—

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 44-26: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	-5	—	+5	%	

Note 1: Frequency calibrated at +25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

TABLE 44-27: INTERNAL LPRC ACCURACY

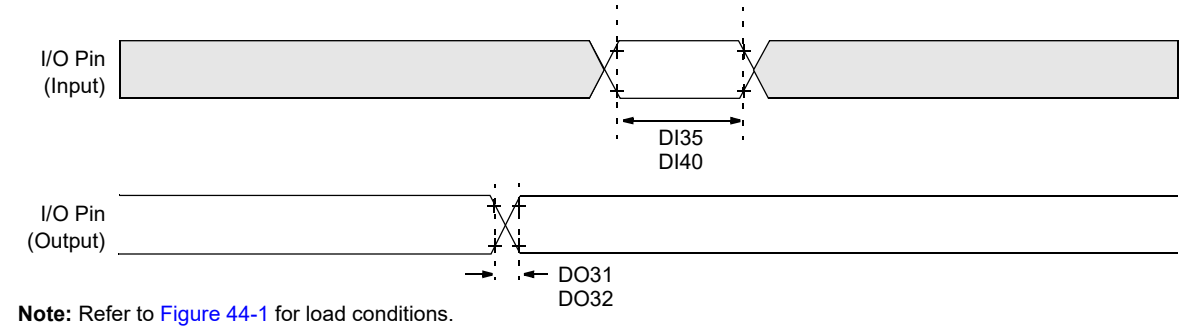
AC CHARACTERISTICS		Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
LPRC @ 32.768 kHz(1)						
F21	LPRC	-8	—	+8	%	

Note 1: Change of LPRC frequency as V_{DDIO} changes.

TABLE 44-28: INTERNAL BACKUP FRC (BFRC) ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal BFRC Accuracy @ 8 MHz(1)						
F22	BFRC	-30	—	+30	%	—

FIGURE 44-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-29: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	**Port Output Rise Time** I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 12x Source Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	3.5	ns	CLOAD = 50 pF
			—	—	2	ns	CLOAD = 20 pF

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

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TABLE 44-29: I/O TIMING REQUIREMENTS (CONTINUED)

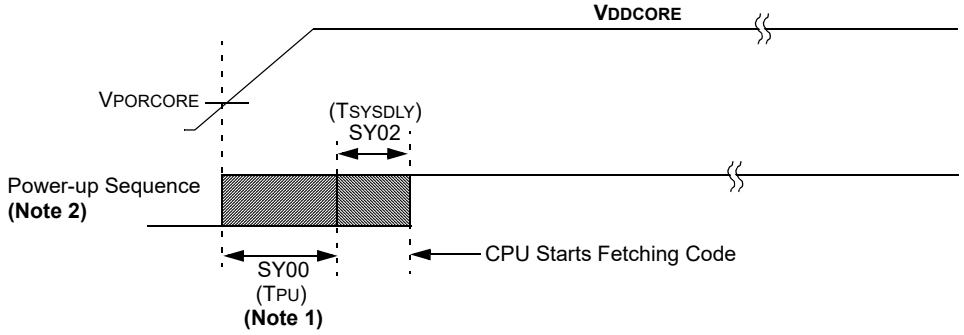
AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO32	TIOF	**Port Output Fall Time** I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Fall Time I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Fall Time I/O Pins: 12x Source Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	3.5	ns	CLOAD = 50 pF
			—	—	2	ns	CLOAD = 20 pF
DI35	TINP	INTx Pin High or Low Time	5	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	5	—	—	ns	—

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

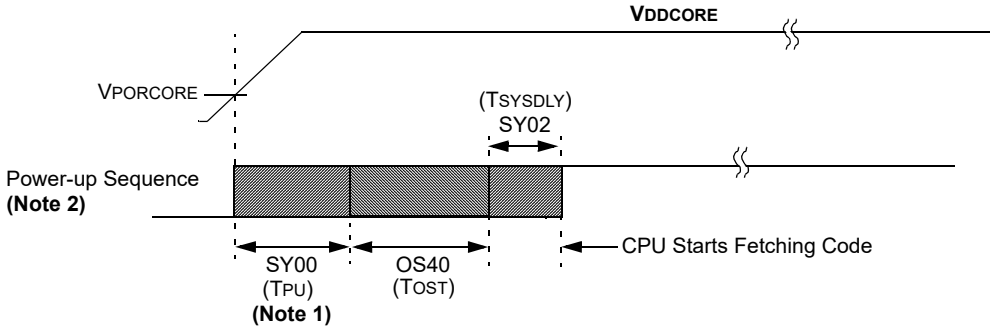
2: This parameter is characterized, but not tested in manufacturing.

FIGURE 44-4: POWER-ON RESET TIMING CHARACTERISTICS

Internal Voltage Regulator Enabled
Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)



Internal Voltage Regulator Enabled
Clock Sources = (HS, HSPLL, and SOSC)



Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR (VDDIO < VDDIOMIN).

2: Includes interval voltage regulator stabilization delay.

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FIGURE 44-5: EXTERNAL RESET TIMING CHARACTERISTICS

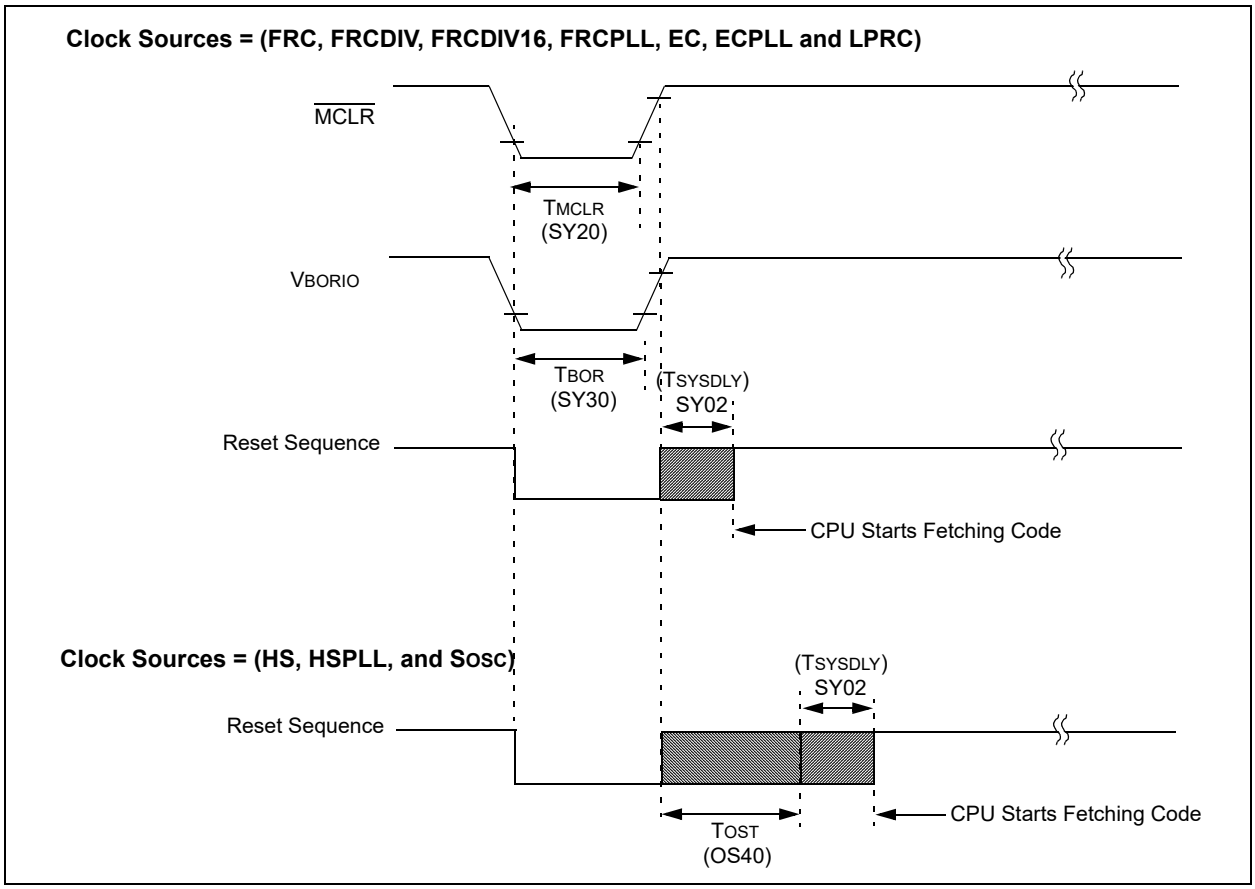
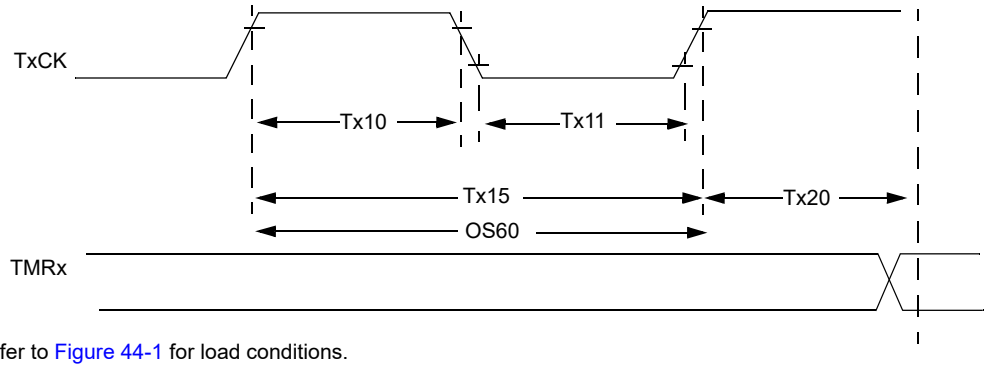


TABLE 44-30: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	—
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	—	1 μs + 8 SYSCLK cycles	—	—	—
SY20	TMCLR	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	μs	—
SY30	TBOR	BOR Pulse Width (low)	—	1	—	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.
2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Characterized by design but not tested.

FIGURE 44-6: TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-31: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(2)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 20 ns or 2 TPBCLK3)/N] + 30 ns	—	—	ns	VDDIO > 2.7V (**Note 3**)
				[(Greater of 20 ns or 2 TPBCLK3)/N] + 50 ns	—	—	ns	VDDIO < 2.7V (**Note 3**)
			Asynchronous, with prescaler	20	—	—	ns	VDDIO > 2.7V
				50	—	—	ns	VDDIO < 2.7V
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	50	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	—	1	TPBCLK3	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

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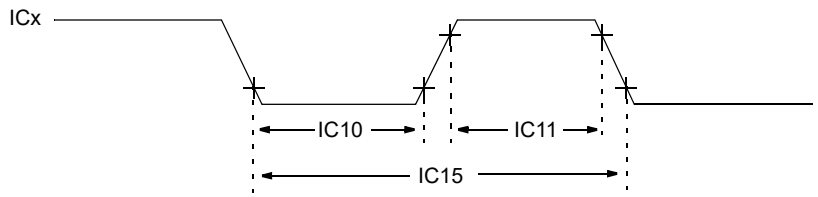
TABLE 44-32: TIMER2-TIMER9 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**		**Min.**	**Max.**	**Units**	**Conditions**	
TB10	T_{TXH}	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 T_{PBCLK3}) /N] + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	T_{TXL}	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 T_{PBCLK3}) /N] + 25 ns	—	ns	Must also meet parameter TB15	
TB15	T_{TXP}	TxCK Input Period	Synchronous, with prescaler	[(Greater of [(25 ns or 2 T_{PBCLK3})/N] + 30 ns	—	ns	V_{DDIO} > 2.7V	
				[(Greater of [(25 ns or 2 T_{PBCLK3})/N] + 50 ns	—	ns	V_{DDIO} < 2.7V	
TB20	$T_{CKEXTMRL}$	Delay from External TxCK Clock Edge to Timer Increment		—	1	T_{PBCLK3}	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 44-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



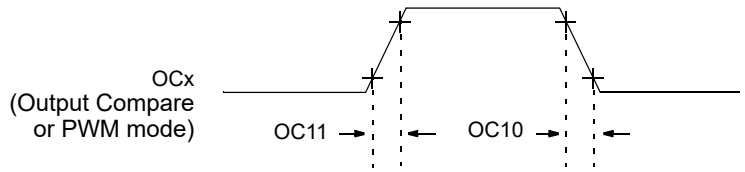
Note: Refer to Figure 44-1 for load conditions.

TABLE 44-33: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	T_{CCL}	ICx Input Low Time	[(12.5 ns or 1 T_{PBCLK3}) /N] + 25 ns	—	ns	Must also meet parameter IC15.	N = prescale value (1, 4, 16)
IC11	T_{CCH}	ICx Input High Time	[(12.5 ns or 1 T_{PBCLK3}) /N] + 25 ns	—	ns	Must also meet parameter IC15.	
IC15	T_{CCP}	ICx Input Period	[(25 ns or 2 T_{PBCLK3}) /N] + 50 ns	—	ns	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 44-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

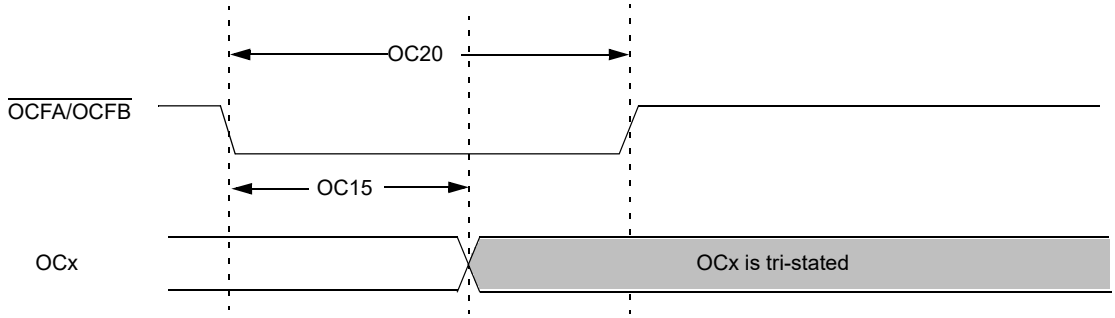
TABLE 44-34: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
OC10	TCCF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TCCR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 44-9: OCx/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-35: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param No.	**Symbol**	**Characteristics(1)**	**Min,**	**Typ.(2)**	**Max,**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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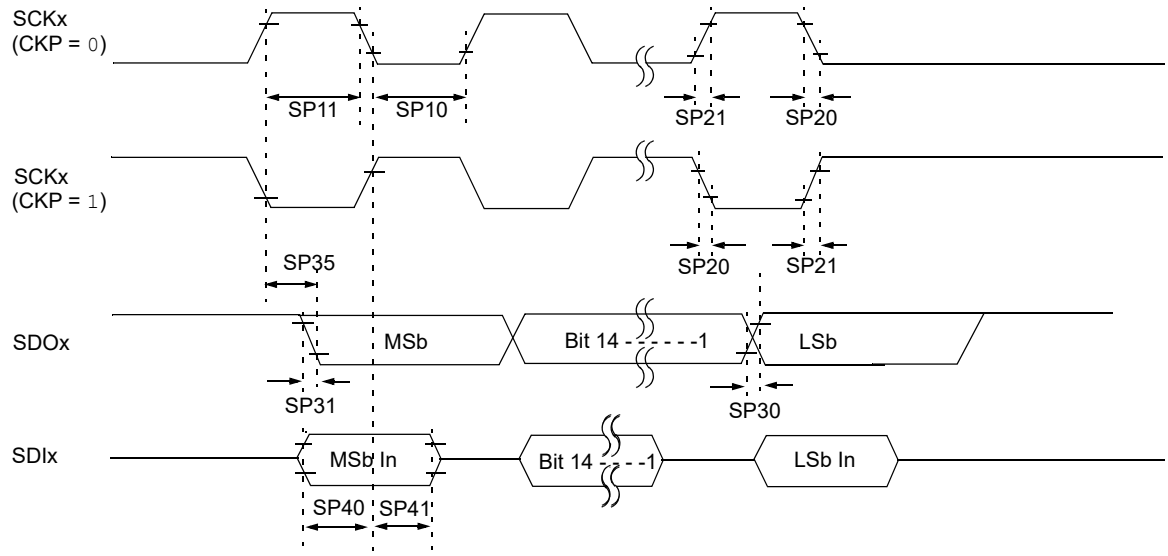
FIGURE 44-10: SPIx MODULE HOST MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-36: SPIx HOST MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time **(Note 3)**	Tsck/2	—	—	ns	**Note 5**
SP11	TscH	SCKx Output High Time **(Note 3)**	Tsck/2	—	—	ns	**Note 5**
SP15	TscK	SPI Clock Speed **(Note 5)**	— — — — —	— — — — —	25 50 25 50 25	MHz MHz MHz MHz MHz	SPI1, SPI3, SPI4, SPI6 SPI2 on RPG7, RPG8 SPI2 on other I/O SPI5 on RPC1, RPC4 SPI5 on other I/O
SP20	TscF	SCKx Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	V_{DDIO} > 2.7V
			—	—	10	ns	V_{DDIO} < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns. Therefore, the clock generated in Host mode must not violate this specification.

4: Assumes 30 pF load on all SPIx pins.

5: To achieve maximum data rate, V_{DDIO} must be greater than or equal to 3.0V and the SMP bit (SPIxCON<9>) must be set to ‘1’.

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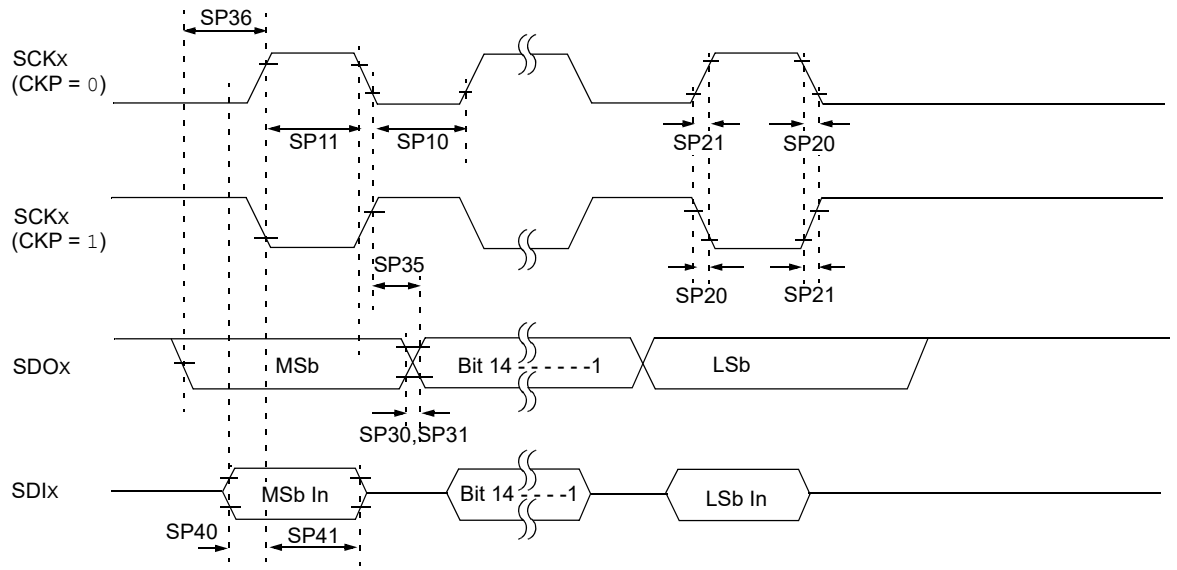
FIGURE 44-11: SPIx MODULE HOST MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-37: SPIx MODULE HOST MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time **(Note 3)**	Tsck/2	—	—	ns	**Note 5**
SP11	TscH	SCKx Output High Time **(Note 3)**	Tsck/2	—	—	ns	**Note 5**
SP15	TscK	SPI Clock Speed **(Note 5)**	— — — — —	— — — — —	25 50 25 50 25	MHz MHz MHz MHz MHz	SPI1, SPI3, SPI4, SPI6 SPI2 on RPG7, RPG8 SPI2 on other I/O SPI5 on RPC1, RPC4 SPI5 on other I/O
SP20	TscF	SCKx Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	V_{DDIO} > 2.7V
			—		10		V_{DDIO} < 2.7V
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	7	—	—	ns	—
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	7	—	—	ns	V_{DDIO} > 2.7V
			10				V_{DDIO} < 2.7V
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	V_{DDIO} > 2.7V
			10	—	—	ns	V_{DDIO} < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns. Therefore, the clock generated in host mode must not violate this specification.

4: Assumes 30 pF load on all SPIx pins.

5: To achieve maximum data rate, V_{DDIO} must be greater than or equal to 3.0V and the SMP bit (SPIx-CON<9>) must be set to '1'.

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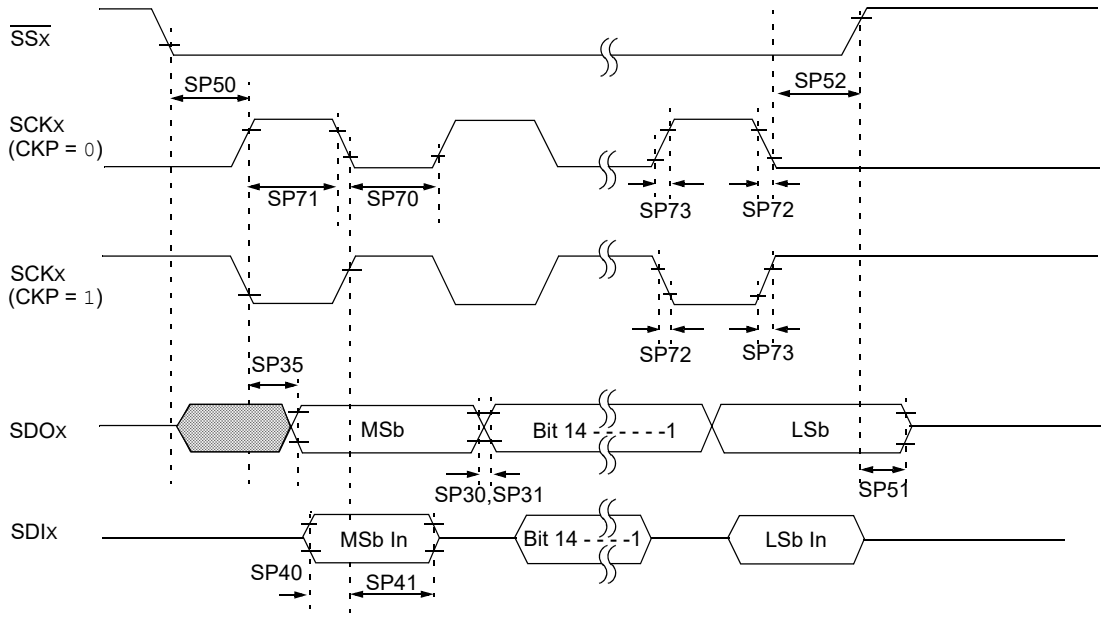
FIGURE 44-12: SPIx MODULE CLIENT MODE (CKE = 0) TIMING CHARACTERISTICS



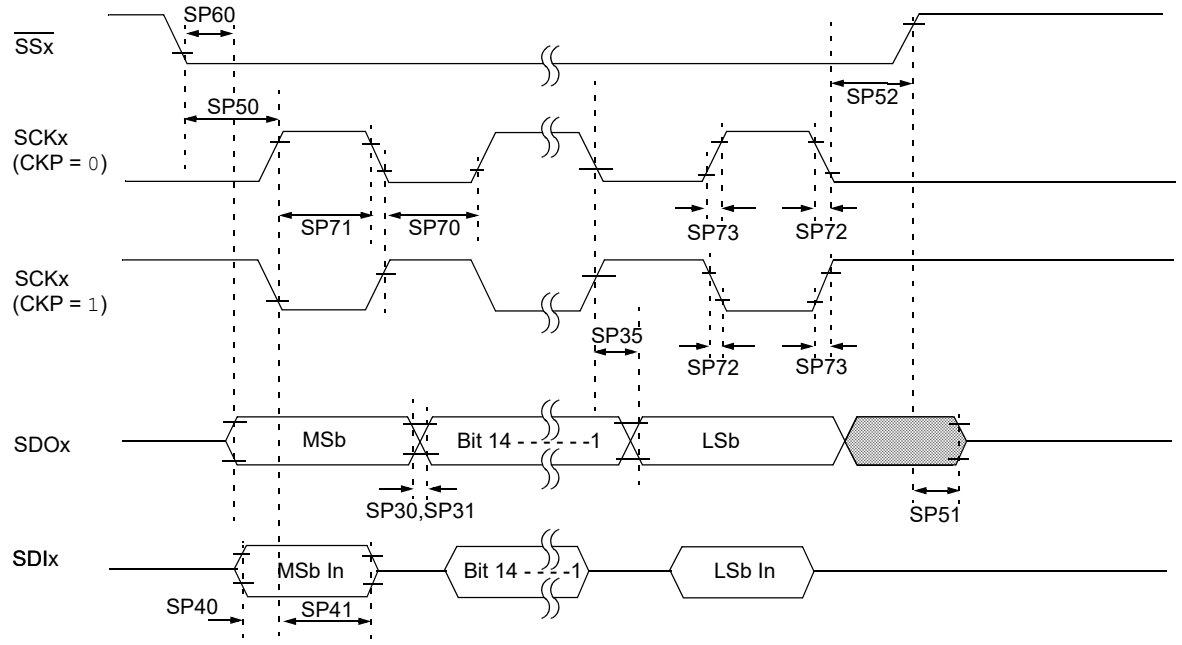
Note: Refer to Figure 44-1 for load conditions.

TABLE 44-38: SPIx MODULE CLIENT MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	ns	**Note 5**
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	ns	**Note 5**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	V_{DDIO} > 2.7V
			—	—	10	ns	V_{DDIO} < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 3)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
3: The minimum clock period for SCKx is 20 ns.
4: Assumes 10 pF load on all SPIx pins.
5: Tsck is 40 ns for SPI1, SPI3, SPI4, and SPI6 and it is 20 ns for SPI2 and SPI5.

FIGURE 44-13: SPIx MODULE CLIENT MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-39: SPIx MODULE CLIENT MODE (CKE = 1) TIMING REQUIREMENTS ('x' = 1, 3, 4, 6)

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	ns	**Note 5**
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	ns	**Note 5**
SP72	TscF	SCKx Input Fall Time	—	—	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	—	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	10	ns	V_{DDIO} > 2.7V
			—	—	15	ns	V_{DDIO} < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 10 pF load on all SPIx pins.

5: Tsck is 40 ns for SPI1, SPI3, SPI4, and SPI6 and it is 20 ns for SPI2 and SPI5.

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TABLE 44-39: SPIx MODULE CLIENT MODE (CKE = 1) TIMING REQUIREMENTS ('x' = 1, 3, 4, 6) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	—
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 10 pF load on all SPIx pins.

5: TSCK is 40 ns for SPI1, SPI3, SPI4, and SPI6 and it is 20 ns for SPI2 and SPI5.

FIGURE 44-14: SQI SERIAL INPUT TIMING CHARACTERISTICS

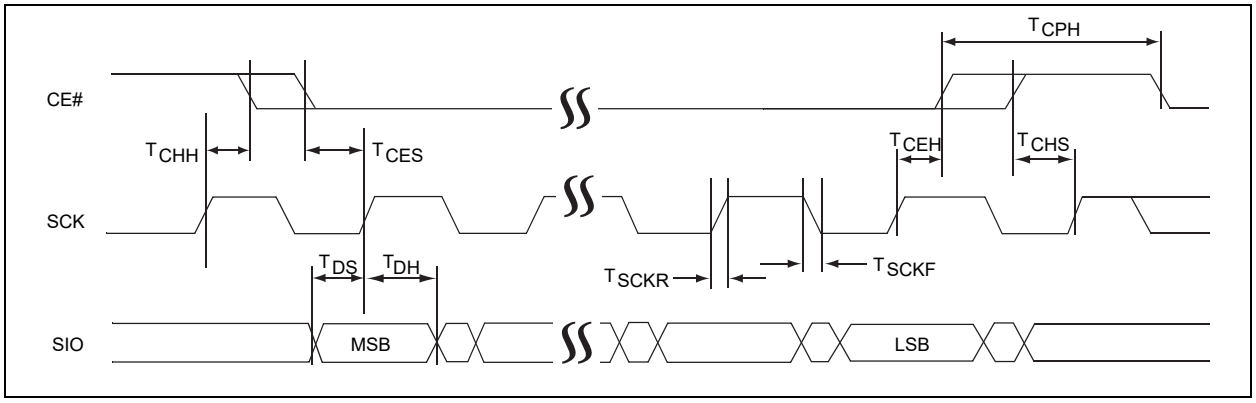

FIGURE 44-15: SQI SERIAL OUTPUT TIMING CHARACTERISTICS

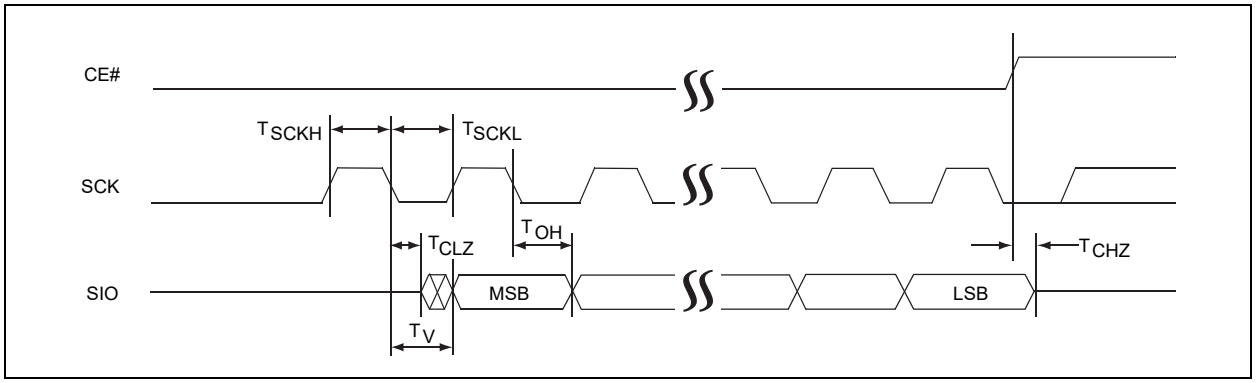

TABLE 44-40: SQI TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SQ10	FCLK	Serial Clock Frequency (1/TSQI)	—	—	73	MHz	DMA Read mode, SDR mode
			—	—	70	MHz	DMA Read mode, DDR mode
			—	—	76	MHz	PIO Write mode, SDR mode
SQ11	TSCKH	Serial Clock High Time	6	—	—	ns	—
SQ12	TSCKL	Serial Clock Low Time	6	—	—	ns	—
SQ13	TSCKR	Serial Clock Rise Time	0.25	—	—	ns	—
SQ14	TSCKF	Serial Clock Fall Time	0.25	—	—	ns	—
SQ15	TCSS (TCES)	$\overline{CS}$ Active Setup Time	5	—	—	ns	—
SQ16	TCSH (TCEH)	$\overline{CS}$ Active Hold Time	5	—	—	ns	—
SQ17	TCHS	$\overline{CS}$ Not Active Setup Time	3	—	—	ns	—
SQ18	TCHH	$\overline{CS}$ Not Active Hold Time	3	—	—	ns	—
SQ19	TCPH	$\overline{CS}$ High Time	6	—	—	ns	—
SQ20	TCHZ	$\overline{CS}$ High to High-Z Data Out	—	—	6	ns	—
SQ21	TCLZ	SCK Low to Low-Z Data Out	0	—	—	ns	—
SQ22	TDS	Data In Setup Time	3	—	—	ns	—
SQ23	TDH	Data In Hold Time	4	—	—	ns	—
SQ24	TOH	Data Out Hold	0	—	—	ns	—

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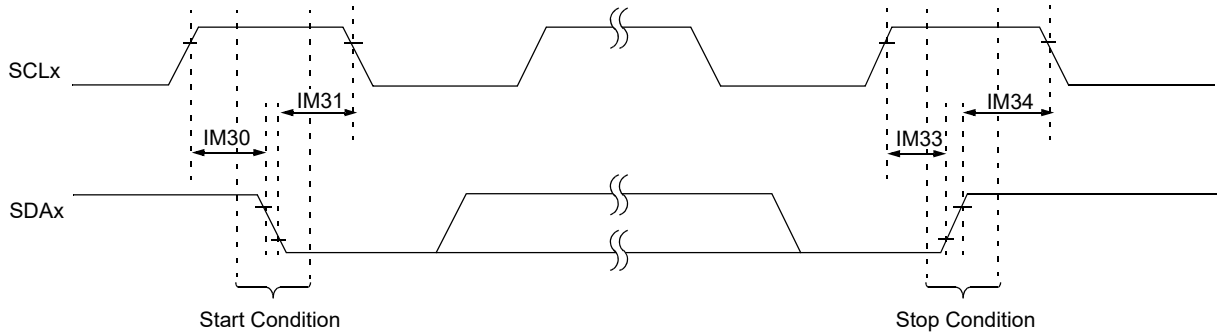
TABLE 44-40: SQI TIMING REQUIREMENTS (CONTINUED)

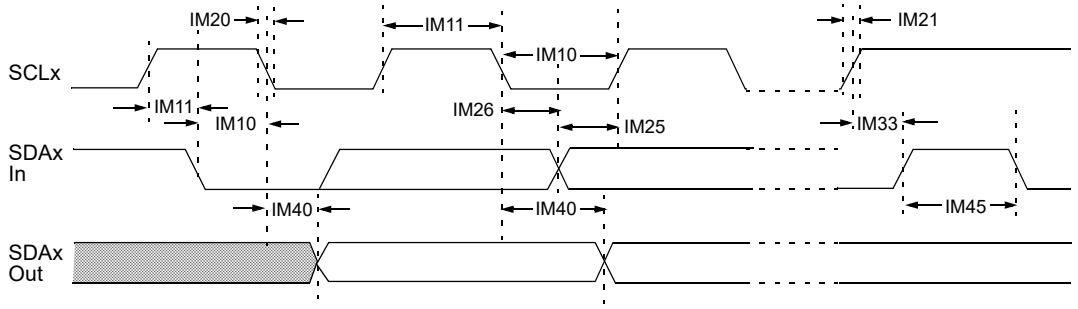
AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SQ25	TOV (TV)	Data Out Valid	—	—	6	ns	—

FIGURE 44-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (HOST MODE)



Note: Refer to Figure 44-1 for load conditions.

FIGURE 44-17: I2Cx BUS DATA TIMING CHARACTERISTICS (HOST MODE)



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-41: I2Cx BUS DATA TIMING REQUIREMENTS (HOST MODE)

AC CHARACTERISTICS				Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	100	ns	

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

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TABLE 44-41: I2Cx BUS DATA TIMING REQUIREMENTS (HOST MODE) (CONTINUED)

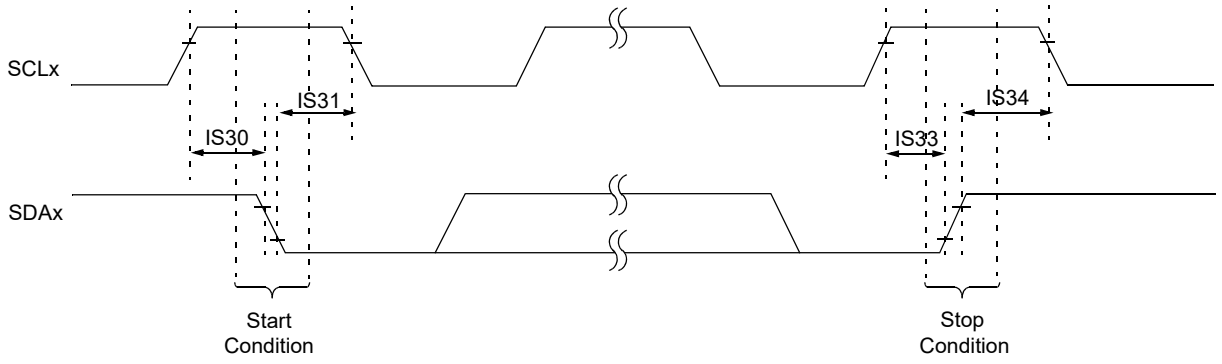
AC CHARACTERISTICS				Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 2)**	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 2)**	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode **(Note 2)**	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	µs	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPBCLK2 * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 2)**	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

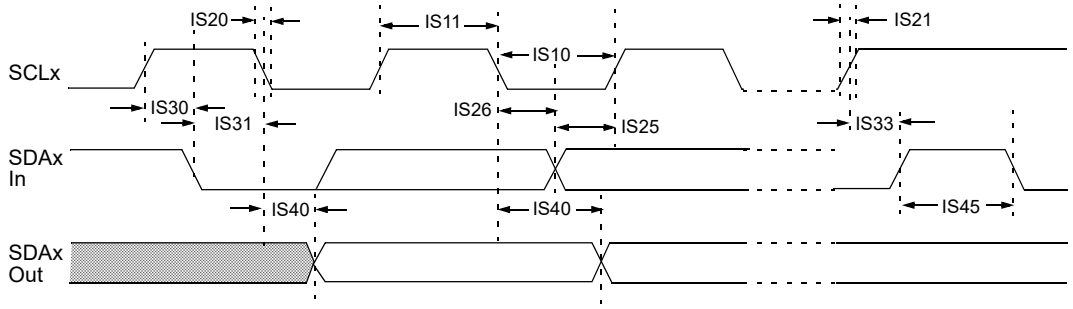
3: The typical value for this parameter is 104 ns.

FIGURE 44-18: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (CLIENT MODE)



Note: Refer to Figure 44-1 for load conditions.

FIGURE 44-19: I2Cx BUS DATA TIMING CHARACTERISTICS (CLIENT MODE)



Note: Refer to Figure 44-1 for load conditions.

TABLE 44-42: I2Cx BUS DATA TIMING REQUIREMENTS (CLIENT MODE)

AC CHARACTERISTICS				Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode **(Note 1)**	0.5	—	μs	—
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	μs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode **(Note 1)**	0.5	—	μs	—

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

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TABLE 44-42: I2Cx BUS DATA TIMING REQUIREMENTS (CLIENT MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 1)**	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode **(Note 1)**	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode **(Note 1)**	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode **(Note 1)**	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	600	—	ns	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	—
			400 kHz mode	600	—	ns	
			1 MHz mode **(Note 1)**	250	—	ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	—
			400 kHz mode	0	1000	ns	
			1 MHz mode **(Note 1)**	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode **(Note 1)**	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	—	pF	See parameter DO58

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

FIGURE 44-20: CANx MODULE I/O TIMING CHARACTERISTICS

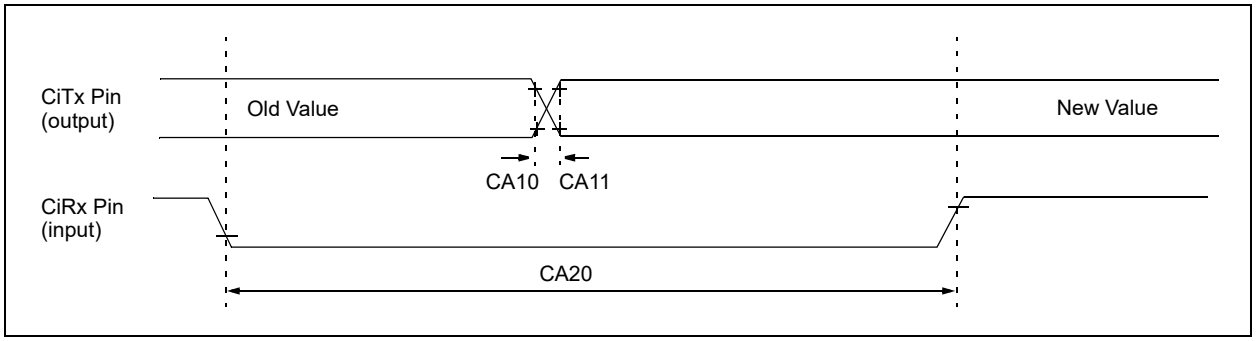

TABLE 44-43: CANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter DO31
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	700	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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TABLE 44-44: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AV_{DD}	Module V_{DDIO} Supply	Greater of V_{DDIO} – 0.3 or 2.3	—	Lesser of V_{DDIO} + 0.3 or 3.6	V	—
AD02	AV_{SS}	Module V_{SS} Supply	V_{SS}	—	V_{SS} + 0.3	V	—
Reference Inputs							
AD05	V_{REFH}	Reference Voltage High	V_{REFL} + 1.8	—	AV_{DD}	V	**(Note 1)**
AD06	V_{REFL}	Reference Voltage Low	AV_{SS}	—	V_{REFH} – 1.8	V	**(Note 1)**
AD07	V_{REF}	Absolute Reference Voltage (V_{REFH} – V_{REFL})	1.8	—	AV_{DD}	V	**(Note 2)**
AD08	I_{REF}	Current Drain	—	102	—	µA	ADC is operating or is in Stand-by.
Analog Input							
AD12	V_{INH}-V_{INL}	Full-Scale Input Span	V_{REFL}	—	V_{REFH}	V	—
AD13	V_{INL}	Absolute V_{INL} Input Voltage	AV_{SS}	—	V_{REFL}	V	—
AD14	V_{INH}	Absolute V_{INH} Input Voltage	AV_{SS}	—	V_{REFH}	V	—
ADC Accuracy – Measurements with External V_{REF+}/V_{REF-}							
AD20c	Nr	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 Resolution Ranges
AD21c	INL	Integral Nonlinearity	—	±3	—	LSb	V_{INL} = AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3.3V
AD22c	DNL	Differential Nonlinearity	—	±1	—	LSb	V_{INL} = AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3.3V
AD23c	G_{ERR}	Gain Error	—	±8	—	LSb	V_{INL} = AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3.3V
AD24c	E_{OFF}	Offset Error	—	±2	—	LSb	V_{INL} = AV_{SS} = 0V, AV_{DD} = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed **(Note 2)**
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	—	65	—	dB	Single-ended **(Notes 2,3)**
AD34b	ENOB	Effective Number of bits	—	10.5	—	bits	**(Notes 2,3)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

4: The ADC module is functional at $V_{BORIOMIN}$ < V_{DDIO} < $V_{DDIOMIN}$, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

TABLE 44-45: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS(2)			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	20	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC4 (Class 1 Inputs)	— — — —	— — — —	3.125 3.57 4.16 5	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	— — — —	— — — —	2.94 3.33 3.84 4.55	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC4 (Class 1 Inputs)	3 4 5 13	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	4 5 6 14	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	See Table 44-46	—	—	TAD	CVDEN (ADCCON1<11>) = 1
AD62	TCONV	Conversion Time (after sample time is complete)	— — — —	— — — —	13 11 9 7	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
AD65	TWAKE	Wake-up time from Low-Power Mode	— —	500 20	— —	TAD μs	Lesser of 500 TAD or 20 μs.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at $V_{BORIOMIN}$ < V_{DDIO} < $V_{DDIOMIN}$, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

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TABLE 44-46: ADC SAMPLE TIMES WITH CVD ENABLED

AC CHARACTERISTICS(2)			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
AD60a	TSAMP	Sample Time for ADC7 (Class 2 and Class 3 Inputs) with the CVDEN bit (ADCCON1<11>) = 1	8	—	—	TAD	Source Impedance ≤ 200Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001
			9				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			11				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			12				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			14				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			17				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			10	—	—	TAD	Source Impedance ≤ 500Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001
			12				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			14				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			18				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			19				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			21				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			13	—	—	TAD	Source Impedance ≤ 1 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			18				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			21				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			23				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			26				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			28				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			41	—	—	TAD	Source Impedance ≤ 5 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001
			48				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			56				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			63				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			70				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			78				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			85				CVDCPL<2:0> (ADCCON2<28:26>) = 111

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at $V_{BORIOMIN}$ < V_{DDIO} < $V_{DDIOMIN}$, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

TABLE 44-47: TEMPERATURE SENSOR SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TS10	VTS	Rate of Change	—	5	—	mV/ºC	—
TS11	TR	Resolution	-2	—	+2	ºC	—
TS12	IVTEMP	Voltage Range	0.5	—	1.5	V	—
TS13	TMIN	Minimum Temperature	—	-40	—	ºC	IVTEMP = 0.5V
TS14	TMAX	Maximum Temperature	—	160	—	ºC	IVTEMP = 1.5V

Note 1: The temperature sensor is functional at VBORIOMIN < VDDIO < VDDIOMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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FIGURE 44-21: PSP TIMING

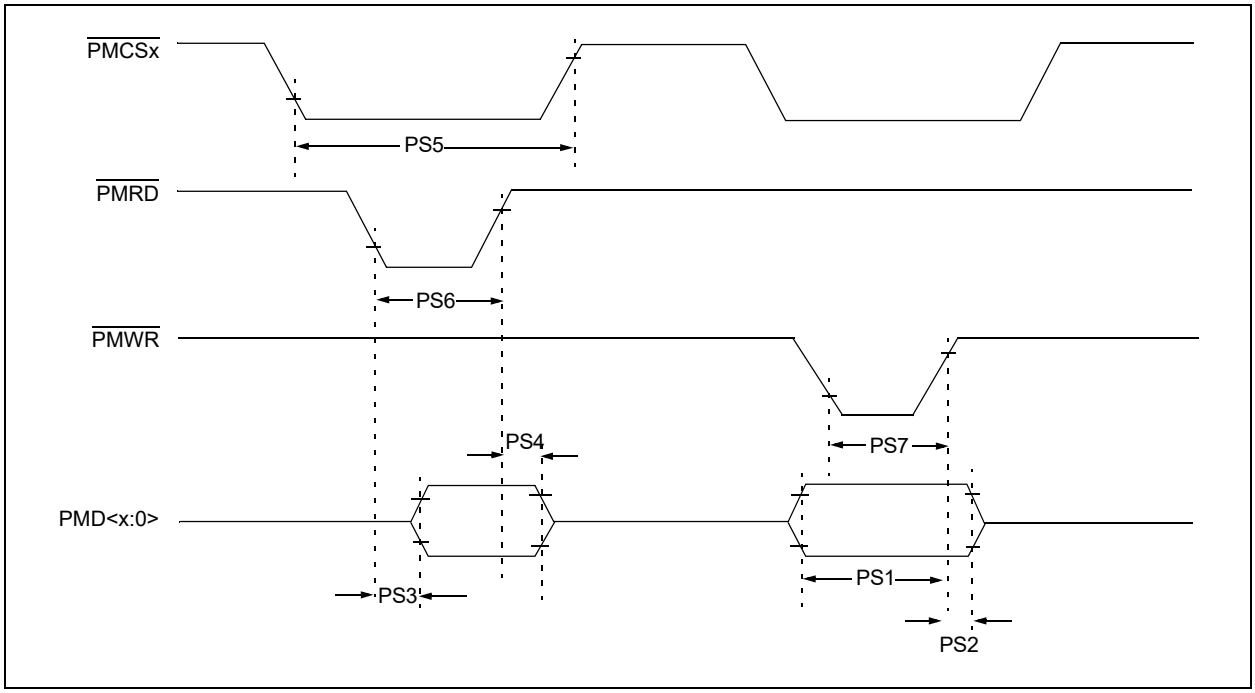

TABLE 44-48: PSP REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Para m.No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{PMWR}$ or $\overline{PMCSx}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtI	$\overline{PMWR}$ or $\overline{PMCSx}$ Inactive to Data-in Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	$\overline{PMRD}$ and $\overline{PMCSx}$ Active to Data-out Valid	—	—	60	ns	—
PS4	TrdH2dtI	$\overline{PMRD}$ Active or $\overline{PMCSx}$ Inactive to Data-out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{PMCSx}$ Active Time	TPBCLK2 + 40	—	—	ns	—
PS6	TWR	$\overline{PMWR}$ Active Time	TPBCLK2 + 25	—	—	ns	—
PS7	TRD	$\overline{PMRD}$ Active Time	TPBCLK2 + 25	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 44-22: PMP READ TIMING DIAGRAM

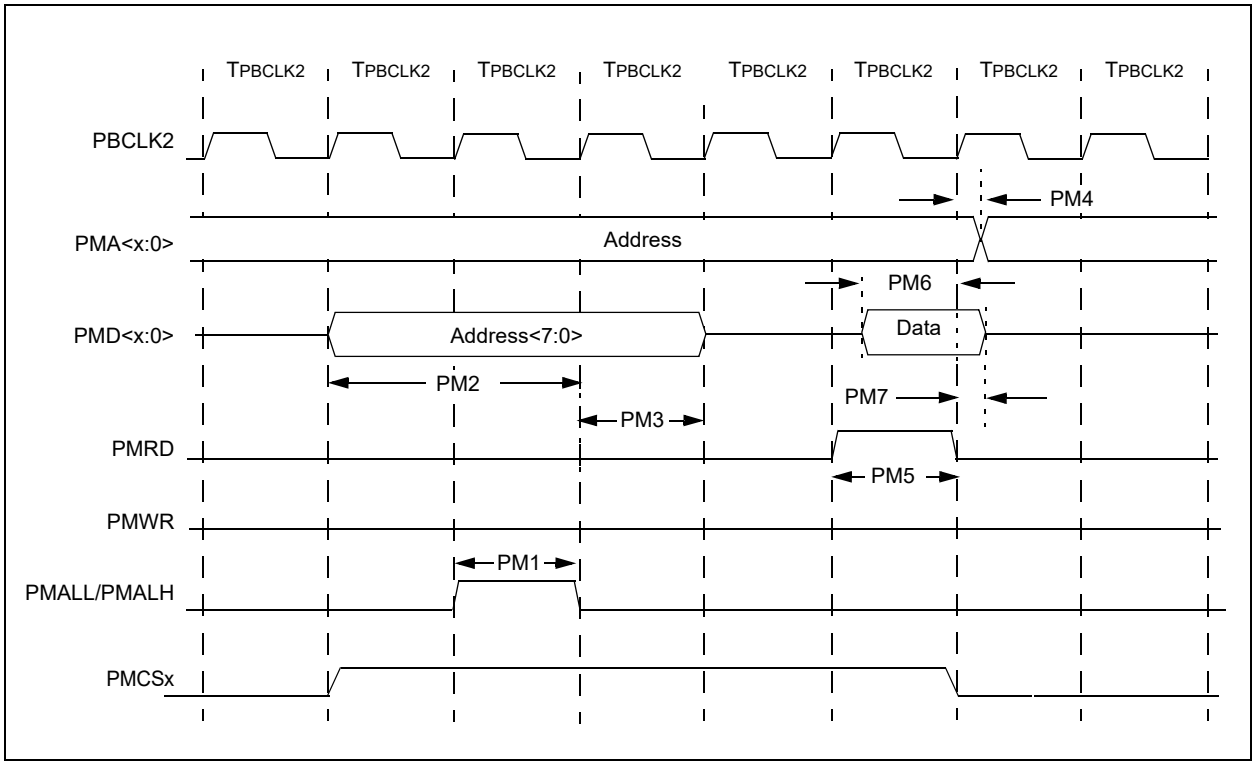

TABLE 44-49: PMP READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPBCLK2	—	—	—
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)	—	2 TPBCLK2	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPBCLK2	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPBCLK2	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	5	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

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FIGURE 44-23: PMP WRITE TIMING DIAGRAM

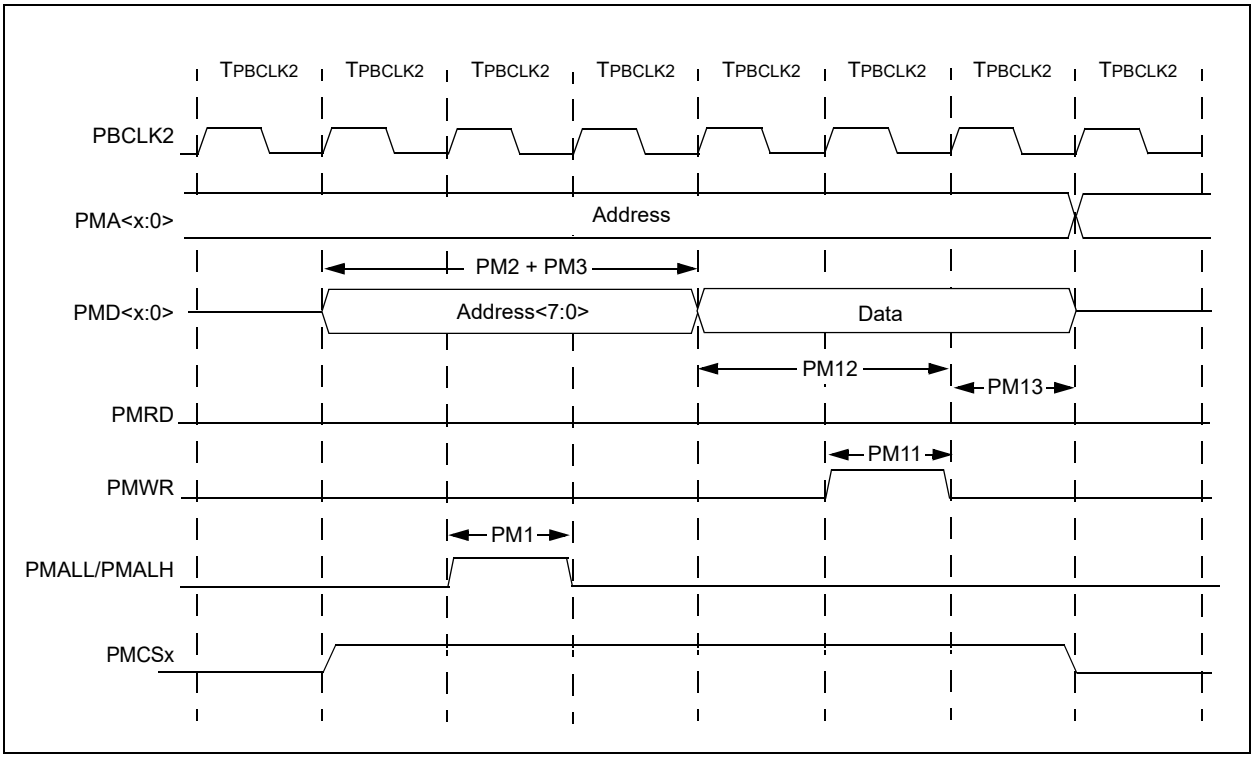

TABLE 44-50: PMP WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM11	TWR	PMWR Pulse Width	—	1 TPBCLK2	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPBCLK2	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPBCLK2	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 44-51: USB OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
USB313	V_{USB3V3}	USB Voltage	3.0	—	3.6	V	Voltage on V_{USB3V3} must be in this range for proper USB operation
Low-Speed and Full-Speed Modes							
USB315	V_{ILUSB}	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	V_{IHUSB}	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	V_{DIFS}	Differential Input Sensitivity	0.2	—	—	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB321	V_{OL}	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to V_{USB3V3}
USB322	V_{OH}	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground
Hi-Speed Mode							
USB323	V_{HSDI}	Differential input signal level	150	—	—	mV	—
USB324	V_{HSSQ}	SQ detection threshold	100	—	150	mV	—
USB325	V_{HSCM}	Common mode voltage range	-50	—	500	mV	—
USB326	V_{HSOH}	Data signaling high	360	—	440	mV	—
USB327	V_{HSOL}	Data signaling low	-10	—	10	mV	—
USB328	V_{CHIRPJ}	Chirp J level	700	—	1100	mV	—
USB329	V_{CHIRPK}	Chirp K level	-900	—	-500	mV	—
USB330	Z_{HSDRV}	Driver output resistance	—	45	—	Ω	—

Note 1: These parameters are characterized, but not tested in manufacturing.

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TABLE 44-52: ETHERNET MODULE SPECIFICATIONS

AC CHARACTERISTICS		Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MIIM Timing Requirements						
ET1	MDC Duty Cycle	40	—	60	%	—
ET2	MDC Period	400	—	—	ns	—
ET3	MDIO Output Setup and Hold	10	—	10	ns	See Figure 44-24
ET4	MDIO Input Setup and Hold	0	—	300	ns	See Figure 44-25
MII Timing Requirements						
ET5	TX Clock Frequency	—	25	—	MHz	—
ET6	TX Clock Duty Cycle	35	—	65	%	—
ET7	ETXDx, ETEN, ETXERR Output Delay	0	—	25	ns	See Figure 44-26
ET8	RX Clock Frequency	—	25	—	MHz	—
ET9	RX Clock Duty Cycle	35	—	65	%	—
ET10	ERXDx, ERXDV, ERXERR Setup and Hold	10	—	30	ns	See Figure 44-27
RMII Timing Requirements						
ET11	Reference Clock Frequency	—	50	—	MHz	—
ET12	Reference Clock Duty Cycle	35	—	65	%	—
ET13	ETXDx, ETEN, Output Delay	2	—	16	ns	—
ET14	ERXDx, ERXDV, ERXERR Setup and Hold	2	—	16	ns	—

FIGURE 44-24: MDIO SOURCED BY THE PIC32 DEVICE

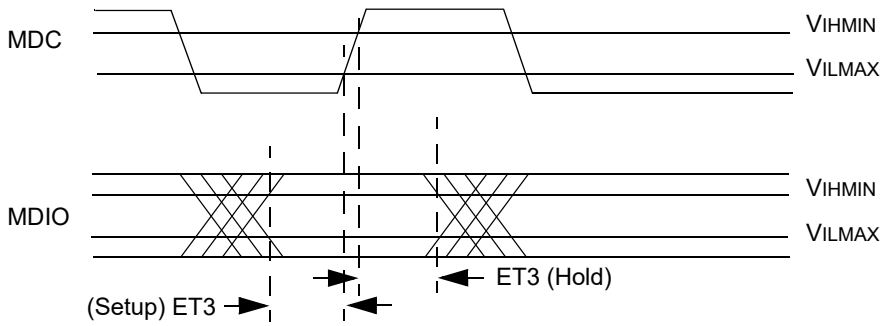

FIGURE 44-25: MDIO SOURCED BY THE PHY

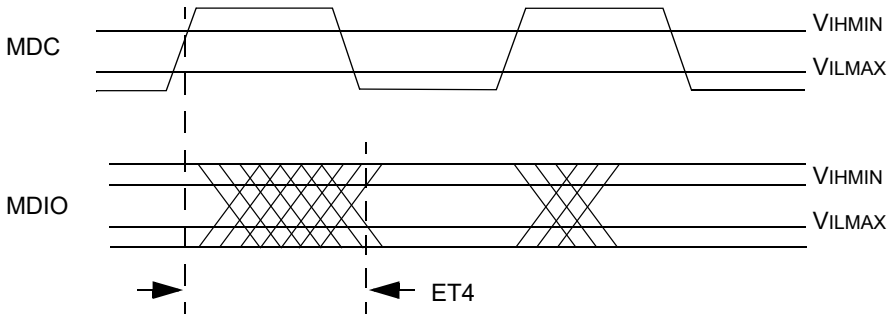

FIGURE 44-26: TRANSMIT SIGNAL TIMING RELATIONSHIPS AT THE MII

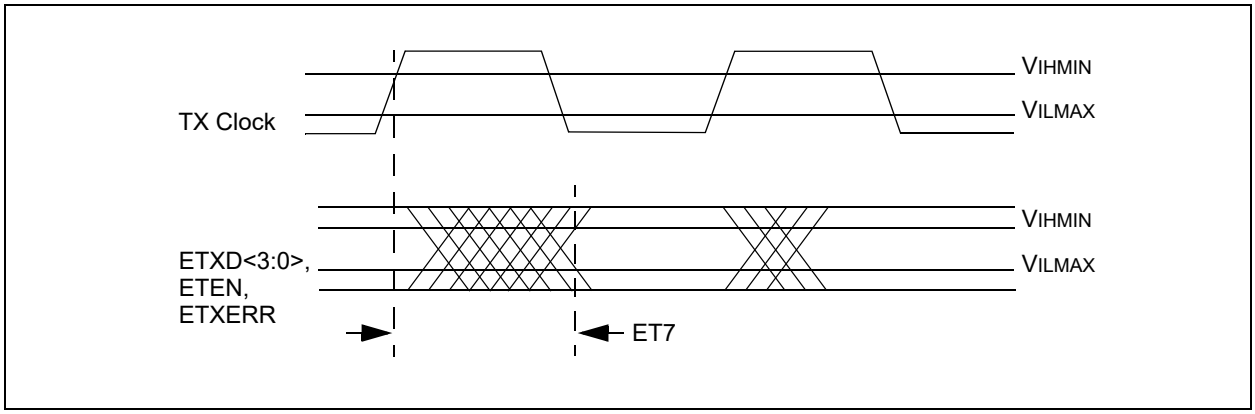

FIGURE 44-27: RECEIVE SIGNAL TIMING RELATIONSHIPS AT THE MII

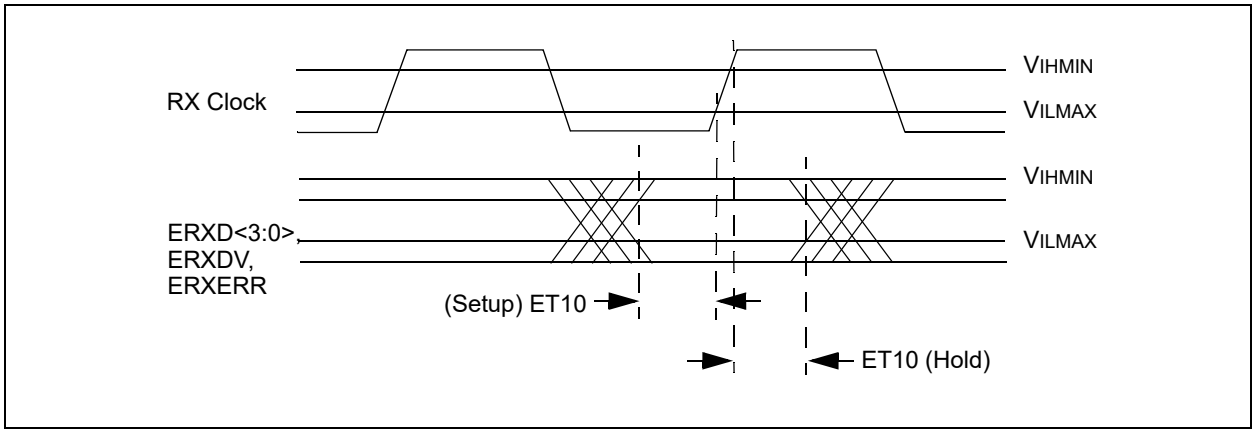

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FIGURE 44-28: EBI PAGE READ TIMING

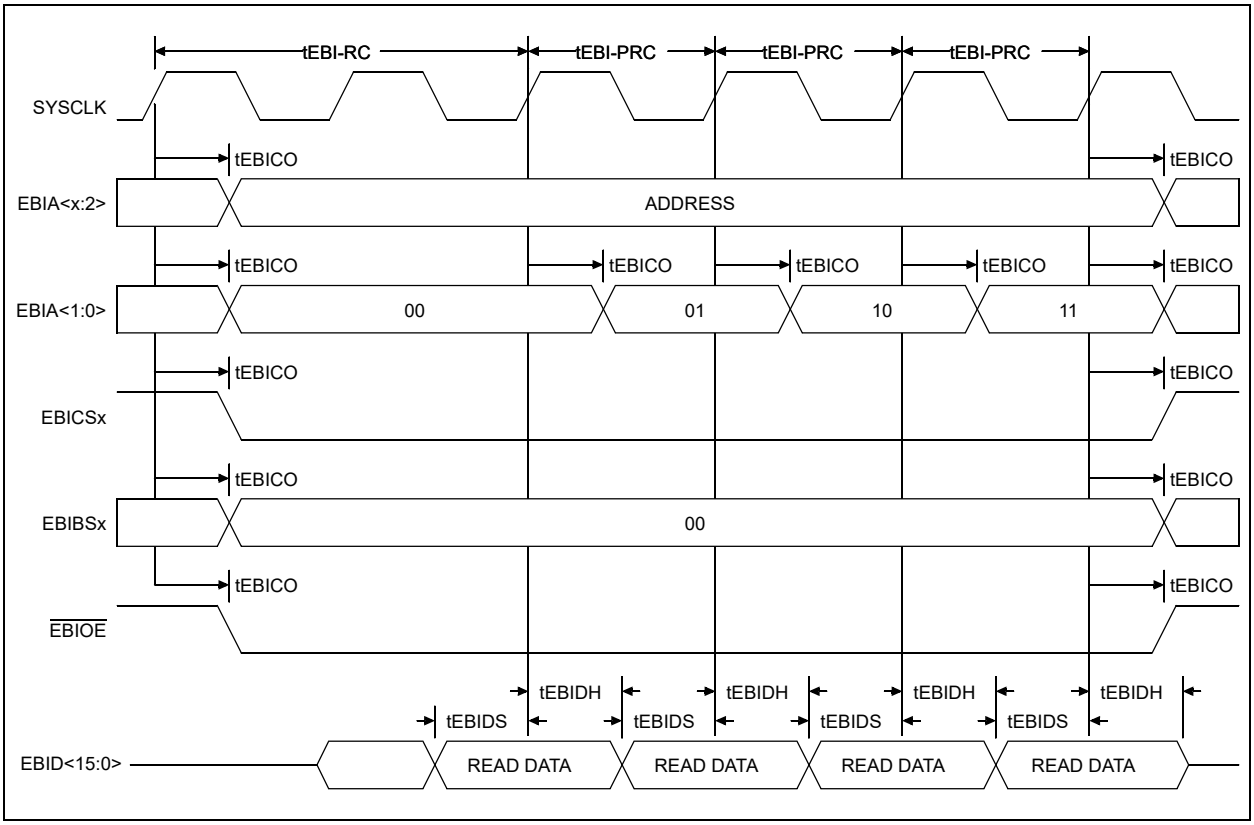

FIGURE 44-29: EBI WRITE TIMING

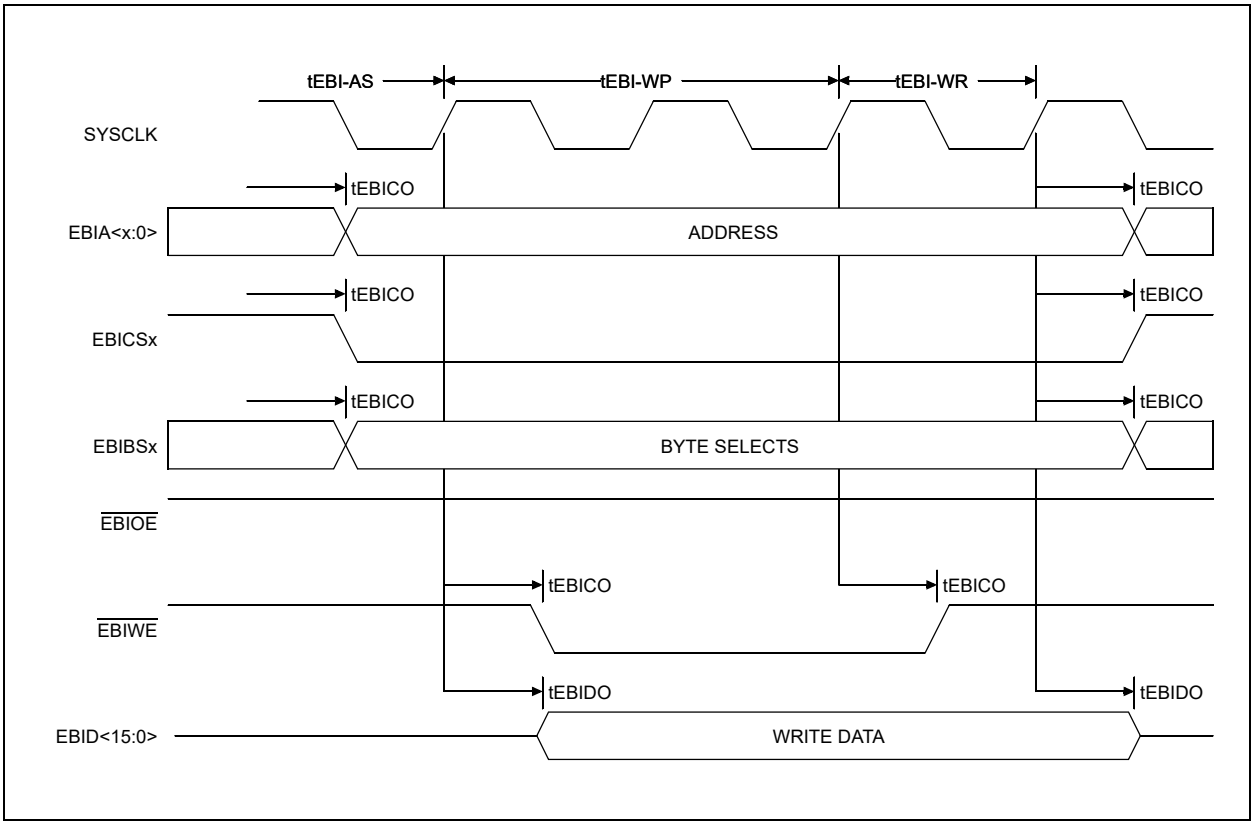

TABLE 44-53: EBI TIMING REQUIREMENTS (1)

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
EB10	TEBICLK	Internal EBI Clock Period (SYSCLK)	5	—	—	ns	—
EB11	TEBIRC	EBI Read Cycle Time (TRC<5:0>)	30	—	—	ns	—
EB12	TEBIPRC	EBI Page Read Cycle Time (TPRC<3:0>)	30	—	—	ns	—
EB13	TEBIAS	EBI Write Address Setup (TAS<1:0>)	15	—	—	ns	—
EB14	TEBIWP	EBI Write Pulse Width (TWP<5:0>)	25	—	—	ns	—
EB15	TEBIWR	EBI Write Recovery Time (TWR<1:0>)	15	—	—	ns	—
EB16	TEBICO	EBI Output Control Signal Delay	4	—	13	ns	See **Note 2**
EB17	TEBIDO	EBI Output Data Signal Delay	4	—	13	ns	See **Note 2**
EB18	TEBIDS	EBI Input Data Setup	10	—	—	ns	See **Note 2**
EB19	TEBIDH	EBI Input Data Hold	3	—	—	ns	See **Note 2,3**

Note 1: EBI Timings Requirements data are from simulation.
2: Maximum pin capacitance = 10 pF.
3: Hold time from EBI Address change is 0 ns.

TABLE 44-54: GLCD CONTROLLER TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
GD20	tGCLK	Pixel Clock Frequency on GLCD pin	—	—	50	MHz	—

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TABLE 44-55: DDR2 SDRAM TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DDR10	tCK	Clock Frequency	—	5	—	ns	—
DDR11	tDUTY	Duty Cycle	48	50	52	%	—
DDR12	tRCD	Active to Read/Write Command Delay Time	20	—	—	ns	—
DDR13	tRP	Precharge to Active Command Period	20	—	—	ns	—
DDR14	tRC	Active to Ref/Active Command Period	65	—	—	ns	—
DDR15	tRAS	Active to Precharge Command Period	40	70000	—	ns	**Note 1**
DDR16	tRFC	Auto Refresh to Active/Auto Refresh Command Period	75	—	—	ns	**Note 2**
DDR17	tREFI	Average Periodic Refresh Interval	—	—	7.8	µs	-40°C ≤ TJ ≤ 85°C **Note 2**
			—	—	3.9		85°C ≤ TJ ≤ 95°C
			—	—	1.95		95°C ≤ TJ ≤ 125°C
DDR18	tCKE	DDRCKE Minimum High and Low Pulse Width	3	—	—	ntCK	—
DDR19	tRRD	Active to active command period for 1 KB page size	10	—	—	ns	**Note 3**
DDR20	tFAW	Four Activate Window for 1 KB Page Size	35	—	—	ns	—
DDR21	tWR	Write Recovery Time	15	—	—	ns	—
DDR22	tWTR	Internal Write to Read Command Delay	10	—	—	ns	**Note 4**
DDR23	tRTP	Internal Read To Precharge Command Delay	10	—	—	ns	**Note 1**
DDR24	tXSRD	Exit Self Refresh to a Read Command	200	—	—	ntCK	—
DDR25	tXP	Exit Precharge Power Down to Any Command	2	—	—	ntCK	—

Note 1: This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.

2: If refresh timing is violated, data corruption may occur and the data must be rewritten with valid data before a valid READ can be executed.

3: A minimum of two clocks (2 * ntCK) is required regardless of operating frequency.

4: tWTR is at least two clocks (2 * ntCK) independent of operation frequency.

5: When DRAM is operated at 85°C < Tj ≤ 125°C the extended Self Refresh rate must be enabled by setting the bit A7 to “1” in extended mode register (2) EMR(2) before the Self Refresh mode can be entered.For detailed information about the EMR(2) register, refer to the DDR2 SDRAM Specification JESD79-2F.

TABLE 44-55: DDR2 SDRAM TIMING SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DDR26	tMRD	Mode Register Set Command Cycle Time	2	—	—	ntCK	—
DDR27	RL	Read Latency	CL	—	—	ntCK	—
DDR28	CL	CAS Latency	3	—	—	ntCK	—
DDR29	WL	Write Latency	RL – 1	—	—	ntCK	—
DDR30	BL	Burst Length	8	—	—	ntCK	—

Note 1: This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.

2: If refresh timing is violated, data corruption may occur and the data must be rewritten with valid data before a valid READ can be executed.

3: A minimum of two clocks (2 * ntCK) is required regardless of operating frequency.

4: tWTR is at least two clocks (2 * ntCK) independent of operation frequency.

5: When DRAM is operated at 85°C < Tj ≤ 125°C the extended Self Refresh rate must be enabled by setting the bit A7 to “1” in extended mode register (2) EMR(2) before the Self Refresh mode can be entered.For detailed information about the EMR(2) register, refer to the DDR2 SDRAM Specification JESD79-2F.

TABLE 44-56: SD HOST CONTROLLER DEFAULT MODE TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SD20	tSDCK	Clock Frequency	—	—	25	MHz	—
SD21	tDUTY	Duty Cycle	—	50	—	%	—
SD22	tHIGH	Clock High Time	10	—	—	ns	—
SD23	tLOW	Clock Low Time	10	—	—	ns	—
SD24	tRISE	Clock Rise Time	—	10	—	ns	—
SD25	tFALL	Clock Fall Time	—	10	—	ns	—
SD26	tSETUP	Input Setup Time	5	—	—	ns	—
SD27	tHOLD	Input Hold Time	5	—	—	ns	—

TABLE 44-57: SD HOST CONTROLLER HIGH-SPEED MODE TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SD30	tSDCK	Clock Frequency	—	—	50	MHz	—
SD31	tDUTY	Duty Cycle	—	50	—	%	—
SD32	tHIGH	Clock High Time	7	—	—	ns	—

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AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SD33	tLOW	Clock Low Time	7	—	—	ns	—
SD34	tRISE	Clock Rise Time	—	3	—	ns	—
SD35	tFALL	Clock Fall Time	—	3	—	ns	—
SD36	tSETUP	Input Setup Time	6	—	—	ns	—
SD37	tHOLD	Input Hold Time	2	—	—	ns	—

FIGURE 44-30: EJTAG TIMING CHARACTERISTICS

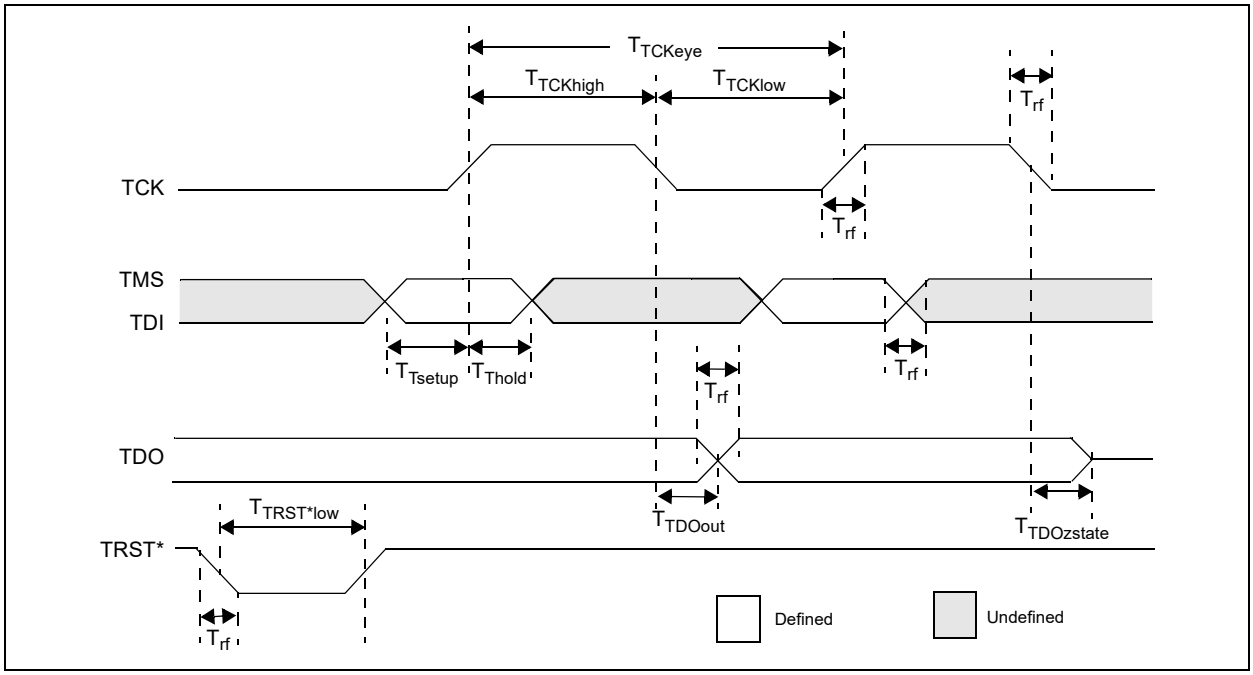

TABLE 44-58: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: V_{DDIO} = 2.2V to 3.6V, V_{DDCORE} = 1.7V to 1.9V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	**Symbol**	**Description(1)**	**Min.**	**Max.**	**Units**	**Conditions**
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	THOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

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45.0 AC AND DC CHARACTERISTICS GRAPHS

Note: The graphs provided are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 45-1: VOH – 4x DRIVER PINS

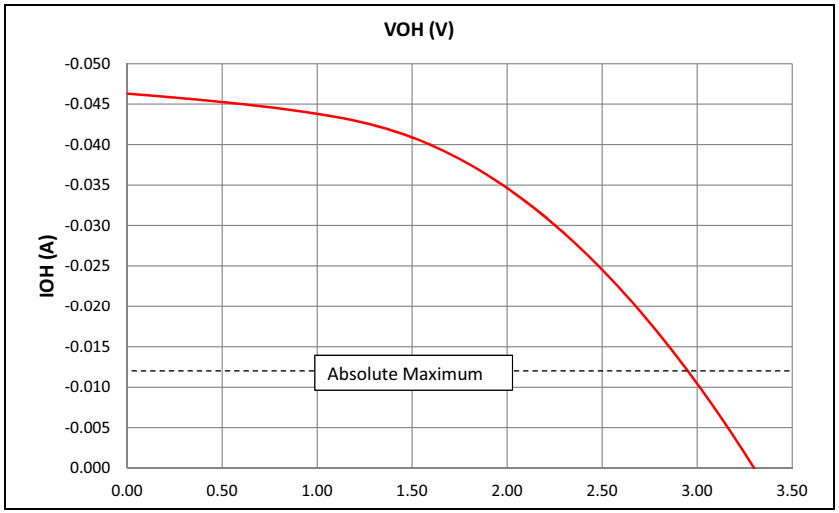

FIGURE 45-2: VOL – 4x DRIVER PINS

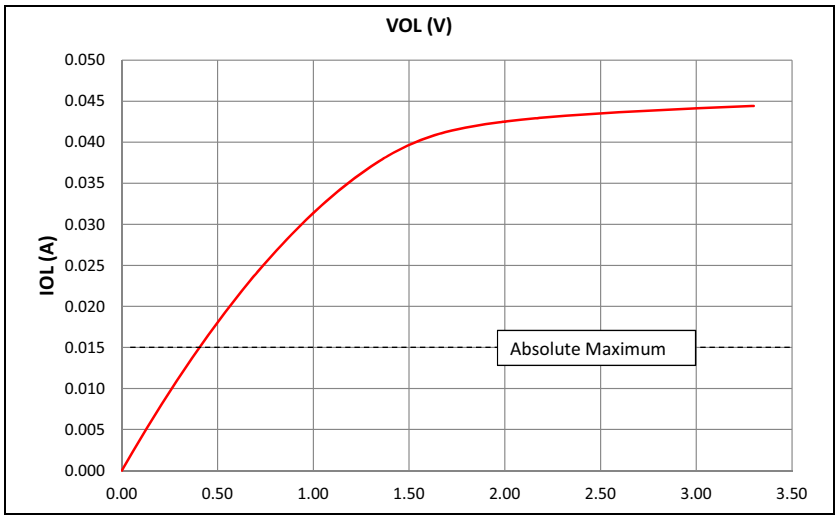

FIGURE 45-3: VOH – 8x DRIVER PINS

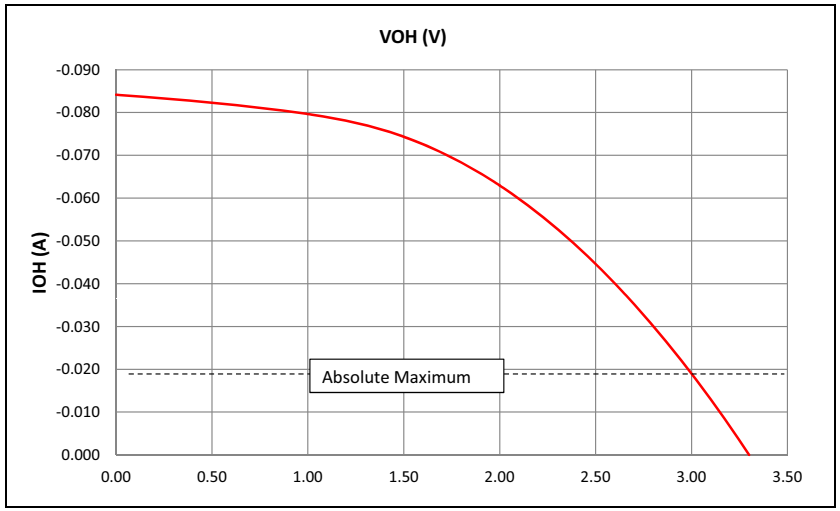

FIGURE 45-4: VOL – 8x DRIVER PINS

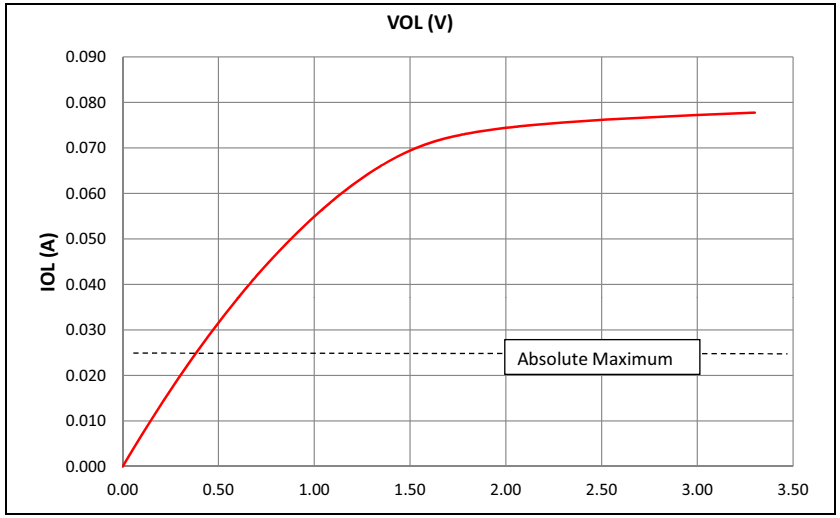

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FIGURE 45-5: VOH – 12x DRIVER PINS

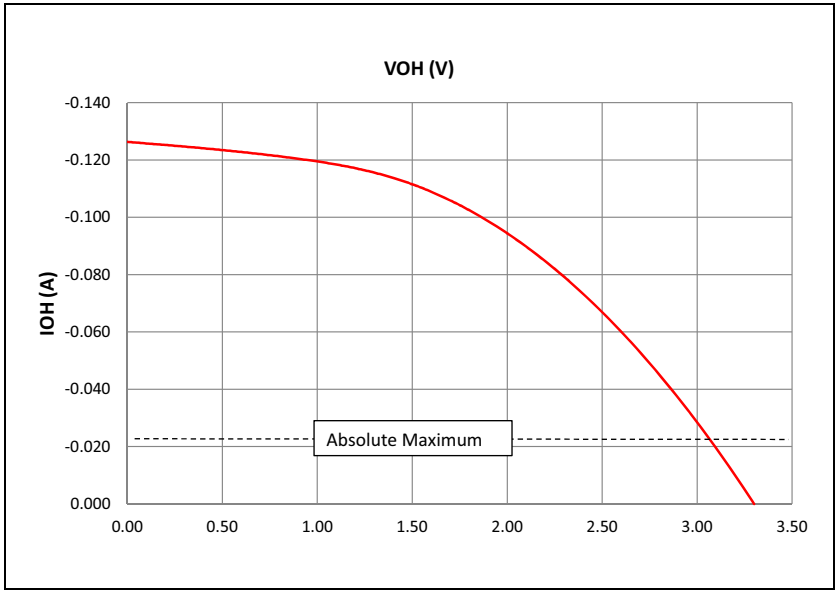


FIGURE 45-6: VOL – 12x DRIVER PINS

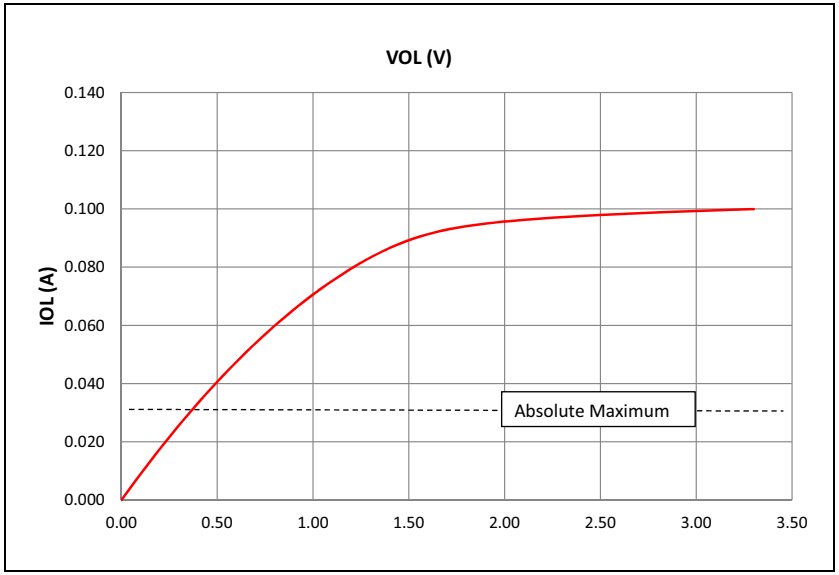
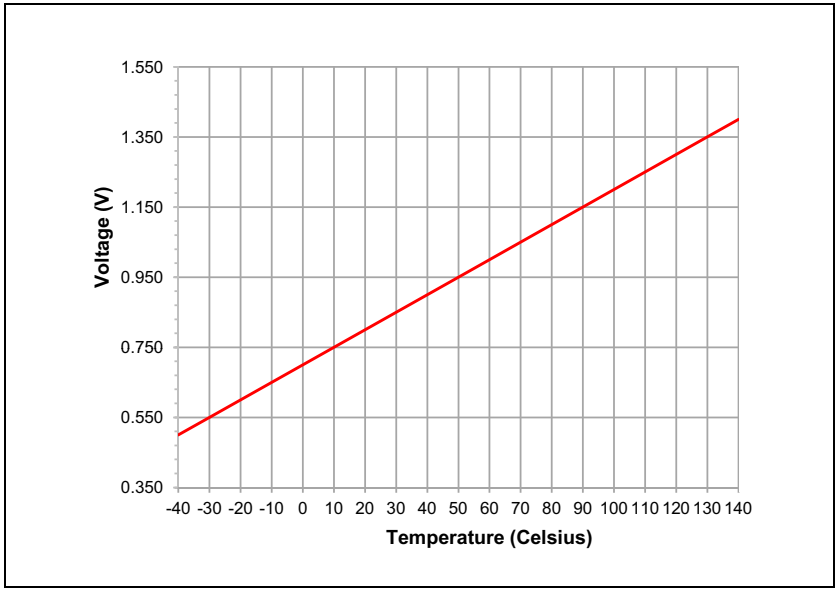


FIGURE 45-7: TYPICAL TEMPERATURE SENSOR VOLTAGE



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46.0 PACKAGING INFORMATION

46.1 Package Marking Information

All devices are marked with Microchip logo and ordering code.
Additional marking is as shown below:

```
*

YYWWNNN
```

Where,

- YY : Manufacturing year (last 2 digits of calender year)
- WW : Manufacturing week (for example, week of January 1 is week 01)
- NNN: Alphanumeric traceability code
- * : Pb-free JEDEC designator for Matte Tin (Sn)

This package is Pb free. The Pb-free JEDEC designator, e3, can be found on this package or outer packaging of this package.

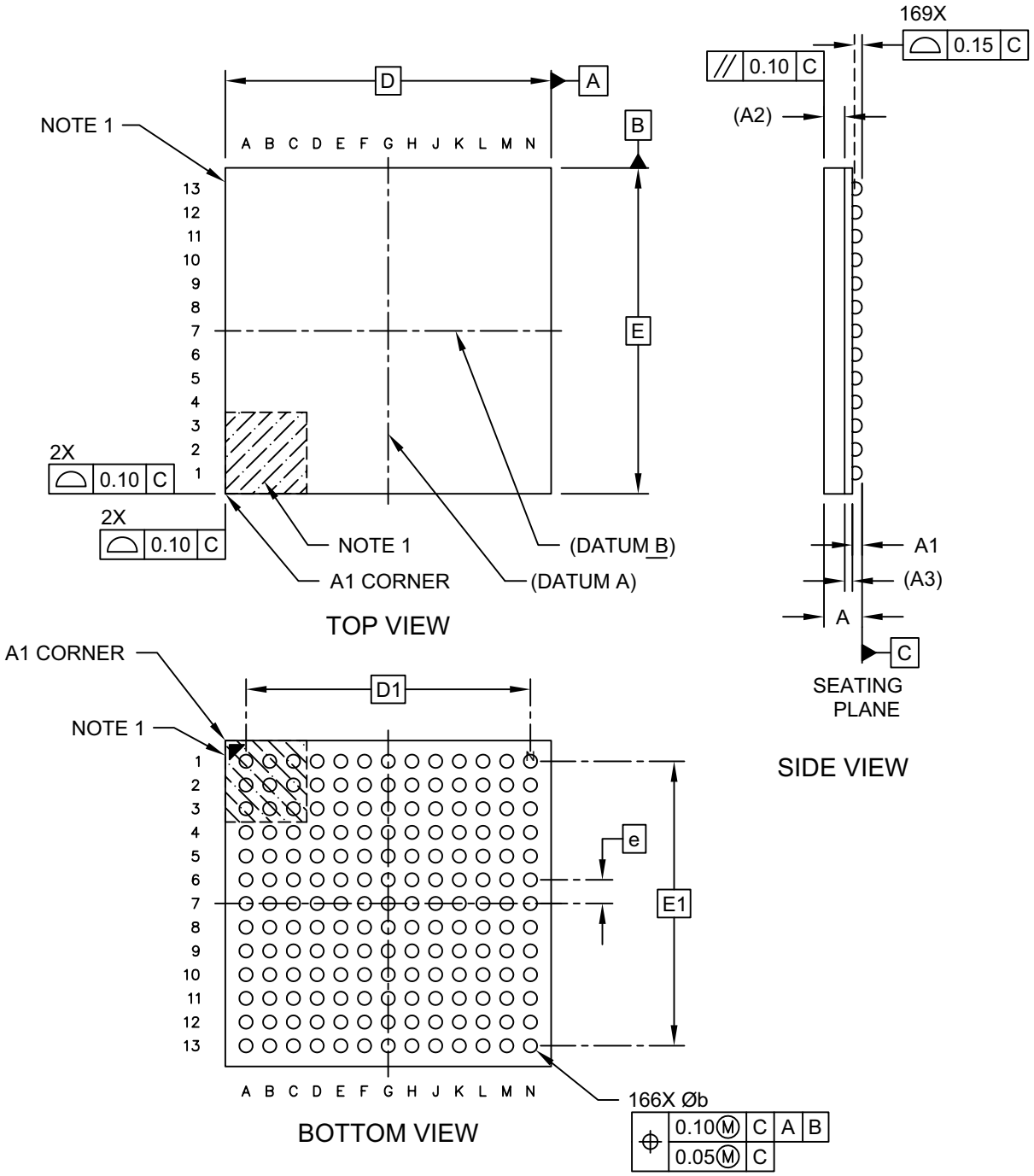
Note: If the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

46.2 Package Details

The following sections provide the technical details of the packages.

169-Ball Low Profile Fine Pitch Ball Grid Array (HF) - 11x11x1.4 mm Body [LFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-365B Sheet 1 of 2

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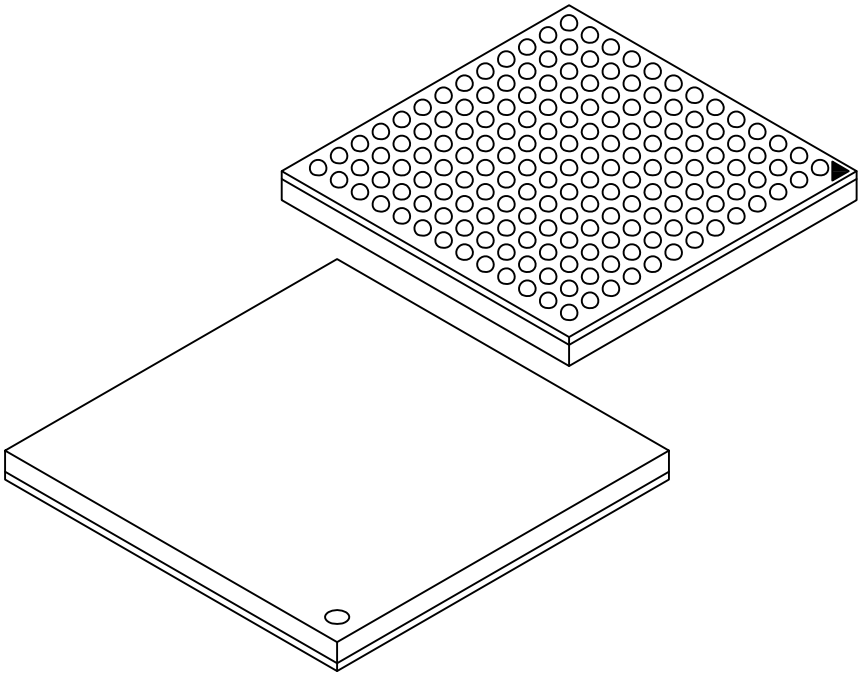
169-Ball Low Profile Fine Pitch Ball Grid Array (HF) - 11x11x1.4 mm Body [LFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals (Balls)	N	169		
Pitch	e	0.80 BSC		
Overall Height	A	1.17	1.285	1.40
Terminal (Ball) Height	A1	0.25	0.325	0.40
Mold Cap Thickness	(A2)	0.70 REF		
Substrate Thickness	(A3)	0.26 REF		
Overall Length	D	11.00 BSC		
Overall Width	E	11.00 BSC		
Overall Ball Pitch	D1	9.60		
Overall Ball Pitch	E1	9.60		
Ball Diameter	b	0.40	0.45	0.50

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

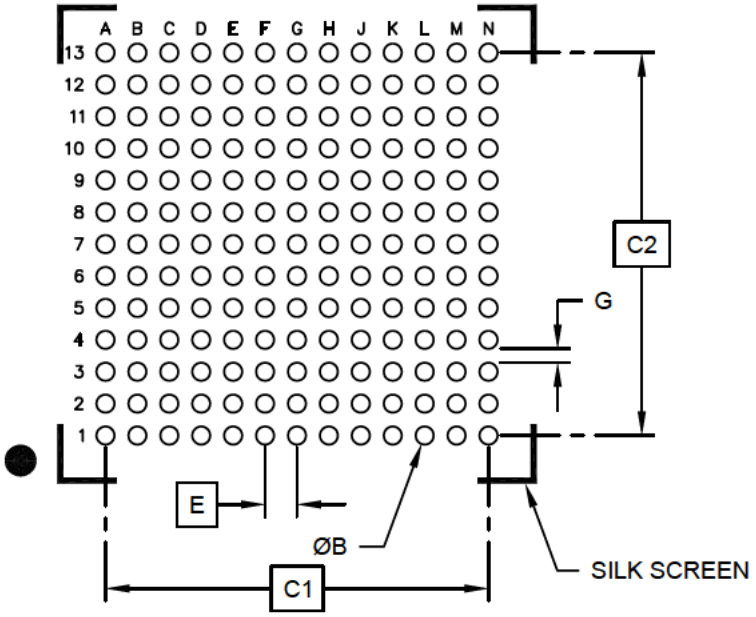
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-365B Sheet 2 of 2

169 Ball Low Profile Fine Pitch Ball Grid Array (HF) - 11x11x1.4 mm Body [LFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1	9.60 BSC		
Contact Pad Spacing	C2	9.60 BSC		
Contact Pad Diameter (X169)	B	0.40	0.45	0.50
Pad-to-Pad Clearance	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2365B

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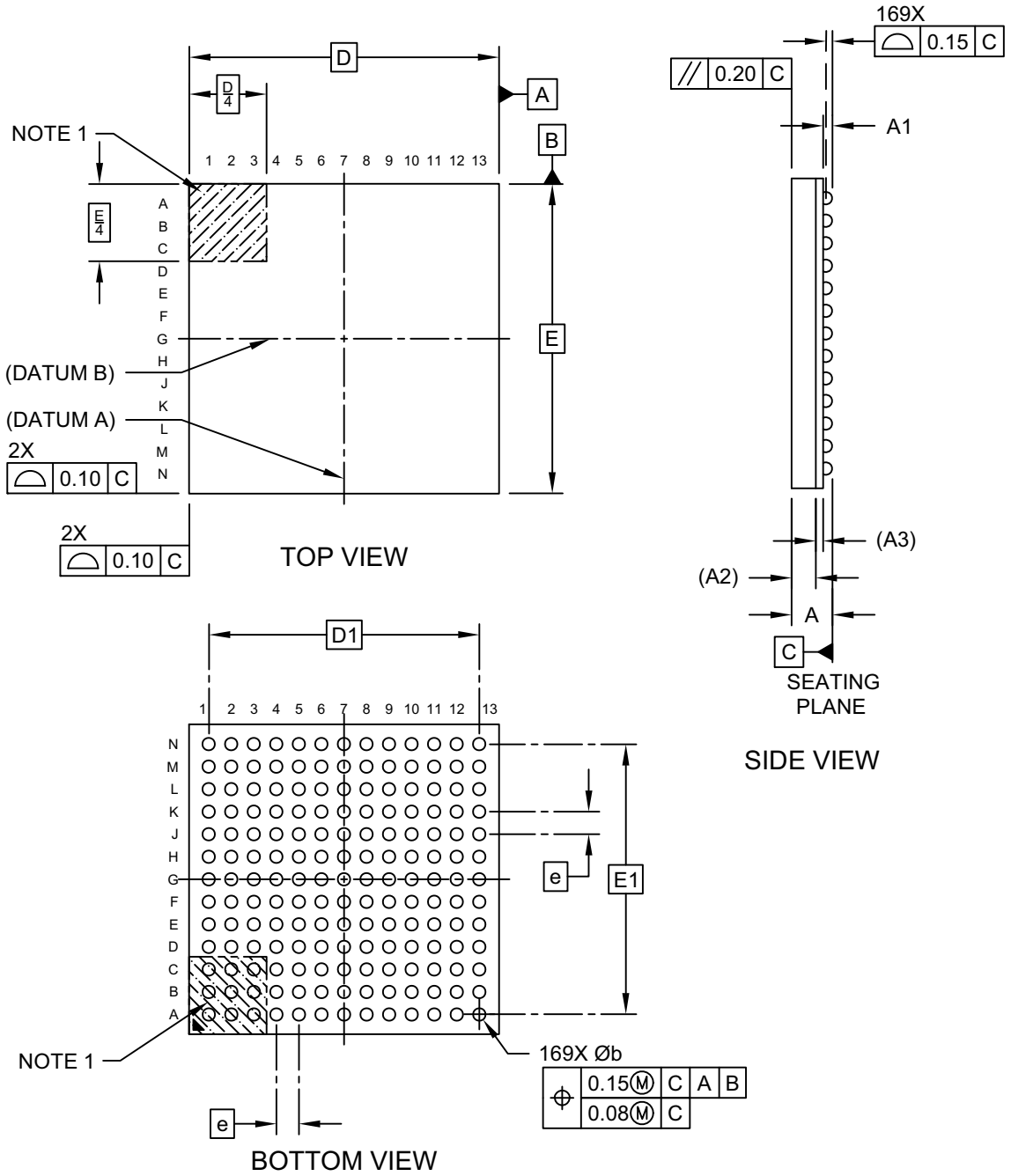
169-Ball Low Profile Ball Grid Array (6J) - 11x11 mm Body [LFBGA]

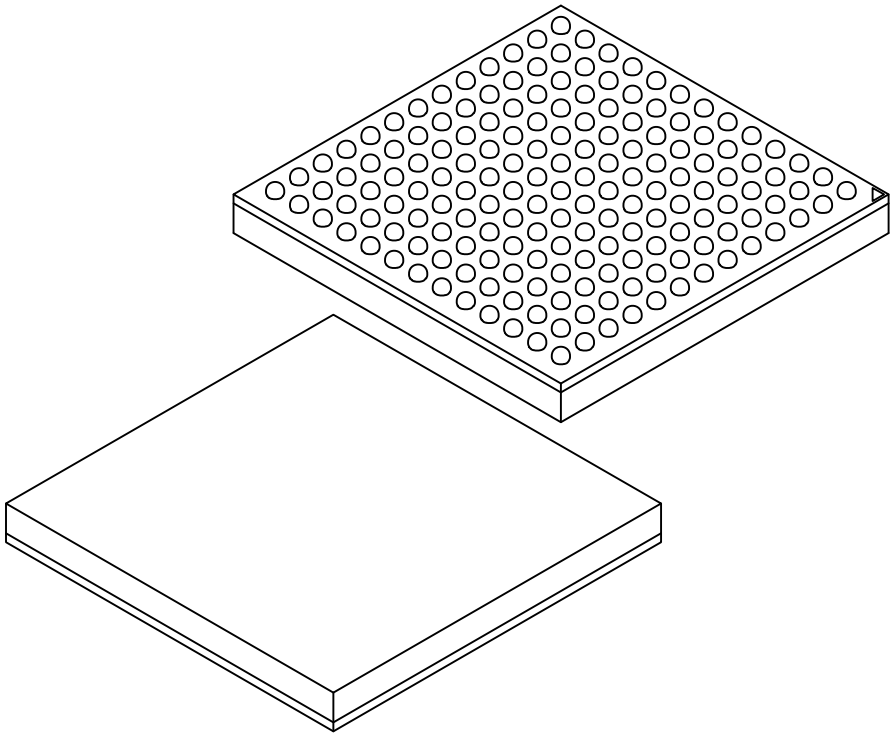
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-439-6J Rev. C Sheet 1 of 2

169-Ball Low Profile Ball Grid Array (6J) - 11x11 mm Body [LFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	169		
Pitch	e	0.80 BSC		
Overall Height	A	1.33	1.445	1.56
Standoff	A1	0.25	-	0.40
Mold Thickness	A2	0.86 REF		
Substrate Thickness	A3	0.26 REF		
Overall Length	D	11.00 BSC		
Overall Terminal Spacing	D1	9.60 BSC		
Overall Width	E	11.00 BSC		
Overall Terminal Spacing	E1	9.60 BSC		
Terminal Diameter	b	0.40	0.45	0.50

Notes:

1. Pin A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-439-6J Rev. C Sheet 2 of 2

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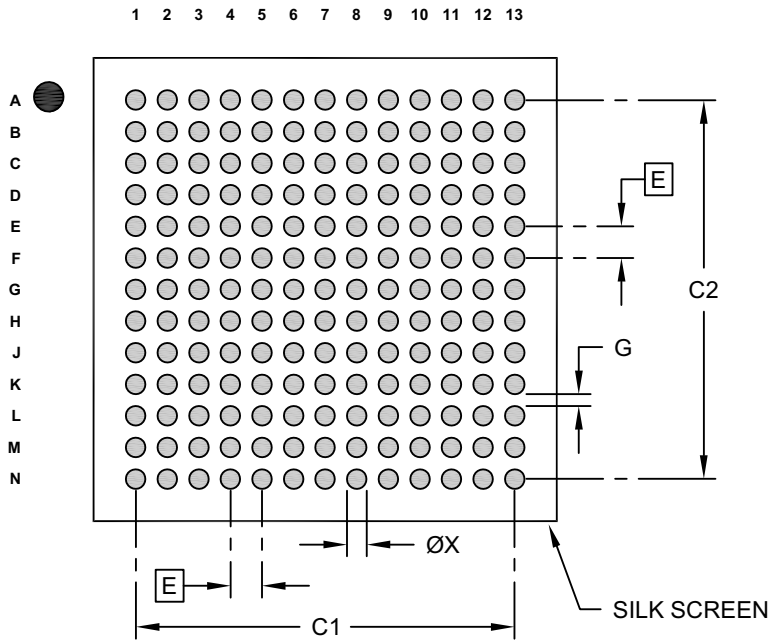
169-Ball Low Profile Ball Grid Array (6J) - 11x11 mm Body [LFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Overall Contact Pad Spacing	C1		9.60	
Overall Contact Pad Spacing	C2		9.60	
Contact Pad Width (X169)	X1			0.50
Contact Pad to Contact Pad	G	0.30		

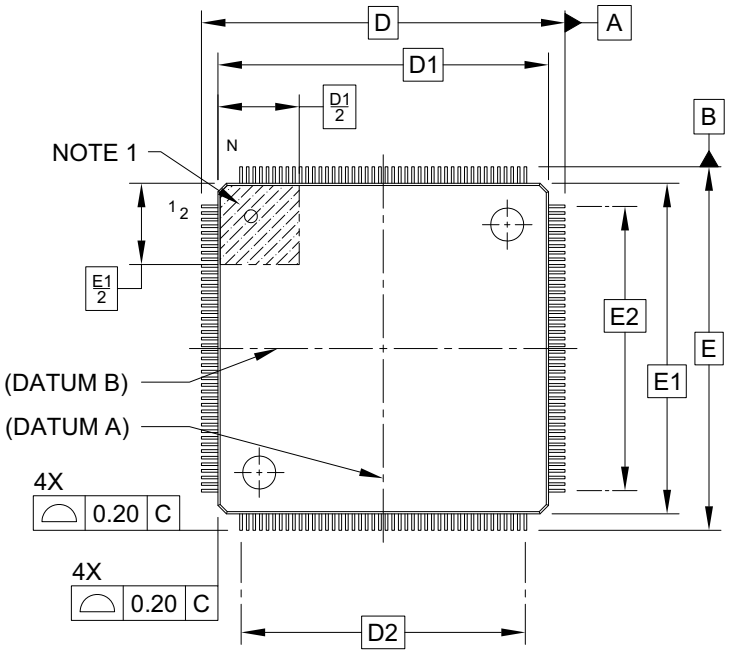
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

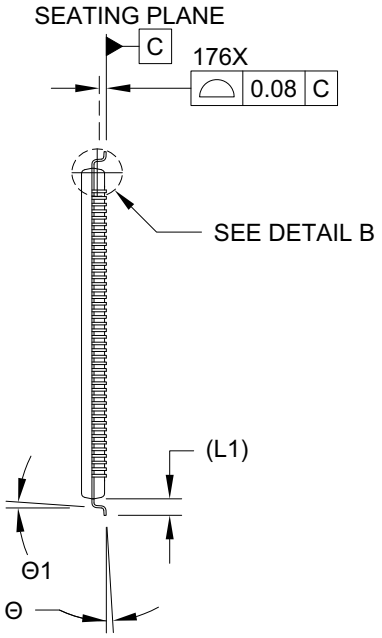
Microchip Technology Drawing C04-2439-6J Rev C

176-Lead Low Profile Quad Flat Pack (2J) - 20x20x1.4 mm Body [LQFP] With 7x7 mm Exposed Pad

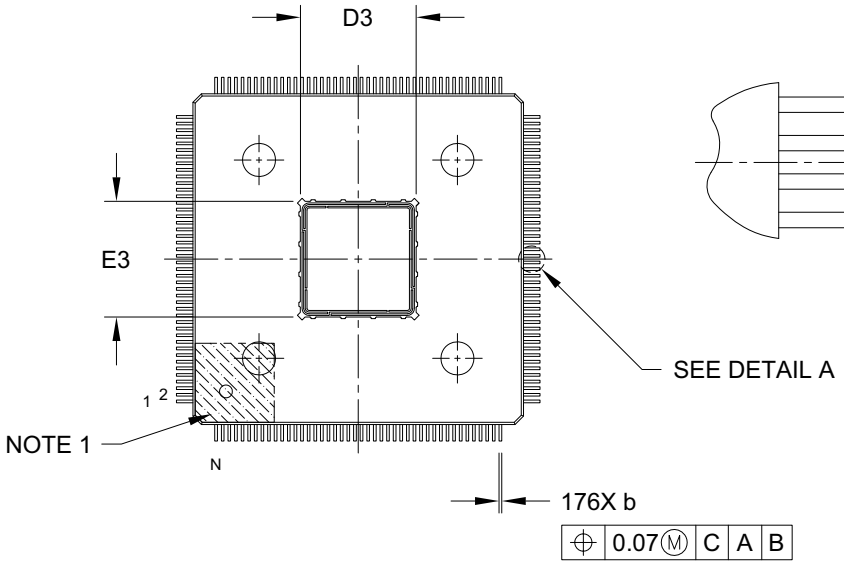
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



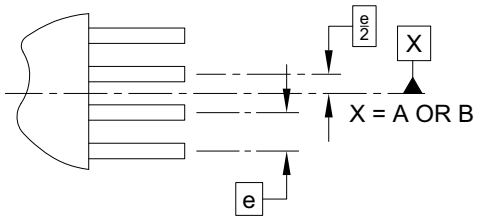
TOP VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL A

Microchip Technology Drawing C04-367A Sheet 1 of 2

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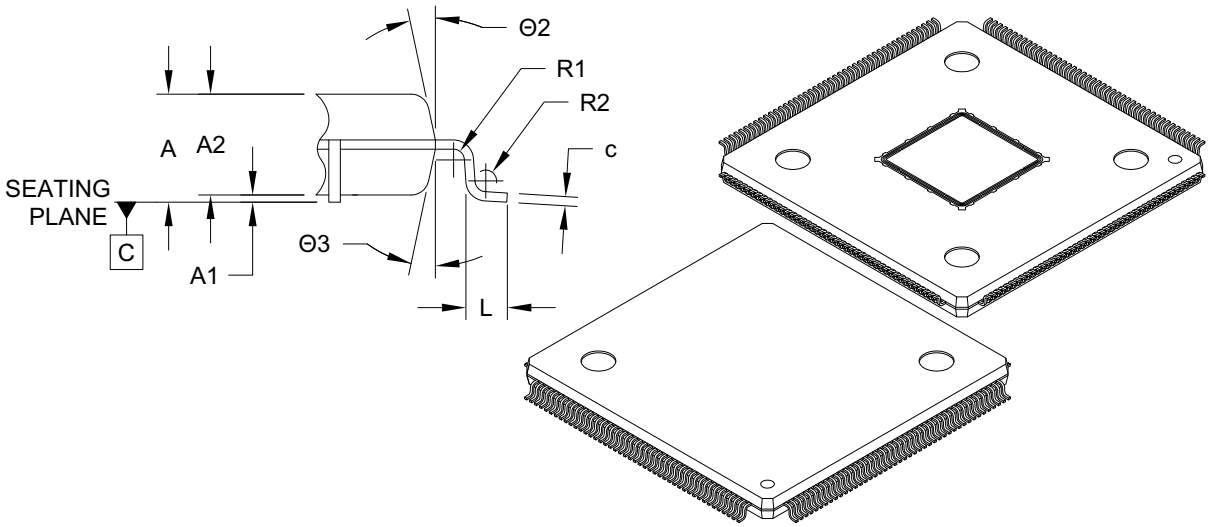
176-Lead Low Profile Quad Flat Pack (2J) - 20x20x1.4 mm Body [LQFP] With 7x7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	176		
Pitch	e	0.40 BSC		
Overall Height	A	-	-	1.60
Standoff	A1	0.05	-	0.15
Molded Package Height	A2	1.35	1.40	1.45
Overall Length	D	22.00 BSC		
Molded Package Length	D1	20.00 BSC		
Overall Lead Pitch	D2	17.20 BSC		
Exposed Pad Length	D3	6.90	7.00	7.10
Overall Width	E	22.00 BSC		
Molded Package Width	E1	20.00 BSC		
Overall Lead Pitch	E2	17.20 BSC		
Exposed Pad Width	E3	6.90	7.00	7.10

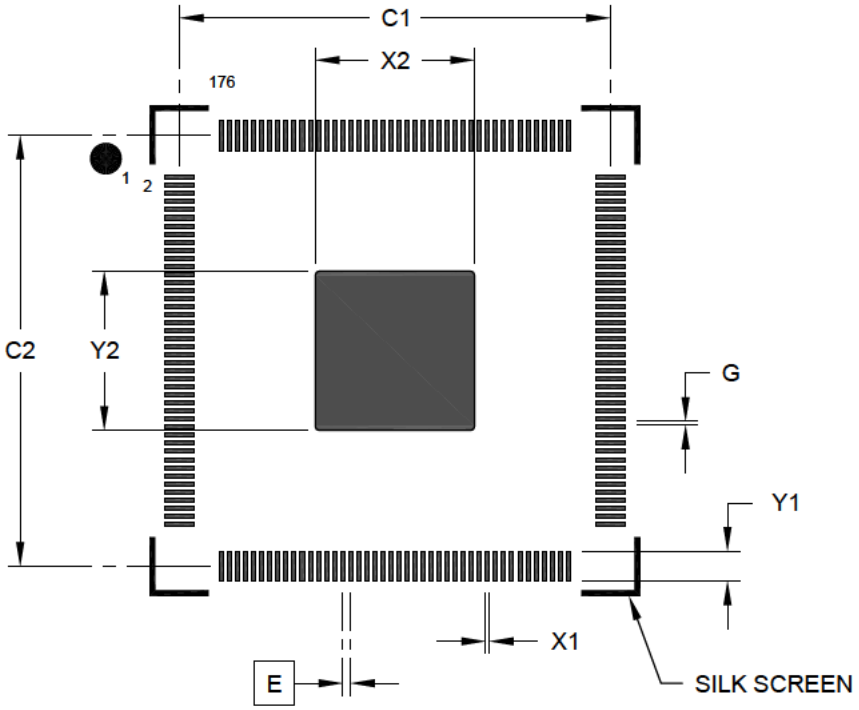
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Lead Width	b	0.13	0.16	0.23
Lead Thickness	c	0.09	-	0.20
Lead Length	L	0.45	0.60	0.75
Footprint	(L1)	1.00 REF		
Bend Radius	R1	0.08	-	-
Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Mold Draft Angle	Θ2	11°	12°	13°
Mold Draft Angle	Θ3	11°	12°	13°

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable Protrusion is 0.25mm per side. D1 and E1 are maximum body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Allowable dam bar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm
   Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and adjacent lead is 0.07mm for 0.40mm pitch packages.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-367A Sheet 2 of 2

176-Lead Low Profile Quad Flat Pack (2J) - 20x20x1.4 mm Body [LQFP] With 7x7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		21.40	
Contact Pad Spacing	C2		21.40	
Contact Pad Width (X176)	X1			0.20
Contact Pad Length (X176)	Y1			1.50
Center Pad Width	X2			7.90
Center Pad Length	Y2			7.90
Contact Pad to Pad (X172)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2367B

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APPENDIX A: MIGRATING FROM PIC32MZ (DAA/DAB/DAG/DAH) FAMILY TO PIC32MZ (DAK/DAL/DAR/DAS) FAMILY

This appendix provides an overview of considerations for migrating from the PIC32MZ (DAA/DAB/DAG/DAH) family of devices to the PIC32MZ (DAK/DAL/DAR/DAS) family of devices. The codes developed for the PIC32MZ (DAA/DAB/DAG/DAH) family of devices can be ported to the PIC32MZ (DAK/DAL/DAR/DAS) family of devices after making the appropriate changes outlined in the Table 46-1:Migration Features.

The PIC32MZ (DAK/DAL/DAR/DAS) family of devices are based on the same architecture, and contain feature improvements over the PIC32MZ (DAA/DAB/DAG/DAH) family of devices.

Note: In the table below, the peripheral differences are indicated in **Bold** type, and these peripheral differences will affect software and hardware migration.

TABLE 46-1: MIGRATION FEATURES

PIC32MZ DAA/DAB/DAG/DAH Features (As documented in the data sheet, *DS60001361*)	**PIC32MZ DAK/DAL/DAR/DAS Features** (As documented in the data sheet, *DS60001565*)
Configuration Word DEVCFG2	
VBATBOREN<1> bit (DEVCFG2<19>) enables BOR during VBAT mode. bit 19 **VBATBOREN: VBAT BOR Enable bit** **1 = Enable BOR during VBAT mode** **0 = Disable BOR during VBAT mode**	Bit (DEVCFG2<19>) **is 'Reserved' and should be written '1'.**
Package Option	
LFBGA 288 pin package option **available.**	LFBGA 288 pin package option **not available.**
Analog-to-Digital Converter (ADC)	
Default value for Analog input Charge Pump Enable Bit AICPMPEN (ADCCON1<12>) is '1'. This bit should not be set if VDDIO is greater than 2.5V.	**Default value for Analog input Charge Pump Enable Bit AICPMPEN (ADCCON1<12>) is '0'**. This bit should not be set if VDDIO is greater than 2.5V.
SQI	
Supports SQI serial clock frequency (Param. No. SQI10) in DMA Read mode, SDR mode up to **80 MHz** and in PIO Write mode, SDR mode up to **100 MHz.**	Supports SQI serial clock frequency (Param. No. SQI10) in DMA Read mode, SDR mode up to **73 MHz** and in PIO Write mode, SDR mode up to **76 MHz.**
Comparator	
Common Mode Rejection Ratio (Param. No. D302) minimum value is **50 dB** over VICM range (Param. No. D301) of 0.8 V to **2.37V.**	Common Mode Rejection Ratio (Param. No. D302a) minimum value is **45 dB** over VICM range (Param. No. D301) of 0.8 V to **2.7V.**
Internal Fast RC (FRC) Oscillator	
FRC Oscillator Tuning bits TUN<5:0> (OSCTUN<5:0>) range is **+/-4%.**	FRC Oscillator Tuning bits TUN<5:0> (OSCTUN<5:0>) range is **+/-2%.**
OPERATING CURRENT	
Operating currents are given in Table 44-7: DC CHARACTERISTICS: OPERATING CURRENT in the data sheet.	Some operating currents are different. Check Table 44-7: DC CHARACTERISTICS: OPERATING CURRENT in the data sheet.

NOTES:

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APPENDIX B: REVISION HISTORY

Revision A (03/2019)

This is the initial released version of this document.

Revision B (08/2019)

The following updates were made during this release.

Section Name or Type	Update Description
Appendix B: "Revision History"	Moved to Appendix B
Appendix A: "Migrating From PIC32MZ (DAA/DAB/DAG/DAH) Family to PIC32MZ (DAK/DAL/DAR/DAS) Family"	Added new Appendix, Migrating From PIC32MZ (DAA/DAB/DAG/DAH) Family to PIC32MZ (DAK/DAL/DAR/DAS) Family

Revision C (09/2020)

The following updates were made during this release.

Section Name or Type	Update Description
"32-bit Graphics Applications MCUs (up to 2 MB Live Update Flash, 640 KB SRAM, and 32 MB DDR2 SDRAM) with XLP Technology"	• Added new temperature range for 105°C • Updated **TABLE 4:Pin Names for 169-pin Devices** and **TABLE 5:Pin Names for 176-pin Devices**with a new note
36.0 "Graphics LCD (GLCD) Controller"	Added **Table 36-1:RGB Color Mapping**.
39.0 "Secure Digital Host Controller (SDHC)"	• Updated **Register 39-1:SDHCBLKCON: SDHC Block Control Register** with (BF8E_#) • Updated **Register 39-13:SDHCCAP: SDHC Capabilities Register** with two new bitfields SLOTTYPE and ASYNCINT
41.0 "Special Features"	Added a new note to INTVREFCON bit for **Register 41-14:CFGMPLL: Memory PLL Configuration Register**.
44.0 "Electrical Characteristics"	• Updated all tables with the Addition of the V-temp range • Added V-temp ratings to **Table 44-2:Thermal Operating Conditions** • Added a note 3 to **Table 44-4:DC Temperature and Voltage Specifications** • Added V-temp ratings to **Table 44-9:DC Characteristics: Power-Down Current (Ipd)** • Updated note 4 with new verbiage for **Table 44-14:DC Characteristics: Program Memory(3)**
"Product Identification System"	Updated the temperature range to include V-temp.

Revision D (06/2021)

The following updates were made during this release.

The I^2C, SPI, and I^2S standards use the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client" respectively.

Section Name or Type	Update Description
General	• Throughout the document, References to both “Master” and “Slave” were revised to read “Host” and “Client” where applicable
2.0 “Guidelines for Getting Started with 32-bit Microcontrollers”	• Updated **2.9.2 “5V Tolerant Input Pins”**, corrected VDD to VDDIO, and updated VDDIO specifications in the text
8.0 “Oscillator Configuration”	• Removed erroneous information within parenthesis on Note 6 for **Table 8-1: “System and Peripheral clock Distribution”** • Updated **Register 8-4: “REFOxCON: Reference Oscillator Control Register (‘x’ = 1-5)”** to properly display x=1-5, and added Note 4
17.0 “Deadman Timer (DMT)”	• Updated the Note for **Register 17-1: “DMTCON: Deadman Timer Control Register”**
21.0 “Serial Peripheral Interface (SPI) and Inter-IC Sound (I^2S)”	• Updated **FIGURE 21-1: “SPI/I^2S Module Block Diagram”** to read “SPI Select” instead of “Slave Select”
25.0 “Parallel HOST Port (PMP)”	• Added a new note to the IRQM bit of **Register 25-2: “PMMODE: Parallel Port Mode Register”** • Added a new note to the IBOV bit of **Register 25-7: “PMSTAT: Parallel Port Status Register (client modes only)”**
35.0 “Charge Time Measurement Unit (CTMU)”	• Added AN5 to AN39 to the first bulleted item on page 585
36.0 “Graphics LCD (GLCD) Controller”	• Corrected typographical errors in bitfield 5-0 for **Register 36-2: “GLCDCLKCON: Graphics LCD Controller Clock Control Register”**
38.0 “DDR2 SDRAM Controller”	• Added a note to the bit 28 of **Register 38-24: “DDRSCLSTART: DDL SELF CALIBRATION LOGIC START REGISTER”** • Corrected a typographical error is the DLYSTVAL bitfield of **Register 38-29: “DDRPHYDLLR: DDR PHY DLL Recalibrate Register”**
40.0 “Power-Saving Features”	• Updated **FIGURE 40-1: “XLP Device Block Diagram”** to properly display VDDCORE • A new note was added to **40.4 “Peripheral Module Disable”**
41.0 “Special Features”	• Added a new note to the FDMTEN bitfield for **Register 41-4: “DEVCFG1/ADEVCFG1: Device Configuration Word 1”** • Corrected typographical errors in **41.4 “On-Chip Voltage Regulator”**

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Section Name or Type	Update Description
44.0 "Electrical Characteristics"	• Updated **Table 44-23:System Timing Requirements** with new conditions for the Reference Clock frequency • Updated **Table 44-25:MPLL Clock Timing Requirements** with a new maximum value for the MP12 Parameter • Updated the characteristics for **Table 44-54:GLCD Controller Timing Specifications** with the addition of GLCD pin verbiage • Updated **Table 44-55:DDR2 SDRAM Timing Specifications** with a correction to note 5
46.0 "Packaging Information"	• Updated the Descriptions for the 169-Ball Low Profile Ball Grid Array
"Product Identification System"	• Updated the Package description for the 169 Lead LFBGA

NOTES:

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PIC32 MZ XX XX DA K XXX T - I / BG - XXX

- **Microchip Brand** — PIC32
- **Architecture** — MZ
- **Flash Memory Size** — XX
- **RAM Size** — XX
- **Family** — DA
- **Key Feature Set** — K
- **Pin Count** — XXX
- **Tape and Reel Flag (if applicable)** — T
- **Temperature Range** — I
- **Package** — BG
- **Pattern** — XXX

Example:

PIC32MZ0512DAK176-I/2J: Graphics MCU Family, PIC32, MIPS32® microAptiv™ MPU core, 512 KB program memory, 176-pin, Industrial temperature, LQFP package.

Flash Memory Family

Architecture	MZ	= MIPS32® microAptiv™ MPU Core
Flash Memory Size	10	= 1024 KB
	20	= 2048 KB
RAM Size	25	= 256 KB
	64	= 640 KB
Family	DA	= Graphics MCU Family
Key Feature	K	= PIC32 DA Family Features, no Crypto, no DDR memory
	L	= PIC32 DA Family Features, with Crypto, no DDR memory
	R	= PIC32 DA Family Features, no Crypto, with DDR memory
	S	= PIC32 DA Family Features, with Crypto, with DDR memory
Pin Count	169	= 169-pin
	176	= 176-pin
Temperature Range	I	= -40°C to +85°C (Industrial)
	V	= -40°C to +105°C (V-temp)
Package	HF	= 169-Lead (11x11x1.4 mm) LFBGA (Low Profile Fine Pitch Ball Grid Array)
	6J	= 169-Lead (11x11x1.56 mm) LFBGA (Low Profile Fine Pitch Ball Grid Array)
	2J	= 176-Lead (22x22x1.4 mm) LQFP (Low Profile Quad Flat Pack)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)	
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